CMOS 324 GHz Signal Generation Based on Linear Superposition Technique

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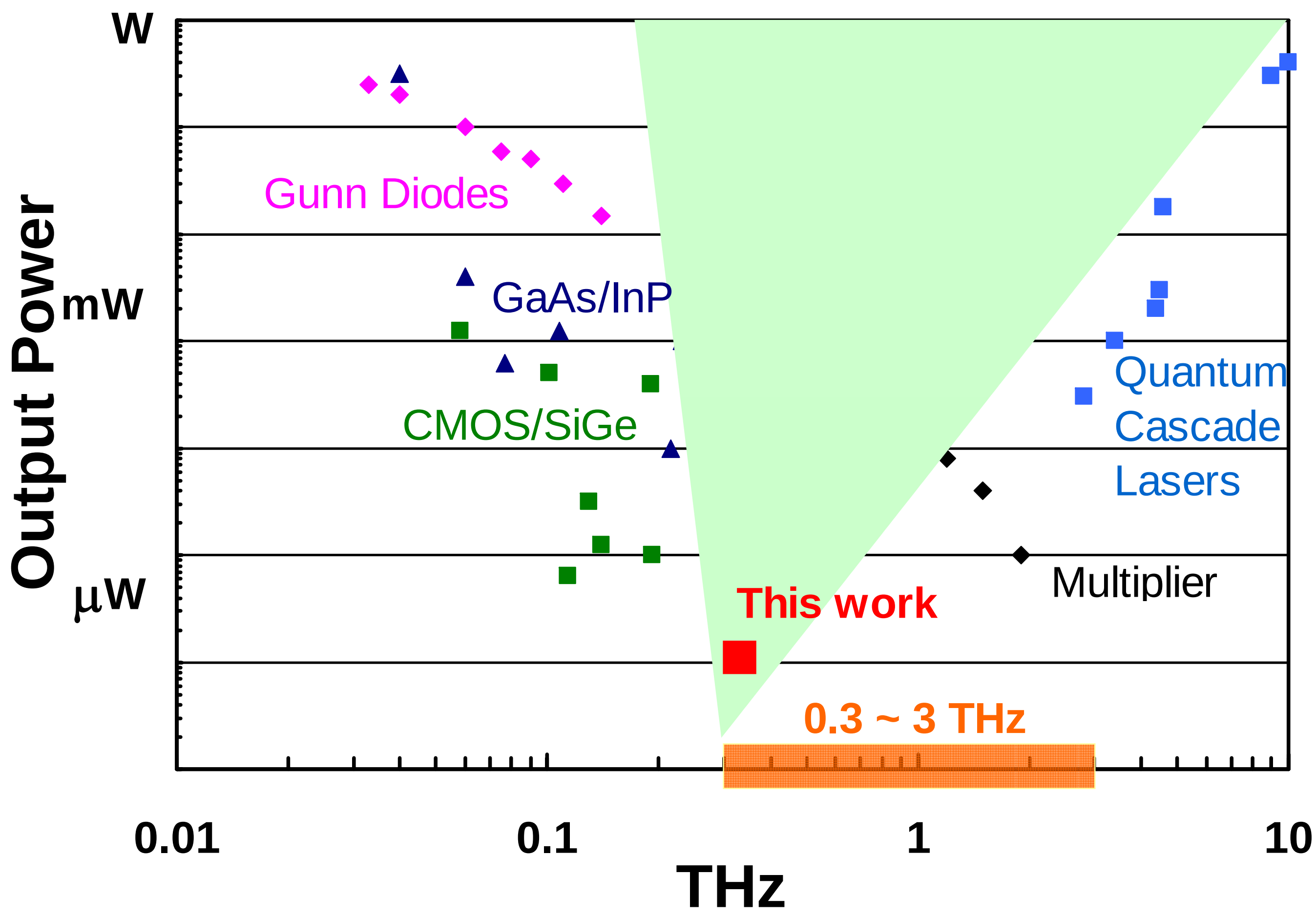
Outline

- Terahertz technology gap and potential system applications
- Linear superposition signal generation technique
- CMOS THz circuit implementation
- Measurement results
- Conclusions

The Terahertz “GAP”

- Lack of compact and portable solid-state THz (0.3-3THz) sources



Potential THz System Applications

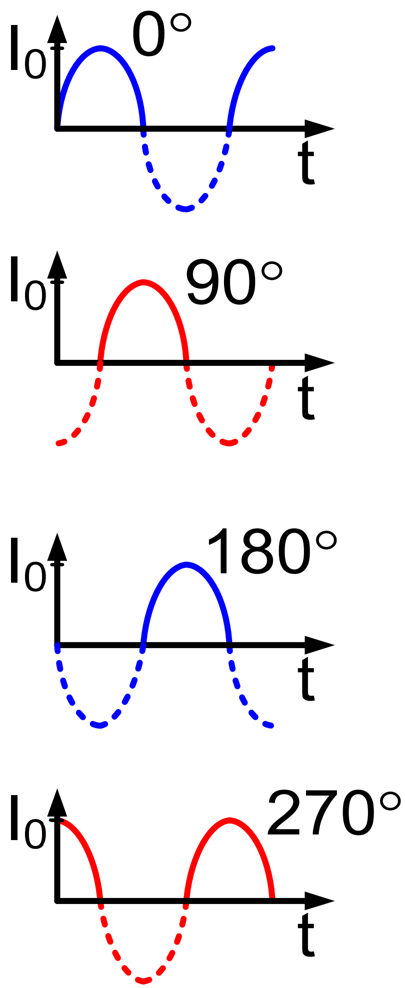
- **Imaging through fog and for concealed objects**
- **Ultra-Short Distance and Ultra-Wideband Communications**
  - 100’s Gigabit/sec RF-Interconnects for **chip-to-chip**, **core-to-core** (CMP), **layer-to-layer** (3D-IC), and **board-to-board** applications
  - 10’s Gigabit/sec data links within 1-10meter range
  - Automotive/Aviation Wireless Harness
  - Space-borne communications

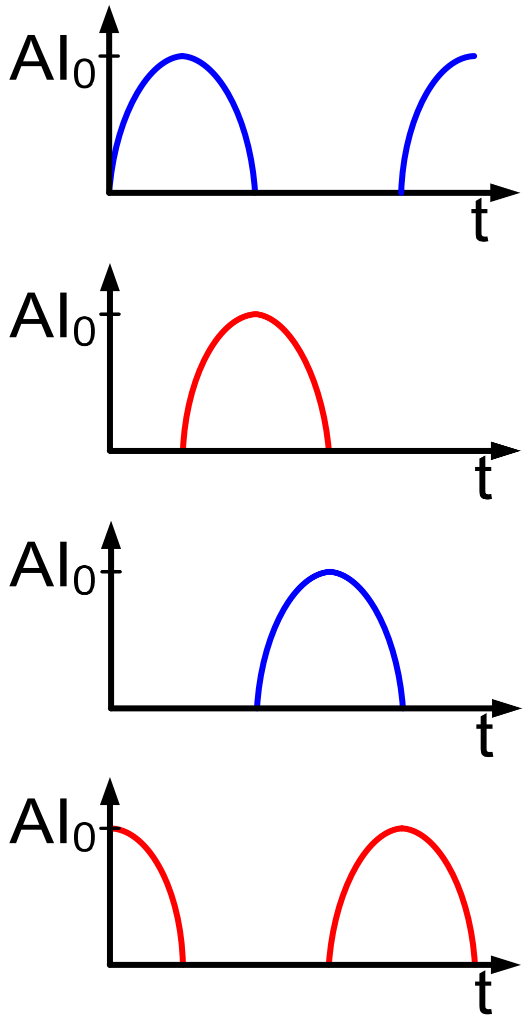
Linear Superposition (LS) Technique

- Generate ***N*** phase-shifted fundamental signals (ω_0) by **2π/*N* in sequence**
- Rectify resultant ***N*** phase-shifted fundamental signals
- Add ***N*** rectified fundamental signal currents to produce a superimposed output at the frequency of $\boldsymbol{N\omega_0}$

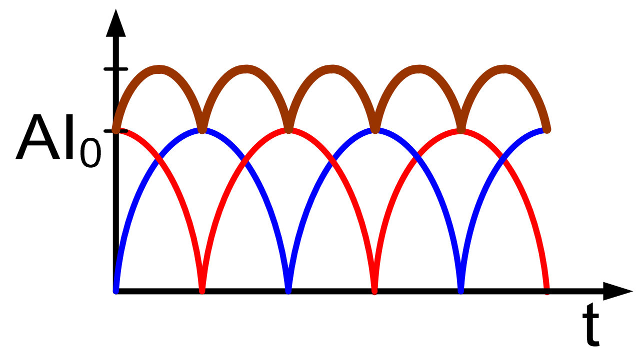
LS Application for *N=4*

Phase shifting → **Rectification** → **Linear superposition**





$$I_C = I_{C0} - \frac{8}{15\pi} AI_0 \cos(4\omega_0 t)$$



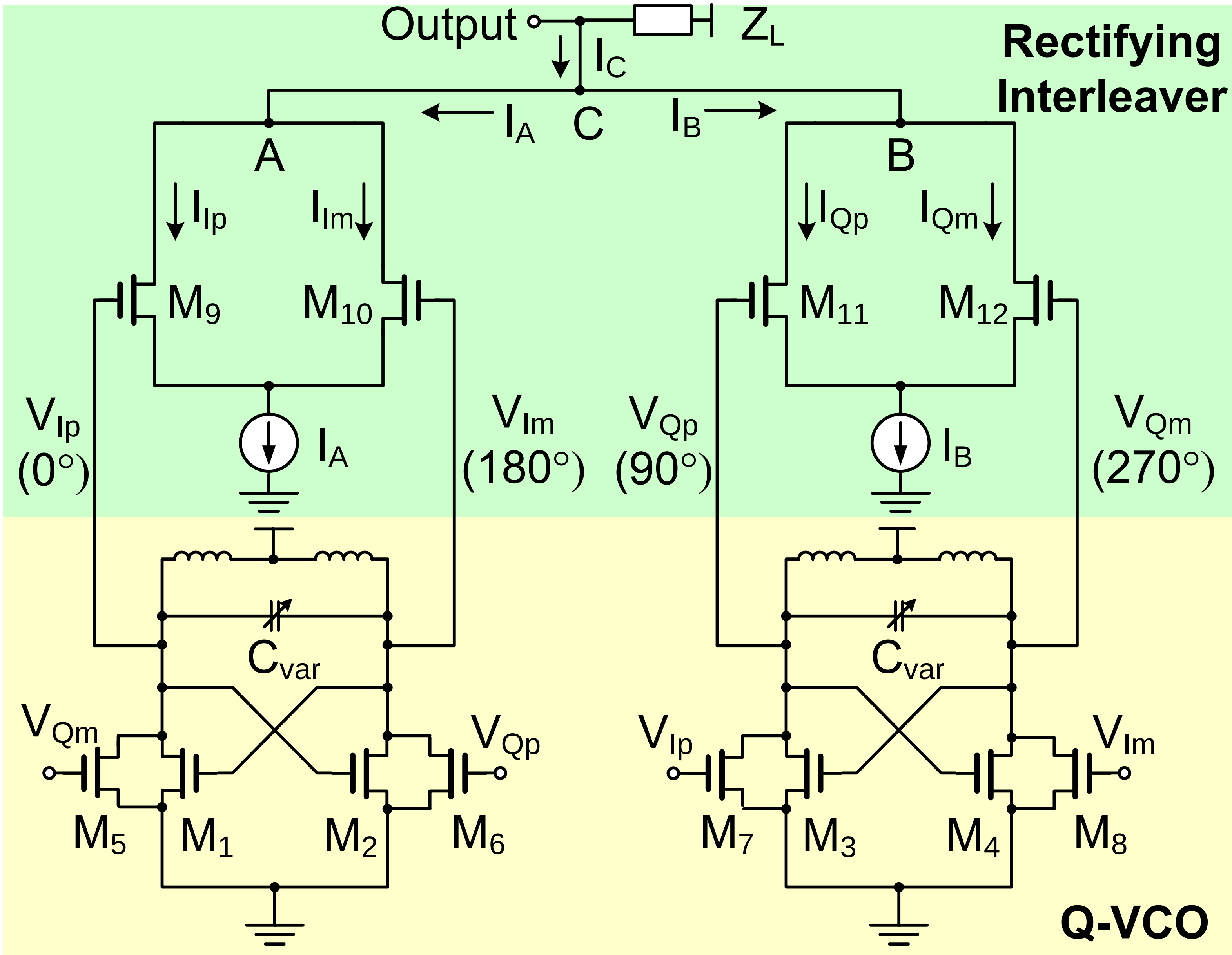
Conversion efficiency

$$\eta = \frac{8}{15\pi} \approx 17\%$$

LS Technique Advantages

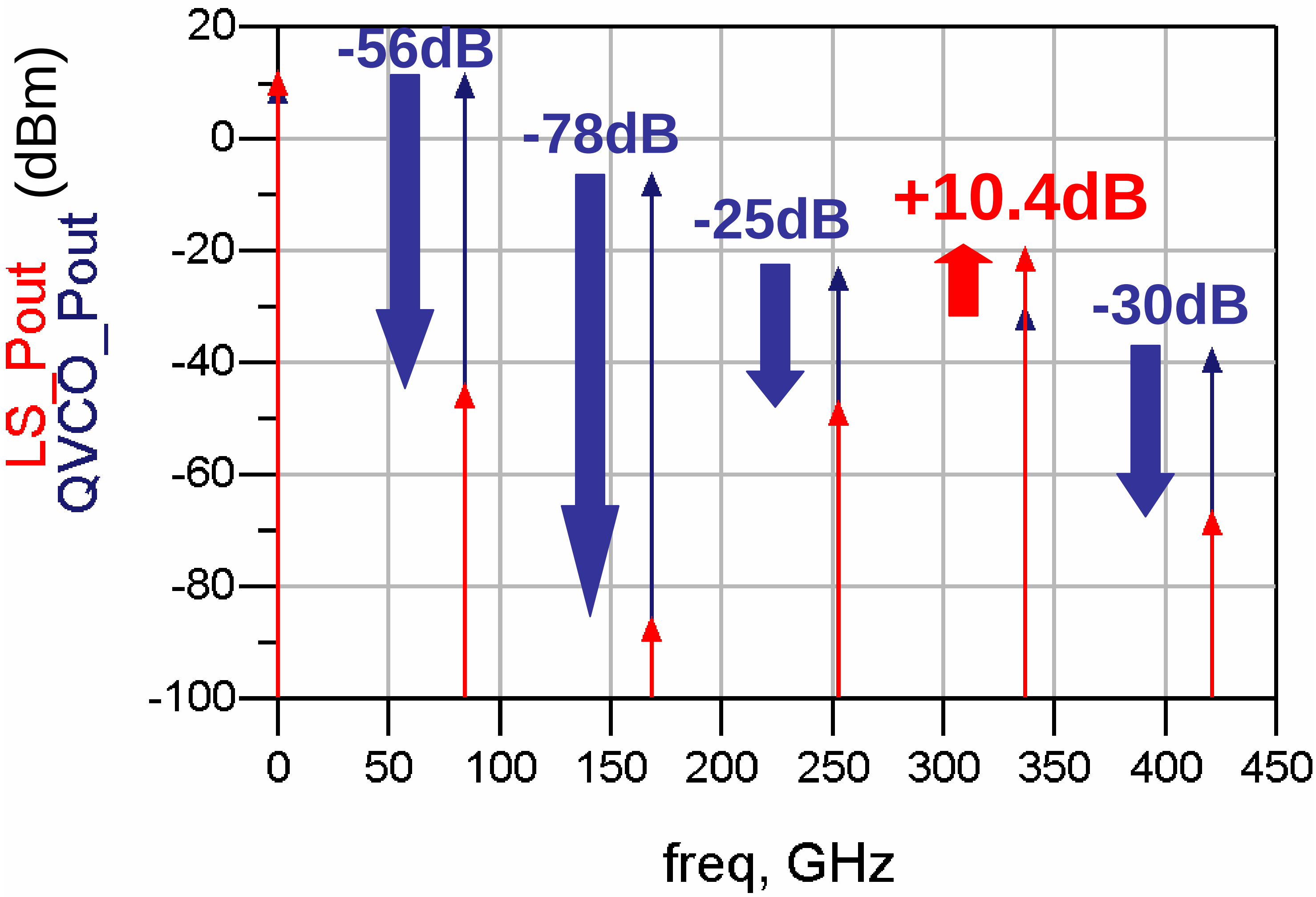
- ❑ Generate oscillation signal at **frequencies much higher** than device f_{max} ($N\omega_{\mathbf{0}}$)
- ❑ Significantly **higher conversion efficiency** ($8/15\pi$ or 17% for $N=4$) than that of nonlinear harmonic generation methods
- ❑ Lower harmonics naturally suppressed and **no need for additional filtering**
- ❑ Possibly phase-locked to $1/N$ of the generated THz frequency

LS Implementation in CMOS

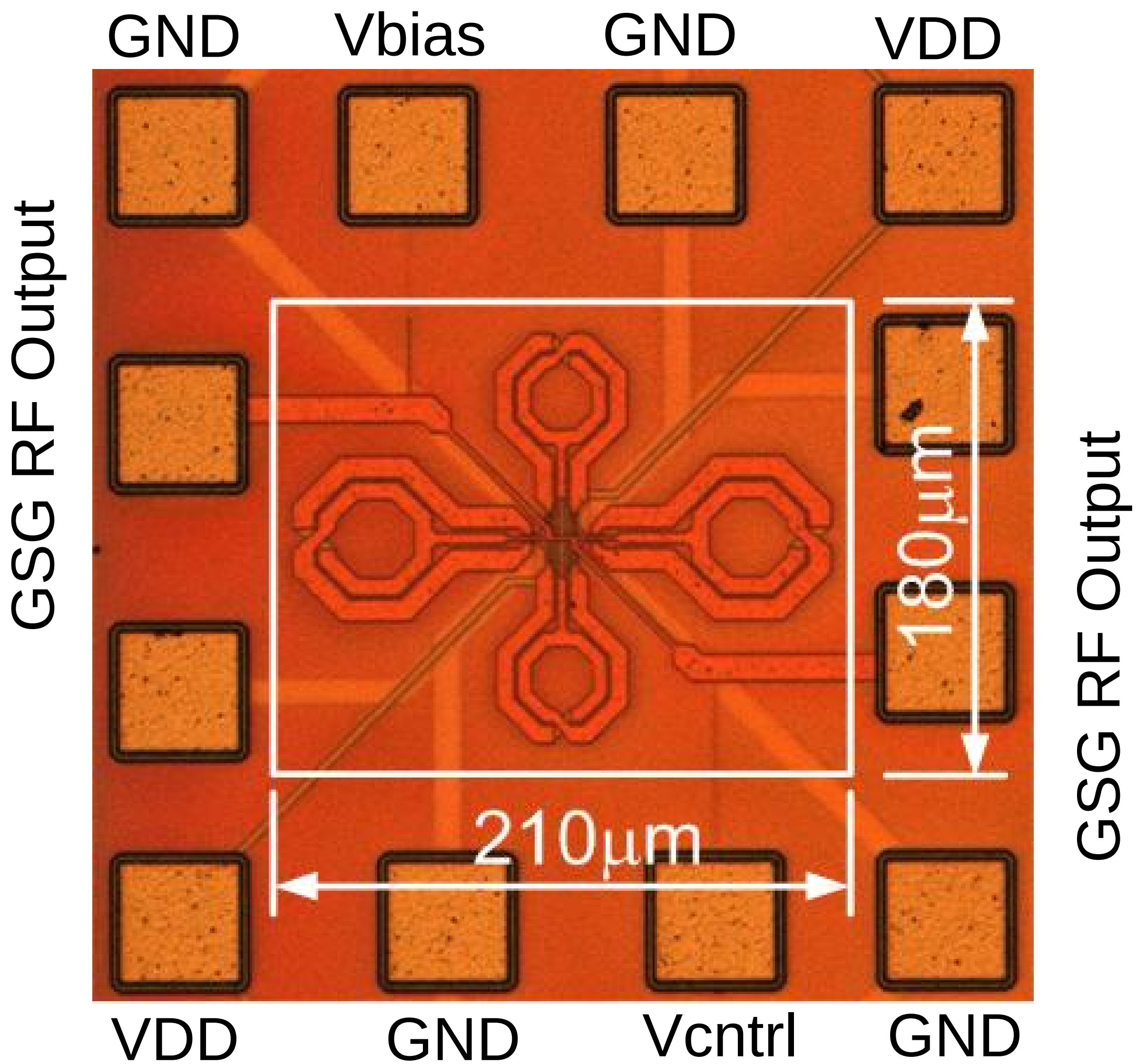


Simulated Output Power

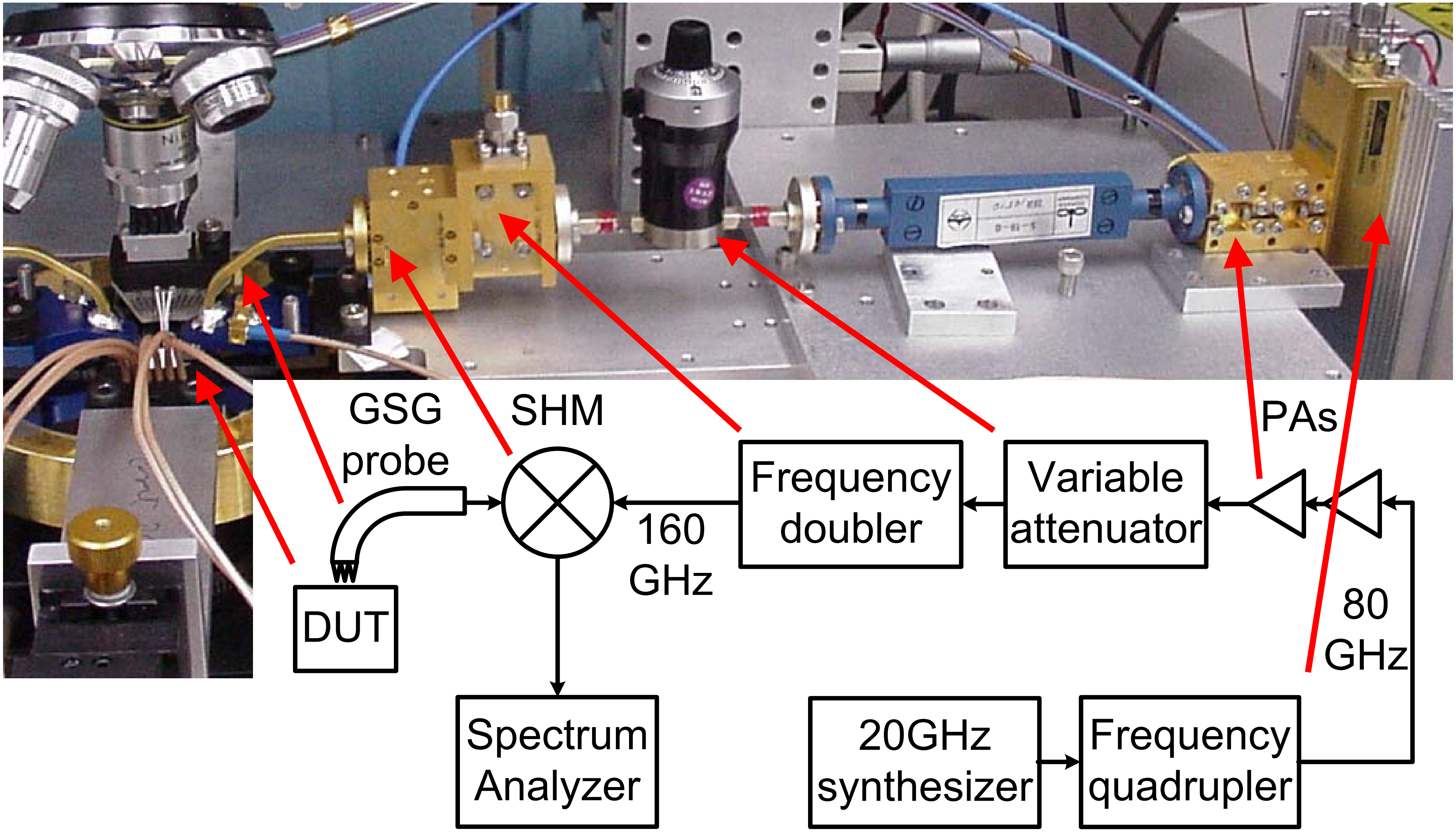
- ❑ Suppressing lower harmonics
- ❑ Boosting 4th harmonic



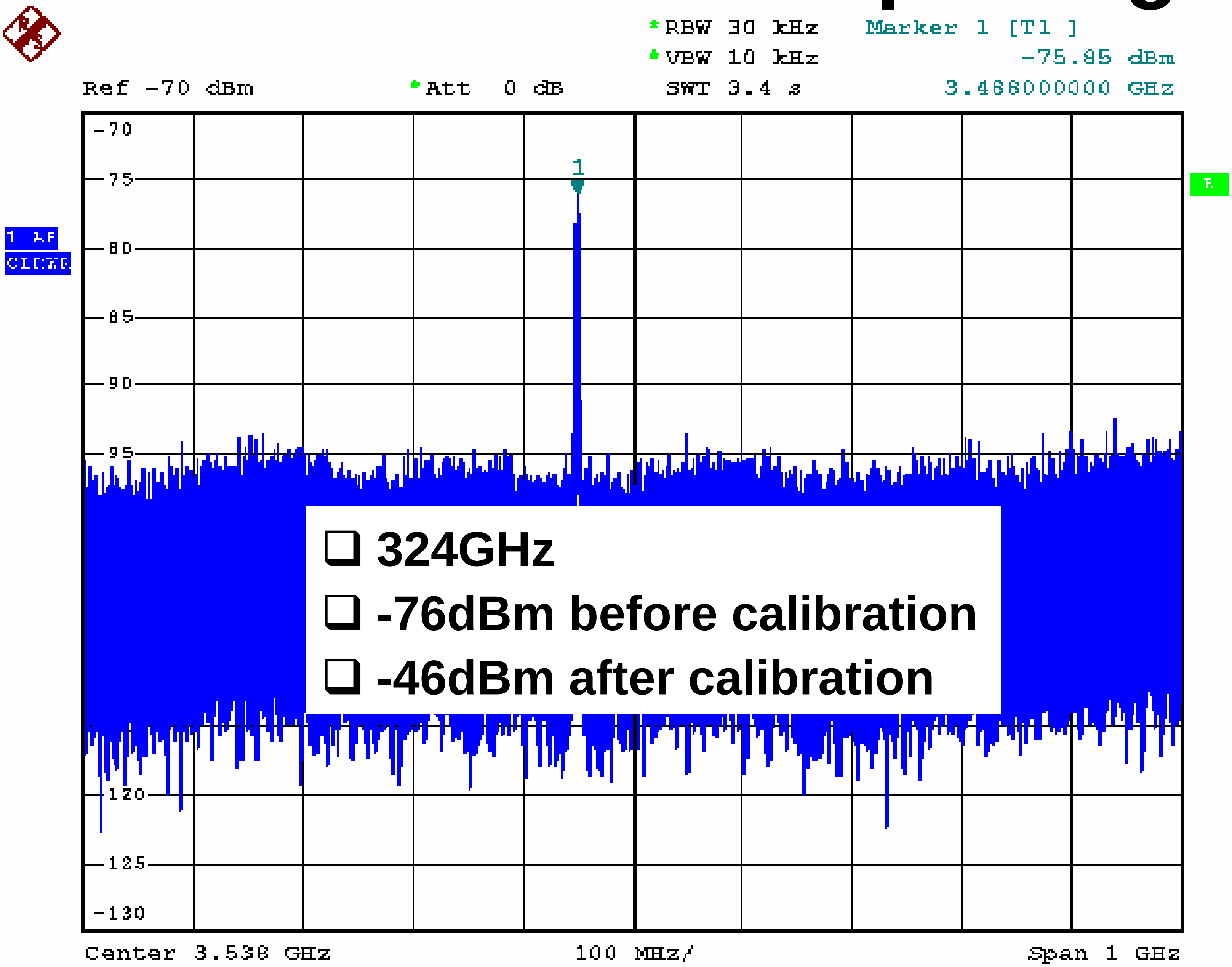
Die Photo


GND
Vbias
GND
VDD
GSG RF Output
GSG RF Output
180μm
210μm
VDD
GND
Vcntrl
GND

324 GHz Test Setup at JPL



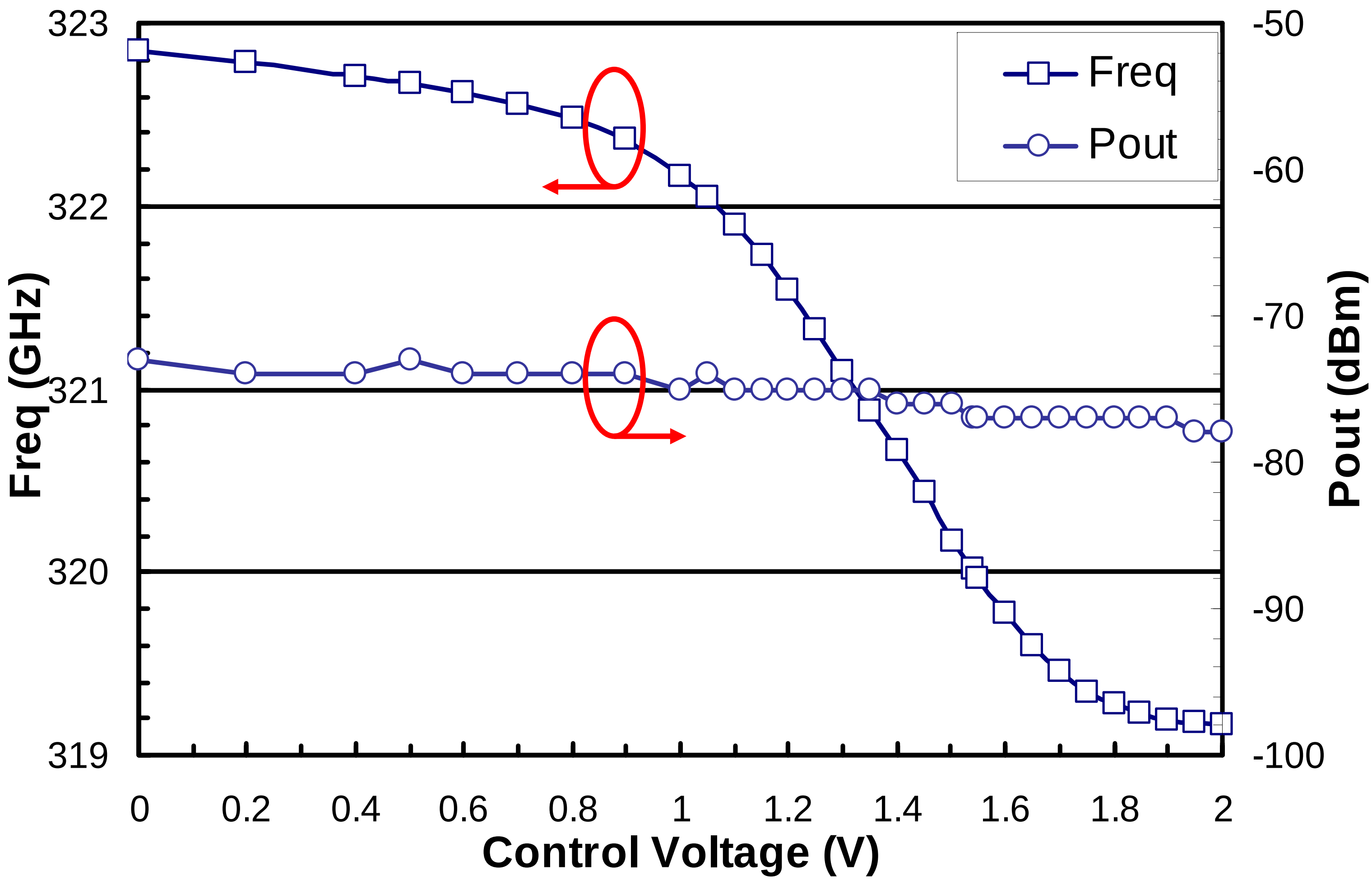
Measured 324GHz Output Signal



- 324GHz
- -76dBm before calibration
- -46dBm after calibration

Measured Frequency Tuning Range

- Approximate 4GHz frequency tuning range
- Less than 5dB output power variation



Performance Summary

Functions	Performance
Output frequency	324GHz
Tuning range	4 GHz
Calibrated output power	-46dBm
Conversion efficiency	17% or -15.4dB
Fundamental tone rejection	>39dB
Estimated phase noise based on fundamental alone Q-VCO measurement	-78dBc/Hz @ 1MHz offset -86dBc/Hz @ 5MHz offset -91dBc/Hz @ 10MHz offset
Current consumption	12mA from 1V supply

Conclusions

- Linear superposition technique devised to generate 324GHz in 90nm digital CMOS with output power of -46dBm and conversion efficiency of 17%
- Measured 4GHz frequency tuning range
- Measured >39dB rejection of fundamental tone at the output node
- Estimated phase noise of -91dBc/Hz @ 10MHz offset

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