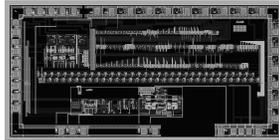


# ADVANCED ELECTRONIC FEATURES FOR HEARING AIDS AND OTHER PORTABLE DEVICES



*IEEE Circuits & Systems Society  
The Dallas Section*

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*Nov. 9, 1999*

## OVERVIEW

- I. HEARING AID TRENDS
- II. RESEARCH GOALS
- III. VOLUME CONTROL RECEIVER
- IV. PROGRAMMABLE INTERFACE RECEIVER
- V. ACTIVE NOISE CONTROLLER (ANC)
- VI. PROJECT CONTRIBUTIONS

## HEARING AID TRENDS

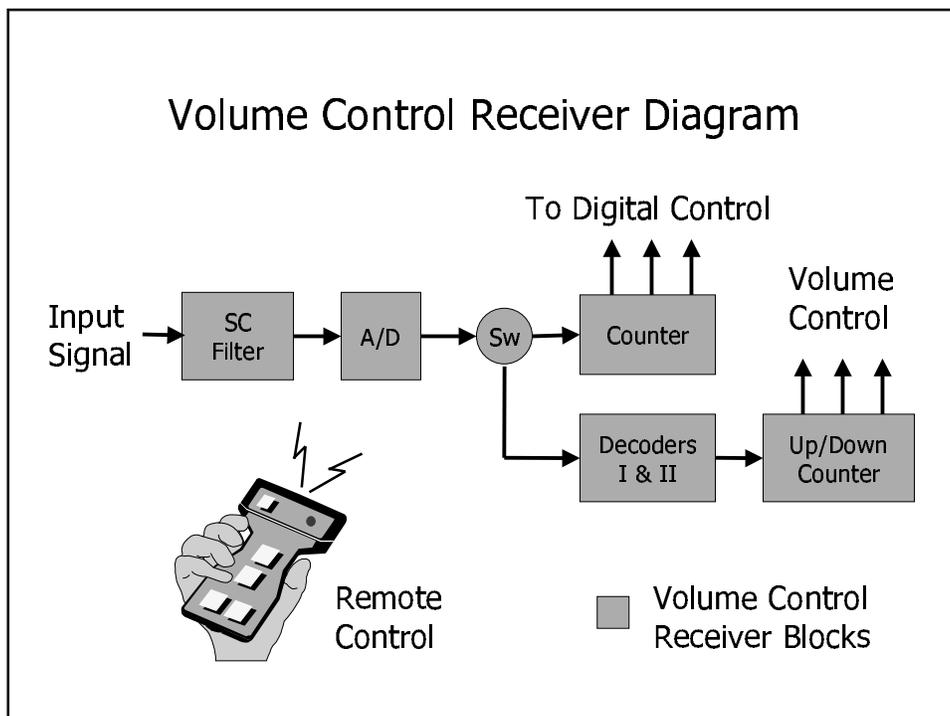
- Present:
  - Perceived invisibility
  - More than 80% sales correspond to in-the-ear (ITE) and completely-in-the-canal (CIC) devices
  - Some HA models are programmable
- Future:
  - Better Performance
  - More advanced features
  - Adjustable (i.e., programmable, flexible)
  - Additional signal processing (i.e., noise cancellation)

## II. RESEARCH GOALS

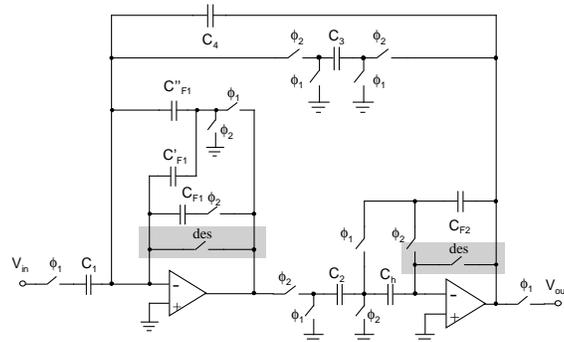
- Research objective is to design, implement & test three (3) novel hearing aid features:
  - Volume Control Receiver, detects incoming signals (audio range) and controls the output of the HA
  - Programmable Interface Receiver, decodes signals and stores preprogrammed settings for each user
  - Noise Reduction System, improves hearing capabilities and speech intelligibility in noisy environments
- Each feature should perform independently, but blocks must be minimized when implemented together

### III. VOLUME CONTROL RECEIVER

- Volume Control Receiver, detects incoming signals (audio range) and controls the output of the HA
  - Input signal is converted from analog to digital
  - Area and power efficient
  - Decodes two (2) commands, which increase & decrease the hearing aid volume
  - Uses standard Dual-Tone-Multi-Frequency (DTMF) tones, which are in the audio range



## Switch Capacitor Bandpass Filter

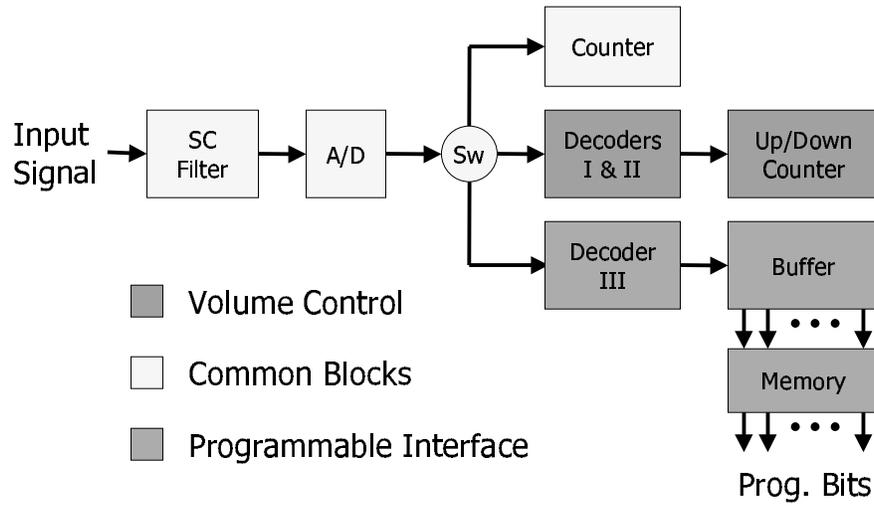


- Four (4) variable center frequencies
- Area efficient (including offset cancellation)
- Additional reset switches across each amplifier

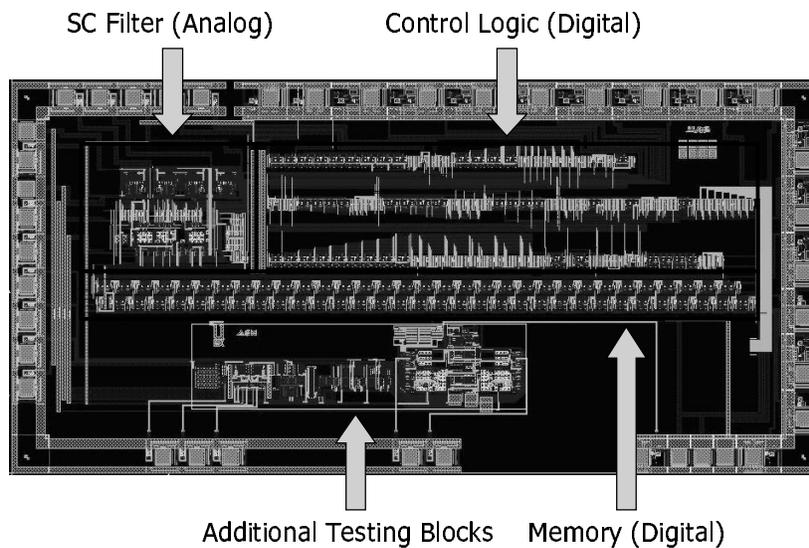
## IV. PROGRAMMABLE INTERFACE RECEIVER

- Programmable Interface Receiver, decodes signals and stores preprogrammed settings for each user
  - Shares several components with previous design
  - Decodes two (2) security codes with variable selectivity
  - Stores up to 45 bits, which can be easily upgraded
  - Stores filter frequency/gain compensation & automatic-gain-control (AGC) settings

## Combined Receiver Diagram

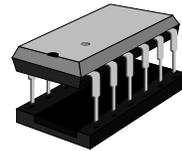


## Combined Receiver Layout



## Combined Receiver IC Implementation

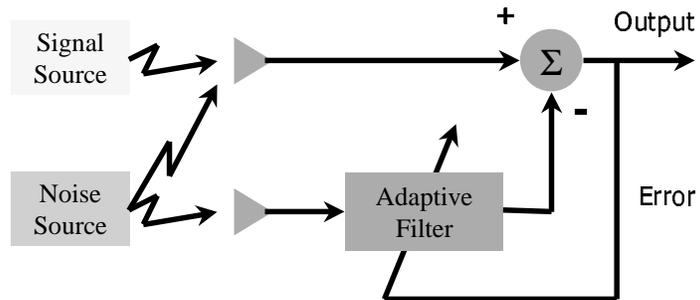
- Fabricated & tested using 1.2 $\mu\text{m}$  AMS technology
- Layout area: 3,000 $\mu\text{m}$  x 1,000 $\mu\text{m}$
- Total power consumption: 1.5mWatts
- Blocks implemented:
  - ➔ Custom Digital Blocks
  - ➔ Amplifiers in Weak Inversion
  - ➔ Programmable Switched-Capacitor Filter



## V. ACTIVE NOISE CONTROLLER (ANC)

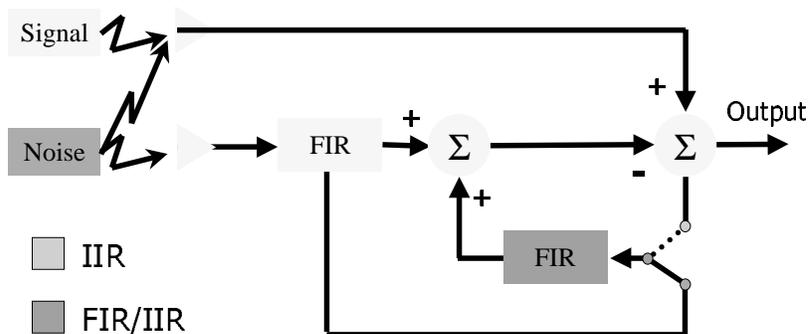
- Noise Reduction System, improves hearing capabilities and speech intelligibility in noisy environments
  - ➔ Combined FIR/IIR topology with analog blocks
  - ➔ Maximum (IIR) and stable cancellation (FIR) for all common environments
  - ➔ Moderate order filter (because of tradeoffs between accuracy and size)
  - ➔ Requires separate reference input for noise source
  - ➔ LMS adaptive algorithm was implemented, but it could be modified to realize other algorithms

## ANC System Diagram



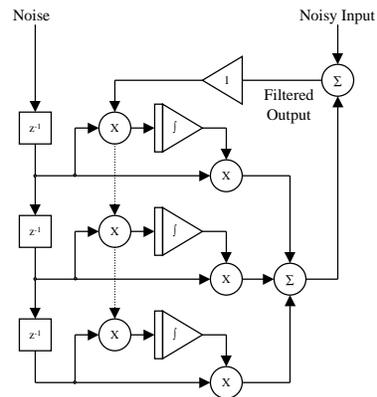
- ✓ Improves speech intelligibility
- ✓ Reduces undesired background noise

## Combined FIR/IIR ANC System Diagram



- ✓ Design implements both FIR and IIR Filters (with automatic or manual control)

## Actual Implementation (FIR Block)

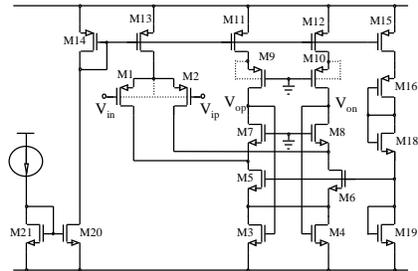


- LMS adaptive algorithm implementation

## ANC Building Blocks

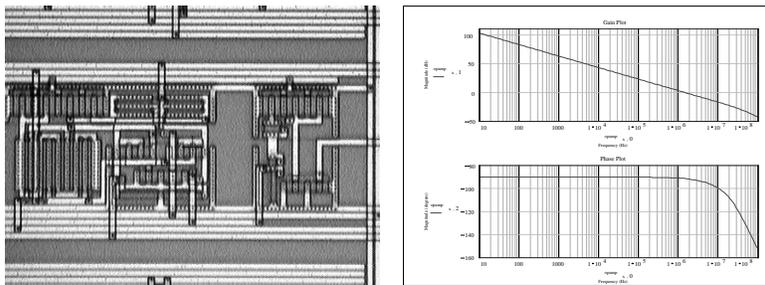
- Building blocks have following characteristics:
  - Analog implementation
  - Non-multiplexed system configuration
  - Implemented with 1.2μm AMI technology
- Following blocks are described in more detail:
  - A. Fully Differential Amplifier
  - B. Four Quadrant Multiplier
  - C. Switched Capacitor Summer
  - D. Switched Capacitor Delay Line

## A. Fully Differential Amplifier Diagram



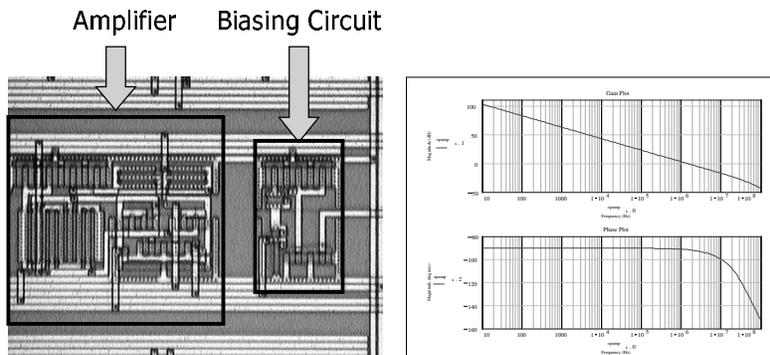
- ✓ Fully differential folded cascode structure
- ✓ Simple and effective continuous common mode feedback (CMFB)
- ✓ Area efficient (reasonable transistor ratios)

## FD Amplifier Characteristics



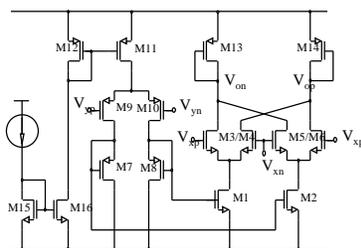
- ✓ Maximum PSRR (Power Supply Rejection Ration)
- ✓ High DC gain
- x Reduced Common Mode (CM) Range

## FD Amplifier Layout and Results



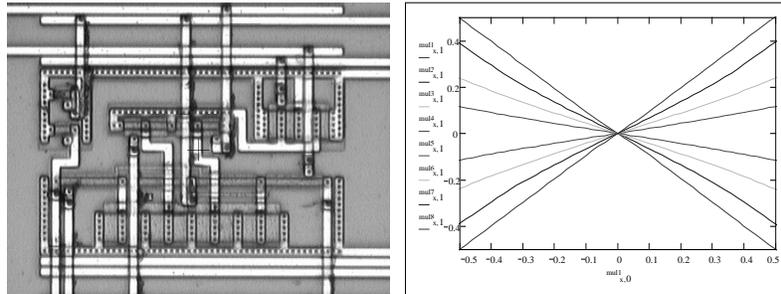
- Area efficient:  $106\mu\text{m} \times 127\mu\text{m}$
- Interdigitated layout for the differential pair and current mirrors (each transistor divided into even numbers)

## B. Fully Differential Multiplier



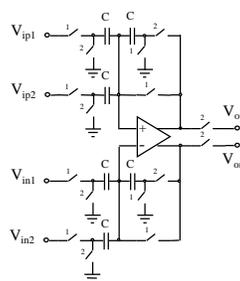
- Valid for all four (4) quadrants
- Crossed-coupled inputs
- Better linearity and wider input range

## FD Multiplier Layout and Results



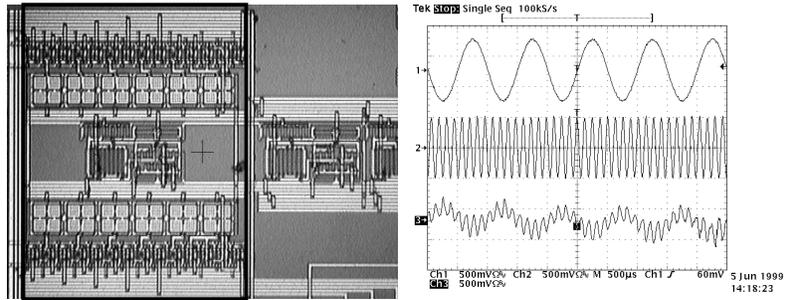
- Compact layout implementation:  $76\mu\text{m} \times 123\mu\text{m}$
- Same biasing circuit as Fully Differential Amplifier
- High linearity for specified input range

## C. Switched Capacitor Summer



- ✓ Simple fully differential configuration
- ✓ Can be used for multiple inputs (i.e., 30)
- ✗ All inputs must be summed every clock cycle (critical when several inputs are required)

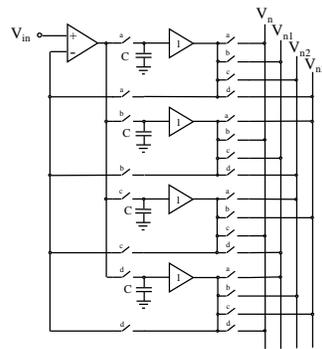
## SC Summer Layout and Results



↑  
SC Summer

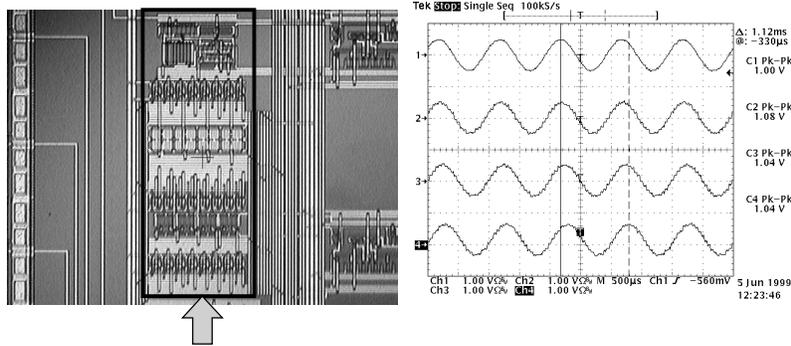
- Very efficient power consumption (one amplifier)
- Moderate layout area:  $342\mu\text{m} \times 260\mu\text{m}$

## D. Discrete Time Delay Line Block



- Only One robust amplifier and several simple buffers are needed

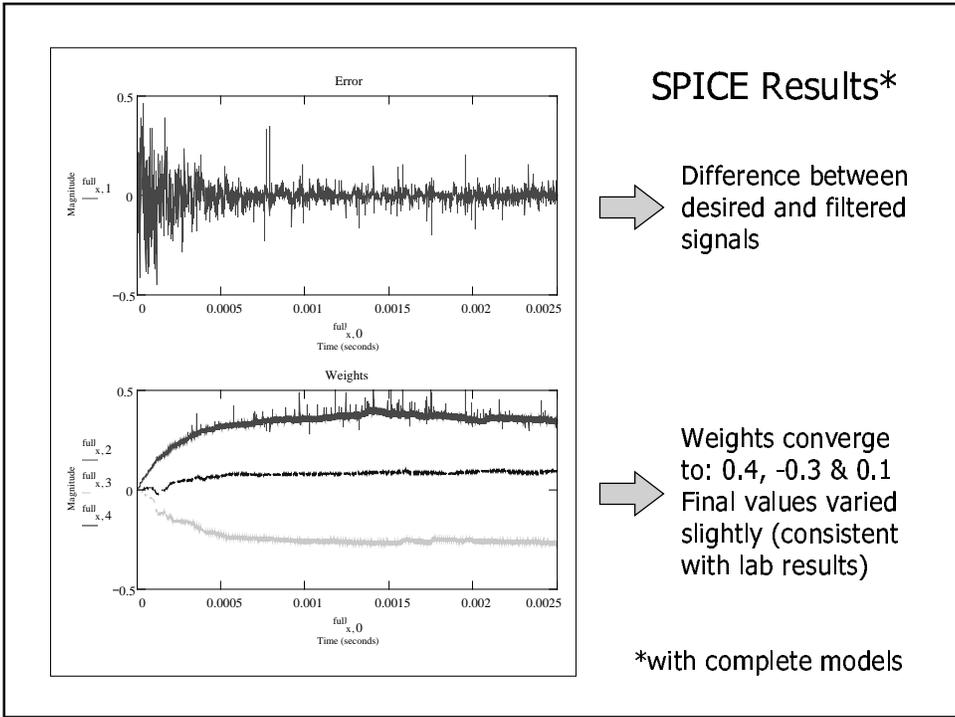
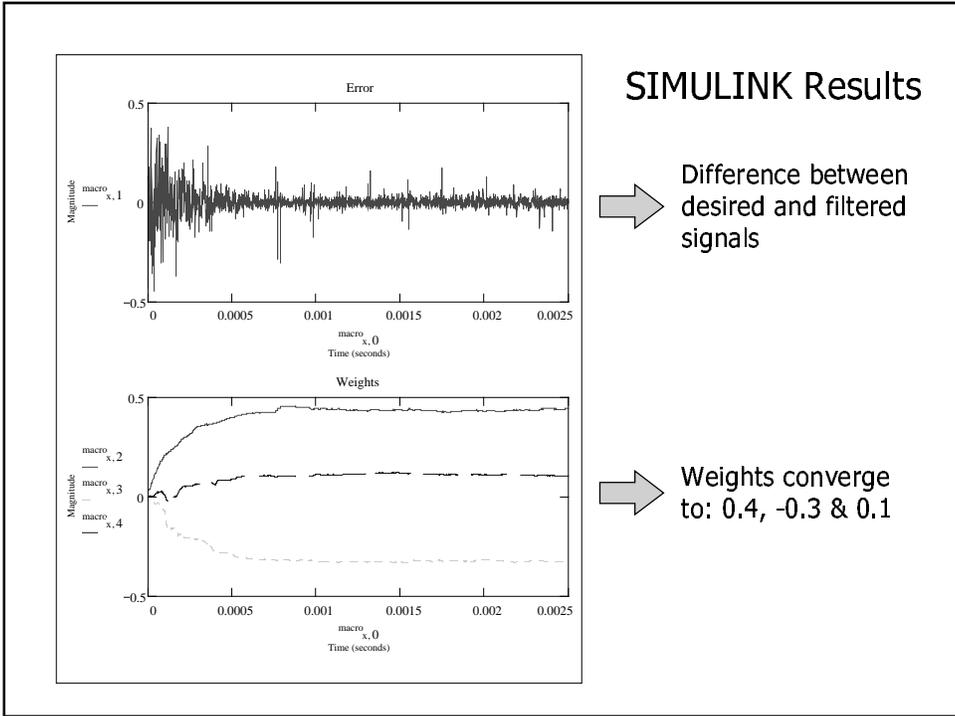
## Delay Line Layout and Results



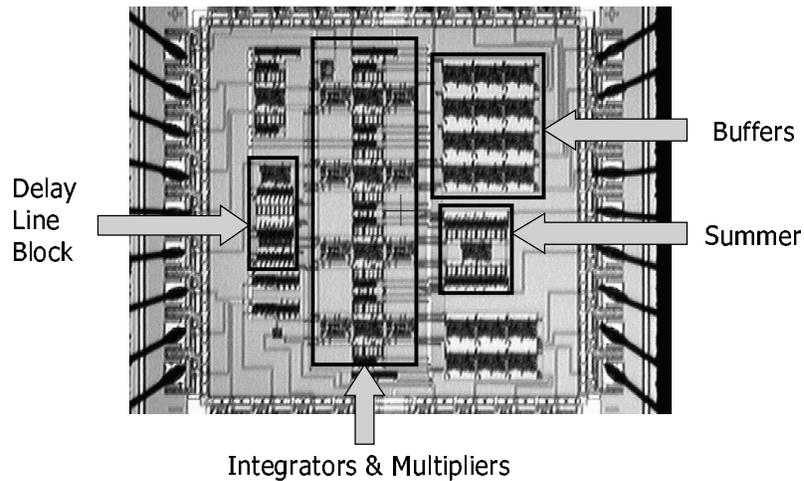
- Excellent power efficiency due to single amplifier usage
- No error accumulation because each delayed output is generated directly from the input signal

## ANC System Results Summary

- FIR with known weights was used to generate desired signal
  - Initial weights set to: 0.4, -0.3 & 0.1
- ANC System was used to mimic FIR with known weights
  - White noise was used as the input signal for FIR with known weights and FIR with LMS algorithm
  - Results were similar for all cases:
    - ✓ Top level simulations with SIMULINK
    - ✓ SPICE simulations with macromodels
    - ✓ SPICE simulations with complete models
    - ✓ Experimental results from fabricated prototypes



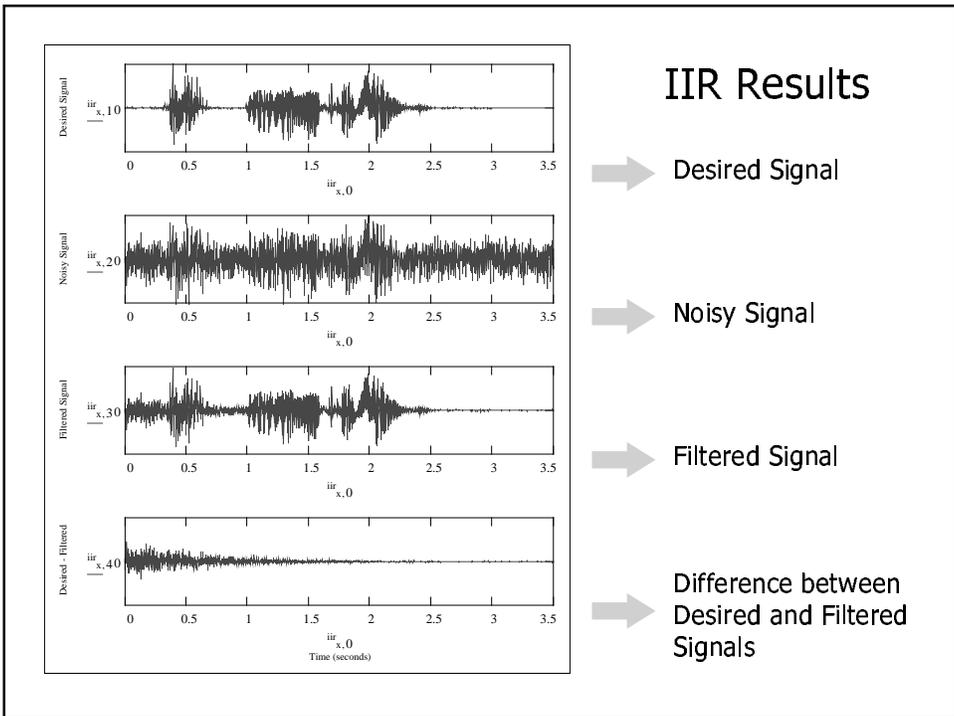
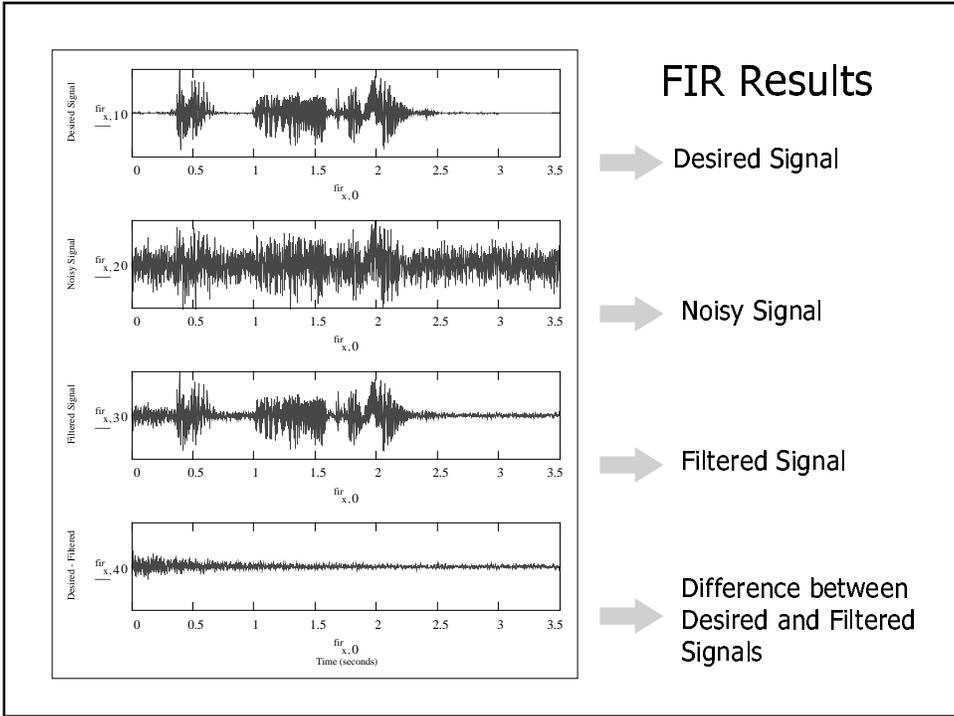
## ANC System Layout



## ANC System IC Implementation

- ANC was fabricated on a  $2000\mu\text{m} \times 2000\mu\text{m}$  microchip using AMI technology
- Experimental Results:
  - Prototype converged to: 0.39, -0.28 & 0.12
  - Final values varied slightly (1% to 2%)
- Possible configurations:
  - System can be connected externally to implement a FIRs with several more weights: 30 taps
  - Implementation of a IIR is also possible





## VI. PROJECT CONTRIBUTIONS

- System engineering approach that transforms ideas into practical system implementations
- Three original system designs that meet demand and consumer/marketing expectations
- Successful implementation of analog and digital designs on single microchips (true mixed-signal circuits)
- Comprehensive and compact system solutions:
  - Volume Control Receiver requires only one filter (similar receivers require at least two filters)
  - Programmable Interface can be upgraded and requires only additional digital logic (not extra analog blocks)

## Project Contributions (Continued)

- Complete analog ANC system was implemented and tested on a single microchip
- ANC system is capable of implementing FIRs and IIRs
- Consists of several outstanding blocks such as amplifiers, multipliers, integrators, summers and delay line blocks:
  - High performance with moderate power consumption
  - Fully differential implementation
- Designs can be implemented in several other applications: cell phones, headphones, portable audio players, hearing protection devices, home and office electronics