

Integrated VCOs for Wireless Communications

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Outline

- Ring Oscillators
 - Circuit Design
 - Test Results
- Phase Noise
- LC Negative- g_m Oscillators
 - BJT implementations
 - CMOS Implementations
 - Simulations
- Conclusions

Voltage-Controlled Oscillators

- Oscillators are very versatile building blocks that are widely used in communication circuits.
- Different applications usually require different specifications, most of which are often in conflict with each other.
- Some of the important specifications are:
 - Phase stability
 - Tuning range
 - Tuning linearity
 - Frequency pushing (dependency of f_{osc} on the power supply)
 - Frequency pulling (dependency of f_{osc} on the load impedance)
 - Low cost

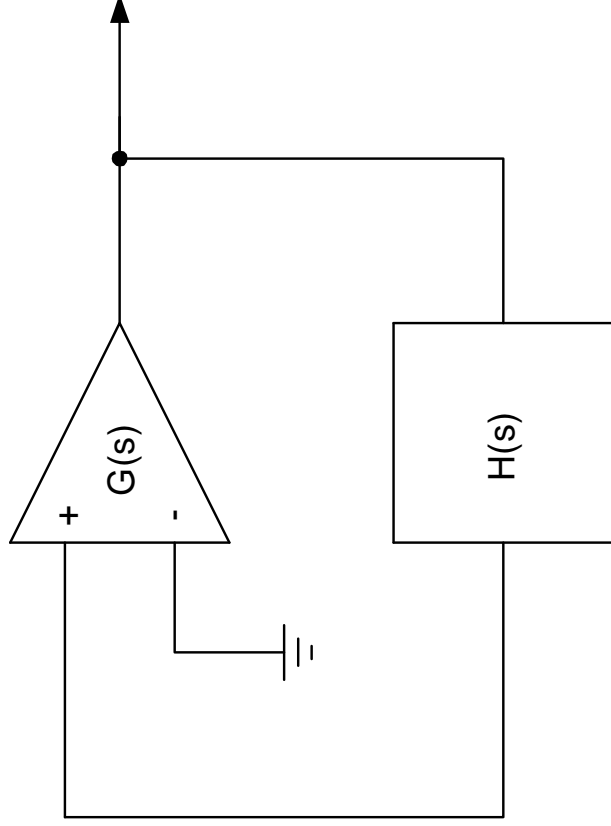
Ring Oscillators

- Ring oscillators are natural candidates for fully integrated oscillators due to their simplicity and ease of integration.
- They are widely used in a lot of PLL frequency synthesizer and clock recovery designs.
- The periodic signal is generated through the use of a ring of inverters.
- The oscillation period is $2nT_d$, with n the number of inverters in the ring and T_d the delay of one inverter.

Ring Oscillators

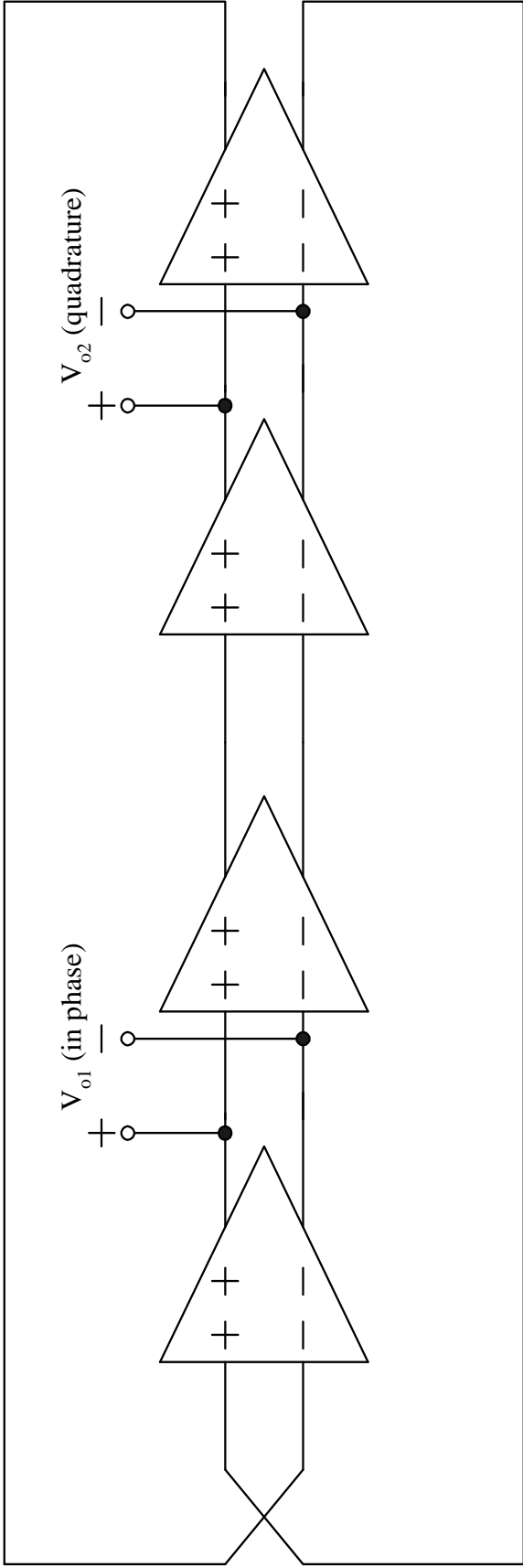
- The main difficulty for using submicron CMOS ring oscillators in wireless communication systems is their relatively poor phase noise response.
- Precaution is required to achieve as low phase noise as possible from CMOS ring oscillators.
 - Dominant noise sources in IC environment are common-mode signals in nature (e.g. power supply noise, substrate-coupled noise).
 - | Fully differential design is a must!

Barkhausen Criteria

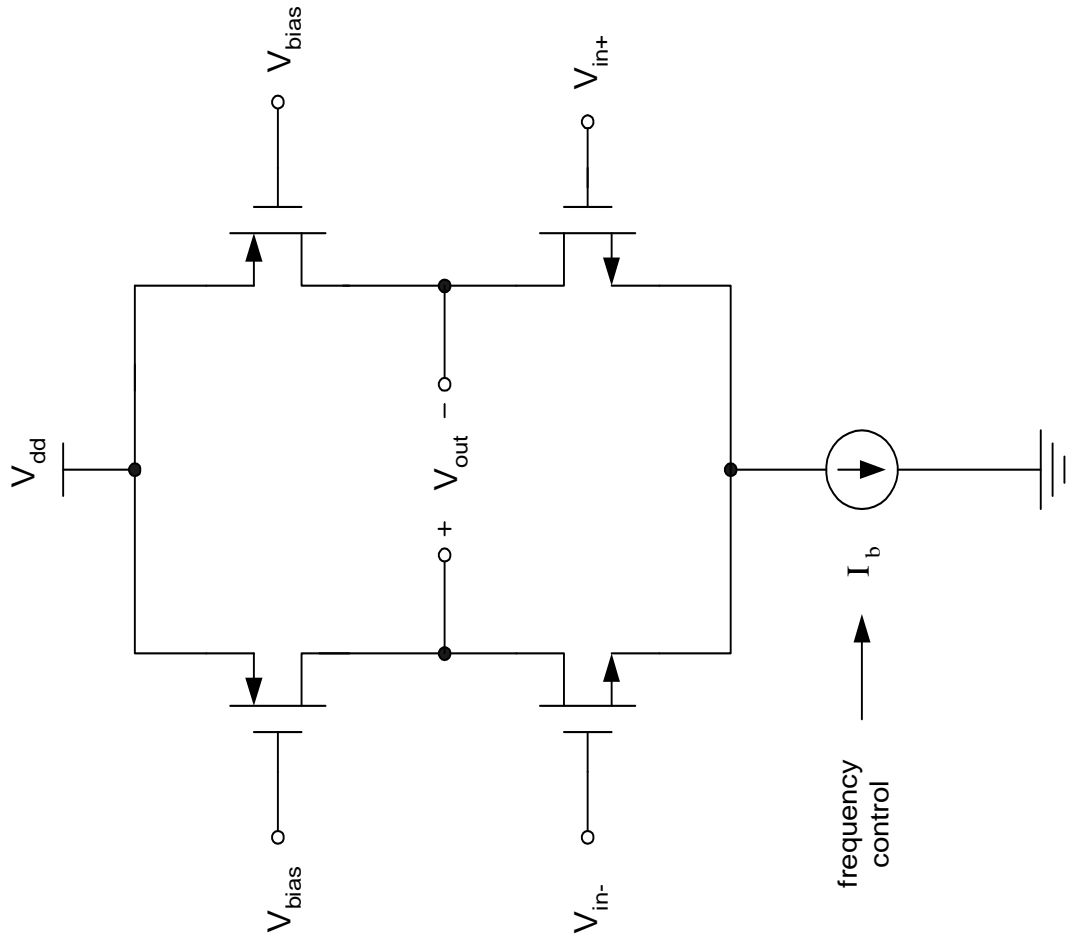


- The net gain around the loop at the frequency of oscillation should be equal to one.
- The net phase shift around the loop must be a positive integer multiple of 2π radians or 360 degrees. This corresponds to the fact that the imaginary part of the loop gain $G(s)H(s)$ should be zero, which gives the frequency of oscillation.

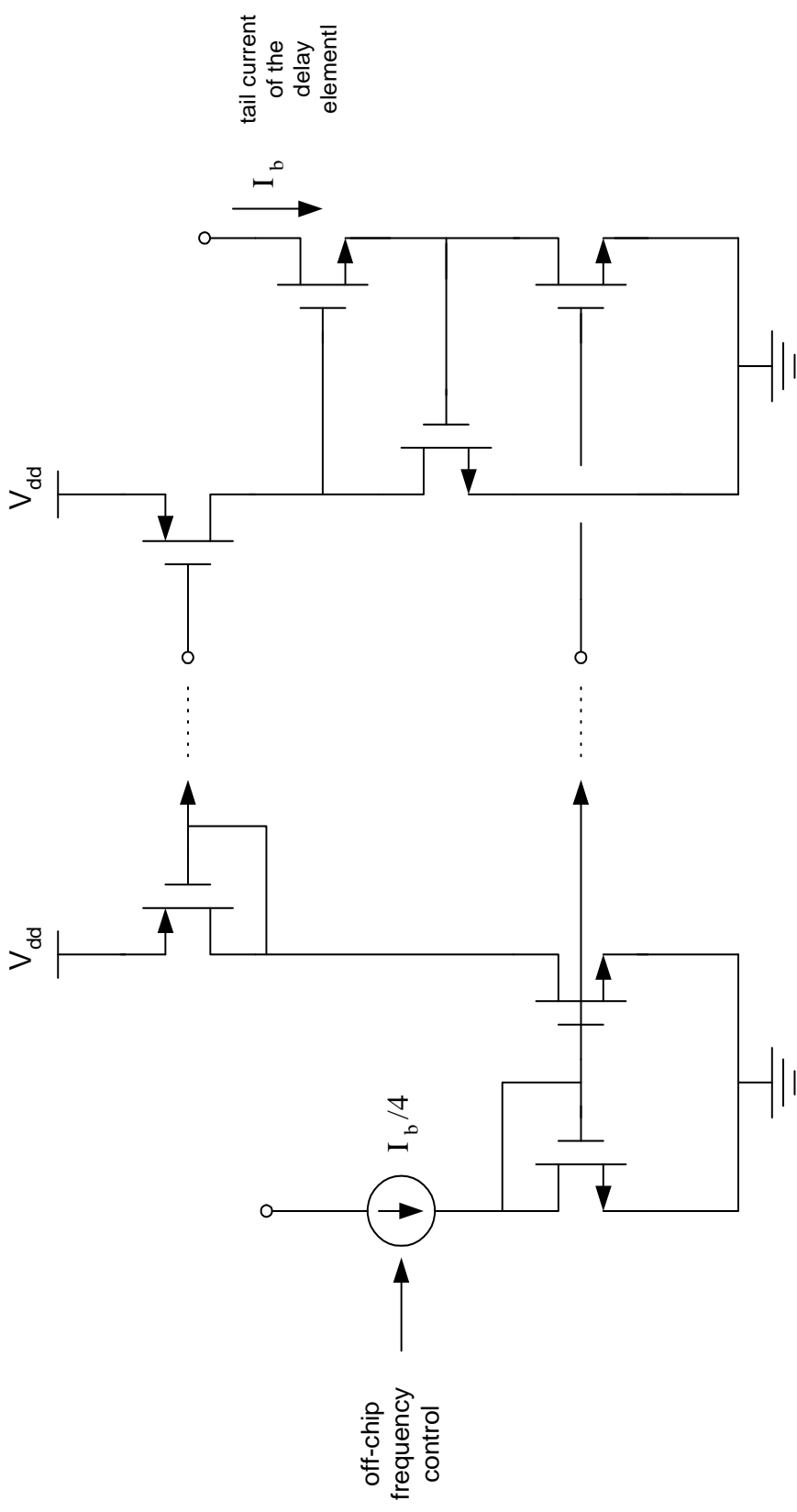
Fully Differential Ring Oscillator



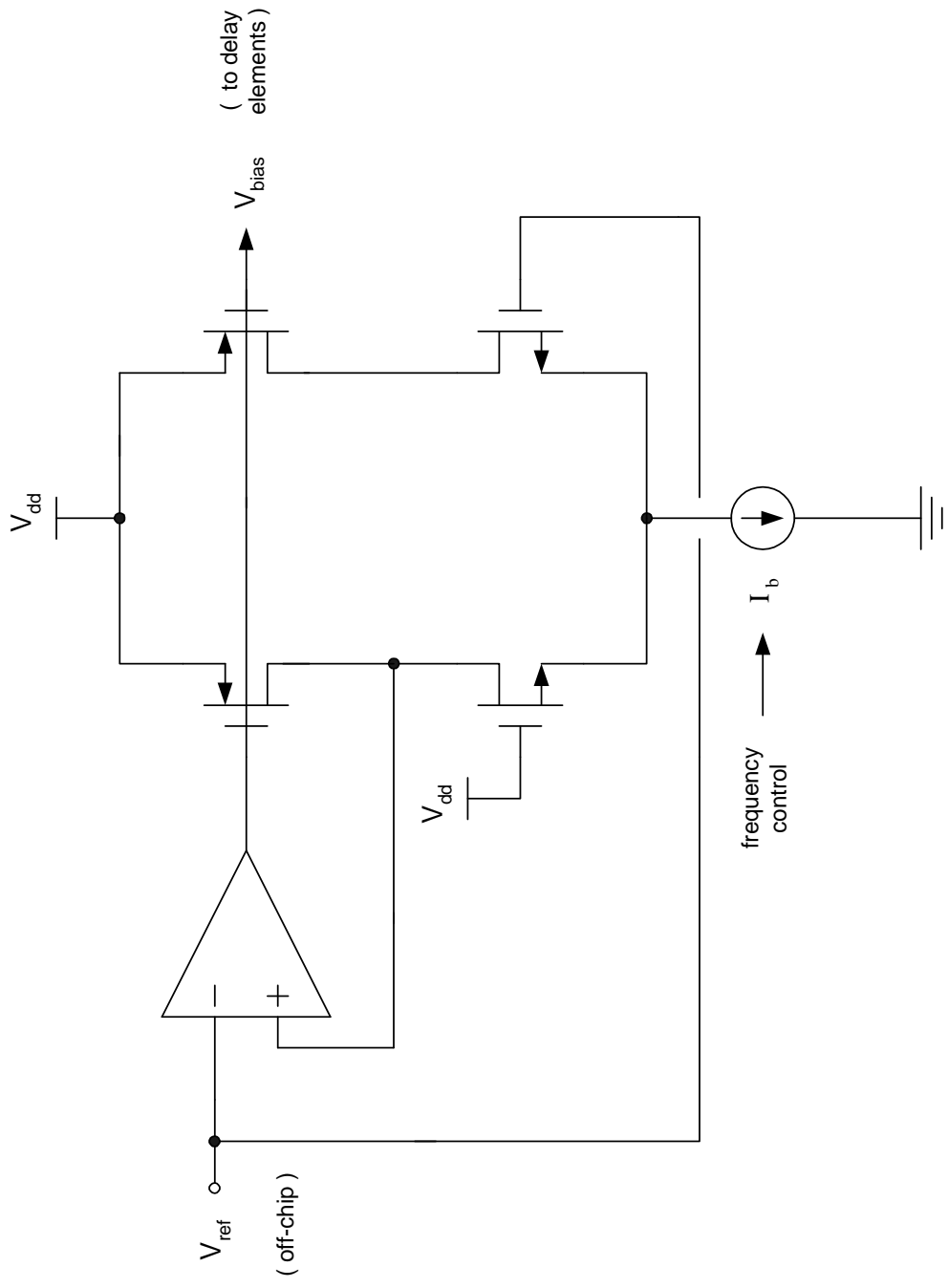
Delay Element



Frequency Control Through Biasing



Replica Biasing

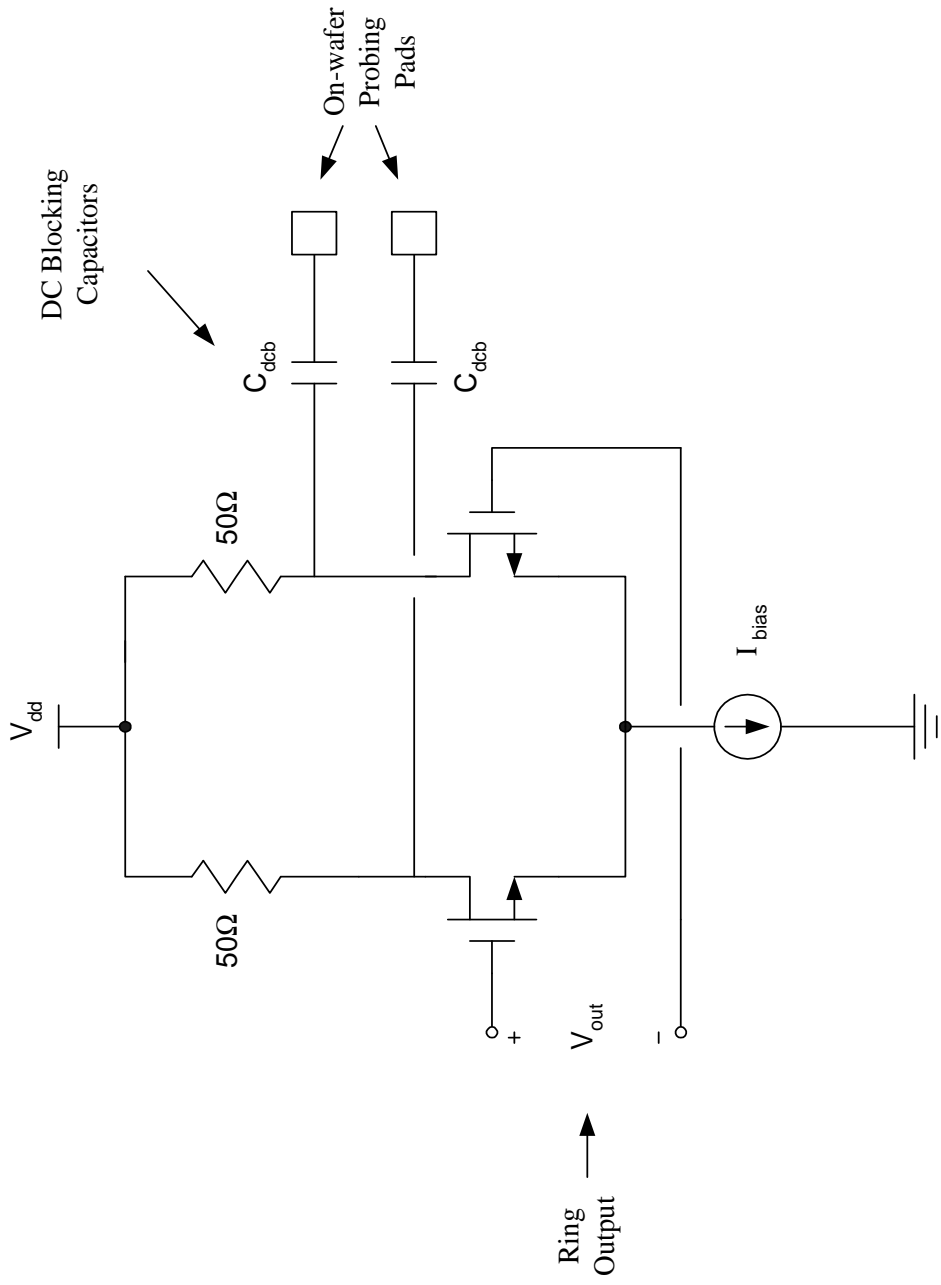


Frequency Control

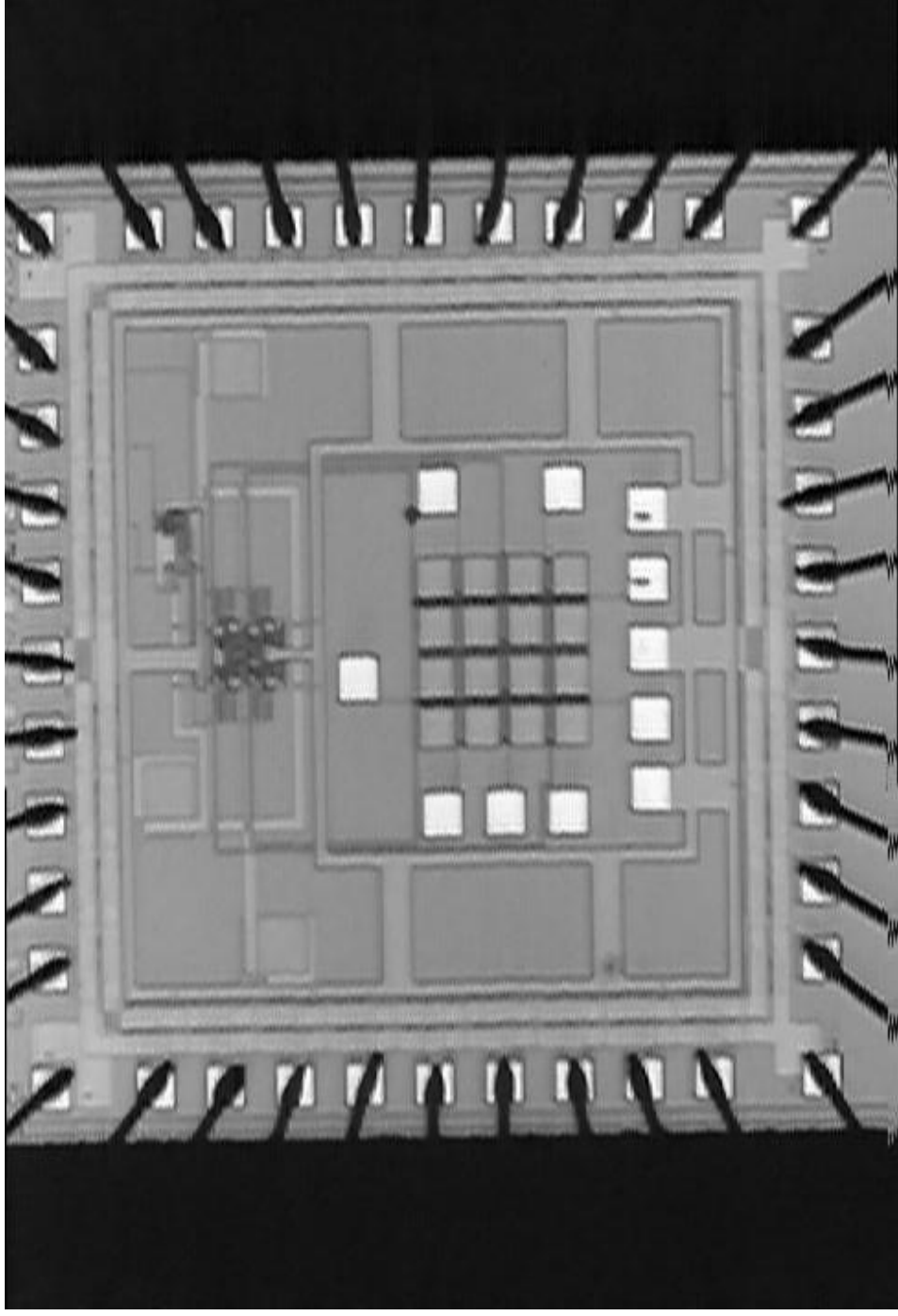
- Frequency of oscillation, (f_{osc}), is controlled through the bias current of a delay element (I_b).
- Maximum peak-to-peak voltage, (V_{pp}), is controlled through the replica biasing.
- Total output capacitance of a delay element, (C_{out}), directly affects the frequency of oscillation.

$$f_{osc} \approx \frac{I_b}{V_{pp} \cdot C_{out}}$$

Buffers for Testing



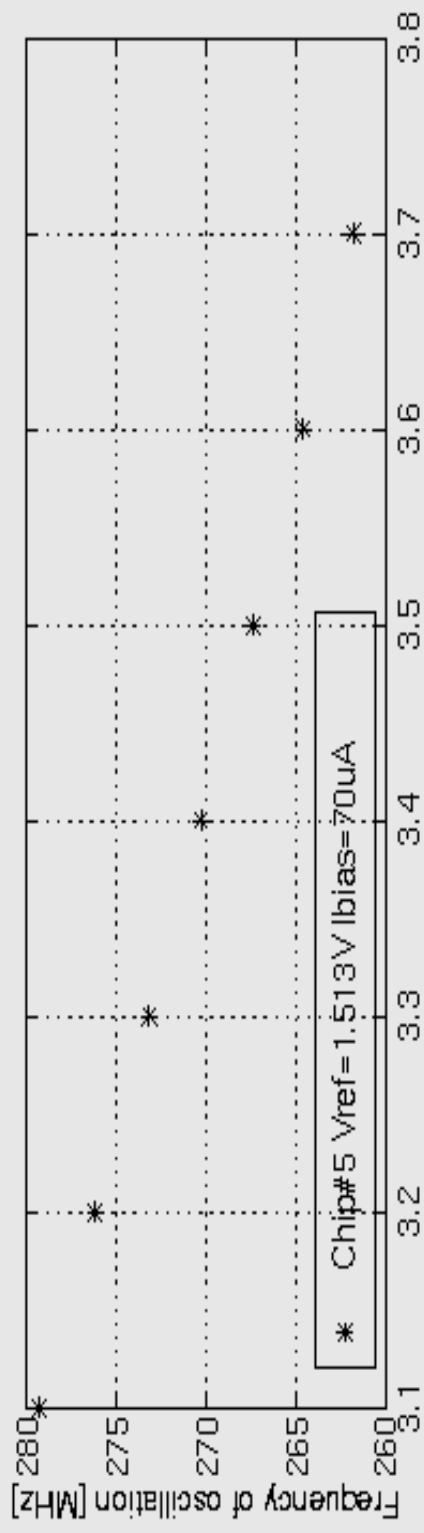
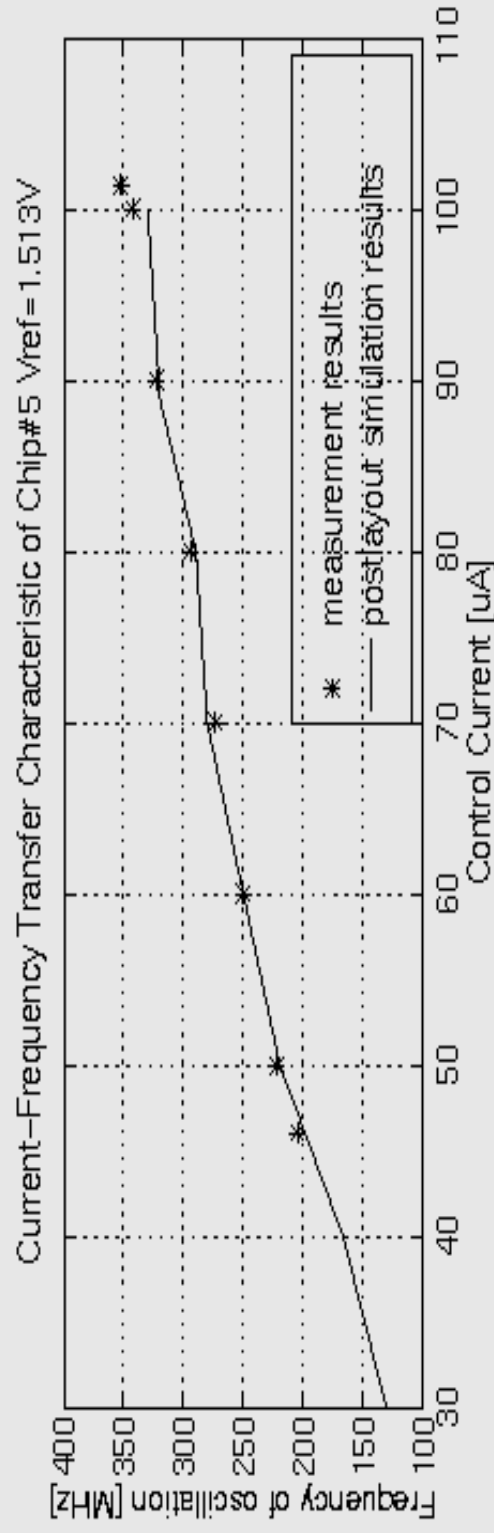
Chip Photomicrograph



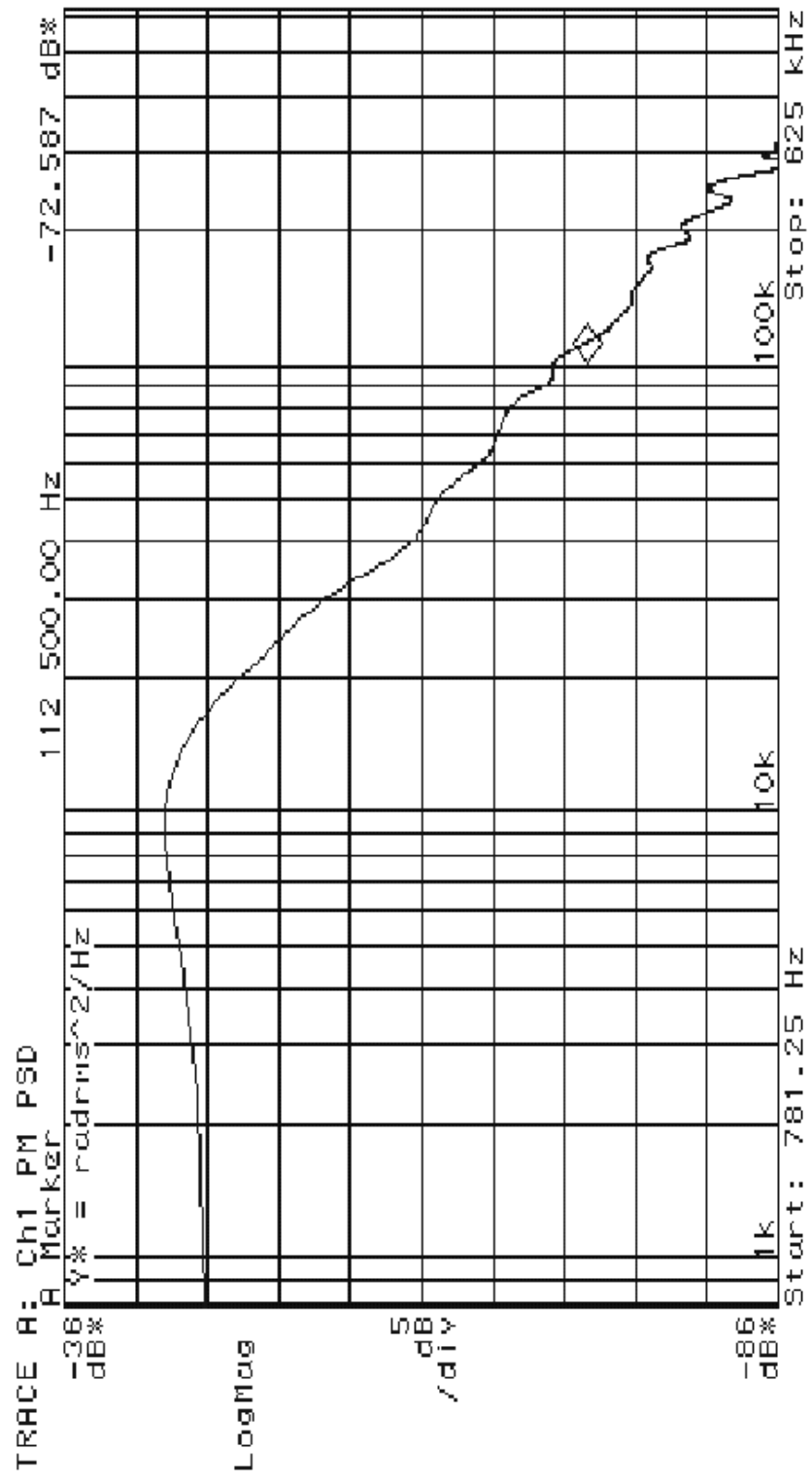
Test Results

- The chip was fabricated with HP 0.5 μ m Digital Technology through MOSIS.
- 25 chips were received and all of them were found functional.
- Another version of the same design in which the outputs were connected directly to the bonding pads was fabricated. 25 chips were received from that version and all the chips were found functional.

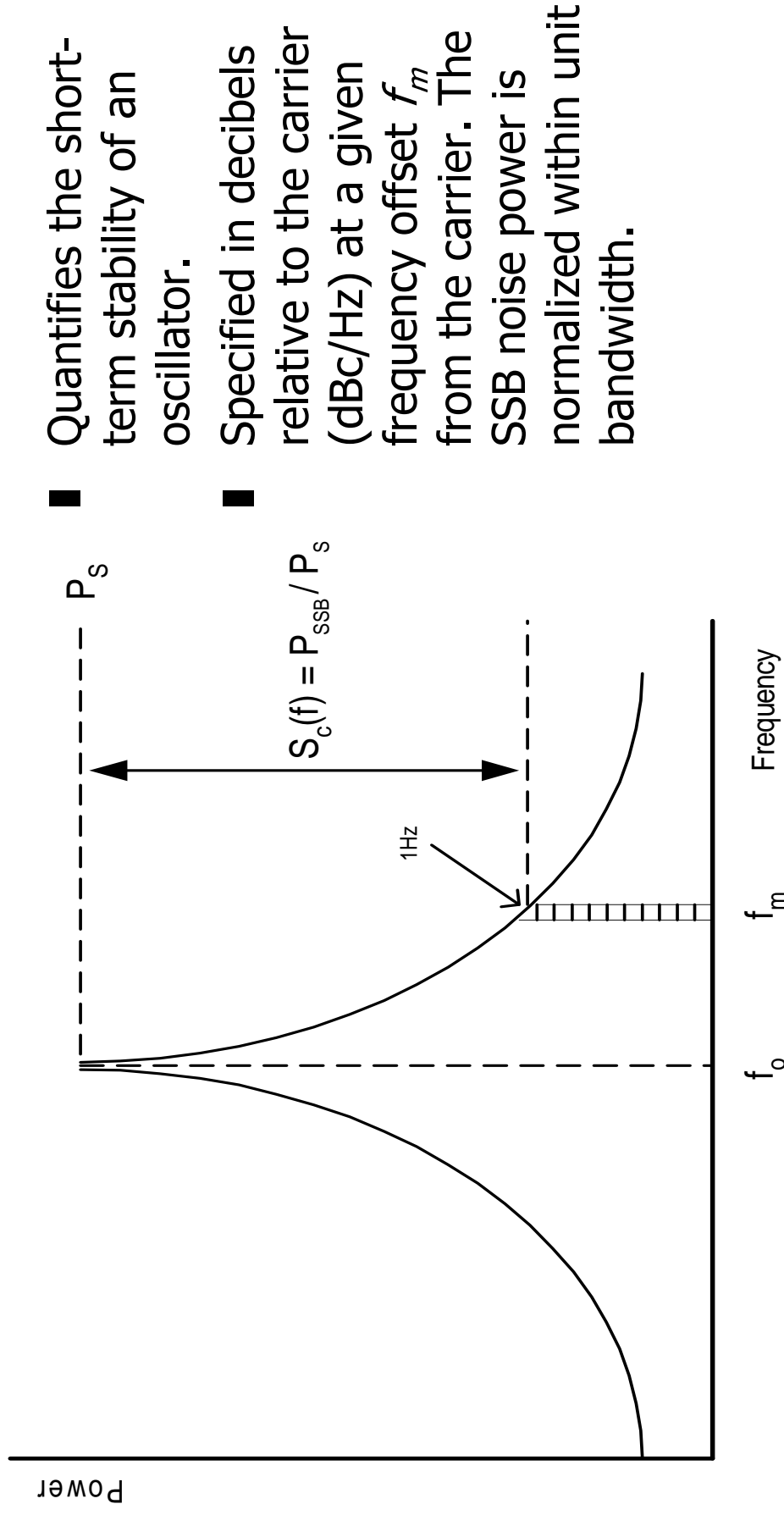
Test Results



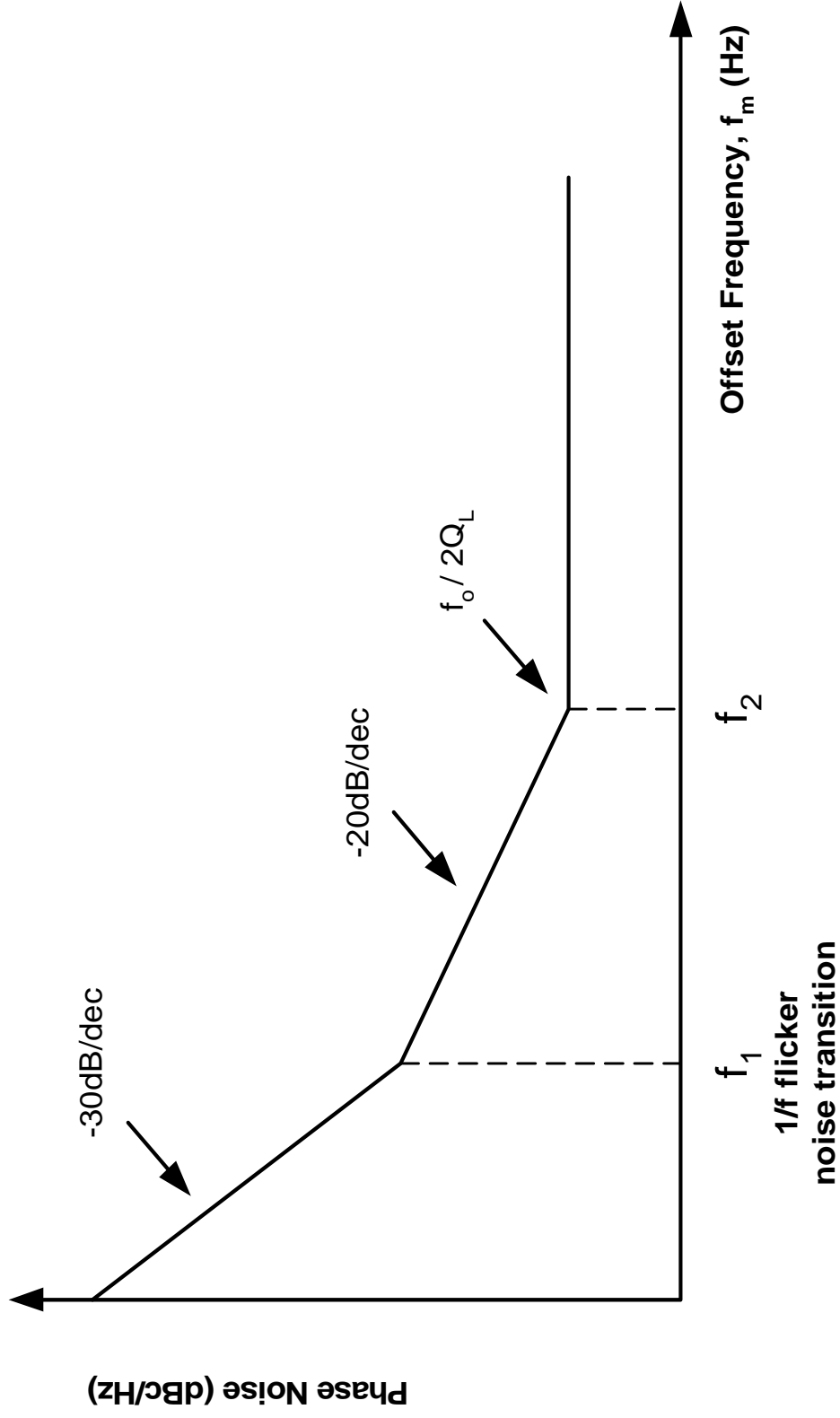
Test Results



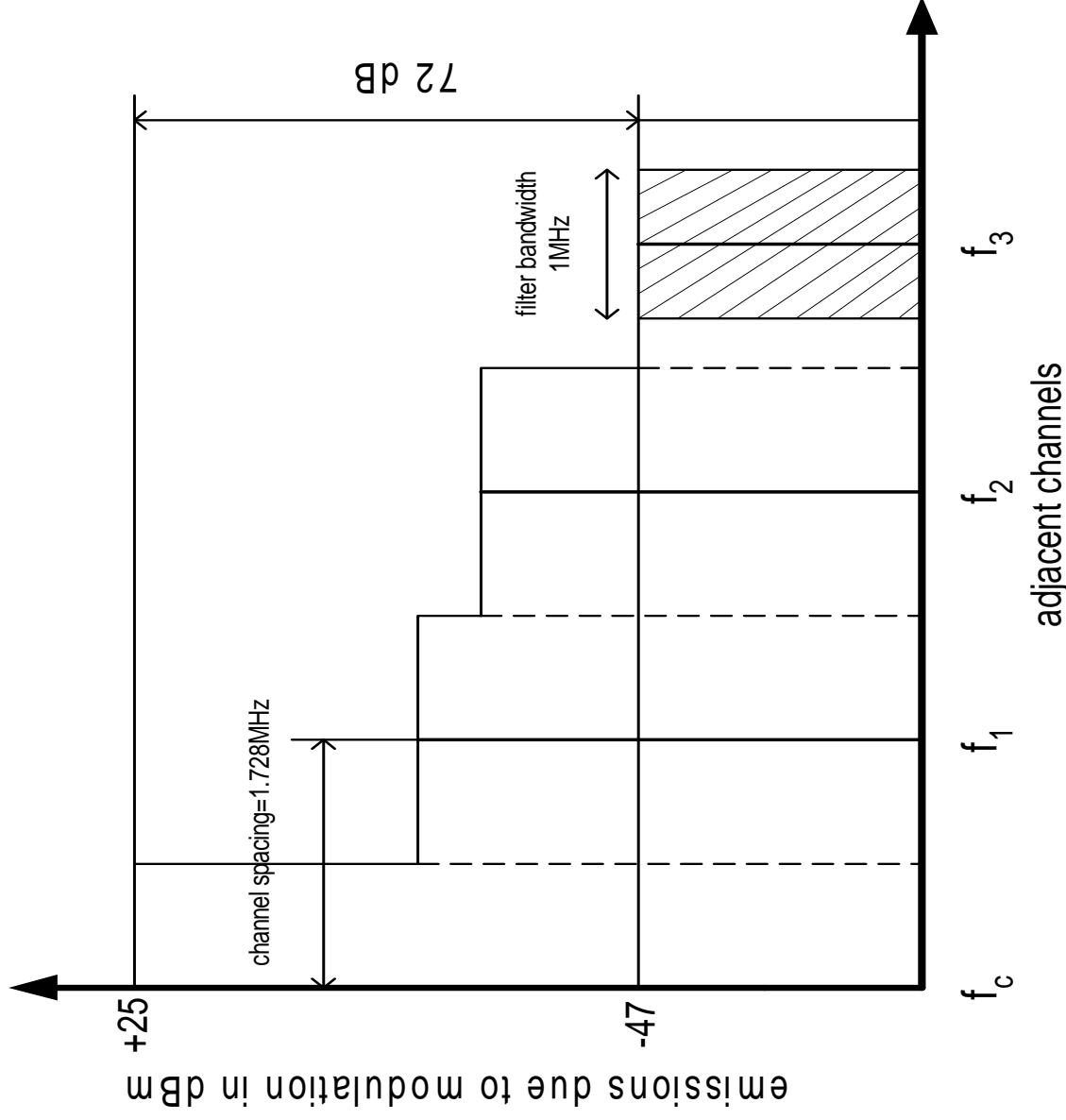
Phase Noise



Phase Noise



Determination of phase noise spec.



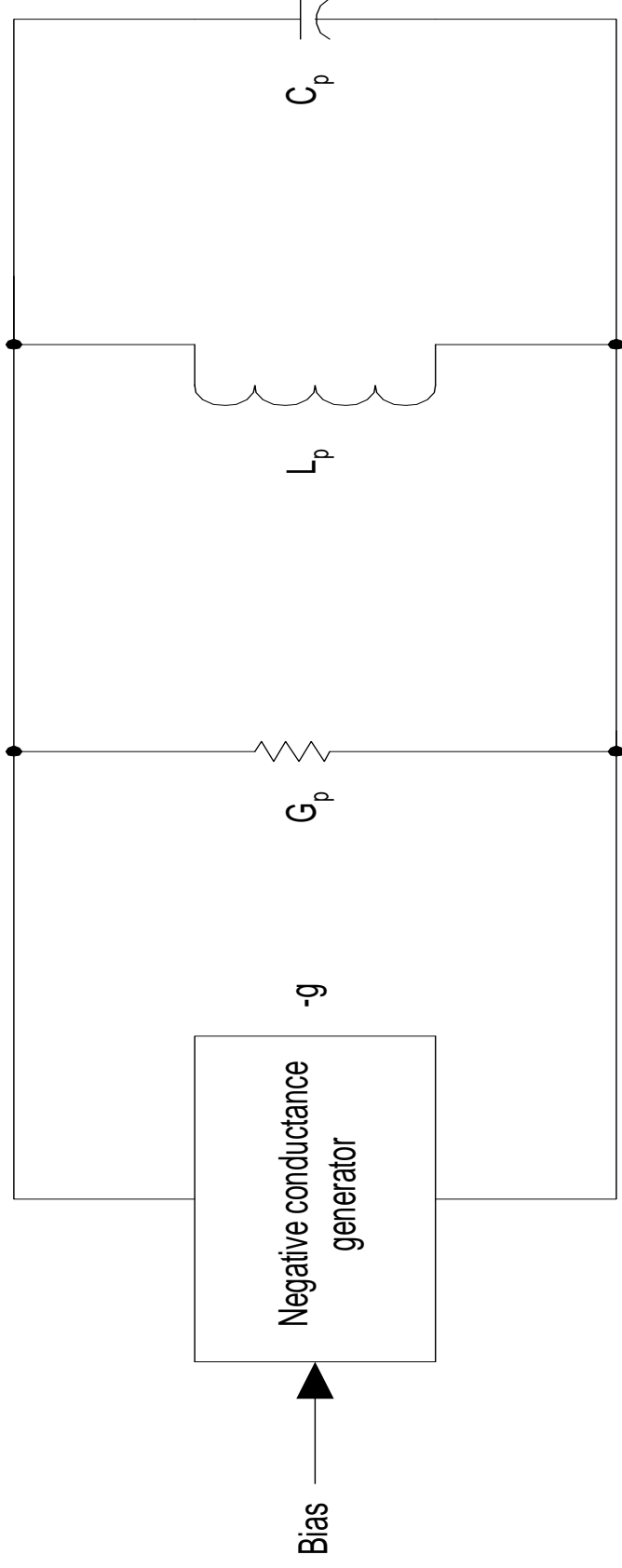
- In the Digital European Cordless Telecommunications (DECT) standard, the critical point concerning the oscillator phase noise is the emissions due to modulation. The emitted power at the output in the third adjacent channel is specified to be smaller than 20nW (-47dBm), [4].

Phase Noise in Ring Oscillators

- A first-order estimate for the phase noise of a fully-integrated ring oscillator, [13]:
- Noise is inversely proportional to the effective bias ($V_{GS}-V_T$), that is limited by the available power supply voltage.
- Phase noise improves with larger supply current I_{SS} .
 - | Lower phase noise with higher power consumption!
- F_1 , noise contribution factor, is directly proportional to the small-signal gain of the inverter. Higher gain implies higher nonlinearity and higher up-conversion of $1/f$ noise, significant especially in the CMOS transistors.

$$S_{\phi}(f_0) \cong \left(\frac{f_0}{\Delta f} \right)^2 \frac{F_1 kT}{I_{SS} (V_{GS} - V_T)}$$

Negative Conductance Oscillators



Negative Conductance Oscillators

- A parallel resonance circuit is connected in parallel with a negative-conductance generator that compensates for the tank losses.
- The condition to be satisfied for oscillation is:

$$|g| \geq G_p$$

- To ensure start-up, the negative conductance is usually designed to be two to three times larger than the equivalent loss in the tank.
 - | The oscillation amplitude grows in magnitude until some nonlinearity in the negative-conductance generator decreases the negative-conductance to the critical value.
- The circuit oscillates at $f \cong \frac{1}{2\pi\sqrt{LC}}$

LC Oscillators

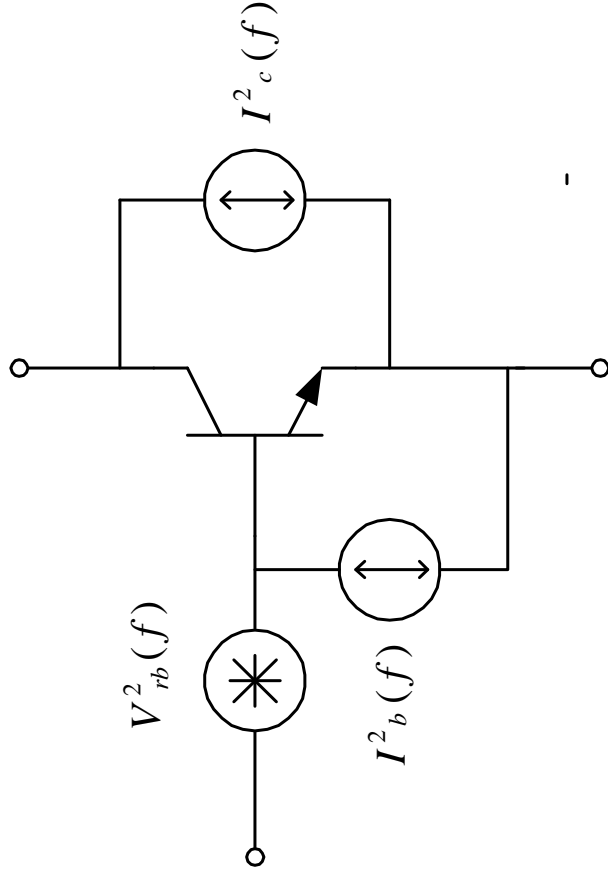
- Negative- g_m (negative conductance) oscillators are known to provide the best phase noise performance among integrated oscillators.
- It is possible to build a fully-differential oscillator with only two transistors in the signal path.
- The phase noise depends on the quality factor of the resonator, the noise figure of the amplifier creating the negative resistance and the energy in the resonator.
- The quality factor of the resonator is usually limited by that of the inductor.

Phase Noise in LC Negative Conductance Oscillators

- A first-order estimate for the phase noise of a fully-integrated LC VCO, [14]:
 - The quality factor of the tank (Q) has a strong effect on the phase noise.
 - The noise factor (F) of the active devices generating the negative conductance affects the performance through the number of times the negative conductance is larger than the tank loss (α).
 - Increasing the oscillation amplitude through increased the supply current helps with the price of increased power consumption.

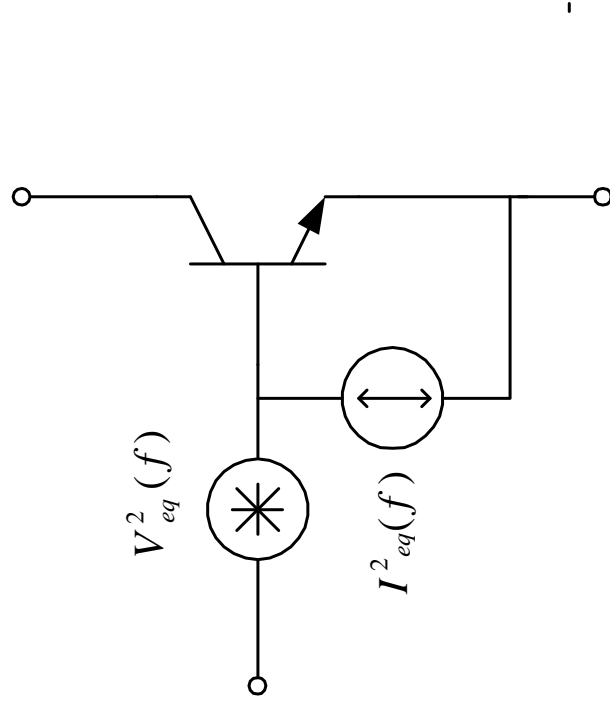
$$S_{\phi}(f_0) = kT (1 + \alpha F) \sqrt{\frac{L}{C}} \left(\frac{1}{Q_{\text{tank}}} \right) \left(\frac{f_0}{\Delta f} \right)^2 \left(\frac{1}{V_{rms}^2} \right)$$

BJT noise sources



$$V_{rb}^2(f) = 4kT r_b \quad I_b^2(f) = 2qI_B + \frac{K_F I_B}{f}$$

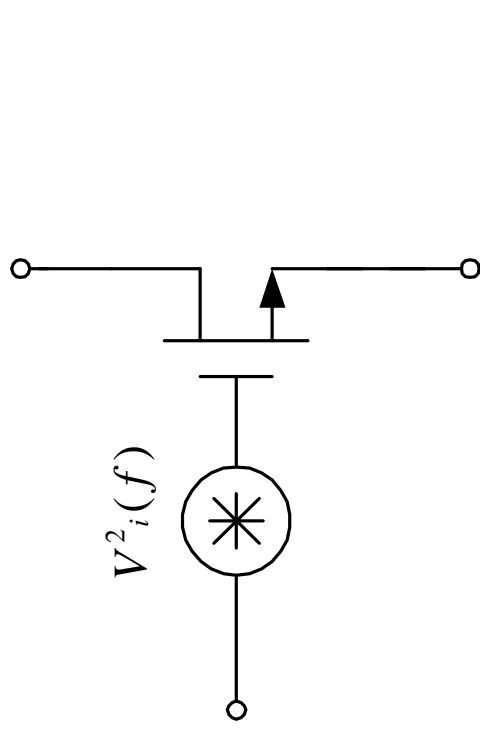
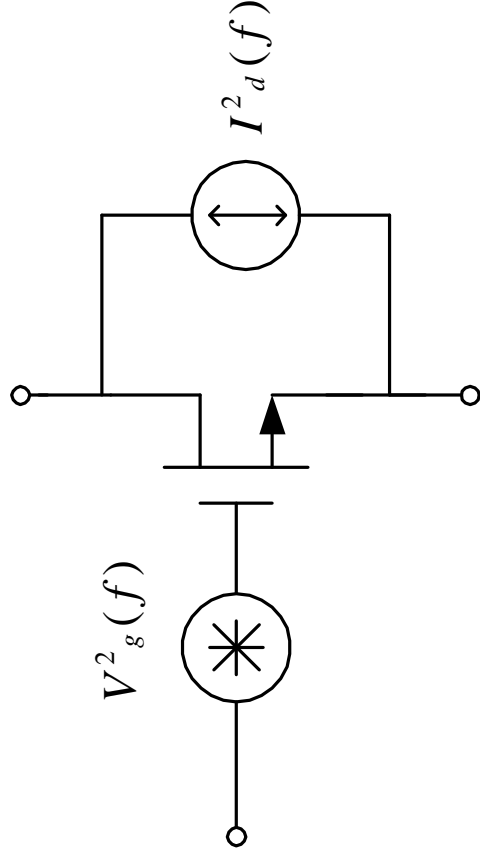
$$I_c^2(f) = 2qI_C$$



$$V_{eq}^2(f) = 4kT \left(r_b + \frac{1}{2g_m} \right)$$

$$I_{eq}^2(f) = 2qI_B + \frac{K_F I_B}{f} + \frac{2qI_C}{\beta(f)^2}$$

MOSFET noise sources



$$V_g^2(f) = \frac{K}{WLC_{ox}f}$$

$$V_i^2(f) = 4kT\gamma\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K}{WLC_{ox}f}$$

$$I_d^2(f) = 4kT\gamma\left(\frac{2}{3}\right)g_m$$

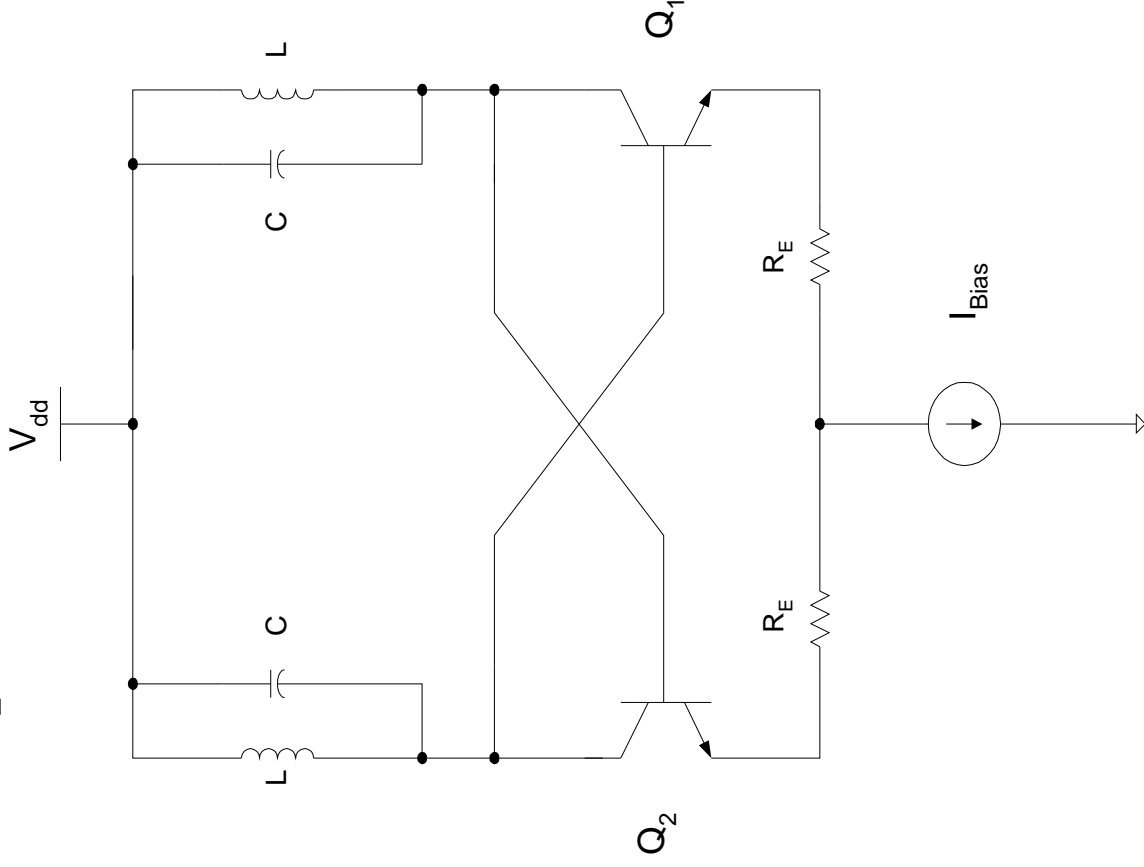
BJT vs. CMOS

- BJTs have less $1/f$ noise than the CMOS transistors. Therefore better phase noise performance is possible with the use of BJT amplifiers generating negative-conductance generators.
- However, increasing the symmetry of the oscillation waveform through the proper design of the amplifier, the up-conversion of the $1/f$ noise can greatly be reduced in CMOS amplifiers, suggesting the viability of the use of CMOS transistors for low noise oscillator design as well, [7].

BJT vs. CMOS

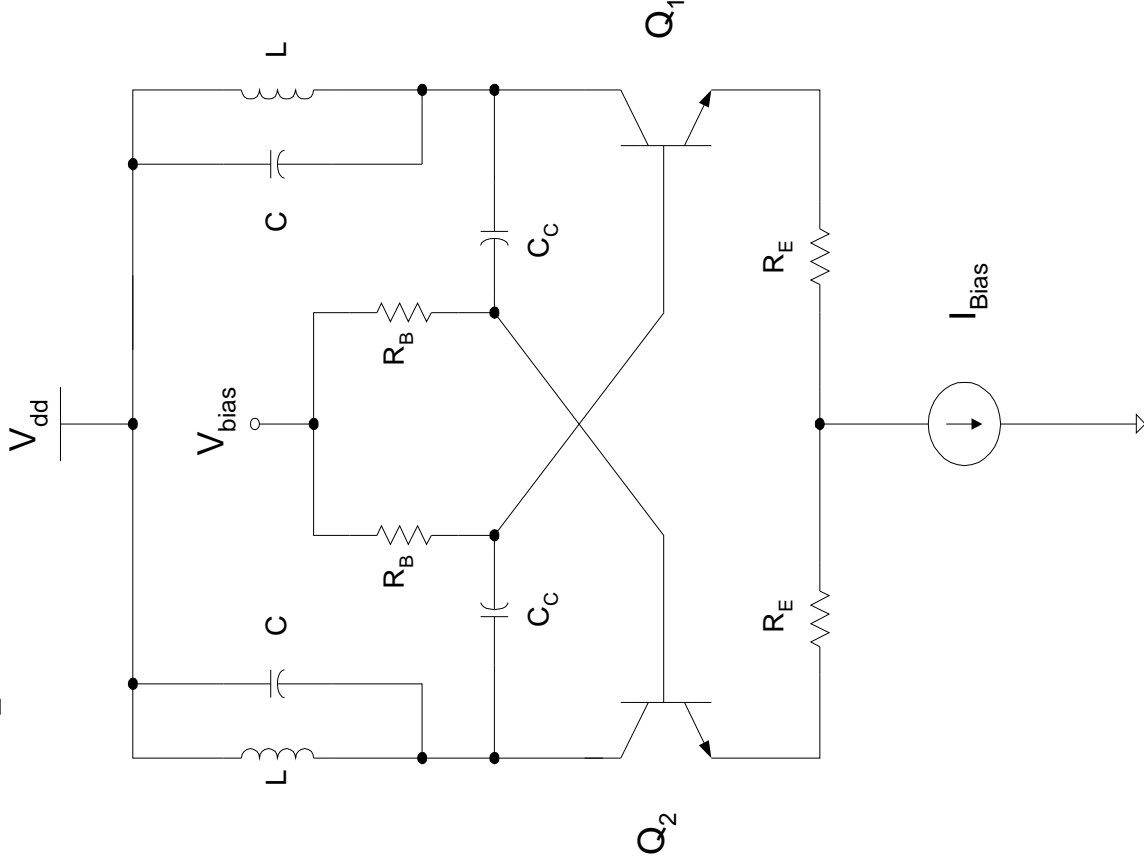
- Large R_b of Bipolar transistors forms a frequency limiting-pole together with the small-signal base-emitter capacitance C_π . This can make high-frequency VCO design more difficult in BJT technologies than in CMOS technologies unless an optimization is done in the process to minimize the base resistance by the technology developers.
- Since the gate resistance of CMOS transistors can always be made arbitrarily small using a large number of fingers in parallel, CMOS oscillators do not suffer from this frequency limit, [1].

Bipolar Oscillator



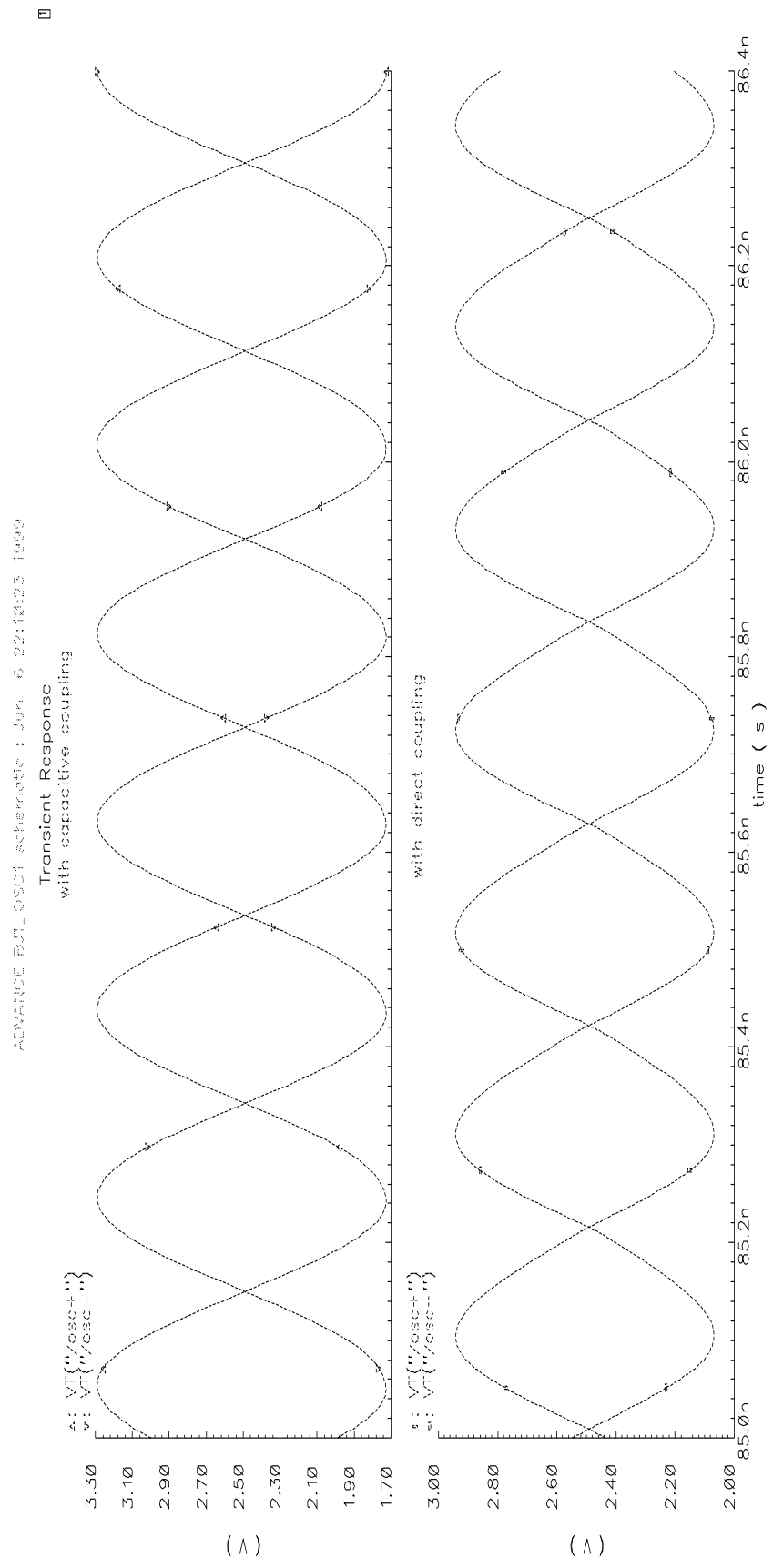
- Simple configuration with direct coupling.
- Amplitude limitation occurs due to the forward-biased CB junction.
- Emitter degeneration is used to linearize the amplifier, which in turn reduces the upconversion of the device $1/f$ noise.

Bipolar Oscillator



- Capacitive coupling is used to alleviate the forward-biased CB junction problem.
- Higher oscillation amplitude is possible, which reduces the phase noise significantly.
- Further increase in the amplitude is possible through adjusting the value of the bias voltage applied to the base terminals.
- Proper design of the capacitive coupling is vital to ensure oscillation.

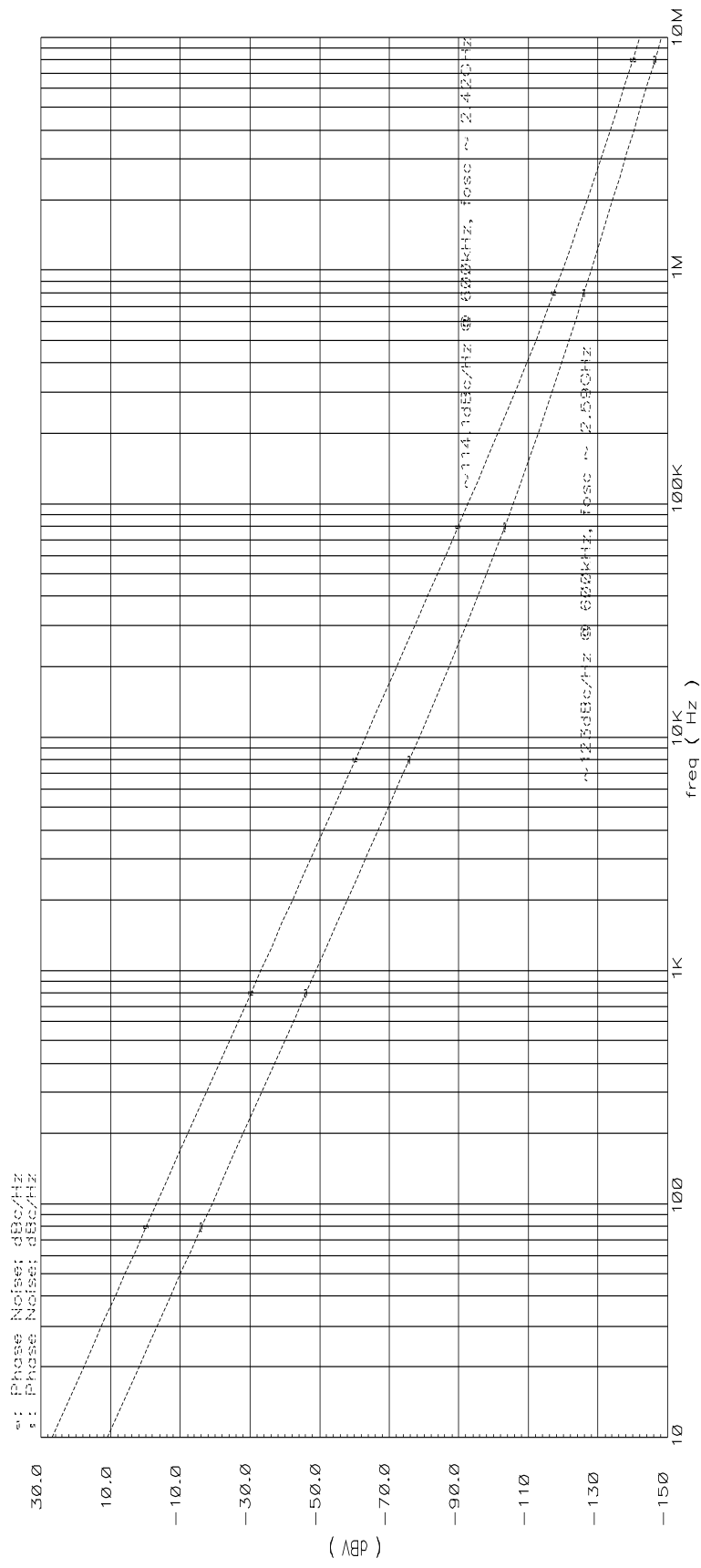
Transient Simulation



Phase Noise Simulation

ADVANCE_EUT_OSCL schematic : Jun 6 22:18:23 1999

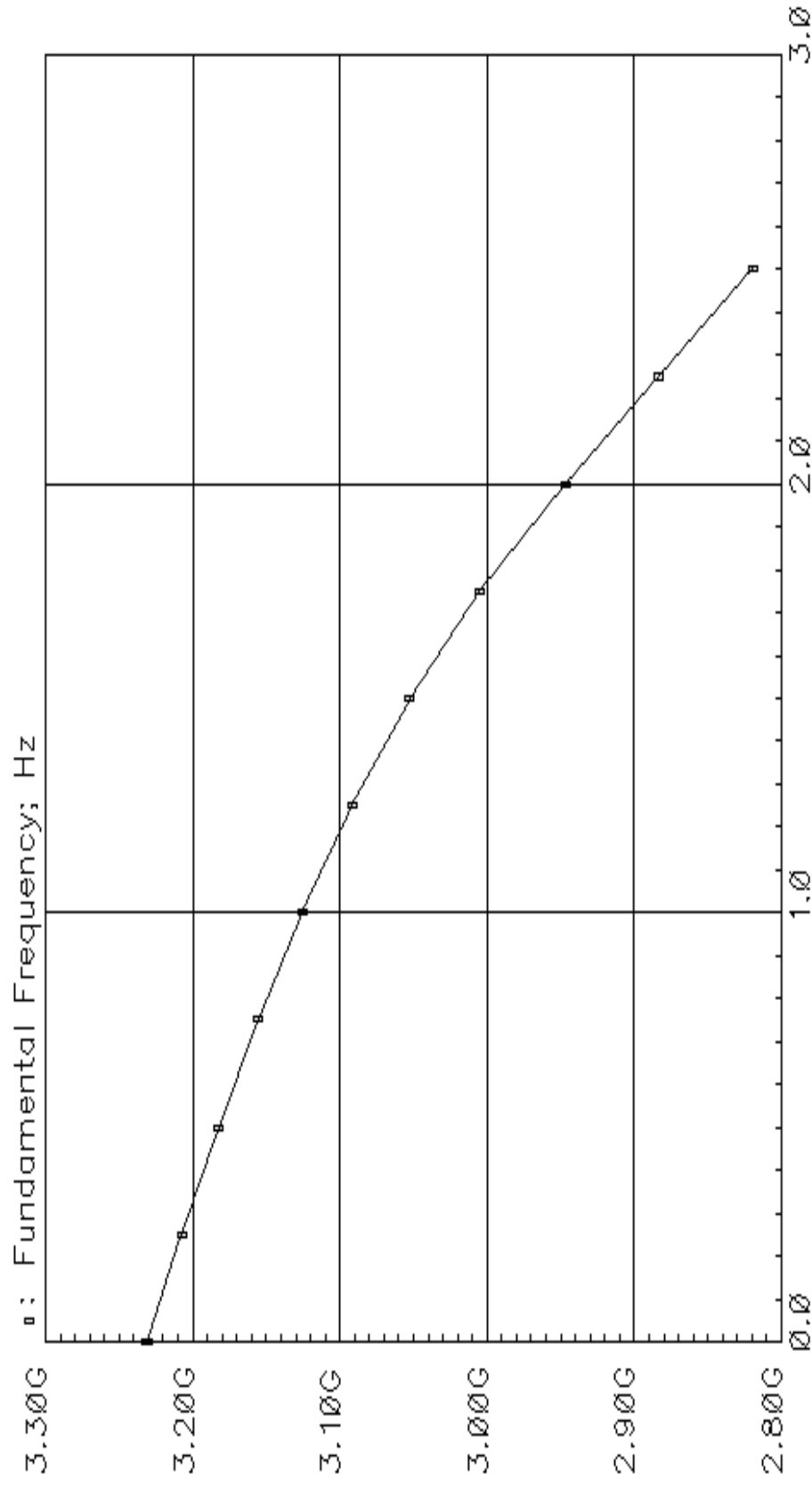
Single Point Periodic Steady State Response



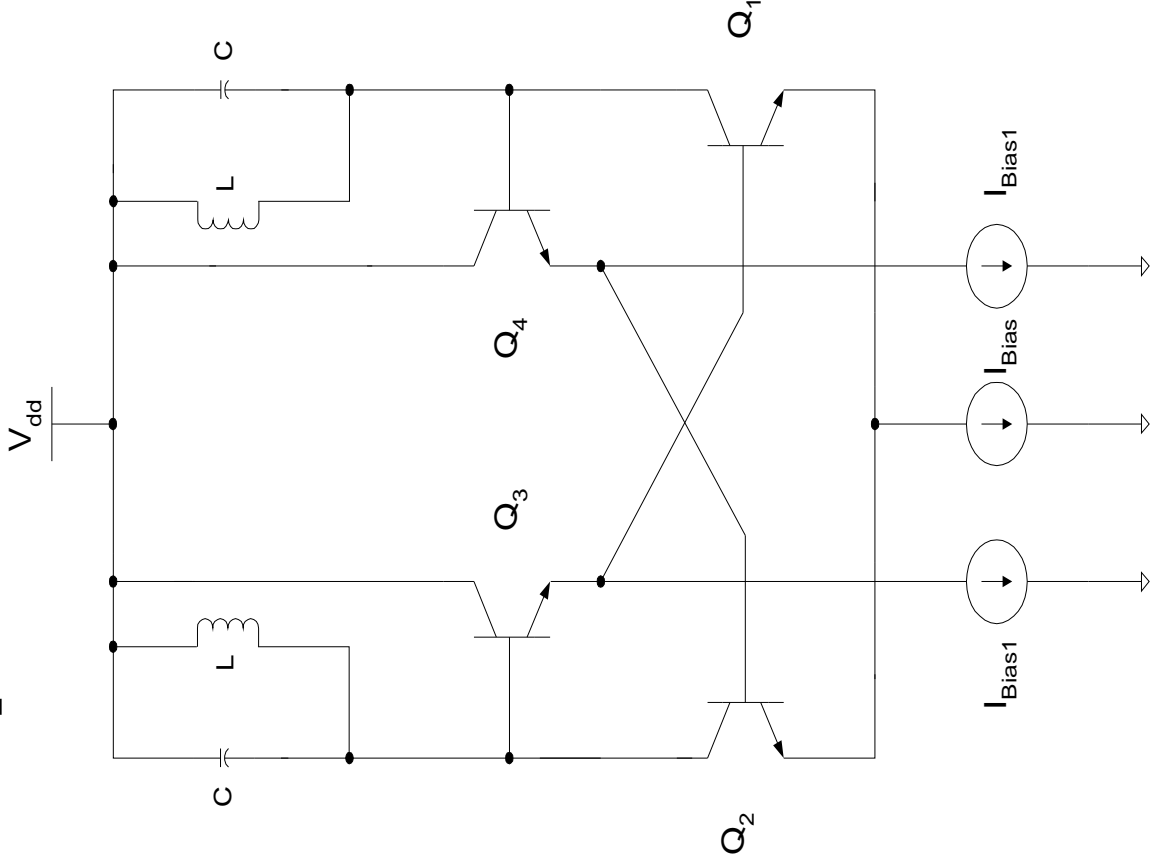
Tuning Range

SYNTHESIZER BJT_OSC3 schematic : Feb 1 17:42:19 1999

Single Point Periodic Steady State Response

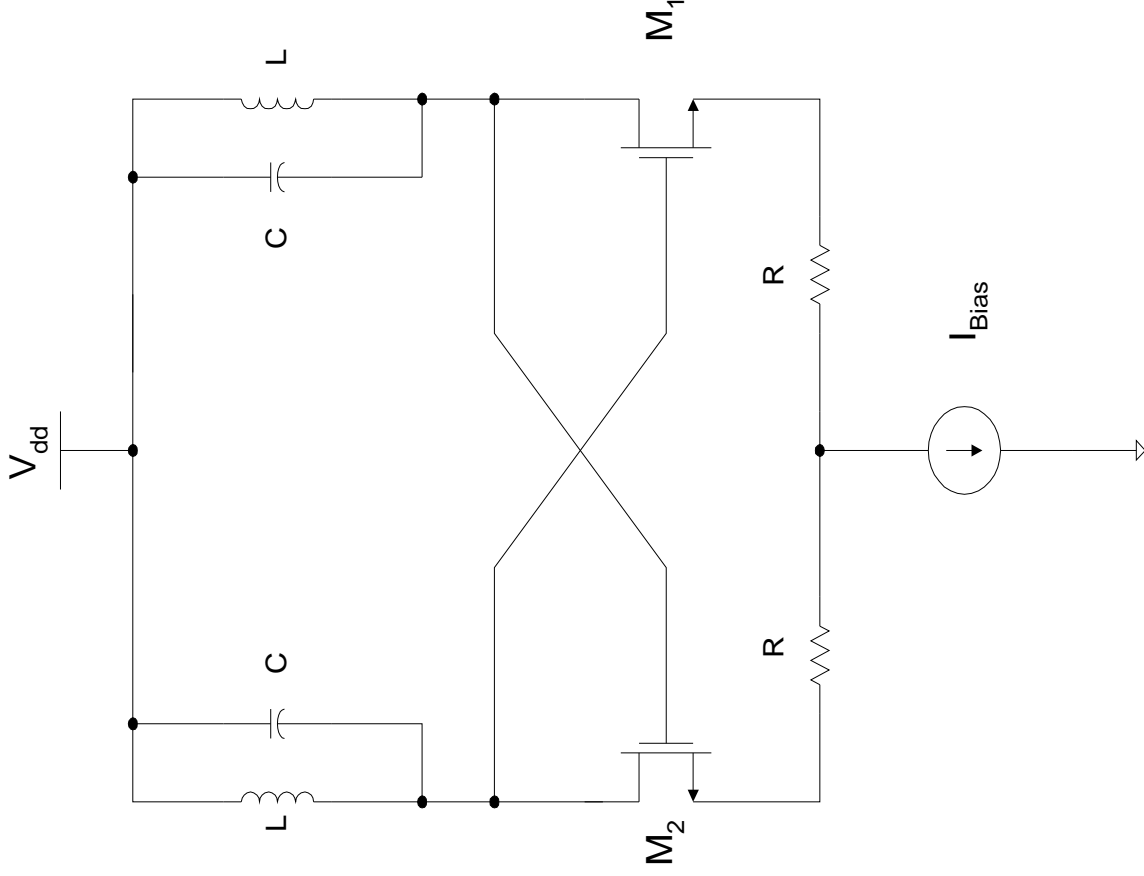


Bipolar Oscillator



- Coupling is through the emitter followers.
- The oscillation amplitude can be quite large as the forward-biased CB junction problem is greatly alleviated.
- The main disadvantages are the increased current consumption due to the additional emitter followers and the increased device noise.

NMOS Oscillator



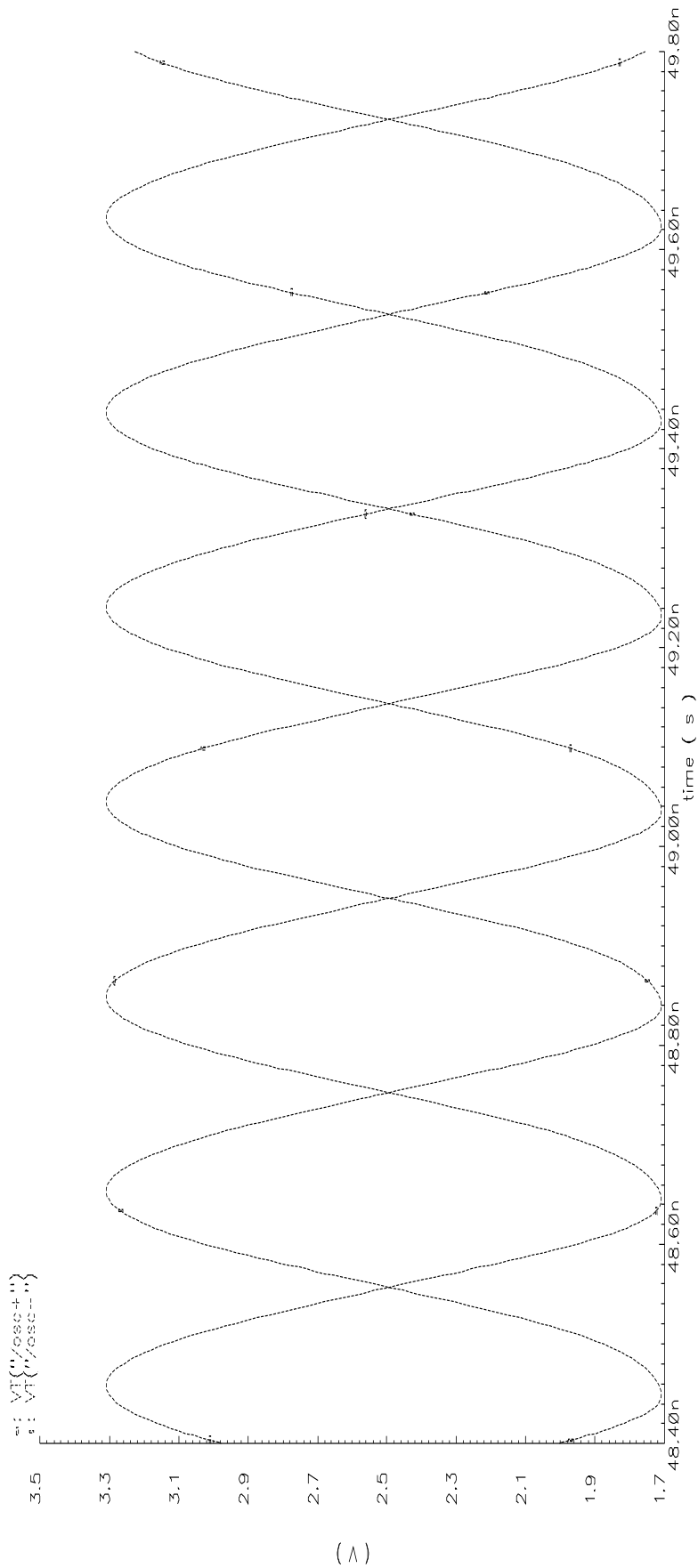
- Direct coupling is possible in the positive feedback amplifier due to the fact that MOS transistors are inherently more linear than the bipolar counterparts.
- Source degeneration resistors reduce the phase noise through linearization.
- $1/f$ noise of the NMOS transistors is an important drawback.

Transient Simulation

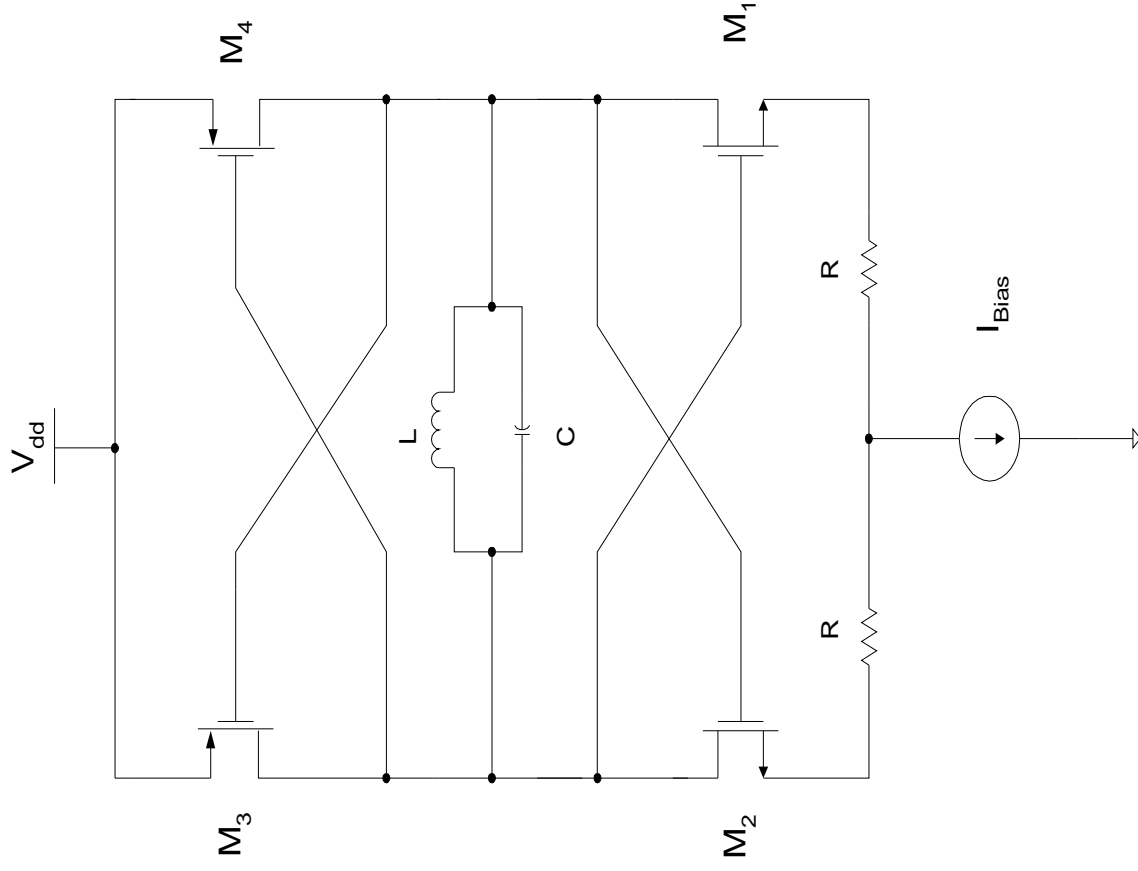
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Transient Response



CMOS Oscillator



- Less current consumption is possible due to the additional pMOS transistors used for negative conductance generation.
- Better waveform symmetry can be achieved through proper sizing of the transistors, [8].
 - Less phase noise due to less $1/f$ upconversion!

Conclusions

- Negative- g_m LC oscillator structures prove to provide the best performance among the integrated oscillators for a given power consumption.
- The main challenge seems to be the immaturity of the integration of the passive tank elements.
- The new advances in the phase noise theory show that the symmetry properties of the oscillating waveform can be exploited to greatly reduce the upconversion of the $1/f$ noise.
 - Thus, low noise RF CMOS oscillators can be as much likely as their Bipolar counterparts with proper design.

References

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