2010 IEEE Dallas Circuits and Systems Workshop
Technical Program

DAY I: Sunday, Oct 17, 2010

1:00 PM	OPENING REMARKS
1:05 PM	**INVITED TALK: Techniques for Fast and Accurate System Level Simulation of Time- Based Circuits Using C++ and Standard Digital Verilog** **Dr. Mike Perrott, SiTime Corporation**
2:05 PM	**INVITED TALK: Ultra Wideband Direct Digital-to- RF D/A Architecture and Circuits** **Prof. Waleed Khalil. The Ohio State University**
3:05 PM	BREAK
3:20 PM	**INVITED TALK: Key Advances in Verification of Nanometer Analog/RF/Mixed- Signal Integrated Circuits** **Dr. Ravi Subramanian, CEO, Berkeley Design Automation**
4:20 PM	**A 110μW Single-Bit Continuous-time ΔΣ Converter with 94.4dB Dynamic Range** Sakkarapani Balagopal, Rajaram Mohan Roy, and Vishal Saxena, Boise State University
4:40 PM	**A Compact Current Steering DAC with Component Swapping Calibration** Kye-Shin Lee and Utthej Nukala, University of Akron, Ohio
5:00 PM	**Accurate Self-Characterization of Mismatches in a Capacitor Array of an All-Digital PLL** Oren Eliezer, Xtendwave, Robert B. Staszewski, Delft University of Technology, Jaimin Mehta, Farooq Jabbar, and Imran Bashir
5:20 PM	SESSION END

Technical Program (Continued)

DAY II: Monday, Oct 18, 2010

8:30 AM REGISTRATION / BREAKFAST / POSTER SETUP

9:00 AM OPENING REMARKS

9:05 AM **INVITED TALK: Design for Resilience in Beyond-22nm CMOS and 3D-IC**
Prof. David Z. Pan, University of Texas at Austin

10:20 AM BREAK

10:35 AM **INVITED TALK: Robustness and Resiliency in Data Conversion**
Prof. Yun Chiu, University of Illinois at Urbana-Champaign

11:35 AM LUNCH and POSTER SESSION

12:45 PM **Device Physics Origin and Low-Cost Solutions to Threshold Voltage Fluctuations in sub 130nm CMOS Incorporating Halo Implant**
Hal Edwards, Tathagata Chatterjee, Mohamed Kassem, Gabriel Gomez, Frank Hou, and Xiaoju Wu, Texas Instruments

1:05 PM **Optimizing Gate Reticle to Si Flow for Variability in Sub-threshold Circuits**
Ashesh Parikh and Mak Kulkarni, Texas Instruments

1:25 PM **INVITED TALK: Nanometer Era Physical IP Process-Design Challenges**
Dr. Greg Yeric, ARM

2:40 PM BREAK

2:55 PM **Design of Power-Optimal Buffers Tunable to Process Variability**
Mario Lok, He Ku, University of Texas at Austin, Murari Mani, AMD, Constantine Caramanis and Michael Orshansky, University of Texas at Austin

3:15 PM **Design Automation Tools and Libraries for Low Power Digital Design**
Mohammad Rahman, Ryan Afonso, Hiran Tennakoon, and Carl Sechen, UTD

3:35 PM **Structural Verification of a WLAN System Using Simple BiSTs**
Dallas Webster, Jesus Cavazos, Paul Patchen, Dolev Guy, Texas Instruments, and Donald Lie, Texas Tech University

3:55 PM **A Reduced-Cost Built-in Self Test for an FM Receiver**
Deepa Mannath, Victor Montano-Martinez, Ioannis Syllaios, Sumeer Bhatara, Mahita Attaluri, Zahir Parkar, Texas Instruments, and Simon Ang, University of Arkansas

4:15 PM BEST PAPER AWARD and CLOSING COMMENTS

List of Papers in Poster Session (Monday, 11:35 AM – 12:45 PM)

1 Low Overshoot, Low Dropout Voltage Regulator with Level Detector
Ralph Oberhuber and Rahul Prakash, Texas Instruments

2 0.6-2.0 V, All-CMOS Temperature Sensor Front-End Using Bulk-Driven Technology
Scott Block, Yiran Li, Texas Tech University, Yi Yang, University of North Carolina, and Changzhi Li, Texas Tech University

3 Performance Robustness Analysis of VLSI Circuits with Process Variations Based on Kharitonov's Theorem
Liuxi Qian, Dian Zhou, University of Texas at Dallas, Sheng-Guo Wang, University of North Carolina at Charlotte, and Xuan Zeng, Fudan University, Shanghai, China

4 Clock Skew Automation for Area and Power Reduction in Deep Sub Micron Designs
Yasaswini Sudarsanam and Anand Rajagopalan, Texas Instruments

5 A Dual Device Load Board with Dual Switched Printed Baluns
Claudio Montiel, Texas A&M University, Kingsville and Parkash Arora

6 Self-Calibration of a Digital Pre-Power Amplifier in a Polar Transmitter
Jaimin Mehta, Xtendwave, Imran Bashir, Vasile Zoicas, Texas Instruments, Oren Eliezer, Khurram Waheed, Mitch Entezari, Scott Larson, Darshan Shrestha, Sameh Rezeq, Robert Bogdan Staszewski, TU Delft, and Poras Balsara, UTD

7 Low Frequency Noise in 45nm Technology Based Bandgap Circuits
Purushothaman Srinivasan and Andrew Marshall, Texas Instruments

8 A Supply Insensitive Resistor-less Bandgap Reference with Buffered Output
Venkatesh Acharya, Texas Instruments and Bhaskar Banerjee, UTD

9 Automated Gm-C Filter Design: A Case Study in Accelerated Reuse of Analog Circuit Design
Sankalp Modi, Syed Askari, Sujan Manohar, Poras Balsara, and Mehrdad Nourani, UTD