IEEE Dallas Circuits and Systems Workshop 2010 (DCAS 2010)

Design Automation, Methodologies, and Manufacturability

October 17-18, 2010
The University of Texas at Dallas
http://www.ewh.ieee.org/soc/cas/dallas/wks2010/

Call for Participation

The increasing complexity and level of integration in today's devices and systems, combined with pressure to reduce design efforts and production costs, demands improvements in design and productization methodologies. The Dallas Chapter of IEEE Circuits and Systems Society is conducting a two-day workshop to provide a forum for sharing recent work and ideas in these fields.

The workshop will be held on **October 17-18, 2010** in the Erik Jonsson School of Engineering and Computer Science at **The University of Texas at Dallas**.

Technical Program

The two-day workshop will include 6 invited tutorials to be given by recognized experts from industry and academia. 8 selected technical papers will be presented by their authors from industry and academia and a dozen of additional papers will be presented by their authors during a poster session. The workshop schedule may be found at the website above. **The workshop is designed for the particular benefit of engineers and managers in design, product, and test groups.**

Registration Details

IEEE Member: $190
Life Member: $50
Non Member: $250
Student: $50

Registration Website:
http://ewh.ieee.org/soc/cas/dallas/wks2010/

Invited Tutorials

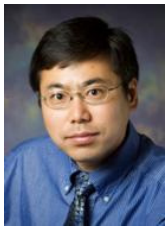
Dr. Ravi Subramanian
CEO
Berkeley Design Automation

Key Advances in Verification of Nanometer Analog/RF/Mixed-Signal Integrated Circuits

Prof. Waleed Khalil

The Ohio State University

Ultra Wideband Direct Digital-to-RF D/A Architecture and Circuits



Prof. Yun Chiu

University of Illinois at Urbana-Champaign

Robustness and Resiliency in Data Conversion

Prof. David Z. Pan

University of Texas at Austin

Design for Resilience in Beyond-22nm CMOS and 3D-IC

Dr. Mike Perrott,

SiTime Corporation

Techniques for Fast and Accurate System Level Simulation of Time-Based Circuits Using C++ and Standard Digital Verilog

Dr. Greg Yeric

ARM

Nanometer Era Physical IP Process-Design Challenges

Organizing Committee

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