Components, Packaging, and Manufacturing Technology Society Newsletter

The Global Society for Microelectronics Systems Packaging

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PRESIDENT'S REPORT

Another very successful BOG meeting and ECTC in Orlando. I 'm happy to tell you that we had a very successful BOG and ECTC conference last week in Orlando, Florida.

The BOG (Board of Governors) tackled the problems of finances and budgets. In spite of IEEE's massive charges to our CPMT Society, the Board has come up with a budget in excess of $500K to drive our strategic initiatives. As a result, we have funded marketing and promotion, International chapters, Faculty Fellowships to develop four more courses this year and next, distinguished lectures, student programs, awards and others. I'm also very happy to tell you that your Board voted to proceed with funding of a Field award in Microsystems Packaging. This should help tremendously in publicizing what "Packaging" is and what our society does in this area. This award will help obtain international attention to CPMT.

Congratulations to all our Awardees

Congratulations to John Stafford for the David Feldman Award, George Harman for Sustained Technical Achievement award, Charlie Lee for Young Engineer of the year award, and Singapore and Hong Kong Chapters as the best Chapters . We had unprecedented number of IEEE Fellows-a total of eight from CPMT Membership. They include Evan E. Davidson of IBM, Daniel De Zutter from University of Ghent, Robert Forrest Kwasnick of General Electric Medical Systems, Chin Chung Lee from University of California Irvine, Wolfgang S. Menzel from University of Ulm in Germany, Luu T. Nguyen of National Semiconductor, Herbert Georg Reichl from Technical University of Berlin, and David B. Tuckerman of CMEA Venture.

ECTC continues as the flagship conference of CPMT Society The ECTC has been a great success in spite of the economic downturn. The total number of attendees were 920 from 23 countries. A total of 400 participated in short courses. The total number of papers presented was 450. The attendees seem to like the quality of papers and the global network that ECTC provides.

I would like to thank the organizing committee of ECTC under the leadership of Pete Slota. Start your plans to attend next years May ECTC in San Diego, this is one of the easiest ways of maximizing your benefits from CPMT.

-- Rao Tummala, President CPMT Society

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Chair Tony Mak leading his breakfast meeting at ECTC

TC-9 Thermal Management and Thermomechanical Design

Tony Mak, Chair of CPMT "Thermal Management and Thermomechanical Design Technical Committee" held a breakfast meeting on Thursday at the Wyndham Palace at Disney World. Tony showed everyone the updated handbook pages for TC-9. He announced the deadline for the TC-9 Newsletter was June 15th.

There was discussion on the success of the San Jose Semi-Therm meeting. The need to add a poster session was reviewed. An evening workshop on Thermal Aspects of Opto-electronic Packaging was mentioned. The "Thermi Paper Award" was won by Clemen Lasance, and the Outstanding paper award went to Linan Jiana.

The 2002 I-Therm meeting will be in the second half of the week as ECTC meetins in San Diego. The Program Program Chair is Christina Amam. More information can be found at itherm.org. The Due date for abstracts is August 15, 2001.

The next Semi-Therm meets in March 2002 with the deadline for abstracts is September 17. the web site is thermengr.com.

Kouchi reported on the 2001 EuroSimE held in Paris on April 8-11. This was the second time it was held and about 100 engineers participated. Most were from Europe but there was international representation. This is the only conference which concentrates on the Thermal-Mechanical concerns, with 50 presentations addressing solutions.

There was some discussion on how EuroSimE and Therminics workshops work together. In both cases Paul Wesling guides the Proceedings through IEEE system. Both events need more volunteer help particularly fro TC-9. In addition, more U.S. involvement should be sought.

Avi-Bar Cohen is now the Distinguished Lecturer for this Technical Committee. Among other things this means that Chapters and Universities can request CPMT help in having Avi speak at their events.

Goram Matijasevic discussed the thermal aspects of the NEMI roadmap which he helped put together. He described the sea change from the past when no one thought hand held applications could possibly have thermal problems. However, as batteries have improved and chips have shrunk in size, 5 watt operation often demands innovative solutions. Another big roadmap challenge is the 300 W microprocessors scheduled for 2012.

TC-12 Technical Committee on Electrical Design, Modeling, and Simulation

The technical committee has been quite involved in organizing its first workshop. This meeting will be held in conjunction with the key conference in the area of electrical analysis and design that TC-12 participates heavily in. The first Future Direction in IC and Package Design workshop will be held the day before the start of the 10th Topical Meeting on Electrical Performance of Electronic Packaging, ECTC'2001, on October 27, 2001, in Cambridge, MA. The meeting will bring together experts in the university and industrial communities and will provide a forum to address the future requirements and developments associated with the design of next generation ICs and packages. Six distinguished speakers were invited to cover a broad range of concerns such as: system design, low-power system trade-offs, chip-scale-packaging, RF packaging requirements, optical interconnections, and field solvers for full-chip or full-package. The invited speakers are representing major research laboratories, companies, and universities from the US, Europe, and Asia. We expect that a large portion of the EPEP'2001 conference will also join the workshop and useful discussions and interactions will take place between the attendees.

The workshop was entirely organized by the TC-12 committee with the technical guidance and support of the Vice President for Technical Activities, Philip Garrou. We would also like to acknowledge the support of the Vice President for Conferences, James Morris, and the Executive Director, Marsha Tickman. Updated information will be posted at www.epep.org and www.cpmt.org/conf/fdip01/fdip.html. Those who are interested in attending the workshop are urged to register with the hotel early in order to take advantage of the discounted room rates offered to the EPEP'2001 attendees.

TC-12 has also been involved in identifying three distinguished lecturers in the area of electrical design, modeling, and simulation. These speakers have extensive experience in the area of packaging in the industrial and academic communities and are recognized for their accomplishments in the field. TC-12 is very strongly endorsing them for any interested forums that would like to use them. Such parties can contact the vice President for Education, Albert Puttlitz or the Vice President for Technical Activities, Philip Garrou, to make the necessary arrangements. The talks that could be offered are as follows:

*George Katopis, IBM: Corporation: "Package design approaches for single pass error free designs", and "System architecture impact on Package Cost Performance"

*Luc Martens, University of Ghent: "Advanced testing for electronic interconnections and packages in high-speed systems"

*Paul Franzon, North Carolina State University: "Future perspectives in Signal Integrity Design and Management" ---Submitted by Alina Deutsch, TC-12 Vice-Chair, Madhavan Swaminathan, TC-12 Chair.

TC-16: RF and Wireless

(TC-16 provides a network with the elite that worry about RF components, packaging and microsystems. This activity is in its second year and would benefit from more active volunteers. Call Craig Gaw to join the team.)

Technical Scope:
The design, development, & technology of RF & wireless components, devices, circuitry & systems.

Topics of interest include:
o Technology of packaging active/passive hybrid and integrated RF & wireless components
o Electrical and physical design; reliability, performance and characterization
o Reliability, reliability physics, failure analysis, degradation models, thermal analysis, simulation, modeling, characterization & prediction, assembly techniques, low noise issues
o Materials (reliability without hermeticity, adhesives, ceramics, plastics, glasses, metals, solders, films, encapsulants, sealants, molding compounds, etc.)
o Processing (bonding, brazing, welding, soldering, sealing, molding, flip-chip, chip-on-board, etc.)
o Devices and Components (RF & wireless modules, amplifiers, transmitters, receivers, MMICs, FETs, HEMTs, HBTs, MEMs, connectors, passive components, etc.
o Systems and Manufacturing (components, design, assembly, reliability, automation)

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Key Conferences:
Planning initiated by Prof. Manos Tentzeris of Georgia Tech for TC-16 sponsored workshop in the "RF & Wireless" technical area.
TC-16 supports ECTC's Components Group

Key Conferences Sponsored by Other Societies:
**International Microwave Symposium sponsored by MTTS
**GaAs IC Symposium sponsored by EDS, MTTS & SSCS
**GaAs Reliability Workshop sponsored by JEDEC, IEEE & EDS

Suggestions for "RF & Wireless" Technical Committee

Conference/Workshop Participation:
Planning initiated for TC-16 sponsored workshop. (Manos Tentzeris is key organizer) In conjunction with ECTC's Components Committee, TC-16 plans to organize a special session/symposia each year for ECTC. (Matt Schwiebert was key organizer for ECTC 2001)

Journals / Publications in "RF & Wireless":

Craig Gaw, Chair

IEEE Transactions on Microwave Theory & Techniques
IEEE Transactions on Electron Devices
Microwave Applications
Microwaves & RF
RF Design

Short courses:
"RF/Wireless Packaging: Status & Challenges", ECTC 2000 & 2001
Manos Tentzeris & Joy Laskar, Georgia Institute of Technology

Activities for past year:
Assisted ECTC Components Committee with review of RF papers submitted to ECTC 2001.
Obtained 2 papers on RF MEMS for Components Committee session at ECTC 2001.
Manos Tentzeris (TC-16 vice-chair) & Joy Laskar presented course on "RF/Wireless Packaging: Status & Challenges" at ECTC 2000 & will present course again at ECTC 2001.
Manos Tentzeris organized & chaired "Cellular & Wireless" session for TC-14's "System Packaging Workshop" (May 8-10, 2001 in Scottsdale, AZ). He also investigated what is required to organize a workshop.
Recruited additional technical committee members.
David Palmer set up the TC-16 web page & keeps it updated.

Goals for upcoming year:
Organize & hold workshop.
In conjunction with ECTC Components committee, TC-16 will organize a special symposium for ECTC 2002.
Broaden representation on technical committee by recruiting new members from key organizations doing R&D within technical scope of "RF & Wireless" technical committee.
Maintain & update web page.

TC-5 Chair Rajen Chanchani talking with Jim Morris (VP Conferences) and C. P. Wong (TAB representative) about next year's Advanced Packaging Materials Conference.

TC-5 Meets During ECTC

Chair Rajen Chanchani of the Materials and Processing Technical Committee held an organizational breakfast meeting during the Orlando ECTC. The team talked about the upcoming Advanced Packaging Materials Conference to be held in Atlanta on March 3 - 6, 2002. This will be the first year this conference will be sponsored 50/50 by IEEE-CPMT and Georgia Tech.

In addition, the globalization of TC-5 Committee was discussed. In the future there will be two TC-5 meetings, one in the U.S. (in conjunction with ECTC) and the other either in Asia or in Europe in the Autumn. To assist in this globalization effort, an online community of people interested in TC-5 activities will be established by creating a list of addresses under a "MAJORDOMO". The goal is to make this the forum of choice for communicating "great" ideas aimed at specific member concerns on packaging materials and processes with each other.

-- Rajen Chanchani

Rajen Chanchani of Sandia Labs, C. C. Lee University of California Irvine, Eric Perfecto of IBM, Bill Brown of University of Arkansas, Charles Lee of Singapore Chapter.

CPMT Awards for the Year 2001

IEEE CPMT Awards Committee is pleased to announce the winners of the following CPMT awards for the year 2001:

David Feldman Outstanding Contribution Award: John Stafford (formerly with Motorola, Inc.) for his outstanding service to the CPMT Society in various roles, and for his technical contributions over 44 years, most of them in the fields encompassed by the CPMT Society.

Outstanding Sustained Technical Contributions Award: George Harman (NIST) for his significant contributions to the microelectronics field and for mentoring electronic packaging community in the area of wire bonding technology.

Electronic Manufacturing Technology Award: Walt Trybula (SEMATECH) for his numerous contributions to manufacturing technology, especially in the development of models and simulation tools which have had and will continue to have significant impact on

Outstanding Young Engineer Award: Charles Wee Ming Lee (Infineon Technologies, Singapore) for his outstanding contributions to electronic packaging technology and for his service to the CPMT Society, in particular to the CPMT Chapter, Singapore.

These awards were presented to them at the 51st ECTC in Orlando, FL, on May 31st. Please visit the website http://www.cpmt.org/awards.html for information about these CPMT awards.

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E. Jan Vardaman, Board Member at Large, and Phil Garrou, Vice President of Technology network at ECTC.

Your Board of Governors Ignores Distractions

It was Memorial Day at Disney World. Everyone in the hotel was going to the theme parks. Everyone except the 35 Society volunteers that found a room without windows and held a Board of Governors meeting.

The meeting started with a boisterous discussion on the economic plight of the central IEEE organization. Because of decisions in the distribution of the library payments for IEEE publication made almost 10 years ago, the income to Headquarters has dried up and the Societies are now rich. However, despite this history, everyone had a great time lecturing on the virtues of thrift for headquarters and conspicuous consumption by the newly rich Society. The bottom line is that our Society will transfer about $600K to Headquarters so they can get rid of their red ink. In addition all future budgets will be balanced at the Institute level and will show a surplus at the Society. Every service a Society or member uses will be paid for directly so that deficits will not sneak up on any part of the organization. Part of the confusion comes from the many new services (IEEExplore, web conference and newsletter sites, job postings...) which are just beginning to develop users.

Ralph Wyndrum, IEEE Director of Division I, explained the new direction of IEEE and how it will effect CPMT. For one they are targeting new technology trends more aggressively than in the past. A number of the new technologies directly impact CPMT. Of most immediate interest is the concentration of Microsystems (System on chip, System on Package). There is no desire to start a new Society or Council, IEEE already has too many. But there is an opportunity for several societies to back a TC or a Transaction and lead the parade.

Anthony Chan, Administrative Vice President, pointed out that there were 9 billion web pages today with 7 million new ones by the end of the day. So any particular CPMT web page is not going to be found by chance but only by systematic linking. He suggested using the standard XML and is looking for a web master who wants to soar.

George Harman, Chair Fellows Committee, said that this year CPMT did submit the appropriate number of nominations to Fellow of the Institute after looking like only 3 would be submitted a week before deadline. There was some discussion of having a search committee be active earlier this year. He predicted that of those submitted through our Society about 3-5 will make the cut this year. There will also be about 3 others that are in our Society but are submitted through other Societies. (Editor note: any member active for a number of years in CPMT, an educator, or application engineer should convince a colleague to help assemble a nomination package. Don't wait to be tapped on the shoulder.)

C. P. Wong reported that about 500 attended the Surface Mount Conference in Nuremberg Germany from April 23 - 26.

Phil Garrou reviewed the Technical Committee that have lost vital signs. TC-6 on high end PWBs has lost all active members to other IEEE activities or to economically challenged job positions. There will be one more attempt to revive it and then it will be sidelined for a while. The MEMs and Sensor Packaging group, TC-17 has no chair do to the frenzy in these fields. TC-20 Bio-Electronics Packaging has proved to be a market place of very competitive companies that do not want to share anything on the pre-competitive or professional level (at least at this time).

Paul Wesling, VP of Publications, described the initial success with tracking Transaction articles in the review process in new software, Manuscript Central. This was the most visible step in our attempt to remain the "publisher of choice" to active members of our profession. Paul wants to expand our publications to include audio lectures, simulations, and tutorials and not just "papers". For example, CPMT owns software that can turn a power point presentation into a web streaming audio synchronized with paging view graphs. He sees the publication job stopping when brief introduction lectures are available to our members on most of our subjects. For digging deeper into the material members will need the services of our Education group or IEEExplore to find the original papers of interest.

He described the difficulty of getting the web version of the Transactions in color. He also described the tension between providing publications in paper, CD-ROM, or on the web. For example, CPMT has a CD set that has all the transaction in it and it is beginning to

Board meeting luncheon. Here is an an excellent opportunity to find out how other companies are doing, to verify your ideas of where technology is heading, and to establish strong professional networks (from left): Johan Liu, Anthony Chan, Ron Gedney, Merrill Palmer, Peter Slota, Jim Steele

sell. We may want to add the last year of Transactions and an updated index to it and sell it to the media wise members. He noted that all conference proceedings were going to CD-ROM and CPMT is keeping them in the Book Broker program so that people who missed the conference can still get a copy.

Koji Nihei, Member at Large from Waseda University, gave the Japan Chapter report to the Board. Koji indicated that the formerly named IEMT/IMC Symposium has become the ICEP - International Conference on Electronics Packaging. It will meet April 17 - 19 in 2002 in the Tokyo R yutsu Center. This year's technical meeting with 96 papers attracted 330 people and the 70 exhibits attracted 13,000 visitors.

Al Puttlitz, Education Vice President, was glowing with the imminent success of the 13 short courses ready for the next day. The thirteen courses were attracting about 400 students. All time popular courses were being professionally converted to CD-ROM courses by IEEE media department instead of the originally intended web course. Market tests had indicated members preferred the CD-ROMs to on-line courses. The input materials supplied were the same.

Rao Tummala, CPMT President and Chair of education sessions at ECTC, discussed the curriculum development that had occurred from 1997 through last year. Our society had invested $120K to the $120K of PRC Georgia Tech plus the $120K NSF. Although this total is small compared to the money used to develop multimedia courses by international companies, quit a bit of progress has been made. A number of good teaching modules are already available: Sensors and a PWB virtual fab lab from T. U. Budapest by Ilayfalvi-Vilez and Peter Gordon, Thin Film virtual lab from Gary May of GIT, Signal Integrity by Jose Schutt-Aine at University of Illinois, and Electronic Packaging Modeling and Simulation by Dr. Bruce Kim from ASU. These modules seem to be an unintended best kept secret. But any member can go to [www.cpmt.org] and click on [education] in the list on the left...and there is a list of modules completed to date. Everyone agreed to encourage completion of existing coursework, transfer of completed work to CD-ROM, and lighting a fire under members to start using them for continued education.

Kanji Otsuka presented a long list of suggestions to improving the interaction between the 10,000 Japanese engineers that should be active in CPMT and our organization. Examples included a Japanese column on the CPMT web site, an introduction in Japanese to conference papers, and more discussion of Japanese component and packaging activities within CPMT publications. One big shift is the technology center has shifted from the large companies to the Japanese Universities and National Labs. CPMT used to have support in the large companies but this means little now.

John Segelken, Chair Nominations, mentioned that the BOG reelection process is starting. (see article elsewhere in Newsletter).

Bill Brown, Chair Student Chapters, announced that the Georgia Tech and Romanian student chapters have been approved. The China and University of Arkansas were undergoing the approval process. Student Sharath Mekala gave a brief description of how the student chapter at Georgia Tech helped with the education process.

Ralph Russell, Membership Chair, discussed how the membership in CPMT gained 7.4% in one year (May to May, 3385 --> 3637). This makes CPMT the 3rd fastest growing Society. Other Societies offer free membership or lifetime membership as techniques to drive their numbers higher. The approach long used by your Society is to provide more and more membership opportunities so most renew their membership and tell their colleagues to join. The number of casual members is not as important as the number of CPMT active and networked members.

Lunch table brainstorming (from left) Kanji Atsuka, Ralph Russell, Phil Garrou, Jan Vardaman, Craig Gaw, Ralph Wyndrum, Rao Tummala, James Morris

There are now 35 Chapter for CPMT. Most of these chapters are outside of North America indicating an active global organization. There are strong possibilities of new chapters opening in Shanghai, Denmark, Ireland, Spain, Mexico, and Israel.

Connie Swager, Marketing Director, reported on what her Marketing Committee had determined with the professional Potomac Communications

Group. A large percentage of CPMT's discretionary budget will be used in these efforts over the next 18 months. Several examples of initiatives include: getting CPMT publicity in the many magazines component/ packaging / manufacturing engineers read, having a short and long list of member benefits including more chances to network with other volunteers, more visibility to awards given by CPMT, more communication with the 10,000 potential members that only flirt with IEEE.

Merrill Palmer, CPMT Treasurer

Treasurer's Report

The March 2001 CPMT Newsletter reported a CPMT operating surplus of $ 365K for the year 2000 but a $417K Reduction of Reserves at year end to cover the Institute-level deficit. Final numbers after all accounting adjustments are $365K surplus, $383K Reduction of Reserves.

CPMT financial performance for 2001 is pretty much tracking the budget except that Transactions revenue and net are down by 18% and 12%, respectively, and a number of CPMT committees are underspending relative to budget. A Reduction of Reserves in excess of $600K is projected for 2001.

The unwelcome reduction of the reserves held by IEEE Societies to cover Institute deficits resulted from several factors that have at last been addressed by the IEEE Board of Directors with tough ground rules for 2002 budgets. Overall IEEE budgets will non-deficit in 2002, even with much lower assumed return on reserves than has previously been budgeted. All IEEE entities must improve their financial bottom line enough that the overall budget is balanced. For CPMT, this means constraints on some of the spending that we were considering.

Still, the 2002 CPMT budget approved by the Board of Governors at their meeting this Memorial Day maintains key services to members, implements Document Central electronic processing and tracking of Transactions papers, includes a marketing thrust to provide greater CPMT recognition, influence, and effectiveness in our technology fields of interest, and continues the strategic thrust efforts that define the direction and future of CPMT.

-- Merrill Palmer, CPMT Treasurer

CALL FOR CANDIDATES

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of this Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways -- either by the Society Nominating Committee, or by petition.

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can automatically become a candidate via petition by following the procedures below. The term of office for this election is 1 January 2002 through 31 December 2004.

** Prepare a petition that contains your name, member number, and statement of your qualifications for office.

** Provide lines for signatories. Each line should include space for a printed name, member number, and signature.

** Have the petition signed by a MINIMUM of 25 CPMT Society members in good standing (Student grade members are not eligible to sign.)

Membership status of all signatories will be validated. It is suggested that you gather more than 25 signatures in order to assure meeting the minimum required number of valid signatures.

- Submit your petition by no later than Friday, July 20, 2001 to:

CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA

or FAX to 732-981-1769.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at m.tickman@ieee.org.

Forthcoming CPMT Conferences

-- Jim Morris, Conference VP

2001

Interpack 2001
Koloa, Kauai HI July 8-13, 2001
Contact smithd@asme.org
www.asme.org

Advanced Semiconductor Manufacturing Conference and Workshop
Boston, Massachusetts September ????
Contact: Margaret Kindling (SEMI)
(202) 289-0440

4th International Symposium on Electronic Packaging Technology (ISEPT)
Beijing, China August 13-18
Prof Jusheng Ma
temptm@mail.tsinghua.edu.cn Tel/fax: 86-10-62772724
http://ISEPT2001E.chimbe.edu.cn

7th International (THERMINIC) Workshop on Thermal Investigations of ICs & Systems
Paris, France September 24-27
Tech Contact Bernard Courtois
Therm2001@imag.fr
http://tima.imag.fr/conferences/therminic/1-33-4-76-57-46-15 fax 1-33-4-76-47-38-14

International Symposium on Semiconductor Manufacturing (ISSM)
San Jose, CA October 8-10
Contact: Suzanne Harkness (SEMI)

Future Directions in IC and Package Design Workshop
Cambridge, MA October 27, 2001
Contact: Paul Baltes
epd@engr.arizona.edu 520-621-3054/fax 520-621-1443
Alina Deutsch deutsch@ieee.org 914-945-2858/fax 914-945-2141
Madhavan Swaminathan
madhavan.swaminathan@ee.gatech.edu
404-894-3340: http://www.cpmt.org/conf/fdip01/fdip.html

10th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP)
Cambridge, MA October 29-31
Contact: Paul Baltes
epd@engr.arizona.edu 520-621-3054/fax 520-621-1443
www.epep.org

POLYTRONIC 2001
1st International IEEE Conference on Polymers & Adhesives in Microelectronics & Photonics
Potsdam, Germany October 21-24
Rolf Aschenbrenner
polyorg@izm.fhg.de
www.izm.fhg.de/polytronic_2001/
+49-(0)-30-46403-155 fax: +49-(0)-30-46403-161

27th International Electronics Manufacturing Technology Conference (IEMT)
Santa Clara, CA 12-13 November
Contact: Ken Schramko
kschramko@semi.org
1-(408)-943-7048 fax: 1-(408)-943-7913
www.semi.org/web/wevents.nsf/url/saIEMTcfp

Area Array Packaging Workshop
Munich, Germany November 12-14
Contact: elke.zakel@ieee.org 49-(0)-30-467-815-55/fax 49-(0)-30-467-815-51
www.pactech.de/CPMT-Germany

3rd International Symposium on Electronic Materials & Packaging (EMAP 2001)
Cheju Island, Korea November 19-22
Contact: EMAP2001 Secretariat,
emap2001@kaist.ac.kr
82-42-869-8285 fax 82-42-869-3095
http://care.kaist.ac.kr/emap2001

2nd International Conference on Advances in Electronics Packaging (APACK 2001)
Singapore December 5-7
Contact: Stephen Wong
kfchan@gintic.gov.sg
65-793-8423 fax: 65-791-2929

2002

Wafer Level Packaging Workshop
Atlanta GA March 1-2, 2002
Contact: www.prc.gatech.edu

8th International Symposium on **Advanced Packaging Materials**
Atlanta GA March 3-6, 2002
Contact Rajen Chanchani
chanchr@sandia.gov

Academic Packaging Conference
Dresden, Germany 19-22 March
Contact: Prof. Klaus Wolter
wolter@iet.et.tu-dresden.de

EuroSimE 2002
Paris, France 15-17 April 2002
Contact: Olivier de Saint Leger
Compete@mta.fr
+33-1-44517400 fax: +33-1-44517401
www.compete.tm.fr/eurosime/eurosime.htm

2002 International Conference on Electronics Packaging (ICEP)
Tokyo, Japan 17-19 April, 2002
Contact: 2002 ICEP Secretariat imaps-j@jiep.jp
http://www.jiep.or.jp/index.html

6th IEEE Workshop on Signal Propagation on Interconnects (SPI)
May 2002
Contact: Flavio Canavero +39-011-564-4060 fax: +39-011-564-4099
canavero@polito.it
Ivan Maio +39-011-564-4100 fax: +39-011-564-4099 maio@polito.it
www.tet.uni-hannover.de/SPI

25th International Spring Seminar on Electronics Technology (ISSE'02)
Prague, Czech Republic 11-14 May, 02
Contact: Pavel Mach mach@feld.cvut.cz

52nd Electronic Component & Technology Conference
San Diego CA May 28-31, 2002
Contact: www.ectc.net

8th Intersoc. Confer. Thermal & Themomechanical Phenomena in Electronic Syst's (I-THERM)
San Diego, CA May 29 - June 1, 2002
Contact: Paul Baltes;
epd@engr.arizona.edu
Univ. of Arizona; Engrg. Prof. Development;1224 N. Vine Ave.;
Tucson, AZ 85719-4552
Tel: +1 520 621 5104; fax: +1 520 621 1443

4th International Symposium High Density Packaging & Component Failure Analysis (HDP´02)
Equatorial Hotel, Shanghai,China June 24-27
Contact: Johan Liu
johan.liu@pe.chalmers.se

4th International Workshop on Smart Card Technologies & Applications
Germany November 18-20
Contact: elke.zakel@ieee.org 49-(0)-30-467-815-55/fax 49-(0)-30-467-815-51
www.pactech.de/CPMT-Germany

4th Electronics Packaging Technology Conference (EPTC'2002)
Singapore December, 2000
Contact: Charles Lee
Charles.Lee@infineon.com
http://cicfar.ee.nus.sg/eptc.html

2001 ELECTRONIC MANUFACTURING TECHNOLOGY AWARD HONORS WALT TRYBULA FOR INNOVATIONS IN SEMICONDUCTOR MODELING

ORLANDO, Fla. - May 31, 2001 - Advancements in the art and science of global economic modeling and lithography simulation for semiconductors and semiconductor packaging earned Walter (Walt) J. Trybula, Ph.D., IEEE Fellow, the 2001 IEEE/CPMT Electronic Manufacturing Technology Award. CPMT Society president Dr. Rao R. Tummala presented the $1,000 award at the annual Electronic Components & Technology Conference (ECTC) held here.

An authority in manufacturing automation and analysis, Dr. Trybula extended his early work in computer-integrated manufacturing to modeling the dynamics of the chip-making business, its equipment and materials supply chain. Lithography is the process in semiconductor manufacturing in which chip designs are projected onto silicon wafers. "The movement in the semiconductor industry to smaller and smaller geometries, the impact of technology acceleration, and related changes in market product mix have profound implications for the lithography segment of the industry," says Dr. Trybula, Senior Fellow at International SEMATECH. "The simulation tools and models we're building today enable manufacturers and equipment designers to evaluate throughput and process costs under an increasingly sophisticated variety of 'real world' manufacturing conditions and business dynamics. It's professionally rewarding to be at the center of the action and to work side-by-side with the best researchers in the world. There's certainly no shortage of challenges."

"Walt Trybula has been transforming skeptics into believers for most of his career," noted Dr. Tummala. "We congratulate him for his leadership role and numerous contributions. The broad interest and acceptance the industry economic model enjoys today, as well as the lively discussions it inspires, are due in no small part to Walt's technical rigor and drive."

Before joining SEMATECH in 1993, Dr. Trybula was President of Ivy Systems, Inc., a manufacturing automation and analysis firm, and earlier, a Senior Consultant with the General Electric Company. He has over 100 publications, including papers, book chapters, encyclopedia articles, teaching modules and published conference proceedings. He received his Ph.D. in Information Science from the University of Texas at Austin, an MBA from James Madison University in Virginia, and a Bachelor of Science degree in Physics from the Illinois Institute of Technology in Chicago. Among numerous honors and associations, Dr. Trybula is an elected member of the Board of Governors of IEEE/CPMT, a CPMT Distinguished Lecturer and founding editor of IEEE Transactions on Electronics Packaging Manufacturing.

Contact: Michelle Dietz
202-466-7391x1125
Kristine Martin
202-466-7391x1132

CPMT GROWS MEMBERSHIP

The IEEE April 2001 Membership Report shows that the CPMT Society has 3,729 members. With a 5.8% growth rate, we are now the fourth fastest growing IEEE Society. The other 35 IEEE Societies are growing at an average of 0.8% rate.

Thanks for your support of the Membership programs and keep renewing your membership to our Society. We grow our membership by word of mouth based on services provided for members. We do not have free membership or bonus offers just to increase a count -- it is active members that help everyone.

Find a colleague that is not yet a member of CPMT and show they our web site.

Ralph W. Russell, II -- Chair
Membership Committee
Dominion Virginia Power
Phone:804-819-2820, Fax Number: 804-819-2829
Pager: 804-273-3030, Pin# 7375
Email: r.w.russell@ieee.org

Rao Tummala Announces Chapter of the Year

It is my great pleasure to inform you that your two chapters have been chosen by a very distinguished panel of judges to be the best IEEE-CPMT Chapters. As you know , there are more than 30 CPMT Chapters world wide and to be chosen to be the best, is quite an honor.

Hong Kong Chapter -- Dr Ricky Lee
Singapore Chap -- Dr. Radhakrishna

This award was given during the CPMT Luncheon at ECTC in Orlando Florida.

Again, congratulations.

Rao Tummala
President of IEEE- CPMT

CPMT French Chapter

In November 2000 a French Chapter of CPMT was initiated. The following is a list of current officers:

Prof. Smail Tedjini, Chapter Chair
INPGrenoble
e-mail: smail.tedjini@inpg.fr

Prof. Gilbert Angenieux
Universte de Savoie
e-mail: angenieux@univ-savoie.fr

Dr. Jean-Louis Carbonero
ST Microelectronics
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Dr. Jean-Marc Bosc
Motorola
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Dr. Philippe Richin
Alcatel
e-mail: Philippe.Richin@alcatel.fr

Student Member of GIT Chapter, Sharath Mekala

The TC-14 CPMT / CS IEEE Barcelona Workshop of the IEEE Systems Packaging Committee January 22-24, 2001, Sitges, Spain

Condensed from a report by Interconnection Decision Consulting

Overview

This 9th European Workshop of the Systems Packaging Committee was held in Sitges, Spain, a resort community near Barcelona. For the first time, it was sponsored not only by the IEEE Computer Society and IEEE CPMT Society, but also by IMAPS Europe. This was part of a recent pattern of having the workshop in Cork, Ireland at alternate times, and having it elsewhere in the Mediterranean on the off years. (The last time away, it was held on Malta.)

Organizing workshops is more and more difficult with recent cutbacks in the electronics and technology industry, but a very satisfactory workshop was compiled, thanks to the efforts of Rolf Aschenbrenner of Fraunhofer IZM and Erich Klink of IBM Germany. Sessions were on Automotive, Microsystems Technology, Space Technology, and Cellular and Wireless. The final session
was on Signal and Power Integrity.

Attendance was just under 70, and the interaction between attendees was worthwhile.

Something interesting happened with the schedule of events. Because Spain normally has dinner at 10:00 PM, the workshop had the usual morning and afternoon sessions and the reception, but then had the evening session immediately thereafter and dinner after the end of the day's sessions - at 10:00 PM.

Session I Monday afternoon Automotive Session

Electronic packaging activity for automotive is particularly active in Europe. Presentations were much easier to arrange than in the U.S.

The first presentation was by Magnus Torvall of Kitron Development, Sweden. Kitron is the current name of what was the Automotive Division of SAAB Combitech Electronics. **The presentation on Future Packaging for Automotive High Temperature Electronics** investigated the performance of electronics at working temperatures of 125 C to 200 C. The modules were ceramic for this under-the-hood application. Engines are going hotter, and there is much concern about the reliability with high heat.

Furthermore, long term reliability is a must. The customer does not like electronics that die in 3 years. The technology is an adaptation of LAN (Local Area Networks) to CAN (Car Area Networks). This approach has 70% less weight of cables and an elimination of the previous $1 cost per cable connection. Manufacture using CAN technology is now 100 Million units per year, but expected to be 500 Million by the year 2008.

There is prior experience in electronics running that hot - oil well logging equipment has similar heat environment requirements, but the automotive environments can also be as low as -40 C.

Ceramic substrates are used, with wire bonded die. Silicon technology works at those temperatures, but diamond interconnect substrate, while possibly good at high temperatures, is not mature enough for general use. NPO capacitors are very good, all others fall off in capacitance “big time”.

There is also die attach on polyimide, with some problems with cracking of the polyimide. Gold solders work well, but are costly; lead solders are good, but there is a forthcoming ban on lead. Silver soldering is a possibility.

Silicone gels are used as the corrosion preventative, and they have a newfound advantage - the gel prevents silver migration, making the use of silver possible !

While the work at Kitron is wire bond, ACREO is continuing the work with the use of flip chip technology.

Jaakko Lenkeri of VTT Electronics, Finland, talked of the use of LTCC technology (Low Temperature Co-Fired Ceramic technology). This seemed to be the standard case for using LTCC - thermal expansions of 5 to 7 ppm/degree C and hermeticity. High interconnect density is possible using photosensitive pastes for the conductors, with line widths possible down to 50 microns, 25 microns for the top layers.

This is ceramic technology with shrinkage of 15% during firing. However, control of shrinkage is +/-0.2%, permitting suitable dimensional control.

Patrick Dall'Agnese & Peter Lewandowshi of Siemens in Toulouse, France, presented their "Introduction of Fine Pitch BGA & CSP for Engine Management." Their project, funded by Escheta, was to develop European sources for Chip Scale Packaging. CSPs are forecast to have future volumes of twice that of BGA packages, or over 5 billion packages per year. The products were to be harsh environment applications like the engine compartment usage, but also passenger compartment applications such as navigation units.

FR4 interconnect boards were used for low pin count devices, and higher density substrates used for higher pin count packages (over 200), and circuits at small pitches less than 0.8mm.

The most notable feature of their technology was the use of stacked solder bumps. Solder bumps of 300 microns were deposited on the substrate, then the substrate was coated with dielectric (epoxy ?), with the tops of the balls protruding above the surface of the encapsulant. These protruding bumps were ground off, leaving a smooth surface with solder lands. The second set of bumps was then applied, using a different solder with a lower reflow temperature. These taller bumps made for improved reliability under conditions of great differences in temperature coefficient of expansion between package and the board.

Fraunhofer IZM is a major developer of electronic modules for the automotive industry. Rolf Aschenbrenner of IZM talked of "Integration of Micro-Mechatronics for Automotive Applications". The term is used to describe assemblies that integrate the manufacturing steps and may eliminate at least one material component of packaging level from the solution.

He described a Multichip Module for motor controls such as window list and sun roofs. Three interconnection layers were eliminated in the coordinated design. The unit was in a transfer molded "saddle" package mounted directly on the sensor. The unit was made by Toshiba with a TCE of 11 and suitable for operation at 200 C.

System-on-a-Package is coming, using 3D packaging on organic interconnect layers (Though they prefer System-in-a-Package, SIPS, for the terminology.) This is chips-on-flex technology, with the silicon chips thinned down and mounted on the flex, which is then folded to produce the assembly.

Only digital chips can be thinned down - analog chips are not suitable.

Microsystems Technology

Heikki Kusima of VTI Hamlin OY, Finland, talked of MEMs Sensor Technology. MEMs technology has totally changed sensor modules from those used 20 years ago. The high volume of automotive applications have paid for the high capital costs.

Air bag accelerometer sensors are made with surface mount technology, using bulk micromachining of silicon. Angular rate of yaw sensors as used in braking systems, however, have substrates of quartz, because it has been difficult to get high actuating forces and high "Q" values with silicon substrates.

Technology is moving to Reactive Ion Etching for the fabrication of the silicon.

Three issues dominate design - the odd shapes of the sensor packages, the extreme sensitivity to mechanical stress, and the sensitivity to humidity. These are always concerns, but in MEMs work the performance implications show up at much lower levels of environmental stress.

Micromachined Silicon resists humidity better, but surface machining devices resist mechanical stress better.

Gerd Bauer of Fraunhofer IPA, Germany, described their "Fabrication Framework for Modular Microsystems. MACH-X". In the MACH-X system, various units with different functions are made by one or more manufacturers, but compatible with combined assembly. The desired application function is produced by combining the various sub-units as needed.

This is 3D stackable packaging, using Top-Bottom Ball Grid Array for the interconnections. For example, for a pressure control system unit, the individual elements in the stack consisted of a pressure sensor and temperature sensor layers, and A/D converter and a microcontroller on another layer of the package, and additional layers for program and data memory and for the buss interface and I/O functions.

Applications included micro-controllers for Siemens, featuring pressure sensors with included ASICS and memory. Magnetic field sensors and autonomous micro dispensers for microfluids were also made. Optical interfaces are also possible, but in that case the stacking of the layers requires optical interconnect from one layer to the other, using mirrors at the edges of the layers to reflect data to the next layer.

Cian O'Mathuna and others from NMRC in Cork, Ireland prepared a talk on Microsystems Packaging and Integration. This is a multidisciplinary field of design and manufacture of electronic assemblies with micro-sensors and actuators, signal processing, communications and memory all in one package. Such complicated packages often make up over 80% of the cost of the electronic system.

Flex interconnect technology is used, sometimes providing active flex that permits pumping action of the mechanical interfaces with the world. The use of flex presents problems at high temperature bonding, after the assemblies shrink and induce

strain. There are tradeoffs between the use of very thin flex and thicker membranes for more strength.

Monday Evening Session - Space Technology

Laurent Ripoteau of Matra Aerospace Missiles discussed "Using Technological Innovation to Minimize Production Costs". EADS / Aerospaciale Matra Missles is developing a missile flight autopilot to maintain or improve existing performance capabilities in a new package that is 50% smaller.

This is one of those that "needed to keep military electronics performing" when the original technology is no longer manufactured. The new units, however, are usually smaller with increased capability.

Michael Massenat, formerly of Astrium (Matra Espace) with Lambert of Bull SA, organized a paper on "Tape Chip Scale Packaging (TCSP) for the Aeronautic and Space Industries". CSPs have been noted for their high volume use in consumer products, and the challenge was to move this technology to military and space applications. Astrium, Bull Comulec and LETI R&D have developed the high performance packages using a new kind of CSP.

The CSP is based on a TAB lead frame on polyimide with fine copper traces, using bumpless TAB bonding on the Fold on Copper pads. The interconnect substrate uses fan-in leads to connect to solder balls under the die on the bottom side of the package, making for minimal footprint area.

The TAB leadframe is the "interposer" and absorbs the differential stresses during thermal cycles, so no underfill is needed !

Connections are made through the flex film using laser cut windows that permit connections to the bottom mounted balls. Conductors were 75 microns on 250 micron centers.

Rene Dupre of Matra BAE Dynamics, France, developed a 3-dimensional interconnection concept, presented in a talk titled "3D Assembly and Packaging Technologies". The work was done with Thomson, DETEXIS and LETI Laboratories.

The assembly was two of Texas Instruments processors interconnected on a PCI interface provided by a FPGA Xilinx component.

This is land grid array packaging, using a multlayer ceramic substrate with three assembly levels.

The first level supports the PCI interface, and second level the master interconnect level, and a third level provides additional interconnect.

The master and slave interconnect are manufactured using master-Si technology with integrated decoupling capacitors, and the resultant assembly is hermetically sealed by a metallic lid. Flip chip technology is used for the die connect.

Connection from the module to the systems printed circuit board is by CINAPSE fuzz buttons, permitting easy attachment and removal of the part without the need for soldering temperatures.

The last presentation in this session was by **Brigitte Breaux of Astrium, on a Multichip Module for a DSP Peripheral Controller.** This was a unit used in many applications in space equipment. The packages are 6-watt packages with 330 I/O, expected to increase to 400 I/O in the future. Die bonding is Aluminum wire, and the ceramic is MCM D/C, organic thin films over a ceramic substrate.

The connection to the board was through the use of "C" shaped flex links reminiscent of the Rogers "Z" shaped copper links, The flexing contacts were captured in a flex layer, making it a high density interposer sheet. Reliability was better than 180 FITS.

Tuesday Technology Session

This was a mixed session of MCMs, CSPs Electro-optic interconnect on PWBs and a new system integrated packaging approach.

The MCM talks were by de Samber of Phillips at Eindhoven on Wafer Scale MCM-D for RF Modules, and a talk by Enric Cabruja of CNM, Barcelona, on an MCM-D for Power Applications. First the Phillips talk. This is wafer scale packaging using CUMULUS technology using 3D lithography. BGA interconnect is used for the die attachment to the PCB, which also mounts the SMD components using solder ball reflow.

The passives are made in wafer scale form in an IC-like technology using thin film capacitors, resistors and inductors. Top to bottom vias connect to the ball grid array pattern on the bottom. The holes are not laser cut, but powder blasted hole cutting as used in dental drilling technology. The application was for a transmit voltage-controlled oscillator for cellular applications.

The power chip MCM-D module was also a wafer scale realization using a silicon substrate(MCM-S) with substrate power chips. Four IPMCMs (Intelligent Power MCMs) modules are soldered to a substrate to build a full-bridge motor control. CNM is a development laboratory in Spain, like IMEC in Belgium.

I/O is ball bonding, placed in etched recesses in the aluminum metallization.

Polymer Stud Grid Array Packaging was proposed for miniaturization of high density packages. Bart Vandervelde of IMEC did the talk. The substrate on which the chip is mounted is a molded polymer body having an array of plastic posts on the bottom side. The whole bottom surface of the substrate is plated with copper, and the posts are electrically isolated using laser cutting of the copper at the base of the posts.

The posts are soldered to the PCB interconnect using conventional soldering, but because the metallized posts replace the solder balls previously used, this is considered as an advance in elimination of the use of lead.

The chips are wirebonded to the top of the molding, and connection to the bottom posts are made by metallization of the substrate around the ends of the substrate and on the surface on the bottom of the array of posts.

This technology is possible only for a modest array of pins - 72 maximum, or 18 per side.

The major point of concern was the reliability during thermal cycling. The plastic posts proved to be resilient enough to afford good reliability.

Rolf Aschenbrenner of Fraunhofer IZM gave a good talk on "A New Approach for System Integrated Packaging", The new approach was to use ultrathin and flexible chips mounted on flex circuits.

The chips are thinned to less than 30 Microns, and the resultant assemblies have greater flexibility than conventional chips mounted on the usual flex substrates. The technology is called "Chips in Polymer".

While the chips are thinner, there is not a great increase in reliability - particularly to bending forces, If the board is bent, the thin silicon must also bend, and that causes stress on the flex bonds. The solution is to apply an extra polymer layer on top of the assembly, both stiffening the assembly and taking some of the bending stress from the chip-to-board bonds.

This top coating can be electroless plated copper, and circuit connections can be brought to the top of this polymer through 40 Micron photo vias. Applications include many digital customer products, providing better performance at lower costs, and high volume manufacturing capability. Time-to-market is also quite low.

They call this System-In-a-Package (SIP) rather than the Georgia Tech advocated name System-On-a-Package (SOP). Same technology.

SIP packages are made three ways; in molded leaded packages, in area array packages, and in stacked thin chips. Having very thin chips on flex permits stacking by folding the flex film assembly on top of a first chip. Passives can also be on a stacked layer, rather than building them into the primary interconnect substrate.

Chips are by Toshiba, applications are for many German and European manufacturers. Volume is already huge. A very successful new technology.

Interconnect technology using Electro-Optics on PCBs was included in this session. The speaker was Peter Dammer of Siemens, Germany. The argument for optical connections at the board level is not only the usual improvement in bandwidth for use with multiplexed signals, but a further unusual one.

Heat dissipation reduction is the newly perceived major benefit. Over 70% of the heat generated on a circuit board assembly is from the drivers, to power the electrical signal lines. While there is power consumed and therefore heat generated in the optical drivers, there are so much fewer of them because multiplexing puts many signals on one optic link.

The light paths on the surface of the PWB are transparent polycarbonate, patterned using LIGA - Micro-optics and deep etch lithography. Traces are 150 Microns wide and thick, spacings are 250 Microns. Attenuation is about 0.1dB/cm. The basic backplane is 20 layer FR4. Of course, the light interconnections have no electromagnetic coupling problems and no electrical energy radiation.

The integration of the light paths into the multilayer board needed no exotic materials and little change in processing. Optics interconnect at the board level is feasible now, and has many advantages.

Evan Kufner of the Institute of Microtechnic in Mainz, Germany, provided the back-up information on LIGA processing. LIGA (Is that for Lithographic Grabenforming Abformisch ?) permits patterning of traces with aspect ratios of 100:1 for the deep etch.

In many applications the circuit features are produced, and the board overmolded to capture the optical materials. This is mold template manufacture. Optical couplers, splitters, and other features can be made just as easily as straight circuits. Coupling of the light path to the chips is done with cylindrical lenses. Applications include the fabrication of scanning windows, and capture and channeling of light energy.

Cellular and Wireless Session, Tuesday Evening

This session had many highlight and future-oriented papers. They included:

The presentation by Lief Bergstadt of Ericsson, who talked of various microwave

modules. The market for microwave modules was formerly military and space, but now the emerging need to wireless telecommunications has produced a need for volume manufacture of these products. A more industrial approach to manufacture is needed.

In fact, the use of wireless microwave technology to produce children's toys has produced more advanced technology than the military. Exotic things are being marketed; Automotive Radar, GPS systems, Wide area LANs, etc, but also Yuppie products from golf ball trackers and skeet shooters scorers. Yuppie products are deliberately used to finance the development of technology which can then be used for more serious and more cost conscious products.

Frequencies are from 55-58 GHz for microwave radio to 77 GHz for automotive radar. Under 60 GHz, conventional design engineering can be used, but over 60 GHz one needs trained microwave engineers - scarce in today's world. It is particularly difficult to re-train microwave engineers from military and space technology to the needs for low cost commercial manufacture.

Radiated microwave RF signals can come right from the IC chips, with the energy focused by using glob top coatings as a microwave lens - a circuit function for the lowly glob top encapsulation.

The other exploding technology is the use of "Bluetooth" modules. **As the creator of the Bluetooth concept, it was fitting that the talk ws by Einar Martinsson of Ericsson Microelectronics.**

Ericsson started work on these 2.4 GHz modules in 1984, and now there are over 2000 companies who have licensed the technology or participated in the development. The modules he showed were surface-mountable, and the manufacturing technology was flip chip on LTCC substrates. Laser trimming is used to trim the voltage-controlled oscillator.

Necessary microwave structures could be implemented in the LTCC designs, including antenna filters and the receiver baluns.

This is one-sided assembly - lowering costs, 11 components are connected with a single reflow soldering operation.

Joerg Baumback of Tyco Electronics (formerly a division of Siemens) talked of their thin Lead Packaging for Rf Multichip Modules. This is MCM-D processing technology with wire bonding of the chips.

These multichip modules are produced in large array processing, 4" square now, 16" square later. Passives are included, using capacitors-in-series concept often proposed by Len Schaper of the University of Arkansas.

The winner talk, as always, was the review of the state of satellite telephony, in the talk " Is there life after Iridium ?" by Augustine Coello-Vera of Alcatel Space. He gave the current status of Iridium, Globestar, ICO, MCO, Orbcom and Ellipso, much of which was new to me, and to others in the meeting.

Satellite systems can be Low Earth Orbiting or Geostationary satellites. The low earth orbiters need a great number of satellites, from the 67 or so for Iridum to the 900 or more for Teledesic.

Reviewing each in turn:

Iridium - the original low earth orbiting system (LEOS) was designed by Motorola using analog technologies, and with the assumption that the growth of cellular tower availability would be slow. It didn't work out that way. So many towers were built that most of the developed world could use local cellular service, which was digital, and superior. Having to go outside a building and point the handset to a satellite was just not attractive enough, except for explorers in the jungle, mountain climbers, and people in darkest Africa with no local phone service.

But you don't get millions of customers for those uses, so Motorola and the other sponsoring companies declared bankruptcy and began bringing down the satellites. BUT THAT PROCESS HAS BEEN STOPPED ! The Pentagon has bought the assets of the system and will use it for military service - for which it really is useful for battlefield communication and world-wide military links.

ICO has been bought by Craig McCaw , and has new life - but not many customers yet.

Globalstar has only 21,000 subscribers, and, though operational, will probably go bankrupt also.

There are too many Low earth Orbit systems to reach profitability - there are not enough global customers. Orbcon, Ellipso, Teledesic, Globalstar and Skybridge are too many systems. Some may survive - Insurance companies are one class of user - people who work out of the office and often in areas with poor or no cellular coverage. Trucking companies are also candidates, though many can get adequate coverage through the cellular systems.

BUT GEOSTATIONARY SYSTEMS ARE ANOTHER MATTER !

A single geostationary system can be put up by one country or a very small group of countries to serve such things as education needs as well as telecommnications. ACES serves Japan, China and Australia. Thuraya serves for commnication between Europe and India, serving over 1 million people with no fixed or mobile phone service.

These are small units, but with a 16 meter antenna on the satellite, easy to deploy because they only have to point to one general direction. Often systems have only two satellites, inexpensive and much easier to manage than the low earth orbiting multisatellite systems.

Contrast the economics. A LEOS System requires 5 to 10 years to develop and the launching of hundreds of satellites costing perhaps $ 3 Million each, and the VERY slow waiting for customers. A **VERY long time** for payback.

Geostationary systems require only one or two satellites, and much simpler ground stations (no hand-off required) They have shorter design times and the user usage tends to be instantaneous - because it pinpoints area that desperately need communication. Fast payoff.

A late development is Digital, Audio Broadcasting. Cars will be sold with 3 band radios, AM, FM, and Satellite reception. For the automotive traveler, that means constant reception for the station of your choice while you travel, and the end of station searching every hundred miles. Ford and Chrysler are already committed to these new radios and will have them in cars quite soon. Service will be $ 9.95 per month and will provide 50 channels. The receiver is $ 200.

Satellite systems are not dead - particularly geostationary systems for local and regional coverage. It is only LEOS that will shake out, with many bankruptcies to adjust system availability to the limited number of global customers.

Wednesday Morning, Signal and Power Integrity

Prof F. Canavero of Politechnico de Torino, Italy, discussed the difficulty of calculating interactions between circuits if the interacting lines are neither parallel nor of constant cross-section. The simple lossless transmission line equations do not work. This work consisted of lossy domain methods of "discretization" of the interacting circuit elements. His optimized code for the simulation of the circuits can out-perform standard non-adaptive simulation schemes.

Jose Schutt-Aine of the University of Illinois at Urbana also discussed simulation to determine transmission line scattering parameters. Here the problem discussed is the frequency dependence of the scattering parameters. Examples were given of the analysis for simple lines and lossy lines.

De-coupling Strategy and Heirarchy Structures for De-coupling Capacitances were discussed by Dr. Thomas Winkler of IBM Boblingen. This was an excellent review of the need for capacitors at the chip level, package level, and board level, and the strategy for the necessary value for each.

The remaining two papers on High Frequency Power Integrity on a chip and in the system were presented by Dr. Roland Frech and by Dr. Bernd Gargen of IBM Germany. Again, these papers were for analyses of major system power noise issues, particularly on the mid-frequency Delta-I noise with finite difference time-domain analysis. Simulation procedures were tested and confirmed within 5% of the actual measured noise.

Conclusions

Again this workshop proved that there is a need for system packaging meetings to cover a variety of issues. There are many special purpose workshops, but a meeting like this provided a broader insight into developing technologies, and highlights things that can be taken from one area and applied to another. In short, this is a generalist's workshop, and brings together people from diverse fields. That seems to be a useful contribution and a tradition worth preserving.

After the US Spring Workshop in Scottsdale in May, the next Systems Packaging Workshop will be in Japan in January 2002.

J. W. Balde, 5/1/2001
Edited by Evan Davidson and Erich Klink from the Report from Interconnection Decision Consulting

Evan Davidson receiving "Fellow of the Institute" plaque from President Rao Tummala

Sample Review of ECTC Presentations

More than 900 component /packaging / manufacturing enthusiasts showed up at the Wyndham Palace Resort for the 51st ECTC. There were six parallel sessions at ECTC for all 3 days. So even someone who attended must rely on the Proceedings to find out about talks they were unable to hear during the meeting. None-the-less we will list some of the notes taken by one happy CPMT member. The meeting was abuzz with people signing in, purchasing CPMT publications, and networking.

At CPMT table

Networking during breaks

Session 1: High speed packaging.

Felix Mederer of University of Ulm described how they fabricated VCSELs with thicker monolithic cavities. This allows a single mode even with a big enough aperture (7 microns) to match standard polymer optical fibers. The target was 10 Gbs information for WAN applications. Michael Vrazel of Georgia Institute of Technology discussed an inverted MSM structure they used to detect high speed information at 1310 nm. The device operated at 3.3V; they have 55fF of capacitance when designed for 2.4 Gbs operation. Isao Yoneda of NEC showed details of a 4 channel parallel optical transceiver. Trench isolation was used between the edge emitters. A fixture on silicon that aligned the 4 fibers and bounced their signal from etched mirrors up to the flip-chip photo detector array was displayed.

Mikko Karppinen of VTT Electronics described an interesting way of obtaining low cost passive alignment of fibers perpendicular to an LTCC structure. The fibers align by vias designed into the LTCC material and the transmitter chips are flip chipped onto the far side of the LTCC structure. No ferule is needed to align the 5 fibers and UV curable adhesive locks things in place.

Eric Grann of Blaze Network described Optical Transceiver in use for Course WDM which is much in demand for short range data transmission (even within a radar system). His system works with multimode at 850 or 1310 nm but this limits you to 1 Gbs for 2 km. He uses injection molded optics, standard interference filters that can be batch made 1000s to a wafer, VCSELs, passive alignment, and no forced cooling on package. This approach was designed to need only the precision of standard pick-and-place machines.

Shimya Abe of Fujikura detailed a very small transceiver using VCSEL and pin photodetector.

Session 10: RF MEMs and Systems

Dave Palmer of Sandia Labs gave a tutorial update on fabrication of RF MEMs switches for applications such as radar phase shifter circuitry.

Wyndham Palace Resort

The many questions indicated the growing popularity of mechanical switching.

Nathan Bushyager of Georgia Tech demonstrated a modeling and design approach to MEMs. It is called MRTD - MultiResolution Time Domain. Typical simulations on a PC still take 3-4 hours but used on clusters of PC should make design more interactive.

Joseph Hobbs of Georgia Tech studied the trade off of expensive on-chip capacitors versus several discretes on the PWB with their frequency limitations. The compromise was distributed capacitors within the PWB. They showed suppression of switching noise by a factor of 7 at the high frequency range (300MHz). Traditional lumped capacitors handle the low frequency problems.

Y. L. Li detailed work on distributed models for capacitors. By modeling capacitor-like tapped transmission lines with mostly C and a little L.

The last presentation from the National Sun Yat-Sen University described success at using a leadframe CSP for RFICs. The motivation is that the frequency performance of transistors is severely degraded by standard packaging.

Session 13: All Optical Networks and MEMS Packaging

Opening remarks by Ron Scotti of Lucent gave an excellent overview of MEMs technology applied to Optical Networks. First he talked about the simple designs that have lead to the big MEMs money makers: Analog Devices accelerometers and Lucent router mirrors. (I don't think the engineers considered them simple at the time of development). He reviewed the positive and negative of the dominant polysilicon MEMS technology. Pro: highly versatile, components have low mass and high resonance frequencies so they are immune from normal vibrations, technology is well understood and can produce robust designs. Con: high temperature processes cause high stress in films, only limited thickness can be used, polysilicon has a grainy poor optical surface, and there is reliability concern in a non-hermetic environment.

He then described a new approach using Deep reactive Ion Etching (Bosch) combined with SOI and wafer bonding. Pro: very good optics, bulk silicon, no stress gradients, and thick structures easy. Con: processing has limited flexibility, hard to get good SOI starting material, high mass structures give lower resonance frequency, limited number of layer.

James Walker continued in the overview mode. He said that MEMS reliability is an unknown since the field is new. For example, SOI MEMS are only 2 years old and optical MEMS are 6 years. There is little mechanical force available in most implementations of MEMS, so moving light beams is a natural application matched to the technology, "photons are very light".

The trend in fiber optics is screaming for MEMS cross bar switching. Need to keep total power small, optical channel spacing is shrinking (DWDM), bit period is shrinking, range of wavelength control increases, carefully engineered fiber links. MEMS could give more dynamic control of links providing gain equalization and dispersion compensation.

"Everyone" is doing optical crosslink for the rapidly expanding DWDM market. Worries that too many "49ers" are chasing too few nuggets. However, 3D MEMS is the only scalable solution to this crosstalk challenge. The other big application of MEMs in the telecommunication world is MEMS tunable VCSELS.

Walker worries that the hype of MEMS has long outrun the reality in this application space. He reminds everyone not to fall in love with one solution to the telecom problems since alternatives always exist. Deliver MEMS not hype or an alternative will win the war.

Steve Robinson of Photons Inc. repeated the theme that 3D crosslink technology was needed. He emphasized the challenge of analog control of the mirrors as being much harder than the digital mirror control of past applications. He saw the crosslink business growing 44%/year arriving at $4B in 2008. He is an advocate of bulk MEMS for optics not surface MEMS (half the audience looked for things to throw at this point). He predicted that within a few years high capacity MEMS switches with 10msec times would be common.

Jeff Bennett of Intel discussed automated fiber alignment regardless of temperature, aging, and shock. The goal was to produce a 10Gbs transceiver in 1/8 the previous volume. A hierarchy of fluxless solders was used. The study of wetting and interactions was a full time effort for some material scientist.

Session 18: Fatigue and Delamination

(Figure: Bob Howard talks to co-chair Donna Noctor as Andrew Tay prepares to talk)

Andrew Tay of National University of Singapore discussed the affects geometry can have on the delaminations in rectangular IC packages. Several design rules of thumb were ferreted out of the computer analysis: a 1 mm border of lead frame pad must be around the chip to stop crack propagation, also the ratio of encapsulant above and below the leadframe and the ratio to the chip thickness made a large difference.

Session 22: Novel Packaging Technology

Kyocera Corporation discussed the use of LTCC (low dielectric constant) for broadband mobile communication up to 50 GHz. They analyzed the

radiation that came from signals going through vias between SMT layers.

Session 25: Optical Interconnects

Larry Coldren of University of California Santa Barbara updated everyone on the development of long-wave length single-mode VCSELs (for long haul telecommunication). Aiming at 1.55 micron intended for 10 Gbs under OC-192 for WDM. He reviewed the GaAs DBR in the 850-980 nm and all the attempts to lengthen the wavelength. The index contrast in this material gets diminished at longer wave lengths. To date the quantum dots and GaAsSb quantum wells do not have enough gain. There has been success by wafer fusing mixed material systems such as GaAs/AlAs mirrors on an InGaAsP active region.

He described the InP based system made using MBE. The system used metamorphic GaAs/AlAs top mirrors to make the system reliable and manufacturable; multiple active regions to overcome bad mirrors, used all n-type material by placing a degenerate tunnel junction to get bias correct. They use oxidation to control the aperture. To get enough power in the fiber he used 8 VCSELs like wedges of pie forming a circle.

Yue Liu of Honeywell Laboratories concentrated on OE arrays. Their goal is to integrate logic and switches in 2D optical array and therefore minimizing channel crosstalk. By placing the VCSEL light emitter, MSM detector, and control electronics in a cell you get a "smart pixel" which allows some control of crosstalk.

Honeywell has been shipping millions of 850 nm VCSELs/month and has recently added oxide confinement to their mass manufacturing process. One unique part of this government consortium effort was the application of arrays of microlens on a wafer with a jet-printer head.

Yuzo Ishii from NTT Telecommunications Energy Laboratories showed flip chip carriers on PWB used to create complex OE systems. The carriers had light source and detector chips placed in a downward cavity of a carrier that has ICs on its top. The PWB has a via hole that allows light to pass from the carrier to optical waveguides or fiber butt ends on the other side. They have obtained 82% coupling efficiency. They also used microlens dispensed by ink-jet printers.

A talk by Aegis Semiconductor detailed a transparent monitor for giving gain control feedback to each individual VCSELs in an Array. Their technology uses amorphous semiconductor from solar cell development and transparent conductive ITO oxide...all put down at less than 300C. They have worked up to 32 x 32.

Jerome Eichenberger of Optobahn Corportation discussed 2.5 Gbs/channel communication. The immediate customer was the short server rack to rack communication, but they also anticipate a board to board business. They showed a 4 channel unit using MT ferule and hermetically sealed. It passed all the environments industry asks for. It used standard pick and place and automatic active optical alignment. Their modules can be reflowed onto customer boards. Alignment in next assembly is not super important because there is lots of power to spare.

Motorola Fellowship

"Low Loss Deep Glass Waveguides Produced with Dry Silver Electromigration Process", by Ricky Chuang (student) and Prof Chin C. Lee from University of California Irvine became the winning paper for the annual Motorola CPMT graduate Fellowship.

Session 16 Co-Chairs Sudipta Ray (IBM) and Joseph Soucy (Draper Labs)

CPMT Luncheon at ECTC

The CPMT Luncheon was held on Wednesday May 31 at the Wyndham Palace Resort. While hundreds of engineers enjoyed the Chicken Marsala, CPMT President Rao Tummala described the successes of CPMT and recognized our many accomplished volunteers.

Rao Tummala presents Chin Lee with Fellow

In particular, Rao introduced the audience to 3 of CPMT's new Fellows of the Institute: Chin Chung Lee, Herbert Reichl, and Evan Davidson. This year eight of our Society earned this recognition.

The front table of the luncheon seated the core of your volunteer officers: Philip Garrou (Technical VP), Anthony Chan (Administration VP), James Morris (Conference VP), Paul Wesling (Publication VP), Albert Puttlitz (Education VP), Ron Gedney (Secretary), Merrill Palmer

New Fellow Herbert Reichl

(Treasurer), Ralph Wyndrum (IEEE Director), and John Stafford (Past President).

John W. Stafford, formerly of Motorola, was presented with the CPMT Society David Feldman Outstanding Contribution Award (below).

George Harman of NIST was recognized with the CPMT Society Outstanding Technical Contributions Award (see below).

The CPMT Society Electronic Manufacturing Technology Award was earned by Walter J. Trybula (see picture below).

Front Table from left: Al Puttlitz, James Morris, Paul Wesling, Phil Garrou, John Stafford, and Rao Tummala at CPMT Lunch

Charles Wee Ming Lee was announced as the CPMT Society Outstanding Young Engineer. Two Chapters tied for the CPMT Award of the Year: Hong Kong and Singapore.

Vice President of publications Paul Wesling reviewed for the audience the nature of the Three CPMT Transactions. Then he awarded the Best Paper Award for the IEEE Transactions on Components and Packaging Technologies. The

winning article was "Development of Virtual Reliability Methodology for Area-Array Devices Used in Implantable and Automotive Applications" by Suresh K. Sitaraman, Rajiv Raghunathan, and Carlton E. Hanna. This article first appeared September 2000.

Next he announced the Best Paper Award for IEEE Transactions on Advanced Packaging. "Ultra-Thin Electronics Device Package" by Kevin Y. Chen, Robert L. D. Zenner, Michael Arneson, and David Mountain had been published in February 2000. Certificates and a cash award are given for these paper awards.

Lastly Dr. Iwona Turlik, Corporate Vice President and Director of Motorola Advanced Technology, then gave her presentation, "Components, Packaging and Manufacturing Roles in the Future."

Figure: John Lau receiving award from President Rao Tummala for all his contributions to ECTC over the years.

ECTC Panel Discussion

Wireless Technology: Is It a Disruptive One? Ephraim Suhir chaired a thought provoking session late Tuesday night (May 29th) as part of the ECTC experience. He set the tone for the discussion by pointing out the by "disruptive" he means that it is something that will change how you think about the markets you serve. Because of this perspective it is often the Marketing groups of companies that force a technology to be disruptive rather than the clever technologists. **(Ephraim Suhir below)**

As engineers, we often guess wrong as to which technology becomes disruptive. We like to believe that it is our genius to transcend the small incremental steps and go for the big leap forward that insures the disruption of the marketplace. With this view, we find that the growing wireless presence (400 million hand held wireless units sold over the last year) is beginning to intimidate many establish ways of communication. If the customer find, or by marketing blitz believe they find, that wireless provides cheaper, simpler, smaller, and more convient use they abandon established, even superior technology. Ephraim Suhir pointed out that many technologies that eventually replace established technologies started out underperforming in some ways but seeming better in some aspects to the users. For example the first small transistor radios were technically as good as tube receivers but they were small and did not need to be plugged in. In analogy, many people are dropping their twisted wire phone service at home and using cell phones for all their communication. Despite defining the terms very well, Dr. Suhir never answered the question as to whether the Wireless Technology was on a disruptive path.

The first presenter was Lou Manzione from Bell Laboratories. He reinforced Suhir's statements agreeing that the disruption is often market driven not technological. He pointed to the fast rate of

Lou Manzione

movement in wireless application developments that could put the marketplace on the verge of major changes. the number of data and voice wireless subscribers is growing rapidly.

He sees this trend only increasing as the handsets get smaller, go digital, add many digital browsing (see Japan), and unified messaging. Another example is the recent explosive growth of wireless LANs. The one advantage of low cost of quick installation has disrupted the market for small offices, schools, retail (Starbucks), and corporate offices. The $100 per connection ($60 PC card + $30 for server). This can be used for Tags on retail items and for Wide area Network (WAN) over 5 miles.

He reviewed the routes of growth:

1.) 802.11 at 5.6 and 2.4 GHz bands has been used at 11 Mbps in the 50 - 500 meter range. The security issues have been addressed with 64 and 128 bit keys using RC4 encryption. This technology is used mostly for data.

2.) Bluetooth can include voice is at 2.45GHz with 10 meter range. Could define a path of lap top to cell phone to LAN. Bluetooth should be less than $10 unit but built on sophisticated LTCC.

So LANs will start having a big impact. Third generation will be at 2 Mbps and fourth at 100 Mbps. The wireless cells will probably shrink from Macro (5 - 30 km) to Micro (1 - 5 km) to Pico (0.2 - 2 km). With Pico cells there would be no acquisition costs for repeater sites since they will be so small. However will need high efficiency power amps, thermal management, smart integrated antennas. Need high reliability at low cost (even in lightning storms), advanced packaging with light weight. If the beam could be steered with a smart antenna system then frequencies could be reused even with cell.

The radio on a chip will allow perhaps 4 different frequencies to used by each wireless unit to increase reliability of service.

Lou Manzione sees the lap top + palm + cell phone = new terminal that could be sold at a higher price point because it has more functions. On the component level he mentioned inductors with MEMs and proliferation of SAWs and embedded passives in the design.

The next presenter was Dr. Seppo Pienimaa of Nokia. He interprets wireless as a more natural approach. that virtual presence is more natural than standing at the end of twisted wire pairs. He pointed out that only 20% of the people in the world have wired phones.

He pointed out that current terminals are 80 cc broken down as: 60% mechanics and interface, 25% batteries, and 15% electronics. However the trend is to go to color which will mean a larger display which will demand the rest of unit must be made thinner. Miniaturization is the enabler. The trends are to extend the options, enhance security, and enhance efficiency. Wireless is replacing fixed wire as well as expanding service to those that

don't have wired service. Encryption

Seppo Pienimaa

implementation will be easier to add onto wireless than to existing hard wired LANs.

The stock prices of companies depending on wired phone and LAN communication at least momentarily indicate the disruption caused by wireless has begun. However, the lack of profits for the wireless companies may make it a hollow victory for disruption.

Editors' Meeting at ECTC

CPMT Vice President of Publications, Paul Wesling, held an editorial breakfast meeting at the annual Society meeting. One of the main topics was the change over to network handling and tracking of submissions of papers to the Transactions. Preliminary testing of this system reveals the potential of eliminating the frustration of the occasional submissions that seem to disappear.

Shown in the picture from the left are Paul Wesling, Walt Trybula, Luu Nguyen, John Segelken, Alina Deutsch, Phil Garrou, and Jim Morris..... Not shown in this picture, but at the meeting, are editors Avram Bar-Cohen, Peter Krusius, and David Palmer.

Short Courses Abound at ECTC

This year there were 13 short courses offered in Orlando the day before the presentation part of ECTC. About 400 signed up despite all the other entertainment in the Disney World area. Continuing Education Units were earned by taking these courses. Al Puttlitz, VP of Education, was the driving force behind these courses. He is turning several of the most popular courses into CD-ROM based study-at-home classes to make continuing education even more available to our members. In particular, "Polymers for Electronic Packaging" by Prof C. P. Wong of Georgia Institute of Technology will be on of the first courses captured in multimedia.

In order to give a flavor of the continued education experience available at a number of the CPMT meetings, lets look at some benefits that come from one of the courses. This year, one of the more popular courses was "System on Package, SOP" presented by Rao Tummala, director of the Georgia Tech Packaging Research Center. This was an afternoon course with about 30 attendees with lots of questions.

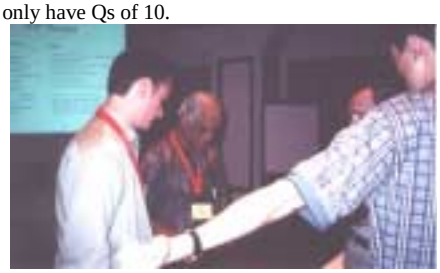
Rao started by reviewing the history of integrating electronics by enhancing packaging. Hybrid Microcircuits starting in the 70s combined unpackaged discretes to higher densities than printed wiring boards. Thin and thick film versions of hybrids have evolved and are used in many industries including the automobile. As ICs proliferated and starting being integrated in packages the term Multichip Module (MCM) became the rallying call. Many companies were started with MCM in their name. Few use the term anymore even though systems with many ICs are still produced. Terms like "integrated MCM" , "SLIM", and Microvia boards have found some acceptance. Whatever the term used, whenever there is an economic benefit more integration occurs in a package.

There was a raging argument in several of the sessions and meetings at ECTC concerning whether the future was "System on a Chip" (SOC) or "System on a Package" (SOP). Part of this is locked in the definition of "system". If a microprocessor with cache memory is a "system" then SOC has a huge part of the electronics market today. However, if a "system" must have not just digital function but analog processing, sensing, communication, or actuation then the cost-effective solution in the near term is almost always SOP. The course ended up with the following definition: SOP: single component system with two or more mixed integrated digital, RF, optical and analog

Al Puttlitz, Vice President Education

signals in the system level package or board. Under this definition of "system" there has been no SOC to date. The difficult history of Wafer scale Integration at Trilogy was mentioned as one of the driving forces behind MCM development. Making a multifunction chip technology would be expensive; even "simple" extensions such as BiCMOS are non-trivial. Design, test would take a long time and would need new tool development. In contrast, with this "system" definition some first generation SOPs are in the marketplace already.

This SOP definition differentiates it from the traditional MCM and Hybrid in that the package supplies more function than just interconnection. ICs are not designed different when committed to MCM than when destined to a single chip package. This is not necessarily true for the future of SOP. The 5-10 year vision is that RF, Opto, and digital ICs will be designed relying on the SOP to provide functions best left off the ICs. One example used was that Inductors put in a package can easily reach Qs of 100 but on an IC inductors typically only have Qs of 10.



Short Course ends in Question Session

The marketplaces of communication, hand held devices, space, computers, biomedical, automobiles, and consumer electronics all are driving the SOP evolution. For example, the use of embedded components in the board of a cellular phone is one entry into the SOP world of design. Even today the existing packaging often degrades not enhances the system. For example, the packaging of the laptop is more expensive than all the ICs and discretes. In general, an IC package slows down the circuit, outweighs the chip, and is the cause of most failures.

The increased expense of following Moore's Law in the IC world is also paving the route to SOP; a wafer fab costing $5B. One example is that although the FET switching time does decrease as the transistor dimensions are scaled down, the circuit response time which also depends on the interconnection Rs and Cs actually increases until it surpasses the switch time.

Rao saw the unfolding of SOP to be similar to that of previous technologies of PWB, IC, or MCM in that many variations of SOP technology will flower followed by convergence to an industry standard technology (because of

economy of scale). There are alternative switching/interconnection technologies that are slowly developing and may eventually eliminate the need for SOP: DNA or molecular computing, all optical processing, and quantum computing. In addition, when an application reaches very high levels of production then an SOC solution will emerge.

MCM-L,-C,-D have all tended to be replaced by a laser microvia technology applied to large panel manufacturing. This is the transition that took expensive MCMs and made them market competitive. This is expected to be a $5.7 B market by 2003. Embedded passives are transitioning from studies reported on at ECTC to manufacturing lines. There are still many different technologies with little standardization.

SOP really makes sense if the finally packaging can be done in the same clean room with a batch process. Wafer Level Packaging (WLP) where all systems on a wafer are capped, tested, and burned in at once is one example.

This interactive course influenced strongly lunch table discussions and presentation questioning for the next 3 days at ECTC; after all, SOP could well be the future for many of those attending the meeting.

ECTC Luncheon

On May 30 the ECTC organizing committee held their luncheon for the hordes of engineers at the Conference. General Chair Peter Slota introduced those at the head table amid the sounds of clanking silverware and smacking lips: Michael McShane (Vice Chair), Robert Willis (Admin Vice Chair), Wayne Howell (Program Chair), Steve Bezuk (Assistant Program Chair), Peter Walsh (Arrangements Chair), John Lau (Publications Chair), Bill Moody (Finance Chair), Mino Dautartas (Web Admin), James Bruorton (Publicity Chair), Glyndwr Smith (EIA/ECA rep).

The best paper from last year's Conference was awarded for "Comparison of Active and Passive Fiber Alignment Techniques for Multimode Laser Pigtailing" by Pentti Karioja, Jyrki Ollila, Veli-Pekka Putila, Kimmo Keranen, Jonna Hakkila, and Harri Kopola of VTT Electronics & Infotech Oulu.

The best Poster Paper went to "Modeling and Simulation of the Dynamic Response of the Electronic Packaging" by Xiaoling He and Robert Fulton of Georgia Tech.

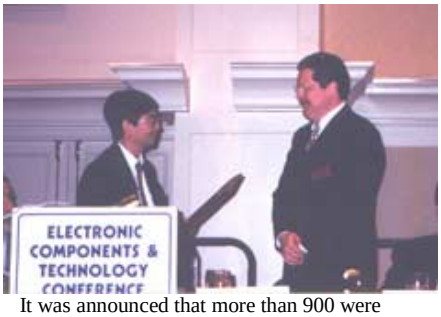
Outstanding Paper Awards for the 2000 Conference were earned for:

"Experimental and Numerical Reliability Investigations of FCOB Assemblies with Process-induced Defects" by A. Schubert, R. Dudek, J. Kloeser, B. Michel, and H. Heichl of the Fraunhofer Institute as well as T. Houck and K. Kaskoun of Motorola.

"A Compact, Low-Cost WDM Transceiver for the LAN" by Brian Lemoff, Lisa Buckman, Andrew Schmit, and David Dolfi of Agilent Laboratories.

The Outstanding Poster Paper went for "Time Dependent Material for Finite Element Analysis of Flip Chips" by Frank Feustel, Steffen Wiese, and Ekkehard Meusel of Dresden University of Technology.

Figure: Luncheons were packed and enjoyed by all. In foreground, Dennis Olsen found 2 desserts.



It was announced that more than 900 were attending ECTC from 23 countries. There were 71 Vendor Displays. On Tuesday there were 13 short courses with 400 continuing students.

A talk was given by Kazuo Eda of Matsushita Electric / Panasonic. He focused on "Mobile Internet - and the needed Advanced Packaging. He stated that there were 400 million portable phones sold last year. This compares with 30 million laptops. Using the very successful I-mode technology in Japan most users can get to the Internet. This consumer trend is called "Keitai" in Japan which is equivalent to "Handheld or Portable" in the U.S.

He quipped that the change I-mode has brought is one from "a conversation culture to a thumb culture". Flip-chip is essential to accommodate the I/O count needed in the small volume. He sees the projections easily going to nano-scale fab and billion unit/year capacity. He referred to IDM (integrated Device Module) as a sytem to simplify manufacturing by integration. One example mentioned was direct conversion detection. He sees SiGeC, multi-layer ceramic as coaxial filter resonators, and complex SAW correlators/filters as some examples of steps in this direction. He sees built-in pins, capacitors, inductors and SAW filters in multilayer ceramic packages (see SOP notes by Rao Tummala). He saw stud bump bonding using gold and conductive resin as taking over from Sn-Pb for fine pitch and operation up to 10 GHz.

Conference Report: 24th International Spring Seminar on Electronics Technology (ISSE)

The ISSE is one of the best-kept secrets in microelectronics and packaging. An annual event in Central and Eastern Europe since 1977, it has only recently begun to develop a following from the West. The 24th ISSE on May 5-9th, 2001 in Calimanesti-Caciulata, Romania, was the first to run with CPMT technical co-sponsorship. There were twenty oral paper presentations, and fifty posters. Participants came from Austria, Bulgaria, Czech Republic, Germany, Hungary, Italy, Poland, Romania, Slovakia, Slovenia, and the USA.

Although there are usually a few industrial papers, the vast majority are from university research groups, albeit often with industrial sponsors as co-authors. There are a few describing educational programs, but the vast majority are technical, with a very high proportion of papers presented by students at both the MS/Dipl.Ing. and PhD levels. Most of the papers are focussed on electronics packaging, (interconnect, manufacturing, reliability, simulation, and education.). The poster paper sessions include a very lively sequence of brief, timed summary presentations. "Best" and "excellent" paper awards are presented at the conference dinner in both oral and poster categories, with senior and junior divisions. The primary awards include prizes donated by the previous year's winners.

Local cultural visits are always a feature. This year the visits included:
**Sibiu, a city on the edge of Transylvania, and the Brukenthal Museum
**The Lotru-Vidra hydroelectric power station, with some unique features, and
**The Turnu and Cozia monasteries, close by the conference hotel.

The conference also hosts the annual business meeting of the joint Hungary-Romania CPMT Chapter, at which the new officers are elected.

The ISSE 2002 Conference Proceedings (ISBN 0-7803-7111-9, Library of Congress 2001-090155) may be obtained from IEEE (Catalog Number 01EX492.) The 25th ISSE will be held 11-14 May, 2002 in or near Prague in the Czech Republic; contact Pavel Mach of the Czech Technical University (mach@feld.cvut.cz) for information. So what does it cost to attend a conference in such an interesting and exotic location, traveling from the USA? I found a fare for just under $500 from Newark, and the conference fee of just over $200 included the hotel for 5 nights and all meals. The conference sponsors provided transportation from the airport to the hotel, and there were no other hidden costs. So the answer to the question is: "Way less than for a similar domestic meeting! And so much more interesting!" See you in Prague.

---Jim Morris, CPMT
Conference Vice President

1. Andrzej Dziedzic and Leszek Golonka (Wroclaw University of Technology) and Ryszard Kisiel (Warsaw University of Technology) are working on the establishment of the Polish CPMT Chapter.

2. At the annual business meeting or the joint Hungarian-Romanian CPMT Chapter (left to right): *Paul Svasta, Chair; *Andrei Drumea, Student Chapter Chair; Mihaela Radu (Technical University of Cluj-Napoca), Student Activities Chair; *Norocel-Dragos Codreanu, ISSE'01 Conference Director; Zsolt Illyefalvi-Vitez (Budapest University of Technology & Economics), Vice-Chair; *Ciprian Ionescu (behind), Treasurer. (*"Polytehnica" University of Bucharest)

3. Paper prize-winners at the conference dinner (left to right): Ioanna Armasu (Hyperion University, Bucharest) Excellent Poster; Andrei Drumea ("Polytehnica" University of Bucharest) Excellent Poster - Young Scientist; Ruszinko Micols accepting for Peter Bojta (Budapest University of Technology & Economics) Best Poster - Young Scientist; Norocel-Dragos Codreanu (Polytehnica" University of Bucharest) Excellent Poster; Mihaela Radu (Technical University of Cluj-Napoca) Best Poster; Angelika Paproth (Dresden University of Technology) Excellent Paper - Young Scientist; Heinz Wohlrabe (Dresden University of Technology) Best Paper; Martin Mundline (Vienna University of Technology) Best Paper - Young Scientist; Ciprian Ionescu ("Polytehnica" University of Bucharest) Excellent Paper.

4. Pavel Mach (Czech Technical University), Reinhard Bauer (University of Applied Sciences, Dresden), and Alena Pietrikova (Kosice University of Technology) during a break. Pavel will chair ISSE'02 in Prague.

5. Johann Nicolics (Vienna University of Technology), Angelika Paproth (Dresden University of Technology), and Jim Morris (CPMT Conferences VP) during a break.

6. Reinhard Bauer (University of Applied Sciences, Dresden) and Klaus Wolter (Dresden University of Technology) in Sibiu. Klaus will chair the next Academic Packaging Conference in Dresden, Germany.

Editor's Turn

The early web edition of the Newsletter went from sparse to packed, and was the only edition for six weeks because most CPMT volunteers were down in Orlando making news at ECTC for a week, and are now trying to catch up before family vacations kick in. This means most are slow at writing up the news, especially your editor.

The annual ECTC meeting sees about 15% of CPMT Society members getting together plus an equal number on non-members. There are approximately 50% of those active in the packaging and component world under one roof. If you missed the meeting you can get a copy of the proceedings through Paul Wesling the VP of Publications. Going from the proceedings and reviews you read in this Newsletter, you will be able to contact the right active engineers to help with your job.

Our Society increases value offered to all members as each member becomes more active. To help yourself and others: consider becoming active in your local CPMT Chapter (if there is one in your area), become active in an annual CPMT meeting by reviewing papers or chairing a session with a topic of interest to you, submit the article to the transactions that you have been putting off, or come to ECTC and listen and network.

I would like to thank all that helped put this newsletter together including: Jack Balde, Alina Deutsch, Marsha Tickman, Ephraim Suhir, Paul Wesling, Al Puttlitz, Rao Tummala, Phil Garrou, Tony Mak, Craig Gaw, Rajen Chanchani, Ralph Russell, Merrill Palmer, Rao Bonda, Jim Morris, Kristine Martin, and many others.

This paper version of the Newsletter was slapped together after ECTC and SensorExpo and during my company's annual Salary review. It is hard to concentrate on photo contrast and correct punctuation when your colleagues' raises depend on your complete concentration. So I apologize to all those that find their name spelled wrong or find their news full of typos.

This newsletter is seldom more than 2 days behind schedule but this time we are 2 weeks late in paper (but 2 weeks ahead on the web). Think with the web and stay ahead of the slow poke editors.

JOB OPENINGS

Engineering Project Manager
Duties: You will lead cross-functional teams to define, develop and deliver company products, features capabilities and processes. This will include developing and maintaining project plans, communicating status to all levels of the organization, participation with Functional Managers in defining and monitoring the technical direction of the project, and working closely with a variety of internal & external organizations including marketing, operations, sales and partners. *Requirements*: A minimum 5 years performing Program or Project Management tasks in an electro-mechanical design product environment is required. Must have an engineering design background. Demonstrated ability to manage complex projects and establish objectives, previous success in building and leading cross-functional teams, 5 years design engineering experience and excellent verbal, written and presentation skills will be needed as well. Technical background with power electronics equipment would be a plus. Contact: jparmer@pedley-richard.com

Japanese Business Development manager
W.L. Handler & Associates, a retained executive search firm, is seeking a Japanese Business Development Manager for a client that is a division of a high-profile company that is a world leader in electrical engineering and electronics and the fourth largest employer in the world. The division manufactures and sells electronics assembly systems and is a world leader in Surface Mount Technology. This position was created to support this division's aggressive growth plans and the incumbent will be responsible for establishing our client's business within Americas based electronics assembly plants of Japanese manufacturers. We are seeking high caliber individuals who have worked with assembly systems/SMT in some capacity, hold a technical degree, and have experience in the Japanese marketplace. While previous sales experience is desirable, the ability to establish long-term client relationships coupled with technical expertise would be a key success factor. Contact information: Angela Hodgkins, WL Handler & Associates, angelah@wlhandler.com.770-805-5020 fax

Mechanical Engineer - Packaging
Duties: You will be responsible for the conceptual design within the system packaging development group. Duties will include: systems and subsystem component packaging for new product management of detail designs and BOM's, thermal evaluation/solutions for active components, and sustaining engineering for existing products. *Requirements*: A BSME or equivalent and a minimum 5 years experience in new products development is required. This should include solid and thermal modeling experience. System packaging, Solid Works, Cosmos, CFD, Sauna and MacroFlow experience would be a plus. Contact: jparmer@pedley-richard.com

Announcement and Call for Papers
The Fifth International IEEE Symposium on High Density Packaging and Component Failure Analysis in Electronics Manufacturing (HDP´02)

June 24 - 27, 2002

Co-sponsored and jointly organized by DaimlerChrysler SIM Technology Co., Ltd, Shanghai, China. & Chalmers University of Technology, Göteborg, Sweden
Technical co-sponsorship with IEEE CPMT

Electronics manufacturing and assembly technology are playing a key technology for the progress of Chinese electronics industry. Today many multi-national companies are establishing new facilities in China for expanding their global business and interest. However, many domestic Chinese electronics companies are still using old-fashioned electronics assembly technologies. The recently established joint-venture companies use more advanced electronics assembly technologies such as surface mount, chip-on-board etc. There is a great gap in technology level between these two types of companies. Therefore, there is a need to find a forum for the domestic Chinese Electronics industry to find out the latest technologies in the developed world. The foreign advanced countries also need to have a forum to establish contacts with the Chinese scientists, engineers and decision makers.

The purpose of this Symposium is to satisfy such a need and to establish a regular forum for information exchange between Chinese industrial community and foreign specialists.

Scope for the Symposium: The Symposium will cover the following areas and subjects:
*High density packaging including electronics and opto-electronics packaging, CSP, BGA, Flip-chip, Chip on Board, Surface Mount Technology and other novel emerging technology
* High density substrate including integrated passives and active devices
* MEMS design, packaging and assembly
* Electronics manufacturing issues including cleaning issues, quality control, logistics, repair, process optimization, statistic process controls, ISO compliance, tooling or equipment, early manufacturing involvement initiatives and yield and test innovations used to enhance manufacturing processes or products related to high density substrates, single chip and multichip packaging, chip bumping and integrated component technologies
*Component failure analysis techniques including non-destructive X-ray, ultrasonic microscopy, IR-microscopy etc
*Simulation and modelling for packaging and electronics manufacturing processes
*Thermal management
* Environmental design and materials development including life cycle analysis and end of life strategy etc
* Cost reengineering, improvements and analysis for electronics packaging processes and products
Documentation: The documentation from the Symposium will be published in a proceedings with CD ROM with a full length papers (max 12 A4 pages) in English.
Location: Shanghai, China
Languages: English will be used. Simultaneous translation into Chinese
Symposium Chair: Le Luo, DaimlerChrysler SIM Technology Co., Ltd.
Symposium Co-chair: Johan Liu, Chalmers University of Technology, Sweden.

You are welcome to submit an **abstract** with max 300 words that cover the topic, experimental approach, results and conclusions for the paper by Feb 28, 2002 to Chalmers University of Technology, Division of Electronics Production, Department of Production Engineering, Attn. Dr Tiebing Wang, Se- 431 53 Mölndal, Sweden or you can email at tiebing@pe.chalmers.se. Notification of abstracts will be made by November 7, 2001. Final Acceptance of the abstract will be made by November 15, 2000. Final paper is due November 30, 2001. Please send the final paper to Chalmers University of Technology for countries outside of China.

We are also interested to have exhibitors from materials, equipment suppliers to exhibit their products. If you are interested in exhibition, please contact Dr Tiebing Wang, Chalmers University of Technology, Sweden.

Please send **abstracts** to (for countries outside of China)

Chalmers University of Technology
Division of Electronics Production
Department of Production Engineering
Mrs Carina Schmidt
Se-431 53 Mölndal
Sweden
Telephone: +46-31-706 6287
Fax: +46-31-706 6289
e-mail: carina.schmidt@ivf.se

Call for Participation for the 7th Annual 2001Workshop on Accelerated Stress Testing AST 2001

September 24th, 25th and 26th, 2001at Doubletree Guest Suites Seattle-Southcenter 16500 Southcenter Parkway, Seattle, WA
Sponsored by the IEEE CPMT Society (TC-7)
And Technically Cosponsored by IEEE Reliability Society

In addition to two days of technical presentations, this workshop will include a one-day tutorial from leaders in the field and a two-day exhibition featuring AST related suppliers. Topics related to Accelerated Stress Testing including the following **targeted topics**:

*Advanced Approaches to AST
* Environmental Testing Conditions
* Reliability Improvement Techniques
* AST Data Collection/Analysis
* Failure Analysis Techniques and Examples
*Reliability Simulation and Prediction
*Application of Physics of Failure Techniques
*Stress Screening Techniques

Our Registration forms and Page is on-line. Please Bookmark this page and visit for updates on the Workshop: http://www.ewh.ieee.org/soc/cpmt/tc7/ast2001/

Tutorial Topics Include:

*Device fabrication and failure modes
*Functional testing during AST
*SMT PWB fabrication and failure modes
* Design verification testing and AST
*AST techniques and technologies AST cost analysis
*AST success stories
*Alternative AST technologies and techniques
*AST shortcomings
*AST data collection and analysis
* Vibration and thermal theory relevant to AST
* Application of Physics of Failure techniques

Hotel Information
Doubletree Guest Suites Seattle-Southcenter
16500 Southcenter Parkway, Seattle, Washington 98188-3388
Telephone : (206) 575-8220
Fax: (206) 575-4743

Polytronic 2001

(including merging of POLY, PEP, Adhesion in Electronics)
October 21 - 24, 2001
Dorint Sanssouci Potsdam Germany
Home web site: http://www.izm.fhg.de/polytronic_2001/

You are invited to submit an abstract for participation at the 1st International Conference POLYTRONIC 2001. The idea of the conference is to continue the successful series of IEEE workshops and conferences on adhesives and polymers. This new joint conference is incorporating Polymeric Materials for Microelectronics and Photonics Application (POLY), Adhesives in Electronics and Polymeric Electronics Packaging (PEP). The main objective is to provide a forum for experts to present their findings and innovations, and to exchange ideas on topics regarding different aspects of adhesives and polymers in microelectronic and photonics. The conference will take place at the Dorint Hotel, located in the historic center of Potsdam near Berlin, Germany.

TOPICS
Materials: themosetting/thermoplastic systems; inorganic adhesives; composites; filler materials; isotropic conductive adhesives; anisotropic conductive adhesive; pastes and films; heat seal connectors; thermally conductive adhesives; polymers with adapted refractive index; photosensitive polymers; high temperature materials; PCB materials, polymer thick and thin films, low and high dielectric materials.
Processing and Manufacturing: Lamination; printing; dispensing; spraying; transfer techniques; injection and transfer molding; potting; adhesion improvement; curing; equipment; statistical process control; economic analyses.
Applications: electrical conductive adhesive joining; underfill; glob tops; die attach; potting compounds; encapsulation; polymer coatings; shielding; smart card tags; plastic packages; optoelectronics and photonics; MEMS; microelectronic systems; polymer optical fibers; polymer wave guides; ultra thin systems; polymer electronic devices; organic displays; polymer batteries; new and emerging technologies.
Design: design, modeling, and simulation of materials and systems.
Reliability and Testing: thermo-mechanical behavior; degradation mechanisms; adhesion; hermeticity; accelerated testing, humidity and environmental sensitivities; non-destructive testing methods; stress behavior.
Environment: Ecology and toxicology; life cycle analysis.

General Chair: Rolf Aschenbrenner - Fraunhofer IZM, Germany
Co-Chairs: Jurgen Berger - VDI/VDE-IT, Germany; Bernd Michel - Fraunhofer ISM, Germany
Advisory Board: Ephraim Suhir - Lucent, USA, Johan Liu - Chalmers University

The 3rd International Symposium on Electronics Materials and Packaging 2001 (EMAP2001)
November 19-22, 2001
HYATT REGENCY CHEJU, Cheju Island, KOREA

The **EMAP2001 symposium** is organized by the Korea Advanced Institute of Science and Technology(KAIST). And it is also jointly sponsored by the IEEE-Component, Packaging and Manufacturing Technology (CPMT), IMAPS-Korea, Korea Society of Mechanical Engineers, The Institute of Electronics Engineers of Korea(IEEK), and ASME Korea Section.

Following the tremendous success in the last two EMAP conferences in Singapore and Hong Kong, which were attended by delegates from 10 major countries, the third symposium will be held in Korea. It will be one of the major conferences on electronic materials and packaging ever to be held in Korea.

Meet world-renowned exports from the Asia-Pacific region, USA and Europe. Join us and get in touch with leading-edge technologies, and find out more about Korea's electronic packaging industries.

Major Topics of Symposium

*Advanced Electronic Packaging Technologies: Wafer Level Packaging, Flip Chip, CSP, DCA, MCM
* Packaging Materials and Processes: Lead-free Solders, Adhesives, Underfills, Encapsulants, PCBs
* Interconnect Technologies: Wire bonding, Fine Pitch, Micro via, Build-up Technologies
* Materials Characterization, Testing and Measurements: Electrical, Thermal, Chemical, Mechanical
* Thermal Management of Packaging
* Package Design, Modeling and Simulation
* Sensors and MEMS Packaging
*Reliability and Failure Analysis: Interfacial Phenomena, Delamination, Moisture effects Polymers and Ceramics for Electronic Applications, Thin films/coatings, Metallization

Important Dates

July 31, 2001 Abstract submission
August 15, 2001 Notification of abstract acceptance
September 30, 2001 Full manuscript due
October 15, 2001 Registration/hotel accommodation

Abstracts and Papers

An electronic form(MS-Word format) of one-page 300 words abstract with name, address, phone/fax number, and e-mail address should be submitted to the Secretariat of Symposium, emap2001@me.kaist.ac.kr by July 31, 2001. Details of further information including registration and accommodation will be announced later through the EMAP2001 homepage http://me.kaist.ac.kr/~emap2001.

Final Program
Future Directions in IC and Package Design Workshop (FDIP)

sponsored by: CPMT Society of the IEEE
organized by:CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-12)
October 27, 2001 -- Royal Sonesta Hotel, Cambridge,MA

The goal of this new workshop is to provide a forum to address the future needs associated with the design of next generation ICs and packages. The Technical Program Committee solicited invited presentations from experts in the university and industrial communities. The workshop is held in conjunction with the 10th IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP 2001) in order to enhance this conference with presentations that give directions for future requirements and developments in the area of electrical analysis and design. The workshop will foster active participation and discussions from all the speakers and attendees during the meeting.

Workshop Chairs: Alina Deutsch & Madhavan Swaminathan

Program

11:00 am - 1:30 pm Registration for workshop and EPEP
1:15 - 1:30 pm Welcome Remarks, Madhavan Swaminathan, GIT, Alina Deutsch, IBM

SESSION I: SYSTEM DESIGN

Session Chair: Chi-Shih Chang, Kulicke & Soffa
1. Next Generation System Design Challenges and Opportunities -- Derek Tsai, SUN Microsystems
2. System and Package Design Using the Low-Power Transmeta Processor -- Robert Montoye, IBM
3. Optimization of Electrical Package Design and PCB Design for CSP Age -- Atsushi Nakamua, Hitachi, Japan

SESSION II: TECHNOLOGY AND TOOLS

Session Chair: Harold Hosack, Semiconductor Research
4. Integration of RF Elements and Passives for Telecommunication -- Paul Collander, P. Laukkala, R. Vogel, Nokia Networks, Finland
5. Optical Interconnections Inside the Processor Box Lewis Terman, IBM Watson Research Center
6. Fast Solvers and "Full Problem Analysis", the Remaining Challenges -- Jacob White, MIT

Workshop will be held at the **Royal Sonesta Hotel**. The address is 5 Cambridge Parkway, Cambridge, Massachusetts 02142-1299, phone: (617) 491-3600, fax: (617) 661-5956. The hotel is holding a block of rooms for participants at a special rate of $125 and the rest at $195 plus 4% city tax and 2.75% CCF tax. Reservations must be made by calling the hotel directly by October 7, 2001 to receive these rates.

Additional information may be obtained from the workshop chairs:
Alina Deutsch or Madhavan Swaminathan
deutsch@ieee.org or madhavan.swaminathan@ece.gatech.edu
and the workshop administration:
Paul Baltes at epd@engr.arizona.edu or phone: (520) 621-3054
fax: (520) 621-1443

Updates will be posted at the **workshop web site** at:
http://www.cpmt.org/conf/fdip01/fdip.html and
http://www.epep.org.

Call for Abstracts

ITherm 2002: Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems

May 29- June 1, 2002

Sheraton San Diego Hotel & Marina, San Diego, California

ITherm 2002 is an exploration of thermal, thermomechanical and emerging technology issues associated with all aspects (die to system) of electronic systems: from pagers to cell phones, from lap-top computers to supercomputers, from consumer and automotive to space electronics.

ITherm 2002 will be **co-located with ECTC 2002**, which offers a broad range of current and new developments in all areas of electronic technology. In addition to paper presentations and panel discussions, ITherm 2002 will include vendor exhibits, keynote lectures by prominent speakers, and professional short courses. Please visit our web site at http://www.itherm.org/ for latest conference related information. Original papers are solicited in general areas of Thermal Management, Mechanics (thermo-mechanical and mechanical) issues and related issues in Emerging Technologies.

Thermal:

· Natural and forced convection air-cooling
· Liquid cooling
· Novel cooling techniques: phase change, heat pipes, thermosyphon, liquid-cooled heat sinks and evaporation
· Microchannel, micro- and nano-scale heat transfer and fluidics
· Thermal management and mechanical issues in high power dissipation packages and systems including novel heat sinks.
· Active: thermo-electric, air movers, refrigeration
· Thermal aspects of systems-on-a-chip
· Methods for mitigating effects of extreme thermal environments
· New approaches to microelectronics thermal management
· Experimental characterization: methods and measurement techniques in thermal management, thermal contact resistance, flow and temperature visualization, performance of thermal interface materials (adhesives, thermal paste)

Mechanics:

· Role of fracture mechanics in electronic packaging
· Solder joint reliability and fatigue: modeling and experimental
· Solder profile modeling, fatigue mechanics of packages, interconnects
· Mechanical reliability of advanced packages, and multilayered structures manufacturing/assembly and field-use conditions
· Impact and vibrational analysis of packages, sub-systems, and systems
· Experimental methods, model validation, material characterization
· Mechanics of environmental-friendly materials in electronics
· Thermal and thermomechanical characterization of materials: organics (dielectrics, solder mask, LTCC etc., solders, PB-free solders)

Emerging Technologies: Thermal, Thermomechanical and/or related underlying multidisciplinary issues in:

· Space systems: earth orbiting and deep-space missions
· Fiber-optics interconnect systems
· Free space optical interconnects
· MEMS: device and package level reliability issues.
· Mechanics, material and process related issues in Nanostructures.
· Portable/handheld electronics, such as cell phone, pager, notebooks, computers, peripheral hardware, disc drives, displays, printers
· Medical, telecommunication, and automotive systems

Panel Discussions:

· Proposals are solicited for panel discussion topics addressing contemporary issues of broad interest to ITherm. These should include a title, an abstract describing the theme(s) to be addressed, and a list of potential panelists.

Software Tools/Techniques: Design, Analysis, Simulation

· CAD, CFD, FEA, EDA software tools and trends in their interoperability.
· Flow network modeling
· Model validation/benchmarking
· Development of behavioral (or compact) models (e.g., component, heat sinks)
· Interoperability and emerging standards across cross-disciplinary software tools

To submit a paper for consideration, please enter a 250-word abstract by August 15, 2001 at the ITherm website at http://www.itherm.org/.

CALL FOR PAPERS EPEP

October 29 - 31 -- Cambridge, Massachusetts

Co-Chairs: George Katopis, IBM Corporation,
John Prince, The University of Arizona

The general **subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. A forum will be provided for the discussion of the following topics as they relate to chip-to-chip and on-chip interconnections in electronic systems:

Package analysis, numerical methods and algorithms
Electro-magnetic analysis tools
Advances in transmission-line techniques
Power distribution and package resonance
Switching noise in multi-layered structures
Impact of OE/EO transducers on performance of module
RF/microwave packaging structures
and about 40 related topics....

Additional information may be obtained from the Meeting Co-Chairs or the Administrative Chair:
George Katopis, email: katopis@us.ibm.com
John L. Prince, email: prince@ece.arizona.edu
Paul Baltes, email: baltes@engr.arizona.edu

PAPER SUBMISSION

Authors are invited to submit papers describing new technical contributions in the areas broadly covered in the Call for Papers.. Submissions should be sent, not later than July 10, 2001, to:Engineering Professional Development
University of Arizona
1224 N. Vine Avenue
Tucson, AZ 85719
Tel: 520-621-5104/Fax: 520-621-1443
Email: epd@engr.arizona.edu