Components, Packaging, and Manufacturing Technology Society Newsletter

The Global Society for Microelectronics Systems Packaging

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www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

PRESIDENT'S REPORT

IEEE CPMT viewed as one of the best IEEE Societies

IEEE Technical Activity Board (TAB) of IEEE recently reviewed our CPMT Society as well as a number of other IEEE Societies. The following is a summary of this review for our Society.

1. Overall **CPMT is a very well managed and dynamic Society**. The Society Review Committee thanks the Society and Prof. Rao Tummala for an excellent presentation about the Society's past and future plans.
2. They are impressed with the effort to **develop strategic direction** and with the appointment of Strategic Directors in Regions 8 and 10 to focus on specific activities.
3. The IEEE TAB likes **positive directions** of CPMT Society such as membership, subscriptions, subscription rates, global conferences, recruitment, and educational programs.
4. They suggest that candidates standing for election or persons accepting committee assignments be **informed of the time** required to actively participate.

The TAB indicated that they would like to see the best practices being implemented by CPMT to be used by other Societies such as establishment of on-going strategy focus and the slide presentation used by Prof. Tummala at the TAB review.

CPMT continues and advances its globalization focus

CPMT continues to make outstanding progress in its globalization. Better than 40% of the Society's membership comes from outside the US. The board membership from outside US continues to grow as well. Plans are underway to further improve both.

The most noteworthy activity during the last three months has been the leadership meetings in Regions 8 and 10; in Kaohsiung, Taiwan and in Singapore in December and in Berlin, Germany in January. The intent of these regional leadership meetings, typically attended by about 10-20 regional leaders, is to identify and attract leaders who are willing to develop CPMT programs in conferences, education, publications and membership for the benefit of the region.

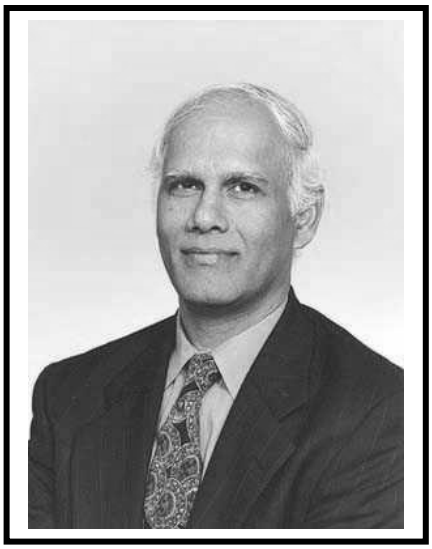
The board members who contributed greatly to the success of these leadership meetings include Paul Wesling, who acted as the overall coordinator for Region 10 meeting, and Jim Morris, CP Wong, and Bill Chen, the Strategic Director for Asia. A similar leadeship meeting led by Rolf Aschenbrenner, the Strategic Director for Europe, Johan Liu, Jim Morris, Tony Chan, and CP Wong was successful as well. This leadership had two milestones: a face- to- face discussion with Europen IMAPS leaders that included Peter Barnwell (North American IMAPS President), Karel Kurtzweil, the IMAPS Europe President, Eric Beyne, the 2005 IMAPS Europe Conference General Chair and Soren Norlying and Paul Collander, the IMAPS Nordic executives, These discussions led to the formation of CPMT-IMAPS committee to review, discuss and propose collaborative programs between the two Societies for the benefit of Europe.

The second milestone is an Emerging Technology Workshop sponsored by CPMT Society, organized by Rolf Aschenbrenner, with such emerging technology topics as Nano-packaging, Bio-packaging, conductive adhesives, and flipchip with underfill, was attended by more than 60 technologists from throughout Europe.

CPMT Embarks on Nano-Packaging as its Next Frontier

CPMT believes Nano-packaging to be the next frontier both at IC level and systems level. To realize its potential, CPMT is proposing a First International Workshop on Nano-packaging to be held in March 2004. Please see the call for abstracts in this Newsletter.

-Rao Tummala



CPMT OFFICERS

President -- Rao Tummala, +1 404 894 9097
Technical VP -- Phil Garrou, +1 919 248 9261
Administration VP -- H. Anthongy Chan, +1 408 924 3656
Treasurer -- John Segelken, +1 540 961 1685
VP Publications -- Paul B. Wesling, +1 408 252 9051
VP Conferences -- James Morris, +1 607 777 4774
VP Education -- Albert Puttlitz, FAX +1 802 879 0466
Senior Past President -- Ralph Wyndrum, +1 732 219 0005
Junior Past President -- John Stafford, +1 602 413 5509
Secretary -- Ron Gedney, +1 703 834 2084
Executive Director -- Marsha Tickman, +1 732 562 5529
IEEE VP TAB -- Ralph Wyndrum, +1 732 219 0005

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Standing Committee Chairpeople

Student Chapter Development -- William D. Brown, wdb@engr.uark.edu
Distinguished Speakers -- A. F. Puttlitz, FAX +1 802 879 0466
Fellows Search--Rao Tummala-rao.tummala@ee.gatech.edu & David Palmer-d.palmer@ieee.org
Fellows -- C. P. Wong, cp.wong@ieee.org
Constituition & Bylaws -- Tony Mak, +1 972 371 4364
Finance -- Ralph Wyndrum, Jr., r.wyndrum@ieee.org
Long Range Planning -- Dennis Olsen, d.olsen@ieee.org
Standards -- "Jack" Balde, +1, 908 788 5190
IEEE Books & C and D Magazine Editor, Joe Brewer, +1 386 445 2593, j.brewer@ieee.org
Membership -- Ralph Russell, cpmt-membership@ieee.org
Chapter Development -- Ralph Russell, II, see membership
Nominations -- John Segelken, +1 540 633 5781
International Relations -- Leo Feinstein, +1 508 870 0051; Europe -- Ephraim Suhir, +1 908 582 5301; Far East -- W. T. Chen, +65 874 8110
Joint Committee on Semiconductor Manufacturing -- G. C. Cheek

Next News Deadline:
June 5, 2003 **2**

CPMT SOCIETY NEWSLETTER

Editor: David W. Palmer, email: d.palmer@ieee.org, FAX +1 505 844 7011, Tel: +1 505 844 2138
Composition: Alina Deutsch: deutsch@us.ibm.com
Proofreading: S. Puccetti & Amity Ming

CPMT Archival Publications

Publications VP: Paul Wesling, email: p.wesling@ieee.org, Tel: +1 408 252 9051.
Transactions-CPT editor, Avram Bar-Cohen, Univ. of Maryland, 2181B Martin Hall, College Park, MD 20742 USA, Tel: +1 301 405 3173; email barcohen@eng.umd.edu
Transactions-AdvP editor; G. Subbarayan, Purdue University, ME Department, Tel: +1 765 494 9770; email ganeshs@ecn.purdue.edu
Transactions EPM editor, Walter Trybula, Tel +1 512 356 3306, email w.trybula@ieee.org

Technical Committee Chairpeople

TC-1 Electrical Contacts, Connectors and Cables--Gerald Witter, Chugai, +1 708 244 6025
TC-2 Discrete and Integral Passive Components—Leonard Schaper, Univ. of Arkansas, +1 501 575 8408
TC-3 IC and Package Assembly – Michele Berry, Intel michele.j.berry@intel.com
TC-4 Manufacturing Design & Process—Walt Trybula, SEMATECH, +1 512 356 3306
TC-5 Materials--Rajen Chanchani, Sandia Labs, +1 505 844 3482, r.chanchani@ieee.org
TC-6 High Density PWB packaging -- John Segelken, jsegelken@Actmicrodevices.com, and Connie Swager, swager@us.ibm.com
TC-7 Environmental Stress & Reliability Test--Kirk Gray, k.a.gray@ieee.org
TC-9 Thermal Management & Thermomechanical Design--Tony Mak, Dallas Semi, +1 972 371 4364
TC-10 Fiber Optics & Photonics—Frank Shi, UC Irvine email: FGSHI@uci.edu
TC-11 Electrical Test -- Bruce Kim, Bruce.Kim@asu.edu, Tel: +1 480 965 3749
TC-12 Electrical Design, Modeling and Simulation--Madhavan Swaminathan, G Tech, +1 404 894 3340
TC-13 Power Electronics Packaging--Doug Hopkins, SUNY Buffalo, +1 607 729 9949, d.hopkins@ieee.org
TC-14 Systems Packaging—Yoshitaka Fukuoka, weisti.fukuoka@rose.zero.ad.jp
TC-16 RF and Wireless-- Craig Gaw, Motorola, +1 480 413 5920, c.a.gaw@ieee.org
TC-17 MEMS and Sensor Packaging—Eric Jung, IZM Berline email: erju@izm.fhg.de
TC-18 Wafer Level Packaging—Michael Toepper, IZM Berline toepper@izm.fhg.de
TC-19 Education--Rao Tummala, G Tech, +1 404 894 9097
TC-21 Green Electronics Manufacturing and Packaging, Hansjoerg Griese, Email: griese@izm.fhg.de

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53rd Electronic Components & Technology Conference Highlights

(New Orleans, Louisiana .....May, 2003)--The Advance Program for the 53rd Electronic Components & Technology Conference at the Sheraton New Orleans Hotel has been completed and will feature over 300 technical papers presented by leaders in their field representing countries from around the world.

The conference is organized into 38 technical sessions covering a wide range of topics, including optoelectronics, RF and MEMS packaging, 3D and high performance package design, flip chip and Pb-free interconnections, wafer-level packaging and manufacturing, reliability test methods, and electrical, thermal and mechanical modeling. Two technical sessions will specifically explore topics related to engineering education and web-based packaging education for the 21st century.

Two poster sessions on Wednesday, May 28 and Thursday, May 29 will offer unique opportunities for authors and attendees to interact, discuss in detail, and exchange ideas in a more relaxed forum.

New this year is the International Academic Workshop (sponsored by the Packaging Research Center) to be held in conjunction with ECTC as a one-day workshop on Tuesday, May 27. The purpose of this workshop is to make the academic community aware of the significant advances being made worldwide in next generation electronic packaging education and to promote international collaborations that serve the global technical community.

The 53rd ECTC will feature a Tuesday evening, May 27 Panel Session on "Trends in Advanced Packaging Development and Manufacturing", and a Wednesday evening, May 28 Plenary Session organized by Dr. Phil Garrou focusing on "The Coming Changes in IC Technology".

An all-day educational seminar will be offered on Tuesday, May 27, 2003 consisting of 14 short courses. Dr. Ronald E. Scotti and the short course committee have brought together industry experts from a wide variety of disciplines to offer state-of-the-art technology reviews and updates in condensed half-day and full-day formats. Course topics cover a wide range of technologies, including RF/wireless packaging, Ghz IC packaging, photonic-optoelectronic packaging and systems, systems on a package, chip scale and wafer scale packaging, integrated passive technology, and polymers for electronic packaging. These courses are eligible for Continuing Education Unit (CEU) credits.

The Technology Corner on Wednesday afternoon, May 28 and Thursday, all-day May 29 will feature exhibits of the newest products and services available in an environment that enables discussion and interaction with the managers, engineers, and scientists attending ECTC.

ECTC attendees can receive Conference Proceedings as a CD-ROM or a printed version. Both the CD-ROM copy and printed may be purchased for an additional $50 charge.

We encourage any editorial coverage you can give the conference and will provide complimentary registration and proceedings for your editorial representative planning to attend.

The 53rd ECTC Advance Program is available from:
Jim Bruorton, ECTC Publicity Chairman
2003 Electronic Components & Technology Conference
c/o KEMET Electronics Corporation
P.O. Box 5928
Greenville, SC 29606
Telephone: (864) 963-6621
Fax: (864) 963-6444
Email: margieballinger@kemet.com

or you may visit the ECTC website at www.ectc.net and download the information and program from that location.

The 53rd ECTC conference is sponsored by the Electronic Components, Assemblies, and Materials Association (the electronic components sector of the Electronic Industries Alliance) and the IEEE Components, Packaging and Manufacturing Technology Society.

ECTC Promise -- an editorial

With tight travel budgets in a slow technology market, the annual ECTC promises to be the biggest ever. Many component and assembly companies (>50) have decided to use ECTC as their key exhibit place where they can meet the maximum number of industrial movers at the minimum amount of expense. There are 300 papers to be presented in 38 sessions: 5 advanced packaging, 2 RF & components, 2 education, 5 interconnection, 2 manufacturing, 5 materials and processes, 6 modelling and simulation, 4 optoelectronics, 5 quality and reliability, and 2 posters.

In addition, all day Tuesday May 27th an International Academic Workshop will be held to allow professors to compare curricula and educational perspectives. In addition, 14 professional development courses will be offered to bring members up to speed on core topics of the CPMT technologies.

This is the one meeting our Society members should insist on attending in these years of business and career uncertainty. In one week, under one roof, lots of education and networking will occur. Hotel reservations should be made by April 28 to get the lowest rate...or plan on spending your nights listening to Jazz in the clubs of the French Quarter.

(see advanced program and details of registration in this newsletter)

Academic Workshop -- New Orleans

Tuesday May 27, 2003 from 8:15 am to 5 pm

This International Academic Conference Workshop will provide opportunity for faculty to present courses, curriculum, and other educational programs they have developed; as well as exchange ideas on how to improve the status of microsystem packaging education.

Structure:

Presentation Session: Novel Electronic Packaging Education Program

Panel Session: Assessment of Packaging Courses and Programs
Moderator -- Avram Bar-Cohen, University of Maryland

Round Table Discussion: International Partnership and Exhange Programs
Moderator -- Rao Tummala, Georgia Institute of Technology

ECTC Plenary Session

Wednesday Night -- May 28th -- 7-9 PM

This session is one of the most anticipated features of ECTC. This year Chair Phil Garrou (DOW at MCNC) intends to provide insight and perspective from technical and business leaders of dynamic companies at the forefront of technology.

Structure

Status of Non-silicon High Frequency Technology
Strained Silicon Technology
Dr. Eugene Fitzgerald -- MIT/Amberwave Inc
Entering the Era of Polymeric Transistors
Dr. Henning Sirringhouse -- Plastic Logic

CPMT Meeting of Interest to Members 2003

**IEEE Internat Symposium on Quality Electronics Design (ISQED), March 24-27, 2003, San Jose, California; Ali Iranmanesh, Alii@tavanza.com, +1 408 330 1236, fax +1 408 986 5095.

**CARTS 2003, Capacitor and Resistor Technology Symposium, March 29 - April 4, 2003, Scottsdale, Arizona, www.cti-us.com.

**4th Conf on Thermal & Mechanical Simulation & Expts in Microelec & Microsyst (EUROSIME), Aix-en-Provence, France, March 30 - April 2, 2003, compete@mta.fr, fax 33 1 4451 7401

**2003 International Reliability Physics Symposium, Dallas, Texas, March 30 - April 3, 2003, http://www.irps.org

**14th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference & Workshop (ASMC), March 31 - April 1, 2003, Munich Germany: Margaret Kindling, mkindling@semi.org, fax: 1 202 289 0441 or Johanna Turpeinen, europrograms@semi.rog, fax +32 2 511 4345.

**2003 International Conference on Electronics Packaging (ICEP), Tokyo, Japan, April 16 - 18, 2003, imaps-j@jiep.or.jp, fax 81 3 5310 2011

**5th International Conference on Electronics Packaging Technology (ICEPT 2003), Shanghai, China, April 21 - 23, 2003, jjwant@srcap.stc.sh.cn, fax 86 21 65643529

**International Spring Seminar on Electronics Technology, High Tatra, Slovakia, May 8 - 11, 2003, alena.pietrikova@tuke.sk, fax 421 55 6023195

**7th IEEE Workshop on Signal Propagation on Interconnects (SPI'03), May 11-14, 2003; Siena Italy, ; canavero@polito.it, +39 011 564 4060.

**2003 IEEE 53rd Electronic Components and Technology Conference (ECTC), May 27 - 30, 2003, New Orleans, Louisianna., jadams@eia.org, fax 1 703 907 7549

**Int'l IEEE conference Environment on Compatible Microelectronics Packaging, Manufacturing, & Design Technology, June 23-24, Hong Kong; June 25-27, 2003 Shenzhen, China; angie Wong, wywong@ee.cityu.edu.hk, fax 852 2788 7579.

**InterPACK'02 (Inter-society Packaging Conference), July 6-11, 2003; Maui, Hawaii; S. K. Bahattacharya, swapan@ee.gatech.edu, fax 1 404 894 0957.

**International Electronics Manufacturing Technology (IEMT) Symposium July 16-18, 2003; San Jose CA Gloria Lou: glou@semi.org +1-408-943-7048 (fax +1-408-943-7913)

**2003 Photonic Devices and Systems Packaging (PhoPack) Symposium, August 10-12, 2003, San Francisco, www.cpmt.org/phopack/, phopack@ieee.org.

**2003 Photonic Materials Reliability (PhoMat) Symposium, August 12-13, 2003, San Francisco, 222.cpmt.org/phopack/phomatcall.pdf, Ephraim Suhir, esuhir@iolon.com.

**9th International Workshop on Thermal Investigations of ICs & Systems (Therminic) September 24-26, 2003; Aix-en-Provence, France Bernard Courtois THERMINIC@imag.fr

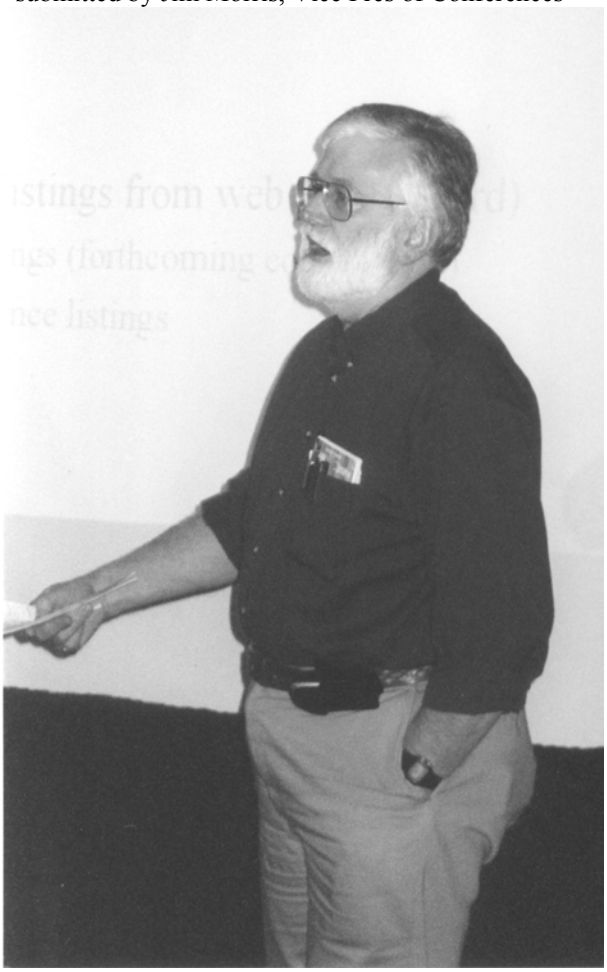
**TC-7 2003 Workshop on Accelerated Stress Test & Reliability (AST'03) October 2-4, 2003; Seattle WA Mark Morelli Mark.Morelli@Otis.com +1-860-676-6140

**MST'03 (Microsystems Technologies), Munich Germany, October 7 - 8, 2003, Erik Jung, erju@izm.fhg.de, fax 49 30 46403 161

**3rd Internat IEEE confer on Polymers & Adhesives in Microelectronics & Photonics (Polytronic 2003), Montreux, Switzerland, October 20 - 23, 2003, Bernard Courtois, polytronic2003@imag.fr

**5th Electronics Packaging Technology Conference (EPTC'03), December 10-12, 2003, Singapore; Mahadevan Iyer, iyer@ime.a-star.edu.sg, fax +65 6774 5747.

--submitted by Jim Morris, Vice Pres of Conferences



Prof. Jim Morris, Vice President of Conferences

CHAPTER NEWS

REGION 10 CHAPTER ACTIVITY ROUND -UP

1) CPMT Taipei Chapter: The Chapter organized-4th International Symposium on Electronic Materials and Packaging (EMAP 2002) from December 4th to 6th at Splendor Kaohsiung Hotel, Taiwan. This 3 day well attended conference with 19 technical sessions included more than 80 papers with 7 keynote address (Dr. Charles E. Bauer, Dr. Yu Tsukada, Dr. Horatio Quinones, Dr. Micheal Pecht. Dr. Yukio Furuta, Dr. Kim Ilung and Dr. Rao Tummala) on topics such as advanced packaging, materials characterization, testing and measurements, thermal management, package design, modeling and simulation, reliability and failure analysis, polymers and ceramics.

This international event was followed by "Leadership Training Workshop" on 6th December for Region 10 CPMT Chapter chairs addressed by several CPMT Board of Governers/members. Discussions included CPMT Society's approach and perspectives, special directives for organisation of technical programmes and other aspects of development of CPMT Chapters in Region 10.

2) Hong Kong Chapter : The CPMT Hong Kong Chapter under the Chairmanship of Mr. Cheung Yiu-Ming Ken has planned to organize **two short courses** :
i) Half day workshop on "BGA Solder Joint Ball Reliablity - Failure Modes and Test Methods" by Mr. Keith Newman.
ii) Full day workshop on "Cleanroom Technology for Microelectronic Photonic Packaging" given by Dr. Ken Goldstein.
Both programmes will be arranged by Mr. Y.H.Chan, duly supported by Mr. Derek Or Siu Wing as Secretary and Mr. Huili Fu as Treasurer of the Chapter.

3) Malaysia Chapter: The CPMT Malaysia Chapter has planned to organize **a short course** by Prof. K.N. Seetharamu (Chapter Chair) and Dr. Vishwas Wadekar on "Advances in Heat Transfer and Heat Exchanger Technology" on 18 & 19th March 2003 at School of Mechanical Engineering, USM Engg Campus, 14300, Nibong Tebai.

4) India Council Chapter : The CPMT India Council Chapter organized a co-sponsored a Conference on **"New Vistas of Electronics Manufacturing"** on Jan 22 and 23rd 2003 at Hotel Oberoi, Bangalore. The two day manufacturing industry oriented conference included 7 technical sessions with 26 technical papers (including 9 papers from experts from Germany, Switzerland, Singapore and USA). The discussions covered relevant latest technology inputs on Electronic Manufacturing Technology - thro' hole technology and SMT PCB's, SMT assembly Technologies, contract manufacturing, Lead free solder printing etc.

CPMT India Council Chapter Technical Activity this year will be supported by Prof. M.M. Shah as Secretary and Mr. S.A. Kukade as treasurer.

Compiled by Dr. P.B. Parikh
Chair, CPMT India Council Chapter

Boston Chapter breaks Silence

Boston IEEE/CPMT Meeting Notes for 2002 and 2003
by Dan Bauks Chapter Chair (dzbauks@aol.com) (978-692-1559)

The Boston CPMT chapter usually has 5 to 6 meetings a year with meetings held the third Tuesday of the month at the Sun Computer East Campus complex in Burlington, MA. (See www.ieee-boston.org for monthly meeting details) Some recent meetings include:
2/25/02 "Flip Chip for Non-Experts" by George Riley - Worcester, MA
5/8/02 "Mems Fabrication in the MIT Micro Engine Project" by Dr. Ravi Khanna - MIT; Cambridge, MA
11/19/02 "Mems Components for Chemical & Biological Detectors" by Dr. John Wright of Sionex Corporation; Waltham, MA
2/25/03 "Liquid Crystal Tunable Filters" by John Noto - Scientific Solutions; No. Chelmsford, MA (Picture)
3/24/03 "Semiconductor Polymer Design for Low-Cost Plastic Transistors" by Dr. Beng Ong, Xerox Research Centre of Canada
4/22/03 "High Density Packaging" by Dominique Numakuba of DKN Research - Haverhill, MA

John Noto getting congratulated by Dan Bauks

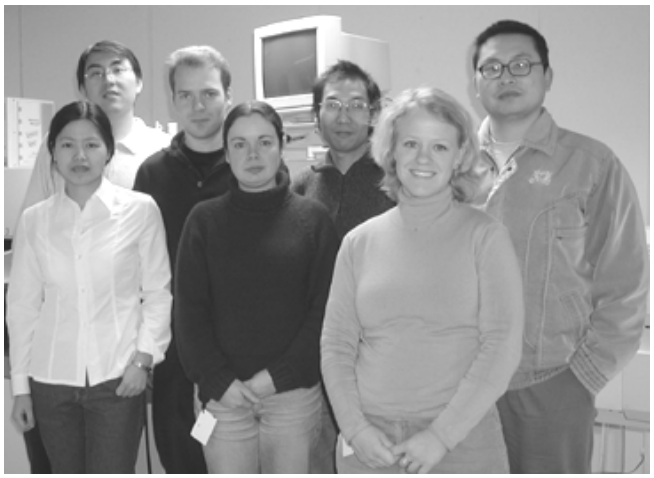
The Boston CPMT local chapter will also be presenting a free Educational Program at the IEEE ELECTRO 2003 Conference held June 10th during the Nepcon-East Show at the Bayside Exposition Center in South Boston. (See www.nepcon.com and click on Nepcon-East Show and Electro Program)
10:00 - 11:00 AM "Lab-On-Chip Technology" by Dr. Colin Brenan of BioTrove Inc. Cambridge, MA (www.biotrove.com)
11:00 - 12:00 PM "Laser-Micro-Machining" by Patrick Sercel of JPSA Inc. Hollis, NH (www.jpsalaser.com)
2:00 - 3:00 PM "Flip-Chip and Advanced Packaging Assembly" by Dan Crowley of MRSI/Newport N.Billerica, MA (www.mrsigroup.com & www.newport.com/mrsi)
3:00 - 4:00 PM "Robotic Haptic Systems" by William Townsend of Barrett Technology Cambridge, MA (www.barrettrobotics.com)

Sweden's Student Chapter

A new IEEE CPMT Student Branch Chapter has officially been formed on the 6th of December 2002 at the Division of Electronics Production, Chalmers University of Technology, Gothenburg, Sweden.

The student branch chapter faculty advisor is the IEEE senior member and chairman for the IEEE Joint Scandinavian CPMT Chapter, professor Johan Liu. The board for the chapter is constituted by Cristina Andersson as chairwoman, Gang Zou, vice chairman, Lisa Ekstrand, secretary and Zhiming Mo as treasurer. All the board members are Ph.D. students at the division of Electronic Production, headed by professor Johan Liu. The branch has presently 13 members, both Ph.D. and undergraduate students at Chalmers University of Technology. Some of the members can be seen in the picture

From left: Caroline Chen, Liqiang Cao, Anders Andrae, Cristina Andersson, Gang Zou, Lisa Ekstrand and Zhimin Mo



Synopsis of the

2002 Optoelectronics Packaging and Manufacturing Symposium,

Binghamton University, State University of New York, Binghamton, New York October 21-23, 2002

John W. Stafford
JWS Consulting P.L.C.
j.stafford@ieee.org

There were **15 presentations** made at the symposium. The presentations were: (1) "Current State of Optoelectronic Networking" by Gary Kunic, (2) "Optoelectronic Opportunities and Developments in the EMS Space" by Srinivas Rao, (3) "International Standards for Optoelectronic Technology" by Thomas D. Newton, (4) "Optoelectronics and Automation for First Level Package Assembly" by Richard Boulanger, (5) "Optimization of the Fiber Optics Splicing Process" by Harjinder Lahhar, (6) "Evaluation of Soldering Techniques in Optoelectronics Assembly" by Alan Rae, (7) "A preview of the NEMI Year 2002 Optoelectronics Roadmap" by John W. Stafford, (8) "The Evolution of Optics in Printed Circuit Boards" by David Haas, (9) "Selective, Scalable Semi-Automation of Fiber Optic Components" by Ernie Bancroft, (10) "Optoelectronics Packaging , Design, Materials and Process Issues by Peter Borgesen, (11) Packaging of High End Photonics Components" by Kevin Dreyer, (12) "40G for $4; Essentials for Next Generation Passive Optical Components" by Laurence A. Harvilchuck, (13) "Demand for Specialist Materials and Components in Optoelectronics" by Melanie Wuthenow, (14) "Optoelectronics Business Development in Asia" by E. Jan Vardaman and (15) "The challenges of Optical MEMs Assembly" by Larry Felton. In addition students at Binghamton University who were working on electronics packaging research projects as part of the Integrated Electronics Engineering Center (IEEC) presented poster papers on their research results.

The keynote speaker was Gary Kunis, VP Cisco Systems. In his second slide he succinctly pointed out the state of network deployment with his statement "The bandwidth party is over". Business deployment is now focusing on metro optical, Ethernet to the home/curb and storage networking. A more realistic business model for deployment of optoelectronics is emerging. He went on and gave an excellent optical network overview.

In a short synopsis it is impossible to give even a short review of the many excellent presentations but there were a number of common themes in several of the presentations. A theme that was echoed in a number of presentations was the need **for standards** to be more quickly developed due to the rapid technology advances. This is particularly true for packages, etc. A number of presentations reviewed optoelectronics packaging and assembly issues including the vexing problem of **fiber handling and splicing**. To complement these presentations a number of presentations discussed the benefits of on board and in board **optical wave guides** and their applications using flip chip vertical cavity surface emitting Laser (VCSEL's) and detectors. Such technology application would be used in Level 3 backplanes. Methodologies for coupling into and out of the wave guide were broadly reviewed and discussed. A number of the presentations focused on the benefits of **automation** (particularly yield) the cost effectiveness of automation.. The review by E. Jan Vardaman on the Optoelectronics Business Development in Asia highlighted the growth and diversity of the optoelectronics technology and business infrastructure in the Peoples Republic of China.

Editor's Turn -- Fellows

Once again your Society board of governors put a simple stake in the ground starting a new strategy for getting Nominations for the IEEE Fellow award. In the past it has been a somewhat market system where those deserving of the nomination and those qualified to nominate and serve as references had to independently come up with the desire to fill out the paper work. This system has worked well for years resulting in 3 - 6 new Fellow awards to CPMT members each year (although approximately half of these nominations came through other societies for our members).

This year Jack Balde led the charge by enlisting a panel of 7 CPMT super-volunteers to make a list of our most deserving members (based on both Society service and technology contributions). The top dozen of this list were given a chance to be nominated (not all volunteers want this honor…some serve best anonymously). Then a nominator volunteered for each candidate and the five Fellow References were picked from the list of 130 existing CPMT Fellows (provide by our executive director, Marsha Tickman). In addition, the historic nomination process continued to generate a few additional packages.

Since each nomination package involves 7 engineers all meeting the same deadline, it is still not clear how many candidates will be submitted by our Society to the IEEE selection committee (it is not unusual to lose 25% of the nominations based on incomplete paperwork). However, it looks like the number will be a bit higher than the historical number, and more to the point, at least a dozen CPMT volunteers now know the high regard the Society has for their impressive accomplishments.

Temptation: This is the hardest Newsletter issue for your editor to produce. A small part of the difficulty is due to a "dead time" after New Year's Day when even the most fervent CPMT volunteer news reporter slows down a bit. A bigger problem is the U.S. 1040 tax form that frustrates and exhausted this editor most evenings during March. But the biggest problem is the large stack of great books that tempt to take up all my time that is not necessary to keep from starvation or job loss…call it March madness. Even as I type this a copy of "Hal's Legacy" from MIT is on the floor begging to be held. So far this month "Ex-libris" and "The Cambridge Quintet" have book-napped the editor for hours at a time. Notice most of these books took years to catch my attention, but there are 100s more just waiting to side track me. Successful editors must read a lot faster than me.

January 2003 IEEE Workshop Blarney Park Hotel, Cork, Ireland

Background

The TC-14 Workshops remain the finest diversified Workshops in Electronic Packaging, and this year was one of the most interesting. The Blarney Park Hotel is a great location for such an event, and attendance was about 60 from 10 countries.

There were many great papers, but also the usual too broad overview papers which gave little to report, and as is my policy I will report on design papers, omitting reliability issues.

Keynote Talks

The two keynote talks on Photonics were from Japan which is leading the world in photonics innovation.

Yuzo Ishi of NTT described their Opto-bump Chip with Planar Optical Connector. Though this paper was given at the ECTC it seems to be the most innovation technology with broad applicability, and should be presented again.

The light from vertical emitting VSCELS is collimated through clear epoxy bumps over each VSCEL. Mating epoxy bumps are put on the PCB substrate. The epoxy is UV cured.

The array of bumps is surrounded by solder bumps whose height is slightly greater than the height of the clear bumps. The flip chip solder connection is done in the usual SMT manner, and the clear bumps do not touch, but are maintained within a few microns.

Spacing gap of the optical bumps is 70 to 100 Microns. The assembly can be removed by the usual solder melting methods and re-used, but that is not expected to be needed.

This is an easy-to-handle technology requiring little change from conventional SMT connections. It is applicable not only to telecommunications but to many other systems applications.

A truly useful innovation.

Naohiro Hirose of ASET, Mushashino, Japan talked of their "Self-Generating Optical Waveguide Connectors". This is single fiber connection work where light from one fiber shines through a light sensitive medium, changing the refractive index and channeling the light in the future.

Not suitable for field splicing, it is more useful for backplane work.

Photonics Session

Richard Otte of Promex discussed issues in Planar Optical Backplanes. After listing the advantages and capabilities, he indicated that the principal problem is the 45 Degree interface required to take the vertical light from VSCELS into the planar waveguide.

There are three principal methods, laser cutting with a slanting laser beam, diamond saw cutting of a glass substrate and embossing grooves into the resin substrate.

The laser cutting is the most difficult to implement but the NTT technology, using a diamond saw to cut grooves in glass and filling the grooves with polymer. If the tip of the diamond grinding saw is 45 Degrees, it cuts into the glass that penetrates through the glass, and at that spot the light can hit the sloping sides of the polymer and turn the corner into the planar polymer channels. A very effective technology.

For mass production of simple optical circuits, a resin substrate can be embossed with grooves that have 45 degree ends. That is really the cheapest after the necessary tooling is made to order.

Dr. Kropp of Infineon talked of Wafer scale assembly test for Optoelectronic components. The technology involved sub assemblies of edge emitting lasers, monitor diodes and a microlens and mirror on a silicon submount at the wafer level. After assembly the parts are separated by diamond sawing and placed in the final package by pick and place.

Enabling Technologies Session II

This Session presented papers on technology for LTCC ceramic and embedding of Resistors and Capacitors.

The first presentation by Hermann Oppermmann of Fraunhofer was on Plastic core solder balls. Height could be tightly controlled, and reliability was good, but there were problems with reliability with underfills. The right underfill material and process is yet to be determined.

Invited Session on Research at IMEGO and NMRC

This session told much about the activities and capabilities at IMEGO and NMRC. Of particular note was the inertial motion tracking system. The technology is usable where GPS is not adequate. The inertial components are mounted on MEMS and include gyroscopes and accelerometers. The modules can stand accelerations in excess of 50g and rotational velocities to 3000 degree/sec.

Katrin Perssson described the work using screen-printable glass to LTCC substrates used then for anodic bonding of silicon wafers giving hermetic encapsulation. The result is an interposer for chip sale packages.

The technology is also being explored for electro-optical assembly. A mix of electronic, opto-electronics and can all be included in the same chip carrier.

A third project using LTCC was for micro-fluidic applications.

Terence O'Donnell focused on the work at NMRC on integrated magnetic components. Technologies are being developed, one for silicon and the other for PCBs.

In the PCB case, a magnetic core of a thin film of NiFe magnetic alloy is microplated onto the outer layers of the PCB and the inner copper layers are used for the winding.

Both inductors and transformers have been fabricated and the capabilities and limitations were presented, and demonstrated in a on power dc-dc converter.

Most exciting was the development of a micro connection technology using electric fields to drive electrophoretic transport selectively as needed by the assembly of the mesoscale elements of the assembly. Alan O'Riordan presented the work showing the assembly of 50 mm and 80 mm GaAs based light emitting diodes on silicon chip substrates.

Truly different and interesting.

Session 4 on System Packaging

Here the main frame presentations showed evolutionary improvements in mainframe technology. Complex packaging technologies were presented, pushing the thermal-mechanical structures and signal processing integrity to new limits.

The talk from Hitachi was on the packaging of their AP899 computer. Akio Idei described their computer based on the IBM 64-bit technology. This had 45 Watt chips on an MCM, with 700 watts on a module. To keep it low cost they used air cooling, improving the heat transfer with a microfin heat exchanger. The cooling fins were copper.

Hubert Harrer talked of the IBM e900 Enterprise server. This had the most complex MCM IBM has ever made, with 35 chips dissipating 1300 Watts.

Processor operating frequency was 918 MHz. Bandwidth was 1.2 terrabits per second.

Complementing this talk was the one from Erich Klink on their 32 way SMP structure one single board, This was an air cooled 4-chip MCM (8-way)glass ceramic construction.

Thin Multichip assemblies

The other papers of the session were on small mutichip system in a package technology.

Gong Zhu, in a paper with John Liu of Chalmers University described their System-in a Package Technology using LCP substrates. After the usual listing of the virtues of LCP technology he described a SIP with a GaAs MMIC chip embedded into the LCP substrate. High frequency performance was indeed capable of 20GHz to 40GHz. This means the technology can be used for RF microwave applications.

Subsequent testing showed that the LCP assembly was better mechanically and thermally than either FR-4 or Teflon. Furthermore LCP has the lowest environmental impact for all chosen categories. The copper adhesion was satisfactory.

Andreas Ostmun did the Fraunhofer Chip in Polymer talk. This was the thinned chips in polymer technology in built up printed circuit boards described in the IMAPS new book . First the 40 micron chips were die bonded onto the dielectric and then embedded in dielectric, the vias are etched later for the connections to the PCB. Surface interconnections was with electroless copper. Conventional surface mount devices, resistors and capacitors can be placed.

One benefit is the very short electrical paths.

Karlheinz Bock of Fraunhofer Munich described manufacturing process for the thin chips for co-planar and stacked 3-D assemblies. Commercialization should be in 5 years.

Cellular Technology

Thales Microelectronics presented their use of LTCC technology with the inclusion of baluns, filters, SAW filters PIN diodes and GaAs switches. Modules were described for WLAN applications.

Manufacture was on a fully automated manufacturing line in Taiwan at ACT Microelectronics. Millions of LCTT substrates have already been produced. Production capability is 11million square inches a month with widths and spaces down to 70 Microns and 100 micron vias.

After overview talks from Analog Devices on CSP technology and a talk by Johnny Widegren of Infineon on the future of wireless devices, Savolainen of Nokia talked of Display Driver Packaging.

"Display Driver Packaging, ACF Reaching the Limit" was Petri Savolainen's discussion of the forthcoming limitation of ACF connections for wireless packaging.

The finer pitches of wireless interconnect make the limitation of ACF technology a problem. One solution is to coat the conductive particles with insulation, permitting the particles to be closer together. The insulating coating breaks down when the particles are pressed between the bumps of the chips and the interconnect track. This and other technologies hold promise for higher density Anisotropic Conductive Film use.

The final presentation in this session was from Dag Strannabe of Orebro University, Sweden on using electromagnetic "Signatures" for test and troubleshooting. The new compact circuits such as those of Bluetooth applications cannot be probe tested or otherwise connected to test circuits. But they do emit electromagnetic fields when in operation and these fields can be analyzed to determine if the performance is satisfactory; voltages and currents can be estimated using the radiated fields.

The "signatures" of properly functioning devices can be stored and analyzed to produce good performance. An adaptive database is used to compare performance with previous records and provide for identification of good units and various faults. The system can not only spot a failing product, but can identify a probable location of the fault.

Seems like a most promising test technology.

Packaging Technologies for Electronic Applications

Some of the papers in this session were just overviews of MEMS technology and there were presentations on the use of getters and laser fast via drilling.

The presentation from IMEC, Belgium was on the RF MEMS packaging . Their technology placed a "cap" over each silicon MEMS chip at the wafer stage level. This protected the chips and made possible the necessary diamond sawing.

The individual devices can then be mounted in plastic SOIC or BGA package. Screening / shielding is provided and mechanical interfaces can be provided to the outside world through fluidics for example. Solder bonding and BCB are used for the sealing layer.

Examples of MEMS devices such as micro-bolometers, micro-relays and RF - MEMS switches were shown.

Weidng Wang of the University of Florida, Ocean Technology Center talked of their ocean salinity sensor. This was an assembly of RF-based inductive conductivity sensors, and thin film temperature and pressure sensors, with fluidic circuits to connect to the water.

Construction was PCB on LCP laminate. Patterning was maskless, using micro-optics and spacial light modulation. Features down to 10 microns can be handled. The technology permits rapid changes in design, lowering costs of R&D and manufacturing.

Dr. Manfred Frischholz of microFAB Bremen also talked of wafer scale technology with through vias and recessed cavities for MEMS CSP designs.

Vias were formed by DRIE or anisotropic wet etching or formed by chemical vapor formed in doped silicon or by electro plating of metal. Sputter deposition was used for the seed layer.

Metal pads on the top side were provided for the attachment of MEMS devices and ASICS, etc. Solder bumps were provided on the bottom side for flip-chip bonding to the PCB, or to the top of another chip for a 3-D assembly. When 3-D recesses lies were designed, recesses were DRIE by DRIE into the bottom chip through the wafer This provided space for MEMS components needed for pressure sensors or microphones to provide an acoustic back chamber.

They showed a silicon microphone on the CSP substrate of integration of a MEMS and an ASIC.

LETI, Grenoble, France also is working in wafer scale packaging of MEMS. Giles Poupon described their technologies. Various sealing technologies were developed, but they presented a new concept for cooling with deep grooves fabricated using deep plasma etching into three wafers.

Conclusions

These TC-14 workshops are the finest diversified workshops in packaging. They present a variety of technologies and applications together to promote new ideas for the attendees. They bring together Photonics, Main Frame, micropackaging, cellular technologies and MEMS at one place. Combined with the Sessions of the Research Triangle Park workshop were also on Electro-optics and Medical applications providing additional diversity.

This workshop was made possible by the organization of Christine Kallmayer of Fraunhofer, Erich Klink of IBM Germany and Cian O'Mathuna of NMRC Ireland. They are held at centers of electronic packaging so local participation can happen. Workshops at isolated locations are now difficult with present tight travel dollars.

The next European workshop will be January, 2005 in Berlin, the next Japan workshop is January, 2004, The next US workshop will be at Research Triangle Park in 2004.

submitted by John(Jack) Balde
Workshop Coordinator, TC-14 System Packaging
Condensed from an IDC Report

*** CALL FOR MANUSCRIPTS ***

The IEEE Potentials Magazine goes to all student members of the IEEE (USA and Canada), presently over 50,000. The level of the article is addressed to the undergraduate/graduate student and has several objectives:

O Interesting the student in a topic for further study
O Explaining technological advances in an area
O A forum for technical ideas
O Articles of interest technically and professionally

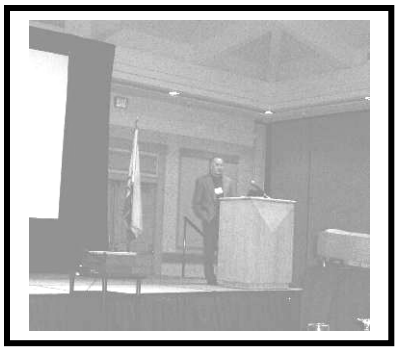
If interested, contact: Dr. George W. Zobrist
Ph: 573-364-6905, Fax: 573-341-4501,Email: zobrist@umr.edu

Successful EPEP in Monterey

The 11th. Topical Meeting on Electrical performance of Electronic Packaging (EPEP) was held from October 21-October 23, 2002 in Monterey, California. The meeting provides a forum for the presentation and discussion of the latest advances in the electrical design, analysis and characterization of on-chip and off-chip package interconnections and structures, covering all the application families and frequency ranges -- namely, digital, RF, microwave and mm-wave applications. EPEP is co-sponsored by the MTT and CPMT societies of the IEEE.

The afternoon of October 19, before the start of the conference, the second annual workshop, sponsored by the IEEE CPMT Society, "Future Directions in IC and Package Design", had record attendance of 50 participants from all over the world. A. Deutsch of IBM Corp. and M. Swaminathan of Georgia Institute of Technology chaired this meeting that had six excellent international invited speakers from the US, Europe, and Asia. The afternoon was divided into two sessions chaired by Tawfik Arabi of Intel Corp. and Prof. Andreas Cangellaris of University of Illinois, Urbana-Champaign. The first three speakers addressed high-end processor and package design issues. The second session covered tools and technology development needs and projections. The workshop was open to all EPEP conference attendees free of charge.

The EPEP meeting this year was organized into eleven sessions of oral presentations and one open forum (poster) session for one-to-one discussions. The papers represent 12 countries (Switzerland, Poland, Belgium, Finland, Korea, Taiwan, Japan, Canada, Italy, Germany, China, and USA).



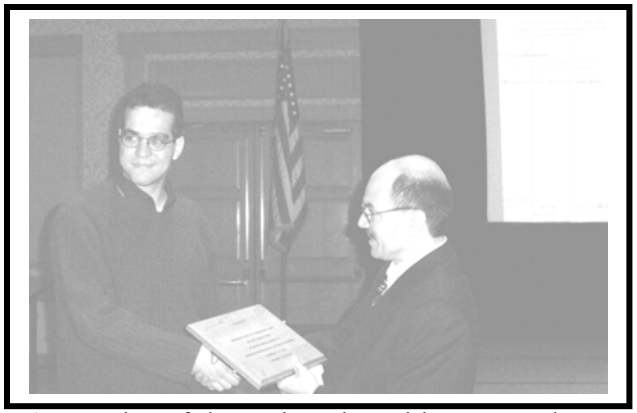
The meeting began with a keynote speech titled " Giga-Hz, Giga-bit, and Giga-Transistors" by Dr. Bill Siu, Vice President and General Manager, Desktop Platforms Group, Intel Corporation. Dr. Siu addressed the challenges posed to the packaging community by the rapid advancements in silicon technology. He postulated that the power removal and power delivery problems could no longer be solved with innovations in packaging alone. Instead, he encouraged the packaging community to look at the platform as a closed loop system and seek solutions at the architecture, circuit, package, and platform levels.

The keynote address was followed by a special session for design issues of synchronous interfaces that are used widely for interchip connections in digital systems. The remaining ten sessions were dedicated to System Design and technology, Power Distribution design and Noise, RF/Microwave, Electromagnetic Issues, Modeling, Transmission Lines, Measurements, On chip Issues (that mainly cover I/O circuit design, clock net design and analysis, and electrical parameter extraction), and Interconnection macromodeling.

On Sunday October 20, five short courses were offered prior to the start of the meeting. The tutorials were given by well-known experts in their fields and covered wide variety of relevant topics including High-Speed Digital Interconnect

Measurements, I/O circuit design, Power Supply system design and analysis, Electrical Interconnect and Package Modeling, and an introduction to RF design issues.

Once again special attention was paid to graduate student attendees of this meeting with the presentation of Intel and IBM Corporation awards to the two most outstanding papers authored by graduate students. Each award consisted of laptop and $2500 cash. A total of 16 papers competed for these awards. The best student award sponsored by IBM Corp. was given to Mr. Dharmendra Saraswat, a student at Carleton University, Canada for his paper titled " A Fast Algorithm and Practical Considerations For Passive Macromodeling of Measured/Simulated Data". Dr. Moises Cases representing IBM presented this award (See figure above). The best student paper award sponsored by INTEL Corp. was given to Mr. Erdem Matoglu, a student at Georgia Institute of Technology for his paper titled "Efficient Statistical Analysis and Diagnosis of High Speed Source Synchronous Interfaces". Dr. Tawfik Arabi representing INTEL Corp. presented this award (see below).



A reception of the students hosted by IBM and INTEL was held on Tuesday October 22 that provided the opportunity to the students to get to discuss package design issues of interest.

In addition, the meeting hosted eight exhibits. Companies represented included: Ansoft, Apache Design Solutions, Applied Simulation technology, GigaTest Labs, Georgia Institute of Technology, Optimal Corporation, Sigrity, and TDA Systems.

A special issue in CPMT transactions based on the paper version of the presentations at this 11th EPEP meeting will be edited by DR. Tawfik Arabi of Intel and Dr. Michel Nakhla of Carleton University (picture left).

Meeting Co-Chairs: George Katopis—IBM, Tawfik Arabi-Intel, Michel Nakhla- Carleton University (regional).

Subject: Arctic trip

By Luu Nguyen, CPMT Fellow, while on Fullbright Fellowship for Packaging in Helsinki

Well, I took a 2-day trip past the Arctic Circle this Christmas and made it back in one piece.

- Fly Helsinki to Kemi (located beneath the Arctic Circle, on the Gulf of Bothnia): The plane landed in blinding snow, howling wind, and -20C weather. Walking from the plane to the arrival gate was quite a challenge. It was only about 100 m away, but it was tough to walk without being blown sideways. My first thought was that with this weather, I will be spending the whole 2-day vacation watching TV in the hotel room. Luckily, the weather cleared up the next day for the boat cruise.

- Snowmobile: I was the only tourist on Saturday 12/21, so I got the guide's full attention. I had several layers of clothes on: thermal underwear, regular shirt, thick sweater, arctic bunny suit, crash helmet, goggles, heavy scarfs, and mittens. It was about -15C in the morning, but when I zoomed on the frozen river at 50 km/h, the wind chill must be in the -50C. Even though the driving handles of the snowmobile were heated, my fingers got numb within 30 min. Gripping the accelerator was painful on the return trip at night when the temperature dropped even further. Driving on the river bed and seeing the sun (on the way out) and moon (on the return trip) on the horizon was quite a sight. Near the Arctic Circle, the sun and the moon do not rise higher than the horizon. And with the long winter nights, we get only a few hours of daylight each day. 10 am looked the same as 10 pm: Dark. Without the snow to reflect light, it would look even bleaker.
- Ice breaker cruise: It was quite a treat to see the ship running full steam, crunching 1 m thick ice as if it were made of rice paper. The ship can in theory crunch over 8 m thick ice. This year, the ice is "thin" (only a few meters) due to "warmer" weather than normal. It was "only" -16C, but the boat was going fast and the wind chill did not help. When the ice crystals hit the face, it feels like being sandblasted. The boat stopped about 1 hr from shore to allow passengers to change to arctic survival gear and jump into the water. It was freaking cold. I was told that last year, some of these guys jump in without the survival gear. After the dip, they ran back to the boat to warm up in the sauna. One has to be born here to consider that sort of thing as fun.
- Train ride from Kemi to Rovaniemi: 1 hr train ride through the postcard-worthy snowy landscape.

Rovaniemi: Located just a few miles below the Arctic Circle. There were too many tourists (Europeans, Russians, and Japanese) this time of the year. They came by bus loads. Things were handled like a production shop. One batch of tourists leaves, the next set arrives and get ready for all the tours and safaris, and so on.

- Lapp ceremony: This is the official ceremony offered by the Lapps (inhabitants of Lapland) to those who crossed the Arctic Circle. They stuck a reindeer horn on your head, mumbled something (supposedly to ward off evil). Afterwards, they stuck fingers into the ashes of a burning fire and wiped the ashes on everybody's forehead. This is supposed to bring good luck. Reindeer milk was offered as a token of hospitality.
- More snowmobile ride: The gear from this second safari outfit was lousier than the first one. My goggles kept on fogging up while driving the snowmobile. I had to remove the mitten from my left hand to clean the condensation quite often while driving to keep up with the convoy. The hand went numb quite rapidly several times. Luckily, with the batch of old and young tourists, the snowmobile convoy traveled at a relatively slow pace, between 20 to 30 km/h. It was quite a sight to see the convoy of some 20 to 30 snowmobiles stretch out on the ice. Kids were pulled in big sleds.
- Aurora Borealis: I walked outside along the river bed, away from the city lights. The temperature was about -30C without the wind. Hands went numb in a matter of seconds without gloves. It was dark but I did not see any Northern Lights, unfortunately. The only ones that I saw were displayed in the Arktikum, the Arctic Museum. The interesting fact I learned from the museum was that in this climate, one needs to eat at least 4500 calories/day to survive, and that the Lapps eat raw freshly killed reindeer and whale meat. The museum had quite a number of displays, including histories of several of the earlier expeditions to the North Pole and how they packed.
- Reindeer racing: I got in a sled pulled by a reindeer around a track and obtained my reindeer driver license - "valid for 5 years." This will be a useful reminder the next time I am stuck in traffic on 101.
- Reindeer meat: This is what happened to reindeers that don't do well at performance reviews time. I had it three times so far in Finland. The Finnish reindeer dish consisted of boiled meat slapped on top of a mountain of wheat and potato ringed with wild berry sauce. Definitely not TV Food Gourmet material. My last dinner in Rovaniemi was a regular burger at McDonald. I have now eaten at McDonalds across most of Europe and Asia, and can certify that McDonald excels at consistency - providing the same "bad" food everywhere. No wonder that they are trying to spice up the menu.
- I skipped the visit to Santa Claus Park and the ice fishing, and also decided against the husky "driving license." I did not feel like arguing with a bunch of wolf-like dogs in -30C weather on whether they should turn left or right. I skipped also a trip to the Northern tip of Finland, which was recommended by people at school.

It was a good experience. Worth a visit to find out what it feels like being thermally cycled down below -40C. Worth a second visit if one truly likes winter sports and the feel of being a Popsicle.

(editor: if in your travels for CPMT technology you have an experience that most of us will never have, please send in a report.)

EDAPS - TC 12 Workshop

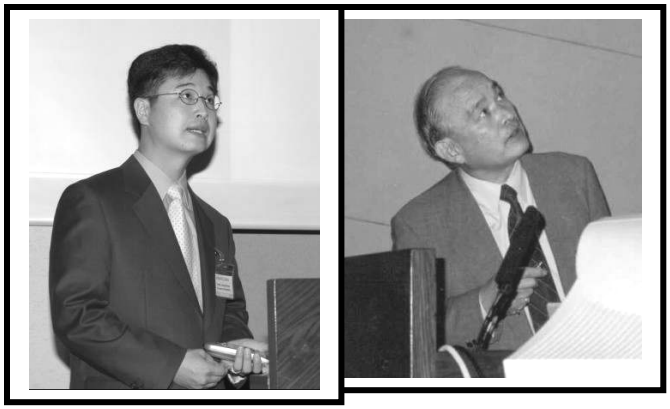
A one day workshop on Electrical Design of Advanced Packaging & Systems (EDAPS) was jointly organized by IEEE ED/CPMT/ Reliability chapter, Institute of Microelectronics (IME), Singapore and Ga Tech Packaging Research Center, USA on 9 December 2002 at IME auditorium. The workshop, first of its kind in Asia was co- chaired by Mahadevan K. Iyer (IME, Singapore) Tohio Sudo of (Toshiba Corporation , Japan) & Prof Joungho Kim of (KAIST, Korea).

Aimed to enhance the awareness of package and system electrical design concepts, issues and challenges ahead for next generation microsystems in this region ,the workshop had 80 registered particpants from Asian countries such as Malaysia, Philippines, Indonesia, Korea & Japan. There were nine invited technical talks by eminent researchers from US, Europe & Asia in the field of electrical design, modeling, test and measurements for advanced packages, modules & systems.

Prof Rao Tummala, President ,IEEE CPMT while inaugurating the event, addressed some of the key challenges ahead for system designers. Dr Lim Thiam Beng, Deputy Director of IME while welcoming the speakers & attendees mentioned the importance of this workshop in Asia.

Prof. Kanji Otsuka (Mesei University) in his key note talk presented an in-depth analysis of differential signalling and the importance of maintaining TEM wave mode in the GHz environment for electronic packaging. Prof Andreas C. Cangellaris (University of Illinois) gave an overview of the EM modeling and discussed trends and needs for substrate noise coupling, global power grid modeling and EMI modeling with case studies.

Dr. Gen Murakami (Hitachi Cable Ltd) in his talk discussed high transfer speed packaging technology, using a novel Micro Interposer Tape Technology. Jong-Gwan Yook (Yonsei University) discused the design issues in a power distribution network in particular for arbitrary shaped systems. A decoupling capacitor methodology was illustrated.



J.G. Yook ***Gen Murakami***

Prof F.G. Canavero (Polytechnic University of Turin) presented a macro-modeling method for system-level EMI-EMC assessment and the application of a RBF (Radial Basis Functions) model for conductive & radiative coupling. Dr. Y. Sugaya of Matsushita Electric Industrial Co. Ltd gave an introduction to a new 3-D System in Module SIMPACTTM and explained how the technology would enable to embed discrete devices into laminates.

David C. Keezer, Ga Tech

Y.Sugaya Matsushita Elect.

Prof David C. Keezer (Georgia Institute of Technology) shared the Test Strategies for High Density Packages and discussed novel test methodologies for wafer level testing. Dr Bruce Archambeault (IBM,) discussed the importance of decoupling power and ground analysis with two applications viz: functionality for transient response and EMC for steady state response. Prof Joungho Kim (KAIST) provided a detailed analysis for Gb/s enhanced eye-pattern of BGA type board-to-board connector and this work is driven by the challenges faced in implementing Gb/s signaling on PCB.

A panel discussion chaired by Prof. Madhavan. Swaminathan (Georgia Tech) laid the platform for a lively exchange of questions and answers on the design challenges for system integration in the future.

It was indeed an intense day packed with enormous amount of information. The event provided a congregation of research and industry professionals and provided a platform for exchange of information and ideas.

B. Archambeault (IBM) & Workshop Chair M. Iyer (IME) with TC 12 Chair M. Swaminathan (Ga Tech)

CPMT has New Senior Members

Every year about 1% of CPMT members achieve senior member status. Please, search the IEEE web site for the qualifications and process. If you have been an engineer for 10 years you probably can achieve Senior Member status.

Dahwey Chu -- Albuquerque New Mexico
Kukjin Chun -- Seoul, Korea
Stephen Clements – Republic of Ireland
Martin Goetz -- Dallas, Texas
Makarem A. Hussein -- Oregon
Charles A. Miller -- Oakland-East Bay , California
Andrew Oliver -- Albuquerque, New Mexico
Emmanouil M. Tentzeris -- Atlanta, Georgia
Surinder Tuli, --Phoenix, Arizona

EDAPS attendees at IME Auditorium, Singapore

Panel Discussion: Joungho Kim, Tohio Sudo, Kanji Otsuka, F.G. Canavero, Andreas C. Cangellaris, Mahadevan Iyer

Participants of EDAPS during Coffee Break

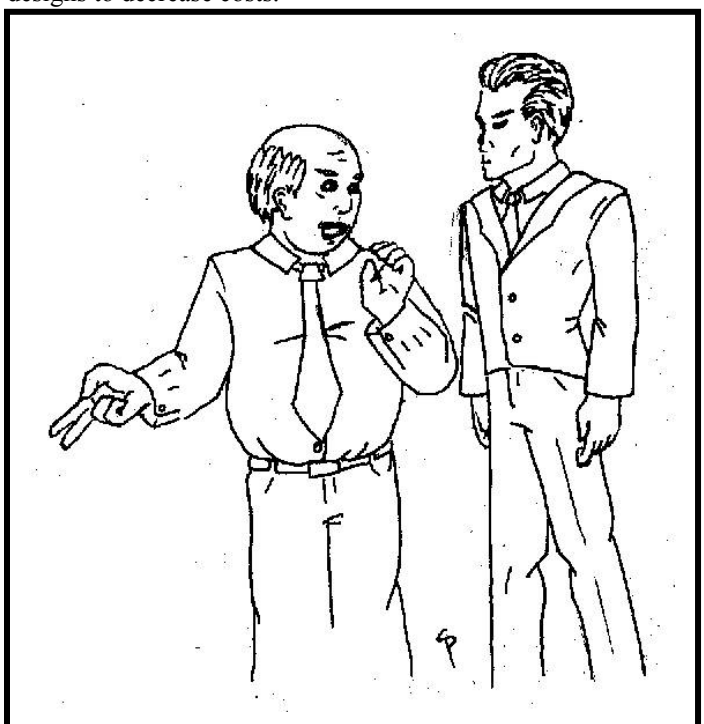
THANKS: This newsletter thanks go to Rao Tummala, Marsha Tickman, Bill Moody, Jim Morris, Dr. P. B. Parikh,Dan Bauks, Johan Liu, John Stafford, Jack Balde, Nguyen, Cristina Andersson, Baul Baltes, Alina Deutsch, Michel Nakhla, Angie Wong, and many others

Wanted SoC -- Dead or Alive?

At the conferences and publications of our CPMT Society there are often firm statements about the nature of the future of microsytems. In particular the argument is typically couched as SoC or SiP -- "System on a Chip" or "System in a Package." Most members operate within a one year horizon and probably have taken these arguments lightly. However, it is not just a debate on those of us who are rooted in assembly and packaging, but this year the debate has publicly broken out among the chip makers.

As reported in the EE Times by David Lammers, the IEEE ISSCC in February had a talk by Jay Heeb of Intel in which the system-on-chip movement was declared "dead." The culprit is the cost of masks and additional processing to get logic, memory, MEMs, opto, and analog functions on the same chip. The economic way to do this, according to Heeb is by making 3-D structures by assembly. He calls this future the So3D, system-in-3D package. He sees this future hybridization of different chips occurring by "molecular velcro" or "capacitive coupling."

In strong contrast, Avner Goren of Texas Instruments pointed out that the recent Bluetooth products under development by TI. Combining digital CMOS with memory blocks they are merging the baseband function with a digital radio and integrated power management for GSM phones. The power amp and bigger passives must still be applied around the chip. Of course the proof will be in the economics, but TI is hoping to reuse blocks of designs to decrease costs.



"What do you mean, you can't find a job with your new degree? Why in my office every engineer has at least two full time jobs for the last few years"
--a new engineer finds the problem, and it is us.

Jim V. Leonard, P.E.
2003 IEEE-USA President

Greetings to U.S. IEEE members. I look forward to serving as your president in 2003.

It looks like our U.S. IEEE membership of about 235,000 is probably only about 25 percent of the market. So my first request is that you join the IEEE Member-Get-A-Member program and sign up at least one new member.

With the terrible events of September 11, 2001, the outlook for the U.S. has drastically changed. We now have a frightful and fanatical enemy. Our government is setting up a homeland security force to help protect us, and IEEE-USA's Technical Policy Council will assist in the effort.

The 9/11 events affected us all. The following week, my aunt and uncle, Anne and Bert Souther, were brutally murdered in their La Habre, Calif., home. The murders are still an unsolved mystery. So, while it's very important for IEEE-USA to plan and support professional careers, it means little if terrorists and other criminals threaten our personal security.

In 2003, we will also look at heroes within IEEE. Our first retreat will be held at the Thomas Edison Museum, named in honor of the man who helped found IEEE. We will also celebrate Pearl Harbor Day there with a visit to meet George Elliott, Jr., an SCR-270B radar operator at the Opana Point (Hawaii) radar site, which first detected the Japanese attack on December 7, 1941. We helped establish the site as an IEEE Historical Milestone during National Engineers Week, 2000.

We hope to hold IEEE-USA Operating Committee meetings at the U.S. Military Academy in West Point, N.Y., and the U.S. Air Force Academy in Colorado Springs, Colo. IEEE has student branches at each one.

In late March, we will hold a Professional Development Conference and IEEE-USA Leadership Workshop at the Seattle Airport Hilton. Please consider sending a PACE representative from each section.

Our CARE program is a grassroots effort to urge U.S. IEEE members to visit their congressional representatives in their home district.

Unemployment among U.S. engineers has climbed steadily over the past several years. We presented our concerns over this and other workforce issues at the National Academies' Pan-Organizational Summit on U.S. Science and Engineering Workforce in November.

We will lobby Congress to restore the yearly 65,000 H-1B visa limit (now 195,000) to help U.S. engineers and computer scientists with increased employment opportunities. And we hope to re-establish IEEE-USA employment assistance at the Section level.

Log on to the IEEE-USA Web site (www.ieeeusa.org) and take a look at our ongoing activities and decide how you, our most valued asset, can help us help you.

Rogue's Gallery:
To left: Ephraim Suhir, Ralph Wyndrum, Ron Gedney and Dennis Olsen do strategic planning for CPMT Society.

On Right facing camera: Rao Bonda, Corey Koehler, Al Puttlitz, and Ephraim Suhir strategically eat for the future of our Society.

Walt Trybula, Ralph Russell, and James Steele compare notes