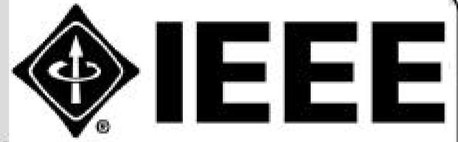
Components, Packaging, and Manufacturing Technology Society



Newsletter

The Global Society for Microelectronics Systems Packaging

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www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

PRESIDENT'S REPORT

Thanks and Goodbye !

I want to thank each and everyone one of you for allowing me to serve as your CPMT Society's President for the last four years. I'm the first president to have served two 2-year terms. I really enjoyed doing so.

In this last message as your president, I thought I would summarize what we have accomplished and what I see are some of the challenges we face as we look ahead. **My focus** has been mostly in four areas:

1. **Globalization:** Everything is going global. The internet changed everything. Almost everybody has access to almost everything from almost anywhere. Most large companies are roughly 50 % inside their country and 50% outside. It is only natural for us in the CPMT Society to reflect this, but there is one more important reason: IEEE organization is truly a global society unlike most of the other engineering societies. Our society board, as of January 1, 2004, will have its first Technical VP and first Conference VP from outside the U.S. in addition to four other board members who are from Europe and Asia. Our individual and chapter memberships also reflect this international trend and about 50% of our conferences now occur outside the U.S.

2. **Strategic Focus:** CPMT is "the" Packaging Society. Since packaging has not been taught traditionally at universities, packaging engineers acquired knowledge and skills on the job. In this day and age, with product cycles every six months, companies cannot afford these training delays, so packaging must become an academic subject. Our society, in contrast to the rest of IEEE, is mostly made up of industry members. The academic community had not participated very actively. Our society must, therefore, engage as many academicians and students as we can. I'm very proud of our accomplishments in this area. We started an international academic conference which brought the academic community together. We then funded courses for them to develop. The result was 12 different courses in such areas as RF, Thermal, Design, Test, MEMS and sensors. We began to develop student programs and chapters at various universities in Europe, Asia and the U.S. The result has been, along with Georgia Tech's role as a Global Research Center dedicated to packaging, the development of courses, curricula, tracks, certificates, degrees, and the first set of textbooks. These programs are spreading rapidly world wide to make packaging an academic subject within a decade.

3. **New Technology Focus:** Going back to mid-90s, CPMT's focus was on traditional packaging technologies such as wirebond, flip chip, QFP, BGA, PCB and SMT. But today's packaging is much more than that

and our society covers some of the most leading-edge technologies, including mixed-signal design, thermo-mechanical reliability, integral RF, optical, MEMS, sensors, green electronics, wafer level packaging, SOP, SIP, mixed-signal test, high-density board etc. We have begun to add nanopackaging by means of a workshop and an ECTC session.

4. **Branding Focus:** CPMT was not well known outside its membership. We have begun to change that through marketing efforts and offering a technical field award. The marketing effort was extensive and included preparing membership materials, revising web sites, and communicating through packaging magazines. The technical field award is meant to recognize the most prominent global contributions of the past decades. See elsewhere in newsletter.

<u>CPMT's Future</u>

The world is changing and most of these changes are because of technologies. CPMT must change too. It must change to more rapidly bring new and emerging technologies for use worldwide. It must change the way members need and use information - anytime, anywhere, and instantly. Some members need to be educated in tutorial fashion while others want it in "discovery" state.

It must educate CTOs as well as students and everyone in between. It must cut across technologies from devices, to packaging of these devices, to systems. It must provide information on various technology options and their trade-offs to the community. It must involve academicians both for leading-edge knowledge and for developing a new breed of engineers well-versed across several disciplines, from design to fabrication to test and reliability.

I expect to continue to play a role in these and other areas, working with you around the world.

Thanks and goodbye. -- Rao R. Tummala, President CPMT

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2006
William D. Brown
Philip C. H. Chan
Charles Lee
Johan Liu
Thomas G. Reynolds
Ephraim Suhir

2004
Rolf Aschenbrenner
N. Rao Bonda
Rajen Chanchani
Ricky Lee
Connie Swager
Naoaki Yamanaka

2005
William T. Chen
L. Merrill Palmer
E. Jan Vardaman
Li Li
Walter J. Trybula
David C. Whalley

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Joint Committee on Semiconductor Manufacturing -- G. C. Cheek

Next News Deadline: March 5, 2004
Members-only Web: UserName: xxxx
Password: xxxxxx (for 1st quarter)

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Inauguration of SMITC at Shanghai

Two CPMT Chapter Chairs meet in China

The San Diego, CPMT chapter chairman while in China visted the China CPMT chairwoman Doctor Ma Jusheng at Tsinghua University. Steve Adamson gave a short presention on design for underfill and was given a tour of the facility.

The picture show Doctor Ma and Steve Adamson with members of the local CPMT Chapter and Asymtek Staff

members from Shanghai. The meeting took place on Monday November 10th, 2003.

JOBS EXCHANGE

People with job openings or wanting positions in CPMT fields such as materials, components, packaging, and manufacturing technology are welcome to use the CPMT website's facilities.

Go to www.cpmt.org

Then select either "Position Wanted", "Positions Available", "Student Resume", or "Faculty Position" links in the low left of the screen.

REGION 10 CHAPTER ACTIVITY ROUND-UP

Shanghai (China) Chapter organised the IEEE CPMT Regional Workshop on Microsystem Integration Technology on 23rd - 24th October 2003 along with a week long short course program (20th to 27th October). The topics covered system design, device fabrication, material characterization, advanced packaging technology and reliability. The event was sponsored by IEEE CPMT China Chapter and Scandinavian Chapter and the forum attracted about 250 participants.

Together with this Regional Workshop, the Chapter also inaugurated Sino-Swedish Microsystem Integration Technology Centre (SMITC) on 27th October 2003 in Shanghai University, China. Initiated by Prof. Johan Liu, Chalmers University of Technology and Head of IVF Division of Electronics Production in Sweden, the Centre is dedicated to the development of the microsystem and microelectronics technology for industrial applications. It is primarily funded by Shanghai and Gothenburg governments, Shanghai University and Chalmers University in Sweden. A photograph of the inauguration session at SMITC is also enclosed herewith.

Dr. Cheung, **Hong Kong Chapter** has reported a topical workshop on "Cleanroom Technology for Microelectronics and Photonic Packaging" on Friday, October 31, 2003 by Dr. Ken Goldstein in HKUST. The chapter has also scheduled a workshop on "Encapsulation of Electronics: Materials, Process and Reliability" by Prof. C.P. Wong on December 18, 2003 in HKUST. The Student activities of the chapter during the quarter included setting up of a Student Chapter webpage, and a visit to Electronics Asia 2003 exhibition in Hong Kong in October 2003. Industrial visits of students to leading companies have also been planned by the chapter.

The new executive committee for CPMT Hong Kong chapter for the year 2004 is announced as under: -

Chairman - Dr. Cheung. Yiu. Ming.
Vice-chair and Chair elect - Dr. Li Ming.
Secretary - Dr. Or. Slu Wing.
Treasurer - Dr. Sham. Man Lung (he replaces Dr. Hulli Fu now relocated in Singapore).

The **India Council Chapter** organised a joint technical lecture with IEEE Electron Device society in October 2003. The chapter is now actively participating in the organisation of a 3-day (12th, 13th and 14th December) Annual Convention being organised at Pune by IEEE India Council to which our chapter is attached. The chapter is also closely involved in the organisation of a 3-day annual seminar on "VLSI Design" at Bombay IIT on 7th, 8th and 9th January 2004.This is a mega-event involving about 500 VLSI Design experts as delegates (includes about 150 participants from abroad)

.Submitted by Dr. Parikh

CPMT **Silicon Valley Chapter Activities** by Tom Tarter

PROFILE OF A CPMT CHAPTER

The Silicon Valley (Santa Clara Valley) chapter of the Components, Packaging & Manufacturing Technology (CPMT) Society, IEEE, has a rich history of involvement in the San Francisco Bay Area engineering community and continues to uphold this history with a tradition of education and information in the manufacturing and packaging sciences, as well as in professional skills. CPMT/SCV has been very active in planning, promoting and supporting a wide variety of technical and professional services and functions. The committee is dedicated to enriching the technical information provided to engineers and scientists in the local area. We do this in several ways. Ongoing activities include monthly dinner meetings, technical conference support, workshops, seminars and professional development classes, as well as joint events with other local chapters and organizations. I would like to share with you some of our activities and give some insight as to how we get things done.

Monthly Dinner Meetings

Dinner meetings are held once per month on the second Wednesday of each month.

Those interested technologists can either come early for a sit-down dinner prior to the talk or may choose to hear the lecture only (which is free of charge). Speakers are selected from personal references, papers or articles which match our member needs. The meetings are very successful and we usually have a large and interested crowd. The speakers typically provide a soft copy of their presentations which are posted on the CPMT/SCV web site for viewing or downloading. After the presentation, audience members can personally interact with the speaker and the other attendees in an informal setting. The following list shows the dinner meetings held in 2003.

January Wireless LAN Markets and Companies: Upcoming Opportunities -- Satya Chillara, Semiconductor Sector, W. R. Hambrecht

February Illumination with LEDs -- Paul Martin, Lumileds

March Hey Buddy, Can you Spare a Paradigm? Update on efforts by the JEDEC JC15.1 Thermal Characterization Subcommittee to develop standards for simulation and test needed for 21st century technology -- Bruce Guenin, Sun Microsystems

April Manufacturing InfoWeb -- Information Web Service for Global Manufacturing - Dr. Ken Ouchi, President/CEO, Avidtecs

May Modeling and Characterization of Electronic Packaging Materials and Reliability of Products -- Sung Yi, Portland State University

June Electronic Manufacturing Service Companies --Still a Growth Segment --

Keith Dunne, RBC Capital, and Michael Morris, Director and Senior Analyst, Electronics Manufacturing Services and Products, for Smith Barney Equity Research

September Wire Bonding to Advanced Copper, Low-k Integrated Circuits: the Metal/Dielectric Stacks, and Materials Considerations -- George Harman, Senior Scientist, NIST

October Flexible Automation - Going Where Human Eyes and Fingers Cannot Go - Charlie Duncheon, Adept Technology, Inc.

November PARC's On-Chip Microcoil Inductor -- Dr. Koenraad Van Schuylenbergh, Palo Alto Research Center and 3M's Embedded Capacitor Material for Decoupling -- Bill Balliette, Electronic Solutions Division, 3M

December Outlook for the Semiconductor Packaging Market for 2004: IC Packaging, SoP, and Testing Directions -- Jim Walker, Dataquest/Gartner Group

Workshops and Professional Development Courses

In addition to the monthly dinner meetings, CPMT/SCV sponsors and organizes professional development classes and workshops for Bay Area professionals. These events are offered for a fee and part of the income goes back into the CPMT/SCV chapter to support other low-cost or free events. The professional development courses are put on by a local independent training service. These courses include titles such as; "Project Management", "Process Metrics", "Speed Reading" and "Transition from Engineering to Management", among others. Workshops consist of half- or full-day lectures from distinguished leaders in fields related to manufacturing, materials, packaging and process. These courses sometimes tie into the monthly dinner meeting so the speaker can get more exposure and those who could not attend the class can get information on the subject. Overall, the classes and workshops are very well attended and very highly rated.

Conference Support

CPMT/SCV is involved quite heavily in several local conferences. These conferences include SEMI-THERM, a semiconductor thermal conference in its 20th year; the Electrical Performance of Electronic Packaging (EPEP) Workshop (in Monterey last year); the International Symposium on Semiconductor Manufacturing (ISSM) in its 12th year; and the IEEE/SEMI International Electronics Manufacturing Technology (IEMT) symposium, focusing on manufacturing, design, test, packaging and other related technologies. The IEMT conference is held in conjunction with Semicon West and this year marks the 29th event. The Santa Clara Valley chapter also sponsors and supports two new conferences: Phopack, a premier photonics packaging conference, and Phomat, which deals with materials and reliability issues related to photonic packaging and manufacturing. In addition to these conferences, we co-sponsor many events in the California area with other IEEE chapters and non-IEEE groups. We also provide core technical sessions and short courses for the IEEE's WESCON exhibition, held alternately in the Bay Area and in Southern California.

Membership Development

The membership chair is responsible for finding and recruiting new members to IEEE and specifically to CPMT. Each year we offer special rates, subsidizing new member dues for the first year for members that are joining CPMT and reside in the local area. We recruit at floor exhibits at the conferences and events we support and heavily utilize documentation and pamphlets from CPMT at our meetings and workshops. The membership chair is also responsible for keeping track of existing members for upgrades to senior or fellow status in the IEEE. Another important duty of the membership chair is to keep on top of non-returning members to find out why they did not sign up and how we can encourage them to return to our chapter.

Keeping in Contact with Members

One of the most important aspects of keeping a long-running chapter healthy is to maintain contact with our members. The

web and email are essential tools for keeping costs low and increasing the potential member base. Having a chapter webmaster is a great plus and increases the visibility of the chapter to members and non-members alike. Our webmaster also administers the email list and sends notices to this list to announce the monthly meetings and special events. Care is taken not to 'spam' the email list, so announcements are sent sparingly but often enough to notify the engineering community of these events. The list currently includes perhaps 200 CPMT members, plus another 300 IEEE members, plus about 1500 non-IEEE members with an interest in materials, packaging, and manufacturing. We see our Chapter charter as extending to the full technical community in the Bay Area, not just to our paid membership. Having a well designed, informative web site is also necessary. Our web master has done an excellent job of posting and maintaining a large amount of data on a very organized and readable page with links to IEEE, CPMT and other related sites. The URL is www.cpmt.org/scv and I encourage you to check out the fine work by our chapter webmaster.

Volunteers

The volunteer committee is the key to organizing and successfully implementing these activities. Without the hard work and dedication of the CPMT/SCV Executive Committee, none of these events would take place. Attracting and keeping committee volunteers is an endless job and we are very fortunate to have a talented and enthusiastic group of people who work together to make things happen. The committee is made up of elected and appointed (*) members.

The CPMT/SCV Executive Committee

Chair Thomas S. Tarter
Vice-Chair Bernie Siegal
Treasurer Annette Teng-Cheung
Secretary Allen M. Earman
Program Chair* Harvey Miller
Education Chair* John Jackson
Membership Chair* Dave Tovar
Web Master/Advisor* Paul Wesling
Advisor / Transactions* Luu Nguyen

Others active in developing the program and projects for the Chapter are Bob Dubin, Jim Mars, Ephraim Suhir, Bill Chen, Janis Karklins, Ron Blankenhorn, Thorsten Teutsch, Sri Seelin, Elliott Alber, Guna Selvaduray, Sue Smith, David Angst, Kazumi Allen, Ken Ariathurai, Rich Blish, Liz Logan, Tom Chung, Terry Dishongh, Joe Fjelsted, and Daryl Martin. We focus on providing meanful tasks for all the interested volunteers.

Executive committee meetings are held monthly. In these meetings we review the upcoming dinner meetings, conference support, student and academia interaction, membership, advertising and web management, among other business, and make decisions based on input from our esteemed colleagues and officers. Because these are volunteer activities it is especially noble for those who give their time and effort to the CPMT to educate and communicate new ideas and better ways of doing things to our members and friends. Without the volunteers, our chapter would not be so successful. The 2003 picnic planning meeting was a great success.

The SCV Chapter executive committee at their summer planning meeting, poolside at Paul Wesling's home. From left: John Jackson, Luu Nguyen, Bill Chen, Tom Tarter, Allen Earman, Paul Wesling, Annette Cheung, Bob Dubin, and Ephraim Suhir.

Conclusion

The various activities sponsored by the CPMT/SCV chapter help engineers to keep up with new and advanced technology and to improve their skill sets for the ever changing job market. The professional development classes and successful technical conferences help to support the chapter financially, which allows us to expand our role in starting new conferences for advanced topics and to offer reasonable costs for such events. Each of these events helps to recruit new members and committee volunteers, and to expand our mailing list for better coverage of the technical community. The informal nature of the evening meetings also fosters a sense of community and outreach where individuals can network to better their jobs or find new opportunities and share essential information that can be found nowhere else.

I hope your chapter can learn from these examples and has the same kind of dedication and determination as our chapter members do. Don't hesitate to contact us for more information.

RESULTS OF ELECTION for IEEE CPMT Society Board of Governors

On behalf of Nominating Committee Chairs CP Wong and John Segelken, I am pleased to report that the votes have been tallied for the election of six Members-at-Large to the CPMT Society Board of Governors. The following individuals (in alphabetical order) have been elected to serve for a three-year term -- 1 January 2004 to 31 December 2006:

William D. Brown
Philip C. H. Chan
Charles Lee
Johan Liu
Thomas G. Reynolds, III
Ephraim Suhir

We thank all candidates for their interest and willingness to serve.

--Submitted by Marsha Tickman, CPMT executive director

Boston Chapter Activities

Boston IEEE/CPMT Meeting Notes for 2003 and 2004 by Dan Bauks Chapter Chair (dzbauks@aol.com).

The Boston CPMT chapter usually has 6 to 8 meetings a year with meetings held the third Tuesday of the month at the Sun Computer East Campus complex in Burlington, MA. (See www.ieee-boston.org for monthly meeting details) Some recent meetings included:

2/25/03 **"Liquid Crystal Tunable Filters"** by John Noto - Scientific Solutions; No. Chelmsford, MA (Picture)

3/24/03 **"Semiconductor Polymer Design for Low-Cost Plastic Transistors"** by Dr. Beng Ong, Xerox Research Centre of Canada

4/22/03 **"High Density Packaging"** by Dominique Numakuba of DKN Research - Haverhill, MA

6/10/03 **"IEEE/CPMT One Day Symposium"** at Nepcon-East Bayside Exposition Center; South Boston, MA

9/30/03 **"Polymer Flip-Chip Assembly"** by James Clayton, President Polymer Assembly Technology; Billerica, MA

Dan Bauks (left) with speaker James Clayton

10/23/03 **"Lab on Chip Drug Screening Technology"** by Dr. Colin Brenan, President. BioTrove Inc. Woburn, MA

11/11/03 **"Automation Machinery for Flip-Chip Component Assembly"** by Peter Cronin of Newport Corporation; No. Billerica, MA

12/16/03 **"Direct Wafer Bonding"** by Ken Turner of MIT - Cambridge, MA.

The Boston CPMT local chapter will also again be presenting a free Educational Program at the IEEE ELECTRO 2004 Conference to be held May 5th during the Nepcon-East Show at the Boston Hynes Center. (See www.nepcon.com and click on Nepcon-East Show and Electro Program)

Topics to include Flip-Chip Assembly, Laser Machining, Wi-Fi Manufacturing and Patent Licensing in Electronic Manufacturing.

Peter Cronin of MRSI

TC-12 Meeting Summary

TC-12, renamed as the Electrical Design, Modeling and Simulation (EDMS) technical committee was adjudged the best technical committee within the CPMT society. The committee was recognized for its technical contributions through a Special Presidential Recognition award at ECTC '03, held in New Orleans in May '03. The award was given by the CPMT President Rao Tummala and received by the TC-12 chair Madhavan Swaminathan on behalf of the EDMS committee.

As in previous years, the committee meeting was held just before the Topical Meeting on Electrical Performance of Electronic Packaging (EPEP) Oct. 25, 2003 in Princeton, New Jersey. Though the meeting started late at 7:30pm and continued until 10:30pm, it was very well attended with around 30 attendees. These included both the committee and non-committee members.

EDMS is the technical sponsor of four CPMT conferences and workshops, which include EPEP, SPI (Signal Propagation on Interconnects), FDIP (Future Directions in ICs and Packages) and EDAPS (Electrical Design and Packaging of Systems). These conferences span three important regions in the world namely, America (EPEP, FDIP), Europe (SPI) and Asia (EDAPS). In addition, EDMS also sponsors the modeling and simulation sub-committee at ECTC.

Every year, the chairs provide an update on each of the conferences. Flavio Canavero (Univ. of Torino), provided an update on SPI, which was held in May '03 in Sienna, Italy. This workshop received special visibility from CPMT this year due to the attendance of Rao Tummala, CPMT President (who gave a keynote talk on System on a Package Technologies) and Paul Wesling, CPMT Vice President (who gave a luncheon talk on the society). The workshop was held in the picturesque Tuscany region of Italy and was very well organized, thanks to the efforts of Flavio Canavero, Ivan Maio, Grivet Talocia and Igor Stevieno who are with the University of Torino. After 3 years in Italy, the workshop will be moving back to Germany and will be held in Heidelberg in 2004. The workshop will be chaired by Hartmut Grabinski of the University of Hannover. Joungho Kim (KAIST) provided an update on EDAPS '02 and '03. In Dec '02, the first workshop was held in Singapore and was well attended with around 70 participants. This year, the workshop was held in Daejon, South Korea on KAIST campus on Nov. 10, 2003 soon after the Asia Pacific Microwave Conference. The work-

shop consisted of invited speakers from all over the world, including USA, Italy, Singapore and Japan. Having attended the workshop, the high point was the excellent hospitality provided by the host Joungho Kim of KAIST and his energetic students. The workshop was preceded by a tour of the Daejon area which included visits to the Buddhist temple and Korean folk village. The food provided was excellent and most of us added quite a few calories when we were there. Following the workshop, a tour of KAIST was organized as well. Tawfik Arabi (Intel) provided an update on EPEP, which is the premier conference on electrical design within the CPMT society. The paper quality was excellent this year and the conference was well attended by experts from both industry and academia. EPEP is unquestionably the pride of EDMS and the CPMT society. George Katopis (IBM) provided an update on the Electrical and Modeling subcommittee within ECTC. The sessions organized by this subcommittee is becoming very popular within ECTC due to the technical quality of the papers. George encouraged the participants to submit more papers. Since the meeting was held soon after FDIP '03, no update was required for this workshop.

The high point of the meeting was an invited talk given by Evan Davidson, who retired from IBM recently. Evan, who is an expert on Systems Packaging, was encouraged to give a non-technical talk by Alina and myself. Evan obliged and gave a very interesting talk on the "Career for Electrical Engineers". The statistics he provided led to interesting discussions. On one of his charts he compared the salaries of mid-level engineers in San Jose, Beijing and Bombay. San Jose engineers salary was ~106K per year compared to the salary in Bombay which was ~10X lower. The Beijing salary was slightly higher than Bombay. However, the skill level was the same everywhere, meaning that companies will look to moving jobs off shore unless there is an incentive to do so otherwise.

Though the attendees wanted to continue the discussion with Evan, we had to adjourn the meeting at 10:30pm since we had to prepare ourselves for EPEP next day, which started at 8:00am.

--Write-up provided by Madhavan who is currently in Chennai (India) on transit to Singapore.

TC-6 Sets Up Workshop for next

CPMT Technical Committee (TC-6) meeting on High Density Board Packaging Technology was held on September 25th, 2003 at the Tokyo branch of IBIDEN co., Ltd. One of the major accomplishments was the detailed planning of a Workshop to be held in conjunction with the 2004 ECTC in Las Vegas.

TC-6 Small **Workshop Program** in conjunction with 2004 ECTC.

Chairman Yoshitaka Fukuoka, Weisti

Co-chairman Kishio Yokouchi, Fujitsu Laboratories of America, Inc.

Presentations:

(1) "Recent Advances in Materials, Processes and High Density Structures at GT-PRC" by Venky Sundaram and Rao R Tummala, Georgia Institute of Technology.

(2) "Dielectric Materials for High Density Interconnect Technology" by Masahiro Ito and Shunsuke Yokotsuka, Asahi Glass Co., Ltd

(3) "IVH Multi-layer Printed Circuit Board with Polyimide Films" by Akihito Kurosaka and Osamu Nakao, Fujikura Ltd.

(4) "Advanced Technology for High Density Substrate and Boards" by Yasuhito Takahashi, Fujitsu Microelectronics America, Inc.

(5) "High-Density and High-Frequency Silicon Substrate Technology for SiP" by Atsushi Takano and Yoshitaka Fukuoka, Dai Nippon Printing Co., Ltd and Weisti

(6) "Passive and Active Components Embedding Technology for High Density Substrate" by Masaaski Katsumata, Matsushita Electronic Components Co., Ltd.

(7) "A Consideration for Total Mechanical Stress in Flip Chip Packaging Utilizing Buildup Substrate Technology" by Yutaka Tsukada, Kyocera SLC Technologies corp.

The Attendees of this TC-6 meeting were: Dr. Yoshitaka Fukuoka (Weisti), Mr. Ryo Enomoto (IBIDEN Co., Ltd.), Mr. Shuhei Tsuchida (Kyocera SLC Technologies Co.), Mr. Rokuro Kambe (NGK Spark Plug Co., Ltd.), Mr Atsushi Takano (Dai Nippon Printing Co., Ltd), Mr. Shunsuke Yokotsuka (Asahi Glass Co., Ltd.), Mr. Masaaki Katsumata (Matsusita Electronic Components Co., Ltd.), Mr. Kishio Yokouchi--by long distance (Fujitsu Laboratories of America, Inc).

New Web Content -- ONLY for CPMT Members!

Your membership in the IEEE and the CPMT Society just got more valuable! Beginning January 10th, all CPMT members can come to our Members-Only webspace to access full-text papers or presentations, in PDF format, from several recent conferences:

**IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '02

**IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '03

**EuroSimE'03: 4th Int'l Conference on Thermal Simulation in Micro-Electronics and Micro-Systems (France)

**Phoenix Chapter Fall'03 Workshop on Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

These are papers and presentations that cannot be found on IEEE's XPLORE. For someone who is not a CPMT member, they can only be purchased on CD-ROM. If you have a need to learn the latest in any of the fields above, check out the Tables of Contents and read some of the fine papers presented there.

Accessing our Members-Only area is very simple:

Point your Browser to: www.cpmt.org/mem/
When you are asked, enter:
Username: xxxx
Password: xxxxxx

(all lower-case. To know what to put in for the xxxx's you must look at page 2 of this or the latest CPMT printed newsletter, a newsletter that is mailed only to members)

Board Meets in Dallas

Thirty five of CPMTs most active volunteers met in Dallas on November 7 and 8th as your Board of Governors.

President Rao Tummala introduced the new slate of CPMT officers to the gathering: Phil Garrou is our new President, Rolf Aschenbrenner our new Vice President of Technology, and Ricky Lee our new Vice President of Conferences. (Figure from Left: Ricky Lee, Rolf Aschenbrenner, Naoaki Yamanaka)

Ralph Wyndrum

In addition, Rao thanked Ralph Wyndrum for his 11 years of serving on the Board of Governors. Ralph is now in charge of IEEE TAB (Technical Activities Board).

In response, Ralph commented that the CPMT Society looked mighty focused and full of momentum from the TAB vantage point. He mentioned that small IEEE societies are proving every bit as important as the larger ones due to their better focus and tighter link to their technology and industry. In contrast with 10 years ago, he is finding that most societies are managing their future well.

Ralph's goal is to drive operational management down to the local level. He believes that the right operational and strategic recommendations have been presented to IEEE and are gradually being adopted. This includes: (1) having a small board with finance and strategic skills, (decentralizing geographically if you want to globalize, (3) solving problems on the local division and industrial level, (4) driving any new policies down to the society or regional level that is appropriate, and (5) price services fairly so activities reflect true economics.

Ralph commented that in the future we need to use the emerging technologies to reinvigorate existing societies and not just use them as an excuse to start new societies. Members are not helped simply by fragmentation even if the some of the new fragments are exciting.

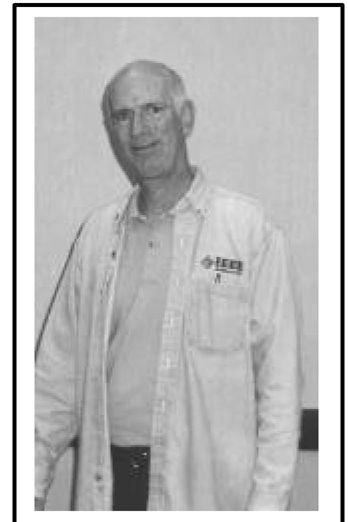
In his capacity at IEEE-USA Ralph has increased the ability to bring policy insight to congress by IEEE members enormously. For example, increasing from only 4 to 275 IEEE volunteers designated to report to congress or federal regulatory organizations (FAA, FCC).

Rao suggested that three topics be given strategic discussion before the normal board decisions be performed. In particular, he wanted discussions on Membership, Emerging Technology, and Gobalization/conferences.

Membership

Ralph Russell and Paul Wesling lead a discussion on membership to CPMT on Friday night. It was pointed out that membership is declining in IEEE and in most professional societies as well as in CPMT. This seems to be partly due to the tough economic times for technology companies. Fewer companies pay the dues for their engineers to join. Unemployed engineers don't join. A second trend is that the source of components, packaging, and electronics manufacturing is now global, and no longer concentrated in countries with a history of professional society participation. A third force is the Internet where any engineer can access much information without any membership barriers.

Although Ralph mentioned that if you are lobbying congress it is powerful to say you represent 300,000 engineers, raw numbers of members to CPMT are not as important as the number of attendees to our conferences and the number of papers submitted to our transactions. It is not clear to the average engineer what the benefits to CPMT membership are when they can attend our conferences and read our publications already.



A survey of board members was performed to sample motivations for being members. Mentioned were: professional development opportunities, easier networking with experts, chance for recognition and awards from peers, service to our profession to perpetuate the good received, and ready access to R&D results. However, several people at the top of our profession were mentioned who had never joined CPMT or IEEE and yet had all these benefits. Many mentioned that you need about 1000 fairly active volunteers to put on the scope of meetings and publications that CPMT owns but the 10,000 others that are attendees, presenters, authors, or readers do not necessarily have to be members to reap rewards.

Suggestions:

1. publish "directory of members" for members only - to help networking
2. have open meetings but make pitch about CPMT and how to join
3. Find out why BSEEs tend not to join
4. continue to have CPMT stress industrial members even though academic volunteer more in our society
5. establish web learning courses free for members

6. establish "members-only" web areas with meeting reviews, keynote presentations, issue specific chat rooms, basic tutorials

Emerging Technology

Phil Garrou lead the discussion on the CPMT strategy for emerging technology. Paul Wesling indicated Society Publications area occasionally stumbles with a fast growing new technology. We can not always find a guest editor who "knows where the emergent bones are buried." Some areas such as Green Electronics and System on a Package arise suddenly everywhere and get much coverage in many societies. (figure from left: Phil Garrou, John Segelken, Ron Gedney, Merrill Palmer)

Ron Gedney mentioned that we do well on pertinent technologies over the long run with our transactions and our established meetings, but we are not nimble with timely workshops on hot new areas. Most organizers think the IEEE system can not do a workshop with 3 months notice (it can), so they seek some other help. It was suggested that we have a one page form for new technology workshops that quickly gets reviewed and turned over to an established workshop administration group.

There was much discussion of having one day meetings at airport hotels to encourage last minute attendance decisions. Another suggestion is to hold the workshop as part of a normal chapter meeting to guarantee local participation. Merrill Palmer suggested locating workshops near the center of the emerging activity.

Examples of emerging technologies include printed electronics, packaging the new ICs with copper and low-K dielectrics, bio-medical sensors/packaging, reliability of lead free (whisker full) component contacts, RFID, integrated passives, high bandwidth packaging, and nanosystem assembly and packaging. Rao Tummala pointed out that 25 papers have already been submitted to the new CPMT nanotechnology conference.

Currently many of the new technologies are introduced by sessions and short courses at ECTC. There was discussion about whether ECTC should be longer to accommodate more emerging technologies or if this should be left to IEMT or ad hoc workshops.

Action: Everyone send in emerging topics with list of key active engineers in these areas. Particularly list those gaps in focus by our Society.

Globalization/conferences

Rolf Aschenbrenner led a discussion on how to empower volunteers all over the world to hold meetings and be active in CPMT. Rolf pointed out that there are good examples of professional organizations that have a presence on all continents and offer the advantage of globally shared publications and meetings and yet are decentralized. That is, each geographic area has its own rules/constitution, events, finances, and some publications.

In contrast, for most non-USA IEEE members it looks like their full dues check is sent away never to return. This is the perception even though the flow of services may indicate the IEEE "subsidizes" many country members.

One solution step would be for CPMT to promote the "affiliate member" which would allow someone active in an engineering society of their own country to simply join CPMT/IEEE at a lower cost affiliate position. This may be the best approach in countries such as Japan where there are historically strong local professional societies.

A similar perception occurs when a local chapter in a country puts on an International meeting using "CPMT" as a sponsor. What real benefits come to the chapter from the CPMT to justify the request to plan the meeting finances with a surplus to be used as Society seed money? Of course, there are meeting advertisements put in the newsletter, transactions, and on the websites. In addition, the Society networking allows finding speakers and attendees, and Society subsidized Distinguished Lecturers are available for presentations.

Much discussion was held on specific meetings in Europe and Asia with more progress on adapting the specifics of each meeting history with the realities of remaining fiscally sound as a Society.

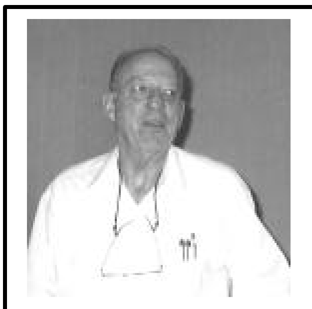
Globalization of meetings was clearly the most contentious of the subjects this year in CPMT. Most of the urgency is due to IEEE having to change its financial structure over the last few years. Many activities that were "free" must now be carefully analyzed on a cost-benefit basis. In particular, the push away from traditional paper transaction and proceedings to digital media is putting half of the future income of the society in question; a question that no one yet knows the answer. The other half of the CPMT income is from meetings and is mostly from the largest, ECTC. Whether the future is a handful of large meeting or a hundred small meetings spread around the globe, our society must figure out how to break even financially.

Society Business

The CPMT Society just created an IEEE Field Award in our area of expertise. Ralph Wyndrum strongly suggested that since this is the first year for the award that the Board should take special steps to make sure several highly qualified engineers are nominated. Several other Field Awards are being offered less often because of lack of good nominations. There are obviously plenty of long term contributors, but writing a nomination package is often not automatic so many qualified individuals are not submitted.

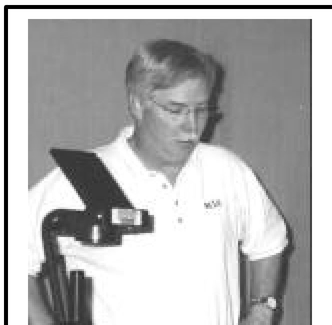
Steve Bezuk discussed the upcoming ECTC. There were 554 abstracts submitted this year compared to 426 in 2002 and 474 in 2003. There will be 39 presentation sessions, 2 poster sessions, and 14 professional development courses. The history with ECTC in Las Vegas indicates there will be a large attendance. Again the expectation is that only half the attendees will be from the US. Two special topics have been added: MEMS and Nanotech. A panel session of packaging ICs with Low K dielectric is planned. The Tech corner is expecting 70 displays. Intel is considering support for a best student paper award in

Model/Simulation or Advanced Packaging. The Motorola graduate fellowship will again be awarded based on ECTC presentations.



Bill Brown discussed the status of CPMT student chapters. The natural growth at schools with a critical mass has already occurred resulting in 5 chapters: Georgia Tech, Romania, Hong Kong, Sweden-Chalmers, U of Arkansas. The ability to have several close universities form one chapter is not easy based on IEEE rules. Several new chapter possibilities were discussed including San Jose. Bill showed the newly constructed student chapter web pages that are accessible from the www.cpmt.org home page.

John Segelken, treasurer, displayed many charts and tables that showed the Society's annual budget projections were accurate with expenses of $1,921K with income of $1,699K resulting in a $222K deficit. Once again the biggest bite from our operating budget is the amount IEEE charges to balance their headquarters budget, of about $450K. There is general belief that the right budget discipline and the right payment for services are quickly being activated so there will be at most one more year of heavy taxation.



Tim Adams discussed the finalized web plans. The space the search engine functions over will be expanded. A business model is being constructed to justify Web page sponsorship. The volunteer resources are being updated. We are benchmarking our site to other equivalent sites.

New Officers:
(left) Rolf Aschenbrenner, Tech VP
(upper left) Ricky Lee, Conference VP
(above) Phil Garrou, President of the CPMT Society

The CPMT Society Names New President with Officers for 2004

Dr. Phil Garrou takes over the reins for outgoing Society President Dr. Rao R. Tummala, whose term ends 31 December. Rolf Aschenbrenner takes over technical vice president duties and Dr. S.W. Ricky Lee becomes the conferences vice president

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) is pleased to announce its new officer lineup beginning 1 January 2004:

President: Dr. Philip Garrou has over 25 years of experience in the microelectronics industry. He is currently the Director of Technology and Director of New Business Development in Dow Chemical's Advanced Electronic Materials (AEM) business unit. He was previously the technical vice president of the CPMT Society, and also serves as an associate editor of the IEEE Transactions on Components and Packaging. Garrou is a Fellow of both IEEE and IMAPS. He has authored two texts on microelectronics, co-authored over 75 peer-reviewed chapters and publications on microelectronic materials. In 2002 he won the Fraunhofer IZM award for outstanding achievements by international specialists in the field of Advanced Packaging. He earned his BS in Chemistry from North Carolina State University and his PhD in Chemistry from Indiana University.

Vice President of Technical Activities: Rolf Aschenbrenner is the deputy director of the Fraunhofer IZM in Berlin, Germany, and head of the Chip Interconnection Technologies department. He has authored over 80 peer-reviewed articles in the area of electronic packaging, holds five patents and has eight patents pending in the microelectronics arena. Aschenbrenner is an elected member of the CPMT Society Board of Governors and plays an active role in the globalization of the Society in terms of membership and chapter development. He previously served as the strategic program director of European activities. He received his MS in mechanical engineering from the University for Applied Sciences in Germany and a BS in physics from the University of Giessen.

Vice President of Conferences: Dr. S.W. Ricky Lee is an associate professor of mechanical engineering at the Hong Kong University of Science and Technology and the director of its Electronic Packaging Lab (EPACK Lab). Lee has been published extensively in international journals, is the co-author of three books and is often invited to teach technical workshops and courses worldwide. He is the former chair of the Hong Kong Chapter of the CPMT Society, a member of its Board of Governors, and serves as associate editor for both IEEE Transactions on Components & Packaging Technologies and IEEE Transactions on Advanced Packaging. He is a Senior Member of IEEE and a Fellow of ASME. Lee received his BS in mechanical engineering from National Taiwan University and PhD in aeronautical engineering from Purdue University.

Officer terms are for two years.

Continuing for another two-year term in their current positions are:

Paul Wesling - Vice President of Publications
Al Puttlitz - Vice President of Education
Tony Chan - Vice President of Administration

REGION 8 CHAPTER ACTIVITY ROUND - UP

As is also reported in the region 10 chapter news**, the Scandinavian chapter** of CPMT jointly sponsored the First IEEE CPMT Regional Workshop on Microsystem Integration Technology at Shanghai University on October 27, 2003. It included 12 invited lectures and the topics covered system design, device fabrication, material characterization, advanced packaging technology and reliability. A number of short courses were also offered. About 250 participants from six countries attended the workshop. The inauguration of the Sino-Swedish Microsystem Integration Technology (SMIT) Center was held together with this workshop.

The **CPMT Student Branch Chapter of the "Politechnica**" University of Bucharest, participated, together with almost 100 Romanian companies, in the sixth National Electronic and Software Exhibition, BINARY'2003, which took place in Bucharest from the 24th to 26th of September at the ROMEXPO Conference Center. This exhibition is the most important annual event intended for the industry's professionals. The Student Branch Chapter members presented posters and electronic products realized by students in collaboration with the Center for Technological Electronics and Interconnection Techniques. The Student Branch Chapter was made an award at the exhibition by Concept Electronics, in recognition of its activities and achievements.

The prize, a laser jet printer, presented by Concept Electronics SRL, INTEL representative, to the IEEE-CPMT Politehnica University of Bucharest Student Branch Chapter

The **joint MTT/ED/AP/CPMT Saratov-Penza Chapter** in the Russian Section recently held chapter officer elections and Dr. Nikita M. Ryskin is the chapter chair and Professor Michael Davidovich is the chapter vice-chair. The chapter currently has 29 members in the cities of Saratov and Penza. They have held several technical and scientific meetings including conferences, workshops, seminars and lectures during the last six months. These have included:

1. "Nonlinear Days in Saratov for Young Scientists" (NDSYS'2003), September 30 - October 4, 2003, Saratov Suburb "Volzhskie Dali" which was chaired by Prof. Dmitry I. Trubetskov.
2. The 7-th International School on Chaotic Oscillation and Pattern Formation (CHAOS 03), October 7-10, 2003, SSU, which was also chaired by Prof. Dmitry I. Trubetskov and attracted more than 100 participants.
3. The Saratov Fall Meeting (SFM'03), October 7-10, 2003. This meeting included 5 Workshops and had more then 120 participants and was organized solely by the Chapter (http://optics.sgu.ru/SFM/2003/)
4. The 8-th Chapter Workshop "CAD and Numerical Methods in Applied Electrodynamics and Electronics", November 25, 2003, SSU. This one day workshop was chaired by Prof. Michael V. Davidovich and was participated in by 12 Chapter members.

During this period the chapter also organized several lectures and seminars on Microwave and Antennas topics, including "Microwave waveguide and coaxial probe structures", "Nonstationary Theory of Pulse excitation and Propagation in the Resonators and Waveguides" by Prof. MV. Davidovich, and "FDTD - Backed network Optimization of Microwave Systems" by Prof. V. Yakovlev, The Industrial Microwave modeling Group, Worchester Polytechnic Institute, USA.

The Chapter also plans the following activities in the coming year:

1. The 9-th Chapter Workshop "CAD and Numerical Methods in Applied Electrodynamics and Electronics", November, 2004, SSU, to be chaired by Prof. Michael V. Davidovich.
2. The International Conference Actual Problems of Electron Devices Engineering (APEDE'2004)" will be held in Saratov State Technical University, Saratov in September, 2004. Chairman - Dr. Alexander A. Zakharov.
3. Saratov Fall Meeting (SFM'04), including a Workshop on "Electrodynamics of Microwaves, Submillimeter and Optic Waves", during the first week of October, 2004 (http://optics.sgu.ru/SFM/2003).
4. "Nonlinear Days in Saratov for Young Scientists" (NDSYS'2004), October, 2004, Chairman - Prof. Dmitry I. Trubetskov.

--Submitted by David Whalley

Upcoming 2004 Conferences in

**Int'l IEEE Confer on Asian Green Electronics (AGEC), January 5-9, 2004; Hong Kong/Shenzhen, China; Angie Wong, wywong@ee.cityu.edu.hk
**2004 IEEE/CPMT 20th Semiconductor thermal Measurement & Management Symposium (SEMI-THERM), March 9-11, 2004, San Jose, cscomm@earthlink.net
**1st International Workshop in Nano Bio-Packaging, May 22-23, 2004; Atlanta GA, wlp@ee.gatech.edu
**5th International Symposium on Quality Electronic Design (ISQED), March 22-24, 2004; San Jose CA, Ali Keshavarzi ali.keshavarzi@intel.com
9th International Symposium & Exhibition on Advanced Packaging Materials, March 24-26, 2004; Atlanta GA, petri.jo.savolainen@nokia.com +358-7180-39382, (fax +358-7180-37143)
**2004 IEEE/SEMI Advanced Semiconductor Manufacturing Conference & Workshop (ASMC), May 4-6, 2004, Boston, mkindling@semi.org
**54th Electronic Components and Technology Conference (ECTC), June 1-4, 2004, Las Vegas NV, www.ectc.net
**Photomask Europa 2004, June 21-24, 2004, Dresden Germany
**2004 IEEE Holm Conference on Electrical Contacts, September 20-23, 2004, Seattle WA, Jennifer Lambert, j.lambert@ieee.org

- submitted by **Jim Morris/Ricky Lee, Vice Presidents** of Conferences

Editor's Turn

("Tell me, Gramps, about when you read ink on paper and flew everywhere to meetings")

What would your CPMT Society cost to operate if volunteers were paid engineering wages? One intent of this gedanken experiment is to determine how to apply improved communication technology to our current activities in the most "cost effective" way … how to give members the most benefits for their volunteer time. Assumptions: $30 per hour with no facility or benefits overhead. $1000 for each airline trip involving hotels. Justification of assumptions: On rare occasions even the most modest engineer will brag about earning more than $100/hour, but since there need be no loading or taxes on this virtual salary and we live in a world with many engineers willing to compete for jobs, the $30 is reasonable. Notice, for most volunteers today their companies, universities, or family supply their facilities and benefits. We all brag about the $200 trip but adding airline tickets, hotel bills, meals, car rentals, and salary enroute the $1000 estimate is probably closer to the volunteer average.

Now that we have the rules, let's look at three periodic activities driven by our members, comparing today's virtual costs with possible future technology induced savings. Remember, we do not have to follow the dollars like rats following the Piper of Hamelin, but if CPMT does not notice at all, probably some other engineering associations will eventually work out the future for us.

1. Putting out an issue of the Newsletter

Volunteer Labor: 25 reporters submitting articles using 2 hours each, one editor cutting and pasting for 30 hours = $2400

Travel: no one travels just for newsletter tasks but combines with conferences and meetings = $0

Photo Supplies and amortized software license for layout = $200

Posting on Internet = $0 (currently free server use at IEEE)

Printing and mailing to 3500 members = $3500 (particularly high cost of mailing out of USA)

Lesson: Volunteers provide at most about 40% of the market costs of the Newsletter. The biggest efficiency gain will occur as technical and cultural improvements allow the Internet version of the Newsletter to predominate without need of paper publishing and distribution. It may be necessary to password protect part of the Newsletter for members only to keep an advantage to being a volunteer in CPMT. A small savings will also grow as more reporters run around with digital cameras saving on film and chemical development.

2. Holding a Board of Governors Meeting

Two or three times a year 35 of your most active volunteers meet in one large room and spend the whole day reviewing Society operational proposals and details so that the many hundreds of other volunteers can do their tasks in a directed unhindered way. To impact volunteers careers minimally these meetings are typically on Saturday or Sunday.

Labor: 35 members for 10 grueling meeting hours + 4 hours preparation = $14,700

Travel: $35,000

Meeting room expenses: $1000

Lesson: Labor is about 30% of this activity and recent advances pushed by VP Anthony Chan have resulted in reduced preparation time by centralizing all participants documents on a website two weeks before the meeting. Thus travel is clearly the big pole in the tent. For the past 10 years one or two members call in to the meeting and doggedly listen to the speaker phone and truly participate. However, this calls for a type of concentration not normal in volunteers. Hotels are the normal site for Board meetings. Unfortunately, to date they do not support the high bandwidth Internet needed for interactive video Board meetings. However, in ten years one can imagine the 35 members sitting in their home (in their pajamas) looking at a 50 cm flat display with 34 tiled windows with live video of each of the participants (only video head shots so the childish superhero pictures on their pajamas will not be seen by others). There should be little cultural resistance to this virtual meeting because most of these active volunteers meet with others regularly face-to-face and will thus be sensitive to the full meaning of each other's statements. In addition, the meeting chair could more easily enforce one person speaking at a time and streaming text computer translation could occur on the screen (for example, when those volunteers from Boston speak and the rest of us wonder what they mean by the word "poahrts"). Many Board members may still come to a meeting room when it is coordinated with a big event such as ECTC, but many others will be able to participate by video. It is possible that many more than 35 will simply watch part of the meetings as passive observers (although this is hard to imagine since the meetings, however important, are only as exciting as CSPAN cable network).

3. Holding the ECTC, our Society premiere conference

Labor: 350 authors x 100 hours of preparation and presentation = $1, 050, 000

100 session and conference chairs x 24 hours = $72,000

Travel: 450 volunteer contributors = $450,000

Meeting room expenses (hidden as higher room costs) = $100,000

Paid labor, marketing, and supplies: $200,000

Lesson: Let's hear it for the volunteers! As engineers, if we work 100 hours perfecting our data and presentation we want to go to Las Vegas or Disney World for a few days. No virtual ECTC for the speakers. We really don't want to stay home (even in our pajamas) and watch a screen with 1000 windows of other participants. On the other hand, if my schedule or my boss's schedule does not let me go to ECTC, how great it would be to have a website where I can down-load a video of any of the presentations (particularly the keynote, plenary, and luncheon).

Would an archival video version of ECTC decrease attendance? Maybe in a very bad economy, but the benefit of chance meetings of new contributors, spontaneous conversations with old friends and contacts, and the excitement of the location will always attract about 10% of our members and many non-members to the conference. However, our Society does sponsor many meetings or workshops that have only 50 participants drawn from across the world. These smaller, but still international, gatherings may develop a culture of virtual real time participation during the next 10 years, but not the large conferences.

Volunteers provide much value to all Society members and to the engineering community. New communication technology and culture will make volunteer communication ever more "cost" effective for publications and small meetings during this decade. None-the-less we will be shaking hands and poking jest with each other at ECTC for decades to come .

■ Dave Palmer

Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications Workshop

Tempe, Arizona, Thursday, November 20th, 2003

Submitted by Vasudeva P. Atluri, Ph.D., Workshop Chair

IEEE Phoenix Section Components, Packaging, and Manufacturing Technology Society Chapter, & Waves and Devices Chapter jointly held An All Day Workshop on Thursday, November 20th, 2003, at the Memorial Building located on the campus of Arizona State University, Tempe, Arizona. The workshop was very well attended with 227 registrants. The breakdown of registrants included 22 organizing committee members, 13 speakers, 32 vendor representatives, 67 IEEE members (included 3 student members), and 93 non-members (included 12 student non-members). The workshop agenda included:

8:00 AM - 10:10 AM: Morning Section I:

Technology Roadmap and Devices Focus

Chair: Dr. Stephen Goodnick, Arizona State University, Tempe

Topic 1: "Keynote Presentation: CMOS Logic Transistor Roadmap - Drivers, Challenges, and Potential Solutions", Presented by Dr. Peter Zeitzoff, International SEMATECH, Austin, Texas.

Topic 2: "Silicon Nano-Transistors and Nanotechnology for High-Performance Logic Applications", Presented by Dr. Robert S. Chau and Dr. Suman Datta, Intel Corporation, Hillsboro, Oregon.

Topic 3: "Trends in Magnetic Information Data Storage and Magnetic Random Access Memory", Presented by Dr. Yang-Ki Hong, University of Idaho, Moscow, Idaho.

10:30 AM - 11:50 AM: Morning Session II**:**

Devices and Interconnects Focus

Chair: Dr. Chuck Weitzel, Motorola, Inc., Tempe, Arizona.

Topic 4: "RF and Mixed Signal Technologies", Presented by Mr. Jim Teplik, Motorola, Inc., Tempe, Arizona.

Topic 5: "Optimal Global Interconnects for Gigascale Integration", Presented by Dr. Azad Naeemi, Georgia Institute of Technology, Atlanta, Georgia.

12:50 PM - 3:10 PM: Afternoon Session I:

Packaging and Characterization Focus

Chair: Dr. Rao Bonda, Motorola, Inc., Tempe, Arizona.

Topic 6A: "High Speed Package Design - Package Characterization and Performance", Presented by Mr. Nozad Karim, Amkor Technology Inc., Chandler, Arizona.

Topic 6B: "Embedded Passives, RF Functional Blocks, and Shields", Presented by Mr. Michael P. Gaynor, Amkor Technology Inc., Atlanta, Georgia.

Topic 7: "Broadband Mixed Signal System Level Packaging", by Mr. Hassan Hashemi, Mindspeed Technologies Inc., Arizona.

Topic 8: "Characterization and Failure Analysis of Silicon Devices: Current and Future", Presented by Dr. Dieter Schroder, Arizona State University, Tempe, Arizona.

Topic 9: "Failure Analysis of Microelectronic Packages: Current and Future", Presented by Dr. Deepak Goyal, Intel Corporation, Chandler, Arizona.

3:30 PM - 4:30 PM: Afternoon Session II: **Technology Trends**

Chair: Dr. Mali Mahalingam, Motorola, Inc., Tempe, Arizona.

Topic 10: "The Road to Ubiquitous Computing, Entertainment, & Communications - Portable Wireless and Broadband Applications and Markets", Presented by Mr. Christopher Taylor, Strategy Analytics, Boston, Massachusetts.

Topic 11: "Vision for Convergence: Next Generation Computing and Communications Solutions", Presented by Mr. Ronald Curry, Intel Corporation, Santa Clara, California.

5:00 PM - 6:00 PM: Panel Discussion Titled **"Future of Computing and Communication Technologies and Applications"**, Moderated by Dr. Stephen Goodnick, Arizona State University, Tempe, Arizona.

The morning session with a focus on technology roadmap, devices, and interconnects was very well received by the workshop audience. Dr. Peter M. Zeitzoff gave an insight into to be recently released version of the International Technology Roadmap for Semiconductors (ITRS) which maps the scaling of the IC technology generations over the next fifteen years. His presentation focused on model-based approach to transistor scaling which is rapidly scaling into the deep submicron regime, with current gate lengths approaching 45 nm (0.045 mm). Dr. Suman Datta talked about silicon-based nano-transistors and nanotechnology enabling of Moore's Law continuation up to 2015 and the approaches that need to be adopted for continuing the law beyond 2015. He emphasized that the future approaches must utilize the modern-day silicon technology's strong foundation and that successful technology options will only emerge from a strong collaboration between the semiconductor industry, the academia and the government agencies. Dr. Yang-Ki Hong gave a brief description of the principles of magnetic recording and MRAM; and the fabrication of media and MRAM. Later part of his talk focused on the history of recording technology, future magnetic recording, characteristics and development trends of the most important magnetic nanoparticles and nanofilms, and also magnetic element shapes for magnetic tunneling junction (MTJ) of MRAM device. Mr. Jim Teplik described the key features required in an RF/mixed-signal technology for wireless applications by examining both the active and passive components as well as reviewing the state of the art, key performance metrics, trends, challenges, and opportunities. The presentation also addressed the importance of effective signal isolation and gave a brief review of opportunities beyond 2GHz. Dr. Azad Naeemi emphasized that the design of GSI chips should shift from transistor-centric to interconnect-centric to facilitate efficient use of valuable on-chip metal levels based the fact that the transistor performance improves with scaling down of physical dimensions whereas interconnect performance degrades with scaling down of cross-sectional dimensions. In his talk, Dr. Azad Naeemi proposed a new interconnect-centric methodology to optimize the design of global interconnects by simultaneously maximizing data flux density and minimizing latency that also offers the best trade-off between energy dissipation and data flux density, and reduces interconnect crosstalk and silicon area used for repeaters substantially.

The afternoon session focused on packaging, characterization, and technology trends. Mr. Nozad Karim mentioned that to address today's complex electronic system designs, a "design chain management" approach should be implemented where silicon layout, IC packaging, and the final system are considered from the start of any project. He emphasized that the need is especially crucial for applications that include advanced packaging solutions, such as RF, high speed digital Gbit+, stacked packaging and system in a package (SiP). In his presentation, Mr. Michael P. Gaynor covered embedded passives,

shields, and RF functional blocks within the module package by utilizing various filters and BALUNs for WLAN and Bluetooth applications. He also briefly reviewed other passive component embedding technologies. The justification for embedding in general as well as for each technology was discussed. He highly emphasized that the embedded technologies provide opportunities for a low cost, size and performance solution to RF module packaging requirements.

Mr. Hassan Hashemi discussed an overview of challenges faced with power distribution in a mixed signal system-on-chip (SOC) device by using common practices and methodologies adopted for digital systems as an example. He also discussed the electrical and physical attributes of a state of the art mixed signal SOC. Trade-offs between common versus separate supply or return path in flipchip and wire bond package implementation of this device is reviewed. Dr. Dieter Schroder suggested that failure site location identification is becoming progressively more difficult due to the small feature size of today's devices, the complex device structure, consisting of many metal layers, flip-chip bonding, etc., pushing many existing characterization tools to the limits. The techniques that were discussed by him included IDDQ testing, liquid crystal, emission microscopy, microprobing, voltage contrast, optical beam induced resistance change, and picosecond imaging circuit analysis. He also suggested that scanning probes with submicron mechanical resolution and transmission electron microscopy with sub-Angstrom resolution allowing imaging of individual impurities, are improving. Dr. Deepak Goyal provided an overview of the typical failure modes and mechanisms observed in the advanced microelectronic packages. A brief introduction to the methodology of failure analysis of packages as well as failure analysis challenges for the next generation packages were presented. In addition, Dr. Deepak Goyal also discussed the current and next generation analytical capabilities for package level fault isolation and failure analysis. Mr. Christopher Taylor suggested that driven by consumer demand and the development of lower cost components, the portable wireless evolution promises lead to ubiquitous access to entertainment, communications and computer power. In his talk, Mr. Christopher Taylor reviewed broadband access and wireless portable markets, and provided an overview of the market trends and component requirements driving the increasingly important wireless segment of the semiconductor industry. In the last talk of the day, Mr. Ronald E. Curry mentioned that the vision for future convergence can be simply stated as "any device, anywhere, anytime" which requires melding of the communication and computing worlds leading to micro and macro level convergence. In his talk, Mr. Ronald E. Curry discussed the concepts of Micro and Macro convergence, and their impact on the society in the future. He also discussed technologies, platforms and initiatives that are accelerating the convergence of communications and computing.

The day ended with an hour long panel discussion consisting of eight speakers and moderated by Dr. Stephen Goodnick. The topic was "Future of Computing and Communication Technologies and Applications". Following a brief statement by each of the panelists on their vision for the future of computing and communications technology, the panel session solicited general questions from the audience. The discussions among panelists and between panelists and audience were lively and interesting.

The workshop was made possible by the hard work of the organizing committee consisting of members from both IEEE Phoenix Section CPMT Chapter as well as WAD Chapter. The overall success of the workshop was due to the long hours of dedicated work over a period of six months by all members of the workshop organizing committee. The workshop organizing committee consisted of the following members:

General Chair: Vasudeva P. Atluri, Ph.D.
Co-Chair: Bruce Kim, Ph.D.
Technical Program: Rao Bonda, Ph.D.

In conclusion, the workshop was very well attended and appreciated by the attendees. The net profits from the workshop are approximately $11843.20. Continuing with the tradition from last year, 50% of the profits, approximately $5921.60, will be donated to the IEEE Phoenix Section Student Scholarship Endowment at the Arizona State University Foundation. In addition to raising funds for local chapters, one of the goals of the workshop is to help increase the scholarship endowment. Over last two years, the workshop organizing committee was able to contribute approximately about $10,000.00 to the scholarship endowment bring the total endowment fund to greater than $35,000.00. This endowment is helping IEEE Phoenix Section give four awards to undergraduate students totaling to $4000.00 every year within IEEE Phoenix Section region. The students from Arizona State University, Devry Institute, Embry-Riddle Aeronautical University, and Northern Arizona State University are eligible to apply for these scholarships. The scholarship fund was initiated about five years ago jointly by IEEE Phoenix Section, IEEE / CPMT Phoenix Chapter, and IEEE / WAD Phoenix Chapter.

Picture of IEEE Phoenix Section Workshop 2003 Organizing Committee members in front IEEE Phoenix Section Display

Kneeling Down (Left to Right): Dr. Rao Bonda, Mr. Jim Drye, Mr. Steve Post, Dr. Chuck Weitzel, Dr. Bruce Kim, and Dr. Prashant Raghu

Standing (Left to Right): Dr. Ellen Lan, Mr. Sam Karikalan, Mr. Eric C. Palmer, Dr. Daoqiang Lu, Dr. Rashaunda Henderson, Dr. Shane Johnson, Dr. Ravi Sharma, Dr. Vasu Atluri, Mr. Steve Rockwell, Dr. Mali Mahalingam, Mr. Bruce Bosco, Dr. Dongming He, and Dr. Dave Penunuri

Not in the Picture: Dr. Steve Goodnick, Dr. Sandeep Sane, and Mr. Nitin Deshpande

New IEEE Fellows in CPMT

IEEE announced the newly-elected IEEE Fellows . The individuals' election to Fellow grade was approved by the IEEE Board of Directors at its 16 November 2003 meeting. Ten of these are members of the CPMT Society.

Rajen Chanchani, Sandia National Laboratories, for contributions to advanced packaging technologies.

Prof. Yan Cheong Chan, City University of Hong Kong, for contributions to electronic product reliability.

Hiromu Fujioka, Osaka University, for contributions to electron beam testing of semiconductor devices and circuits.

Erik H. M. Heijne, CERN, for contributions to semiconductor detector systems and radiation tolerant detector readout electronics.

Prof. R. Wayne Johnson, Auburn University, for contributions to electronics that must operate in harsh environments.

Kenneth Meade Lakin, TFR Technologies, for contributions to thin-film resonator technology and applications.

Douglas Strain, for leadership in the development of automated test and calibration systems.

Toshio Sudo, Toshiba Corporation, for contributions to high-density packaging.

Prof. Stuart K. Tewksbury, Stevens Institute of Technology, for contribtuions to telecommunication and interconnections in high performance digital systems.

Prof. Ifeanyi Charles Ume, Georgia Institute of Technology, for contributions to the thermomechanical reliability of microelectric packaging.

As details of each of these contributors become available we will feature each in this newsletter.

Rajen Chanchani now Fellow of Institute

Rajen Chanchani has been elected as IEEE-Fellow for his contribution to the development of advanced packaging concepts including technologies for high density interconnects, chip-scale-packages, micro-system integration, multichip modules and substrates, and for outstanding contribution and leadership in serving IEEE-CPMT society.

Rajen has received his Ph.D. and M.S. in Material Science & Engineering from the University of Florida. Since 1990, Rajen is working at Sandia National Labs in Albuquerque, New Mexico. Prior to that, Rajen worked for 5 years at AT&T Bell Labs, which was then the parent company of Sandia National Labs.

Rajen is an elected member of the Board of Governors, he has chaired CPMT Technical Committee on Materials & Processes and organized several IEEE-CPMT sponsored conferences. Rajen has developed and published in 1994 a pioneering wafer-level chip-scale-packaging concept, which has revolutionized IC packaging. Rajen has developed new concepts for packaging of advanced micro-system for use in National Security applications. This effort has led to several innovations including (i) integration of microfluidics with microelectronics and sensors, (ii) Tamper-resistant multichip modules, and (iii) Integrated Substrate Technology and System-on-chip. Rajen has published over 50 technical papers and has two patents.

Y. C. Chan Elected Fellow of Institute

Professor Y.C. Chan is best known for his high quality research in the electronic product reliability, failure analysis and reliability engineering. His research contributions, particularly in the area of intermetallic compounds effects on surface mount solder joints along with findings that the fatigue life times of certain types of solder joints are a function of the process parameters, all have contributed significantly to process improvement for manufacturing reliable electronic materials and assemblies.

He is also internationally known and famous for his establishment of the Electronic Packaging and Assemblies, Failure Analysis and Reliability Engineering Center (known as the EPA Center) at the City University of Hong Kong since 1997. Via the EPA Center, he is the first faculty in Hong Kong to establish a consortium of 50 local and multinational electronics companies with a view to improving the technological competitiveness in electronic product reliability.

The research results from Prof. Chan have been fruitfully used to benefit these companies. This has distinguished him from conventional academics whose primary research outputs appear in technical publications only. In the last few years, he initiated and is currently directing a research program on conductive adhesive technology, and his research team is publishing new reliability findings on particle micromovements and degrad-ation mechanisms in anisotropic conductive joints. In collaboration with local electronics manufacturers, his research findings has already led to the development of improved manufacturing processes for more reliable chip-on-flip LCD products.

He is also the Founding President and Honorary Chairman of the Hong Kong Electronic Packaging and Manufacturing Services Association (HKEPMSA). He must be the first person, as general chair of conference, to hold the three important international conferences: (1) Business of electronic product reliability and liability - January 13-17, 2003, Hong Kong and Shenzhen, China (2) Asian Green Electronics Manufacturing, June 23-26, 2003, Hong Kong and Shenzhen, China, and (3) Business of electronic product reliability and liability - April 27-30, 2004, Shanghai, China - where the IEEE CPMT is the technical sponsor for (1) and (2) and Reliability Society for (3).

Toshio Sudo now Fellow of IEEE

Toshio Sudo joined Toshiba Corporation, Japan, in 1975, where he has devoted himself to the development of high-density multi-chip modules to overcome the limitation of thick-film technology. His earlier development of copper/polyimide thin-film process on a silicon wafer has been presented since late 80's(ISHM'88, ECTC'90, IEICE'91, JSSC'95). He received the best paper award for this achievement in the Microelectronics Symposium in 1989 in Japan. He also contributed to the development of the high-pin count packaging for CMOS ASICs and microprocessors so as not to induce a large amount of simultaneous switching noise (SSN). He disclosed a lot of experimental data of SSN and package modeling approach in the 90's (ECC'89,EPEP'93, ECTC'94, '95, '96) by using a dedicated test chip. Furthermore, he presented many papers on the on-chip crosstalk noise of GaAs interconnects and the characterization of chip/package-level EMI (EMC'01, SPI'02). Toshio Sudo co-edited three books on the VLSI packaging technology including the translation to Japanese of the Microelectronics Packaging Handbook, 1st edition, Van Nostrand Reinhold ('91), and the contribution as a co-author to the 2nd edition, Chapman & Hall ('97).

CPMT Board Member Promoted

Johan Liu has been appointed as head of Division of Electronics Packaging in the National Swedish Institute for Production Engineering Research (IVF), Gothenburg, Sweden. Currently he is a professor in Electronics Production and head of the Division of Electronics Production, Chalmers University of Technology, located in Gothenburg, Sweden. After the appointment, Johan will run these divisions together and the staff from the organizations will be merged into one unit and physically sit together. Thus Ph D students at Chalmers University will work closely together with senior staff at IVF to conduct applied research, industrial projects and education in the field of integration technology and reliability for microsystems and microelectronics.

IEEE Awards Professor Rao Tummala

The IEEE EAB Major Educational Innovation Award recognizes IEEE members who have distinguished themselves by extensive outstanding educational innovation in a field of interest of the IEEE. The award consists of $1000 and a brass and walnut plaque. The proposed citation reads:

"For reforming Microsystems Packaging education by unparalleled, systematic and innovative approaches to courses, curricula, tracks, books, degrees and conferences while mentoring and catalyzing other centers of excellence around the world".

Rao has been the President of the CPMT for the last 4 years where he has guided the Society to encourage many universities to establish component, packaging, and manufacturing technology curriculum. He has recently authored the book "Fundamentals of Microsystems Packaging" which is used by many university students and working engineers to become knowledgeable in this new growing field. Rao received the award in Seattle on November 14th at the IEEE TAB meeting.

Auburn Wireless Program Receives $3.15 Million Vodafone Grant

Auburn University is one of three universities selected nationwide to receive nearly $3.2 million in funding for its wireless engineering program through the Vodafone-US Foundation Fellows Initiative according to an announcement by Larry Benefield, dean of the Samuel Ginn College of Engineering.

The five-year grant will be used for undergraduate scholarships, graduate fellowships and course and laboratory development. The University of California at Berkeley and the University of Illinois at Urbana-Champaign were also named as grant recipients.

The focal point for Auburn's activities centers on its Wireless Engineering Research and Education Center (WEREC), which is building on a $25 million gift from Auburn alumnus Samuel Ginn to develop a cutting-edge program in wireless engineering. A key element has been the creation of an undergraduate wireless degree program - the first of its kind in the nation.

The wireless engineering degree is offered through two departments within Auburn's College of Engineering - Computer Science and Software Engineering and Electrical and Computer Engineering - with hardware, software and network options.

-- submitted by Cheryl Cobb

12th Topical Meeting on Electrical Performance of Electronic Packaging

The 12th. Topical Meeting on Electrical performance of Electronic Packaging (EPEP) was held from October 27-October 29, 2003 in Princeton, New Jersey. The meeting provides a forum for the presentation and discussion of the latest advances in the electrical design, analysis and characterization of on-chip and off-chip package interconnections and structures covering all the application families and frequency ranges namely, digital, RF, microwave and mm-wave applications. EPEP is co-sponsored by the MTT and CPMT societies of the IEEE.

The afternoon of October 26, before the start of the conference, the third annual workshop, sponsored by the IEEE CPMT Society, **"Future Directions in IC and Package Design"**, had very good attendance of 60 participants from all over the world. Alina Deutsch of IBM Corp. and Madhavan Swaminathan of Georgia Institute of Technology chaired this meeting that had 7 excellent international invited speakers from the US, Europe, and Asia, that were divided into three sessions chaired by Greg Taylor of Intel Corp. and George Katopis of IBM Corp.

The first three speakers addressed high-end processor and package design issues. The second session covered tools and technology development needs and projections and the third special session addressed CAD tool development. The workshop was open to all EPEP conference attendees free of charge.

The **EPEP meeting** this year was organized into twelve sessions of oral presentations and one open forum (poster) session for one-to-one discussions. The papers represent 9 countries (Belgium, Sweden, Korea, Taiwan, Japan, Canada, Italy, Germany, and USA).

The meeting began with a keynote speech titled "Architecting Interconnect" by Peter Hofstee, IBM. (Dr. Hofstee, Vice President and General Manager, Desktop Platforms Group, IBM Corporation). Dr. Hofstee made the observation that the optimum pipeline depth for a microprocessor has 6 to 10 fan out
4 gate delays per pipe stage. He emphasized that Machines must be balanced for performance and power and that speculative computation is expensive. He quoted Gelsinger's Law: "New generation micro architectures use twice as many transistors for a 40% increase in performance". This implies a 30% reduction in efficiency. As a result, Dr. Hofstee sees multithreaded / multi core chips as the way of the future with software as the major bottleneck. With a fixed core micro architecture, I/O bandwidth needs to grow 40% per node as the number of cores per chip doubles. This path will lead to a need for 1 TB/s per socket at the end of the decade. Using 20% of the power budget of a 200W chip means that we'll need I/O that runs on 5 mW/(Gb/s).

The remaining eleven sessions were dedicated to System Design and technology, Power Distribution design and Noise, RF/Microwave, Electromagnetic Issues, Modeling, Transmission Lines, Measurements, On chip Issues (that mainly cover I/O circuit design, clock net design and analysis, and electrical parameter extraction), Interconnection macro modeling. This year, the conference also featured One session (7 papers from industry and academia) on on-chip CAD Issues.

On Sunday October 26, Two short courses were offered prior to the start of the meeting. The tutorials were given by well-known experts in their fields. One tutorial covered I/O circuit design and the other covered system power distribution.

Once again special attention was paid to graduate student attendees of this meeting with the presentation of Intel and IBM Corporation awards to the two most outstanding papers authored by graduate students. The IBM award consisted of laptop and $1000 cash and the Intel award consisted of $2500 cash. A total of 26 papers competed for these awards.

The best student paper award sponsored by Intel corporation was given to Anestis Dounavis, from Carleton University for his paper entitled "Delay Extraction and Passive Macromodeling of Lossy Coupled Transmission Lines.", Anestis Dounavis, Natalie Nakhla, Ram Achar, and Michel Nakhla.

The best student paper award sponsored by IBM corporation was given to Rohan Mandrekar from Georgia Institute of Technology for his paper entitle "Extraction of Current Signatures for Simulation of Simultaneous Switching Noise in High Speed Digital Systems.", Rohan Mandrekar, Madhavan Swaminathan, and Sungjun Chun.

An industry reception for students hosted by IBM was held on Tuesday October 28th that provided the opportunity to 14 students to get to discuss package design issues of interest with industrial representatives. In addition, the meeting hosted five exhibits.

Companies represented included: Intel (Israel), Optimal Corporation, Ansoft Corporation, Sigrity, Inc, and TDA Systems.

A special issue in CPMT transactions based on the paper version of the presentations at this 12th EPEP meeting will be edited by Dr. Tawfik Arabi of Intel and Dr. Robert Jackson from the University of Massachusetts.

--submitted by Tawfik R. Arabi

Future Directions in IC and Package Design Workshop

Oct. 26, 2003 -- Princeton, NJ

The third Future Directions in IC and Package Design, FDIP'03, workshop was held on October 26, 2003 in Princeton, NJ and was very well attended by 60 participants from all over the world. The meeting had seven excellent international invited speakers that were divided into three sessions. The sessions were chaired by George Katopis from IBM Corp. and Gregory Taylor from Intel Corp. For the first time this year, the third mini-session was added to cover one topic in depth by two experts in the field. The workshop was chaired by Alina Deutsch of IBM Corp. and Prof. Madhavan Swaminathan of Georgia Institute of Technology. The first three speakers addressed system design issues. The second session covered testing challenges and future developments. The third session addressed the requirements and developments in the area of on-chip CAD tools. The workshop was held the day before the start of the 12th IEEE Topical Meeting on Electrical Performance of Electronic Packaging, EPEP'03.

The first speaker, George Chiu from IBM, described a new supercomputer architecture paradigm using cost-effective system-on-a-chip approach together with high level of system integration. The Blue Gene/L supercomputer is aiming at a peak performance of 180TFLOPS and uses 65,536 nodes interconnected by a 3D torus, a combining tree, a Gb Ethernet , a global interrupt network, and JTAG. Each 15W node relies only on a single ASIC in 0.13 µm technology with 700 MHz PowerPC 440 cores.

The second speaker, Frank O'Mahony from Intel, reviewed the current state-of-the art in microprocessor clock networks. He noted that conventional techniques do not scale well and skew and jitter are increasing relative to clock period. New techniques are being explored to solve this timing uncertainty problem, namely optimal H-tree and deskew circuits, networks of coupled oscillators such as PLL arrays, VCO arrays or rotary arrays, and standing-wave clock networks with active transconductors to compensate for loss.

Y.L.Li from Intel addressed the challenges in containing the computer system electromagnetic radiation as the clock frequencies, the number of signal pins needed, and the power consumption are increasing. He showed several design options that were studied such as ground patches, via stitching, checkerboard via pattern, retreated power plane, and decoupling. The last three showed good performance in suppressing EMI.

Prof. Gordon Roberts from McGill University explained the need for developing embedded test capabilities for accessing the analog signals in mixed-signal applications. He showed several novel methods that have digital interface at the chip boundary and all the analog probing and processing is performed locally on the die. Such examples included on-chip sampling oscilloscopes, spectrum analyzers, pico-second timing analyzers, and relied on signal processing techniques such as pulse density modulation, coherent sampling, and others that were implemented already in 0.18um CMOS technology and gave 19-ps resolution for 5GHz clock frequency.

Prof. Luc Martens from Ghent University described the challenges encountered in modeling and characterizing complex multi-pin high-speed connectors commonly used for transmitting Gbps signals in digital and communication systems. Because of the complex geometry and the spectral content of the signals, both the modeling and parameter extraction are difficult to perform. 2-port measurements have to accommodate N-port systems with imperfect shielding and non-ideal connector-to-board transitions. Field solvers have to accommodate arbitrary shapes with many dielectric regions.

The last session was specially dedicated to CAD tool development and two experts in the field covered the needs encountered in the industry and how the university research in the area is trying to supply the demands. Howard Smith from IBM summarized the state-of-the-art in available on-chip CAD tools for analyzing crosstalk, common-mode noise, delta-I noise, static noise propagation, circuit leakage, and effect of noise on timing. All these effects are currently analyzed separately and linear superposition is employed. Global nets are in the order of 200K and TAT time needs to be around 8 hours to allow iteration in the design cycle. The key challenge is to find efficient and accurate algorithms that allow full-chip extraction, frequency-dependent and non-linear simulation to address all these effects simultaneously . Prof. Andreas Cangellaris from Univ. of Illinois presented 'Toward Full-Chip Analysis with Electromagnetic Accuracy". He called for synergism between device engineering, semiconductor process, system architecture, circuit design, interconnect technology and package design in order to achieve the goals of an SoC (system-on-a-chip) analysis. Advances have been made in fast field solver techniques, massively-parallel distributed computing practices, and model order reduction methods. Advanced EM-CAD technology will only be possible through the use of abstractions that result from the mathematical description of the specific physical models. He postulated that the ultimate objective is to develop model order reduction technology that hybridizes not only circuit simulation and electromagnetic modeling but also addresses the complexity of multi-physics modeling in support of META-chip design.

All the talks have been posted on the IEEE CPMT Society web page, under the Activites of the Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS) at http://www.ewh.ieee.org/soc/cpmt/tc12/

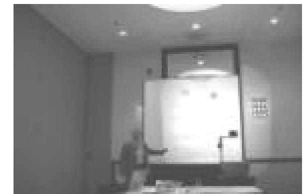
Alina Deutsch & Madhavan Swaminathan, Co-chairs

George Katopis, IBM

George Chiu, IBM

Frank O'Mahoney, Intel

Y. L. Li, Intel


Greg Taylor, Intel

Gordon Roberts McGill University

Luc Martens, Ghent Univ.

Howard Smith, IBM

Phoenix Chapter Workshop Success

Thursday, November 20th, I went to a workshop on Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications at ASU in Tempe, Arizona. While embedded passives are still a hot topic, it seemed this year a concurrent theme was the tendency to go smaller and what issues are being faced in this quest for miniaturization.

The morning session was focused on devices and the first speaker was the keynote one, Peter Zeitzoff from SEMATECH and a CMOS roadmap. Moore's law was mentioned and while its focus is on device size, the real issue associated with it is increased speed and increased function density of future ICs. The International Technology Roadmap for Semiconductors (ITRS), of which Mr. Zeitzoff is an integral part, is an effort to map IC technology for the next 15 years, addressing key needs, solutions and stimulating R and D. Used to project this map is a scaling approach, where some of the targets are speed and power. Maximum speed is the inverse of the intrinsic delay, so naturally the desire to scale down this delay is key. Seventeen percent every year is the goal, set by current transistor scaling. Lower power dissipation is also desirable and is directly associated with leakage current and Vdd, two significant parameters in the scaling goal. Some solutions to these issues are high k dielectric materials to replace SiO2 (for leakage current), strained channels (speed, improves u) and metal gates (leakage current). There are a number of other avenues being pursued to remedy the many challenges presented by scaling so quickly into the sub-micron regime.

Next was a presentation on Silicon Nanotechnology by Suman Datta from Intel. Nanotransistors will allow Moore's Law to accurately predict the scaling of transistors and technology. A Pentium 4 now has about 40 million transistors, a number that is predicted to increase to about 1 billion by 2007. A 15 nm gate length transistor is projected by 2010 and 10 nm early next decade. Included in nanotechnology ideas is a 5-nm silicon nanowire ready by 2013 and offering additional gate control. New process techniques are necessary for nanotransistors and can include atomic layer deposition, high k dielectric stack, and strained silicon or metal gates. Challenges predicted are phonon interaction effects with high k dielectric materials and physics limitations on just how small is realizable.

Yang-Ki Hong from the University of Idaho addressed Trends in Magnetic Information Data Storage and MRAM. With the need for increased storage comes new development and characterization of magnetic nanoparticles and nanofilms that include CoCrPt-based alloys, self assembled CoPt and FePt. New advances in shapes of magnetic tunneling junctions for MRAM devices are being made. In addition to the already existing shapes of rectangle, hexagon and ring MTJs, Dr. Hong presented a Pacman shape that offers high switching field and the narrowest switching field distribution over the other shapes. Dr. Hong and his team at the University of Idaho are actively researching magnetic storage solutions.

Jim Teplik from the SPS at Motorola presented RF and Mixed Signal Technologies. The SiGe HBT offers high fT and a high fmax by having a thin base region and a low Rb, respectively. Graded Ge yields an improved output conductance over non-graded Ge and strained SiGe offers the lower Rb, which can increase current gain, b. When carbon is added to the structure, this helps keep the base region thin, increasing the fts. Vertical scaling was also mentioned, improving frequency performance through the base profile, collector resistance and collector doping. Integrating SiGe HBTs with CMOS was presented as an attractive technology (BiCMOS) with a low noise figure and high b, but the cost is still high. Signal isolation is also an issue of system on a chip type integration. RF CMOS was also addressed with effective length and oxide thickness being scaled now. Challenges with decreasing size, however, dominate the use of RF CMOS. Leakage current, lower gain and dynamic range are a few of the problems that affect RF CMOS. Passive structures were also mentioned for their role in matching. Although improvements have been made (metallization, dielectric materials), area is still a large concern.

Azad Naeemi from Georgia Institute of Technology spoke of Optimal Global Interconnects for Gigascale Integration. With the roadmaps predicting smaller and smaller feature sizes, interconnects have become a dominant concern as they do not scale with technology. Optimal dimensions were emphasized for small latency (faster communications) and large bisectional bandwidth (larger transfer of information). Dr. Naeemi introduced a new design approach, an interconnect-centric rather than a transistor-centric one for GSI chips. Since interconnects contribute to the limitations, the designs should center around those, focusing on optimal wire widths and aspect ratios. Optimizing these for maximum data flow and minimum energy is the ultimate goal. Issues presented include delay variation, multilevel and intra-level crosstalk and energy per bit.

The afternoon focus was on packaging and began with Nozad Karim from Amkor talking about High Speed Package Design. He emphasized the need for a design chain that considers layout, IC packaging and the final system from the beginning of a project. This is especially important when a complex package is necessary. Package selection, pre-design, and simulations are all key in reducing design iterations. Add nanometer designs and more challenges arise like capacitance, current leakage and package issues like metal pitch. Package considerations should be addressed as soon as possible for all aspects of design, power/ground structures, I/O signals, and EMI concerns. Advantages of certain packaging techniques should be known, e.g., when to use a flipchip design or wirebonds, each having their own tradeoffs. Package consideration at the start of a project helps reduce the design cycle in system on a chip designs.

Michael Gaynor, also from Amkor, addressed Embedded Passives, RF Functional Blocks and Shields. Cost reduction, routing and height reduction were the main reasons mentioned for embedded RF functions. Various laminates were discussed like Getek, LTCC, and a Getek - BT-MG combination, all of which can be utilized for RF functional blocks such as filters and baluns. They have developed a library offering filters, BALUNs and diplexers with the goal of reducing design time and lowering development costs. Getek is the preferred substrate for embedded RF functions where the functions presented were utilized for the cell phone or wireless communication industry. Embedded passives hope to offer more integration, lower cost and better reliability than soldered passives. Some of the substrates used for this are ceramic filled FR4, thick and thin films and silicon. Although highly desired, embedded passives still face challenges. Right now the tools and processes are immature which affects cost and reliability, major factors in the success of embedded passives. Embedded shielding and its desired effect of reduced coupling was also mentioned. Experiments have been done but design rules are still being defined at this time.

Hassan Hashemi from Mindspeed Technologies talked about Broadband Mixed Signal System Level Packaging, which focused on power distribution in a mixed signal system-on-chip device. Some of the challenges facing mixed signal IC-package-board design are power distribution system (PDS) simulation, deciding which design technique works well for a mixed signal design and correlating measurements to simulations. PCB PDS designs were examined and utilized for a system level and package level design. Tradeoffs between wire bonding and flipchip techniques were also discussed. Isolation and how to tradeoff the analog and digital supplies were a couple of the challenges PDS designers are faced with.

Characterization and Failure Analysis of Silicon Devices, Current and Future was presented by Dieter Schroder from Arizona State University. With decreasing device sizes, new materials and different structures, failure analysis is now more difficult. The challenge lies in determining where the failure site location is with new packaging technologies (flipchip) and increasing metal layers. Techniques discussed to locate the failures include picosecond imaging circuit analysis, voltage contrast, IDDQ testing and microprobing, among others, all of which were discussed in detail. Failures detected by some of these are gate oxide shorts, incorrect timing or slow switching, and physical defects. Failure analysis today pushes the limits of existing tools, but with the development of new tools, some mentioned in this presentation, characterization and analysis are overcoming some of these challenges.

Deepak Goyal of Intel presented Failure Analysis of Packages, first talking about typical failure mechanisms in packages. ON the 1st level interconnections, wire bond damage is fairly common with damage occurring at the neck and heel, depending on what type of bond was done. C4 interconnections can show cracks between bumps, also considered 1st level. On a package level, there can be corrosion, "popcorning" (die surface delamination), via adhesion issues and PCB cracking. Solder balls and bumps also exhibit cracks or fatigue from underfill. With the new technology showing thinner packages and more complex structures (mixing packaging techniques) come different failure mechanisms and increased difficulty isolating where the failure occurred. New techniques are being developed that include x-ray tomography, thermal imaging and laser milling all of which have their own tradeoffs. The focus of the next generation of tools is to develop non-destructive techniques.

Christopher Taylor from Strategy Analytics addressed The Road to Ubiquitous Computing, Entertainment, and Communications focusing on wireless and broadband markets. The first topic was broadband access and its increasing trend. More consumers are opting for broadband connections and seeing the advantages of doing so. This increase drives the WLAN devices in homes to share this connection; WLAN almost doubled from 2002 to 2003. This trend leads to developments in the WLAN future like home video distribution, mesh networking and WLANs connected via 802.16. 802.16 capabilities will further increase wireless mobility. UWB is also on its way up, an attractive alternative to USB for digital cameras and camcorders. The 3G cellular market is also increasing, but not at the same rate as the broadband market; consumers are not completely convinced of its benefits. These increasing markets dictate component trends with goals of lower cost, more integration, higher Ft and longer-term cost, more integration, higher Ft and longer-term products. More functionality is also a goal of the digital processors necessary to complete these products and make them competitive. Though still uncertain, UWB, mesh networks and RFID are just a few of the promising technology that awaits society.

Vision for Convergence: Next Generation Computing and Communications Solutions was presented by Ron Curry from Intel. "Anytime, anywhere, any device." This was the vision presented by Mr. Curry that sets the goal that a user will have access to information or services at any given moment and place. Micro and macro convergence is when computing and communication come together on both small and large scales. Micro-convergence offers integration with reduced cost and new capabilities. This leads to macro-convergence that produces new businesses, infrastructures, and new societal norms. New devices like sensors, and areas of technology like silicon photonics, fluidics and healthcare are being enabled by the marriage of computing and communications. Convergence is ever accelerating and with it comes new and exciting technologies.

■ submitted by Emily Selves

Editor's Note

It is late Sunday night and this Newsletter must be mailed early tomorrow to the printer. Articles are still coming in. Several articles in this issue were spill overs from last issue. For example, a great report on the Student chapter in Bucharest just arrived, but I am out of room and time for this issue. I will keep putting these new items on the web Newsletter(see page 1 for the link). I will also not repeat a lot of the meeting ads in this issue since most of them are past paper submission date.

Thanks to everyone who worked so hard submitting material including David Whalley, Dr. Parikh, Emily Selves, Marsha Tickman, Rao Bonda, Rao Tummala, Ricky Lee, Steve Adamson, Alina Deutsch, Madhavan Swaminathan, Tom Tarter, Dan Bauks, Yoshitaka Fukuoka, Paul Wesling, Vasudeva Alturi, Angie Hughes, Cheryl Cobb, Tawfik Arabi, and Susan Puccetti.

There is no room for the follow upcoming meeting ads but they have good web pages so you will be able to find out how to attend and what papers and speakers will be there.

ECTC: Las Vegas, Nevada, June 1-4, 2004, home web site, www.ectc.net

ISQED: San Jose California, March 22-24, 2004, home web site, www.isqed.org

Nano Bio-Packaging, Atlanta, Georgia, March 22-23, 2004, at www.prc.gatech.edu/news_events/2004nwlp/2004nwlp.htm

Nominations Solicited for IEEE CPMT Society Awards

CPMT Society solicits nominations for the following awards for the year 2004. These wards are offered for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society. For nomination guidelines, basis of judging, and further information about the awards, please visit the website http://www.cpmt.org/awards/index.html. Nomination forms can be obtained from the website, or from the CPMT awards committee chair. **The due date for receiving the nominations is January 31, 2004.**

David Feldman Outstanding Contribution Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
Prize: $2,500 and Certificate
Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2003.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate
Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2003.

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate
Eligibility: No need to be a member of IEEE and CPMT Society.

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
Prize: $2,500 and a Certificate.
Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2003. There are no requirements for service to the IEEE or CPMT Society.

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.
Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.
Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2003, and must be 35 years of age, or younger, on December 31st, 2003.

Please send nominations to CPMT Society Awards Committee Chair by e-mail, fax or mail:

Rao Bonda, Ph.D.
Motorola, Inc.
2100 East Elliot Road,
Mail Drop: EL725
Tempe, AZ 85284, USA
Phone: +1-480-413-6121
Fax: +1-480-413-4511
Email address: r.bonda@ieee.org or rao.bonda@motorola.com

Winners will be notified by February 29, 2004 and the awards will be presented at the 54th Electronic Components and Technology Conference, June 1-4, 2004, in Las Vegas, Nevada, USA.

Call for Papers

The 7th ***VLSI PACKAGING WORKSHOP of JAPAN***

Nov. 30 - Dec. 2, 2004

Kyoto Research Park, Kyoto, Japan

Sponsored by the IEEE CPMT Society and National Institute for Standards and Technology

The VLSI Packaging Workshop of Japan has been held every other year since 1992 in the best season of Kyoto, the ancient capital of Japan, and it has become a well-known international workshop for advanced packaging technologies. The committee strongly encourages you to attend this workshop and participate in the discussion, in order to understand technology trends and find the proper target for technology development. Bring your latest research results and share with the participants who are experts from industry and the grove of Academe, and discuss with them. Anybody contributing to human progress through electronics is very welcome at this workshop. The following areas of technology are primarily of interest to the participants:

+ Advanced Fine Pitch Packaging
+ 3D Packaging & COC (Chip on Chip)
+ Micro Bumping Technology
+ Laminated Materials & Processing
+ RF Components & Modules
+ Integrated Passives
+ Packaging for Optoelectronics
+ Failure Mechanisms & Reliability Improvement
+ Electrical Performance & Thermal Management
+ Wafer Level CSP
+ Manufacturing Technology
+ Pb Free Interconnections
+ Materials for High Speed Application & Wafer Process
+ RFID tags
+ System in Package (SOP)
+ MEMS Packaging Technologies
+ Assembly and Packaging Challenges for Cu/Low-k Chips
+ Wafer Level Burn-in

The official language of this workshop is English. 30 minutes is allocated for each presentation, and it should include 5 - 10 minutes for Q&A. Authors who give outstanding papers will receive official recommendations for paper submission to the IEEE Transactions by the Japan Chapter and the Workshop Committee. This workshop will be held at Kyoto Research Park where the 6th Workshop was held in 2002.

Commercial purpose exhibition will also be held there, as was done at the previous Workshop, in order to promote commercial products for packaging. Those who are promoting new products for packaging should not miss this opportunity. The details of the exhibition will be available shortly on the web site of this Workshop.

http://homepage1.nifty.com/ieeetokyo/chapter/cpmt/vlsip.html

***Submission of abstracts*:**

Those who wish to contribute to the workshop should send a two-page summary of their paper (including figures) to the Program Chair **by May 28th, 2004**. The title of the paper as well as the names and affiliations of all authors must appear on the summary. If the paper is accepted, the summary shall be written to fit in a four-page format for the workshop's Proceedings **by September 3rd, 2004**. Notification of acceptance will be given **by July 9th, 2004**.

Program Chair

Michitaka Kimura, Renesas Technology Corp.
4-1, Mishear, Tami-shi, Hyogo, 664-0005, Japan
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Tel: +81-72-784-7127, Fax: +81-72-780-2676

General Chair:

Masahiko Kohno, Dow Chemical Japan Limited
Email: mkohno@dow.com

Vice Chair:

Tomoshi Ohde, Sony Computer Entertainment Inc.
George Harman, NIST

Japanese Committee:

Fuminori Ishitsuka, NTT Electronics
Noboru Iwasaki, NTT
Nobuo Kamehara, Fujitsu
Harufumi Kobayashi, Oki
Kaoru Kobayashi, Kyocera SLC Tech.
Hiroshi Manita, Casio
Tadaaki Mimura, Matsushita Electronics
Hirofumi Nakajima, NEC Electronics
Atsushi Nakamura, Renesas Tech.
Atsushi Okuno, Japan Rec
Kanji Otsuka, Meisei Univ.
Hiroshi Shibata, Osaka Inst. Tech.
Toshio Sudo, Toshiba
Takeshi Takamori, Oki
Hiroshi Yamada, Toshiba

US Committee

Phillip Garrou, Dow Chemical
Sheng Liu, Wayne State Univ.
Len Schaper, Univ. of Arkansas
Ephraim Suhir, IOLON
E. Jan Vardaman, TechSearch

European Committee:

Rolf Aschenbrenner, IZM, DE
Soeren Noerlyng, Micronsult, Denmark
David Whalley, Loughborough Univ. UK

Asian Committee:

C. P. Hung, ASE, Taiwan
Jung-Ihl Kim, Amkor, Korea
Ricky Lee, HKUST, Hong Kong
Thiam-Beng Lim, IME, Singapore
Kyung-Wook Paik, KAIST, Korea

IEEE CPMT Japan Chapter:

Nobuo Iwase, Toshiba

29th International Electronics Manufacturing Technology Symposium

to be held as the SEMI Technology Symposium (STS: IEMT) at SEMICON West

July 14-16, 2004 -- San Jose, California

CALL FOR PAPERS

Semiconductor Equipment and Materials International (SEMI), and IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society invite manufacturing professionals from around the world to submit abstracts to STS: IEMT at SEMICON West 2004. STS: IEMT continues to be one of the leading technical conferences for discussing solutions that improve the electronics manufacturing process. For equipment and materials suppliers, and device manufacturers, STS: IEMT provides unparalleled opportunities for both electronics and microelectronics professionals to network and learn the latest in manufacturing strategies and methodologies to achieve manufacturing excellence. Abstracts are peer-reviewed and are selected based on a clear outline of problem, analysis, solution/results and conclusion. Presentations on original, non-commercial and non-published works are being solicited in the following areas:

3D PACKAGING

TEST, ASSEMBLY AND PACKAGING ADVANCED MANUFACTURING PROCESSES

ADVANCED MATERIALS AND RELIABILITY

ENVIRONMENTALLY FRIENDLY MANUFACTURING (CFM):

Ultraclean technologies; Clean materials; Mini environments; Environmental factors; Carrier influence; Recyclability

COST REDUCTION:

Cost management; Cost of ownership; Benefit of ownership; Justification/ROI for capital expenditures; Supplier/Customer continuous improvement programs

TEST, ASSEMBLY AND PACKAGING FACTORY DYNAMICS:

Continuous improvement processes; Qualification strategies; Extending current capabilities; Manufacturing line performance; Methods to determine capacity components and magnitudes; Capacity detractors and analyses of causes for detractors and cycle time losses (tool, operator, WIP, etc); Cycle time and fabricator load/capacity relationships; Activities undertaken to reduce capacity detractors; Deployment and implementation of work method changes into manufacturing, EMS/IC assembly, Semiconductor assembly

WIRELESS AND OPTICAL NETWORK COMPONENT AND SYSTEMS MANUFACTURING TECHNOLOGY:

OE/EO components and assembly; RF, Planar and Other lightwave circuits manufacturing and packaging

ADVANCES IN WAFER LEVEL AND CHIP SCALE PACKAGING:

Wafer bumping; Photolithography challenges; Singulation; Wafer breaking/scoring; Overmolding; Redistribution; 300 mm manufacturing challenges; Wafer thinning; 3D assembly

TIME-TO-MARKET:

Design for manufacturability (DFM); Technology transfer; Quality functional deployment (QFD); Early manufacturing involvement; Theory of constraints (TOC)

YIELD ENHANCEMENT:

Wafer level/Board level inspection tools and techniques; Defect inspection methodologies; Wafer level reliability (WLR); Failure analysis; Yield modeling; Process defect reduction; Defect reduction in materials; Defect-to-yield correlations; Design for manufacturability; Product Yield Risk Assessment (PYRA); In-line inspection; Intelligent data analysis; Systematic yield problems

PRODUCT TEST AND TEST PROCESS OPTIMIZATION:

High speed testing; High bandwidth; Mechanical probing; SOC; SIP; Structural testing; Dynamic burn-in

OFFSHORE VS. ONSHORE MANUFACTURING:

Technology transfer and resources; Local content; Culture/Language barriers; Maintaining yield; Fabless and manufactureless

MEMS/MOEMS TECHNOLOGY:

Manufacturing techniques; Novel materials and problems unique to specific projects; Meaning of volume manufacturing to MEMS suppliers; Implications of using smaller wafers and older tools

PANEL DISCUSSIONS AND/OR WORKSHOPS

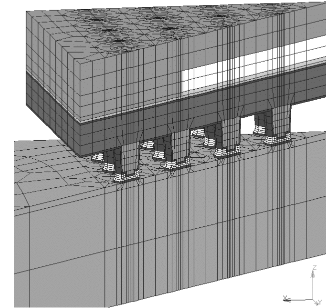
SUBMISSIONS:

Papers co-authored by a user and a supplier and/or academia that address practical solutions to real problems are highly encouraged. Abstracts are welcome from all those involved in electronics manufacturing including: merchant and captive IC manufacturers, equipment and materials suppliers, packaging foundries, contract assemblers, and academia and research institutions.

Prospective authors are requested to submit the following by February 7, 2004: a 250 word abstract, paper title, author name(s), company/affiliation(s), a 25-word biography of the principal author, and primary contact information. Because correspondence is conducted electronically, e-mail address is mandatory. Authors selected to present at the conference will be notified via e-mail by mid-March. A final camera-ready manuscript in MS Word file and IEEE copyright form must be submitted by the determined due date to be published in the STS: IEMT 2004 proceedings and in order to present at the conference.

Please submit your abstract to the following:

Online: www.semi.org or www.cpmt.org/iemt E-mail to: techspeakers@semi.org Please note subject line: STS: IEMT 2004 Abstract Submission



Fifth conference on

Thermal & mechanical simulation and experiments in micro-electronics and micro-systems

May 9-12, 2004 in Brussels, Belgium

The Conference: May 10-12, Brussels, Belgium

EuroSimE 2004 will address the results of both fundamental research and industrial application for **thermal**, **mechanical** and **thermo-mechanical** solutions of (micro)-electronics, focusing on advanced **simulation** and **experiments**. A preliminary program will be available **by Jan. 15**. Brief overview of conference topics (oral and poster sessions):

- Trends in Microelectronics & Microsystems
- State of the Art in Thermal and Mechanical Simulations
- Reliability of (leadfree) Solder Interconnection
- Advanced Packaging and MEMS Designing
- Designing for Endurance and Reliability
- IC Process Reliability Modeling and Characterization
- MEMS, Sensors and Actuators
- Characterization and Modeling of Materials and Reliability
- Adhesives, Encapsulation, and Underfill
- Simulation and Optimization in Microelectronics
- New Techniques in Modeling and Characterization
- Dynamic Compact Thermal and Electro-Thermal Models
- Thermal Behavior Modeling and Characterization
- Small Scale Thermal and Fluid Aspects in Microsystems
- CFD and FE Modelling of Thermal Performance

Short courses: May 9, Leuven, Belgium

Up to **six** professional development **short courses** will be offered, taking place at IMEC-Leuven.
Final course topics will be announced by Jan. 15. Following topics are planned:

- Wafer level packaging technologies
- Lead-free solder joint reliability
- Static and dynamic compact thermal models for the thermal analysis
- Heat sink design and analysis for microelectronic equipment
- Microvias and high density interconnects for advanced packaging
- Micromechanical Sensors

Other conference features

- On Monday evening, a conference dinner with surprise act is planned. Tuesday evening comprises a special Belgian beer tasting event.
- A parallel **exhibition** from industrial contributors and simulation and optimization software companies.

Registration / Preliminary program / Latest information

http://www.eurosime.com/ Information local organiser: Bart.Vandevelde@imec.be ;
Marion.Hegemann@imec.be (tel.: +32 16 281 849)