

Components, Packaging, and Manufacturing Technology Society



Newsletter



The Global Society for Microelectronics Systems Packaging



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www.cpmt.org
www.evh.ieee.org/soc/cpmt/newsletter

PRESIDENT'S REPORT

Greetings to all CPMT Society members and friends.

As I begin my term as CPMT Society President, I'm excited about how far we've come as a Society and am looking forward to helping take CPMT to the next level in the industry, building on the contributions of my predecessors.

I'd first like to thank Dr. Rao R. Tummala for the wonderful job he did as immediate past President. He left the Society in great shape and will be a tough act to follow. And, as always, we are lucky to have Marsha Tickman, our Executive Director on board to help ease the transition.

Increased Global Presence

A lasting legacy that Rao's administration left behind is the increased participation by a broad global audience. He really helped to shape the notion of CPMT as a global society. To continue growing an active and robust organization, I believe we need to continue on this path and expand our efforts. One way to do this is to increase leadership presence outside of the United States. While many of our members continue to be located in the United States, we have seen a large growth in Asia and Europe, as well as in Latin America and Canada. In recognizing this trend, we now have two officers from outside the United States. Dr. Ricky Lee (Hong Kong) accepted the role as Vice President of Conferences, and Dr. Rolf Aschenbrenner (Germany) is taking the helm as Vice President of Technical Activities. This is a first in the CPMT Society's 50-year plus history.

Continuing on the path of global expansion, I plan to introduce additional proposals that would increase local representation, leadership presence and more tailored conference coordination around the world. The goal is to have our members, wherever they may reside, feel that they have a voice and ownership in the direction of the Society.

Enhanced Web Site

With these increased global efforts, comes a need for better coordination and communication. Living in the "Internet age" gives us opportunities to link together as we never have before. As such, look for a redesigned and enhanced Web site at



www.cpmt.org. We hope to make the site the first place you will go for all of your CPMT Society information, conference news, publications information, education opportunities and other tools to keep you in step and involved.

A great way to show your support for this effort is to sponsor a Web page on the Web site. If you or your organization are interested, please contact Tim Adams at t.adams@ieee.org or Paul Wesling at p.wesling@ieee.org.

(continued on page 3)

CPMT OFFICERS

President -- Phil Garrou, +1 919 248 9261
Technical VP -- Rolf Aschenbrenner, +4930-46403164
Administration VP -- H. Anthony Chan, +1 408 924 3656
Treasurer -- John Segelken, +1 540 961 1685
VP Publications -- Paul B. Wesling, +1 408 252 9051
VP Conferences -- Ricky Lee, +852 2358 7203
VP Education -- Albert Puttlitz, FAX +1 802 879 0466
Senior Past President -- John Stafford, +1 602 413 5509
Junior Past President -- Rao Tummala, +1 404 894 9097
Secretary -- Ron Gedney, +1 703 834 2084
Executive Director -- Marsha Tickman, +1 732 562 5529
IEEE VP TAB -- Ralph Wyndrum, +1 732 219 0005

Elected Board Members

2004: Tim Adams, N. Rao Bonda, Rajen Chanchani, Ralph Russell, Connie Swager, Naoaki Yamanaka

2005: William T. Chen Li Li, L. Merrill Palmer, Walter J. Trybula, E. Jan Vardaman, David C. Whalley

2006: William D. Brown, Philip C. H. Chan, Charles Lee, Johan Liu, Thomas G. Reynolds-III, Ephraim Suhir

Standing Committee Chairpeople

Student Chapter Development -- William D. Brown, wdb@enr.uark.edu
Distinguished Speakers -- A. F. Puttlitz, FAX +1 802 879 0466
Fellows Search--Rao Tummala-rao.tummala@ee.gatech.edu & David Palmer-d.palmer@ieee.org
Fellows -- C. P. Wong, cp.wong@ieee.org
Constitution & Bylaws -- TonyMak, +1 972 371 4364
Finance -- Ralph Wyndrum, Jr., r.wyndrum@ieee.org
Long Range Planning -- Dennis Olsen, d.olsen@ieee.org
Standards --
IEEE Books & C and D Magazine Editor, Joe Brewer, +1 386 445 2593, j.brewer@ieee.org
Membership -- Ralph Russell, cpmt-membership@ieee.org
Chapter Development -- Ralph Russell, II, see membership
Nominations -- John Segelken, +1 540 633 5781
International Relations -- Leo Feinstein, +1 508 870 0051; Europe - Ephraim Suhir, +1 908 582 5301; Far East -- W. T. Chen, +65 874 8110
Joint Committee on Semiconductor Manufacturing -- G. C. Cheek

Next News Deadline: June 5, 2004

Members-only Web:

UserName: xxxx (join CPMT to find out)

Password: xxxxxx (for 2nd quarter)

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CPMT SOCIETY NEWSLETTER

Editor: David W. Palmer, email: d.palmer@ieee.org,
FAX +1 505 844 7011, Tel: +1 505 844 2138
Composition: Alina Deutsch: deutsch@us.ibm.com
Proofreading: Janice Washington

CPMT Archival Publications

Publications VP: Paul Wesling, email: p.wesling@ieee.org,
Tel: +1 408 252 9051.
Transactions-CPT editor, Avram Bar-Cohen, Univ. of Maryland,
2181B Martin Hall, College Park, MD 20742 USA,
Tel: +1 301 405 3173; email barcohen@eng.umd.edu
Transactions-AdvP editor; G. Subbarayan, Purdue University, ME
Department, Tel: +1 765 494 9770; email ganeshs@ecn.purdue.edu
Transactions EPM editor, Walter Trybula, Tel +1 512 356 3306,
email w.trybula@ieee.org

Technical Committee Chairpeople

TC-ECCC (1) Electrical Contacts, Connectors and Cables--
Gerald Witter, Chugai, +1 708 244 6025
TC-DIP (2) Discrete and Integral Passive Components—
Leonard Schaper, Univ. of Arkansas, +1 501 575 8408
TC-Assy (3) IC and Package Assembly – Michele Berry, Intel
michele.j.berry@intel.com
TC-EM (4) Manufacturing Design & Process—Walt Trybula,
SEMATECH, +1 512 356 3306
TC-M (5) Materials—Rajen Chanchani, Sandia Labs,
+1 505 844 3482, r.chanchani@ieee.org
TC-HDSB (6) High Density PWB packaging -- Yoshitaka Fukuoka,
weisti.fukuoka@rose.zero.ad.jp
TC-ASTR (7) Environmental Stress & Reliability Test--Kirk Gray,
k.a.gray@ieee.org
TC-Therm (9) Thermal Management & Thermomechanical Design--
Tony Mak, Dallas Semi, +1 972 371 4364
TC-Opto (10) Fiber Optics & Photonics—Frank Shi, UC Irvine
email: FGSHI@uci.edu
TC-Test (11) Electrical Test -- Bruce Kim, Bruce.Kim@asu.edu,
Tel: +1 480 965 3749
TC-EDMS (12) Electrical Design, Modeling and Simulation--
Madhavan Swaminathan, G Tech, +1 404 894 3340
TC-PEP (13) Power Electronics Packaging--Doug Hopkins, SUNY
Buffalo, +1 607 729 9949, d.hopkins@ieee.org
TC-SP (14) Systems Packaging— John Segelken, jsegelken@
Actmicrodevices.com, and Connie Swager,
swager@us.ibm.com
TC-RF+W (16) RF and Wireless-- Craig Gaw, Motorola,
+1 480 413 5920, c.a.gaw@ieee.org
TC-MEMS (17) MEMS and Sensor Packaging—Eric Jung, IZM
Berline email: erju@izm.fhg.de
TC-WLP (18) Wafer Level Packaging—Michael Toepper, IZM
Berline toepper@izm.fhg.de
TC-Ed (19) Education--Rao Tummala, G Tech, +1 404 894 9097
TC-GEMP (21) Green Electronics Manufacturing and Packaging,
Hansjoerg Griese, Email: griese@izm.fhg.de
TC-NANO Nano Packaging -- Rao Tummala, Georgia Tech,
rao.tummala@ee.gatech.edu

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Let Me Reintroduce You

I'm often asked at conferences and in the workplace to describe what the CPMT Society is, exactly. So I thought it might be worthwhile to re-introduce the Society to you, and let you know what we offer. The CPMT Society is one of 42 Societies within the IEEE. The IEEE is comprised of 350,000 members worldwide and is one of the largest technical organizations in existence.

Local Chapters

Members of the IEEE have the option to join one of 42 special interest groups (Societies), ranging from the Aerospace and Electronic Systems Society to the Vehicular Technical Society. All Societies are global in nature like the CPMT Society and have local chapters as we do. To find a chapter near you, visit www.ewh.ieee.org/soc/cpmt/chapters. Looking forward, we hope to create additional chapters to serve our members everywhere.

CPMT Society Fields of Interest

Within the IEEE, the CPMT Society claims responsibility for component design and manufacture as it pertains to the packaging of active devices and the assembly of such packaged devices into sub-systems as part of the manufacture of complete electronic systems. For a more complete description, visit www.cpmt.org/cpmtwho.html.

Technical Committees

Technical Committees are designed to address specific needs within our fields of interest. They change as needed to reflect changes in technology, as new topics emerge and others begin to fade. A complete list of these committees can be found at www.cpmt.org/tc/index.html. I encourage you to explore the currently available topics and lend your expertise.

Education Focus

I feel strongly that our Society should take seriously the charge to disseminate information that contributes to the education of our members and to the students who will follow us into our profession. Over the past several years, we have developed a number of courses that are available for universities and others around the world to use. You can view them online at www.cpmt.org/education/index.html. We plan to continue adding content to this important area.

Number One Source for Archival Information

Another way we service those in our profession is to use the resources of the IEEE to archive relevant technical information of our industry. Over the years, the CPMT Society has developed three peer journals – *Transactions on Components and Packaging Technologies*; *Transactions on Advanced Packaging*; and *Transactions on Electronics Packaging Manufacturing*. They allow and encourage professionals to submit their work to be evaluated by expert peers in their technical area. When accepted, it is published and then indexed and archived for posterity. A recent IEEE study revealed that IEEE journal articles are overwhelmingly cited in research and used for patent applications. For details on these journals and how to submit original manuscripts, visit www.cpmt.org/trans/index.html. **3**

Most Importantly – You!

To keep these worthwhile activities fresh and relevant we need the members and their collective expertise to stay actively involved. I strongly encourage every one of you to find an area where you think you can make a contribution and get started! You can provide as little or as much time as you wish, and it need not involve travel or a long-term commitment. To find the right opportunity for you, contact the leadership listed on the Web site or contact Marsha Tickman at m.tickman@ieee.org.

I look forward to working for each and every one of you and thank you for your loyalty to the Society.

Editor's Turn

Once again many of your fellow volunteers sent in news items for this newsletter. In particular we must thank: Dr P. B. Parikh, David Whalley, Paul Wesling, Phil Garrou, Ricky Lee, Ralph Russell, Johan Liu, Wayne Johnson, Romina Macabinski, Nihal Sinnadurai, Margie Ballinger, Gabriel Gaus, Reed Crouch, and C. P. Wong. Also we benefit with Janice Washington joining our team working on layout and proofing.

This is also the season where all the paperwork must be submitted for IEEE Fellow nominations. The whole CPMT Board would like to thank the brave handful of volunteers who served as nominators for our next crop of Fellows. Many hours go into composing the long nomination form. In addition, we should all thank the existing 110 CPMT Fellows, many of whom took the hour to fill out the Reference form to back up the Nomination form. Each nomination takes at least 5 Fellow references. In a typical year about 10 CPMT members get nominated so you can see the mountain of paperwork. However, it is paperwork for a good cause.

Remember you must be a Senior Member to be considered for the Fellow title. Most of our members qualify for Senior Member status but never take the hour needed to look up the IEEE web page and initiate the email action. For example, if one has a BS technical degree plus 7 years of experience you qualify. To affirm this qualification you need to email 3 Senior members of your choice to electronically send in a one paragraph recommendation. There are more than 26 thousand Senior members (~10% IEEE voting membership), so you know at least 3 of them.

Once a Senior Member, to optimize your chance of gaining Fellow recognition a safe strategy is to both publish articles based on your work for your employer and being enthusiastically involved in some aspect of CPMT volunteer effort. Guiding a chapter's activity, working on conference organization, taking on publication responsibility, or governing from the CPMT Board are examples of accomplishments a Fellow candidate typically exhibit.

ECTC is coming up in the ever popular Las Vegas. Just remember that clever engineers lose money gambling on the average just the same as silly tourists. See you there!

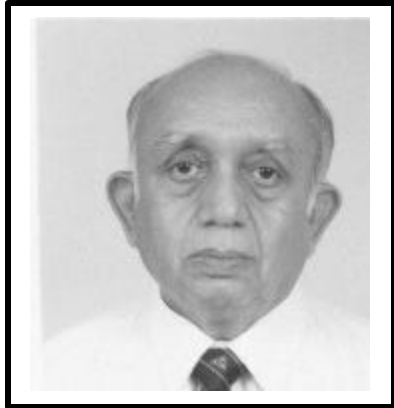
■ editor

CHAPTER NEWS

REGION 10 CHAPTER ACTIVITY ROUND-UP

-- by Dr. P. B. Parikh

** Dr. Cheung Yiu-Ming, Ken reported extensive year 2003 activity for **HongKong Chapter** having conducted five workshops and the chapter plans



similar activity for the year 2004 as well. These workshop programs for 2004 would include topics such as MEMS packaging, chip-on-flex, electronics packaging, system reliability along with the general trend for lead-free and 3-D packaging. The chapter's plans on this year's students activity include a student symposium in May 2004 and a number of industry visits for student members. Dr. Ming Li of CUHK (the current Chapter Vice-Chair) and Dr. Derek Or of PolyU (the current Chapter Secretary) have been elevated to Senior Member grade.

The executive committee for IEEE-CPMT HongKong for the year 2004 continues to be:

Dr. Cheung Yiu Ming - Chapter Chairman
Dr. Li Ming - Chapter Vice-Chair and Chair-Elect
Dr. Or Siu Wing - Chapter Secretary
Dr. Sham Man Lung - Chapter Treasurer

Dr. Lih-Shan Chen has reported that **Taipei CPMT Chapter participated in the co-organisation of an International Conference on "Informatics, Cybernetics and Systems" at I-Shou University, Kaohsiung, Taiwan on December 14-16 2003. The event attracted more than 200 participants. Dr. James L. Massey and Dr. Vijay K. Bhargava were invited to deliver the keynote speeches at the conference.

The executive committee for CPMT Taipei chapter for the year 2004 is announced as:

Dr. Shen-Li-Fu - Chairman
Dr. Lih-Shan Chen - Secretary

Prof K N Seetharamu of **Malaysia Chapter reported two technical programs during this quarter, one on "BioMEMS-Cell based Micropump" on 26th December 2003 and the other is a technical talk by Mr. Teck Joo Goh on "Analysis and design of Thermal Test Vehicle" scheduled on 17th March 2004. The chapter would also co-organise the 6th EMAP International Conference on Electronics Materials and Packaging in December 5-7, 2004.

The executive committee for CPMT Malaysia Chapter for the year 2004 is as under:

Prof K N Seetharamu - Chairman
Prof. Dr. Zulkify Md. Abdullah - Vice-Chairman
Mr. Chew Chee Hong - Vice-Chairman
Mr. Goh Teck Joo - Intel - Secretary
Prof P A Aswatha Narayana - Treasurer
Members - Prof Dr. Mani Maran
Prof Dr. Zaini Allmuddin Zainal Alauddin

Mr. Ahmad Baharuddin Abdullah

Mr. Omar Ghazali

As reported by Dr. Mo Zhimin, the **Shanghai CPMT Chapter has planned their 7th IEEE CPMT International Academic Conference on, "Next Generation Microsystem Packaging Research and Education," June 28-30, 2004, followed by the 6th IEEE CPMT conference on, "High Density Microsystem Design and Packaging and Failure Analysis," June 30-July 3, 2004, both at Shanghai University, China. These will be jointly organised with the Scandinavian Chapters.

The executive committee of CPMT Shanghai Chapter for the year 2004 is as under:

Dr. Johan Liu - Chairman
Dr. Rolf Jansson - Treasurer
Members - Mr. Bo Wikstrom
Mr. Peter Frisk
Mr. Kare Gustafsson
Mr. Jakob Janting
Mr. Henrik Jacobsen
Mr. Johan Anderson
Ms. Cristina Anderson
Mr. Li-Rong Zheng
Mr. Roger Rorgren

Prof Paik of **Korea Chapter has reported that the chapter provided technical support for conducting "SMT/PCB Technical Seminar" on 25th February 2004 at Seoul, Korea. The chapter has also planned a workshop on "3-D chip stacking technology" in June 2004 at Seoul, Korea, as a joint program with CPMT Deajon Korea chapter.

The Chapter officers have been announced as:

Prof. Kyung W Paik - Chapter Chair
Prof Joung-Ho Kim - Vice-Chair
Dr. Jae-Woong Nah - Secretary/Treasurer
Technical Chairs - Dr. Soon-Jin Cho
Mr. Se-Young Jang
Mr. Sung-dong Cho

The **India Council Chapter reported a spurt in the chapter activities in the year 2003 with as many as 8 technical programs (including 5 technical lectures and 3 two-day seminars/conferences). In addition, the chapter also organised 3 administrative sessions at various locations to facilitate meetings with the outstation members (Delhi and Bangalore).

During this quarter, the chapter provided support for the organisation of a 3-day Annual Seminar on "VLSI Design" at Bombay on the 7th, 8th and 9th of January 2004. This mega event involved participation of 430 VLSI Design experts as delegates. The chapter also participated with COMPONEX as a co-organiser for a 2-day International Conference on "Commercialisation on Microsystems and Nanotechnology" on 13th and 14th of February 2004 in New Delhi. The event with 5 technical sessions involved presentation of 19 papers and was very successful with large-scale industry participation at all India levels.

The executive committee for CPMT India Council Chapter for the year 2004 is as under:

Dr. P. B. Parikh - Chapter Chairman
Dr. Shankara Prasad - Chapter Vice-Chairman
Prof M. M. Shah - Chapter Secretary/Treasurer
Members - Dr. Maneesh Guru Dhingra
Dr. J. N. Roy
Mr. I. M. Rao



Dr. Shen-Li-Fu - Chairman, Tipai Chapter

REGION 8 CHAPTER ACTIVITY ROUND - UP

CPMT Student Branch Chapter of the "Politehnica" University of Bucharest

On December 22, 2003, the CPMT Student Branch Chapter of the "Politehnica" University of Bucharest together with CPMT Hungarian Romanian Joint Chapter organized the workshop: "Actual issues in developing the technological environment" at the Politehnica University of Bucharest, Center for Technological Electronics and Interconnection Techniques, which attracted thirty participants.

The first 2004 Meeting of the chapter, in January, was dedicated to officer elections: Simion Zanescu is the chapter chair, Romina Macabinski, vice-chair; Iulian Talpiga, secretary; Florin Streza, treasurer; and Professor Dr. Paul Svasta is the chair advisor. The chapter has now increased in size to 24 members.

The Student Branch Chapter, together with the Center for Technological Electronics and Interconnection Techniques, attracts undergraduate students by proposing several projects which are displayed on the Internet. The project topics are related to the CPMT fields of activity. Based on the preliminary information and theoretical aspects of the chosen project, every team of students builds a small educational software program. In this way the theoretical aspects become better understood and the students use their skills and creativity to make the theory more attractive. The evaluation of the projects is made by elder Student Branch Chapter members together with the advisor. This activity starts on the 1st of March, at the same time as the second semester every year. This activity is now in its second year and is becoming a tradition.

News from the Nizhny Novgorod joint ED/MTT/AP/CPMT/SSC-SS Chapter

On 14 November 2003, the chapter held its annual joint technical meeting attended by 18 chapter members and 3 other invited attendees. The program included a presentation by the Director of the Nizhny Novgorod Physical Engineering Institute, Dr. Prof. O.N Gorshkov, describing the institute's branches, main topics of investigation and technologies and analytical facilities. There was also a contribution by Prof. D. Pavlov on "Er-doped optical active phosphate films" and a tour of the Institute.

The Chapter provides technical and financial assistance for regular seminars on Microwaves and Electrodynamics at the Nizhny Novgorod State Technical University (NSTU). Four Chapter members have regularly attended the seminars which have included, "Finite Element Method for Development of new UHF - EHF assembles and applications of it," by Dr. Yu. G. Belov, NSTU on 25/09/03 and "Non-linear scattering of radio waves and some applications of its theory", by Mr. A. A. Vasenkov, NSTU on 20/10/03.

On 27 - 29 August 2003, the Chapter co-sponsored a seminar attended by 98 people on "SHF -EHF engineering", which included 65 contributions on topics such as high power tubes and systems using them, solid state devices and assemblies, semi-conductors and super pure materials for SHF-EHF engineering and radio systems.

On 16-17 September 2003, the chapter co-sponsored an inter-regional seminar on "Precise processing of dielectric materials", with 7 contributions and attendance by 25 people, including 5 IEEE (MTT, ED, SSC, CPMT-SS) members.

On 18 November 2003, the chapter co-organized, together with the Volga regional department of Scientific Council of Russian Academy of Science, "Radio waves propagation" branch and the Nizhny Novgorod Radio Physics and Applied Physics Research Institutes, the second regional (river Volga basin) scientific seminar on "Microwave propagation in natural media" at the Nizhny Novgorod, Radio Physics Research Institute. There were 15 contributions and 40 participants, of which 5 were IEEE (AP, MTT) members. Topics included; microwave refraction and molecular absorption in the atmosphere; mitigation, scattering and polarization effects of microwaves at the system "atmosphere - ground surface"; microwave fluctuation along the ground and slant traces; remote sensing of the ground surface and atmosphere, including the meteorological and environmental aspects of the problem; simulation of microwave propagation and remote sensing of natural media; and facilities and techniques for study of mi

-- submitted by David Whalley



CPMT Society Chapters

Do you know...

- The most effective way to enhance your IEEE CPMT membership experience?
- How to maximize your professional development?
- How to plug into networking opportunities?
- How to share in the best ideas brewing among your peers?
- The best win-win opportunity available to all IEEE CPMT members?

Your IEEE CPMT Local Chapter does!

Visit a CPMT Chapter event in your area and increase the value of your CPMT membership! To find a chapter near you, visit <http://www.cpmt.org>.

Submitted by:

Ralph W. Russell, II

Director - Global Chapter Development

SCV Chapter's Recent Activities

The Santa Clara Valley CPMT Chapter continues its activities on behalf of local engineers and developers. Our program has four components: evening technical meetings and networking; technical short courses; professional-development classes; and local and international conferences.

Our monthly dinner meetings started 2004 with two events: "OLED Display Technology and Applications" with Homer Antoniadis, OSRAM Opto Semiconductors in January, and "Titanium 2 Package Development Tradeoffs" by Kevin Haley, Intel in February.

We mount the presenter slides for many of our talks on the CPMT Society's "Members-Only" website, so others worldwide can review the points and conclusions. This is a way to quickly familiarize oneself with the technology or predictions that we've heard at our regular meetings. The Chapter now has so many potential speakers for our dinner meetings that we are starting a lunch series (to be once a quarter at first, but may expand to monthly). The talks emphasizing technology will remain in the evening, where we have more time to explore a topic; presentations that lean more toward management issues and technology predictions will have the shorter lunchtime venue.

One of our charters is to bring training and new techniques to our technical membership base. Last September we presented the one-day class on "Principles in Wirebonding for Microelectronics" with CPMT Fellow George Harman of NIST. He also was our featured speaker at our September meeting (and his slides are on the Members-Only website).

Then, in December, we had two half-day classes: "Printed Circuit Technology: Materials and Processes" with Joseph Fjellstad, and "Thermal Test Methods for Integrated Circuits" with CPMT Fellow Bernie Siegal of Thermal Engineering Associates.

In March we are promoting Short Courses that come to our area with major CPMT conferences: "Experimental Measurements in Thermal Management of Electronic Systems" with Profs. Ortega (UA), Moffat (Stanford), Westphal (WSU), and

Rhee (SJSU), "How to Achieve Electromagnetic Compatibility While Solving Thermal Problems" by Dr. Tom Van Doren, "Compact Thermal Modeling: Theory and Practice" with Clemens Lasance (Netherlands) and Heinz Pape (Germany), "Thermomechanical Reliability of Microsystem Packaging" with Prof. Jianmin Qu, and "Compact Modeling and Analysis for Nanometer-scale CMOS Design" with speakers from IBM, Georgia Tech, U-Michigan, UC-SD, Purdue, and Intel.

Bringing new technology to our members (and, for higher registration fees, our local non-members) is a key goal of our Chapter.

We conducted eight Professional Skills classes during autumn, including

"Breakthrough Project Management" and "Collaborative Negotiating" with Barry Flicker,

"Presentation Skills for Engineers" with Peter Roselli, "Time Management Made Easy" with Peter Turla,

"Transitioning From Individual Contributor to Manager" with Dr. Andrew Oravets, and

"Process Metrics to Improve Results" with Roxanna Dunn.

We thank our corporate hosts for these classes: Hewlett Packard, Philips Semiconductor, Tibco Software, and Sony.

We have scheduled an additional nine courses for the winter/spring season.

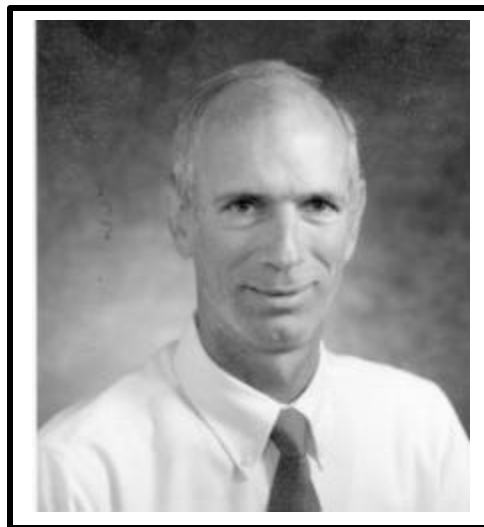
Other CPMT Chapters might wish to arrange to have these Skills classes given in their areas; we have already conducted several of them in Texas and Colorado.

Lastly, we host a number of great conferences here in Silicon Valley each year. Coming up in March are the CPMT's SEMI-THERM Symposium (now in its 20th year) and the International Symposium on Quality Electronic Design (ISQED), in its 5th year. We will have membership display tables at both, giving away past CPMT Transactions and our CPMT brochures to prospective members and gathering names and email addresses for our Chapter's DList.

This summer we host the International Electronics Manufacturing Technology (IEMT) Symposium.

Our Chapter elected new officers for 2004: Tom Tarter as chair, Bernie Siegal as vice-chair, Allen Earman as secretary, and Annette Cheung as treasurer. Janis Karklins takes over as membership development chair.

Submitted by Paul Wesling, Chapter Advisor



UKRI Chapter Announcement

In order to serve the technical community served by CPMT, the UKRI CPMT & Reliability Chapter has recognised the benefits of working with kindred societies to ensure that we do not act in a divisive manner in planning and delivering our technical programme. Accordingly, we have reached an agreement with the International Microelectronics and Packaging Society (IMAPS) UK Chapter, that we will aim to work together and to co-sponsor technical conferences and seminars serving the same interests. Additionally, the international IMAPS body arrived at the same decision at a meeting at the major Conference in Boston in November 2003.

We are pleased to announce that two such collaborative events were held in the UK in 2003.

The first was the Ceramics Interconnection Initiative Conference held earlier in the year at the Novotel at Heathrow. A number of eminent ceramics technology experts from the USA, Nordic countries and the UK presented leading edge papers to an international audience comprising over 70 IEEE members, IMAPS members and non-members.

The second event which was held at the Hayley Conference Centre at Stratford-upon-Avon during 1-2 October 2003, also attracted over 70 international and national delegates and speakers. The conference themes were, "Microelectronics in Medicine - the Convergence of Bioscience and Microsystems Technology," "Polymers for Advanced Microelectronics Fabrication & Structure," and a "Market Watch" session. There was very active participation in the Market Watch session, which will be a feature at future events.

Planning is well advanced for a co-sponsored Conference on "Packaging for Optoelectronics" to be held in early March 2004 at the Moller Centre of Cambridge University.

--Prof. Nihal Sinnadurai
Chairman CPMT & Reliability Chapter

JOBS EXCHANGE

People with job openings or wanting positions in CPMT fields such as materials, components, packaging, and manufacturing technology are welcome to use the CPMT website's facilities.

Go to www.cpmt.org

Then select either "Position Wanted", "Positions Available", "Student Resume", or "Faculty Position" link in the low left of screen.

Annual CPMT Scandinavian Chapter Meeting

The 2003 Annual IEEE-CPMT Scandinavian Chapter meeting was held at IVF, Göteborg, Sweden on Dec. 8. Delegates from Denmark, Norway and Sweden joined the meeting. Johan Anderson presented the annual report from



the 2003 board and Cristina Andersson the annual activities of student chapter. The new board for next year was established and Johan Liu continues to chair the Scandinavian chapter. Besides the administration issues, academic lectures were given by Thomas Lewin, Henrik Jakobsen and Anders Andrae, covering microwave system design, MEMS packaging and environmental assessment.

CPMT has New Senior Members

Moises Cases -- Texas
William F. Fouse -- Ohio
Deepak Goyal -- Arizona
T. Tom Jiang -- Idaho
Werner Johler -- Switzerland
Prassana Karpur -- Arizona
David C. Keezer -- Georgia
Karl F. Schech, Jr -- Maryland
Andrew F. Skipor -- Midwest
Harold L. Snyder -- Texas
Daniel S. Stevens -- New Hampshire
Gangqiang Wang -- Missouri

SIITME 2003 – September 18-21, TIMISOARA, Romania

Between September 18 and 21, 2003, the Electronics and Telecommunications Faculty of the 'Politehnica' University of Timisoara and the Center for Electronics Technology and Interconnection Technique from the Politehnica' University of Bucharest organized the **9th International Symposium for Design and Technology of Electronic Packages, (SIITME 2003)**.

This prestigious international scientific symposium, constituted as a forum for presentation of fundamental and applied research, presents a bridge between the university environment, research institutes and firms working in Electronic Technology fields such as hardware, software, RF-wireless, microelectronics, and optoelectronics and so on.

The 9th edition brought together both local and foreign personalities in the field of Electronic Packaging, many of them members of the IEEE - CPMT Society.

Most important is that Technical Universities from Romania promote electronic packaging and they are now capable of shaping high quality human resources in the fields of conceiving, designing and manufacturing high fidelity miniaturized electronic components that will later contribute to support Small and Medium Enterprises.

One of the first activities of the SIITME 2003 conference was a meeting of IEEE - CPMT Hungary & Romanian Joint Chapter members.



IEEE - CPMT Hungary & Romanian Joint Chapter members.

Members of the IEEE-CPMT Student Branch Chapter from 'Politehnica' University of Bucharest also attended this meeting, which was to promote electronic packaging in the field of interconnection design, joint projects and teleworking activities. The news of receiving the "2003 Best Student Branch Chapter of the Year Award" during the ECTC 2003 conference was shared with all of the Joint Chapter members. This award represents the CPMT Society's recognition of the Student Branch Chapter activities.

The Opening Ceremony of the SIITME 2003 Symposium was held in the "Plauşius Andronescu" amphitheater. The Ceremony was chaired by the Rector of "Politehnica" University of Timisoara, Professor Ioan Carji, together with the Dean of Ele c-

tronics and Telecommunications Faculty, Professor Viorel Popescu and the Conference Chairman, Professor Paul Svasta.



SIITME 2003 Opening Ceremony

The large number of participants presented 57 papers, in six oral presentations sessions and two poster sessions covering the following topics:

- electronic packaging education and training
- CAE - CAD - CAM for electronic packages and modules; modeling and simulation;
- advanced technology;
- thermal management, reliability and life time prediction;
- technology, quality and testing of electronics equipment.

It is important to emphasize the large involvement of students from five Technical Universities of Romania and other foreign countries (the Czech Republic, Germany Hungary, Poland, and Slovenia), with over 25 students and PhD students attending SIITME 2003.



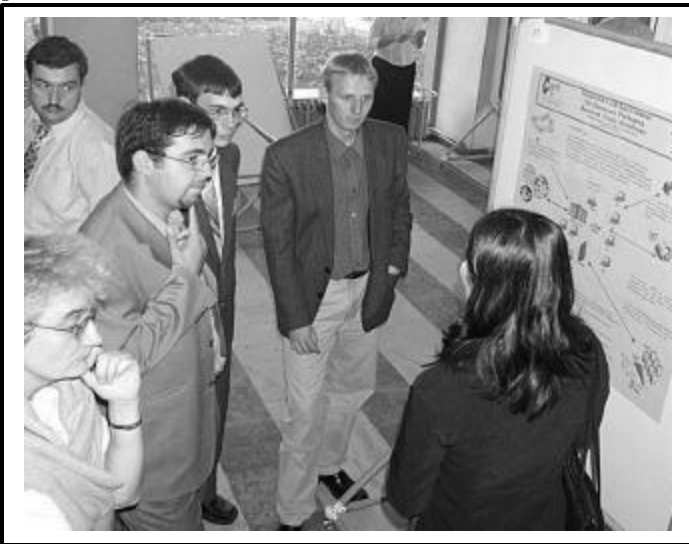
Some of student participants at the conference

Students participated in this conference with oral papers and also posters, most of them being greatly appreciated by the SIITME 2003 Steering Committee. Two papers and two posters represent the Student Branch Chapter contribution to this symposium.



Student Diana Chirileasa, presenting her Poster to the Evaluating Committee: Professors Pavel Mach(CZ), Darko Belavic(SLO, Dan Pitica(RO), Pal Nemeth(HU), Virgil Golumbeanu(RO and Alimpie Ignea(RO), (from left to right)

The quality of the posters made by students has improved every year. The participants had many questions relating to the topics presented in the posters, so interesting discussions took place.



Student Camelia Popescu (RO) presenting her Poster to participants

As the participants came from different countries, new important connections have been established and the first steps for future collaborations were made.

Based on the results of the International Steering Committee evaluation the organizers of the SIITME 2003 symposium offered separate awards for young scientists and for senior scientists. These awards were “**Excellent Award**” and “**Best Award**” for papers or posters.

At the end of the awards ceremony, the participants were presented with information on SIITME 2004, the 10th edition, which will take place between September 23 and 26 in Bucharest.



From left to right: Ovidiu Pop and Gabriel Chindis, Ph.D Students from Technical University of Cluj – Napoca, Professor Ioan Lita from Technical University Pitesti, Marina Zarnik PhD, Josef Stefan Institute, Slovenia and Professor Paul Svasta from Universitatea Politehnica Bucurest

Romina Daniela Macabinski,
Press Officer - IEEE Student Branch Chapter of Politehnica
University of Bucharest, Romania
romina@cetti.ro

New Web Content -- ONLY for CPMT Members!

Your membership in the IEEE and the CPMT Society just got more valuable!

Beginning January 10th, all CPMT members were enabled to use our Members-Only webspace to access full-text papers or presentations, in PDF format, from several recent conferences:

**IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '02

**IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '03

**EuroSimE'03: 4th Int'l Conference on Thermal Simulation in Micro-Electronics and Micro-Systems (France)

**Phoenix Chapter Fall'03 Workshop on Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

These are papers and presentations that cannot be found on IEEE's XPLORE. For someone who is not a CPMT member, they can only be purchased on CD-ROM. If you have a need to learn the latest in any of the fields above, check out the Tables of Contents and read some of the fine papers presented there.

Accessing our Members-Only area is very simple:

Point your Browser to: www.cpmt.org/mem/

When you are asked, enter:

Username: xxxx

Password: xxxxxx

(all lower-case, notice to know what to put in for the xxxx's you must look at page 2 of the latest CPMT printed newsletter, a newsletter that is mailed only to members)

New IEEE Fellows in CPMT

IEEE announced the newly-elected IEEE Fellows. The individuals' election to Fellow grade was approved by the IEEE Board of Directors at its 16 November 2003 meeting. Only 0.1% of voting IEEE members can be promoted to the Fellow position each year (around 250 engineers). Ten of these are members of the CPMT Society.

Rajen Chanchani, Sandia National Laboratories, for contributions to advanced packaging technologies.

Prof. Yan Cheong Chan, City University of Hong Kong, for contributions to electronic product reliability.

Hiromu Fujioka, Osaka University, for contributions to electron beam testing of semiconductor devices and circuits.

Erik H. M. Heijne, CERN, for contributions to semiconductor detector systems and radiation tolerant detector readout electronics.

Prof. R. Wayne Johnson, Auburn University, for contributions to electronics that must operate in harsh environments.

Kenneth Meade Lakin, TFR Technologies, for contributions to thin-film resonator technology and applications.

Douglas Strain, for leadership in the development of automated test and calibration systems.

Toshio Sudo, Toshiba Corporation, for contributions to high-density packaging.

Prof. Stuart K. Tewksbury, Stevens Institute of Technology, for contributions to telecommunication and interconnections in high performance digital systems.

Prof. Ifeanyi Charles Ume, Georgia Institute of Technology, for contributions to the thermomechanical reliability of microelectric packaging.

As details of each of these contributors become available we will feature each in this newsletter. Nomination forms for the class of 2004 Fellows were submitted by the March 15, 2004 deadline and will be announced this November. See "Editor's Turn" for a description of the process one must follow to be a future Fellow. There are 5602 Fellows in the 360,000 member IEEE. This is a recognition that not only is given to the accomplished individual but to the company or university for which they associate.

R. Wayne Johnson now IEEE Fellow

Dr. Johnson is a Ginn Professor of Electrical Engineering at Auburn University and Director of the Laboratory for Electronics Assembly and Packaging (LEAP). At Auburn, he has established teaching and research laboratories for advanced packaging and electronics assembly. Research efforts are focused on materials, processing, and reliability for electronics assembly and for high temperature electronics. He has published and presented numerous papers at workshops and conferences and in technical journals. He has also co-edited one IEEE book on MCM technology and written two book chapters in the areas of silicon MCM technology and MCM assembly and one book chapter on high temperature packaging. He is an Associate Editor of the IEEE Transactions on Electronics Packaging Manufacturing. He received the 1997 Auburn Alumni Engineering Council Senior Faculty Research Award for his work in electronics packaging and assembly.

Dr. Johnson was the 1991 President of the International Society for Hybrid Microelectronics (ISHM). He received the 1993 John A. Wagnon, Jr. Technical Achievement Award from ISHM, was named a Fellow of the Society in 1994 and received the Daniel C. Hughes Memorial Award in 1997. He is a Fellow of IEEE, and a member SMTA, and IPC.

Dr. Johnson received the B.E. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and the Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in electrical engineering. He has worked in the microelectronics

industry for DuPont, Eaton, and Amperex.



UPCOMING CPMT CONFERENCES

**2004 IEEE/SEMI Advanced Semiconductor Manufacturing Conference & Workshop (ASMC) May 4-6, 2004; Boston MA, mkindling@semi.org 1-202-289-0440, fax:1-202-289-0441

**8th IEEE Workshop on Signal Propagation on Interconnects (SPI'04) May 9-12, 2004; Heidelberg, Germany, Hartmut Grabinski, Universität Hannover, Phone: +49-511-762-5030; Fax: +49-511-762-5051; email grabinski@lfi.uni-hannover.de

**5th int'l Conf on thermal, Mechanical and Thermo-mechanical Simulation and Experiments in Micro-Electronics and Micro-Systems EuroSimE 2004, May 10 - 12, 2004; Brussels, Belgium; Bart Vandeveld (Bart.Vandeveld@imec.be); Marion Hegemann (Marion.Hegemann@imec.be -(tel.: +32 16 281 849)

**27th International Spring Seminar on Electronics Technology (ISSE) 13-16 May, 2004; Sofia, Bulgaria Technical University of Sofia; isse-office@tu-sofia.bg

**2004 IEEE 54th Electronic Components & Technology Conference (ECTC'04), June 1-4, 2004; Las Vegas NV, jadams@eia.org Judy Adams 1-703-907-7536 (fax: +1-703-907-7549)

**Photomask Europa 2004 ; June 21-24, 2004; Dresden, Germany

**7th IEEE International Academic Conference on Next Generation Microsystem Packaging Research and Education, June 28-30, 2004; Shanghai, China ; Ms Chen Jie, smit@mail.shu.edu.cn

**6th IEEE Conference on High Density Microsystem Design and Packaging and Failure Analysis (HDP'04); June 30-July 3, 2004; Shanghai, China ; Ms Chen Jie, smit@mail.shu.edu.cn

**29th International Electronics Manufacturing Technology Symposium (IEMT); July 14-16, 2003 ; San Jose CA, held at SEMICON West; Gloria Lou, SEMI glou@semi.org or +1.408.943.7048

**2004 IEEE Holm Conference on Electrical Contacts (HOLM); September 20-23, 2004; Seattle WA; Jennifer Lambert (IEEE Conf Mgmt) j.lambert@ieee.org; 1-732-981-3870 fax: +1-732-981-1203

**7th VLSI Packaging Workshop of Japan (VLSI Pkgng) ; Nov 30 - Dec 2, 2004; Kyoto, Japan ; Dr. Max Kohno, Dow Chemical. +81-550-82-8030 mkohno@dow.com

**6th International Conference on Electronic Materials & Packaging (EMAP); December 5-7, 2004; Penang, Malaysia; Prof. K N Setharamu, USM, knseetharamu@hotmail.com

**6th Electronics Packaging Technology Conference (EPTC'04); December 8-10, 2004; Singapore; Prof. Toh Kok

Chuan, Nanyang Technological Univ, +65 6790 5583. mkctoh@ntu.edu.sg

ECTC Professional Development Courses on June 1, 2004

**Optoelectronic Components and Modules for Communication; Bill Ring, Tyco Electronics Networks, wsring@tycoelectronics.com

**Advanced Organic Substrate Package Design & Manufacturing for RF and Broadband, Hassan Hashemi, Mindspeed Technologies, Inc., hassan.hashemi@mindspeed.com

**Integrated Passive Technology and Commercialization; Richard Ulrich, University of Arkansas; rulrich@uark.edu

**Polymers for Electronic Packaging; C.P. Wong, Georgia Institute of Technology; cp.wong@mse.gatech.edu

**System-on-Package (SOP) vs. System-in-Package and System-on-Chip (SOC) – New Paradigms in Electronics; Rao Tummala, Georgia; Institute of Technology; r.tummala@ee.gatech.edu

**NANO – The Next Technology? Overview of NanoTech: Walt Trybula, SEMATECH and Deb Newberry, Newberry Technologies; w.trybula@ieee.org -- dmnewberry2001@yahoo.com

**Microelectronic and MEMS Sensors; Garbor Harsanyi and Zsolt Illyefalvi-Vitez, Budapest University of Science & Electronics

**Microelectronics Packaging and Interconnection – A Worldwide Perspective; Jan Vardaman, TechSearch International, Inc.; tsi@techsearchinc.com

**RF/Wireless Packaging; Manos Tentzeris and Jay Laskar, Georgia Institute of Technology; etentze@ece.gatech.edu; jlas-kar@ece.gatech.edu

**Wafer Level - Chip Level Packaging; Luu Nguyen, National Semiconductor Corporation; l.nguyen@ieee.org

**Microvias & High Density Interconnects for Advanced Packaing; Ricky Lee, Hong Kong U. of Science and Technology rickylee@ust.hk

**Interconnects and Packaging Challenges for 10 Gb/s and 40 Gb/s; Roberto Coccioli, Inphi Corp. Telecom and Datacom; and Hassan Hashemi, Mindspeed Technologies, Inc.; rcoccioli@inphi-corp.com hassan.hashemi@mindspeed.com

**Packaging Failure Analysis – Failure Mechanisms and Analytic Tools; Deepak Goyal and Rajen Dias, Intel Corporation; deepak.x.goyal@intel.com rajen.c.dias@intel.com

**Advanced Thermal Management Materials; Carl Zweben, Advanced Thermal Management Materials Consultant

**Introduction to Nano Packaging and Systems; Rao Tummala and Zhong L. (ZL) Wang, Georgia Institute of Technology; r.tummala@ee.gatech.edu

**Lead Free Solders for Robust IC Electronic and Optoelectronic Packaging; John Lau, Agilent Technologies, Inc.: john_lau@agilent.com

submitted by Albert Puttlitz, VP Education → →

54th Electronic Components & Technology Conference Highlights (ECTC)

(Las Vegas, Nevada)--The program for the 54th Electronic Components & Technology Conference at Caesars Palace will feature 325 technical papers presented by leaders in their field representing countries from around the world.

The conference is organized into 39 technical sessions covering a wide range of topics, including optoelectronics, RF and MEMS packaging, 3D and high performance package design, flip chip and Pb-free interconnections, wafer-level packaging and manufacturing, reliability test methods, and electrical, thermal and mechanical modeling. Two special topic areas will explore MEMS and nanotechnology as part of an ongoing effort to bring emerging technologies that have great future potential together with key established packaging technologies.

Two poster sessions on Wednesday, June 2 and Thursday, June 3 will offer unique opportunities for authors and attendees to interact, discuss in detail, and exchange ideas in a more relaxed forum.

New this year is the NEMI Tin Whisker Workshop on June 1 beginning at 8:30AM. A one day registration for the ECTC conference will be required to attend the workshop.

The 54th ECTC will feature a Tuesday evening, June 1 Panel Discussion on "Low K Dielectric", and a Wednesday evening, June 2 Plenary Session focusing on "High-Density Substrate Technology."

An all-day educational seminar will be offered on Tuesday, June 1, 2004 consisting of 16 Professional Development Courses. Mr. Albert Puttlitz and the Professional Development Course committee have brought together industry experts from a wide variety of disciplines to offer state-of-the-art technology reviews and updates in condensed half-day and full-day formats. Course topics cover a wide range of technologies, including Nano - The Next Technology, Optoelectronics Components and Modules for Communication Networks, Integrated Passive Technology and Commercialization, Microelectronics and MEMS sensors. These courses are eligible for Continuing Education Unit (CEU) credits.

The Technology Corner on Wednesday afternoon, June 2 and Thursday, all-day June 3 will feature exhibits of the newest products and services available in an environment that enables



discussion and interaction with the managers, engineers, and scientists attending ECTC.

ECTC attendees can receive Conference Proceedings as a CD-ROM or a printed version. Both the CD-ROM copy and printed may be purchased for an additional \$50 charge.

The 54th ECTC Advance Program is available from this newsletter or from:

Jim Bruorton, ECTC Publicity Chairman
2004 Electronic Components & Technology Conference
c/o KEMET Electronics Corporation
P.O. Box 5928
Greenville, SC 29606
Telephone: (864) 963-6621
Fax: (864) 963-6444
Email: margieballinger@kemet.com

or you may visit the ECTC website at www.ectc.net and download the information and program from that location.

The 54th ECTC conference is sponsored by the Electronic Components, Assemblies, and Materials Association (the electronic components sector of the Electronic Industries Alliance) and the IEEE Components, Packaging and Manufacturing Technology Society.



In Praise of TC-materials:

"Sure, you can design the universe in 6 days, but it will take billions of years to develop the materials needed to build it to specification."



Announcement and Call for abstracts
The Seventh IEEE CPMT International Academic Conference on
Next Generation Microsystem Packaging Research and Education

Time: June 28-30, 2004

Venue: Jia Ding Campus, Shanghai University, Shanghai, China

Co-sponsored by

IEEE CPMT Society, USA

Shanghai Science and Technology Commission, Shanghai Government

Gothenburg City Government, Sweden

IEEE CPMT Scandinavian Chapter

IEEE CPMT China Chapter

SMIT Centre, Chalmers University of Technology, Sweden and Shanghai University, China

PURPOSE OF THE CONFERENCE

The purpose of the conference is to make the academic community aware of all the significant advances made worldwide in both next generation microsystem integration and packaging research and education. In addition one of the goals of this conference is to promote international collaborations in areas of mutual interest to serve the global technical community better.

SCOPE OF CONFERENCE

The 7th International Academic Conference will be organized by Sino-Swedish Microsystem Integration Technology (SMIT) Center, Shanghai and held between June 28-30, 2004 at Shanghai University. This conference will be held in an area (Shanghai) where there is a fast growth of microsystem manufacturing and packaging industry. This conference will help to line up the academic and industrial community in Asia as well as in the rest of the world and strengthen its collaboration with the counterparts in Europe and USA. It is essential to make microsystem integration and packaging research, education and training a global focal point. The 7th International Academic Conference will have the following sessions:

Research Sessions:

- Key note talks
- Invited talks
- Microsystem Packaging Research in the China and the rest of the world.
- MEMS integration and packaging technology
- Photonics integration and packaging
- Bio-chip integration and packaging
- Nanointegration and packaging

Education Sessions:

- Microelectronics integration and packaging graduate and undergraduate education programs and curricula
- Pre-college and vocational programs/novel internship program
- Workshop on web-based teaching

Training Sessions:

- Continuing professional development programs
- On-line tutorials and short courses
- Technical management in microsystem integration and packaging

SUBMISSION OF ABSTRACTS

You are welcome to submit an abstract for any one of the above sessions by March 30, 2004. The Abstract should cover the title, results and conclusions. Also necessary contact information about authors are expected. The program will be finalized by April 30, 2004.

OFFICIAL LANGUAGE:

English.

For further information please contact Professor Johan Liu at johan.liu@me.chalmers.se. or Dr Jiang Hua Zhang at jhzhang@mail.shu.edu.cn.

29th International Electronics Manufacturing Technology Symposium (IEMT)

to be held as the SEMI Technology Symposium at SEMICON West, July 14-16, 2004 -- San Jose, California

CALL FOR PARTICIPATION

Semiconductor Equipment and Materials International (SEMI), and IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society invite manufacturing professionals from around the world to participate in IEMT. For equipment and materials suppliers, and device manufacturers, IEMT provides unparalleled opportunities for both electronics and microelectronics professionals to network and learn the latest in manufacturing strategies and methodologies to achieve manufacturing excellence. Abstracts are peer-reviewed and are selected based on a clear outline of problem, analysis, solution/results and conclusion. Presentations will be in the following areas:

3D PACKAGING

TEST, ASSEMBLY AND PACKAGING ADVANCED MANUFACTURING PROCESSES

ADVANCED MATERIALS AND RELIABILITY

ENVIRONMENTALLY FRIENDLY MANUFACTURING (CFM):

Ultraclean technologies; Clean materials; Mini environments; Environmental factors; Carrier influence; Recyclability

COST REDUCTION:

Cost management; Cost of ownership; Benefit of ownership; Justification/ROI for capital expenditures; Supplier/Customer continuous improvement programs

TEST, ASSEMBLY AND PACKAGING FACTORY DYNAMICS:

Continuous improvement processes; Qualification strategies; Extending current capabilities; Manufacturing line performance; Methods to determine capacity components and magnitudes; Capacity detractors and analyses of causes for detractors and cycle time losses (tool, operator, WIP, etc); Cycle time and fabricator load/capacity relationships; Activities undertaken to reduce capacity detractors; Deployment and implementation of work method changes into manufacturing, EMS/IC assembly, Semiconductor assembly

WIRELESS AND OPTICAL NETWORK COMPONENT AND SYSTEMS MANUFACTURING TECHNOLOGY:

OE/EO components and assembly; RF, Planar and Other lightwave circuits manufacturing and packaging

ADVANCES IN WAFER LEVEL AND CHIP SCALE PACKAGING:

Wafer bumping; Photolithography challenges; Singulation; Wafer breaking/scoring; Overmolding; Redistribution; 300 mm manufacturing challenges; Wafer thinning; 3D assembly

TIME-TO-MARKET:

Design for manufacturability (DFM); Technology transfer; Quality functional deployment (QFD); Early manufacturing involvement; Theory of constraints (TOC)

YIELD ENHANCEMENT:

Wafer level/Board level inspection tools and techniques; Defect inspection methodologies; Wafer level reliability (WLR); Failure analysis; Yield modeling; Process defect reduction; Defect reduction in materials; Defect-to-yield correlations; Design for manufacturability; Product Yield Risk Assessment (PYRA); In-line inspection; Intelligent data analysis; Systematic yield problems

PRODUCT TEST AND TEST PROCESS OPTIMIZATION:

High speed testing; High bandwidth; Mechanical probing; SOC; SIP; Structural testing; Dynamic burn-in

OFFSHORE VS. ONSHORE MANUFACTURING:

Technology transfer and resources; Local content; Culture/Language barriers; Maintaining yield; Fabless and manufactureless

MEMS/MOEMS TECHNOLOGY:

Manufacturing techniques; Novel materials and problems unique to specific projects; Meaning of volume manufacturing to MEMS suppliers; Implications of using smaller wafers and older tools

PANEL DISCUSSIONS AND/OR WORKSHOPS

Online:

www.semi.org

or www.cpmt.org/iemt

13th Topical Meeting on Electrical Performance of Electronic Packaging

EPEP 2004

October 25-27, 2004
Portland, Oregon

Sponsors

The IEEE Components, Packaging and
Manufacturing Technology Society

IEEE Microwave
Theory and Techniques Society

Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

- Current and future issues related to on-chip interconnections
- Router friendly models and modeling tools: accuracy & efficiency
- Modeling and design of high speed digital IO circuits: signal propagation and reception
- On-chip power delivery and regulation
- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
- Power distribution and package resonance
- Long distance propagation in large switching complexes
- Switching noise in multi-layered systems
- Optoelectronic packaging; structure and system applications
- Electrical issues in MEMS packaging
- New and innovative interconnect packaging structures and their electrical performance
- RF/microwave packaging structures and their electrical performance
- MMIC modules and high density packaging
- Experimental characterization techniques
- EMC/EMI sources & effects
- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for one chip radios: design and modeling
- Performance of packaging for automotive radar systems

Conference Co-chairs: Tawfik Arabi, Intel Corp.; Robert W. Jackson, University of Massachusetts

Conference Web Page: Detailed and updated information can be found at <http://www.epep.org>

Paper Submission: Detailed information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 10, 2004**.

Student Paper Award: Two awards will be presented to the best two papers submitted by students

Short Courses/Workshops: On Sunday, October 24, 2004, a workshop entitled "Future Directions in Packaging" will be presented and short courses/tutorials will be offered.

**6th International Conference on Electronics Materials and Packaging
(EMAP 2004)
5-7 December 2004, Penang, Malaysia**

**FIRST ANNOUNCEMENT AND
CALL FOR PAPERS**



About EMAP

The 6th Electronics Material and Packaging Conference (EMAP 2004) is an international event organized by the School of Mechanical Engineering, Universiti Sains Malaysia, and IEEE CPMT Chapter with joint technical co-sponsorship from CPMT society of IEEE.

EMAP 2004 will feature short courses, technical sessions, and exhibition. It aims to provide good coverage of developments in all areas of electronics materials and packaging, from design to manufacturing and operation. EMAP 2004 is a major forum, providing opportunities to network and meet leading experts in addition to exchange of up to date knowledge in the field. Since 1999, EMAP has gained a reputation as a premier electronics materials and packaging conference in Asia Pacific where the bulk of the packaging activities are taking place.

Conference Topics

The topics of interests are specific to micro systems/MEMS, their packaging, electronics materials and reliability issues. Extended abstracts are being sought from, but not limited to, the following areas:

- **Automotive Electronics**
- **Chip-Scale Packaging/Flip Chip**
- **Electrical Modeling & Signal Integrity**
- **Green Materials**
- **High Density Displays**
- **High Density Packaging**
- **Interconnection Technologies**
- **Low Cost Packaging Methods**
- **Manufacturing Technologies**
- **Mechanical Modeling and Structural Integrity**
- **MEMS Packaging and Applications**
- **Microelectronic Materials & Processes**
- **No Flow Underfilling Process**
- **Optoelectronics/Photonics**
- **Polymer Materials & Microelectronic Applications**
- **Printed Wiring and Flex Boards**
- **Quality & Reliability**
- **Thermal Design, Analysis, and Characterization**

- **Electronic Inspection**
- **Thick & Thin Film Materials**
- **Wafer Scale Packaging**
- **Wireless Sensor Packaging & Applications**
- **Vibration on Electronic Devices**

Important Dates:

Submission of Abstract **31 May 2004**
Notification of Acceptance **15 July 2004**
Submission of Manuscript **31 August 2004**

Extended Abstract and Paper Submission

Extended abstracts are invited to describe original and unpublished work. The extended abstract should be about 500 words stating clearly the purpose, methodology, results, and conclusions of the work. Key references to prior publications and how the work enhances the existing knowledge should be included in the extended abstract. Authors are requested to designate appropriate areas for the purpose of abstract review. All submissions must be in English and should be made via electronic mail to abstract_emap2004@eng.usm.my. The required file format is either MS Word or Adobe Acrobat® PDF with only one single file for each submission.

The abstracts must be received by 31 May 2004. Authors are requested to include their affiliation, mailing address, telephone and fax numbers, and e-mail address. Authors will be notified of paper acceptance and instruction for preparing final papers by 15 July 2004. The final manuscript for publication in the conference proceedings is due by 31 August 2004.

Short Courses:

The conference program includes short courses, which will be conducted by leading experts in the field. Details will be provided in the conference website and available in subsequent mailings.

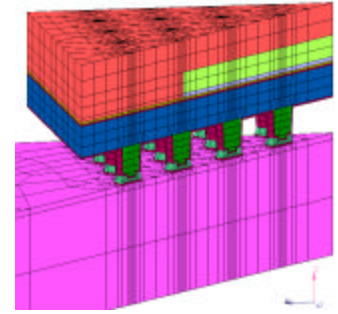
Exhibition:

A tabletop exhibition from suppliers of materials, equipment, components, software, and service providers of electronics industries will be held at the venue of the conference

Conference Information and Contacts:

Website: <http://www.eng.usm.my/mekanik/emap2004.html>

General Chair	Technical Program Chairs	
Dr. Zaidi Mohd Ripin mezaidi@eng.usm.my Tel: 60-4-593-7788 (ext: 6300) Fax: 60-4-594-1025	Prof. K. N. Seetharamu knramu@eng.usm.my Tel: 60-4-593-7788 (ext: 6309) Fax: 60-4-594-1025	Mr. Teck Joo Goh teck.joo.goh@intel.com Tel: 60-4-253-1236 Fax: 60-4-253-1028
Secretariat		
School of Mechanical Engineering, Engineering Campus, Universiti Sains Malaysia 14300 Nibong Tebal, Seberang Perai Selatan, Pulau Pinang jaa@eng.usm.my Tel: 60-4-593 7788 (ext. 6301) Fax: 60-4-594 1025		



Fifth conference on

Thermal & mechanical simulation and experiments in micro-electronics and micro-systems

May 9-12, 2004 in Brussels, Belgium

The Conference: May 10-12, Brussels, Belgium

EuroSimE 2004 will address the results of both fundamental research and industrial application for **thermal**, **mechanical** and **thermo-mechanical** solutions of (micro)-electronics, focusing on advanced **simulation** and **experiments**. A preliminary program will be available **by Jan. 15**. Brief overview of conference topics (oral and poster sessions):

- Trends in Microelectronics & Microsystems
- State of the Art in Thermal and Mechanical Simulations
- Reliability of (leadfree) Solder Interconnection
- Advanced Packaging and MEMS Designing
- Designing for Endurance and Reliability
- IC Process Reliability Modeling and Characterization
- MEMS, Sensors and Actuators
- Characterization and Modeling of Materials and Reliability
- Adhesives, Encapsulation, and Underfill
- Simulation and Optimization in Microelectronics
- New Techniques in Modeling and Characterization
- Dynamic Compact Thermal and Electro-Thermal Models
- Thermal Behavior Modeling and Characterization
- Small Scale Thermal and Fluid Aspects in Microsystems
- CFD and FE Modelling of Thermal Performance



Short courses: May 9, Leuven, Belgium

Up to **six** professional development **short courses** will be offered, taking place at IMEC-Leuven. Final course topics will be announced by Jan. 15. Following topics are planned:

- Wafer level packaging technologies
- Lead-free solder joint reliability
- Static and dynamic compact thermal models for the thermal analysis
- Heat sink design and analysis for microelectronic equipment
- Microvias and high density interconnects for advanced packaging
- Micromechanical Sensors



Other conference features

- On Monday evening, a conference dinner with surprise act is planned. Tuesday evening comprises a special Belgian beer tasting event.
- A parallel **exhibition** from industrial contributors and simulation and optimization software companies.

Registration / Preliminary program / Latest information

<http://www.eurosime.com/> Information local organiser: Bart.Vandeveld@imec.be ;
Marion.Hegemann@imec.be (tel.: +32 16 281 849)



Announcement and Call for Papers

The Sixth IEEE CPMT Symposium on High Density Microsystem Design and Packaging and Component Failure Analysis (HDP'04)

Date: June 30 – July 3, 2004

Venue: Bao Long Hotel, No 180, Ye Xian Road

Co-sponsored by

Shanghai Science and Technology Commission, Shanghai Government

IEEE CPMT Society, USA

DaimlerChrysler SIM TECH, Shanghai, China.

Chalmers University of Technology, Sweden

IVF Industrial Research and Development Corporation, Sweden

IEEE CPMT Scandinavian Chapter

IEEE CPMT China Chapter

Shanghai Institute of Microsystems and Information Technology, China

Jiaotong University, China

SMIT Centre, Shanghai University, China

Microsystem manufacturing, assembly and packaging technology is playing a key technology for the progress of the microsystems and microelectronics industry in the world. China is not an exception. Therefore, many multi-national companies are establishing new facilities in China for expanding their global business and interest. Following the successful previous conferences, we are proud to announce the sixth International IEEE CPMT Symposium on High Density Microsystem Design and Packaging and Component Failure Analysis in Electronics Manufacturing (HDP'04).

Scope for the Symposium: The Symposium will cover the following areas and subjects:

- High density design and packaging including micro- and nanosystems, microelectronics and opto-electronics design and packaging, CSP, BGA, Flip-chip, Chip on Board, Surface Mount Technology and other novel emerging technology
- High density substrate including integrated passives and active devices
- MEMS and MOEMS design, packaging and assembly
- Microsystems manufacturing issues including cleaning issues, quality control, logistics, repair, process optimization, statistic process controls, ISO compliance, tooling or equipment, early manufacturing involvement initiatives and yield and test innovations used to enhance manufacturing processes or products related to high density substrates, single chip and multichip packaging, chip bumping and integrated component technologies
- Component failure analysis techniques including non-destructive X-ray, ultrasonic microscopy, IR-microscopy etc
- Simulation and modelling for packaging and microsystems and microelectronics manufacturing processes
- Thermal management
- Environmental design and materials development including life cycle analysis and end of life strategy etc
- Cost reengineering, improvements and analysis for electronics packaging processes and products

Documentation: The documentation from the Symposium will be published in a proceeding with CD ROM with a full length papers (max 12 A4 pages) in English.

Journal publication: In addition, high quality papers will be selected for consideration to be published as special editions of the IEEE CPMT Transactions.

Languages: English will be used.

You are welcome to submit an abstract with max 300 words that cover the topic, experimental approach, results and conclusions for the paper by March 30, 2004 Notification of abstracts will be made by April 15, 2004, Final paper is requested by April 30, 2004.

We are also interested to have exhibitors from materials, equipment suppliers to exhibit their products. If you are interested in exhibition.

For further information please contact Professor Johan Liu at johan.liu@me.chalmers.se or Dr Jiang Hua Zhang at jhzhang@mail.shu.edu.cn.

ITherm
Mirage Hotel & Casino
Las Vegas Nevada
June 1 - June 4, 2004

ITherm is an international conference to disseminate research and development related to thermal management, mechanical, thermomechanical and materials aspects associated with electronic and photonic components and systems in the existing and emerging technologies such as micro- and nanotechnologies, MEMs, bio-chips, 3D interconnects, cell phones, pagers, lap-top computers to supercomputers, in consumer, automotive, satellite-based and military electronics. ITherm brings together engineers and scientists from industry, academia, and government research organizations from all over the globe.

ITherm 2004 will run concurrent with the Electronic Components and Technology Conference (ECTC) (ECTC), which offers a broad range of current and new developments in all areas of electronic. In addition to the technical paper presentations, ITherm includes: vendor exhibits, keynote lectures by international experts, panels on topics of current and future interest to ITherm community, and professional short courses.

ITherm 2004 can be contacted through the University of Arizona.

University of Arizona
Engineering Professional
Development
1224 N. Vine Avenue
Tucson, AZ 85719-4552
Phone: 520-621-3054
FAX: 520-621-1443
contact@ITherm.org

ITherm Technical Courses

Three upcoming technical courses of possible interest to ITherm attendees.

1) Polymeric Materials and Their Characterization by Thermal Analysis
Techniques
www.mse.arizona.edu/shortcourse/MSEUAshortcourse.pdf

2) Die and Packaging-Level Microelectronics Assembly
www.dpla.org

3) Area Array Technology
www.area-array-technology.org

please visit <https://www.itherm.org>

Organizers:



Hungarian &
Romanian Joint
Chapter

Sponsors:



Ministry of Education
Research and Youth



ARIES

Romanian Association
for Electronic and
Software Industry



Romania Section



Association for
Promoting
Electronic Technology

The 10th International Symposium for Design and Technology of Electronic Packages

Bucharest, Romania, September 23-26, 2004

You are cordially invited to submit papers to the **International Symposium for Design and Technology of Electronic Packages** (SIITME). The conference is a high scientific event focused on **electronic packaging**, an annual event in Central and Eastern Europe since 1995. In September 23-26, 2004 we will celebrate the **10th jubilee edition** at the University Politehnica of Bucharest, Romania, in conjunction with BINARY 2004, the **7th Romanian Electronic and Software Fair**, September 24-26, organized by ARIES at the Conference Center ROMEXPO, Bucharest, Romania.

The conference is dedicated to debating the role of Universities as Research and Development Centers in today's Industrial and Economical Environment. The conference continues on meeting tradition of specialists in the electronics technology field and it is focused on dissemination of information and scientific results relating to education, research development and manufacturing of electronic packages in the following topics:

- CAE - CAD - CAM for electronic packages and modules; modeling and simulation;
- electromagnetic compatibility and signal integrity analysis; electrostatic discharge;
- printing wiring board - new materials, processing, process simulation and application;
- thermal management, reliability and life time prediction;
- quality management: Q- assurance, Q- control, Q- inspection;
- concurrent engineering and project management on electronic packages;
- electronic components and packaging (SMD, BGA, CSP, FC);
- electronic and optoelectronic modules manufacturing (SMT/PCB/ MCM);
- reliability of new packaging concepts interconnection technology;
- design for environment and environmentally conscious manufacturing;
- clean technologies;
- technology and testing of electronics equipments;
- optical investigation in circuit-test systems;
- fault tolerant digital design;

The conference will include regular technical sessions, plenary sessions and tutorials. Regular sessions will include poster and oral sessions. Prospective authors are invited to submit their manuscripts reporting work, as well as proposals for special sessions, tutorials and areas presented above. The abstract shall be half page of text (200 - 250 words), using no smaller than 12-point type font. They will receive manuscript format and layout instructions for paper submission. Please use E-mail to siitme2004@cetti.ro for any correspondence, submission of abstract and paper.

Planned joint Events:

- IEEE - CPMT Hungary - Romanian Joint Chapter Meeting
- IEEE- CPMT Student Branch Meeting

Organized by:

- **Hungarian & Romanian Joint Chapter**
- Politehnica" University of Bucharest
- Center of Technological Electronics and Interconnection Techniques
- IEEE-CPMT Student Branch Chapter of "Politehnica" University of Bucharest

Chairman: Prof. Paul Mugur Svasta , Ph.D, UPB-CETTI, Romania

Important dates:

Submission of Abstracts **May 7, 2004**
Notification of Acceptance **June 1, 2004**
Submission of Manuscripts **September 3 , 2004**

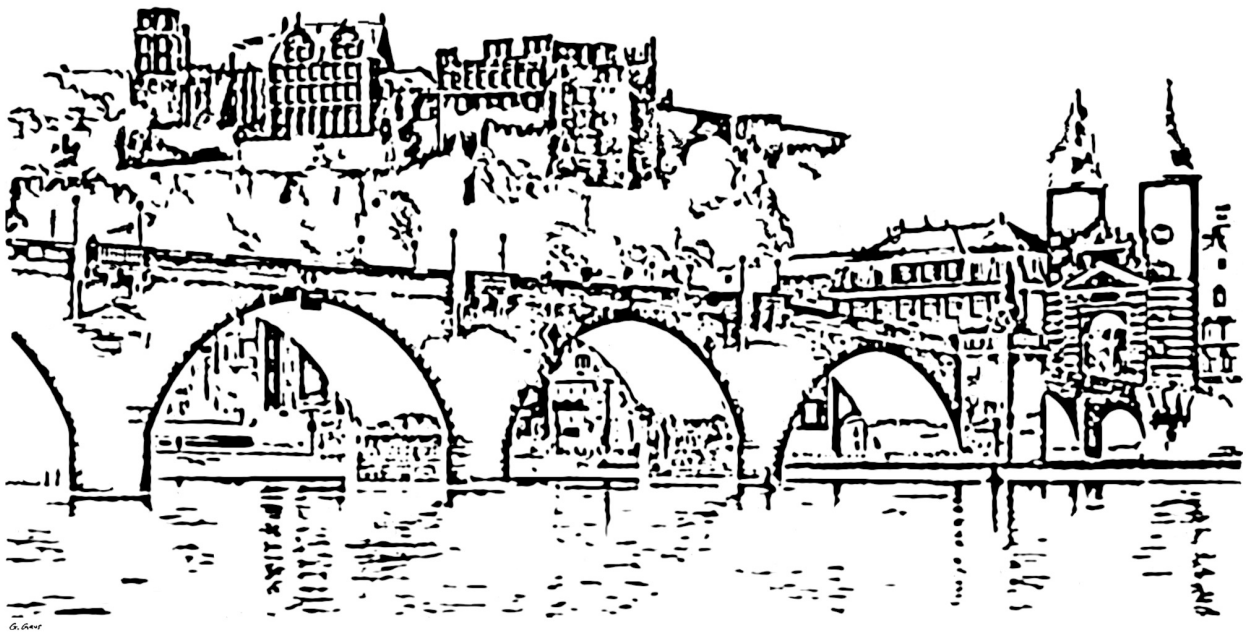
Organizing Secretariat SIITME 2004:

Splaiul Independentei, nr 313, Sector 6, 060032, Bucuresti, ROMANIA
Phone: +40-21-4116674
Fax: +40-21-4115182
E-mail: siitme@siitme.ro

Web site: www.siitme.ro



CALL FOR PARTICIPATION



8th IEEE WORKSHOP ON

SIGNAL PROPAGATION ON INTERCONNECTS

Sponsored by the IEEE Computer Society – Test Technology Technical Council (TTTC)
and by the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society
May 09-12, 2004 · “Hotel Crowne Plaza” · Heidelberg, Germany

During the last seven years, the IEEE Workshop on Signal Propagation on Interconnects has been developed into a forum of exchange on the latest research results in this area. The aim of this ensuing workshop is to report on the most recent developments in the field of interconnect modeling, simulation and measurement on chips, boards, and packages. The event is also meant to bring together developers and researchers from industry and academia in order to encourage cooperation. In view of the last years' success, the committee is looking forward to the 8th IEEE Workshop on Signal Propagation on Interconnects where world class developers and researchers will share and discuss leading edge results in the famous and beautiful historic city of Heidelberg, Germany. The social events bundle takes care you'll never forget where you learned the latest and hottest news about interconnects and testing: we are going to have a guided tour through old Heidelberg and even have dinner in the famous castle.

The workshop will be held in English. Detailed information about the workshop and its location are available on the website <http://www.spi.uni-hannover.de>. We are all looking forward to see you in Heidelberg.

Main topics of the workshop will include, but are not limited to:

- Frequency Domain Measurement Techniques
- Time Domain Measurement Techniques
- Modeling Techniques of Package & On-Chip Interconnects
- Macro-Modeling
- Simulation Techniques for Interconnect Structures
- Electromagnetic Field Theory
- Analysis and Modeling of Power Distribution Networks
- Propagation Characteristics on Transmission Lines
- Coupling Effects on Interconnects
- Substrate Effects
- Guided Waves on Interconnects
- Radiation & Interference
- Electromagnetic Compatibility
- Power/Ground-Noise
- Testing & Interconnects
- Optical Interconnects

Workshop Standing Committee:

Flavio G. Canavero, Politecnico di Torino, Dipartimento di Elettronica, Torino (I); canavero@polito.it

Hartmut Grabinski, Univ. Hannover, Laboratorium für Informationstechnologie, Hannover (D); grabinski@lfi.uni-hannover.de

Michel S. Nakhla, Carleton University, Department of Electronics, Ottawa (CAN); msn@doe.carleton.ca

Jose E. Schutt-Ainé, Univ. of Illinois at Urbana-Champaign, Center for Comp. Elm., Urbana (USA); jose@decwa.ece.uiuc.edu

Madhavan Swaminathan, Georgia Institute of Technology, Atlanta (USA); madhavan.swaminathan@ece.gatech.edu

Chair: Hartmut Grabinski, Laboratorium für Informationstechnologie, Schneiderberg 32, 30167 Hannover (Germany) - Phone +49-511-762-5030; Fax +49-511-762-5051; grabinski@lfi.uni-hannover.de

Program-Chair: Uwe Arz, Physikalisch-Technische Bundesanstalt, High-Frequency Measurement Group (2.22), Bundesallee 100, 38116 Braunschweig (Germany) - Phone +49-531-592-2297; Fax +49-531-592-2228; uwe.arz@ptb.de

Future Directions in IC and Package Design Workshop, FDIP'04

sponsored by:



organized by:

CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

October 24, 2004

Portland, Oregon

The goal of this workshop is to provide a forum to address the future needs associated with the design of next generation ICs and packages. The Technical Program Committee will solicit invited presentations from experts in the university and industrial communities. The workshop will be held in conjunction with the **IEEE Topical Meeting on Electrical Performance of Electronic Packaging** in order to enhance this conference with presentations that give directions for future requirements and developments in the area of electrical analysis and design. The workshop will foster active participation and discussions from all the speakers and attendees during the meeting.

The following talks are planned:

- *Gigascale Integration – Design Challenges and Opportunities, Shekhar Borkar, Intel Corporation*
- *Emerging Trends in High-Speed Interconnects and Packaging Engineering, Sergio Camerlo, Cisco Systems*
- *Analog RF CMOS and Optical Design Techniques for 10+ Gbps Datacom, Martin Schmatz, IBM Corporation*
- *Power Distribution: Status and Challenges, Madhavan Swaminathan, Georgia Institute of Technology*
- *Signal Integrity Modeling and Simulation for IC/Package Co-Design, Ching-Chao Huang, Optimal Corporation*
- *Current and Future Directions in Simulator Development, Sani Nassif and Jaijeet Roychowdhury from IBM Corporation and University of Minnesota*

Workshop Chairs:

Alina Deutsch
IBM Watson Research Center

Madhavan Swaminathan
Georgia Institute of Technology

Technical Program Committee:

Tawfik Arabi – Intel Oregon
Andreas Cangellaris - University of Illinois
Moises Cases - IBM Austin
Chi-Shih Chang – Consultant
Paul Franzone - North Carolina State University
Hartmut Grabinski - University of Hanover, Germany
Harold Hosack - Semiconductor Res. Corp.
Lewis Terman – IBM Watson Research

Mahadevan Iyer - IME, Singapore
George Katopis - IBM Poughkeepsie
Istvan Novak - SUN
Toshio Sudo - Toshiba, Japan
Gregory Taylor - Intel Oregon
John Prince – University of Arizona
Ryszard Vogel - Nokia, Finland

Workshop will be held at the Hilton Portland and Executive Tower, 921 SW Sixth Ave., Portland, OR 97204, 503-226-1611. The hotel is holding a block of rooms at \$99.00 (no tax). Reservations must be made by September 30, 2004 in order to guarantee this rate. Be sure to mention that you are attending the EPEP conference in order to secure this rate. For more information on the hotel go to <http://www.portland.hilton.com>

Additional information may be obtained from the workshop chairs:

Alina Deutsch
deutsch@ieee.org
phone: (914) 945-2858, fax: (914)945-2141

Madhavan Swaminathan
madhavan.swaminathan@ece.gatech.edu
phone: (404) 894-3340

Attendees interested in the workshop will be charged a \$60.00 fee that will cover afternoon refreshments, digest of abstracts, and posting of the foils on the CPMT Society TC-EDMS web site. All attendees must register by September 13, 2004 using the EPEP'04 website at www.epep.org in order to assure that the workshop is being held. On-site registrants will be admitted depending on availability of seating.

Call for Papers

ISQED 2004 5th International Symposium on QUALITY ELECTRONIC DESIGN

March 22-24, 2004
San Jose, CA, USA



2004

www.isqed.org

In Technical Sponsorship of:
IEEE EDS, IEEE CPMT, and in cooperation
with ACM/sigDA, IEEE CASS, and FSA

ISQED is the leading international conference dealing with the design for manufacturability and quality issues front-to-back. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting near 100 technical presentations, six keynote speakers, two-three panel discussions, workshops /tutorials and other informal meetings. Conference proceedings are published by IEEE Computer Society and made available in the digital library. Proceedings CD ROMs are published by ACM.

Papers are requested in the following areas

- ❖ Design for Manufacturability & Quality
- ❖ Package - Design Interaction & Co-Design
- ❖ Design Verification and Design for Testability
- ❖ Embedded Test Methodologies
- ❖ Robust Device, Interconnect, and Circuits
- ❖ EDA Tools & IP Blocks; Interoperability and Implications
- ❖ Physical Design, Methodologies & Tools
- ❖ Effect of Technology on IC Design, Performance, Reliability & Yield
- ❖ Design Quality Definitions, Metrics, and Standards
- ❖ Quality Driven Design Flows; SoC, ASIC, FPGA, RF, Memory, etc.
- ❖ Quality of Modeling Abstractions and Methods (Device, Interconnect, Micro and Macro Cells, IP Blocks, ...)
- ❖ Redundancy & Self Correction Design Techniques
- ❖ Management of Design Process, and Design Database
- ❖ Global, Social, and Economic Implications of Design Quality
- ❖ Quality based EDA Tools, Design Techniques, and Methodologies, dealing with issues such as:
 - Timing Closure*
 - R, L, C Extraction*
 - Ground/Vdd Bounce*
 - Signal Noise/Cross-Talk /Substrate Noise*
 - Voltage Drop, Power Rail Integrity*
 - Metal Migration, Hot Carriers*
 - High Frequency Effects*
 - Thermal Effects*
 - Power Estimation*
 - Plasma Induced Damage, and other yield limiting effects*
 - EMI/EMC*
 - Proximity Correction & Phase Shift Methods*
 - Verification (Layout, Circuit, Function, etc.)*
 - EOS/ESD*
 - Packaging Modeling and Simulations*

IMPORTANT DATES:

Paper Submission Deadline	October 24, 2003
Acceptance Notification	November 17-19, 2003
Final Camera-Ready Paper	December 15, 2003

Submission Process

The guidelines for the final paper format is provided on the conference web site at www.isqed.org. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 6 pages). To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. Submit your papers using the **on-line** paper submission procedure available in the ISQED web site. Please check the as-printed appearance of your paper before submitting the paper. In case of any problems email the following 3 files to publication@isqed.org; i) The Full-length Manuscript in PDF ii) A 200 Words Abstract and iii) A Cover Letter (not need if submitting on-line). Address all other inquiries to publication@isqed.org.

About ISQED

The International Symposium on Quality Electronic Design (ISQED), is a premier Design & Design Automation conference, aimed at bridging the gap between and integration of, electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading conference dealing with design for manufacturability and quality issues front-to-back. The conference provides a forum to present and exchange ideas and to promote the research, development, and application of design techniques & methods, design processes, and EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. The conference attendees are primarily designers of the VLSI circuits & systems (IP & SoC), those involved in the research, development, and application of EDA/CAD Tools & design flows, process/device technologists, and semiconductor manufacturing specialists including equipment vendors. ISQED emphasizes a holistic approach toward design quality and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities.



Call for Papers



The 7th VLSI PACKAGING WORKSHOP of JAPAN

Nov. 30 - Dec. 2, 2004

Kyoto, Japan

Sponsored by the IEEE CPMT Society and National Institute for Standards and Technology

The VLSI Packaging Workshop of Japan has been held every other year since 1992 in the best season of Kyoto, the ancient capital of Japan, and it has become a well-known international workshop for advanced packaging technologies. The committee strongly encourages you to attend this workshop and participate in the discussion, in order to understand technology trends and find the proper target for technology development. Bring your latest research results and share with the participants who are experts from industry and the grove of Academe, and discuss with them. Anybody contributing to human progress through electronics is very welcome at this workshop. The following areas of technology are primarily of interest to the participants:

- + Advanced Fine Pitch Packaging
- + 3D Packaging & COC (Chip on Chip)
- + Micro Bumping Technology
- + Laminated Materials & Processing
- + RF Components & Modules
- + Integrated Passives
- + Packaging for Optoelectronics
- + Failure Mechanisms & Reliability Improvement
- + Electrical Performance & Thermal Management
- + Wafer Level CSP
- + Manufacturing Technology
- + Pb Free Interconnections
- + Materials for High Speed Application & Wafer Process
- + RFID tags
- + System in Package (SIP)
- + MEMS Packaging Technologies
- + Assembly and Packaging Challenges for Cu/Low-k Chips
- + Wafer Level Burn-in

The official language of this workshop is English. 30 minutes is allocated for each presentation, and it should include 5 - 10 minutes for Q&A. Authors who give outstanding papers will receive official recommendations for paper submission to the IEEE Transactions by the Japan Chapter and the Workshop Committee. This workshop will be held at Kyoto Research Park where the 6th Workshop was held in 2002.

Submission of abstracts:

Those who wish to contribute to the workshop should send a two-page summary of their paper (including figures) to the Program Chair **by May 28th, 2004**. The title of the paper as well as the names and affiliations of all authors must appear on the summary. If the paper is accepted, the summary shall be written to fit in a four-page format for the workshop's Proceedings **by September 3rd, 2004**. Notification of acceptance will be given **by July 9th, 2004**.

Program Chair:

Michitaka Kimura, Renesas Technology Corp.
4-1, Mizuhara, Itami-shi, Hyogo, 664-0005, Japan
Email: kimura.michitaka@renesas.com
Tel: +81-72-784-7127, Fax: +81-72-780-2676

General Chair:

Masahiko Kohno, Dow Chemical Japan Limited
Email: mkohno@dow.com

Vice Chair:

Tomoshi Ohde, Sony Computer Entertainment Inc.
George Harman, NIST

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Noboru Iwasaki, NTT
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Harufumi Kobayashi, Oki
Kaoru Kobayashi, Kyocera SLC Tech.
Hiroshi Manita, Casio
Tadaaki Mimura, Matsushita Electronics
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Atsushi Nakamura, Renesas Tech.
Atsushi Okuno, Japan Rec
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