Components, Packaging, and Manufacturing Technology Society Newsletter

The Global Society for Microelectronics Systems Packaging

Vol. 27, No. 3, September 2004 (ISSN 1077-2999)

www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

PRESIDENT'S REPORT

The times they are a changin'

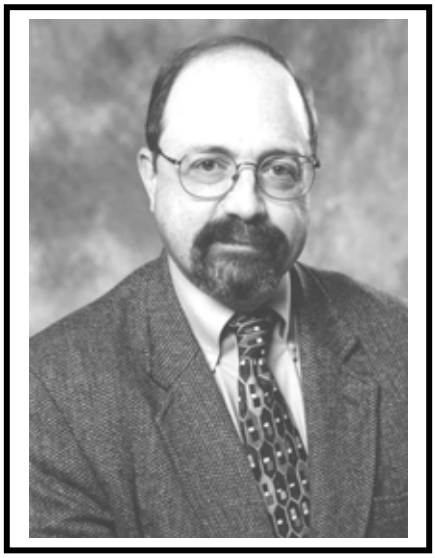
Having grown up in New York City in the early 60's, I can recall sitting in the coffee houses in Greenwich Village, sipping espresso and listening to the music of Bob Dylan. His catchy 1964 tune, "The Times They are A-Changin, "ends with the lines:

"…The order is
Rapidly fadin'.
And the first one now
Will later be last
For the times they are a-changin'."

Although those words were written to foretell the coming political and social turbulence of that era, they can be used as well today to express the turbulence in our microelectronics industry. We have all seen the massive layoffs and personnel cuts at the giants like IBM and Motorola in recent years and we have seen the startup foundries in Taiwan, Korea and now China taking over world chip production. Although we usually see these things from afar and have expressed concern for those affected, more and more of us continue to become affected.

In the last few months, Dow, my employer of 29 years, has undergone a massive top down restructuring which has recently resulted in the elimination of my job. I knew it was coming and in fact predicted it to my co-workers. When all is said and done, the reality of this "new world" in which we are living is that loyalty is between individuals, not the corporation and the individual, and that leaves us all vulnerable to the decisions of whoever is in charge. So… now everyone has to stop calling me Dr. BCB as I begin a new, as of yet undefined, career path.

With that said, how can we ameliorate the effects of such workplace actions? Well one way is through our professional affiliations. Your membership in IEEE CPMT offers you access to the latest information available in your field and we all know how valuable that is in the information age. Keeping yourself current is one of the best things you can do to ensure your value in the marketplace. Attending local and national meetings is also important because it allows you to network with other professionals on whom you may some day depend to help you find another job. As in all things in your lives, you need to be proactive and not wait until something bad happens. Think of your IEEE CPMT membership as a preemptive action -- as an insurance policy to ensure a rewarding professional career is always available to you. By the time you read this your IEEE membership renewal will be on its way to you. I hope you all will make the decision to continue your membership.



…Election time

This newsletter will also arrive during a period of elections in the USA. The decisions made by the US voters every four years have an impact on everyone else in the world. It is also election time in IEEE and your CPMT Society. We hope you will take the time to vote in these elections since they will choose the leaders who will make the policy for these organizations that will affect you .

As I mentioned in the last newsletter (V.27 #2), I proposed and the Board of Governors passed, a resolution to change the CPMT bylaws to require voting by region for local representatives. Thus, once the bylaws are rewritten and enacted (2005 elections) we will all be voting for only our local representatives apportioned by the regional percentage of the total membership population. So, North American members will be electing only our North American representatives and the same will be true for Europe and Asia. We think these are positive changes that will allow CPMT management to better reflect the desires of our broad global membership. We hope you agree.

(continued on page 3)

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Next News Deadline: December 5, 2004

Members-only Web:

UserName: cpmt (don't tell non-members)
Password: topdog (for 4th quarter)

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*****IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. $1.00 per member per year (included in Society fee) for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. For circulation information call IEEE customer Service 908 981 1393, or FAX 9667.

(continued from page 1)

….global management team

One more comment on the globalization process. As you know by now, my management team includes Rolf Aschenbrenner of Germany as Technical VP and Ricky Lee of Hong Kong as VP of Conferences. There were those who questioned whether the organization could operate if it were spread out all over the globe. In fact, there have been no problems whatsoever, most assuredly, due to the fact that computers and the internet have allowed us to communicate smoothly. They have both been a pleasure to work with and I thank them for their hard work and service to the organization, and for supporting CPMT Society activities.

IEMT Symposium Success at Semicon West

The 29th International Electronics Manufacturing Technology (IEMT) Symposium was held in San Jose, CA, in July 14-16, 2004, during Semicon West week. Co-sponsored by IEEE, the Components, Packaging and Manufacturing Technology (CPMT) Society, and SEMI, the Symposium provided an important venue for significant work in various areas of electronics manufacturing technologies.

Topics covered this year included: how to meet process challenges for the 90 nm node, latest trends in final manufacturing, latest development in advanced packaging, materials, design for test, and reliability.

This year's IEMT has grown significantly, marking a couple of firsts with six new Professional Development Courses (PDCs) and a Technology Workshop entitled, "Future Trends in Semiconductor Packaging," sponsored by Henkel Loctite. There were 69 papers distributed among eleven technical sessions and one dedicated poster session.

Walt Trybula, from International Sematech, presented the keynote address on "Macro, Micro, Nano, and Beyond." There were a total of 166 attendees, with close to 75 % of the registrants from the US, 15% from Asia and the remaining 10% from Europe.

Close to 100 registrants attended the six PDCs covering "Flip Chip", "Advanced Packaging", "Materials, Processes and Defects", "Failure Mode Analysis", "Nanotechnology", and "Lead-Free Soldering". There were over 120 attendees at the Henkel Technology Workshop, which covered the latest development in areas of Low-k Devices and Cu Interconnect, Lead-free Material Sets, Green Packages, 3D Architectures for Packaging, Thermal Management, and, High Speed Dispensing.

Hosting the IEMT in conjunction with Semicon West also provided plenty of opportunities for networking in a large trade show environment. Next year, along with Semicon West, IEMT will move to the Moscone Center in San Francisco, CA. A Call For Papers will be issued in the near future. Keep those papers coming! For the Call for Papers, see www.cpmt.org/iemt/

--submitted by Luu Nguyen, National Semiconductor Corporation

CPMT Manufacturing Technology Award

The IEEE CPMT Manufacturing Technology Award was presented to Michael Varnau of Delphi for his flip chip developmental work. Mike is a technical fellow at Delphi in Kokomo, Indiana. The award was presented by CPMT Board of Governors members Dr. William Chen of ASE and Jan Vardaman of TechSearch International during the IEEE CPMT Symposium held in conjunction with SEMI during SEMICON West in July.

New Senior Members in Our Society

Mostafa N. Abdulla -- Sacramento Valley
Rolf Aschenbrenner -- Germany
Torsten Wipiejewski -- Hong Kong
Benjamin P. Yen -- Hong Kong
Ming-Cheng Cheng -- Mohawk Valley
Petri J. Savonlainen -- Finland
Mahesh G. Varadarajan -- Bangalore
Wing Yiu Cheung -- Hong Kong

"… a candidate shall be an engineer, scientist, educator, technical executive or originator in IEEE-designated fields. The candidate shall have been in professional practice for at least ten years and shall have shown significant performance over a period of at least five of those years."

Less than 10% of CPMT Society members have applied for the senior member status even though about 50% meet the requirements. See the following website for your path to this deserved honor.
http://www.ieee.org/organizations/rab/md/smprogram.html

Mark Your Calendar!
Saturday, 22 January 2005
San Diego, California
"Packaging of Biomedical Electronics Devices" Seminar

** Miniaturization
** Low Power Design
** Implantable Materials
** Reliability and Testing

See http://www.cpmt.org/docs/sd-bio.html

IEEE-CPMT Society Awards for Year 2005

(Nomination Due Date: January 31, 2005)

Your CPMT Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society.

David Feldman Outstanding Contribution Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
Prize: $2,500 and Certificate.
Basis for Judging: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.
Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2004.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate.
Basis for Judging: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably 10 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).
Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2004.

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate.
Basis for Judging*:* Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.
Eligibility*:* No need to be a member of IEEE and CPMT Society.

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
Prize: $2,500 and a Certificate.
Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.
Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2004. There are no requirements for service to the IEEE or CPMT Society.

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.
Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.
Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.
Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2004, and must be 35 years of age, or younger, on December 31, 2004.

Guidelines for Nominators:

Ø Past recipients of an award are not eligible to receive that same award. For list of past awardees, see the CPMT Society Home page (http://www.cpmt.org/awards/).
Ø An individual may submit only one nomination per award but may submit nominations for more than one award.
Ø It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
Ø Please send nominations to CPMT Society Awards Committee Chair by e-mail, fax or mail:

Rao Bonda, Ph.D.
Freescale Semiconductor, Inc.
2100 East Elliot Road,
Mail Drop: EL725
Tempe, AZ 85284, USA

Phone: +1-480-413-6121
Fax: +1-480-413-4511

Email address: r.bonda@ieee.org or rao.bonda@freescale.com

Winners will be notified by 28 February 2005, and the awards will be presented at the 55th Electronic Components and Technology Conference, May 31- June 3, 2005, in Orlando, Florida, USA.

IEEE CPMT Society & the Scouting Movement:

Working together to attract Students to IEEE and the Engineering Profession IEEE CPMT Society Volunteers and Staff assembled a Peer Review Team, lending their time and expertise to help the Boy Scouts of America (BSA) update their Electricity Merit Badge Pamphlet which had not been revised since 1996. Specifically, the team reviewed the electrical history, safety, terminology, and electrical experiments outlined in the pamphlet. Significant suggestions for improvement, corrections and updates were made. The listing of IEEE and the IEEE Virtual Museum were also added to the pamphlet as additional resources.

Ralph W. Russell II, of Richmond, Virginia., USA-based company Dominion, organized the peer review. Within the IEEE, Russell wears many hats. He is a member of the Educational Activities Board Pre-College Education Coordinating Committee, IEEE Technical Activities Board Components, Packaging, and Manufacturing Technology (CPMT) Society Board of Governors, IEEE-USA Energy Policy Committee, and Project Manager of the IEEE Regional Activities Board 2005 National Scout Jamboree Electronics Merit Badge Project to be held at Fort A. P. Hill, Va. in Caroline County, Va, USA. Russell is also a former Scoutmaster and six-time U.S. National Scout Jamboree staff member.

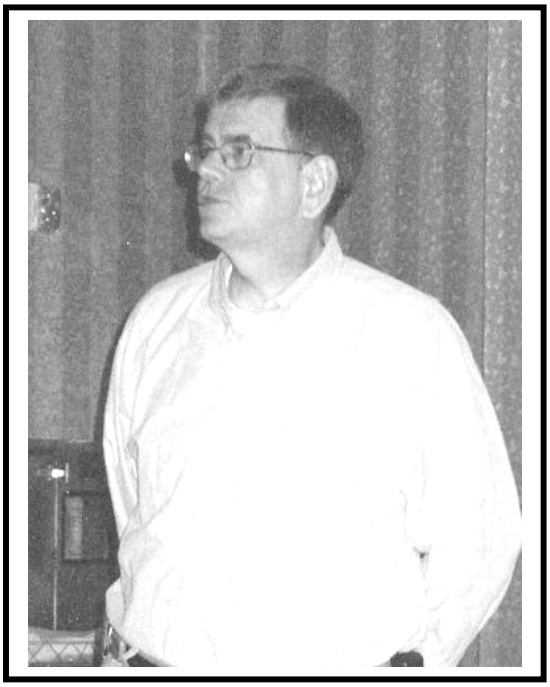
Members of the peer review committee include: Al Mouton, Cedar Creek, Texas, president of AGM Systems and Scouter; Lee Reed Sr., Richmond, Va., senior safety specialist for Dominion Resources Services; Rick Tavan, Truckee, Calif., retired Executive VP, Engineering and Operations at TIBCO, Electricity merit badge counselor, and father of two Eagle Scouts; Dan Ward, Richmond, Va., principal engineer for Dominion Virginia Power; Paul Wesling, Saratoga, Calif., vice president of publications for IEEE's CPMT Society, Eagle Scout, 15-year Scoutmaster, Venture Crew leader, BSA Heroism and Silver Beaver awards; Michael N. Geselowitz, Ph.D., director of the IEEE History Center and father of a Cub Scout. Dr. Geselowitz has also served as a Cubmaster, Den Leader, Pack Committee Member, Troop Committee Member and a Member of his Council's Jewish Committee on Scouting.

The EAB Pre-College Education Coordinating Committee became involved in the review process as a result of a formal partnership proposal submitted to the BSA this past April. The Electricity Merit Badge pamphlet review is the first BSA activity completed by the EAB committee. The IEEE TAB CPMT Society conducted the peer review process. When asked if this is an activity the group would engage in again, Russell said, "Yes. We were recently asked to do a peer review of the Computer Merit Badge as well." Discussions regarding the partnership between IEEE and the BSA will continue as it is still to be finalized. The IEEE also plans to work with the global World Organization of the Scout Movement and The World Association of Girl Guides and Girl Scouts to form partnerships.

Though this is a new activity for the EAB committee, IEEE RAB has been supporting the BSA National Scout Jamboree by coordinating the Electricity and/or Electronics Merit Badge Booths at the BSA Jamboree since 1981. The National Scout Jamborees are held every four years, and are usually attended by over 35,000 scouts and 5,000 adult leaders from the U.S. and the rest of the world. IEEE funding and volunteers were provided at the Jamborees held in 1981, 1985, 1989, 1993, 1997, and 2001. At the June IEEE Board Series, RAB approved $50,000 in funding for the local geographic area to support the IEEE Electronics Merit Badge booth at the 2005 U.S. National Scout Jamboree.

Coordination of the Electronics Merit Badge Booth primarily comes from the IEEE Richmond, Virginia, USA, Section of Region 3, the Southeast part of the US. Region 3 has been a supporter of the project since 1981. Activities of the Region 3 volunteers include implementation of a web site to promote the electrical and electronics engineering profession to students, the development of instructional electrical and electronic programs and an electronics kit. A new website, www.emeritbadges.org is currently under development.

Submitted By:
Ralph W. Russell, II
Project Manager
IEEE "emeritbadges.org" Project
emeritbadges@ieee.org



CALL FOR NOMINATIONS 2006 IEEE COMPONENTS, PACKAGING & MANUFACTURING TECHNOLOGY AWARD

IEEE Components, Packaging & Manufacturing Technology Award is presented for meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The Award is sponsored by the CPMT Society. The recipient of the award receives a bronze medal, certificate, and cash honorarium.

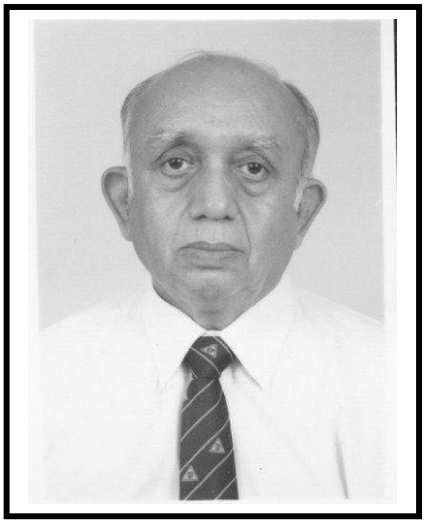
The nomination deadline is 31 January 2005. For nomination forms, visit the IEEE Awards Web Site, www.ieee.org/awards, or contact IEEE Awards Activities, 445 Hoes Lane, Piscataway, NJ, USA, 08855-1331; tel: +1 732 562 3844;
email: awards@ieee.org.

--submitted by Kerry Ann Ward, IEEE

CHAPTER NEWS

REGION 10 CHAPTER ACTIVITY ROUND-UP.

by **Dr. P.B. Parikh**·



Hong Kong

Dr. Cheung Yiu-Ming, Ken Chairman of CPMT Hong Kong chapter has reported that the technical workshop (reported in our earlier issue) by Dr. Michael Pecht on "Monitoring the Health (Reliability) of Products" held on 9th June was very successful. The CPMT Hong Kong chapter has subsequently arranged four more technical events during the quarter as follows:

Ø "Trends in High Density Packaging and Portable Microelectronics" by E. Jan Vardaman (Dr. Ming Li, Vice Chair of Hong Kong Chapter is introducing speaker in picture) on June 29, 2004.

Ø "Migration to Lead-Free Microelectronics Assembly and Some Key Technical Issues" by Dr. Karl Puttlitz on July 23, 2004.

Ø "Conductive Adhesive Joining Technology for Electronic Packaging Applications" by Prof Johan Liu on July 26, 2004.

Ø "Preparation and Implementation of Lead-Free Soldiering", by Dr. Ning-Cheng Lee on August 20, 2004.

The chapter also plans one more workshop on "Trend and Design of MEMS and Advanced Packaging" by Dr. K. N. Chiang in September 2004.

Dr. Cheung also informed us that he would step down from the Chairmanship in December 2004 and Dr. Ming Li would be the chapter chairperson for the next two-year term 2005 and 2006. The chapter would schedule their AGM in December for the elections of Chapter Vice Chair and Chair elect.

Taipei Chapter

· As reported earlier, CPMT Taipei chapter had arranged a technical lecture on "Thermal-Fatigue Life Prediction of Electronic and Optoelectronic Lead-Free Interconnects" by Dr. John Lau (Dr. Shen Li Fu, Taipei Chapter chair welcomes John) on June 13, 2004, at Kaohsiung, Taiwan. In addition to this Dr. John Lau gave another talk at Industrial Technology Research Institute, Hsinchu, Taiwan on June 14, 2004.

Dr. Lih-Shan Chen Secretary of CPMT Taipei chapter has further reported a technical workshop by Dr. Ning-Cheng Lee, Vice President of Technology of Indium Corporation of America on "Preparation and Implementation for Lead-Free Soldering" on August 16, 2004. This workshop was designed to help manufacturers to prepare for and successfully implement lead-free soldering procedures. Considerations on choice of solder alloys and surface finishes, selection of equipment, design of soldering processes, inspection, rework, and supply chain preparation were presented in detail at the workshop.

Shanghai Chapter

· We welcome the establishment of the new Shanghai Chapter during this quarter (as reported by Dr. Zhimin Mo). A range of activities are being organized by Dr. Sam Zhang for the chapter.

India Council

· During this quarter the India Council CPMT chapter had co-organized a technical talk by Mr. Rajinder Kumar on "Creating Awareness on Lead Free Interconnect Technology" on 20th August at Hotel Sun-n-Sand with SMTA IC in Bombay.

The chapter had earlier planned to organize 2 technical lectures and one administration (Execom) meeting during the months of July and August. The Execom however had to cancel these commitments in view of lack of funds (Annual chapter rebates of 2002 as well as 2003 not yet received in spite of many requests and reminders).

Our chapter Secretary, Prof M M Shah is now back in India and would now be taking interest in our chapter activities.

Report by REL/CPMT/ED Singapore Chapter

1. Technical talks Section's meeting on 27 Jul 2004

· Apr 15, Professor Chandan Kumar Sarkar (IEEE EDS distinguished lecturer) of Jadavpur University, India gave a talk on "Gate Oxide Degradation in MOS Devices under high field stress-breakdown issues and the model".
· May 20, Professor Kishor S. Trivedi of Duke University, USA gave a talk on "Reliability modeling: tools & techniques".
· May 27, Dr. Lakshmi Kanta Bera of Institute of Microelectronics, Singapore gave a talk on "Strained-Si MOSFETs and high-K gate dielectrics for advanced CMOS applications".
· July 13, Professor Juin J. Liou (IEEE EDS distinguished lecturer) of University of Central Florida, USA gave a talk on "Characterization and simulation of reliability of MOS devices".
· July 14, Professor Ananth Dodabalapur of University of Texas at Austin, USA gave a talk on "Finding applications for organic transistors".
· On July 15, Mr Steve Groothuis of Micron Technology Texas LLC, USA gave a talk on "Advanced CAE simulations in the semiconductor industry".
· On Aug 04, Dr Ahila Krishnamoorthy, Institute of Microelectronics, Singapore gave a talk on "Interfacial engineering to improve the reliability of Cu interconnects".

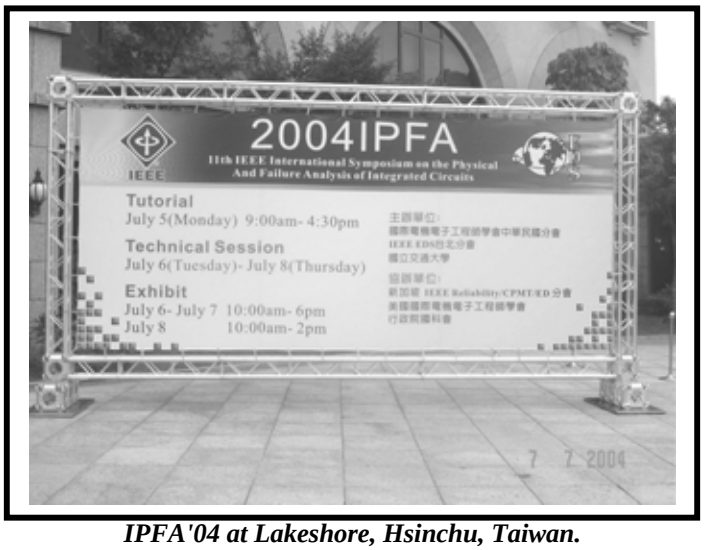
2. EPTC'04

The 6th EPTC is scheduled for 8 - 10 December 2004. The Call for Papers has received a good response and close to 200 abstracts have been received, topping the submissions in 2003. All the arrangements for a successful conference are being made including the short courses, keynote and invited speeches, table-top exhibition and social events. A new feature will be an executive forum on the trend and directions in key packaging thrusts targeted at technology leaders in the region. With the industry pick-up and the impending lead-free implementation, it is expected that EPTC 2004 will generate even greater interest and participation.

3. IPFA'04

The 2004 International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA'04), jointly organized by IEEE ED Taipei Chapter, IEEE Taipei Section, National Chiao Tung University (NCTU) and IEEE Rel/CPMT/ED Singapore Chapter, and technically co-sponsored by the EDS was a great success. More than 70 technical papers were presented, including two Keynote speeches on "Opportunities and challenges for high-k gate dielectrics" by Prof. T. P. Ma of Yale University, USA and "Technology and reliability challenges: A foundry perspective" by Dr. Jack Sun of TSMC, Taiwan. As per the IPFA tradition, four tutorial sessions and an equipment exhibition were held in conjunction with IPFA'04. A special IEEE Transaction on Device Materials and Reliability (TDMR) issue will be published for the selected IPFA'04 papers after going through the standard vigorous peer review.

IPFA'04 banquet (picture to right). From left to right: Dr. Guido Groeseneken of IMEC, Belgium, Dr. Alastair Trigg of IME, Singapore, Prof. TP Ma of Yale University, USA and Dr. MJ Sai of ITRI, Taiwan.



IPFA'04 at Lakeshore, Hsinchu, Taiwan.

IPFA'05

The organizing committee of IPFA'05 has been formed by the general chair, Dr. Alastair Trigg of the Institute of Microelectronics, Singapore. It will be held in Singapore, 27 - 31 June 2005. The first call for paper, was announced at IPFA'04 in Taiwan in July 2004.

4. WIMNACT

The 4th Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology (WIMNACT-Singapore) was successfully held on July 12, 2004, in Singapore. This mini-colloquium was organized and sponsored by the IEEE Rel/CPMT/ED Singapore Chapter, and co-sponsored by the EDS Distinguished Lecturer (DL) Program and Subcommittee for Regions/Chapters (SRC) as well as the School of Electrical & Electronic Engineering (EEE) at Nanyang Technological University (NTU). The Guest-of-Honor was Prof. Meng Hwa Er, Deputy President and Dean, School of EEE, NTU, who delivered a welcome address to the invited guests and the audience. There were five invited DL speakers, including four from overseas and one from the local Chapter. The first talk was given by Prof. Cary Yang from Santa Clara University entitled "Carbon Nanotubes as On-chip Interconnects," followed by the talk on "Trends on Low-Voltage SOI CMOS VLSI Devices and Circuits" given by Prof. James Kuo of National Taiwan University.

After lunch at the NTU staff club with the invited guests and

Chapter committee members, Prof. Juin Liou from University of Central Florida gave the talk on "On-Chip Spiral Inductors for RF Applications: An Overview," following by the talk on "An Overview of CMOS Technology for RF IC Applications" given by Dr. Yuhua Cheng from Skyworks Solutions. The Workshop ended with the talk by Prof. Xing Zhou on "Technology-Based Predictive Compact Model Development for Next Generation CMOS." In summary, the 4th WIMNACT-Singapore has been another successful event after the 3rd WIMNACT-Singapore, which was organized by the Chapter in October 2003. The Workshop received enthusiastic response with more than 100 attendees from the local industries and academic institutions. They showed deep interests in the invited talks, which covered a wide range of important topics of current and future technologies. The complete information on the 4th WIMNACT-Singapore, including all the slides and snapshots, has been made available from the following website: http://www.ntu.edu.sg/eee/eee6/conf/WIMNACT04.htm.

From right to left: James Kuo (Speaker, National Taiwan University), Kin Leong Pey (Chapter Chair, NTU), Juin Liou (Speaker, University of Central Florida), Meng Hwa Er (Guest-of-Honor, NTU), Cary Yang (Speaker, Santa Clara University), Yuhua Cheng (Speaker, Skyworks Solutions), Chaw Sing Ho (Chapter Committee Member, Chartered Semiconductor Manufacturing), Chee Lip Gan (Chapter Committee Member, NTU), Xing Zhou (Speaker, NTU, Chapter Committee Member)

5. Donation

The Chapter has donated S$1,200 to Temasek Polytechnic for a Bronze Course Medal Award in 2004 and 2005.

6. Plans

§ One technical talk has been organized in August.
§ A series of video courses on the past IEDM short courses will be organized between Sep and Dec 2004.
§ A series of short courses on ICFA has been planed for Oct-Dec 2004.
§ A one-day course on "Advanced Cu interconnects" by Dr. Jeffrey Gambino of IBM has been planned in Dec 2004.

-- By KL PEY, Chair, REL/CPMT/ED Chapter

List of Malaysia Chapter Activities

The details of the activities of the IEEE-CPMT Malaysia Chapter for the months of June to August, 2004

1 An Introduction to MEMS and MEMS Packaging.
Prof. K N Seetharamu, School of Mech. Eng. USM
Date: June 9, 2004
Time: 3.15 P M
Venue: Seminar Hall, School of Mechanical Engineering
USM Engineering Campus, 14300 Nibong Tebal
Attendance: 32

2 Executive Committee meeeting
Date: June 23, 2004
Time: 4.15 PM
Venue: Meeting Room, School of Mechanical Engineering,
USM Engineering Campus, 14300 Nibong Tebal

3 Distiguished Lecture
(Supported by IEEE-Cpmt HQ and School of Mech. Engg. USM) "Lead Free Solder"
Dr. John Lau, Agilent Technologies, USA
Date: July 9, 2004
Venue: Bilik Persidangan, Chancellery,
USM Main Campus, Penang.
Time: 4.00-7.00 PM
Attendance: 72

4 Winning with advanced micro devices
Mr Rodzaki Saad, Manager, Devices analysis, AMD, Penang
Date: August 25, 2004
Venue: DK 4, USM Eng. Campus,14300, Nibong Tebal
Time: 3.00-5.15 P M
Attendance: 62

Projected Activities for September-November, 2004

1 **Optoelectronics- A light Introduction**
by Prof. K N Seetharamu

2 **Characterization and Development of Thermal Interface Material - Reliability Performance**
by Mr. Wong shaw Fong, Intel, Malaysia

3 **Enterpreunership in Semiconductor Sector in Malaysia**
by Mr. Vyasa Kandasamy, SIRES Labs, MSC, CyberJaya.

--submitted by K. N. Seetharamu

Rajen Chanchani Wins IMAPS Award

International Microelectronic and Packaging Society (IMAPS) has announced that Rajen Chanchani is the winner of this year's William D. Ashman award. This award also makes Rajen a Fellow and life member of IMAPS. Rajen is the Chair of the CPMT Materials Technical Committee, an active session chair in ECTC, and a frequent Board of Governors contributor.

The criteria for this award.

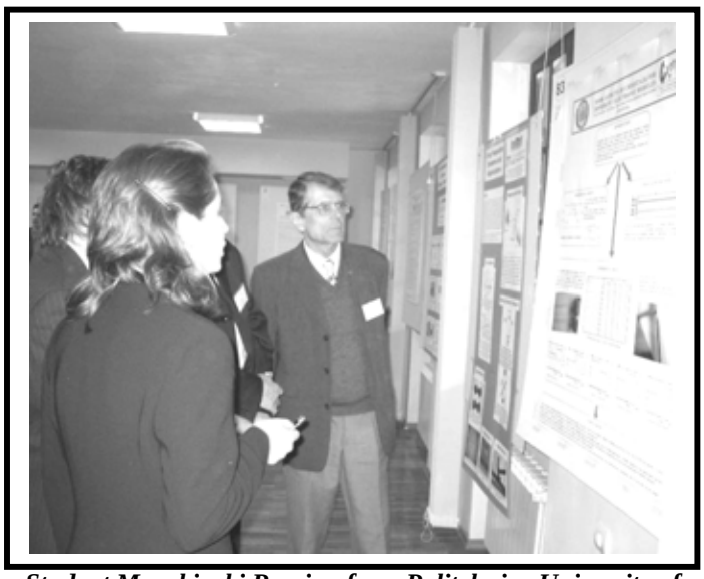
The William D. Ashman Memorial Achievement Award recognizes an individual who, in the opinion of the William D. Ashman Achievement Award Selection Committee, has provided significant technical contributions to the electronics packaging industry, while participating and demonstrating support of activities to enhance the electronics packaging profession as a member. Recipients of this award automatically become "LIFE MEMBERS and FELLOWS" of the Society.

News from IEEE CPMT SBC Politehnica University of Bucharest and Hu&Ro Joint Chapter

Students from Student Branch Chapter of Politehnica University of Bucharest participated with great success at the 27th International Spring Seminar on Electronics Technology, 13-16, May, 2004, in Sofia, Bulgaria.

The four posters, made by students, presented at the Poster Session, covered many areas of interest: Complex Evaluation of SMT Defects, Some Aspects of Crosstalk for Different Electronic Modules, Finite State Machines and their Applications in Software for Industrial Control, Remote Access Solutions for Industrial Control Systems. For the students, this was the first participation to an international conference.

Student Camelia Popescu from Politehnica University of Bucharest presenting her two posters to the Poster Session Chair: Dr. Pavel Mach and Prof. H. Wohlhrabe



Student Macabinski Romina from Politehnica University of Bucharest presenting her poster to the Poster Session Chair: Dr. Pavel Mach and Prof. H. Wohlhrabe and to Prof. Zsolt Illyefalvi-Vitez

Very appreciated were the posters and presentations containing theoretical aspects, experiments and simulations of the studied aspects. The ISSE Steering Committee accorded the "Excellent Poster Award for Young Scientists" to student Macabinski Romina, who also participated at the Oral Session with „Analysis of Reflection for Different Electronic Modules".

Student Macabinski Romina from Politehnica University of Bucharest receiving the "Excellent Poster Award for Young Scientists", from Prof. Klaus-Jurgen Wolter, Chairman of ISSE

The „Best Presentation Award" was awarded to Dr. Ciprian Ionescu from Politehnica University of Bucharest for the Oral Presentation „Thermal Characterization of Planar Transformers". The planar transformers were realized in collaboration with Fela.

At the Gala Dinner Dr. Ciprian Ionescu, awarded with "Best Presentation Award" and Dr. Norocel Codreanu, lecturer from Politehnica Universty of Bucharest

Gabriel Chindris PhD. from Technical University of Cluj-Napoca receiving the "Best Presentation Award for Young Scientist" from Prof. Klaus-Jurgen Wolter, Chairman of ISSE and a gift from the Bulgarian organizers of ISSE2004

The "Best Presentation Award for Young Scientist" was accorded to Gabriel Chindris Ph. D student from Technical University of Cluj-Napoca for the Oral Presentation "How to Adapt the Electronics Packaging Teaching Process to Current Needs-A Perspective".

In front of Bankia Castle the Roamnian team. From left to

right: Prof. Lita Ioan, Dr. Norocel Codreanu, Dr. Ciprian Ionescu, student Macabinski Romina, Prof. Paul Svasta, student Popescu Camelia and student Florin Streza

The conference was a very good occasion to exchange experience with the student colleagues from other universities from Romania, Bulgaria, Hungary, Germany and Poland.

The Interconnection Techniques in Electronics CAD student contest, TIE 2004 atracted 25 students from seven Universities of Romania: „Gh. Asachi" Technical University - Iasi, „Politehnica" University - Timisoara, Technical University - Cluj-Napoca, Politehnica University - Bucharest, University - Pitesti, North University - Baia Mare, „Stefan cel Mare" University - Suceava. This year the contest was organized by the Technical University of Cluj (www.utcluj.ro) on 22-23 May, 2004. Two students of the Student Branch Chapter of Politehnica University of Bucharest participated at the contest and obtained good results in the finals. The winners of the contest are students at „Politehnica" University of Timisoara from professor Horia Carstea.

Participants and organizers at TIE 2004. From left to right: Alexandru Borcea ARIES President, Prof. Paul Svasta, Assistent Professor Rangu Marius and Prof. Horia Carstea from Politehnica University of Timisoara.

Students found it a challenging and interesting contest and they look forward to take the prize next year.

The „Gh. Asachi University" will organize the next TIE 2005 contest. Good luck to all 2005 participants!

-- submitted by Macabinski Romina Daniela, Vice Chair IEEE CPMT Student Branch Chapter of Politehnica University of Bucharest, Romania -- romina.macabinski@cetti.ro

Editor's Turn

I want to thank all those CPMT members who took an hour from their vacation and sent me news for this issue. In particular, please smile next time you meet: W. Ross Stone, Bart Vandevelde, Margie Ballinger, Reed Crouch, Vasu Atluri, James Morris, Alina Deutsch, Evan Davidson, Toshio Sudo, Rajen Chanchani, Kerry Ann Ward, Ralph Russell, Jan Vardaman, Rao Bonda, Luu Nguyen, K. N. Seetharamu, Macabinski Romina Daniela, L. L. Pey, Dr. Parikh, Merrill Palmer, Paul Wesling, Marsha Tickman, and Phil Garrou. There were many others whose names I can not retrieve from my old gray cells while typing; my thanks to everyone.

It looks like the technology economy of the world is starting positive growth that could last 5 more years. Let us all work as individuals, companies, and in the CPMT Society to use this period to make permanent gains in education, publication, technology, and conferences. One advantage of our engineering globalization is that for each professional thrust there should be some region in a good position to lead progress.

This week it was necessary to stop reading my paper mail and email so that this Newsletter can get out on time. Spending evenings sifting through the slowly accumulating stacks of glossy paper and double clicking on entrancing email titles has become a way of life. Each communication is received with great anticipation since it may be the last piece in one section of life's jig saw puzzle which will finally let me figure out "if engineers really have more fun" or "why chimpanzees seem to be happier than humans even with the same genes". It is ironic that my own in-box is getting backlogged to the detriment of the next several months just so 4000 of you can have 24 pages added to your in-boxes. With any luck a piece to your jig saw is within these 24 pages. May your puzzle be coming together.

New Web Content -- CPMT Members Only!

All CPMT members are enabled to use our Members-Only webspace; to access full-text papers or presentations from several recent conferences:
**IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '02
**IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '03
**EuroSimE'03: 4th Int'l Conference on Thermal Simulation in Micro-Electronics and Micro-Systems (France)
**Phoenix Chapter Fall'03 Workshop on Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications
**IEEE Photonics Materials Reliability (PhoMat) Symposium '03
**NEMI Tin Whisker Workshop, Las Vegas '04
These are papers and presentations that cannot be found on IEEE's XPLORE.
IAccessing our Members-Only area is very simple:

Point your Browser to: www.cpmt.org/mem/
When you are asked, enter:
Username: xxxx
Password: xxxxxx

(all lower-case, notice to know what to put in for the xxxx's you must look at page 2 of the latest CPMT printed newsletter)

Upcoming Conferences

2004

****Polytronic 2004**: 4th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics September 12-15, 2004, Portland, Oregon -- Contact Dennis McCal at dennis.mccal@ieee.org

****2004 IEEE Holm Conference on Electrical Contacts** September 20-23, 2004; Seattle WA Jennifer Lambert (IEEE Confer Mgmt) j.lambert@ieee.org 1-732-981-3870 fax: 1-732-981-1203

****Future Directions in IC and Package Design Workshop** (FDIP), October 24, 2004, Portland Oregon, www.epep.org

****13th Electrical Performance of Electronic Packaging** (EPEP) October 25-27, 2004, Portland Oregon, www.epep.org

****Electrical Design of Advanced Packaging and Systems** (EDAPS), November 29, 2004, Kyoto, Japan, www.kuee.kyoto-u.ac.jp/EDAPS2004/

****7th VLSI Packaging Workshop of Japan** (VLSI Pkgng) ; Nov 30 - Dec 2, 2004; Kyoto, Japan ; Dr. Max Kohno, Dow Chemical. +81-550-82-8030 mkohno@dow.com

****Phoenix workshop on Device and Packaging for Wireless**, December 3, 2004, Phoenix Arizona, www.ieee.org/phoenix

****6th International Conference on Electronic Materials & Packaging** (EMAP); December 5-7, 2004; Penang, Malaysia; Prof. K N Setharamu, USM, knseetharamu@hotmail.com

****6th Electronics Packaging Technology Conference** (EPTC'04); December 8-10, 2004; Singapore; Prof. Toh Kok Chuan, Nanyang Technological Univ, +65 6790 5583. mkctoh@ntu.edu.sg

2005

****European System Packaging Workshop**, January 31 - February 2, 2005, Berlin, Germany, www.ewh.ieee.org/soc/cpmt/tc14

****21st Semiconductor Thermal Measurement and Management Symposium** (SEMI-THERM'05), March 15-17, 2005, San Jose, California -- contact Bonnie Crystall, cscomm@earthlink.net

****2nd International Workshop on Nano & Bio-Electronics Packaging**, March 22-23, 2005, Atlanta Georgia, www.prc.gatech.edu/nanobiopack

****6th Quality Electronic Design** (ISQED), March 28 - 30, 2005, San Jose, California, www.isqed.org

****EuroSime2005**, April 17 - 20, Berlin Germany, www.eurosime.com

****55th Electronic Components and Technology Conference** (ECTC'05), May 31 - June 3, 2005, Orlando, Florida -- Contact: Donna Noctor, noctor@ectc.net

****30th International Electronics Manufacturing Technology Symposium** (IEMT'05), July 11 - 13, 2005, San Francisco, California -- Contact: Gloria Lou, glou@semi.org. **11**

Call for Papers

*The 7th **VLSI PACKAGING WORKSHOP of JAPAN***

Nov. 30 - Dec. 2, 2004

Kyoto, Japan

Sponsored by the IEEE CPMT Society and National Institute for Standards and Technology

The VLSI Packaging Workshop of Japan has been held every other year since 1992 in the best season of Kyoto, the ancient capital of Japan, and it has become a well-known international workshop for advanced packaging technologies. The committee strongly encourages you to attend this workshop and participate in the discussion, in order to understand technology trends and find the proper target for technology development. Bring your latest research results and share with the participants who are experts from industry and the grove of Academe, and discuss with them. Anybody contributing to human progress through electronics is very welcome at this workshop. The following areas of technology are primarily of interest to the participants:

+ Advanced Fine Pitch Packaging
+ 3D Packaging & COC (Chip on Chip)
+ Micro Bumping Technology
+ Laminated Materials & Processing
+ RF Components & Modules
+ Integrated Passives
+ Packaging for Optoelectronics
+ Failure Mechanisms & Reliability Improvement
+ Electrical Performance & Thermal Management
+ Wafer Level CSP
+ Manufacturing Technology
+ Pb Free Interconnections
+ Materials for High Speed Application & Wafer Process
+ RFID tags
+ System in Package (SIP)
+ MEMS Packaging Technologies
+ Assembly and Packaging Challenges for Cu/Low-k Chips
+ Wafer Level Burn-in

The official language of this workshop is English. 30 minutes is allocated for each presentation, and it should include 5 - 10 minutes for Q&A. Authors who give outstanding papers will receive official recommendations for paper submission to the IEEE Transactions by the Japan Chapter and the Workshop Committee. This workshop will be held at Kyoto Research Park where the 6th Workshop was held in 2002.

Submission of abstracts:

Those who wish to contribute to the workshop should send a two-page summary of their paper (including figures) to the Program Chair **by May 28th, 2004**. The title of the paper as well as the names and affiliations of all authors must appear on the summary. If the paper is accepted, the summary shall be written to fit in a four-page format for the workshop's Proceedings **by September 3rd, 2004**. Notification of acceptance will be given **by July 9th, 2004**.

Program Chair:

Michitaka Kimura, Renesas Technology Corp.
4-1, Mizuhara, Itami-shi, Hyogo, 664-0005, Japan
Email: kimura.michitaka@renesas.com
Tel: +81-72-784-7127, Fax: +81-72-780-2676

General Chair:

Masahiko Kohno, Dow Chemical Japan Limited
Email: mkohno@dow.com

Vice Chair:

Tomoshi Ohde, Sony Computer Entertainment Inc.
George Harman, NIST

Japanese Committee:

Fuminori Ishitsuka, NTT Electronics
Noboru Iwasaki, NTT
Nobuo Kamehara, Fujitsu
Harufumi Kobayashi, Oki
Kaoru Kobayashi, Kyocera SLC Tech.
Hiroshi Manita, Casio
Tadaaki Mimura, Matsushita Electronics
Hirofumi Nakajima, NEC Electronics
Atsushi Nakamura, Renesas Tech.
Atsushi Okuno, Japan Rec
Kanji Otsuka, Meisei Univ.
Hiroshi Shibata, Osaka Inst. Tech.
Toshio Sudo, Toshiba
Takeshi Takamori, Oki
Hiroshi Yamada, Toshiba

US Committee:

Phillip Garrou, Dow Chemical
Len Schaper, Univ. of Arkansas
Ephraim Suhir, Univ. of Illinois
E. Jan Vardaman, TechSearch

European Committee:

Rolf Aschenbrenner, IZM, DE
Soeren Noerlyng, Micronsult, Denmark David Whalley, Loughborough Univ. UK

Asian Committee:

C. P. Hung, ASE, Taiwan
Jung-Ihl Kim, Amkor, Korea
Ricky Lee, HKUST, Hong Kong
Thiam-Beng Lim, IME, Singapore
Kyung-Wook Paik, KAIST, Korea

Institute of Electrical and Electronics Engineers, Inc.

Phoenix Section

Components, Packaging, and Manufacturing Technology Society Chapter

&

Waves and Devices Chapter

PRESENT AN ALL DAY WORKSHOP ON

Devices and Packaging For Wireless Communications

Date: Friday, December 3rd, 2004 **Time:** 7:00 A.M. - 5:00 P.M.
Location: Arizona Room, Memorial Union Building, Arizona State University, Tempe, Arizona

AGENDA

REGISTRATION and CONTINENTAL BREAKFAST: 7:00 A.M. – 8:00 A.M.

WELCOME and INTRODUCTION – Dr. Vasu Atluri, Manager, Intel Corp.: 7:50 A.M. – 8:00 A.M.

MORNING SESSION (Chairs: Dr. Dragan Zupac / Dr. Olin Hartin): 8:00 A.M. – 11:30 A.M.

- **Keynote Talk: Next Generation of Wireless Devices – Challenges and Issues**
  Dr. Sayfe Kiaei – Professor and Director of Connection One, Arizona State University
- **Research Toward More Flexible Radio Systems**
  Dr. Kevin C. Kahn – Senior Fellow, Director, Communications Technology Lab, Intel Corp.
- **Silicon for Millimeter Wave Wireless Applications**
  Dr. Modest M. Oprysko – Department Group Manager, Communication Technologies, IBM Research

BREAK: 9:45 A.M. – 10:00 A.M.

- **Nanoelectronics, Near-Term and Long-Term Opportunities**
  Dr. Stephen M. Goodnick – Chair, Electrical Engineering Department, Arizona State University
- **Modeling and Characterization of Noise and Linearity for RFIC Design**
  Dr. Guofu Niu – Professor, Electrical and Computer Engineering Department, Auburn University
- **Wireless Communication Standards and Regulations**
  Dr. Michael J. Marcus – Associate Chief for Technology (Retired), Office of Eng. and Tech., FCC

BUFFET LUNCH / VENDOR DISPLAYS: 11:30 A.M. – 12:30 P.M.

AFTERNOON SESSION (Chairs: Dr. Rao Bonda / Mr. Sam Karikalan): 12:30 P.M. – 4:00 P.M.

- **Keynote Talk: System-in-Package - Challenges / Directions for Communications and Wireless Products**
  Mr. Ken Brown – Senior Manager, Assembly Technology Development, Intel Corp.
- **Integration of Passives**
  Mr. Dean P. Kossives – Member of Technical Staff, STATS ChipPAC, Inc.
- **High Power RF Packaging for Wireless Infrastructure**
  Dr. Mali Mahalingam – Fellow of Technical Staff and Manager, Freescale Semiconductor, Inc.

BREAK: 2:15 P.M. – 2:30 P.M.

- **Wafer Level Packaging for Wireless Applications**
  Dr. Luu Nguyen, Engineering Manager, National Semiconductor Corp.
- **System Level Packaging for Wireless Applications**
  Dr. Amit Agrawal, Principal Scientist, Signal Integrity and Package Development, Broadcom Corp.
- **Keynote Talk: Enabling Mobility – Future Wireless Technologies**
  Mr. Behrooz Abdi – Vice President and General Manager, Qualcomm Inc.

PANEL DISCUSSION: 4:00 P.M. – 5:00 P.M.

- **Future Market Opportunities in Wireless Communications**
  Moderator: Dr. Chuck Weitzel – Manager, Freescale Semiconductor, Inc.

For General Information
http://www.ieee.org/phoenix

Vasu Atluri	(480) 554-0360	Steve Goodnick	(480) 965-6410	Mali Mahalingam	(480) 413-5368
Rao Bonda	(480) 413-6121	Olin Hartin	(480) 413-3831	Sujit Sharan	(480) 552-8073
Chuck Weitzel	(480) 413-5906	Dragan Zupac	(480) 413-3964	Sam Karikalan	(480) 222-1722

For Workshop Registration Forms
http://www.ieee.org/phoenixcpmt
Victor Prokofiev (480) 552-0228

For Vendor Registration Forms
http://www.eas.asu.edu/~wadweb/
Ellen Lan (480) 413-4128

First International Workshop on 3S Electronic Technologies

Tentative Date:
September 22 & 23, 2005

Global Learning & Conference Center

at Technology Square

84 Fifth Street, Atlanta, GA, 30308 USA

The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market IC-package-system co-design flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP's design simplicity, lower cost and higher system function integration, electrical performance, without the intellectual property issues that dominate SOC. The SOP is also different from and offers advantages over 3D packaging and SIP. The 3D packaging is typically stacking of similar, or dissimilar, chips such as DRAMS. The SIP goes beyond to embed both actives and passives but the passives are discrete, thick and bulky components. The SOP goes one step further in the ultimate 3D integration of components in thin film form at microscale, in the short term, and nanoscale in the long term. The SOP focuses on integrating both single function as well as heterogeneous system functions, optimizing ICs for transistors and package for integration of digital, RF, optical, sensor and others. It accomplishes this by both build-up SOP, similar to ICs and stacked SOP, similar to parallel board fabrication.

This workshop reviews the latest R & D and manufacturing status of each of the 3 electronic technologies around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.

Proposed sessions:

SOP, SIP, SOC and 3D Technologies

- Mixed Signal Design,
- Mixed Signal Tools
- Embedded Digital integration and modules
- Embedded Optical integration and modules
- Embedded RF integration and modules
- Multifunction integration and modules
- Fabrication and Assembly
- Mixed Signal Test
- Mixed Signal Reliability
- Stacked ICs
- Stacked Packages
- Manufacturing
- Applications & Products

For registration and continuously updated info, visit:
www.prc.gatech.edu/3s

13th Topical Meeting on Electrical Performance of Electronic Packaging

EPEP 2004

October 25-27, 2004
Portland, Oregon

Sponsors

The IEEE Components, Packaging and Manufacturing Technology Society

IEEE Microwave Theory and Techniques Society

Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

- Current and future issues related to on-chip interconnections
- Router friendly models and modeling tools: accuracy & efficiency
- Modeling and design of high speed digital IO circuits: signal propagation and reception
- On-chip power delivery and regulation
- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
- Power distribution and package resonance
- Long distance propagation in large switching complexes
- Switching noise in multi-layered systems
- Optoelectronic packaging; structure and system applications
- Electrical issues in MEMS packaging
- New and innovative interconnect packaging structures and their electrical performance
- RF/microwave packaging structures and their electrical performance
- MMIC modules and high density packaging
- Experimental characterization techniques
- EMC/EMI sources & effects
- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for one chip radios: design and modeling
- Performance of packaging for automotive radar systems

Conference Co-chairs: Tawfik Arabi, Intel Corp.; Robert W. Jackson, University of Massachusetts

Conference Web Page: Detailed and updated information can be found at http://www.epep.org

Paper Submission: Detailed information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 10, 2004.**

Student Paper Award: Two awards will be presented to the best two papers submitted by students

Short Courses/Workshops: On Sunday, October 24, 2004, a workshop entitled "Future Directions in Packaging" will be presented and short courses/tutorials will be offered.

3rd Asian Workshop on Signal Integrity EDAPS 2004

Electrical Design of Advanced Packaging and Systems (EDAPS) 2004

November 29, 2004 (Monday)
Clock Tower Centennial Hall, Kyoto University, Kyoto, Japan
Technically sponsored by IEEE CPMT TC on Electrical Design, Modeling and Simulation (TC-EDMS)

Sponsored by
* The 21st Century Center of Excellence (COE) Program, Kyoto University
* The Institute of Electronics, Information, and Communication Engineers (IEICE)

Objective:
The EDAPS Workshop is to enhance the technical awareness in the Asia region specifically in area of package and system electrical design concepts, issues, and challenges ahead for next generation electronic products.

Workshop Topics:
* High-speed digital signal integrity design
* RF/Microwave packaging for mobile phone
* EMI/EMC & electromagnetic modeling
* High-density packaging; CSP, BGA, and SiP
* EDA tools for on-chip, package, & board design
* Power distribution network modeling
* Interconnect modeling & simulation
* High-speed & high-frequency characterization
* High-performance packaging for SOC,

Workshop Location:
Int'l Conf. Hall (I), Clock Tower Centennial Hall, Kyoto University Yoshida-Honmachi, Sakyo-ku, Kyoto, 606-8501, Japan
Website: http://www.kuee.kyoto-u.ac.jp/EDAPS2004/

Preliminary Program for EDAP 2004, November 29
9:00 - 9:50 Registration
9:50 - 10:00 Opening Remarks, Toshio Sudo, Toshiba Corp., Japan

10:00-10:30 Performance Prediction of On-chip Global Signaling,
Masanori Hashimoto, Akira Tsuchiya, Akinori Shinmyo, Hidetoshi Onodera, Kyoto University, Japan
10:30-11:00 Microsystem Integration: Electrical Design & Test challenges,
Mahadevan K. Iyer, IME, Singapore
11:00-11:30 Design Challenge for Mobile Platform SiP, Heeseok Lee, Package Division, Samsung Electronics, Korea
11:30-12:00 Electromagnetic Interference in a Mobile Phone, Shinji Tanabe, Mitsubishi Electric, Japan

13:15-13:45 Fundamental Approach for 10 Gbps/pin I/O Interface System with Differential Transmission Line without Ground Plane, Kanji Otsuka and Yutaka Akiyama, Meisei University, Japan
13:45-14:15 Modeling and Simulation of High-Speed Serial Links in Complex Backplane Electrical Environments, Jared Zerbe, Rambus Inc, USA
14:15-14:45 Giga-Hertz Characteristics of Flip-chip BGA Package, Kazuyuki Nakagawa,
Renesas Technology, Japan
14:45-15:15 Spread Spectrum Clock Generator with Delay Cell Array to Reduce the EMI from a High-Speed Digital System, Jonghoon Kim, Memory Division, Samsung Electronics, Korea

15:45-16:15 Power Delivery Isolation Methods in Integrated Mixed Signal Systems,
Madhavan Swaminathan, Jinwoo Choi and Vinu Govind, Georgia Institute of Technology, USA
16:15-16:45 Suppression of GHz Range Power/Ground Inductive Impedance and Simultaneous Switching Noise using Embedded Film Capacitors in Multilayer Packages and PCBs, Joungho Kim, KAIST, Korea
16:45-17:15 Decoupling Simulation Method for System Electromagnetic Susceptibility
and Interconnects Modeling, Li Er Ping, Institute of High Performance Computing, Singapore
17:15-17:45 TBD

18:00-20:00 Welcome party

Final Program

Future Directions in IC and Package Design Workshop (FDIP)

October 24, 2004, Portland, OR

sponsored by:

IEEE COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY SOCIETY

organized by:

CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

1:15 - 1:30 pm **Welcome Remarks, Madhavan Swaminathan, GIT, Alina Deutsch, IBM**

SESSION I: SYSTEM DESIGN

1:30 - 3:15 pm

Session Chair:Ravi Kaw, Agilent Technologies

1:30pm – 2:05pm	Gigascale Integration – Design Challenges and Opportunities, Shekhar Borkar, Intel Corporation
2:05pm – 2:40pm	Emerging Trends in High-Speed Interconnects and Packaging Engineering, Sergio Camerlo, Cisco Systems
2:40pm – 3:15pm	Analog RF CMOS and Optical Design Techniques for 10+ Gbps Datacom, Martin Schmatz, IBM Corporation

3:15 – 4:00 pm - Refreshment Break

SESSION II: MODELING CHALLENGES

4:00 – 5:20 pm

Session Chair: Hartmut Grabinski, University of Hannover

4:00pm - 4:35pm	Power Distribution: Status and Challenges, Madhavan Swaminathan, Georgia Institute of Technology
4:35pm – 5:10pm	Signal Integrity Modeling and Simulation for IC/Package Co-Design, Ching-Chao Huang, Optimal Corporation

5:10 – 5:20pm - Break

SESSION III: SIMULATION CHALLENGES

5:20 – 6:35 pm

Session Hao-Ming Huang, IBM Corporation

5:20pm –6:30pm	Current and Future Directions in Simulator Development, Sani Nassif , IBM Corporation, and Jaijeet Roychowdhury , University of Minnesota
6:30 - 6:35 pm	**Closing Remarks, Madhavan Swaminathan, GIT, Alina Deutsch, IBM**

Information about the workshop can be obtained at www.epep.org

6th Electronics Packaging Technology Conference (EPTC 2004)

8 - 10 December 2004, Pan Pacific Hotel, Singapore

CALL FOR PAPERS

About EPTC

The 6th Electronics Packaging Technology Conference (EPTC 2004) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter with joint technical co-sponsorship from the CPMT Society of IEEE and IMAPS.

EPTC 2004 will feature technical sessions, short courses and exhibition. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Inaugurated in 1997, the EPTC has gained a reputation as a premier electronics packaging conference in South East Asia where the bulk of the world's packaging activities are taking place. Since 2002, it has been held annually in December, due to the growth in the number, scope and quality of its presentations.

Conference Topics

You are invited to submit an abstract presenting new development in the following categories:

1. Advanced Packaging: Single chip and multi chip packaging, wafer level thinning, bumping, packaging and 3D integration, Embedded Passives & actives on substrates, high power, high frequency / RF packaging, SiP and other system integration technologies

- Interconnection Technologies: gold and copper wire bonding and flip chip (eutectic/lead-free solders) on standard and copper low k wafers, solder replacement flip chip (ICP, ACP, ACF, NCP), under bump metallurgy, microvia and build-up technologies, nano interconnects.
- Manufacturing Technologies: Process characterization, yield improvement, cost and cycle time reduction, environmental improvements, Statistical process control.
- Materials & Processes: Advancements in adhesives, encapsulants, underfills, solder alloys, halogen-free materials, dielectrics, ceramics, composites, thin film processes on laminates, nano-materials and processes for packaging.
- MEMS Packaging: Packaging solutions for Inertial MEMS - Pressure sensors, actuators, microrelays Bio-MEMS, RF MEMS – Resonators, Switches and Optical MEMS- Switches, Crossconnects etc
- Electrical Modeling & Signal Integrity: Modeling simulation & measurement for coupling, reflection & switching noise, EMI/EMC analysis on package & subsystems, Time & frequency domain measurements for advanced modules.

2. Thermal Characterization & Cooling solutions: Modeling & simulation methodology for thermal characterization of advanced packaging, modules & systems. Novel thermal management solutions. Enhanced air & liquid cooling techniques.
3. Mechanical Modeling & Structural Integrity: Structural analysis, modeling and simulation of modules, sub-assemblies and systems. Failure mechanics and damage modeling. Thermo-mechanics. Multi-physics modeling. Moisture effects. Impact and dynamic effects. Experimental techniques and model validation. Numerical methods. Design optimization..
4. Optoelectronics: Passive components (waveguides, splitters etc), Photonic interconnects, Design, Modeling & Measurements for Gb/sec & Tb/sec modules and Optical backplanes.
5. Quality & Reliability: Component, board and system level reliability assessment, failure analysis, interfacial adhesion, accelerated testing and models, component and systems

Important Dates

31 July 2004	**Submission of abstract**
31 August 2004	**Notification of Acceptance**
9 October 2004	**Submission of manuscript**

Extended Abstract and Paper Submission

Extended abstracts are solicited to describe original and unpublished work. The abstract should be about 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories for abstract review. All submissions must be in English and should be made either online at www.eptc-ieee.net or via electronic mail to abstract@eptc-ieee.net . The required file format is Adobe Acrobat® PDF with only one single pdf file for each submission. Please limit the file size to a maximum of 2MB.

The abstracts must be received by 31 July 2004. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance and publication instruction by 31 August 2004. The final manuscript for publication in the conference proceedings is due by 9 October 2004.

Outstanding Technical Papers

The conference proceedings will be an official IEEE publication. Top quality papers will be submitted to IEEE/CPMT Transactions to be considered for publication. Author(s) of Outstanding Technical Paper(s) will receive an award at the next conference.

Short Courses

The conference program includes full-day short courses that will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings.

Exhibition

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference.

For latest conference information & contacts: **Website: http://www.eptc-ieee.net**

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6th International Conference on Electronics Materials and Packaging (EMAP 2004)
5-7 December 2004, Penang, Malaysia

FIRST ANNOUNCEMENT AND CALL FOR PAPERS

About EMAP

The 6th Electronics Material and Packaging Conference (EMAP 2004) is an international event organized by the School of Mechanical Engineering, Universiti Sains Malaysia, and IEEE CPMT Chapter with joint technical co-sponsorship from CPMT society of IEEE.

EMAP 2004 will feature short courses, technical sessions, and exhibition. It aims to provide good coverage of developments in all areas of electronics materials and packaging, from design to manufacturing and operation. EMAP 2004 is a major forum, providing opportunities to network and meet leading experts in addition to exchange of up to date knowledge in the field. Since 1999, EMAP has gained a reputation as a premier electronics materials and packaging conference in Asia Pacific where the bulk of the packaging activities are taking place.

Conference Topics

The topics of interests are specific to micro systems/MEMS, their packaging, electronics materials and reliability issues. Extended abstracts are being sought from, but not limited to, the following areas:

- **Automotive Electronics**
- **Chip-Scale Packaging/Flip Chip**
- **Electrical Modeling & Signal Integrity**
- **Green Materials**
- **High Density Displays**
- **High Density Packaging**
- **Interconnection Technologies**
- **Low Cost Packaging Methods**
- **Manufacturing Technologies**
- **Mechanical Modeling and Structural Integrity**
- **MEMS Packaging and Applications**
- **Microelectronic Materials & Processes**
- **No Flow Underfilling Process**
- **Optoelectronics/Photonics**
- **Polymer Materials & Microelectronic Applications**
- **Printed Wiring and Flex Boards**
- **Quality & Reliability**
- **Thermal Design, Analysis, and Characterization**
- **Electronic Inspection**
- **Thick & Thin Film Materials**
- **Wafer Scale Packaging**
- **Wireless Sensor Packaging & Applications**
- **Vibration on Electronic Devices**

Important Dates:

Submission of Abstract	**31 May 2004**
Notification of Acceptance	**15 July 2004**
Submission of Manuscript	**31 August 2004**

Extended Abstract and Paper Submission

Extended abstracts are invited to describe original and unpublished work. The extended abstract should be about 500 words stating clearly the purpose, methodology, results, and conclusions of the work. Key references to prior publications and how the work enhances the existing knowledge should be included in the extended abstract. Authors are requested to designate appropriate areas for the purpose of abstract review. All submissions must be in English and should be made via electronic mail to **abstract_emap2004@eng.usm.my**. The required file format is either MS Word or Adobe Acrobat© PDF with only one single file for each submission.

The abstracts must be received by 31 May 2004. Authors are requested to include their affiliation, mailing address, telephone and fax numbers, and e-mail address. Authors will be notified of paper acceptance and instruction for preparing final papers by 15 July 2004. The final manuscript for publication in the conference proceedings is due by 31 August 2004.

Short Courses:

The conference program includes short courses, which will be conducted by leading experts in the field. Details will be provided in the conference website and available in subsequent mailings.

Exhibition:

A tabletop exhibition from suppliers of materials, equipment, components, software, and service providers of electronics industries will be held at the venue of the conference

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Conference Information and Contacts: **Website:** http://www.eng.usm.my/mekanik/emap2004.html

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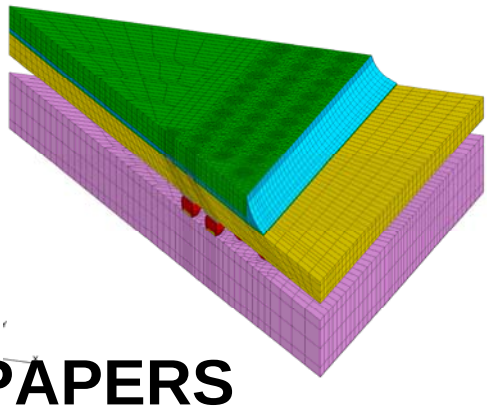
EuroSimE 2005



CALL FOR PAPERS

Thermal, mechanical and multi-physics simulation and experiments in micro-electronics and micro-systems

April 17-20, 2005

Berlin, Germany

The Conference

After five successful editions of the EuroSimE conference, a sixth edition is planned in 2005 and will take place in Berlin. This EuroSimE 2005 will address the results of both fundamental research and industrial application for **thermal**, **mechanical** and **multiphysics** solutions of (micro)-electronics, focusing on advanced **simulation** and **experiments**. The conference will include keynote presentations and sessions with a wide range of topics including, but not limited to:

Subjects:

- Mechanical simulation (static & dynamic)
- Thermo-mechanical simulation
- Thermal simulation (steady state & transient)
- Multi-physics simulation (coupled thermo-fluidic problems, coupled electro-mechanics, fluid-structure interactions)
- Validation of simulations by experiments
- Material characterisation, experiments and modelling
- Failure criteria and damage-modelling (fatigue, creep, delamination, cracks, buckling, large deformation, moisture-induced failures, yield)
- Process modelling
- Advanced numerical and analytical simulation methodologies and tools
- Behavioural modelling (HDL-A)
- Thin-film mechanics, interface strengths
- Simulation-based optimisation, virtual prototyping in product and/or process design
- Compact modeling and model order reduction

Applications:

- Components and packaging (traditional packages, flip-chip, BGA, CSP, Wafer-Level packages, MCM)
- MEMS (pressure, accelerometers, gyroscopes) and MOEMS
- Chip level reliability
- Nanotechnology
- Opto-electronic packages
- High Temperature Packaging
- Piezoelectric components
- Wafer processing and chip design
- PWB design and application
- Packaging for Harsh Environments
- Fluidic Components (microvalves, ink-jet nozzles, …)
- Infrared sensors and cameras, thermal actuators

To Submit an Abstract

You are invited to submit an abstract of about 500 words describing the scope, content, and key points (originality, specific results, potential impact).

Upload your abstract on **http://www.eurosime.com/**

Abstracts must be received by **October 15, 2004**. Authors will be notified by **December 1, 2004**. Deadline for the final manuscript is **January 28, 2005**.

Local organiser: Rainer Dudek (dudek@che.izm.fhg.de)

European System Packaging Workshop
Berlin, Germany

January 31 -- February 2, 2005

The 9th European Workshop of the IEEE CPMT and Computer Societies' Systems Packaging Committee (TC-SP) will be held this year in Berlin, Germany at the Park Inn Hotel, Berlin-Alexanderplatz. General Chair: Rolf Aschenbrenner (IZM Germany) General Co-Chair: Christine Kallmayer (IZM Germany)

BACKGROUND

The IEEE Computer Society's and the IEEE CPMT's Technical Committee on System Packaging will be holding its Year 2005 European Packaging Workshop in Berlin, Germany next January. Because of today's plethora of packaging meetings mainly covering the component and technology spectrums, the Systems Packaging Technical Committee now focuses on the trade-offs required for good system design. Typical topics include component choices, functional partitioning, signal I/O requirements, electrical design, cooling techniques, technology processes, reliability, cost and overall system performance.The goal of our workshops is to maximize the exchange of system-level packaging concepts and experiences for new and future products.
Program updates can be obtained from our web site at: http://www.ewh.ieee.org/soc/cpmt/tc14/

Preliminary Program

Keynote Presentation "The History of Electronic Packaging" Evan Davidson (IBM US-Ret.)

Session 1: Ambient Intelligence

Subtopics: Smart Card, RF/ID (Radio Frequency Identification),Wireless Technology, Micro-power
Session Chairs: Cian Mathuna (NMRC), Christine Kallmeyer (IZM)

Session 2: Biotechnology & Biomedical Technologies

Subtopics: Medical implements, Bio-sensors, Bio-chips, Point-of-Care Diagnostics Session
Chairs: Dr. Meyer (Dräger), Melcholm Wilkinson

Session 3: Photonics & Interconnect Technology

Subtopics: Optical Devices, and Waveguides Embedded in Circuit Boards
Session Chairs: Prof. Elmar Griese, Dr. Padraig Hughes (NMRC)

Session 4: High Performance Computing

Subtopics: Electrical Verification, Telecommunications, Power & Cooling
Session Chairs: George Katopis (IBM US), Paul Callender (Nokia)

Keynote Presentation "Current View of Package Technology Opportunities in the 45 nm Silicon Generation" Bob Guernsey (IBM US)

Session 5: MNT (Micro & Nano Technology) Heterogeneous System Integration

Subtopics: Low-Temperature-Cofired-Ceramics, MCMs, Wafer Scale Integration,
System-on-a-Chip, MEMS Packaging, RF-MEMS, System-in-a-Package
Session Chairs: Christian Val, Rolf Aschenbrenner

Keynote Presentations "New Advances in System-in-a-Package"
Prof. Rao Tummala (Georgia Tech US)

CALL FOR ABSTRACTS

Second International Workshop on Nano & Bio-Electronic Packaging

March 22-23, 2005, Atlanta, Georgia

Program Agenda and Further Information: www.prc.gatech.edu/nanobiopack

The "Second International Workshop on Nano and Bio-electronics Packaging" is a two-day event offering informative keynote presentations and technical sessions on Nano technology. The currently scheduled technical sessions and their chairs are as follows:

Nano Package Design
James Libous - IBM & Madhavan Swaminathan - Georgia Tech

Nano Biomedical Packaging
Jorma Kivilathi - Helsinki University of Technology and Terry Dishongh - Intel

Nano Photonics
Avi Bar-Cohen - University of Maryland and Ephraim Suhir - Designed Nano-Materials

Nano Packaging Materials
Goran Matijasevic - University of California

Nano Manufacturing
Srinivas Rao - Solectron and Randy Rannow - Hewlett-Packard

Industry Perspective
Charles Lee - Infineon, Singapore

NEMS & Fluidics
Michael Wahl - University of Siegen

Nano Interconnections
Andrew Tay, National University of Singapore

Nano Lithography
Ajay Malshe, University of Arkansas

Nano Testing, Modeling and Imaging
Sheng Liu, Wayne State University

Conference Coordinator: Dr. Swapan Bhattacharya (swapan@ee.gatech.edu)
An IEEE-CPMT Society workshop, sponsored in cooperation with NEMI and the Georgia Tech Packaging Research Center

Call for Papers

ISQED 2005
6th IEEE International Symposium on

QUALITY ELECTRONIC DESIGN : www.isqed.org

March 28-30, 2005 -- San Jose, CA, USA

DESIGN FOR QUALITY IN THE ERA OF UNCERTAINTY

ISQED is the pioneer and leading international conference dealing with the design for manufacturability and quality issues front-to-back. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting near 100 technical presentations, six keynote speakers, two-three panel discussions, workshops /tutorials and other informal meetings.

Conference proceedings are published by IEEE Computer Society and hosted in the digital library. Proceedings CD ROMs are published by ACM. In addition, continuing the tradition of reaching a wider readership in the IC design community, ISQED will continue to publish special issues in leading journals. The authors of high quality papers will be invited to submit an extended version of their papers for the special journal issues.

Paper Submission Deadline	September 30, 2004
Acceptance Notification	November 17-19, 2004
Final Camera-Ready Paper	December 15, 2004

Papers are requested in the following areas:

- Design for Manufacturability & Quality
- Package - Design Interaction & Co-Design
- Design Verification and Design for Testability
- Embedded Test Methodologies
- Robust Device, Interconnect, and Circuits
- EDA Tools & IP Blocks; Interoperability and Implications
- Physical Design, Methodologies & Tools
- Effect of Technology on IC Design, Performance, Reliability & Yield
- Design Quality Definitions, Metrics, and Standards
- Quality Driven Design Flows; SoC, ASIC, FPGA, RF, Memory, etc.
- Quality of Modeling Abstractions and Methods (Device, Interconnect, Micro and Macro Cells, IP Blocks, ...)
- System-level Design, Methodologies & Tools
- Redundancy & Self Correction Design Techniques
- Management of Design Process, and Design Database
- Global, Social, and Economic Implications of Design Quality
- Quality based EDA Tools, Design Techniques, and Methodologies

Submission Process

The guidelines for the final paper format is provided on the conference web site at www.isqed.org.
Address all other inquiries to isqed@isqed.org.

55th Electronic Components & Technology Conference
Call for Papers

The **55th Electronic Components & Technology Conference** will be held at Wyndham Palace Resort & Spa in Orlando, Florida USA on May 31 – June 3, 2005.

This conference comprises papers covering a wide spectrum of topics, including not only electronic components, but also exciting new developments in all areas of electronics technology (for example, electronics assembly, packaging, systems packaging, optoelectronics, reliability and materials). In 2004, over 300 papers and posters, and 16 Professional Development Courses were presented by companies, universities and research institutions from around the world. The audience included representatives from leading universities and companies eager to stay abreast of the rapidly changing and emerging technologies in the electronics field.

Major Topics for ECTC: Advanced Packaging, Components and RF, Emerging Technologies - Biomedical Packaging & Nano-Scale Packaging, Interconnections, Manufacturing Technology, Materials & Processing, Modeling & Simulation, OptoElectronics, Quality & Reliability

Professional Development Courses:

Proposals are also solicited from individuals interested in teaching educational short courses (~4 hours) on topics described in the Call for Papers. Proposals including course descriptions must be submitted to Rao Bonda, at rao.bonda@freescale.com no later than October 15th, 2004.

Paper Submission

You are invited to submit a 750-word abstract that describes the scope, contact, and key points of your proposed paper via the website at www.ectc.net. Please check the website for details on how to submit abstracts electronically. For additional information regarding abstract and paper submissions, authors may contact perfecto@us.ibm.com.

The abstracts must be received by October 15, 2004. Your submission must include the mailing address, business telephone number, facsimile number and email address of the presenting author and the names and affiliations of all authors. Please indicate no more than two Program subcommittees that should evaluate you paper for acceptance. Authors will be notified of paper acceptance with instructions for publication by December 15, 2004. At the discretion of the program committee, abstracts may be considered for poster sessions. Manuscripts are due in final form for publication in the Conference Proceedings by February 7, 2005. The work submitted should be original and no previously published, and avoid inclusion of commercial content. In addition to a printed copy conforming to the ECTC format, a computer file for CD-ROM is needed in the preferred MS Word format.

The 55th ECTC conference is sponsored jointly by the Electronic Components, Assemblies, and Materials Association (the electronic components sector of the Electronic Industries Alliance) and the IEEE Components, Packaging and Manufacturing Technology Society.