

# Components, Packaging, and Manufacturing Technology Society



# IEEE

## Newsletter



The Global Society for Microelectronics Systems Packaging



Vol. 28 No. 2, June 2005 (ISSN 1077-2999)

[www.cpmt.org](http://www.cpmt.org)

[www.evh.ieee.org/soc/cpmt/newsletter](http://www.evh.ieee.org/soc/cpmt/newsletter)

## President's Report

Returning from the ECTC Conference in Orlando, what else can there be to talk about? The ECTC was once again a rousing success. Preliminary attendance figures showed 900+ attendees from all over the world. A big BRAVO goes out to Donna Noctor -General Chair and Eric Perfecto - Program Chair. Of course none of this could have happened without the efforts of the entire conference committee and the 100+ members of the program committee who work to put the technical program together.

There was a very useful "lead free" panel discussion manned by Amkor, AMD, IBM, Flextronics, Infineon, Kyocera and NEC as well as a great CPMT-sponsored session from Japan on "Advanced Flex Circuit Board Technologies" There were several good sessions on wafer level and 3D packaging (topics close to my technical heart) and good sessions updating the attendees on the latest in the nano and Rf fields. The biggest complaint we still hear has to be that the attendee has to choose from among six parallel sessions and its hard to know what to go see in person.....but that's a good problem to have.

Aside from all the technical information that is stuffed into these three days after Memorial Day, the most important opportunity that presents itself is the opportunity to network with the leaders of the industry that are in attendance. I know I love getting back together with folks I have worked with in the past and meeting new people. In the old days, I enjoyed being introduced to all the "old timers" from Bell Labs and IBM who really knew what was going on. Now, many years later, as one of the old guys I enjoy meeting the younger engineers -- the ones full of energy and ready to change the world.

Speaking about changing the world, at the CPMT lunch we presented the IEEE CPMT "technical field award" to Tsukada-san from IBM Yasu for the work he did in the areas of high density laminates (SLC for those who know the lingo) and the brilliant concept of underfilling bumped chips when they were mounted on PWB to alleviate the stress and CTE mismatch issues. As I said at the luncheon -- in hindsight this probably does not sound astounding to you NOW, but I was there back then and bumping was a high-end, high-cost packaging technique that was only used for mainframed and only in combination with ceramic packages. The work of Tsukada and his co-workers at IBM Yasu revolutionized the industry and allowed bumping to be used in low cost consumer applications. To quote myself "Many of you out there today, would not have jobs or miniature cell phones if it were not for this activity 15 to 20 years ago."

**Hope to see everyone at next year's ECTC in San Diego !**

### Congratulations to our new fellows:

**Mr. Paul B. Wesling**

Self-employed

*for contributions to multimedia education development within the IC packaging.*

**Prof. Jorma Kalevi Kivilahti**

Helsinki University of Technology

*for contributions to the reliability of lead-free electronics.*

**Dr. William D. Brown**

University of Arkansas

*for leadership in furthering education of high density electronics.*

**Prof. Yonhua Tzeng**

Auburn University

*for contributions to diamond manufacturing processes..*



*I. Charles Ume*

Georgia Institute of Technology

**Electronics Manufacturing Technology Award**

*Robert C. Pfahl, Jr.*

iNEMI.

**Exceptional Technical Achievement Award**

*Tseung-Yuen Tseng*

Chiao-Tung University

**Outstanding Young Engineer Award**

*Lara J. Martin*

Motorola, USA

**Congratulations to our newly elected CPMT Board of Governors members :**

*Eric Beyne - IMEC*

*Steve Bezuk - Kyocera*

*Kitty Pearsall-IBM*

And our other award winners:

**David Feldman Outstanding Contribution Award**

*James E. Morris*

Portland State University

**.Outstanding Sustained Technical Contribution Award**

## CPMT OFFICERS

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## Elected Board Members

**2007:** Eric O. Beyne, Steve J. Bezuk, N. Rao Bonda, Rajen Chanchani, Kitty Pearsall, CP Wong

**2005:** William T. Chen Li Li, L. Merrill Palmer, Walter J. Trybula, E. Jan Vardaman, David C. Whalley

**2006:** William D. Brown, Philip C. H. Chan, Charles Lee, Johan Liu, Thomas G. Reynolds-III, Ephraim Suhir

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**Next News Deadline: September 5, 2005**

**Members-only Web:**

**UserName: xxxx (join CPMT to see web)**

**Password: xxxxxxxxxxxx**

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## CPMT SOCIETY NEWSLETTER

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\*\*\*\*IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 park Avenue, 17th Floor, New York, NY 10016-5997. 41.00 per member per year (included in Society fee) for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved, copyright(c) 2005 by the CPMT Society of IEEE. Authors and Artists given full permission for further use of their contributions. For circulation information call IEEE customer Service 908 981 1393, or FAX 9667.

## Board Meets at Disney World

President Phil Garrou opened the Board meeting early Saturday June 4 immediately after the highly successful ECTC meeting. Forty Board Members attended, a new record. He started by lauding the many years of volunteer positions that John Segelken (CPMT Treasurer) and Connie Swager (CPMT Marketing) had performed. At the end of the meeting John and Connie rode off into the animated sunset. Phil then introduced some new members of the Board including Jusheng Ma (Beijing Chapter Chair), Eric Beyne (IMEC), Philip



Chan, and Kitty Pearsall (IBM).

### Division I Director

**Lewis Terman**, Director of IEEE Society Division I, gave an eye opening talk on the workings of IEEE. He stressed that the Societies and Councils are where the value comes from in IEEE. All the technical publication and conference intellectual property is initiated from the 42 groups like CPMT. From the 324,561 IEEE members there are 316,396 memberships in these generation groups. However, each member averages 1.6 societies so only about 57% of IEEE members claim a technical society. This number is dropping, perhaps partly because one can get publications electronically rather than only through society membership



Over the last 4 years the IEEE headquarters finances were making most of the headlines. In 2003 the total IEEE reserves rose by \$26M and by the end of 2005 they should reach \$130M which is about 50% of the annual budget (the litmus test for a healthy organization). The reserves are being very conservatively invested. He worries that only about \$2M are available for new initiatives each year; a small amount for an innovative profession.

The IEEE membership is up by 0.5% in the same 12 months over which society membership was down 3.9%. Regions 7 - 10 have 38% of the members and are growing the fastest. About 8% of our members (25,000) are life members, a category that may not be financially sustainable in the future. Many considerations are being given to attracting members from related growing fields such as healthcare instrumentation.

Publications have historically fed the surplus by \$30M/year. IEL/XPLORE are growing to be an income producing product that will replace the paper transactions of the past. An access plan for small companies has been launched. The dispute of working with articles from "black-listed" countries was resolved to IEEE satisfaction. However, the easy electronic access to articles is a mixed blessing. For example, since IEL is available without being a Society member, many have lost need to associate with a society. Recently the number of electronic articles retrieved have been equally from conference proceedings as from archival journals.

He reports that the TAB has refocused on the future and the most important challenges to continued success. He empathized with the CPMT complaint that the tax of 1/3 of our net income to support the IEEE infrastructure was too high. There was a discussion on ways to increase income of chapters and increasing fees for international meetings

### ECTC Report

**Pat Thompson** reported that there were slightly more than 900 total attendance (750 full paid). This is the largest turn-out other than during Las Vegas years. Pat wondered if this large number was due to the excellent program, the theme parks, or the follow on convention at the Hotel. There were 16 professional development courses with 285 pupils. The Tin Whisker workshop was well attended with about 100. The new special topics meetings saw 100 at the Nano-technologies, and 50 at the Bio-tech. The education session was scheduled in conflict with many sessions that demanded professors to attend so next year the timing will be optimized. Pat indicated that the special student poster sessions on the last day resulted in more visits and more visibility of the students.

Although hotels for a group as large as ECTC must be arranged way ahead of time, there is action toward moving to the Contemporary hotel in Orlando in the future and moving to a cooler part of Nevada (Reno) next time. These changes should save our members 40% on hotel fees also. This year's ECTC should make a respectable surplus for the continuation of our Society. Next year Rao Bonda will be assistant Program Chair, Torsten Wipiejewski will be program Chair, and Eric Perfecto will be Vice General Chair.



### Society Business

Vice President **Ricky Lee** reviewed the many CPMT conferences. A big debate occurred concerning the impact the expanding multi-focus Society meetings in Europe and Asia will have on the 55-year old ECTC which is always held in the United States. To date the success of the EPTC has correlated to expansion in all other society activities including more region 10 attendees and speakers at ECTC (this year set an attendance record for a non-Vegas ECTC). Decision was to



go ahead with the European ESTC and continual growth of the Asian EPTC while monitoring impact on all other meetings.

Vice President **Rolf Ashenbrenner** reported that our iNEMI roadmap involvement started late but proved worthwhile on the individual volunteer level. Rolf also reported that Martin Goetz of IBM has agreed to Chair the IC and Packaging Assembly Technical Committee. In addition, the TC-"Discrete and Integrated Passives" is being merged with the RF and Wireless since much of the current research falls in both areas.

The informal task force structure is now in place to allow quick response to apparent trends in technology without having to establish a standing technical committee. It is anticipated that most task forces will finish their activities within 2-3 years and not need to continue forever.

Vice President **Paul Wesling** introduced Vasu Alturi of Intel as the next Newsletter editor, starting in December. He also mentioned Philip Chan as the New Director of IP Mining and Ontology for CPMT Publications. In addition, Avram Bar-Cohen is now the Editor-in-Chief of our three Transactions.



Paul described how our transactions "Impact Factors" have been recomputed by ISI and show considerable improvement. This factor is important for Universities to quantify the importance of publishing in our Transactions. Since we changed our Transaction names recently, the established ISI way of measuring Impact based on references to only the new name was vastly undercounting the true impact. Both by having editors and reviewers remind authors of recent work

pertinent to their paper and by speeding the time from submittal to publication, the "Impact" of the transactions can increase considerably.

Paul discussed the two possible solutions to the financial problem presented by the switch of publications to all Internet. First, IEEE could charge an up-front fee to the authors of an article (say \$1000) to pay for the peer review, editing,





cross referencing, and inserting in the huge IEEE publication library. A second approach is to charge only the readers each time another paper is searched. Right now we are mostly following the second approach with 50% of the publication income to our Society coming from the IEL database usage of CPMT articles. Another 35% of the income is proportional to the fraction of articles coming from CPMT.

Nomination Chair **John Segelken** announced that C. P. Wong would take over this position. Under the new system of the 6 new Board members to be elected this autumn, 4 will be from the Americas, one from Europe and one from Asia. For example, the ballots to members in region 10 will allow for voting for one of the listed candidates from Asia. Nominations must be in by 22 July.

Fellow Committee Chair **C. P. Wong** thanked everyone for the hard work producing and reviewing many Fellow nominations from among the CPMT membership. A discussion was held as to how the IEEE Fellows committee decides how many Fellows to award to each Society each year. No one knew the formula...if there is one.

Membership Chair, **Ralph Russell** described the thinking behind the slowly retreating membership numbers for most Societies. Of our members, approximately 13% are very active in producing the publications and conferences (the people that get their pictures in the Newsletter). Another 33% of members are motivated as users of the publication and meeting content. They are very active users. Both these groups tend to remain CPMT members for



decades unless their careers take a large technology change (they go from components to marketing). However another group of 33% tends to be young and non-USA. This group is neither active as volunteers or as intense users of CPMT "product". They are just "kind-of" interested. The future of any society depends on engaging a reasonable percentage of this group. Ralph described several

approaches to this group: more communication, IEEE portal, membership package sent to chapters and conferences, a disposable membership display for chapters putting on conferences, and including some CPMT promotion at each conference we sponsor (visibility). As of April 2005 our membership stood at 2756 down 6% in the last year, about the same as for all IEEE societies.

Ralph also described the two Boy Scout Merit Badge books and electronics kit that resulted from an IEEE committee that he has headed for several years.



Asia Liaison Chair **Bill Chen** presented the CPMT Sister Chapter Program that is being developed between Santa Clara Section and the Malaysia Chapter. Since many engineers travel between the two regions it is hoped to enlist these people to give tutorials and share experience on both sides of the Pacific. They hope to share: seminar speakers, seminar materials, experimental WEB chapter meeting broadcasts, and good ideas.

Rao Tummala mentioned that we have had two CPMT IEEE Field award winners of note to the whole industry. We want to keep this trend. He suggested that we look in the CPMT many technologies and list all breakthroughs in the last 15 years. Then by each breakthrough list the people most responsible for the vision and the practice should be listed. Those individuals that stand out should be submitted to the Field Award.



Vasu Atluri announced that the Phoenix Chapter was putting on its annual workshop on November 10th. It will involve RF devices, Interconnects, and Packaging for the Next Generation.

Student Chapter Chair **Bill Brown** discussed the 3 student chapter booths in this years exhibition: Hong Kong, Sweden, and University of Arkansas. The Sisphus task of bringing chapter to San Jose, Romania, and Shanghai is continuing. A Student Chapter web site keeper is being looked for.

**Johan Liu** of Chalmers University gave the Region 8 report. Many meetings have been held with good eastern European countries participating. Three new Senior Members were earned recently. Already eight separate Chapters in Europe are supporting the upcoming Polytronics'05 in Poland. The new all-Europe ESTC is aimed at Dresden in 2006. Some exciting scenes of the city were shown to motivate Board members to start practicing their German conversation.



Treasurer John Segelken had some black numbers on his ledger. In 2003 we had a surplus of \$349K from a revenue of \$1,386K. This brought our reserves to \$2M. In 2004 the surplus grew to \$497K from a revenue of \$2,150K. With investment growth the reserves at the end of 2004 was \$2.5M. Projections for 2005 say \$76K surplus from revenue of \$1,813. Our bill to IEEE is still the second largest claim against the revenue but a growing proportion is being used prudently to expand member services.

Education Vice President Al Puttlitz updated the board on the Distinguished Lecturer activity and asked for a 50% expansion of travel assistance for this group of lecturers. He also announced the Motorola Ph.D Fellowship winner. The successful professional development courses now have an excellent Certificate designed by Kristine Martin of Potomac Communication.

## Editor's Turn

The ECTC (ECC) has been the most heavily attended annual meeting of our Society for more than 50 years. This is the best chance we have to renew friendships and compare research notes across a large group of technologies that are the focus of CPMT. It was good to see so many this year.

This was to be the last issue of the Newsletter with me as editor. But it looks like Vasu Atluri will not take over until December. This means that the September issue will not be top priority for anyone. It may be electronic only since the paper version represents a lot of pain for volunteers. Please contact Vice President Paul Wesling for any volunteer work you can do for future newsletters. Please keep sending your news to the new editor, it is the member volunteers that make the Newsletter function. Thanks for 25 years of assistance.

My thanks to all the volunteers that sent in news this issue. This includes Phil Garrou, Marsha Tickman, Paul Wesling, Rajen Chanchani, Kishio Yokouchi, Craig Gaw, P. B. Parikh, Kristine Martin, Al Puttlitz, Yoshitaka Fukuoka, Megan McRaney, Reed Crouch, Swapan Bhattacharya, Boyd Wiedenman, Rao Bonda, Ricky Lee, Alina Deutsch, and Suresh Subramanyan..

## CALL FOR CANDIDATES

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of this Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways -- either by the Society Nominating Committee, or by petition.

As reported in past issues of the Newsletter, beginning with this year's election, members-at-large will be elected to achieve totals proportionate to the geographic distribution of CPMT members. This translates as follows:

Regions 1-6, 7 and 9 (US, Canada, South and Central America): elect 4 members (for total of 12)

Region 8 (Europe, Africa, Middle East): elect 1 member (for total of 3)

Region 10 (Asia/Pacific): elect 1 member (for total of 3)

Voting members will elect members-at-large from within their Region only (that is, members in Region 8 will vote for members-at-large from Region 8 only, etc.)

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can become a candidate via petition by following the procedures below. Members of the Board of Governors must be willing to attend two annual Board meetings and participate actively in areas of their interest (publications, conferences, membership development, chapter development, etc.) The term of office for this election is 1 January 2006 through 31 December 2008.

- Prepare a petition that contains your name, member number, and statement of your qualifications for office.

- Provide lines for signatories. Each line should include space for a printed name, member number, and signature.

- Have the petition signed by a MINIMUM of 25 CPMT Society members in good standing (Student grade members are not eligible to sign.)

Membership status of all signatories will be validated. It is suggested that you gather more than 25 signatures in order to assure meeting the minimum required number of valid signatures.

- Submit your petition by no later than Friday, 22 July 2004 to:

CPMT Society Nominations Committee  
c/o Marsha Tickman  
IEEE CPMT Society Executive Office  
445 Hoes Lane, PO Box 1331  
Piscataway, NJ 08855-1331 USA

or FAX to 732-981-1769.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at [m.tickman@ieee.org](mailto:m.tickman@ieee.org).

## Vice President of Publications

### New IEEE Press books:

"Integrated Passives" by Rick Ulrich (U-Ark) was published by Wiley/IEEE Press and is selling well.

We are self-publishing a monograph on Electrical Contacts this summer, a translation of an out-of-print book in German. TC-ECCC (old TC-1) has taken the lead, with Jerry Witter doing the editing following the translation. The cost to CPMT will be about US\$3700, and income expected of \$4000 to \$14,000. We are looking for other good manuscripts that can be co-published by IEEE Press and Wiley.

### CPMT Newsletter:

Dave Palmer, after perhaps 80 years as Editor (I jest!), has indicated that he will be retiring from the position this year after the June issue. I approached a number of active CPMT Board-level people about taking on this position. **Vasu Atluri**, a long active Phoenix Chapter officer, has volunteered to assume the



editor's position for the December issue.

### The CPMT Society Website:

I have received positive feedback from those conferences who have requested that I put a rotating banner ad for their CFP or Advance Program on our various web pages (Home Page, plus a number of

second-level pages). Click-through rates for these run from 0.3% of the number of times shown (for small regional conferences) up to 1.83% (this one was for ISEPT'05). A click-through rate of 1% of impressions is considered very good for websites, and these little display ads enhance the awareness of members and non-members. I'm happy to compose them for any CPMT event, on request.

### "Open Positions" in the Publications/Web field:

I'm seeking one or two members (and recommendations of other potential volunteers) with an interest in service to our membership, to take on some level of leadership within Publications. If this sort of multi-year assignment appeals to you, with a level of effort to be defined by you and me, then please let me know!

### Potential Assignments:

- Assistant Webmaster: coordinate a portion of the work, such as taking responsibility for the TC/Chapter sites, or the educational modules. Requires HTML, FTP, Server knowledge.
- Assistant Webmaster: streaming technology, server mirroring, on-line meetings software -- select software or services; install on our systems or select ISPs; prepare instructions for use.
- IEEE Press: Develop the structure for soliciting authors for manuscripts suitable for IEEE to publish or co-publish, on CPMT's behalf; work with Joe Brewer, our IEEE Press Liaison.
- Other assignments: I can offer all or part of any of the jobs outlined above, or we can custom-fit one to your interests. Our members see our publications as being the primary reason for belonging; we want to enhance our publications offerings and visibility, for a stronger Society. Give me a call!

-- Paul Wesling

## TC-Materials Meets at ECTC

The committee meeting was held on June 1, 2005, in conjunction with 55th ECTC at Lake Buena Vista, FL. Ten Packaging Material enthusiasts from around the world attended the meeting: Kwang-Lung Lin Chen Kung University, Taiwan; Richard Benson John Hopkins APL; Bill Brown U of Arkansas; Ephraim Suhir UC, Santa Cruz; C.C. Lee UC, Irvine; Charles Lee Infineon, Singapore; V. Kripesh IME, Singapore; John Pang Nanyang Tech. University, Singapore.



The main topic of discussion was the future of Advanced Packaging Materials Conference. This conference will be held in Atlanta in 2006, in Silicon Valley in 2007. The potential venue for 2008 is Dallas, and the potential venue for 2009 is again in California.

-- submitted by **Rajen Chanchani**, chair TC-5

## Publication's Committee at ECTC



VP Paul Wesling leads the publication technical committee in decisions on improving the Impact Factor of our transactions, on Avram Bar-Cohen agreeing to be the Transactions Editor-in-chief, introduces the new Newsletter editor (Vasu Atluri), and discusses how the Society might position itself with the many changes at IEEE on financially rewarding societies for publication.

The need to make it easier for authors and reviewers to insert references for previous articles which build the foundation for the new work was discussed -- the Ontologies.

## TC- High Density Substrates and Boards Meets at ECTC

On Wednesday (June 1st) morning, the High Density Substrates and Boards TC-6 had a seven Committee Member meeting chaired by Dr. Yoshitaka Fukuoka (third from right in picture). Dr. Paul Wesling also attended as adviser.



The first discussed item regarded member change confirmation. Mr. Rokuro Kambe (NTK) was replaced by new member Mr. Yukihiro Kimura (NTK) in April. Mr. Kisho Yokouchi (Fujitsu Labs) changed from USA to Japan regional member. There was much discussion regarding increasing international region membership, because to date TC-6 has consisted of mostly Japanese committee member. At the same time, committee communications and meetings in a local area are very convenient. TC-6 will have to continue to discuss this issue.



The second agenda item regarded details for operation of the CPMT TC-6 Seminar "Advanced Flexible Circuit Board Technologies" scheduled for the evening of June 2nd. Our biggest concern was the late seminar starting time at 7:30 p.m. Ways to increase attendance at late evening meetings were discussed. Seminar speakers were invited to this morning meeting for introduction to one another and explanation of a preparatory plan. (The CPMT seminar attracted over 80 audience members in spite of the fact that it was a late evening meeting.)

The last item regarded preparation of next seminar at ECTC 2006. For this item, TC-6 will have next committee meeting at Tokyo in August. We will fix the main theme of our next seminar, and we will initiate a call for papers.(working TC picture)

-- submitted by Kishio Yokouchi, TC-6 committee member

# ECTC Professional Development Courses

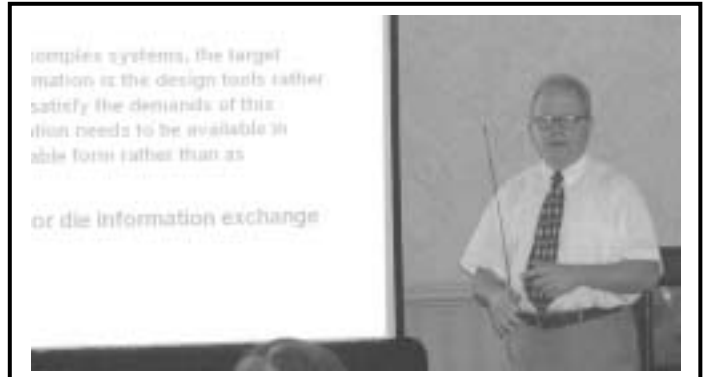
There were 16 topics offered to 285 eager engineers wanting to increase their professional talents and earn Continuing Education Units.



Ricky Lee, Rao Bonda, and Al Puttlitz were the leaders who organized the day of learning.



Prof. Rick Ulrich from University of Arkansas lectures on "Embedded Passive Technology and Commercialization"



"Final Manufacturing for Stacked SIP Products" by Larry Gilg



"Lead-Free Soldering -- Metallurgical Fundamentals" with instructor Ning-Chen Lee.



Luu Nguyen of National Semiconductor is instructor for "Wafer-Level chip-Scale Packaging"

Eric Beyne, IMEC, new to Board



"3D Integration Technologies -- An Overview" presented by Rajen Chanchani.



Connie Swager still smiles after much CPMT Society service





## Second ECTC iNEMI Tin Whisker Workshop

The iNEMI held the second annual Tin Whisker Workshop the day before ECTC started in Orlando May 31, 2005. Chaired by **Ron Gedney** and moderated by **Henning Leidecker** from NASA about 100 engineers wrestled with the consequences of pure tin coatings on electronic component leads. Pure tin has become one of the common options now that the long successful Pb-Sn coatings are discouraged for environmental reasons. Results of more than 9,000 hours of testing under various stress tests were discussed. Leidecker started the session by saying this is a real problem that was responsible for destroying a space craft 8 years ago. A whisker caused an arc that became a 100 Amp event. He pointed out that the thousands of fuses in the Hubble can arc uncontrollably with only 25 V once the air leaks out of their package.



Valeska Schroeder of HP described the incubation time before the whisker growth begins. The several accelerated test methods turned out not to be all that accelerating however humidity, temperature cycling, and sustained high temperature seemed to be an accelerant. The humidity above 85% would cause condensation in a non-uniform chamber and thus corrosion which was directly correlated to whisker growth.



**William J. Boettinger** of NIST described his study of the correlation of compressive stress in the tin plated film with whisker growth. He also mentioned that the columnar grain structure encouraged whisker growth whereas the vertically multi-grain structure as seen in SnPb films suppresses whisker growth. For example he found tin on copper leads has x10 the compressive stress of a plated Tin/Lead finish. Adding Cu to Sn caused compression whereas Pb additions

put it in tension. He recommended pulse plating of tin to attempt to get horizontal grain boundaries that slow down whisker growth.

George Galyon of IBM made a grand attempt to summarize all the results of the study groups. First he stressed that compression in the tin film is the driving force even in those few cases where whiskers appear to grow in tension. He noted that at the tin-copper interface, the copper diffused so fast that Kirkendall void developed. This diffusion could result in build up of compression in the tin film. However, if this tin film is kept thinner than 2 microns the whisker problem is usually controlled. In contrast, tin on nickel sees voiding in the tin and hence tends to put tin in tension.

Chen Xu of Cookson used X-ray data to confirm the state of stress in the tin films. He reported that the tin in Sn/Ni on copper leads are tensile after aging if not before. Also the tin directly on copper leads get more compressive during aging up to 20 MPa. The flexure beam work of S. Lal of FCI added confirmation to these results although everyone was cautioned that the stress state of the complete beam system was not the same as the stress state within the surface tin.

John Lau mentioned that when performing the high temperature surface soldering of the assembly line the resulting tension supplied by the board may wipe-out any initial compression in the isolated tin lead. The moral may be to assemble soon after tin plating. Luu Nguyen mentioned that most high volume manufacturers for consumer products prefer to keep using standard matte tin that they have already qualified at great expense despite the growing understanding from the iNEMI groups. It was also suggested that since there is no grant money chasing the whisker problem there have been few academic champions of this complex phenomena.

**Asa Frye** of IBM used EBSD to obtain the find the local details of grain crystal structure near the whisker base. This approach allowed one to know the stress state of the grains in question and to confirm the zonal structure analysis which tried to determine the stress of each layer in a multilayer / multiprocessed structure. This data added to the suspicion several group members have developed that unintended copper contaminants in tin plating are often the cause of unwanted stress.



Marc Dittes described the humidity tests performed. He confirmed that condensation induced corrosion also was advantageous for whisker growth. The difficulty of making chambers uniform throughout means that high humidity tests result in condensation that causes corrosion. He also confirmed that board mounting of the lead stops whisker growth. Thus, he suggested that the component should not be the level tested by the manufacturers, but rather the final system configuration.

Peng Su of Freescale stated that the potential between exposed Cu and Sn was the main driver for corrosion in condensation and that this appeared a driver for much whisker growth. With board mounted devices he had seen no whisker growth even with pure tin remaining exposed above the solder wetted region. He noticed that the bare tin was always coated with carbon compounds coming from the flux residue, thus protecting the tin. It was also noted that mechanical trimming of the leads caused local compression regions even in otherwise tensile tin



and corrosion and whiskers soon followed. Sharp cutting tools caused less problem than dull.

J W Osenbach of Agere mentioned philosophically that every lead will eventually corrode since tin wants to become oxide. He stressed that coupon tests miss the important edge effects of leads. He showed how easy it was to see Kirkendall where there are none. He also mentioned that once condensed water occurred it took several weeks for it to evaporate in typical test chamber conditions. Mobile devices could be seeing lots of condensation in normal use.



**Joe Smetana** of Alcatel presented an engaging visual image of how the whiskers grow out of tin grains. Andre Egli of Rohm & Haas saw whisker growth as a means of reducing compressive stress when general extrusion is not allowed by the system diffusion. The SnO on the surface inhibits normal surface diffusion from relieving stress. He showed how the surface morphology changed enormously from the first 30 seconds after plating to 6 days later at room temperature. In particular, all the initial screw dislocations have disappeared. He showed a sequence of under the surface changes that determined if whiskers would be encouraged or discouraged. He saw the dynamics as a race between surface "fibrous" structure formation that blended the grains versus whisker formation.

## Gary May Earns Chair

The Georgia Institute of Technology has selected Gary May, professor and executive assistant to Georgia Tech President Wayne Clough, to be the new Steve W. Chaddick Chair for the School of Electrical and Computer Engineering (ECE). He will start as chair on May 1, assuming the duties of Roger Webb, who retired in December.

The School of Electrical and Computer Engineering is one of Georgia Tech's largest schools, with more than 130 academic and research faculty members and 2,300 students at all degree levels. U.S. News & World Report recently ranked both of Tech's programs (electrical and computer) sixth in the nation.

May earned his bachelor's degree in electrical engineering from Tech in 1985, moving on to the University of California at Berkeley for his master's and doctoral degrees. He returned to Georgia Tech as an assistant professor in 1991 and accepted the Motorola Foundation Professorship in 2001.

May has been intimately involved in developing programs aimed at increasing the number of minority students who pursue advanced degrees.

-- submitted by Megan McRainey

## Shenzhen China -- ICEPT/ISEPT

The 6th International Conference on Electronics Packaging Technology will be held in Shenzhen Convention & Exhibition Center - Shenzhen, China on August 30 - Sept. 2, 2005

For further info, please visit:

<http://www.prc.gatech.edu/events/icept05/index.htm>

**ABSTRACTS** were DUE May 25, 2005

but presentation participation may still be possible if you send your proposal via email to [wangcq@hit.edu.cn](mailto:wangcq@hit.edu.cn), including your affiliation, email address, zip code, mailing address, and phone number.

### ABOUT ICEPT

Since 1994, ICEPT electronic packaging conferences have been held in China every two years. Over 400 attendees have presented and exchanged information at ICEPT which attracts researchers, developers and producers of packaging technology for ICs, MEMs, Opto, LEDs, LCDs, sensors, package substrates, PCBs and assembly.

### SESSION TOPICS

- System Packaging & Integration
- Electrical & Mechanical Design, Modeling & Tools
- Materials & Processes
- High Density Substrate & PCB
- Micro-joining & Assembly
- Surface Mount Technology
- Flip Chip & Wafer Level Packaging
- MEMS, LED, LCD & Optoelectronics Packaging
- Manufacturing
- Reliability
- Poster Session by CPMT for the past five (5) years

## Advanced Wirebond Interconnection Technology

### Book Review

Author: Shankara K Prasad, INKROMA Bangalore  
2004 Kluwer Academic Publishers, 670 pages



This book is intended for an assembly production house setting, appropriate for management, designers, chief operators, as well as wirebond production engineers. Operational issues such as specifying and optimizing wire and automatic bonders for a product line are included.

The book is very good with "visual" explanations for quick grasping of the issues. In addition, the fundamental metallurgical or mechanical root causes

behind material and process choices are presented.

The book has a clear prose style and a very readable font and page layout. The figures, although effective, are simply low

resolution screen prints from a personal computer and thus have aliasing and fuzziness.

This book has excellent overall tutorial and enough description of wire and bonding equipment so the reader could specify and negotiate correctly for with suppliers. The majority of the book dwells on establishing the bonding process for a particular product; determining the "window" of adjustments. The book ends with discussions on establishing quality metrics and reliability assurance tests. A CD comes with the book and contains close-ups and animation of the different wire bonding methods - a great visual learning tool which is a step ahead of past books.

Each chapter of the book includes enough tutorial information to allow it to alone with little need to page backwards. A short but good reference section is at the end.

If you have not read a wirebonding book, or the one you read 10 years ago was borrowed and never returned, now is the time to buy this book. --reviewed by David W. Palmer, editor

## Upcoming Meetings

\*\* Organic Microelectronics Workshop (ACS/MRS/CPMT) July 10-13, 2005 -- Newport, Rhode Island, USA -- more information at [www.organicmicroelectronics.org](http://www.organicmicroelectronics.org)

\*\*30th International Electronics Manufacturing Technology Symposium (IEMT'05) --July 11-12, 2005 -- San Francisco, CA USA -- Contact Sheri Mukai, [smukai@semi.org](mailto:smukai@semi.org)

\*\*ICEPT05 -- August 30 - September 2, 2005 -- Shenzhen China -- [www.prc.gatech.edu/icept05/index.htm](http://www.prc.gatech.edu/icept05/index.htm)

\*\*ISSM 2005, September 13-15, 2005 -- San Jose, CA -- [www.issm.com](http://www.issm.com)

\*\*First Int'l Workshop on 3S Electronics Technologies System-on-Package, System-In-Package, System-on-Chip September 22 - 23, 2005 -- Atlanta, GA USA -- more information at [www.prc.gatech.edu/3s](http://www.prc.gatech.edu/3s)

\*\*Therminics, September 27-30, 2005, Italy -- more info at <http://tima.imag.fr/conferences/therminic>

\*\*Workshop on Accelerated Stress Testing & Reliability (ASTR'05) -- October 3 - 5, 2005 -- Austin, TX USA -- contact [alex.porter@entela.intertek.com](mailto:alex.porter@entela.intertek.com)

\*\*FDIP05, October 23, 2005 -- Austin TX -- [www.epep.org](http://www.epep.org)  
\*\*EPEP05, October 24-26, 2005 -- Austin Tx -- [www.epep.org](http://www.epep.org)

\*\*5th IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics (POLYTRONIC'05) 23-26 October, 2005 -- Wroclaw, Poland -- more information [www.polytronic2005.org](http://www.polytronic2005.org)

\*\*Packaging Workshop -- November 10, 2005 -- Phoenix AZ -- [www.ieee.org/phoenix](http://www.ieee.org/phoenix)

\*\*EPTC05 --Dec 7-9, 2005 -- Singapore -- [www.eptc-ieee.net](http://www.eptc-ieee.net)

\*\*EDAPS05 -- December 12-13 -- Bangalore India -- <http://ewh.ieee.org/rio/bangalore/cpmt/events.html>

\*\*EMAP05 -- December 11-14 --Tokyo Japan -- [www.sms.titech.ac.jp](http://www.sms.titech.ac.jp)

## New Senior Members in CPMT

Faa-Ching Wang -----Dallas  
Dennis Horwitz -----Buenaventura  
Jian Cai-----Beijing

## Region 10 Chapter Activity Round up

**Dr. Pey Kin Leong, Chapter Chair of Singapore IEEE REL/CPMT/ED Chapter** has reported activities during this quarter as under:

### (a) Technical Talks

(i) "Nanoscale Elastic Circuits" by Prof. Arokia Nathan of the University of Waterloo, Canada, on March 14, 2005.

(ii) "Novel Nano- crystals and SONOS-type Nano-dots Flash" by Mr. Chen Jinghao of the National University of Singapore on March 28, 2005.

(b) The **Chapter has donated** a sum of S\$800 to the Student Chapter of the Nanyang Technological University branch for organizing the IEEE Science Symposium (2005) and IEEE - Student Professional Awareness Conference.

(c) The CPMT Singapore Chapter is preparing for the 7th Electronics Packaging Technology conference (**EPTC - 2005**) on 7th - 9th December, 2005, with Mr. Y.C. Mui of advanced Micro Devices as General Chair and Mr. James How from Motorola and Mr. John HL Pang from Nanyang Technological University as technical chairs. The call for papers has been initiated to 6000 fellow Researchers, Managers etc.

(d) The Chapter is organizing the **12th IPFA** event being held from June 27 to July 1, 2005 (5 days). About 70 papers with six tutorials would be presented at the symposium. The exhibition has already received bookings for 26 booths.

(e) The Chapter has also reported organization of **8th WIMNACT** being held on July 2, 2005 at Singapore. Four Overseas Distinguished Lecturers and other local distinguished lecturers have agreed to make presentations at the workshop on the latest developments on Nanoscale CMOS Technology.

**Malaysia Chapter** had their AGM on Mar 19-2005, and have elected Dr. CH Chew (from ON Semiconductor) as chapter chair. Professor Seetharamu will continue as past Chapter Chair Advisor. The Chapter would like to express its gratitude to Prof Seetharamu for his distinguished service.

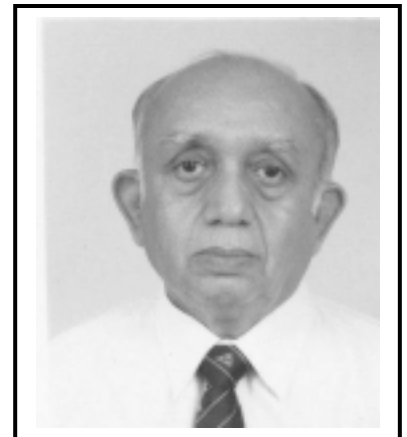
During January-June 2005, the chapter has two organized talks (from the industry experts in the area of semiconductor packaging) as under:-

- (i) "Understanding Of Leadframe Manufacturing" and
- (ii) "Fundamental Knowledge of Bonding Wire".

An industrial visit was also organized for students from the University of Nottingham (Malaysia Campus) to a semiconductor packaging house.

The **India Council Chapter** is busy organizing their annual seminar co-sponsored with SMTA-India Chapter. This 5-day event will be organized from July 16, 2005 - July 20, 2005, at New Delhi and would also include a Surface Mount Technology Certification course conducted by overseas experts. On behalf of India Council CPMT Chapter Dr. Parikh will be actively associated with the organization of this event.

-- submitted by  
Dr. P. B. Parikh



# Global Manufacturing

The ECTC plenary Session was held the evening of June 1.

**Torsten Wipiejewski** of ASTRI was the chair.

Rolf Plieninger of Infineon pointed out that his company was now #4 in the world semiconductor manufacturing after Intel, Samsung, and TI. He pointed out that of the three cycles that face manufacturers (industry-wide economy, technology, products) that an individual company could only influence "products" strongly and "technology" moderately. He listed the big drivers that occur at about 10 year intervals: 1985-PCs, 1995-communication, 2005-convergence, 2015-?bio/health/safety. In each driver the percent value due to semiconductor chip has dropped in time from 60% for the first PCs to 40% of today's cameras.

Despite the many negative trends (shorter product lifetimes, relentless cost pressure, 20% of cash flow going to capital) it is a great business as long as you are a global player and take advantage of local skill sets and can spread exchange rate risks. He saw design as becoming balanced throughout the world. He sees custom SIP as beating ASIC except in huge production runs.



**Picture from left: Rolf, Ping, and Dongkai**

Ping Wang of Freescale Semiconductor described some challenges of going global. They have moved part of their R&D to Asia. However, most fresh student graduates in Asia have had no exposure to processing equipment as well as having no "work place skills". Much training must take place in the first year with Westernized teachers dominating conversation to the detriment of building a company culture. Once trained, many new workers then try to find another job in one of the large cities. She remains optimistic.

Dongkai Shangguan of Flextronics showed charts indicating that IC production followed GDP growth trends although GDP grows at 2.5% compared to a 10% annual semiconductor growth. He predicted the trends of America's 38% ownership of manufacturing in 2002 dropping to 28% by 2020. Part of this is due to China growing over the same period from 7% to 34%. Although mass production will still be the method, personalization will become the overlay. Part of this will see the global market as being the sum of coordinated regional markets.

Historically the companies have seen that captive manufacturing leads to hierarchical costs. Thus, EMS providers out-source globally. However, the downside is that the supply chains are long and less able to anticipate any economic downturn with the chance of bigger losses to suppliers in a recession. EMS companies are

taking on some design and product development (called ODM). In the future he sees design as a commodity. One of the big challenges for a global company will be to develop win-win relationships with Chinese OEMs. Another challenge is for a global EMS to compete with emerging regional EMSs. A problem across the board is lack of experienced electronics manufacturing engineers.

He recommends the following strategic directions: (1) Ubiquitous manufacturing to gain from every regional advantage, (2) expand in scale and global reach with a deep set of skills and capabilities, (3) have innovation, productivity, efficiency, and lean manufacturing, (4) provide your customers with green services to get more visibility and loyalty.

Michael Lebbey of OIDA described the history and projection of the opto-electronics marketplace starting with LEDs in the 60s with lots of fundamental R&D at IBM and AT&T; the discrete communication lasers of the 70s; the improvement in quality in the 80s with Bellcore, Nortel, Siemens taking the R&D lead; the material breakthrough of the 90s (InGaAIP/InGaN); and this decade perhaps being measured by the manufacturability improvements in communication electro-optics and the huge growth of entertainment rather than communications sectors.



Despite the sustained 12% growth in market, industrial engineers are still 'recovering' from the communication bubble pop of 2000. The flat display panel, CD/DVD reader heads, and high brightness LEDs represent more than 80% of the market today. In contrast, the communication sector is still overbuilt with InP fabs still mostly empty. There should be consolidation, but each company thinks their IP mix is better than the other guys. In particular, there are 30 different ways to make a High Brightness LED and thus lots of IP and trade secrets. However, markets have a way of overcoming egos and Michael predicts reorganization and emergence of a strong InP industry by 2009.

**CPMT Board members before the all day meeting: seated from left: Ricky Lee, Jusheng Ma , Li Li, Ephraim Suhir, Charles Lee. Standing from left: Ralph Russell, Rao Bonda, Rolf Ashenbrenner, John Segelken, Jan Vardaman, David Whalley, Rajen Chanchani, Bill Chen + 27 off camera**





## CPMT Applauds its Finest

With a crowd of almost 700 people on hand to celebrate, the CPMT Society honored its top peers for their distinguished performances in technical excellence and dedication to the Society at the CPMT Society sponsored luncheon at the 55th Electronics Components and Technology Conference (ECTC) in Lake Buena Vista, Florida.

Phil Garrou, CPMT Society president, along with N. Rao Bonda (awards chair), Marsha Tickman (executive director) and Society officers and Board of Governor members, presented the awards.

"The CPMT Society is proud to recognize these individuals for helping to further technology in our fields of interest and, at the same time, helping to strengthen the Society," said Bonda,

### Honored at this year's luncheon:

· **Prof. James E. Morris** (Portland State University, Portland, Ore., USA) - The David Feldman Outstanding Contribution Award - for his exceptional service to IEEE and CPMT Society in various leadership roles and for his pioneering work in electrically conductive adhesives. An IEEE Fellow, Morris has served in many CPMT Society leadership positions over the years, including as an associate editor in adhesives for the IEEE Transactions on Component and Packaging Technologies.



· **Prof. I. Charles Ume** (Georgia Institute of Technology) - Outstanding Sustained Technical Contribution Award - for his contributions to thermomechanical reliability in electronic packaging. His inventions are helping to improve the quality and reliability of packaged microelectronic and electronic packaging products and pulp and paper products. He is an IEEE Fellow and serves as associate publisher of the IEEE Transactions on Components and Packaging Technologies.



· **Prof. Tseung-Yuen Tseng** (Chiao-Tung University, Taiwan) - Exceptional Technical Achievement Award - for his contributions to the applied technology and basic science in electronic ceramics, in particular to ceramic capacitors. His technical contributions have been documented in technical journal and conference papers, as well as several patents and book chapters. He invented the first base metal Z5U dielectric formulation adopted by the Philip Company and brought it into large-scale commercial use.



· **Ms. Lara J. Martin** (Motorola, Plantation, Fla., USA) - Outstanding Young Engineer Award for her contributions to electronic product development, manufacturing and reliability and for supporting CPMT Society activities and conferences. In the past five years, Lara has contributed publications to a dozen industry journals and conferences, as well as PC Fab magazine. At Motorola, Lara has made significant contributions to development and implementation of a new product reliability system based on next generation statistics. Lara holds two patents with another pending.



Paul Wesling, Vice President of Publications, presented **best paper awards:**

The 2004 IEEE Transactions on Components and Packaging Technologies Best Paper Award was for the article titled,



"Characterization of Hygroscopic Swelling Behavior of Mold Compounds and Plastic Packages" - Published in the September 2004 issue, authored by Eric Stellrecht (DRS Technologies, USA), Bongtae Han (University of Maryland, USA), Michael G. Pecht (University of Maryland, USA)



The 2004 IEEE Transactions on Advanced Packaging Best Paper Award was for the article, "Design of Integrated Low Noise Amplifiers (LNA) Using Embedded Passives in Organic Substrates" - published in the February 2004 issue Vinu Govind, Sidharth Dalmia, Madhavan Swaminathan (All authors from the Georgia Institute of Technology, USA)



And finally, the 2004 IEEE Transactions on Advanced Packaging Commendable Paper award was presented for the article titled, "The SOP for Miniaturized, Mixed-Signal Computing, Communication, and Consumer Systems of the Next Decade" - published in the May 2004 issue. It's large team of author includes Rao R.Tummala, Madhavan Swaminathan, Manos M Tentzeris, Joy Laskar, Gee-Kung Chang, Suresh Sitaraman, David Keezer, Daniel Giudotti, Zhaoran Huang, Kyutae Lim, Lixi Wan, Swapan K. Bhattacharya, Venkatesh Sundaram, Fuhun Liu, P. Markondeya Raj (All authors from the Georgia Institute of Technology, USA)



The Society's global chapters are a crucial link to the local communities. The 2005 **Chapter of the Year Award** went to West Ukraine Chapter, and the 2005 Student Chapter of the Year Award went to the University of Arkansas. Chris Thomason, Vice President; Matt Kelley, Secretary; and Colin Furrow, Treasurer were on hand to accept from the University of Arkansas.



The Society was also lucky to have two of our newest IEEE Fellows on hand. Phil Garrou presented certificates to **Paul Wesling and Bill Brown**, Strategic Director for Student Programs.



One award not presented at the luncheon was the Electronics Manufacturing Technology Award. The winner of that award is **Dr. Robert C. Pfahl, Jr.** (International Electronics Manufacturing Initiative (iNEMI), Herdon, Va., USA) - for developing new manufacturing processes, reducing the environmental impact of electronic manufacturing processes and fostering collaboration within the manufacturing technology community. Dr. Pfahl led and edited the first National Electronics Manufacturing Technology Roadmaps in 1994, and in 1996 helped champion the formation of the National Electronics Manufacturing Initiative (NEMI). Pfahl will receive the award at the International Electronics Manufacturing Technology (IEMT) Symposium, 11-13 July 2005 - held in conjunction with SEMICON West in San Francisco, California USA.

Do you have a colleague deserving of recognition? Visit [www.cpm.org/awards](http://www.cpm.org/awards) for nominations information and awards criteria.

-- submitted by Kristine Martin

## Lead-Free ECTC Panel

On May 31, an evening session Discussion was held entitled "Lead-Free Industry Update". With looming deadlines to remove 6 hazardous items from electronics in Europe and China, it was time to share progress. Robert Lanzone of Amkor Technology was the Chair.

**Raj Masters** of AMD first defined the details of the law that dictates Pb, Hg, Cd, and Cr6+ controls. For lead the exceptions are only those where no readily available option exist such as: high temperature attachment where Pb >85%, Pb in high end servers and communication equipment, Pb in many element alloys, Pb die attach in carriers that are flip. SnAg solders are being used to replace passive device lead attach and for BGA balls. In general, the greatest challenge is for the high reliability, long life time systems.



**Sudipta Ray** described the IBM Lead-Free Road Map. Although covered by exception today, IBM is developing a Lead-Free C4

bump and package. He discussed bumps of plated Sn/Ag or Sn/Cu as well as balls of 3-4% Ag and SAC alloys. In the case where long columns are needed, IBM is studying Cu columns with Sn/Ag solder coating.

**Han Park** discussed the Japanese market. The first step was to achieve lead-free solder paste over the 2000-2002 period. This demanded higher temperature reflow and much tighter profile control of the reflow oven temperatures. The second step has been lead-free terminals on the components. The last step will be full lead-free systems. Everything in the system must survive 260 C heating. There has been a change-over from wave soldering machines to high temperature processes.



Strongly suggested that more standardization should occur for the lead-free solders used throughout the world. Currently Japan supports Sn3Ag0.5Cu, NEMI Sn3.9Ag0.4-0.8Cu, and Europe Sn3.4-4.1Ag0.45-0.9Cu.

**Juergen Winterer** of Infineon indicated that 70% of their products are shipped lead-free today. They use Sn plating that is usually 7 microns thick and matte finish. They also use SnAgCu

for attaching BGAs. SnPb will only be used in niche technologies after 2006.



**Sherry Zhu** of Kyocera described changing solder processes in a way where some backward compatibility would exist in components. Today a complete shift is lost when converting a line from SnPb to Lead-free. Tools used for Pb must be segregated from the lead-free. They use SnAgCu #305, 405, 382. They change the part number to avoid confusion in the next assembly performed by their customers. They are busy applying six sigma methodology on the new solder processes. A point was made that the SnZn9% material has a very short shelf life and easily oxidizes.



**Robert Darveaux** of Amkor indicated that the material properties on the different solders are often much different than those mentioned in the literature. Some of this is due to the difference of measuring pure materials in "dogbones" versus solders in action forming interfaces, but much was just

the dependence of solder properties on preparation details that were often hidden from even the researcher. Bottom line: measure the properties you need under the conditions the materials actually encounter.

**Dongkai Shanggaun** of Flextronics indicated they had switched from R&D to operational focus. In particular, they were working the "end of life" issues such as cost of electronics recover, reuse, and recycling. He indicated that they test the reliability of their PCB after 6 cycles of 260 C processing. In general they used the SAC solders where Ag is 3-4% and had narrowed their process windows considerably. He pointed out that most SAC solders were not bound by IP.



## CPMT Seminar at ECTC--Advanced Circuit Board Technologies

**Yoshitaka Fukuoka** of Weisti chaired the CPMT Seminar on Thursday, June 2 evening. Five excellent detailed presentations were made on next generation flex circuit capability. Attendance exceeded 80 despite the excellent food and drinks in the overlapping reception.



**Masahiko Takeuchi** of Nippon Steel Chemical Co. discussed the details of the ESPANEX series M and L. Cost is kept low by using roll to roll manufacturing. The uptake of moisture is very low and thus the dimensional changes are small. The dielectric constant of the LCP film is 2.8, the dissipation factor is .0025, and the M-series is good to 25 GHz and L-series is good to 37 GHz. Via holes of 50 micron are possible.



**Yasuhito Oowaki** of Nitto Denko Corporation discussed Ultra-thin Flex. By using photosensitive polyimide they demonstrated 3 orders of magnitude more flex cycles than past flex materials.

**Yoshihisa Katoh** of CMK Corporation discussed Rigid-Flexible Circuit Board developments. The ability to let the flex provide connection rather than connectors allows designers to save much volume in consumer electronics. In addition, the resistance for a connection is often x10 lower. The advances are



being pushed by the automotive applications which demand 3200 cycles from -30 to +110 C.

**Masaaki Katsumata** of Panasonic Electronic Devices discussed the IVH Structure substrate. Of particular interest was their use of silver coated copper particles in a past to fill laser vias. The resistance of these vias showed no change in aging experiments.



**Koichiro Nakase** of NEC Corporation discussed thin-film embedded passives concentrating on the 1 GHz range. He showed many techniques to achieve high self-resonance frequencies, well above those of circuit operation.



**Craig Gaw** of Freescale leading a breakfast meeting of the RF and Wireless Technical Committee at this year's ECTC.

# International Electronics Manufacturing Technology (IEMT) Symposium: Theme: "Manufacturing at the Wafer Level"

July 11-12, 2005

Five Professional Development Courses

Moscone Convention Center & Marriott Hotel, San Francisco, California

## Executive Committee:

Visit [www.cpmt.org/iemt/](http://www.cpmt.org/iemt/)

Thomas S. Tarter, Neophotonics, General Conference Chair  
Brian Toleno, Henkel Technologies, Program Chair

## Description:

The IEMT is an international forum on electronic components and systems manufacturing technology. The conference is a joint effort of SEMI and the IEEE CPMT society. This year the event will address the topic: *Manufacturing at the Wafer Level*. The conference features invited talks by leading experts in this exciting area. Presentations focus on wafer-level packaging, including the use of underfill materials applied at the wafer level. Test is an increasingly important area for many applications, and the focus for the forum is on memory testing. The introduction of low-k dielectrics on the wafer presents its own set of assembly problems that are addressed at the seminar. A series of presentations will focus on system-in-package (SiP).

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## Future Directions in IC and Package Design Workshop, FDIP'05

organized by: CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

October 23, 2005 ---- Austin, Texas [www.epep.org](http://www.epep.org)

The goal of this workshop is to provide a forum to address the future needs associated with the design of next generation ICs and packages. The Technical Program Committee will solicit invited presentations from experts in the university and industrial communities. The workshop will be held in conjunction with the IEEE Topical Meeting on Electrical Performance of Electronic Packaging in order to enhance this conference with presentations that give directions for future requirements and developments in the area of electrical analysis and design. The workshop will foster active participation and discussions from all the speakers and attendees during the meeting.

### The following talks are planned:

Designing Servers In a Commodity World – Carl Anderson, IBM Corporation

Signal Interconnect Trends and Challenges Inside the CEC – George Katopis, IBM Corporation

High Volume Signal and Power Integrity Design for ASICs – Brian Young, Texas Instruments

Electromagnetic Field Visualization System for IC/Package Design Based on Optical Techniques – Mizuki Iwanami, NEC

Harnessing the Power of Parallel Computation on the IBM BlueGene/– Raj Mittra, Pennsylvania State University

Computational Electromagnetics for Circuits Simulations – the Challenges – Weng Cho Chew, University of Illinois

Workshop will be held at the Radisson Hotel & Suites Town Lake, 111 E. Cesar Chavez, Austin, Texas 78701 (512) 478-9611. They are holding a block of rooms at \$109.00 plus tax. Reservations must be made by September 30, 2005 in order to guarantee this rate. Be sure to mention that you are attending the EPEP conference in order to secure this rate. Additional information can be obtained at [www.epep.org](http://www.epep.org). Workshop chairs are Alina Deutsch ([deutsch@us.ibm.com](mailto:deutsch@us.ibm.com)) and Madhavan Swaminathan ([madhavan.swaminathan@ece.gatech.edu](mailto:madhavan.swaminathan@ece.gatech.edu))

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## 11th THERMINIC -- 27 - 30 September 2005 -- Lake Maggiore Italy

THERMINIC Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. These questions are becoming more and more crucial with the increasing element density of circuits packaged together and with the move to nanotechnology.

This year THERMINIC will address in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomena in "high-tech" systems.

The Workshop is sponsored by the IEEE Components, Packaging, and Manufacturing Technology Society, the IEEE Computer Society, Test Technology Technical Council and TIMA Laboratory in cooperation with the Thermal Committee of IEEE CMPT

<http://tima.imag.fr/conferences/therminic>

AREAS OF INTEREST include, but are not limited to, the following topics:

- Thermal and Temperature Sensors
- Thermal Simulation
- Electro-thermal Simulation
- Thermal Modelling and Investigation of Packages
- Reliability Issues
- High Temperature Electronics
- Heat Transfer Education
- Flow Visualisation Techniques
- Turbulence Modelling in Complex Geometries
- Defect and failure modelling
- Measurement of Thermal Properties
- Acquisition and analysis of Thermal data
- Temperature Mapping
- Novel and Advanced Cooling Techniques
- Thermal Performance of Interconnects
- Heat Transfer Enhancement
- Validation of Thermal Software
- Coupled (Thermo-mechanical, Thermo-optical, etc.) Effects.
- Thermal Stress: Theory and Experiment
- Reliability evolution and prediction
- Multiphysics simulation
- Nanoengineering issues
- Education
- Thermal Stress Failures: Prediction and Prevention
- Nanotechnology Applications



## EPTC 2005 Call for Papers - 2nd Notice

**7th Electronics Packaging Technology Conference (EPTC 2005) -- 7 - 9 December 2005, Singapore**

On behalf of the organising committee, it is our great pleasure to invite you to submit an abstract to the 7th Electronics Packaging Technology Conference (EPTC 2005), which will be held from 7 - 9 December 2005 at the Grand Copthorne Waterfront Hotel, Singapore.

EPTC 2005 aims to provide a good coverage of technological developments in electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field. Your abstract(s) may be in one or more of the following areas: Emerging Packaging Technologies

Interconnection Technologies	Manufacturing Technologies
Materials & Processes	MEMS Packaging
Electrical Modeling & Signal Integrity	Thermal Characterization & Cooling Solutions
Mechanical Modeling & Structural Integrity	Optoelectronics
Quality & Reliability	

Since its inauguration in 1997, the EPTC has developed into a premier electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world. The 6th EPTC in December 2004 featured 148 presentations from various parts of the world and was attended by some 260 participants from 26 countries. It is our sincerest wish to continue developing this conference series as the premier conference for the packaging industry in this region.

**for more information: [www.eptc-ieee.net](http://www.eptc-ieee.net)**

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<http://www.polytronic2005.org>

### **Polytronic 2005**

**The 5th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, October 23-26, 2005 in Wroclaw, Poland.**

The conference provides a unique opportunity for the meeting of polymer developers with polymer users from the electronics industries. Research paper presentations will cover all aspects of adhesives and polymers in microelectronics and photonics, including new polymers, organic devices, polymers in packaging, and adhesive applications.

Polytronic 2005 will be the fifth in the Conference series, begun in 2001 as an amalgamation of the previously successful series of IEEE Conferences on adhesives and polymers: Polymeric Materials for Microelectronic & Photonic Applications (POLY), Adhesives in Electronics, and Polymeric Electronics Packaging (PEP).

**The topics that will be covered include:**

**Materials:** Thermosetting/thermoplastic systems; inorganic adhesives; composites; filler materials; isotropic conductive adhesives; anisotropic conductive adhesives; underfill compounds; pastes and films; heat seal connectors; thermally conductive adhesives; polymers with adapted refractive index; photosensitive polymers; high temperature materials; PCB materials, polymer thick and thin films, low and high dielectric materials.

**Processing and Manufacturing:** Advanced packaging; lamination; printing; dispensing; spraying; transfer techniques; underfilling; potting; adhesion improvement; curing; equipment; statistical process control; economic analyses.

**Design and CAD:** Design, modeling, simulation, CAD of compounds and processes; thermomechanical behavior.

**Reliability and Testing:** Degradation mechanisms; adhesion; hermeticity; accelerated testing; humidity and environmental sensitivities; non-destructive testing methods; stress behavior.

**Functional Polymers for Microelectronics:** Conductivity of polymers; electronic transport; self-assembly; photoactivity; polymeric materials for molecular electronics.

**Applications:** Polymer electronic devices; polymer optical fibers; polymer wave guides; organic displays; polymer batteries; e-paper; flexible electronics.

**Environmental Issues:** Ecology and toxicology; life cycle analyses.

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ACS/MRS/IEEE CPMT

### **Organic Microelectronics Workshop**

**July 10 - 13, 2005 Newport, Rhode Island, USA**

**[www.organicmicroelectronics.org](http://www.organicmicroelectronics.org) phone 202 872 4600 email [acsprospectives@acs.org](mailto:acsprospectives@acs.org)**

The Workshop will bring together a broad spectrum of chemists, materials scientists, physicists, and engineers from both industry and academia in a stimulating forum to share information and ideas in the emerging field of Organic Microelectronics. The goal is to build an interdisciplinary community working on applications such as RFIDs, displays, sensors and photovoltaics while addressing some of the common scientific and manufacturing challenges to help these technologies advance in a more rapid, effective, and economical manner.

The technical program will focus on the areas of synthesis, theory, novel processing/ patterning/ fabrication and device physics through a series of presentations by renowned invited speakers and poster sessions.



## INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

COMPONENTS, PACKAGES AND  
MANUFACTURING TECHNOLOGY SOCIETY  
Components & RF Program Committee  
RF & Wireless Technical Committee



**ECTC 2006 – May 30 - June 2**  
**Sheraton San Diego Hotel & Marina**  
**San Diego, CA**

The CPMT RF & Wireless Technical Committee and the ECTC Components & RF Program Committee encourage you to submit an abstract to ECTC 2006 in the area of RF & microwave components & packaging technology. In particular, RF & microwave papers are solicited for focus sessions on “RF & Microwave Component-Like Modules” and “Integrated Passives for RF Applications” as described below. At ECTC 2005 the Components & RF program comprised 21 technical presentations in 3 focused sessions in addition to numerous related papers in other sessions.

### **“RF & Microwave Component-Like Modules”**

Emerging high-performance applications, such as WLAN, RF-optical networks & automotive radar have defined a trend toward flexible & reconfigurable systems. RF & microwave front-end modules are the foundation of these systems & their integration poses a great challenge. These components & modules require better performance, lower cost & increasingly smaller front-end size. Abstracts for papers are solicited in the area of “RF & Microwave Component-like Modules”. Topics may include:

- ◆ Auto radar, adaptive phased array antennas, filters, baluns, UWB (ultra wide band) modules
- ◆ High power & high efficiency RF/microwave power amplifiers & packaging
- ◆ Antennas integrated in compact RF/microwave modules, RFID
- ◆ Integrated transceivers for Zigbee, Bluetooth, DVB-H, ...

### **“Integrated Passives for RF/Microwave Applications”**

- ◆ Integrated de-coupling for RF/microwave, analog, digital & mixed signal applications
- ◆ Embedded passives (inductors, capacitors) for RF/microwave applications & evaluation of their performance in terms of Quality Factor (Q), component value, fabrication challenges & cost

We recommend that the technology used for each submitted paper be compared with competing technologies & evaluated in terms of advantages & disadvantages for the specific components.

### **SUBMISSIONS:**

Please submit abstracts using the ECTC web site: [www.ectc.net](http://www.ectc.net) by October 15, 2005. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the “Components & RF” focused sessions on RF & microwave topics, **YOU MUST SELECT**

### **“Components & RF” committee as your PRIMARY subcommittee preference**

when you submit your abstract at the ECTC web site. Again, to have your paper considered for the RF & microwave components sessions, please do the following:

- STEP #1: Submit abstract through the ECTC web site ([www.ectc.net](http://www.ectc.net)) and select **“Components & RF” as PRIMARY subcommittee preference**
- STEP #2: Email abstract copy and author’s email & contact information to:  
Craig Gaw at [c.a.gaw@ieee.org](mailto:c.a.gaw@ieee.org) & Li Li at [L.Li@freescale.com](mailto:L.Li@freescale.com)

# 7th International Conference on Electronics Materials and Packaging (EMAP 2005)

December 11-14, 2005, Tokyo Institute of Technology, Japan

## Announcement and CALL FOR PAPERS



The 7th International Conference on Electronics Materials and Packaging will be held at Tokyo Institute of Technology, Japan. The former six conferences were held in Singapore (1999), Hong Kong (2000), Korea (2001), Taiwan (2002), Singapore (2003) and Malaysia (2004) all of which were successful and have gained a reputation as a premier electronics materials and packaging conference in Asia Pacific where the bulk of the packaging activities are taking place.

The purpose of the conference is to promote awareness of new advances in materials, design and simulations, fabrication, reliability, and thermal management of microsystem/MEMS packages. This will also provide an excellent opportunity for researchers and engineers to gather to discuss generic and practical applications and new directions.

The organizing committee seeks original papers that demonstrate how new technologies and applications are expanding and redefining the international role of microelectronics. Contributions are very welcome from industry participants and researchers from academic institutions. The topics of interests are specific to micro systems/MEMS, their packaging, electronics materials and reliability issues. Papers are being sought from, but not limited to, the following subjects:

- Automotive Electronics
- Chip-Scale Packaging/Flip Chip
- Electrical Modeling & Signal Integrity
- Electronic Inspection
- Green Materials
- High Density Displays
- High Density Packaging
- Interconnection Technologies
- Low Cost Packaging Methods
- Manufacturing Technologies
- Mechanical Modeling and Structural Integrity
- MEMS Packaging and Applications
- Microelectronic Materials & Processes
- No Flow Underfilling Process
- Optoelectronics/Photonics
- Polymer Materials & Microelectronic Applications
- Printed Wiring and Flex Boards
- Quality & Reliability
- Thermal Design, Analysis, and Characterization
- Thick & Thin Film Materials

- Wafer Scale Packaging
- Wireless Sensor Packaging & Applications
- Vibration on Electronic Devices

### SECRETARIAT

All inquiries concerning the conference should be addressed to:

Prof. Satoru AIHARA, Secretary General of EMAP2005  
EMAP2005 Secretariat (I1-36)  
Tokyo Institute of Technology  
2-12-1 Ookayama, Meguro-ku, Tokyo 152-8552, JAPAN  
Phone & Fax: +81-3-5734-2532  
E-mail: info@emap2005.sms.titech.ac.jp

### Conference Information & Contacts

Website: <http://www.sms.titech.ac.jp/emap2005>

### IMPORTANT DATES

**Submission of Abstract: June 30, 2005**

**Notification of Acceptance: July 31, 2005**

**Submission of Manuscript: September 30, 2005**

### EXTENDED ABSTRACT AND PAPER SUBMISSION

Extended abstracts are invited to describe original and unpublished work. The extended abstract should be about 500 words starting clearly the purpose, methodology, results and conclusions of the work. Key references to prior publications and how the work enhances the existing knowledge should be included in the extended abstract. Authors are requested to designate appropriate areas for the purpose of abstract review. All submissions must be in English and should be made via the conference web site. The required file format is either MS Word or Adobe Acrobat PDF with only one single file for each submission.

### SELECTION OF PAPERS

The Technical Committee of the 7th EMAP will select papers with quality and originality for presentation at the Conference and for publication in the Conference Proceedings. Only papers of those authors who have paid the registration fee and intend to attend the Conference will be published in the Conference Proceedings (Author Registration).

### CONFERENCE SCHEDULE

Sunday, December 11	Registration and welcome drink (evening)
Monday, December 12	Keynote Lectures
Tuesday, December 13	Keynote Lectures Technical Sessions Banquet/Student Reception
Wednesday, December 14	Technical Visit (full day)

### COMMITTEE

General Chair: Prof. Kikuo KISHIMOTO  
Tokyo Institute of Technology, Japan

Co-Chairs

Prof. Mikio HORIE	Tokyo Institute of Technology, Japan
Dr. Takashi KAWAKAMI	Toshiba Corporation, Japan
Prof. Noriyuki MIYAZAKI	Kyoto University, Japan

# 14th Topical Meeting on Electrical Performance of Electronic Packaging

## EPEP 2005

October 24-26, 2005  
Austin, Texas



### Sponsors

The IEEE Components, Packaging and  
Manufacturing Technology Society

IEEE Microwave  
Theory and Techniques Society

## Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

- Current and future issues related to on-chip interconnections
- Router friendly models and modeling tools: accuracy & efficiency
- Modeling and design of high speed digital IO circuits: signal propagation and reception
- On-chip power delivery and regulation
- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
- Power distribution and package resonance
- Long distance propagation in large switching complexes
- Switching noise in multi-layered systems
- Macromodeling techniques
- Signal integrity in mixed signal integrated circuits
- Electrical issues in MEMS packaging
- New and innovative interconnect packaging structures and their electrical performance
- RF/microwave packaging structures and their electrical performance
- MMIC modules and high density packaging
- Experimental characterization techniques
- EMC/EMI sources & effects
- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for one chip radios: design and modeling
- Performance of packaging for automotive radar systems

**Conference Co-chairs:** Robert W. Jackson, University of Massachusetts; Moises Cases, IBM

**Conference Web Page:** Detailed information can be found at [www.epep.org](http://www.epep.org)

**Paper Submission:** Information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 9, 2005**.

**Student Paper Award:** Two awards will be presented to the best two papers submitted by students

**Short Courses/Workshops:** On Sunday, October 23, 2005, a workshop entitled "**Future Directions in Packaging**" will be presented and short courses/tutorials will be offered.



# CALL FOR PAPERS

**Abstract Submission:** Please send your title and 300-word abstract, electronically, to [nbep@ece.gatech.edu](mailto:nbep@ece.gatech.edu) by **October 14, 2005**. For further info, please visit [www.prc.gatech.edu/nanobiopack](http://www.prc.gatech.edu/nanobiopack)

Third International Workshop on

March 20-22, 2006

## Nano & Bio-Electronic Packaging

**Georgia Institute of Technology**  
Technology Square Research Building  
[www.gatech.edu/technology-square](http://www.gatech.edu/technology-square)

### General Chairs

Prof. Rao Tummala ([rao.tummala@ee.gatech.edu](mailto:rao.tummala@ee.gatech.edu)), Director,  
Packaging Research Center - Georgia Institute of  
Technology

Prof. Z. L. Wang ([zhong.wang@mse.gatech.edu](mailto:zhong.wang@mse.gatech.edu)), Director,  
Center for Nanoscience & Nanotechnology - Georgia  
Institute of Technology

### Technical Chair

Prof. C.P. Wong ([c.p.wong@mse.gatech.edu](mailto:c.p.wong@mse.gatech.edu)) - Georgia  
Tech PRC (Others to be determined.)

**Conference Coordinator:** Dr. Swapan Bhattacharya  
([swapan@ee.gatech.edu](mailto:swapan@ee.gatech.edu)) - Georgia Tech PRC

### International Planning Committee

Avi Bar-Cohen ([abc@eng.umd.edu](mailto:abc@eng.umd.edu)), University of  
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Karl Becker ([becker@jzm.fhg.de](mailto:becker@jzm.fhg.de)), Fraunhofer Institute of  
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of Singapore

Michael Wahl ([michael@rs.uni-siegen.de](mailto:michael@rs.uni-siegen.de)), Universitat  
Siegen

### SHORT COURSES

March 20

**Half day course on Nano Packaging**  
Prof. C. P. Wong & Rao Tummala

### PLENARY SESSION

March 21

**Half day of keynote addresses from  
renown guests**

### TECHNICAL SESSIONS

March 21-22

#### Nano Biomedical Packaging

Jorma Kivilahti - Helsinki University of Technology

Roger Narayan - Georgia Institute of Technology

#### Nano Photonics

Avi Bar-Cohen - University of Maryland

Ali Adibi - Georgia Institute of Technology

#### Nano Packaging Materials

Goran Matijasevic - University of California

C. P. Wong - Georgia Institute of Technology

#### MEMS, NEMS & Sensors

Farrokh Ayazi - Georgia Institute of Technology

Ajay Malshe - University of Arkansas

#### Nano Interconnections

Andrew Tay - National University of Singapore

#### Nano Thermal Interfacing Materials

William Chen - ASE Inc.

Srinivas Rao - Solectron

#### Packaging of Nano Cu-Low K

G.Q. (Kouchi) Zhang - Philips Semiconductors

### INFORMATION UPDATES

[www.prc.gatech.edu/nanobiopack](http://www.prc.gatech.edu/nanobiopack)



An  
IEEE workshop  
sponsored in  
cooperation  
with the  
IEEE-CPMT  
Society, iNEMI  
and the  
Georgia Tech  
Packaging  
Research  
Center



iNEMI





# Institute of Electrical and Electronics Engineers, Inc. Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter  
&  
Waves and Devices Chapter

## PRESENT AN ALL-DAY WORKSHOP ON Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

**Date:** Thursday, November 10<sup>th</sup>, 2005 **Time:** 7:00 A.M. – 5:00 P.M.  
**Location:** Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

### Abstract

The one-day workshop will focus on device, interconnect and packaging challenges for next generation computing and communication applications. Participants will hear from leading contributors from industry, academia and the national labs. Long-range technology roadmaps will be reviewed and state-of-the-art processor, memory, and mixed-signal technologies will be addressed. Chip, package, and board-level interconnect issues will be discussed. Key materials, process, and performance challenges for physically realizing the required devices, interconnects and packaging will be presented. Market trends in computing and communications are within the scope of the workshop as well. A panel discussion on the future of computing and communications will bring closure to the day's workshop. Vendors representing the entire supply chain of chip, package, and board will display their products and services.

### Topics

- **System & Architecture:** Future computing approaches (local vs. net-centric, personal & server computer); convergence of computing and communication; advances in processor technology such as multi-core, high-bandwidth buses and advanced drivers/receivers; memory/processor integration; SoC partitioning, modeling, and testing challenges/issues.
- **Materials & Processing:** ITRS roadmap for CMOS technology; Moore's law/prognosis in the context of the next few technology nodes; BEOL processing (low-k/Cu, ultra low-k/Cu); advances in memory technologies.
- **Simulation & Modeling:** Simulation for advanced devices; EM simulation in RF circuit/module/package design; signal noise analysis for SoC.
- **Advanced Packaging:** New packaging technologies, especially flip-chip, lead-free, 3D interconnect, multi-chip, and RF modules.
- **Special Topics:** Signal integrity; power delivery and distribution; cooling/thermal management.
- **Panel discussion on the future of computing and communications.**

**Vendor Displays**

Vasu Atluri (480) 554-0360	Bishnu Gogoi (480) 413-8836	Mali Mahalingam (480) 413-5368	Ravi Sharma (480) 792-7920
Rao Bonda (480) 413-6121	Steve Goodnick (480) 965-6410	Mel Miller (480) 413-6111	Chuck Weitzel (480) 413-5906
Henning Braunisch (480) 552-0844	Rashaunda Henderson (480) 413-5374	Sujit Sharan (480) 552-8073	Dragan Zupac (480) 413-3964

For General Information:  
<http://www.ieee.org/phoenix>

For Workshop  
Registration Forms: **Ellen Lan**  
(480) 675-5283

For Vendor  
Registration Forms: **Sam Karikalan**  
(480) 222-1722



# ELECTRICAL DESIGN OF ADVANCED PACKAGING AND SYSTEMS (EDAPS)

4<sup>th</sup> Asian Workshop

12 and 13 December (Monday and Tuesday) 2005, Bangalore, India

Windsor Manor Sheraton & Towers, 25 Sankey Road, Bangalore 560052

## Objective

The EDAPS Workshop is to enhance the technical awareness in the Asia region specifically in area of package and system electrical design concepts, issues and challenges ahead for next generation electronic products.

## International Advisory Committee

Alina Deutsch : IBM Corp., USA  
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Andreas Weisshaar : Oregon State Univ., USA  
Ching Chao Huang : Rambus, USA  
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Robert Jackson : Univ. of Massachusetts, USA  
Tawfik Arabi : Intel Corp., USA

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**Co-chairs** – Mahadevan Iyer, IME, Singapore

Joungho Kim, KAIST, Korea

Toshio Sudo, Toshiba Corp., Japan

PR Patel : Intel Pvt. Ltd., India

NJ Rao : Indian Inst. Of Science, India

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SLN Murthy : ECAD Tech. Ltd., India

Karunakaran S : SAMEER, India

Arun Chandrasekhar : Intel Pvt. Ltd., India

Manish Rawat : Wipro Tech., India

Parthasarathy Ramaswamy: Intel Pvt. Ltd., India

G Ananda Rao : Indian Inst. Of Science, India

Rajkumar : Texas Instruments, India

Anil Kumar M : SLN Tech. Pvt. Ltd.

MK Gunasekaran: Indian Inst. Of Science, India

## Joint Organisers



## Technically sponsored by:

IEEE CPMT TC-12 Subcommittee on Electrical Design, Modelling and Simulation

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URL: <http://ewh.ieee.org/r10/bangalore/cpmt/events.html>

# First International Workshop on 3S Electronic Technologies

September 22 & 23, 2005

Global Learning & Conference Center at  
Technology Square

84 Fifth Street, Atlanta, GA, 30308 USA

**General Chair:** Prof. Rao R Tummala, Director GT-PRC

**Technical Chairs:** Erich Klink (IBM) & Evan Davidson (IBM-ret)

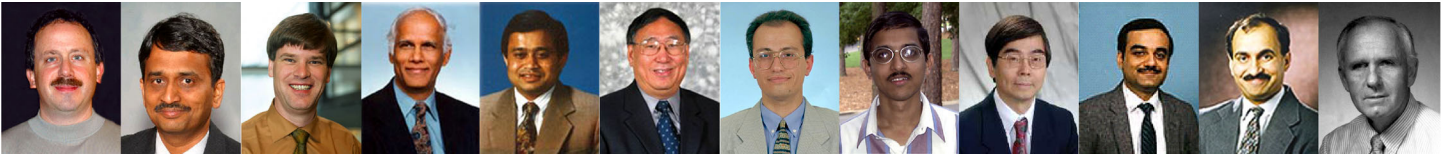
**Program Coordinator:** Boyd Wiedenman  
boyd.wiedenman@ece.gatech.edu



## CALL FOR ABSTRACTS

**Due June 15, 2005**

Send abstracts (300 words or less) to Boyd Wiedenman:  
boyd.wiedenman@ece.gatech.edu



Packaging of electronics is no longer making discrete components and interconnecting them, since it leads to bulky, costly and low-performance and low-reliability systems. The new and emerging paradigm is about package and systems integration enabled by thin film component integration leading to ultra miniaturized, lower cost, higher performance and higher reliability systems. This Package integration is taking place every where—at IC level, package or module level and at system level. At IC level, it is by means of a package overlay on CMOS; at module level, it is by means of SIP; and at system level, it is by means of SOP. The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market, system-driven, IC-package-system co-design flow. The advantages of the SOP and SIP paradigms that are based on package integration appear overwhelming due to their design simplicity, lower cost, higher system integration and electrical performance, without the intellectual property issues that dominate SOC. While package integration is common, SOP and SIP are different. The 3D packaging is typically the stacking of similar or dissimilar chips. The SIP goes one step beyond by stacking packaged components leading to sub-system modules. The SOP is the ultimate 3D integration of thin film components at IC, package and system levels leading to heterogeneous digital functions.

This workshop reviews the latest R & D and manufacturing status of each of these 3 “hottest” electronic technologies around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.

### Keynote Speakers

**System-In-Package (SIP)** - Ken Brown, Mgr. Non-CPU Packaging (Intel)

**System-In-Package Roadmap** – Joe Adams (Sky Works)

**System-On-Chip (SOC)** - Mahesh Mehendale, TI Fellow (TI)

**Wafer Level SIP** - Pieter Hooijmans, V.P. & RF Program Mgr. (Philips)

**SOCs with 3D Interconnects** – Bernie Pogge, IBM Fellow (IBM)

**System-On-Package (SOP)** - Rao Tummala, Director (GT PRC)

### Sessions/ Chairs

**Mixed Signal Design & Tools** - Madhavan Swaminathan (GT PRC)

**Embedded Optical Integration & Modules** - Gee-Kung Chang (GT PRC) & Ray Chen (University of Texas)

**Embedded RF Integration & Modules** - Manos Tentzeris (Georgia Tech PRC)

**SOP Fabrication in Ceramics vs. Organics** - Venkatesh Sundaram (Georgia Tech PRC)

**Wafer Level Assembly** - C. P. Wong (GT PRC) & Dr. Luu Nguyen (National Semiconductor)

**Mixed Signal Electrical Test** - Abhijit Chatterjee (GT PRC)

**Mixed Signal Package Reliability** - Suresh Sitaraman (GT PRC)

**SIP** – Joe Adams (Sky Works) & George Conner (Philips)

**Embedded Actives & Passives** – Dr. Mahadeva Iyer (IME, Singapore)

### Panel Discussion

**SOP vs. SIP vs. SOC** – Rao Tummala

Online registration & program updates:

[www.prc.gatech.edu/3s](http://www.prc.gatech.edu/3s)

