Components, Packaging, and Manufacturing Technology Society

Newsletter

The Global Society for Microelectronics Systems Packaging

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President's Column…..

Dr. William T. Chen
IEEE Fellow
President, IEEE CPMT Society
Santa Clara, CA, USA
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Greetings!!!

ECTC 2007

ECTC 2007 in Reno Nevada came and went very fast. For me personally it started with the 2007 ITRS Assembly and Packaging Working Group meeting on Tuesday morning May 28th , (the same day as the PDC courses and Tin Whisker Workshop). The week ended with the CPMT Board of Governors Meeting on Saturday June 2nd. Of the three exciting ECTC days in between, there were the Technical Committee meetings starting bright and early at 7:00 am (and one Transactions editors meeting at 6:30 am), and three Panel Sessions ending around 9:30 pm and 10:00 pm. In between were the parallel technical paper sessions, poster sessions, technical exhibits, and more committee meetings. The coffee breaks, lunches and dinners provided great opportunities to meet people and exchange gossip. I saw friends and colleagues from all over the globe. For me ECTC has always been a celebration, a celebration that unites people from diverse disciplines and geographies to share their discoveries, knowledge and data, triumphs great and small with their peers from all over the world.

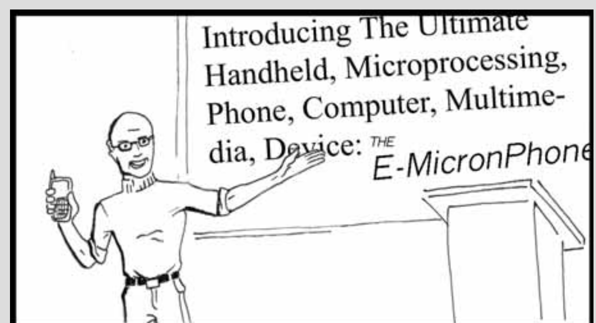
Unscientific Survey

I took an unscientific and incomplete survey. I asked some ECTC attendees for their comments on the technical programs. Almost to a man (or woman) they said that the technical program was outstanding. There were the complaints that parallel sessions made it perplexing as to which paper and what session to attend. They particularly liked the three evening panel sessions. (For the sake of full disclosure, I chaired one of the sessions.) For me the top prize must go to Technical Committee - HDSB for their 3D Packaging Panel held between 8:00 pm to 10:00 pm drawing a room full capacity crowd. The comments on the quality, relevancy, and timeliness of the technical papers were unequivocal. My thanks go to Eric Perfecto, Rao Bonda, and their technical program committees for their tireless efforts and dedication.

(Continued on Page 3)

Cartoon of the Month:

Fine Line between Product Success and Failure



… By Dave Palmer

IEEE CPMT Society Newsletter

June, 2007

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Chapters and Student Branches

Refer to www.cpmt.org for CPMT Society Chapters and Student Branches list

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2007 Deadlines for Submitting Articles:
August 25th, 2007
November 25th, 2007
Members-only Web (www.cpmt.org/mem/)
UserName: [available to Members --
Password: join CPMT!]

President's Column (Continued from Page 1)

Awards & Recognition

A highlight of ECTC has always been the CPMT lunch where IEEE and CPMT recognized exceptional individuals in our midst for their major and significant contributions to our profession and our society. I had the honor to present the IEEE CPMT Field Award to Dimitry Grabbe for his many contributions to advanced printed circuit board technology and connector technology in a professional career of over a half century. I was also privileged to share the podium with Dr Kitty Pearsall, CPMT Strategic Director for Awards and Recognition, to present this year's CPMT Society Awards for contributions and achievements. The list of award recipients and corresponding citations appear elsewhere in this newsletter. Last but not least, we recognized those members in our midst who have attained the highest membership level as an IEEE Fellow this year. The award winners and Fellows comprise a group of extraordinary professionals. Each in his/her own way has contributed much to our profession. And it is important that we recognize our own in major CPMT conferences, including ECTC, EPTC, ESTC, EMAP, IEMT and many others.

Winds of Change

If one should ask me, what were the over-riding impressions that I carry with from ECTC 2007, I would say they are the accelerating pace of technology change, and perhaps equally important, an expanding mindset welcoming change among the participants. The winds of change are gale winds blowing strong.

The traditional perspective of the roles of the packaging engineer is (a) make electrical interconnects and maintain off-chip signal integrity, (b) keep the IC and package temperature in check, (c) keep the IC and package from breaking down over its service life. Moore's Law drives the industry front-end for timed invention, innovation and their implementation. With the waves of SiP, wafer level packaging and 3D packaging technologies coming to the front, the roles of packaging engineers are taking on new dimensions. On the one hand the advancements of WLP and TSV are breaking down the walls between the foundry and packaging. On the other hand the forces unleashed by SiP technologies lead directly to system integration and electronic product realization. In this world of electronics industry the walls between the supply chains are fast vanishing. Are we ready for the challenges and opportunities presented by the advancing and sometimes disruptive technologies and evolving industry business model.

A Safe Harbor

In this fast-changing world of shifting opportunities, the global IEEE/CPMT community is becoming a safe harbor for relevant knowledge, technology innovations, life-long education, global networking, and peer recognition. I would like to invite you to participate in other CPMT conferences and workshops in different regions world-wide. There is still time for abstract submissions and technical exhibitions. They are great opportunities for technical vitality and building your personal networking within those regions. At the Board of Governors workshop last week we asked the Regional Strategic Directors to co-ordinate participation from publications, technical committees and membership at CPMT related conferences and workshops. I am confident that they will be working enthusiastically towards those ends.

Do go to the CPMT Web Page to see which technical conferences are of professional interest. Check out the Transactions for the latest developments in your field. Volunteer to be a speaker at your local chapter meeting. The Transactions editors would welcome your contributions as authors and reviewers. Tell your colleagues about CPMT and invite them to join.

A vital global CPMT Society is of benefit to everyone, especially today.

CPMT Society News:

IEEE Components, Packaging and Manufacturing Technology Society Board of Governors Meeting June 1st – 2nd, 2007 Reno, Nevada, USA

Report

Submitted by Ms. MarshaTickman, Executive Director, IEEE CPMT Society

The IEEE CPMT Society Board of Governors held its first meeting of 2007 on 1st and 2nd June 2007 in Reno, Nevada, USA, following the 57th ECTC.

The meeting began on Friday evening, 1 June 2007, with the third in a series of workshops allowing for informal discussion on strategic issues. This workshop continued discussion on creating global communities to serve members of our profession – and methods and strategies to achieve this. Topics included: defining the CPMT Society value propositions, breaking down silos within Society activities and building linkages, creating/utilizing a Regional organization.

On Saturday 2 June 2007, the Board of Governors meeting was called to order at 8:30 am. The following actions were taken:

- Approved minutes of the November 2006 Board of Governors meeting.
- Ratified actions approved via e-mail ballot between the November 2006 and current Board of Governors meetings.
- Approved employing additional staff to support the Transactions Editors and improve review process cycle time.
- Approved change in cosponsorship for the International Electronics Manufacturing Technology Symposium (IEMT): 50% CPMT Santa Clara Valley Chapter; 50% CPMT Society.
- Approved change in cosponsorship for the Organic Microelectronics Workshop: 25 % American Chemical Society, 25% Materials Research Society, 25% American Physical Society, 12.5% Solid-State Circuits Society (IEEE), 12.5% CPMT.
- Approved change in cosponsorship for the International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces (APM'07): 50% CPMT Santa Clara Valley Chapter; 50% CPMT Society.
- Approved new 100% Sponsorship of the International Workshop on Advances in Sensors and Interfaces (IWASI).
- Approved new Technical Cosponsorship w/fee of the 2007 Workshop on 3D Integration.

- Approved new Graduate Fellowship of $10K with $5K travel support to begin in 2008; modeled after the Motorola/IEEE CPMT Graduate Fellowship.
- Approved Johan Liu as a CPMT Distinguished Lecturer.
- Approved George Harman as a CPMT Distinguished Lecturer.
- Approved appointment of Eric Beyne as Strategic Director, Region 8.

Reports were presented as follows:

- CPMT President's Vision for CPMT Society
- Finances
- Publications
- Transactions
- Conferences
- Region 10 Activities
- ECTC Integration/57th ECTC
- Education
- Nominations
- Fellows Evaluation
- Fellows Search
- Constitution and Bylaws
- Technical Programs
- Region 8 Programs
- Membership and Chapters
- Student Programs
- Awards and Recognition
- Marketing

The next meeting of the CPMT Board of Governors is scheduled for 9-10 November 2007 following the ECTC Paper Selection Meeting, Dallas, TX, USA.

The meeting was adjourned at 4:30 pm.

Board of Governors Workshop Summary

Submitted by Dr. Dave Palmer, IEEE Fellow, Sandia National Laboratories

CPMT President William Chen held the third workshop for the Society Board of Governors on Friday, 1st June 2007, evening in Reno right after the ECTC. A few "new" members were introduced: Petri Savolainen, Kitty Pearsall, Paul Franzon, Eric Beyne, and Philip Chan.

The President quickly reviewed the results of the first workshop where each of the thrusts of our Society (publications, conferences, technical committees, education programs, chapter and membership development, and awards and recognition) were reviewed with the "value proposition" perspective to see how to enhance the impact for our members and our profession.

The second workshop addressed the Society's efforts at Globalization to serve the more geographically dispersed members. A few potential chapter areas (high member density) have been chosen to concentrate our effort: Ottawa, Austin, Germany, Norway, Japan, Malaysia, and Korea.

Much discussion was on the attempt not to let the good work of various parts of the Society to be limited within their own Silo (stovepipe). For example, the great organization of ECTC does feed into Chapter development, publications (best papers are fed into the Transactions input), technical committee growth (TCs meet at breakfast meetings), and awards (given at luncheons). However not all of our activities are this synergistic.

Several topics were discussed in some detail including publications enhancements such as shortening time to print and eliminating laggard manuscripts. Linking publications to specific conferences and expanding our stakeholders by adding authors, editors, and reviewers for the Transactions were examples of using publications as a catalyst for the Society.

Dimitry Grabbe Presented IEEE Technical Field Award for Components, Packaging and Manufacturing Technology

Submitted by Ms. Jacqulyn Hampton, Potomac Communications Group

- *Dimitry Grabbe awarded IEEE Technical Field Award for Components Packaging and Manufacturing Technology - Award is one of the highest honors conferred by the IEEE*
- *Grabbe's contributions have played an integral part in advancing U.S. space exploration*

PISCATAWAY, N.J., June 14, 2007 - Dimitry Grabbe was presented the IEEE Technical Field Award for Components, Packaging and Manufacturing Technology on May 31 during the 57th Electronic Components and Technology Conference in Reno, Nev. USA. Grabbe was recognized for his contributions to the fields of electrical/electronic connector technology and development of multi-layer wiring boards. The award is part of the Technical Field Awards program and is sponsored by the IEEE Components, Packaging and Manufacturing Technology Society. It recognizes commendable contributions to the advancement of components, electronic packaging or manufacturing technologies.

"There are very few engineers who have made as many contributions to advancing electronic and optoelectronic connectors and associated technologies," said Grabbe's peer who nominated him for the award. "For the last fifty years, Dimitry has been a leader in creating new products and new manufacturing approaches that have accounted for many significant improvements."

Dr. William T. Chen, President of the IEEE CPMT Society noted, "Mr. Grabbe is a brilliant individual whose efforts in electrical/electronic connector technology and the development of multi-layer wiring boards has contributed to major advancements in this industry."

Grabbe currently assists in research on gyroscopes and accelerometers with Dr. Pryputniewicz, professor of mechanical engineering and founding director of the Center for Holographic Studies and laser micro-mechaTronics at Worcester Polytechnic Institute in Mass.

Highlights from Grabbe's career:

- Pioneered work that has produced nearly 500 U.S. and foreign patents covering machine design, semiconductor packaging, electronics assembly and optoelectronic conductor design.

- His work in printed circuit board technology for electronic packaging led to the development of large, multi-layer printed circuit boards. This was crucial in helping U.S. astronauts gain greater real-time control of their space exploration activities.
- Founded the Maine Research Corporation which specialized in high-end printed circuit boards in 1964.
- Worked for AMP, Inc. and facilitated the organizations leadership in electrical/electronic connector technology, test socket technology and miniature semiconductor packages starting.
- Received the Leonard da Vinci Award from the American Society of Mechanical Engineers.
- Recognized by AMP (now part of Tyco Electronics) with a Lifetime Achievement Award.
- Named an IEEE Life Fellow.

Past recipients of the IEEE Technical Field Award for Components, Packaging and Manufacturing Technology:

2006 - C. P. Wong, Regent's Professor at Georgia Institute of Technology, Atlanta, Ga. For contributions in advanced polymeric materials science and processes for highly reliable electronic packages.

2005 - Yutaka Tsukada, Managing Director/General Manager of Advanced Packaging Technology Development, Kyocera SLC Technologies Corporation, Shiga-Ken, Japan. For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process.

2004 - John W. Balde, Senior Consultant, Interconnection Decision Consulting, Flemington, N.J. For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing.

About the IEEE Technical Field Award for Components, Packaging and Manufacturing Technology

The award was first presented in 2004 and may be presented to an individual or a small team involved in device and systems packaging, including packaging of microelectronics, optoelectronics, RF and wireless and micro-electro-mechanical systems (MEMS).

Nominations are encouraged for next year's CPMT Field-Award; contact Len Schaper for details: schaper@uark.edu

IEEE CPMT Society Honors 2007 Award Winners

Submitted by Ms. Jacqulyn Hampton, Potomac Communications Group

- *Awards presented during the 57th Electronic Components Technology Conference (ECTC) in Reno, Nevada, USA*
- *Georgia Institute of Technology faculty members receive two of six awards.*
- *Winners represent the depth and diversity of CPMT's global community of professionals*

Piscataway, N.J., June 11, 2007 - The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) recognized its 2007 award winners at the 57th Electronic Components and Technology Conference (ECTC) in Reno, Nevada, USA on May 31, 2007. William T. Chen, CPMT Society president, presented the awards during the annual awards luncheon in front of an audience of more than 800 conference attendees. The Society gives these awards for distinguished performance in technical fields and dedication to the Society and profession.

"It is with great honor that I am able to present these awards to such fine recipients," said William T. Chen, President, CPMT Society. "Their exceptional contributions to the fields of components, packaging and manufacturing technology should be celebrated by all in this profession."

"It is these achievements that allow our industry to grow and thrive."

- **Rao R. Tummala** (Georgia Institute of Technology, USA) – *IEEE CPMT David Feldman Outstanding Contribution Award* – for the breadth of his contributions to the CPMT Society in numerous leadership roles, as well as their global impact; including his unprecedented two terms (four years) as CPMT Society President. This award is presented to recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.

Tummala served as the CPMT Society President from 2000 - 2003. In this role he was responsible for revolutionizing the Society and identifying a number of critical and strategic needs. During his time in office he was able to expand the society by assisting in the formation of several Student Chapters and the creation of a number of CPMT Society Chapters throughout the world.

In addition to his work for the CPMT Society, Tummala is a successful industrial technologist and academician. He was named an IBM Fellow and served as the Director of the NSF Centers in Packaging. He has received many industry and academic awards including one of the Stars in U.S. for industry competitiveness and multiple awards from IEEE, IMAPS, I-ASM., SME, DVM and AM, Ceramic Society. He was named as a Distinguished Alumni from the University of Illinois and the Indian Institute of Science in Bangalore. He also received the highest faculty award from the Georgia Institute of Technology, the Class of 1934 Distinguished Professor Award.

- **Philip Garrou, Ph.D.,** (Cary, North Carolina) – IEEE CPMT *Outstanding Sustained Technical Contribution Award* – for 25 years of technical contributions and leadership in thin film dielectric materials and microelectric applications including multichip modules, bumping and wafer level packaging, integrated passives, oLEDs, and most recently 3D IC integration. This award is presented to an individual who has demonstrated outstanding sustained and continuing contributions to the technology fields encompassed by the CPMT Society.

As well as his more than two decades of service to the CPMT Society, Dr. Philip Garrou, is a global technical expert in thin film dielectric, or BCB. In the late 1980s there were several polymer dielectrics being used by several U.S. and Asian companies that were attempting to compete with the incumbent polyimide materials. Under Dr. Garrou's leadership,

BCB was the only product that made significant advancement in the field of thin film dielectrics. Dr. Garrou worked with universities such as Georgia Tech, University of Arkansas and Linköping University, various institutes and large R&D operations at corporations such as Motorola, AT&T, Bell Labs, Nortel, Trinquint, NEC, Sumitomo Bakelite, ST, Simens, Amkor and ASE to discover and publish new applications that were enabled by the use of thin film polymer.

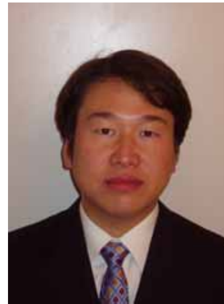
- **Chin C. Lee, Ph.D.,** (University of California - Irvine, USA) – IEEE CPMT *Exceptional Technical Achievement Award* – for his pioneering contributions to fluxless soldering and bonding technology. This award recognizes an individual for exceptional technical achievement in the fields encompassed by the CPMT Society.

With more than 25 years of experience, Dr. Chin C. Lee has pioneered research in diversified topics such as materials science, electronic packaging, manufacturing, thermal measurement and management, acoustic microscopy, integrated optical devices, electronics, semiconductor devices, and microwave theory. He developed a fluxless process that eliminates the root of flux requirement in soldering processes. It thus prevents oxidation from the beginning to the end of the entire process – from solder manufacture to the finish of the soldering process. In addition to his work with fluxless soldering and bonding technology, Dr. Lee was elected as the Director of the School-wide Interdisciplinary Materials and Manufacturing Technology Graduate Program at UC-Irvine. This is one of the few existing programs for manufacturing technology. In this role he expanded the faculty to 25 members and added courses to enhance the manufacturing technology curriculum.

- **Herbert Reichl, Prof. Dr.-Ing. Dr.-Ing. E.h.,** (Fraunhofer IZM, Germany) – IEEE CPMT *Electronics Manufacturing Technology Award* – for his outstanding contributions in research and education in the field of microelectronics packaging and for his pioneering role in the integration of reliability aspects. This award is presented to an individual who makes major contributions to Electronic Manufacturing Technology in the fields encompassed by the CPMT Society.

Reichel is responsible for many innovations and developments in the field of microelectronic packaging. Included in his achievements is the introduction of new methods to determine and achieve a high level of electrical, thermo-mechanical and thermal reliability in micro systems. Dr. Reichl has incredible foresight in this industry as he merged technology development, design and simulation many years before hardware and technology co-design found its way into the technical discussion. He was also one of the first researchers to turn his attention from consideration of single technologies and components to the broader spectrum of system solutions. This development has yielded a movement toward all-round system integration. Dr. Reichl's achievements have been recognized by many industry societies. He is as Fellow of IEEE and of IMAPS and received the David Feldman Outstanding Contribution Award from the CPMT Society in 2002.

- **Myung Jin Yim., Ph.D.,** (Georgia Institute of Technology, USA) – IEEE CPMT *Outstanding Young Engineer Award* - for his outstanding contributions to the field of electronic packaging materials and technology through numerous inventions and technical publications, and for services to the CPMT Society. This award recognizes an individual who has made outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.



As a post doctorate researcher for the Georgia Institute of Technology Myung Jin Yim has spent the last 10 years working on the design, synthesis and characterization of polymeric composite materials, especially anisotropic conductive adhesives for electronic packaging applications. He has published more than 20 original papers in prominent peer reviewed journals and has presented his findings more than 40 times at prestigious technical conferences. He has made significant technical contributions including new concepts of anisotropic conductive adhesives applicable to flip chip assembly on organic substrate with dual function of electrical interconnection and underfilling. Additionally, he has a growing reputation as one of the recognized leaders in the field of flip chip technology using electrically conductive adhesives for low cost, low temperature, ultra fine pitch and environmentally clean (lead free) packaging material solutions. Dr. Yim currently holds more than 50 issued patents and patent pending applications. In the past six years he has acquired seven U.S. patents – an unprecedented number for someone so early in their career.

"It's an honor to recognize those professionals who have made significant contributions to our industry through technical or professional achievements," said Kitty Pearsall, CPMT Society awards chair. "We encourage everyone in the profession to nominate their colleagues for next year's awards."

To learn more about the CPMT Society awards, view past winners, or to learn how to nominate a colleague for the 2008 awards, visit **www.cpmt.org/awards**.

About the CPMT Society

The IEEE Components, Packaging and Manufacturing Technology (CPMT) Society is the leading international forum for scientists and engineers engaged in the research, design and development of revolutionary advances in microsystems packaging and manufacturing. Visit **www.cpmt.org** for more information.

Best 2006 CPMT and ECTC Paper Awards

By Dr. Vasudeva P. Atluri, CPMT Newsletter Editor

Two Best Transaction Paper awards were given at the CPMT Luncheon on Thursday during 57th ECTC 2007 in Reno, Nevada.

Best Paper in the 2006 issues of the Transactions on Components and Packaging Technology:

Paper Title: "On-Chip High-Speed Localized Cooling Using Superlattice Microrefrigerators", Volume 29, Issue 2, June 2006.

Authors: Yan Zhang, James Christofferson and Ali Shakouri, UC-Santa Cruz; Gehong Zeng and John Bowers, UC-Santa Barbara; and Edward Croke, HRL Laboratories LLC

Abstract: In this paper, we addressed heating problems in integrated circuits (ICs) and proposed a thin-film thermionic cooling solution using Si/SiGe superlattice microrefrigerators. We compared our technology with the current most common solution, thermoelectric coolers, by strengthening the advantages of its compatible fabrication process as ICs for easy integration, small footprint in the order of /spl sim/ 100x100 um2, high cooling power density, 600W/cm2 and fast transient response less than 40 us. The thermoreflectance imaging also demonstrated its localized cooling. All these features combined together to make these microrefrigerators a very promising application for on-chip temperature control, removing hot spots inside IC.

The award was presented by Paul Wesling, VP-Publications, to James Christofferson. It consists of a certificate, plus US $2,000 divided between the authors.

Best Paper in the 2006 issues of the Transactions on Advanced Packaging:

Paper: "Novel Method for Simultaneous Formation of Wires and Vias of a Printed Circuit Board using Nanoporous Body", Volume 29, Issue 2, May 2006.

Authors: Koji Asakawa, Shigeru Matake, Yasuyuki Hotta and Toshiro Hiraoka, Toshiba Research and Development Center

Abstract: A new type of a flexible printed circuit board with landless vias is developed using a novel method called interconnection via nanoporous structure (INPS). This method can make wires and vias of the printed circuit board simultaneously by a single photo-exposure process. A new photo-induced selective plating method was used to impregnate a nanoporous substrate with copper, and a new photomask was designed, which constitutes of a completely vacant large hole for via and aggregation patterns of very fine holes for wire. Because of the simple process, the INPS board is characterized by landless vias and very fine circuit. Owing to the structure, it is also characterized by flexibility and detachable wires.

The award consists of a certificate, plus US$2,000 divided between the authors. The award was presented by Paul Wesling, CPMT Society VP – Publications, to a representative from Toshiba who received the award on behalf of the authors.

Best ECTC Papers from 56th ECTC 2006:

The Electronic Components and Technology Conference executive committee have also announced the “Best of Conference” and “Conference Outstanding” papers selected from the preceding 56th ECTC 2006. The authors of the Best Session Paper share a check for US $2500 and the authors of the Best Poster Paper share a check for US $1500. The winning authors also receive a personalized certificate commemorating their achievement. The winning authors for Conference Outstanding Paper receive a personalized certificate commemorating their achievement and will share a check for US $1000.

Best of Conference Papers from 56th ECTC 2006 were:

Best Session Paper (Session 20, Paper 7)
Paper Title: Interface Failure in Lead Free Solder Joint
Authors: Robert Darveaux[1,2], Corey Reichman[1,2], Nokibul Islam[1] - [1]Amkor Technology, Inc., [2]Arizona State University

Best Poster Paper (Session 38, Paper 9)
Paper Title: Flex-Circuit Chip-to-Chip Interconnects
Authors: Henning Braunisch, James E. Jaussi, Jason A. Mix, Mark B. Trobough, Bryce D. Horine, Victor Prokofiev, Daoqiang Lu, Rajashree Baskaran, Pascal C.H. Meier, Dong-Ho Han, Kent E. Mallory, Michael W. Leddige - Intel Corporation

Conference Outstanding Papers from 56th ECTC 2006 are:

Outstanding Session Paper (Session 3, Paper 3)
Paper Title: Thin Electroless Cu/OSP on Electroless Ni as a Novel Surface Finish for Flip Chip Solder Joints
Authors: Young-Doo Jeon, Yong-Bin Lee, Young-Sik Choi – Samsung

Outstanding Poster Paper (Session 37, Paper 3)
Paper Title: A Novel Synthesis Method for Designing Electromagnetic Band Gap (EBG) Structures in Packaged Mixed Signal Systems
Authors: Tae Hong Kim[1], Daehyun Chung[2], Ege Engin[1], Wansuk Yun[1], Yoshitaka Toyota[3], Madhavan Swaminathan[1] – [1]Georgia Institute of Technology, [2]Korea Advanced Institute of Science and Technology, [3]Okayama University

These papers and other CPMT Transactions and ECTC papers can be reviewed by accessing **ieeexplore.ieee.org**.

15th Motorola – IEEE CPMT Society Graduate Student Fellowship for Research on Electronic Packaging

Submitted by Dr. Rao Bonda, Program Chair, 57th ECTC 2007

The IEEE CPMT Society announced the 15th Motorola-IEEE CPMT Society Graduate Student Fellowship for Research on Electronic Packaging at 57th ECTC 2007 held in Reno, Nevada. The purpose of the Fellowship is to promote graduate-level study and research in electronic packaging. An annual award will be made to a student enrolled full-time in a graduate curriculum leading to a Ph.D. and whose major field of study is in electronic packaging. For the purpose of this award, electronic packaging research is defined as the fundamental study of the design, analysis, characterization, manufacturing, thermal management, or reliability of electronic interconnect assemblies including semiconductor / photonic devices and printed wiring board technologies. The award is based on a student paper competition held at ECTC for the abstracts submitted by the students indicating a desire to be considered for Motorola Fellowship.

This year’s winning paper at 57th ECTC 2007 was presented by Kiwon Lee and was titled “Ultrasonic Anisotropic Conductive Films (ACFs) Bonding of Flexible Substrates on Organic Rigid Boards at Room Temperature”. Kiwon Lee’s co-authors included

Hyoung Joon Kim, Il Kim and Kyung Wook Paik. Kiwon Lee and all are from Korea Advanced Institute of Science and Technology (KAIST). Dr. Lih-Tyng Hwang from Motorola, Inc. presented the award. The winning student author receives a three-year fellowship grant of $21,000 at his university. For information regarding the Fellowship, please contact Dr. Andrew Skipor, Motorola Chair, at aas002@email.mot.com.

Intel Best Student Paper Award

Submitted by Dr. Rao Bonda, Prog. Chair, 57th ECTC 2007

Intel Corporation sponsored an award for the best paper submitted and presented by a student at the 57th ECTC 2007. To enter the Intel Best Student Paper Award competition, students have checked the "Intel Best Student Paper Award" box in the "Fellowship" section of the on-line abstract submission form. Students considered for the award, are all full time students for at least one semester after the conference conclusion. Only students that were lead authors, and presented the paper at 57th ECTC 2007 were considered. Finalists were determined by review of the completed manuscripts by the judging committee. Manuscripts were reviewed for relevance to the competition topics, technical content, and originality. Finalists were notified by email, and each finalist submitted an affidavit from their faculty advisor certifying that the student meets the eligibility requirements.

This year's winning paper at 57th ECTC 2007 was presented by Jiongxin Lu of Georgia Institute of Technology and was titled "Tailored Dielectric Properties of High-k Polymer Composites Via Nanoparticle Surface Modification for Embedded Passives Applications". Her advisor Dr. C.P. Wong is a co-author on the paper. Mr. Debendra Mallik from Intel Corp. presented the award. The student receives a check for $2500 and a certificate.

Prof. José Schutt-Ainé Appointed Transactions on Advanced Packaging Editor-in-Chief

Submitted by Paul Wesling, CPMT Society VP - Publications

IEEE CPMT Society Board of Governors at June 2nd, 2007 Board Meeting, have nominated Dr. José Schutt-Ainé, Professor of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, as a second Editor-in-Chief for the Transactions on Advanced Packaging, to work alongside Prof. Ganesh Subbarayan, Professor of Mechanical Engineering, Purdue University, who continues as Editor- in-Chief. He is nominated for a four-year term commencing in March, 2007, which is renewable. This nomination adopts the model implemented in 2006 for the Transactions on Components and Packaging Technologies, in which the Transactions is divided topically, so that roughly half of the submissions can be handled by each of two Editors-in-Chief.

José's research focus is on signal integrity, electronic packaging, microwave theory and measurements, digital circuit modeling, integration of modeling and simulation tools, high-speed circuit design, and high-performance computation for simulation of packages. He has been active in the Technical Committee on Electrical Design, Modeling and Simulation, and in both the conference on Electrical Performance of Electronics Packaging (EPEP) and the Workshop on Signal Propagation on Interconnects (SPI).

José served as an Associate Editor for the IEEE Transactions on Circuits and Systems from 1997 to 1999, served as Guest Editor for a special section in IEEE Transactions on Advanced Packaging in 2004, and has been an Associate Editor for Transactions on Advanced Packaging since that time.

José E. Schutt-Ainé (M'82–SM'98) received the B.S. degree from MIT in 1981 and the M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC), in 1984 and 1988, respectively. From 1981 to 1983, he worked at the Microwave Technology Center, Hewlett-Packard, Santa Rosa, CA, as an Application Engineer for microwave amplifiers. During his graduate studies at UIUC, he held summer positions at GTE Network Systems, Northlake, IL, as a Signal Integrity Engineer. In 1996, he worked at Digital Equipment Corporation, Hudson, MA, as a Computer-Aided Design Consultant. He is currently a Professor of electrical and computer engineering at UIUC.

There was a concensus among the key researchers in this field that José would be their choice as Editor-in-Chief, and he has their confidence as he assumes this role. Please assist José as he assumes this new position, and continue to offer support to Ganesh as they work to further improve Transactions on Advanced Packaging.

CPMT Society Officer Interviews:

Interview with Dr. Albert F. Puttlitz,

Vice President (Education), IEEE CPMT Society

By Dr. Vasudeva P. Atluri, CPMT Newsletter Editor-in-Chief

Editor: Tell us a little about yourself, and your family

Al: I was born and lived in Kingston, New York until I left for college. I have an Associate Degree in Mechanical Technology from the State University of New York at Canton, New York (1956), a Bachelor of Science Degree in Mechanical Engineering from Rochester Institute of Technology, Rochester, New York (1959), and a Master of Science Degree in Engineering Mechanics from Michigan Technological University, Houghton, Michigan (1961).

I began my career with the IBM Federal Systems Division in Kingston, New York in 1956. I took three leaves of absence from IBM to pursue my Bachelors, Masters and Doctoral degrees. I received my Ph.D. degree in Engineering Mechanics from Michi-

gan Technological University in 1968. After graduation, I returned to IBM in Essex Junction, Vermont and joined their Microelectronics Division. During 36 years with IBM, I have held group leader/engineering assignments in semiconductor process development, manufacturing engineering, reliability, product assurance, testing, contamination analysis, failure analysis, tooling, mechanical analysis/design and education. Additionally, I set up a mechanical testing laboratory (thermal, shock, vibration, etc.), specified liquid and gaseous filtration processing requirements for semiconductor manufacturing lines, and developed various semiconductor ion implant doping processes and "back-end-of-line" processes for insulators and metallization. I received IBM's first level invention Achievement Award and served as Invention-Disclosure-Review-Board member. I have taught college-level engineering courses at Michigan Technological University and IBM. I retired from IBM in 1992; I now consult, is active as a licensed Realtor in the State of Vermont, USA and is more involved with ECTC and CPMT.

I hold the IEEE/CPMT membership grade of Senior Member, is a member of ASME and the US Power Squadron, and is active in community and church affairs. I has been married to my wife, Marie, for almost 45 years. They have two children and two grandsons.

Editor: Tell us how you got involved in the field of packaging and something about your career

Al: I have numerous external and internal IBM publications. I became acquainted with the CPMT Society after I presented his first paper at ECTC. I was presenter and/or co-author of papers at four ECTC Components sessions (1985, 1986, 1989, and 1992). I received the best CPMT Transactions Paper Award in 1985 (with Sang Kim). I am a 20-year member of the IEEE-CPMT Society, served on ECTC Components and RF Paper Review Committee for the past seventeen years, was the ECTC Components and RF Subcommittee Program Chair during 1991-1993, and served as the ECTC Components and RF session Chairman or Co-chairman for nine years. I served as the Professional Development Course (Short Course) Chairman for eight years, with rotations as its chair every three years with other members of the Professional Development Course Committee, and was the chair of the ECTC 2007 Professional Development Course Committee. I introduced "Continuing Education Units" credits for attendees of ECTC-Professional Development Courses (sponsored by the IEEE Education Department) and was responsible for institution of the "CPMT Professional Development Certificate of Achievement". During my tenure as the ECTC-Professional Development Course chair/committee member, attendance at the Professional Development Courses has grown from about 50 attendees to now 300+ attendees.

I was elected to five terms as a Member-at-Large on the CPMT Board of Governors. He has been the CPMT VP of Education for the past 10 years and currently holds that position.

Editor: What do you see as the needs of our members around the world - what are the most important issues the CPMT Society can address?

Al: One of the critical short term and long-term issues facing CPMT (and all IEEE societies) is to determine what needs to be done so that our members repeat their membership year to year. CPMT membership has been declining for a number of years; the number of non-repeating members exceeds new members. While various "perks" have been offered to retain membership, they haven't done much good. *We need to "crack this nut"!* One of CPMT's previous draws for retaining membership was receipt of a hard copy of the their publications…but now, publications can be viewed on-line.

Related to the above is the unclear distinction between various grades of CPMT membership. IEEE's membership statistics show that members who hold "Senior Member" and "Fellow" grades repeat their memberships more often than just society members. While the prestige of being a CPMT Fellow is clear, the advantage of being a CPMT Senior Member versus just a Member is not defined. Being a Senior Member so that you may become a Fellow is true but not enough! I will propose several initiatives of being a Senior Member to the Board of Governors at the November 2007 Board of Governors meeting for their consideration.

Editor: What are your visions for the Society in short and long term?

Al: I envision a greater and more active student population in CPMT in the future, which will be obtained by fulfilling the needs of the students now. Today's CPMT students are tomorrow's CPMT leaders. Increased number of student scholarships and fellowships, and increased student participation at our workshops and conferences are key. Furthermore, in addition to increasing the number of CPMT chapters worldwide, we need to focus on establishing active student chapters worldwide. This means we need active and dedicated CPMT people to guide the students.

In year 2008, CPMT will be offering a new $5,000 Ph.D. fellowship in addition to the Motorola-CPMT Fellowship of $21,000+ in Electronic Packaging. CPMT's new Ph.D. fellowship is open to candidates obtaining their Ph.D. in any field of interest to CPMT, not just Electronics Packaging.

Editor: What would be your advice to engineers who are in or entering this field for career growth?

Al: My advice to engineers in this field (or any other occupation) is to compete, get involved, stay involved and keep current. Give papers at workshops and conferences, teach and help the students. With especially students, you'll get back much more than you give, as your help will be repeated many times during the student's future. Keep abreast of changes in your field…if you don't you will rapidly become obsolete.

Editor: Where (on what tasks) could you use help from members?

Al: The most important need for CPMT members is to be our ambassadors at conferences, workshops, colleges and universities. I encourage the use of CPMT Distinguished Lecturers at any CPMT (co)sponsored venue and chapters. We have 30 Distinguished Lecturers in many fields of interest to CPMT; an updated list of Distinguished Lecturers with their topics of expertise will soon be available on-line at **www.cpmt.org**. Additionally, Distinguished Lecturers, organizers of their venues and CPMT chapters can contact me at a.f.puttlitz@ieee.org for details.

Editor: What are you're accomplishments as CPMT VP of Education for the past seven years?

Al: My accomplishments during past seven years included:

- As an initiative to promote the CPMT Society worldwide, I have led a delegation to Hong Kong in year 2000 and was a member of the year 2000 Singapore delegation.
- I have been a member of the ECTC Electronic Packaging Paper Review Committee and was the Chairman of several of the ECTC Electronic Packaging Sessions for four years.
- I was a member of the Electronic-Packaging-Education-Faculty-Grant Committee (with Prof. Leyla Conrad, Mr. Paul Wesling, and Prof. Andrew Tay). Over 12 Grants, sponsored by CPMT and Prof. Rao Tummala of the Packaging Research Center at Georgia Institute of Technology, have been awarded to professors at various colleges and universities for developing multimedia/web-based Electronic Packaging Courses for the 21st Century. The last grants were awarded at the 2003-ECTC.
- I served as the Director of the CPMT Distinguished Lecturer Program. To-date, the program has 30 Distinguished Lecturers. The program is in worldwide use with new members added yearly.
- I am a member of the CPMT-Motorola Ph.D. Fellowship Committee responsible for awarding a yearly fellowship in excess of $21,000 in Electronic Packaging to a Ph.D. student, who presents his/her work at ECTCs.
- I also assisted in the development of the Short Course program at the first *Electronic System-Integration Technology Conference* held during 2006 in Dresden, Germany.

Editor: What are your future goals or plans for the Society within as VP of Education?

Al: My future goals are as follows:

- Continue to promote CPMT worldwide as the premier packaging society by continuing to offer educational courses, programs and opportunities for its members.
- Enhance the CPMT Distinguished Lecturer Program by obtaining members from non-US countries as well as the US. Eight non-US members have been elected as CPMT-Distinguished Lecturers in the past year. Additionally, encourage the use of Distinguished Lecturers in CPMT (co) sponsored venues by expanding the current CPMT Distinguished Lecturer Travel Assistance program.
- Initiate/support students/student programs financially at CPMT (co)-sponsored venues including conferences, workshops, chapters as well as high schools, colleges, universities, etc.
- Expand the visibility and desirability of the CPMT-Motorola Ph.D. Fellowship and introduce new CPMT (co)-sponsored Educational Scholarships and Fellowships.

Editor: What do you like to do in your spare time? What's a good book you have read recently?

Al: I enjoy traveling, entertaining family and friends, spending time with grandsons and boating on Lake Champlain. Volunteering for the Ronald McDonald House Charities for the past 15 years has enriched my life. Reading is also one of my priorities when I have the time; I am currently reading "The DaVinci Code".

Editor: Thank you, Al!!!

Interview with Dr. Thomas G. Reynolds III,

Vice President (Finance), IEEE CPMT Society

By Dr. Vasudeva P. Atluri, CPMT Newsletter Editor-in-Chief

Editor: Tell us a little about yourself, and your family

Tom: With a background in mechanical engineering (BS Univ. of VA) and materials science (MS Univ. of VA, PhD Brown Univ.), I have come to IEEE CPMT with an emphasis on materials, synthesis, properties and manufacturability. Early career activities were in the development and fabrication of barium titanate semiconductors for Texas Instruments, development and fabrication of isostatic hot pressed MnZn ferrites and fabrication of magnetic recording heads, activities included analytical chem. lab and electronics lab for a division of Philips Electronics. Later work in Philips (Holland) focused on development and implementation of manufacturing process for wet chemical synthesis of ceramic capacitor materials and technology transfer of capacitor technologies between European operations and Japanese joint venture. My last position as Director of Technology for Murata Manufacturing Co. Ltd (USA) involved implementation of new and novel capacitor technologies (i.e. low inductance SMD caps, and thin film caps), RF components, and filters. I was also involved evaluation of merger and acquisition candidates. I am currently retired and consult on a part time or project basis.

Editor: What do you see as the needs of our members around the world - what are the most important issues the CPMT Society can address?

Tom: Currently VP Finance for the CPMT Society, I would like to see the CPMT and its premier conference, ECTC, continue on a firm financial footing.. and in my view that means growth for our membership through continued linkage to developing and future technologies. Over the last 10-20 years the discrete components area has matured. Although the components have continually shrunk from 1206 (0.0120 x 0.060) to as small as 1.0 x 0.5 mm, it is clear that thin film and embedded technologies will result in shorter interconnects, lower parasitics and higher component densities. In addition the package is no longer a "discrete" component. The package itself is circuit, contains either embedded or attached passive and active components. The result is a much more integrated view of packaging as a complete "system". This approach carries with it demand for much more sophisticated circuit design and much much higher manufacturing yields and product reliability. These areas as well as the areas of the high speed interconnection of signals (eg optical interconnects) and power management (thermal dissipation) will continue to be limiting steps in the future advancement of components and packaging. A final area that should be aggressively addressed is the evolution of sensors and actuators of all types...

Editor: What are your visions for the society in short and long term?

Tom: Our members should view CPMT as their worldwide community for a whole range of activities: data and information exchange... the place where they turn first to find out what is going on in their field and in new areas of interest. Through personal interactions- via email, conferences, chapter meetings and individual contact - the membership of CPMT should be able to communicate easily with each other and come to rely on each other for ideas, solutions and opportunities. Continual development of a "worldwide community of CPMT" will serve their interests and assure our continued growth.

Editor: Tell us how you got involved in the field of packaging and something about your career

Tom: In addition to my activities with IEEE, during 35 years that I was involved in the development and implementation of electronic ceramics, I was very active in the American Ceramic Society: Chairman Electronics Division, elected Fellow of the Society, elected VP of the Society and numerous Committee assignments. I have also been actively involved with the Electronic Components and Technologies Conference (ECTC) since 1992 as: Program Chairman, Chairman-elect, Chairman for the 50th ECTC anniversary meeting and I remain a member of the Executive Committee and the Finance Chair of ECTC.

Editor: What do you like to do in your spare time?

Tom: Gosh, my interests are pretty well-known by most people... SAILING. My wife Dr. Lynne and I own a Catalina 34 sailboat which we berth at the Ft Walton Yacht Club in Ft Walton Beach, Florida. We get a great deal of enjoyment from sailing. In fact, she and I sailed across the Gulf of Mexico together when we purchased the boat several years ago. Although I have raced and crewed in local club races for many years, we really use "Celebration" for short or long term cruises. Being involved with the Ft Walton Yacht Club for more than 7 years, I enjoyed serving as Commodore for the year 2006. In that activity we focused on physical improvements to the club, protection of the property from storms and increasing our membership. I am currently involved in an extensive refit of the mast, running rigging and sails to upgrade to SOTA condition.

Editor: What's a good book you have read recently?

Tom: I've lately been reading an eclectic collection of books... always a lot of sailing, cruising and racing tactics books. In addition to these I am interested in the technology and accomplishments of what we consider to be ancient civilizations... the Mayan calendar and how it was derived and also the construction of ancient monuments and sites.

Editor: Thank you, Tom!!!

Member Recognition:

Dr. C.P. Wong Honored by Sigma Xi

By Vasudeva P. Atluri, CPMT Society Newsletter Editor

Congratulations on being selected as the winner of the 2007 Sigma Xi (The Scientific Research Society) Monie A. Ferst Award! The Award is given annually to an educator in engineering or science who has made "notable contributions to

the motivation and encouragement of research through education." Its purpose is to "recognize significant contributions to scientific research by an educator in engineering or science." It consists of a medal and $5,000 and is made annually to an educator who has inspired his or her colleagues to significant scientific achievements. A One-day Symposium will be held in honor of Prof. Wong during Fall of 2007.

Conference Reviews:

57th Electronic Components Technology Conference, Reno, Nevada May 29th – June 1st, 2007

Submitted by Dr. Patrick Thompson, Junior Past Chair, ECTC Executive Committee

John Ascuaga's Nugget Hotel in Reno, NV was home base for the more than 1,000 technical professional who attended this year's Electronic Component and Technology Conference (ECTC) from May 29 to June 1, 2007, the 57th time this premier international packaging conference has been held. From workshops and tutorials, to panel and plenary sessions and the technology corner, to oral and poster paper presentations, attendees had a wide array of technical forums from which to choose. In addition extended morning and afternoon coffee breaks and multiple receptions provided great networking opportunities.

Eric Perfecto, 2007 ECTC General Chair, addresses the audience at the ECTC Luncheon

Technical papers provide the backbone of the ECTC. This year, more than 250 oral and 50 poster papers were presented in 36 oral and 2 poster sessions covering nine technical areas: advanced packaging, modeling & simulation, optoelectronics, interconnections, materials and processing, quality and reliability, manufacturing technology, components and RF and emerging technologies. ECTC has a tradition of providing state of the art information on both established and emerging technologies. This year's emerging technology sessions included Nanotechnology and Bio and Flexible Electronics. Poster presentations provided the authors and attendees the opportunity for extended technical discussions on the subjects of interest. This year, the ECTC organizers again held a poster session just for students. The emphasis of this poster session is to provide a venue for students to hone their paper preparation and presentation skills.

Tutorials comprise the second key component of the ECTC. We are fortunate to have leading technologists from industry and academia eager to present their material at ECTC. This year, attendees could choose from 16 tutorials covering a wide range of packaging-related topics. Nearly 300 persons took advantage of the chance to learn the basics of a new area or deepen their understanding of a specific subject.

The Technology Corner completes the tripart focus of the ECTC. With a more intimate format than tradeshows, the Technology Corner allows attendees and representatives from material, process and service providers to discuss opportunities for problem solving and collaboration. This year, more than 60 organizations staffed booths.

John Stafford and Phil Garrou relax at the Gala Reception

In addition to the core technical activities of the ECTC, there are additional technical meetings. NEMI again held its Tin Whisker Workshop in parallel with the tutorials. Several CPMT Technical Committees met throughout the conference. A large format technical presentation was offered each night of the conference.

On Tuesday night, Bill Chen, President of CPMT, hosted the ECTC Panel Session, "More Moore" and "More than Moore" – When Market Meets Technology'. Four speakers addressed how packaging can enable the drive for ever-increasing function per volume in the consumer-driven electronics market. The speakers and audience participated in a lively Q&A session following the speakers' remarks.

Eric Perfecto with representatives of KOA, a Gala Reception sponsor

Wednesday night, Wolfgang Sauter of the ECTC Program Committee hosted the Plenary Session, "Where Does Packaging Research and Development Take Place: Current Trends and Predictions". Using the manufacturing trend of more outsourcing at lower cost as a basis, the speakers addressed the question, is the same migration occurring with packaging research and development? The audience heard perspectives from IDM, system house, contract manufacturer and academia representatives. The combination of views led to a spirited Q&A session.

The Advanced Packaging Technical Committee of CPMT held the final evening session on Thursday. In "Advanced 3D Packaging Technologies," attendees heard the expanding role 3D packaging is playing in the push for small and thin electronic equipment. Speakers addressed developments in 3D packages, such as Chip on Chip and Package on Package (PoP) technologies, and covered the latest developments in advanced 3D packaging in Japan.

Exceptional papers presented at ECTC will be awarded the Motorola-IEEE CPMT Society Graduate Student Fellowship, Intel Best Student Paper award, and best outstanding paper awards.

Although it might seem hard to imagine with all the technical activities, ECTC also provides significant professional and social interaction time. Forty-five minute coffee breaks each morning and afternoon allowed attendees to follow up with a speaker on an interesting paper, touch base with a colleague, or form new friendships. The luncheons each day provided a venue to learn about the conference and CPMT, as well as network with table mates. A variety of receptions presented a relaxed environment for attendees and their companions to interact.

A young assistant (Ms. Sirisha Bonda, daughter of 57th ECTC 2007 Program Chair, Dr. N. Rao Bonda) helps Tom Reynolds with the traditional Program Chair's Luncheon door prize give-away

The ECTC Executive and Program committee strive to put on an excellent conference each year, and each year recognize excellence from the participants. At Tuesday's ECTC Luncheon, Best Paper awards were presented from the 2006 ECTC. On Friday, the Intel Best Student Paper, and Intel Fellowship awards were presented.

If you were unable to attend the 2007 ECTC, you can obtain the proceedings from . Please make plans to attend the 2008 ECTC at the Contemporary Resort and Walt Disney World in Orlando, Florida, from May 27-30, 2008.

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The Electronic Components and Technology Conference - Background Information

Pete Walsh, Arrangements Chairman and Vice Chairman Administration, ECTC

In May of 1950, over 57 years ago, a "Symposium of Improved Quality Electronic Components" was held in the Department of Interior auditorium in Washington, D.C. The motivation for this meeting was expressed by the Chairman of the Steering Committee…..written at a time when many people had not yet even heard of the transistor.

"Most of the modern electronic equipment is made up very large numbers of components….The probability of failure of the equipment is therefore enormously greater than the probability of failure of any one component…. the present industrial situation does not provide (sufficiently) high quality articles plentifully nor do current ideas on permissible size and weight of equipment allow such components to be used generally"

"This Symposium was held for the purpose of inviting a thorough public discussion of the problem within the profession and with the objective of stimulating new effort on the part of component engineers, was well as electronic equipment engineers toward a solution."

The 1950 Symposium was sponsored by the American Institute of Electric Engineers (AIEE), Institute of Radio Engineers 9IRE) and Radio Manufacturers Association (RMA) (now IEEE and EIA) with active participation by agencies of the U. S. Department of Defense and the National Bureau of Standards. It had as a precursor a 1948 Conference on Printed Circuits sponsored by the Bureau of Aeronautics and the National Bureau of Standards. Gil Reid was chairman of the 1948 Conference and Program Chairman in 1950.

There seems to be no evidence that the organizers of the original meeting expected it to become an Annual event. However, its success and the continuing pressure for a forum for engineers to discuss component development and applications resulted in a second symposium in 1952 and annual meetings thereafter. In addition, in 1951, the L.A. Section of the IRE and the UCLA sponsored a Components Symposium in Los Angeles.

In 1954, the Joint Electronic Components Executive Committee 9JECEC) was formed by the sponsoring organizations, to which the Western Electronics Manufacturers Association (WEMA) had been added, with responsibility for management of the annual conferences. This Committee was known as the Electronic Components Conference Coordinating Committee (EC4-now known as the Governing Council). In 1962, WEMA dropped out so that, with the AIEE-IRE merger, sponsorship fell to the IEEE and EIA. The membership of EC4, including the officers, was provided by the administrative committee of the IEEE Components, Hybrids and Manufacturing Technology Society (IEEE-CHMT) and later changed to the Components, Packaging and Manufacturing Technology Society (CPMT) and by the Parts Division (later changed to the Components Group and to the Electronic Components, Assemblies & Material Association of the Electronic Industries Association and later changed to Electronic Industries Alliance (EIA). IEEE/CHMT was formed in 1977 by the merger of the IEEE Professional Technical Group on Parts, Materials & Packaging 9IEEE-PHP) with the IEEE Manufacturing technology Group.

The roles of the Sponsors…The basic role of the sponsors of the conference is to provide operational support and promotion through the resources of their respective organizations. The financial responsibilities are shared equally between the sponsors. Operationally, the sponsors have separate responsibilities as follows:

Administration – The EIA/ECA has the primary responsibility for providing administrative support to the Conference, eg.: coordination of arrangements and operations, by providing the Vice Chairman of Administration responsible for the coordination and general supervision of all Executive Committee functions not associated with the development of the technical program. He works closely with the Arrangements Chairman, Publications Chairman and Publicity Chairman to help insure a smooth running conference.

Technical Program – The IEEE/CPMT Society has the primary responsibility for providing the support to the conference technical program by providing members and leadership candidates for the Conference Program Committee

To give more detail to the above, the EIA/ECA provides support and services for pre-conferences, onsite and post-conference logistics and administration for the conference and technical corner, including site selection and negotiation, pre-registration, onsite registration and administration, and post-conference administration and wrap-up.

Site Selection

- Solicit hotel bids based on Executive Committee city/ies recommendation
- Receipt-review, negotiate and do site inspection/s
- Prepare and present recommendations to the Executive Committee for selection
- Further negotiate, received General Counsel approval and administer contract
- Arrange pre-conference November familiarization tour by General Chairman, Vice Chairman Or Program Chairman, Technology Chairman and Arrangements Chairman

Site Logistics

- Configure hotel meeting space for conference, registration and technology corner
- Establish catering requirements
- Establish A/V requirements
- Request bids and contract for security and temporary services
- Request bids and contract for exhibit management services
- Review/production of all signage including sponsorships, exhibit, registration, session, etc.
- Request bids and contracts for conference shirts, tote bags, etc.

Information Technology

- Monitor, update, and maintain data base
- Monitor, update, and maintain web site (basic)
- Establish secure online conference data base

Pre-Conference Registration

- Receive and process all conference pre-registrations
- Process and verify all payments (checks, wire transfers, credit cards)
- Confirm registration

- Produce badges and onsite materials
- Solicitation of reception, shirt, tote bag, refreshment sponsors, etc.
- Coordinate/produce all conference awards, including plaques, certificates, etc.

Technology Corner

- Prepare and distribute exhibitor manuals
- Assists Technology Corner Chairman with exhibit contractor requirements (re hotel Contract)

Onsite

- Attend onsite pre-conference meeting with hotel to iron out all details
- Set up and supervise onsite registration area
- Develop and administer all guarantees to hotel
- Supervise tote bag suffers
- Distribute shirts to selected members
- Receive and process onsite registration
- Receive and distribute onsite conference materials
- Supervise room setups and A/V requirements
- Position and continually update conference signage
- Supervise hotel accommodations and services negotiated in contract

Post-Conference Registration

- Verify and process registrations (credit cards, etc.)
- Develop and provide necessary documentation on attendees for Executive Committee
- Ship all conference materials purchased, i.e – proceedings, registration packets for Attendees who could not attend, signage, etc.

Accounting

- Process and verify all conference payments and credit cards (exhibitors)
- Process and receive various sponsor and miscellaneous payments
- Prepare monthly reports
- Process and transact revenues and expenses as appropriate
- Develop and maintain all revenue and expense documentation as necessary, including
- Overall expenses incurred by ECA
- Review and authorize revenue and expense invoices as necessary

ECA Incurred Expenses (for reimbursement)

- Conference materials needed for registration and staff office
- Conference print materials needed for sessions, PDCs, registration, etc.
- Postage (regular and overnight)
- Credit card usage fees incurred from AMX, Visa and M/C
- Other items not mentioned above

Off-site/Year-Round Administration

- Planning and contract for November program meeting
- Web site maintenance

Pete Walsh has served the EIA/ECA for the past 38 years ranging from positions of director, marketing services, staff vice president, vice president, and two stints as acting CEO

of the Components Group. In those positions, Mr. Walsh has been providing national membership services and association liaison with Group members, as well as planning and organizing meetings, conferences and exhibitions. Mr. Walsh, for the past twenty-five years, has been Arrangements Chairman, as well as Vice Chairman of Administration for the ECTC.

57th ECTC 2007 General Chair and Program Chair

By Dr. Vasudeva P. Atluri, CPMT Newsletter Editor

Eric Perfecto (SM'01) was the General Chair at this year's 57th Electronic Components & Technology Conference (ECTC) in

Reno, NV, and the Program Chair at the 55th ECTC. He served for two years as the Materials and Processes Subcommittee Chair ('02-'03). He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers (SPE), and is a member of the Society of Hispanic Engineers (SHPE). He has served as President of the SPE Mid-Hudson section (1993-5, 2001-3) and has been a member of the organizing committee for the "Photopolymers" and the "Polymers in Electronic Packaging" conferences since 1991. He is the Chair of the mentoring committee of the IBM East Fishkill Technical Vitality Council, and for 4 years participated as a mentor for the local high school. He also volunteers as a math tutor for the local junior high school, and has been a frequent judge at the county science fair.

Eric is a Senior Technical Staff Member at IBM, with 25 years of thin films and C4 experience working in the process development of advanced packages at IBM Microelectronics. He holds an M.S. in Chemical Engineering from the University of Illinois and an M.S. in Statistics & Operations Research from Union College.

Eric's technical involvement has been in the development of multi-chip modules (MCM) for IBM's High end systems. There he developed and implemented multi-level thin films technology on top of ceramic substrates. He has led a number of projects in the areas of photolithography, etching, photosensitive polyimide, pattern electroplating and bonding metallurgies for C4 joining, wirebonding and LGA. Through his publications, he led an industry-wide investigation of large format processing to lower the TF cost, and led the development of thin film transfer technology and the optimization of the joining materials (metallurgy and adhesives) and processes (solder and thermoplastic joining). He is currently responsible for the yield and implementation of the C4NP technology. His technical interests include Pb-free solders, chip package interaction, 3D interconnect, and design for manufacturing.

Eric has published over 50 external papers and 12 IBM internal technical reports. He received the 1994 CPMT Trans. - Advance Packaging Prize Paper Award, and the Best Paper Award from the 1st ESTC Conference held in Dresden, Germany in 2006. He holds 30 US patents, has received 3 IBM Patent Awards, and holds the IBM 9th Plateau Invention Achievement Award. He received an IBM Outstanding Technical Achievement Award for the development, optimization and implementation of multi-level thin film modules.

Dr. N. Rao Bonda has been actively participating in the Electronic Components and Technology Conference (ECTC) for several years. He has served as the chairman of the Components and RF sub-committee and has chaired the sessions at the ECTC. He has chaired the ECTC's Professional Development Courses committee and served on the committee for three years. He was the Assistant Program Chair for the 2006 ECTC and Program Chair for 2007 ECTC. He is the Vice General Chair for 2008ECTC.

Rao is currently a member of research and development staff in Freescale Semiconductor, Inc. (formerly known as Motorola's Semiconductor Products Sector) in Tempe, AZ. He received a Ph.D. in Materials Science and Engineering from the University of Pennsylvania, Philadelphia, PA, in 1985. After receiving Ph.D., Rao continued research in materials science at the Ohio State University, Columbus, OH and the University of Wisconsin, Madison, WI until 1989. From 1989 to 1994, he was a research member at IBM T.J. Watson Research Center, Yorktown Heights, NY, and IBM Microelectronics Division, Endicott, NY. In IBM, he developed electronic packages and processes involving flip chip and wire bond chip joining methods, and worked on qualification of several ceramic and plastic packages. His other research work in IBM included failure mechanism studies of Pb/Sn solder alloys to improve the thermal fatigue and reliability of solder joints in electronic packages.

In 1994, Rao joined Motorola's Semiconductor Products Sector in Tempe, AZ, as a team leader for packaging of an optical display module. He developed a fine pitch flip chip bonding process for this display module and improved its yield and reliability through innovative designs. After completion of the display module project, he led new package introductions from design to manufacture implementation and qualified plastic packages for wireless communication and networking systems applications. He currently provides packaging development and technical support for a major wireless communications customer and works with package assembly subcontractors to fulfill the customer's product requirements and packaging roadmaps. He has over 20 technical publications and a US patent.

Rao has been a member of the Board of Governors for the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society for nine years. He was the Chair of its Awards Committee from 1997-2005. Currently, he is the Vice President-Technical for the Society. He is also an Associate Editor for IEEE Transactions on Advanced Packaging journal. He is very active in CPMT Phoenix Chapter and IEEE Phoenix Section. He has served as the chair and program chair for the Chapter and as the treasurer, secretary and vice chair for the IEEE Phoenix Section. He is currently the Chair for the Phoenix Section.

Rao is a member of the IEEE and IEEE CPMT Society. In addition to a Ph.D., he holds an MS and a BS in Metallurgical Engineering from Indian Institute of Technology, Kanpur, and Regional Engineering College, Warangal (India), respectively. He also received an MBA from the Arizona State University, Tempe, AZ, in 1998.

57th ECTC 2007 Sessions Summary

Submitted by Dr. Dave Palmer, IEEE Fellow, Sandia National Laboratories

The ECTC had 250 presentations with 6 given at a time in parallel, as well as 65 posters. One person can only sample a small percentage of the information face-to-face but the proceedings CD or book allow one to catch up after the conference.

In **session 4 on RF Components** Edward Pillai (in picture at left – Edward Pillai presenting in session 4) showed how an upgrade to IBM legacy printed wiring boards were possible using a micro T-coil to match high frequency signals to the existing boards. An improvement from 3 – 12 GHz was possible. Deji Akinwande of Stanford gave a tutorial on parallel and serial RF power combiners/dividers. From this perspective he described a parallel plate TEM mode wave guide that had one input and N microstrip outputs when used as a divider. Li Li of Freescale presented for Lianjun Liu a cavity packaged RF MEMs switch giving 25 dB of isolation up to 40 GHz. The cell phone is one target for this technology. Georgia Tech presented a planar antenna using liquid crystal polymer substrate with embedded resistors that allowed for beam shaping with a large weather antenna as the target. Remco Strijbos of NXP Semiconductors discussed processes that gave high Q ~ 2500 to Bulk Acoustic Filters on solid substrate (contrast with FBAR). Bau-Nan Li of National Sun Yat-Sen University described a miniature band pass filter equivalent to a 3-order Chebyshev using BT laminate and metal traces using only 2.6 x 1.9 mm of surface area. Sandia Labs described passive wireless sensors with 8 bit measurement accuracy which give a 1 milliwatt range of 10 meters based on surface acoustic wave devices.

In **Session 10 on Nanotechnology** Azad Naeemi (in picture at right – Azad Naeemi preparing to talk in session 10 with chair Vasudeva Atluri) of Georgia Tech discussed using carbon nanotubes to improve power distribution on-chip. Combining copper with tubes presents many challenges. Yang Chai of Hong Kong University described the growth of high density arrays of carbon nanotubes with thermal conductivity of 6000 W m / K with the low temperature transfer to another substrate. Rabindra Das of Endicott Interconnect Technologies described materials and processes that would allow embedded capacitors that could be trimmed both by changing dielectric thickness and constant. Chia-Ming Chang of Sun Yat-sen University presented a method of using carbon nanaotubes in polyimide matrix to provide EM shielding to a system. Density of 30% was needed to achieve useful conductivity. Chung-Jung Wu of National Tsing Hua University discussed the mechanical models of conductors that could approach 25 million amps/ cm2. Jiongxin Lu of Georgia Institute of Technology presented the use of nano composites to achieve high-K polymer dielectrics to use as the gate for organic transistors. $BaTiO_3$ with epoxy had been used in the past achieving K=35 but with a high loss. BCB polymer was used this time and

the losses were .016 with K=50. The leakage at 6 V remained small.

In **Session 13 on Wafer Level Packaging** Kai Zoschke (in picture at left - speaker Kai Zoschke with chair Joseph Soucy at session 13) of Fraunhofer IZM presented the next generation of embedded passives on wafers with patterned glass. As a low temperature vapor deposited glass it tested well up to 20 GHz with K=4.3. Won Kyu Jeung of Samsung Electro-Mechanics Co. described a wafer level packaging approach for surface acoustic wave devices resulting in surface mount devices with low stress. The package volume was reduced to 25% of current CSP approaches.

In **Session 17 on Packaging and Assembly Challenges** Li Li of Cisco described minimizing any popcorn effect by careful control of water diffusion over the edge of the chip surface (using seal ring metallization at the edge of die/polyimide interface. Laser dicing was discussed by Taegyeong Chung of Samsung Electronics. In particular the improvement in edge chipping compared to standard sawing of thinned wafers was analyzed. UV laser was not recommended because of redeposit of ablation. Chris Hartsough of University of Maryland described a promising new measurement method to monitor warpage during the increasing complex reflow and assembly steps. Amin Rida of Georgia Tech described an inexpensive coated paper based ink jet antenna for RFID silicon chips. Everyone in the room got excited and had something to ask or add to the presentation…one of those great moments at a conference.

In **Session 22 on RF Modules** A. den Dekker of NXP Semiconductors discussed passive integration on Silicon. His target is the cellular and Bluetooth markets and they develop caps, resistors and inductors. Bo Gao of Hong Kong University discussed low cost passive UHF RFID packaging and the sensitivity to nearby metal surfaces and even moisture in cardboard backing. They developed a ferro antenna that isolates the EM from the backing so they can have an on-metal tag. George White of Jacket Micro Devices presented GURU (Global Universal Radio Units) and the process to obtain high Q passives using organic multilayer board to come up with an inexpensive alternative to the LTCC approach. John Park of Cadence described a complete family of RF silicon in Package design tools recently developed with the strong financial backing of 3 of their clients.

In **Session 25 on MEMS Packaging** Mark Wagner of Sensorcon described using packaging materials not silicon to give low cost MEMS package that will not be integrated directly on an IC. Suk-Jin Ham of Samsung Advanced Institute of Technology described a wet etch high resistivity silicon cavity package to protect FBAR structures from further oxidization. The package was sealed in nitrogen at 260 C with AuSn solder. Tests were done at 2 GHz.

In **Session 27 on Nano, Bio and RF** Matt Lueck (in picture at right column top – Matt Lueck presenting in session 27) of RTI International described a silicon interposer with embedded through wafer inductors. The interposer with passives would be positioned between two face –to-face ICs. 400 micron thick wafers were used with Bosch etching and copper metal to achiever Qs of ten. Frank Theunis of NXP Semiconductors described customer RF MEMS package family with nitrogen back filling. The cavity is only 3x3 mm. SnAu solder seal is only 80 microns wide so it does not provide large parasitics with the I/Os. Chien-Hsiang Huang of National Sun Yat-sen University showed a modeling design system that could achieve Qs of 100 with both LTCC and thin film processes in the L band. This work was done with closed form formulas not fancy workstation numerics. Hanyi Ding of IBM described the design and testing that went into entering a millimeter wave general Wilkinson divider into the IBM library. The confirmation testing was done at 94 GHz.

In **Session 31 on Advanced Packaging** Moody Dreiza of Amkor Technology described a high density Package on package with a top memory on a bottom logic package. Known good units had to be used for the high volume cellular market. "Dipping Paste" was used on solder bumps to help compensate for any warpage. Kazuo Ishibashi of Nokia Japan talked of warpage on PoPs and minimizing yield loss. Kai Liu described technology for many RF modules intended for WLAN market. The approach was to have many chip scale modules that could be used as building blocks for any application needed to provide quick product cycle time. Cher Bai of Qualcomm described the analysis using die size, thermal via count, and amount of copper on board to predict the thermal performance of modules for mobile handsets. Tae Kyun Kim of Samsung described screen printing in a high vacuum and how this is better than glob top for System-in-Package applications. Raj Pendse of STATSChipPAC discussed extremely thin wafers and using flip-chip. Even removing bumped chips from tape after singulation proved challenging. Three stacked chips on BGA (.24mm) resulted in only 1.4 mm thickness after molding.

Lots of excitement at Poster Sessions

57th ECTC 2007 Invited Sessions and Meetings Summary

Submitted by Dr. Dave Palmer, IEEE Fellow, Sandia National Laboratories

Luncheon Keynote:

Jeff Jonas of IBM Las Vegas gave a titillating ECTC lunch speech. He presented several proven techniques to defraud casi-

nos of more than $100,000 in one hour. We all had to promise not to divulge this information so this article will remain vague on details.

Jonas is an IBM distinguished engineer who has written the book "Cheating Las Vegas." His main theme for this talk was that you must treat your data like a question or you will never know its relevance unless someone just happens to ask the right timely question. He described NORA (Non-Obvious Relationship Awareness) as a set of software that takes many databases and "asks" questions that result in important correlations.

One example presented was that there are 38 million visitors a year to the 20 largest Vegas hotels. Enough data exists at the hotels that with the proper data mining software they could have prevented the few thousand known cheaters and thieves in this 38 million from entering their doors. However, today they only find out about the correlations after the criminal has left. Jonas defined this as Enterprise Amnesia, where one part of the company has data needed by another but never asked for. Each year many people are hired by a casino that were arrested in past years for committing crimes at the same casino. Many more are hired who are related to such criminals or are suppliers of critical supplies to the casino. Many conflict of interest issues are actually "known" in the casino data archives.

He pointed out one weakness of slot machines (that is now fixed). When a new $100 bill was issued it could not be read right by the slot machine so it would give the correct amount in tokens plus give back the bill. He also showed a little light emitting stick that could allow a slot player to empty all the coins in the machine no matter how minor the actual win.

Another term he introduces was "perception isolation." The cure was to run all kinds of cross checkers (ask the right questions) every time new data is entered. For example, notice that D. William Banks used to work at the casino and was fired and now David W Banks has just interviewed. So each piece of data is really a set of data base queries and each query should find related queries. If ten different queries are generated in the last week on some variations of D. W. Banks this is probably not coincidence but should be investigated.

Jonas described one application of these software ideas concerning the effort to reunite New Orleans residents after the Katrina Hurricane. They entered 1.5 million Internet postings for missing people. Reduced this to 38,865 unique real persons (there were many redundant or fake entries). This resulted in more than 100 families being reunited (some matches did not want to reunite and many were false matches).

He stressed that as computer power and storage is growing we are often ironically getting dumber. The right automatic query tools help but privacy must also be protected. He described a future Analytics in an Anonymized Data Space. Using this, many government agencies or casinos could compare databases in an encrypted memory bank so that no one person could see all the data. However, if the D. W. Banks showed up in numerous data bases with a dark cloud then the Software could suggest to each data owner that they have reason to ask particular other data holders about "Banks". At this point human judgment can enter the picture.

After his talk there was a rush to both Radio Shack and the casino.

CPMT Seminar:

In Reno at ECTC the CPMT seminar was held Thursday evening, May 31. The subject was "Advanced 3D Packaging Technologies" and the meeting was chaired by **Yoshitaka Fukuoka** of Weisti and co-chaired by **Kishio Yokouchi** of Fujitsu Interconnects Technologies, Inc. The meeting room was packed and so were the viewgraphs. For those that need the details it would be best to obtain copies of the visuals either from the speakers or from the "members only" section of the CPMT web site.

The first speaker was **Haruo Shimamoto** of Renesas Technology Corporation with "Technical Trend of 3D Chip Stacked MCP/SiP." He saw SiP as the driver of advanced packaging as a result of the increased I/O count, the higher data transfer rates (particularly from memory), need for less delay in data paths, and need for small volume. He saw flip-chip growing in popularity for SiP, continued improvement in through silicon vias for chip stacking, and a general expansion of 3D packaging.

Hiroaki Ikeda of Elpida Memory addressed "3D Stack DRAM using Through Silicon Vias." The driver for this industry is the need for x3 speed improvements in memory every 2 years and the need for x2 bits every 2 years. Clever stacking has been able to give the system designer the memory needed 6 years before Moore's law makes a monolithic solution possible. So the design goal is to stack while simplifying the data paths. He presented 8 memory chip layers in a stack with the internal bus connections. Where necessary interposers from Oki were used between layers. He discussed placing high temperature resistant poly-Si vias in the wafer before any transistor processing was performed (via first). To minimize the amount of poly needed the process leaves Si posts in the via which is about 28 microns in diameter resulting in 4 ohm resistance. Larger vias are made for power distribution. There is a redundancy of vias so that a circuit can be repaired if one via connection is substandard.

Naotaka Tanaka of Hitachi presented "Silicon through-hole Inter-

connection for 3D-SiP Using Room Temperature Bonding." His goal was heterogeneous stacking; a mix of memories and microprocessors. These vias were copper to achieve low resistance. The processes were designed to use existing equipment but the mechanical caulking method developed was new and used compressive pulses to deform the copper bumps into the laser drilled vias in the wafer. He claimed that even with 7% of the chip becomes vias it is still not fragile and can be handled with normal production equipment. Final assembly was possible using 10 micron alignment accuracy.

Yasumitsu Orii of IBM Japan discussed "Ultra thin PoP technologies with 50 micron pitch Flip Chip C4 Interconnection." The mobile phone push to have a TV option is pushing this technology, because they can add functionality and still keep the necessary thinness. The motivation for this research is the better yield of flip-chip on PoP than with wirebond on BGA. The process was developed so each package can be tested before assembly. He went into detail on the solder on copper post technology used where the crust of the solder is controlled so it helps the yield. This technology takes 3 years for IBM to qualify.

Katsumi Kikuchi of NEC Corporation presented "a High-Density SiP Technology for Inter-Chip Wide-Band Data Transmission. A technology named SMAFTI was developed for SiP to give high data transfer rate from memory to logic. Silicon was used for most layers to keep CTE match possible. For example the interposer was a 15 micron thick silicon patterned chip with the memory on one side and the logic on the other.. Copper vias 10-20 microns in diameter were used. Much development went into the resin overmold material and process to be compatible with the rest of the system.

ECTC Plenary Session:

The ECTC Plenary session was held Wednesday night, May 30, chaired by Wolfgang Sauter of IBM Corporation. The Panel theme was "Where does Packaging Research and Development take place: Current Trends and Production."

Wolfgang Sauter set the urgent tone by noting: (1) the cost of packaging must always go down, (2) outsourcing of assembly is increasing, (3) packaging complexity is increasing, and (4) one big source of packaging research, North America, is decreasing in publications at a rate suggesting "zero" research by the year 2032. (Fortunately most in the audience quickly realized they would be retired by doomsday).

Mostafa Aghazadeh

First, Mostafa Aghazadeh of Intel addressed where development will occur. The main driver is that critical tech development occurs where the suppliers are located, such as that needed for high density flip chip. The other driver is in competitiveness; costs are lowered by development/designs in geographies where customers vote.

He used an "Ecosystem" model. Just as many semiconductor companies were driven by cost to go "fab-lite", he suggested that a market with a broad set of specialty packaging technology vendors could provide better solutions than the past in-house solutions.

Mostafa predicted continued strong growth in both the chip and assembly business through 2010. He saw increased R&D by the assembly subcontractors in order to give them a market edge. However, with the increased cost of technology and complexity of assemblies, the push will be for more efficient use of R&D funds. This will lead to: (1) an improved model for collaboration in technology development, (2) a push of R&D upstream in the value chain, and (3) leverage consortium to derive a common agenda.

He predicted ever increasing interaction between wafer fab and packaging technologies as the scaling, Low-K, System-on-chip, and wafer level packaging trends continue. The boundary between fab back-end and assembly front-end may not exist anymore. Particular emphasis will be on thinning and bumping.

Geographically he sees the continued flight of electronics to Asia: assembly went in the 60s and 70s, fab lines in the 90s, and now system design. He pointed out that salaries in India and China are 25% of North America and that Asian countries produce 4 times the engineering grads.

Rao Tummala

Next Rao Tummala of Georgia Tech discussed the roles of universities in this R&D adventure. First is exploring all technology possibilities with a 10 year horizon. Although most will not reach production, it is important to consider all options. Second, the universities must educate the next generation of packaging engineers with (1) system perspective, (2) global view, (3) cross-disciplinary knowledge, and (4) leadership skills.

Rao pointed out that there were 50 universities active in packaging in North America, 35 in Europe, and 65 in Asia. These numbers had greatly expanded from the 1970s when most universities only studied circuits and silicon transistor fabrication. He pointed out that university work included blue sky and strategic research as well as technology development.

Rao emphasized SOP, system on the package, which combined the best of system and IC integration. However, today further IC integration only accounts for 10-20% of system size diminution. Whereas system integration (passives, antenna, power, interconnect) is the major driver.

Rao sees universities as complementary to the necessarily shorter future focus of industry. He pointed out projects at Georgia Tech supported by 50 companies. He pointed out Sony, IBM, and Intel as good partners for mutual research despite their past history of excellent vertical integration.

On a visionary note, Rao Tummala declared "miniaturization brings everything else." Going from today's cell phones that do about 10 different functions (audio phone, camera, voice recorder,

music play back, text message, gps, Internet e-mail), he projected in about a decade we would have affordable electronics systems of 5 cc volume with a million functions. To reach this goal, the weakest link to be strengthened is system packaging.

Wayne Howell

Next Wayne Howell of IBM discussed leveraging packaging technology for product innovation. He stressed we must have a Business Model innovation to make progress. There must be an efficient way to optimize the assets you have and the assets you must partner for. A business model must give guidance on when/how to partner and when to go it alone.

Wayne stressed the mantra "A package is a happy home for a chip" with the I/O as the only functional connections. His rules for the packaging engineer were:

1. Do no harm
2. Be transparent – as simple as possible
3. Enable more performance from the chips
4. Provide unique capability – build a market edge

The Howell taxonomy:

If it is possible it is exploratory research.

If it is useful it is technology development

If it is called product integration than it can be manufactured

Wayne Howell stressed that many companies were very innovative but few were on all three needed fronts: technology level, manufacturing level, and business level.

Robert Darveaux

Lastly Robert Darveaux of Amkor underlined much of what the previous speakers indicated but he emphasized that a

better Intellectual Property model is needed to foster quick, effective cooperation between potential package development partners. He listed a number of attempted cooperations that were scuttled by lawyers because the legal structure for IP was not mature in our industry.

Robert Darveaux also stressed that the business model is just as hard to innovate, maintain, and grow as the technology efforts most often discussed at ECTC. However one particular technology challenge facing industry is the testing of product with many functions and many layers of software.

ECTC President's Panel:

An exciting panel session occurred Tuesday May 29th at this year's ECTC. President William Chen led a discussion of future electronics technology entitled "When technology Meets market: More Moore and More than Moore." The large audience slowly figured out the title as the evening proceeded.

Chen pointed out that Moore's original article not only predicted that the number of transistors on an IC would periodically double but he predicted that complex electronics would be sold in department stores (this was before the term "big box stores" was coined. He also pointed out that economists look at the $1.4T share electronics has in the economy and see it as about the seventh largest contributor globally.

Bob Sankman

Bob Sankman from Intel started the discussion with the status of 45nm CMOS IC technology, "Challenges in 45nm and Beyond". He reviewed the start of 130nm in 2001 and suggested 45nm will begin in late 2007 – showing that the number of transistors are still doubling every 2 years.

To package this technology it will take the equivalent of 100 C4 bumps per square millimeter, which has proven possible. However, scaling pins at this density for 45nm will not be mechanically practical because of fragility. Bob made it clear that it is important for substrate experts to optimize very high density features to help solve this packaging challenge.

The substrate may also need low-K dielectric material. This will increase a problem since Low-K are mechanically weak materials and the many small bumps will bring high stress.

Another concern is that the next generation of ICs will have even more localized heating as groups of transistors switch fastest in one location or drive the longest lines in another location. To date heat spreaders and sinks treat chips as isothermal planes.

Lastly, packages are desired to be thinner. Thinner implies more warpage unless much more process and material development occurs. Design tools need to include signal integrity monitors while developing routing in the package.

Despite these hurdles for 45nm packaging, Bob Sankman saw no "show stoppers" even for the next step of 25nm CMOS.

Brandon Prior

Next Brandon Prior of Prismark spoke of high production volume systems that will drive the future with the title "Games Systems and Packaging Technology". Brandon felt that many of the packaging solutions are in place for next generations. Unlike cell phones, the game industry is producing product with X2 in size and X4 in weight from the last generation. This more powerful generation produces more heat and is still obeys the limitations of lower cost printed wiring boards.

Each generation lowers its price as it is revised. Silicon integration does take place to help lower costs, but the packaging challenges remain. Typical approach uses BGAs with an internal flip-chip. They use 200-250 micron bump pitch which is well established. For cost the BGA has a copper heat slug or a heat pipe. In general the game units get hot. Memory is sometimes within graphics processor package for speed. One recent challenge has been the evolution to Pb-free. SnAgCu solders are used.

The AMD/ATI fusion has influenced the game market. They are using the one package with many chips solution where possible. In addition, much integration to silicon is taking place.

Prior predicts that the tablet PC as the next killer application. In this case size and weight needs will require better board technol-

ogy. HDI-type technology adapted from mobile phones perhaps. The PoP, packaging on package, approach will be used where a memory stack is placed on top of a wire-bonded large die.

Petri Savolainen

Next Petri Savolainen representing Nokia in Finland presented "Packaging for Mobility, Intelligence & Style." He suggested something that the engineering audience had trouble accepting, namely that consumers often decide on which cell phone to buy based on "style" and not necessarily the best functionality.

He pointed out that the phone is becoming a computer to get e-mail and is taking on other functions such as photography. These increased abilities are often the goal now that the size race is no longer the main decider. Even though the size/weight is no longer the sole metric, "you can never be too thin."

Advanced Packaging is still the key to each generation of mobile phones. The quest for more phone intelligence is resulting in die stacking, package-on-package, and package embedded ICs. Tomorrows phones will need faster ICs which do not need larger batteries. The phone is the internet link most of the time for more people.

Given all this exciting component and packaging challenge, Savolainen reminded the audience that success in this arena without having your product make a fashion statement and passing the "looks cool" test would result in a business failure.

Herbert Reichl

Prof. Herbert Reichl of IZM Germany presented a "Research vision for More Moore and More". He discussed the European Technology Platform work labeled "Nano-electonics" but indicated that the whole advance electronics effort would be better called "heterogeneous Integration". By this Reichl meant the expansion of the system packaging to include batteries, antenna, and sensors. It would be a smart system with some components made "package-sized" by the use of nano-materials: advanced cooling, low-temperature interconnect, and self positioning.

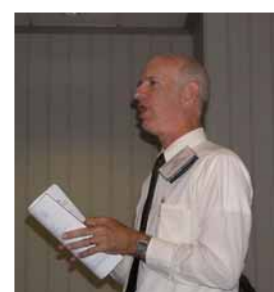
Reichl showed the "old" digital IC as only a part of the system with wireless, power supply and sensors also being integrated on the chip. He saw more of the historic "packaging" taking place at the wafer level further blurring the "back-end" from the assembly. He agreed that thinner was a continuing theme.

On the module level he saw polymer build-up technology with embedded passives not unlike the BCB-Cu technology that was popular a decade ago before the tech crash. He also saw the packaging build the battery layer by layer as the rest of the package was fabricated.

CPMT Publication Quality Strategy Meeting:

Early Friday morning at 57th ECTC 2007 meeting in Reno, Nevada, a CPMT Publication Quality Strategy meeting was led by Avram Bar-Cohen and Paul Wesling to improve Publications quality.

President William Chen set the tone for the 15 attendees stating: (1) we have improved the official impact metric of our Transactions over the last few years but they can become greater for all members benefit, (2) today's article cycle time can be slow and articles have been lost, (3) a lot of the quality of CPMT to our profession comes from our quality publications, and (4) as activities continue to move to Asia we must strive for more Asian reviewers, editors, and readers. "We are never too proud to improve."



Paul Wesling added that our publications serve a large community (80,000) in addition to our society members (3000). However, since IEEE Xplore Internet access to articles is virtually universal, we must optimize our quality for our much more transparent community.

Avi Bar-Cohen enumerated and facilitated discussion on the publication challenges. Since packaging science and engineering are intertwined, our Society must be a home for both the practitioners and the academicians. Often practitioners want immediacy and novelty in publications whereas professors are driven by citations and journal "impact factor". We must benefit both, since publications are key to the CPMT "value proposition."

IEEE Transactions expectations are (1) half of manuscripts finish first reviews in 3 months, and (2) No manuscripts are laggard for more than 12 months.

Our Transactions were born more than 60 years ago. Two reformulations in 1994 and 1999 resulted in our 3 current transactions:

- Components and Packaging Technologies
- Advanced Packaging (partnering with LEOS)
- Electronics Package Manufacturing

Each year 400 manuscripts are submitted and about 300 are published taking about 2100 pages to 5000 subscriptions. In addition, articles are called up by subject searches using Xplore.

A journal's "impact" is determined by the number of times its articles are referenced within two years after publication. Clearly the impact goes up if results are published quickly so others in the field have your current work, if other authors to our Transactions are aware of previous similar articles in the same Transactions (90% of references to our Transactions are in other journals), and if our articles are filed by the best descriptive titles and key words so they are found in computer searches.

Attributes of a High Impact paper:

- Original contribution of data, understanding, techniques, or process
- Furthers state-of-art
- Removes barriers for implementation
- Previously unpublished work
- Sufficiently detailed so the work can be repeated
- Clearly identifies prior art and how this work builds on that
- Written in proper English
- Right words in title and key word section so it can be found
- Clearly implemented so review process will go quickly

The path of the manuscript takes about 6 months from submittal to the mailed out Transactions. Quick response by the editors and authors can cut a bit of time from this but this remains the goal because typically busy schedules add some time to the process. To increase the value of the Transactions our Society will add an IEEE staff person to bird-dog the manuscripts. Editors will help authors with higher impact titles, references, and key words. Many of our best written communication remain in the "non-archival" conference Proceedings which does not have the reach and completeness of the reviewed/edited Transactions. It is hoped that these quality improvements will entice more conference presenters to do the extra work to help the profession through a Transactions paper.

Components and RF/Wireless TC meets:

Your Technical Committee concerning RF and Wireless as well as your ECTC committee covering Advanced Components and RF met for a breakfast meeting under the leadership of Mahadevan Iyer, Georgia Tech. Ten volunteers attended and Craig Gaw contributed over the speaker phone. Attendees included: Lih-Tyng Hwang, Tim Lenihan, Nanju Na, Hideki Sasaki, Len Schaper, Eric Beyne, Amit Agrawal, J. J. Maloney, and Dave Palmer.

This group is responsible for attracting many RF and Component papers for the ECTC meeting as well as for the Transactions. The sessions chaired by this group had about 100 attendees. It was stressed at the meeting that authors must submit advanced component papers through this group and not just RF component papers. The goal is 45 papers.

Nanja Na, J.J. Maloney, Hideki Sasaki, Lih-Tyng Hwang, and Mahadevan Iyer at Components and RF / Wireless TC Meeting

A list of past authors, future possible authors, and organizational volunteers was again updated in preparation for another year of ECTC preparation and member communication. A call for papers for the next ECTC was outlined with the final being released soon by Craig Gaw and Mahadevan Iyer. Some of the topics to emphasize were integrated passives processes and yield, high performance discretes such as decoupling capacitors, and high frequency modules.

Workshop Reviews:

Summary of the 10th European System Packaging Workshop Como, Italy

January 29th-31st, 2007

www.packagingworkshop.polito.it/

Submitted by Evan Davdison, IBM (Retired)

The Technical Committee on Systems Packaging had a very successful workshop in Como, Italy last January. Fifty-eight people attended. Most were from Europe with significant contingents from Asia and North America. It was a thorough program including topics on: wearable electronics, medical devices, portable equipment, 3D packaging systems, high-speed optical communications, electromagnetic simulators, microprocessor packaging, computer systems, process technologies, MEMS and market analysis. This breadth of papers was typical for a Systems Packaging workshop (the full program can be seen at the above website).

TCSP workshops focus on the need to integrate all aspects of an electronic system to create a product. Throughout its forty-year **history**, TCSP has been doing this. In this age of non-vertically integrated companies, external component vendors, contract manufacturers and outsourcing; our mission is especially important. The company that markets the final product has to create the system design, procure all the parts, build the prototype and be responsible for functionality, design integrity, design aids, component specifications, qualifications, cooling, and overall reliability. TCSP workshops are unique in the sphere of technical meetings by providing an emphasis on gluing all these total systems technology elements together at the final product level. Quite often the role of hardware integration falls to the system package designer and it is the needs of these people that TCSP meetings address.

The 10th European Workshop was chaired by Flavio Canavero (Politecnico di Torino) and Carlo Cognetti (STMicroelectronics) with help from Flavio's able assistant, Carla Giachino: the treasurer and logistics expert. Thomas Winkel (IBM Germany) and Cian Ó'Mathúna (Tyndall) were the Program Chairs. There were seven keynote presentations from the following well-known experts: Madahavan Swaminathan (Georgia Tech), Herb Reichl (Fraunhofer IZM), Len Schaper (U. of Arkansas) Carlo Cognetti (STM), Bob Guernsey (IBM USA), Christian Val (3D Plus) and Jan Vardaman (TechSearch USA). Some of these and other presentations can be seen at the workshop website.

There was a multitude of advanced work presented at this workshop. Most of it is already in products. Some of the key take-away points are:

- Thinness and low power in portable devices are new key drivers for semiconductor and packaging technologies.

- Computer, networking and telecommunication products are still driving performance and technology complexity for both semiconductors and packages.
- Embedded passives and optical waveguides on packages with on-chip electro-optical devices is finally ready for primetime.
- 3D packaging with through-hole vertical silicon vias and bump connection technology is making thin products even thinner.

The website contains many of the paper abstracts and presentation slides. To fully understand the comprehensiveness and value of this workshop, we encourage you to have a look.

Needless to say, Lake Como was a beautiful serene place to meet people and have a workshop that taught us so many new things. The next European workshop will be held in 2009 at Blarney, Ireland in County Cork: another wonderful place to learn and meet new friends. The 2008 Japanese TCSP workshop will be held in the beautiful Hakone resort region of Japan.

Check at the TC website (www.ewh.ieee.org/soc/cpmt/tc14/) for upcoming information.

Chapter Reports:

Backend Wafer Processing Technologies

Submitted by Dr. Mali Mahalingam, Tutorial Committee Chair, IEEE CPMT Society Phoenix Chapter

This half-a-day tutorial was taught on behalf of IEEE CPMT Society Phoenix Chapter on April 18th 2007. Dr. Mali Mahalingam, chair for the tutorials technical program worked with his fellow Phoenix CPMT officers in organizing this totorial. Four major areas of ***Backend Wafer Processing Technologies*** that precede and enable backend assembly and packaging were the focus of the tutorial. Forty six professionals took advantage of this professional learning opportunity.

Stacked Die Packaging and many consumer applications are driving ***Wafer Thinning*** technologies relentlessly. High performance applications demanding excellent thermal, electrical and mechanical performance for die attach are making continuous demands on ***Wafer Backside Metallization***. Flip Chip interconnect assembly is pervasive in high performance applications and now expanding to consumer applications thus propelling further growth in ***Wafer Bumping*** technologies. Numerous new challenges have arisen in ***Wafer Dicing*** due to use of Cu metallization and low-K dielectric materials in wafer fabrication. Each presenter presented an overview of basic technologies, discussed current challenges, and offered solutions in their respective areas.

Mr. Scott Drews, a Senior Applications Engineer for SEZ America, Inc. presented the topic of **Wafer Thinning.** As consumers demand greater product functionality in smaller packages, device manufacturers look for ways to integrate, through system-in-package (SiP), system-on-chip (SoC) and stacked die packaging. In order to maintain low die profiles in stacked die packaging, most manufacturers target final silicon thicknesses below 100um. While several methods exist for wafer or die thinning prior to packaging, manufacturers must take into consideration issues relating to process integration, waste abatement, reliability, die yield and cost-of-ownership when selecting which method (or combination of methods) to implement.

Dr. Jonathan Harris, President of CMC Interconnect Technologies, presented the topic **Wafer Backside Metallization.** Backside metallization of semiconductor devices followed by solder based die attach results in a die bond with excellent thermal, electrical and mechanical properties. The presentation focused on the back-side metallization of semiconductor wafers to achieve this type of high performance die attach. Both silicon and GaAs devices spanning applications in RF & Microwave, Power Control and Optical Devices were discussed. Various backside metallization systems, the design attributes for these metallization systems and the material science behind achieving key back side metallization requirements for each application were discussed. Deposition technologies including sputtering, evaporation and plating technology were discussed and compared.

Mr. Ted Tessier, Chief Technical Officer at Flip Chip International in Phoenix Arizona presented the topic of **Wafer Bumping: The Past, The Present and The Future.** After a rather lengthy period of development and adoption for high performance computing and automotive applications, wafer bumping and flip chip assembly technologies are now rapidly being accepted for use in consumer electronics and handheld communications applications. From these initial Flip Chip in Package beginnings, a number of bumping technologies have emerged to support a wide range of semiconductor device requirements and packaging applications. This presentation provided an overview of the history of wafer bumping technologies including the adoption of thin film redistribution options to broaden the applicability of wafer bumping to ICs designed with wirebond centric peripheral pad arrangements. The emergence of Wafer Level Chip Scale Packaging (WLCSP) was discussed and the differences between flip chip and WLCSP bumping technologies were compared.

Mr. Alan Magnus, a Member of the Technical Staff at Freescale Semiconductor Inc. in Tempe, Arizona, presented the topic of **Wafer Dicing.** The drive for low cost microelectronics with enhanced electrical performance has introduced wafer fabrication materials and advanced packaging requirements that present an ever increasing challenge for the wafer dicing operation. Some complications stem from the wafer fabrication materials such as multi-level interconnects of Cu metallization and low k interlayer dielectric materials. Packaging constraints play a role through die thickness and mechanical strength requirements, as well as bumping or back metal needs. Finally economic issues, whether reduced scribe widths to increase the number of good die per wafer,

or simply cost reduction at saw through increased feed speeds and blade life all contribute to the increasing difficulty of dicing wafers. This presentation provided an overview of the wafer dicing process and the available dicing technology options. More focused discussions were on mechanical saw and the key process parameters that need to be optimized in order to meet the growing process challenges.

The First CPMT Micromouse Best Packaging Award

Submitted by Allen M. Earman, CPMT-SCV Chapter Vice-Chair

It has been years since I witnessed an IEEE Micromouse contest – many years. The Micromouse competition has been around for decades. IEEE Spectrum Magazine first introduced the microprocessor-controlled, autonomous Micromouse in 1977 with the first competition held in June 1979. I was a graduating Senior at Virginia Tech in June 1979 and the *new* Micromouse competition was a much talked about topic in the EE department that year. Back then there were no "Tips & Tricks" webpages, or even articles on the subject. Still, more than 6000 teams across the United States submitted their entries to the IEEE competition that year.

Flash forward twenty-seven years to January 2006: As the Chapter Chair for the Santa Clara Valley chapter of CPMT, I was busy putting together my Chapter Goals for 2006. Along with the usual topics of "Improve Chapter Finances," and "Increase Chapter Membership," I was looking for something new to engage the IEEE student members at the local universities. Our chapter already was quite involved at the student level as we were in the final stages of establishing a CPMT Student Chapter at San Jose State University. In April of that year, the SJSU CPMT Student Chapter received its charter as only the sixth CPMT Student worldwide and only the third in the U.S. But,…What else could we do? More importantly, "What else could we do – within the range of our local chapter capabilities?" Enter the Micromouse. I don't recall precisely from where the idea came. Perhaps I was trying to remember what excited me all those years ago as an undergrad EE student – tempered with the hoary experience of 25 years in new product development. The idea gelled. What if the Micromouse was more than an apparatus for autonomous navigation of the maze? What if the Micromouse was a New Product? What would you need to consider if you were planning to engineer the device for introduction as a consumer product? How would you design and build it?

Being an active member of CPMT and involved in the packaging and reliability of new products in my work life, several things immediately sprang to mind: power consumption, thermal management, size/weight, RFI/EMC, and quality and reliability. This might work! The Santa Clara Valley Chapter could sponsor an Award for "Best Packaging" for a Micromouse Competition! Thus, began the idea that resulted in the first CPMT Micromouse Best Packaging Award presented at the Region 6 – Central Area Spring Meeting at California State University at Chico in April 2007.

As to be expected, something like this does not happen overnight. There were many steps of intermediate accomplishment on the way to the actual prize award. First, our local CPMT chapter agreed to our stated goals for 2006. Next, I needed the support of the Director and Student Activities Chair for Region 6. This process began as a series of e-mail messages describing the concept to the Region 6 officers. Some thought it an admirable concept, others thought it would detract from the primary Micromouse competition. After a few back-and-forth messages with ever increasing length and detail, it was suggested that I produce a Formal Proposal to Region 6 Executive Committee that could be reviewed and voted upon at the next ExCom meeting. The proposal was accepted with the conditions that I also provide a complete set of contest Guidelines, Entry Form, and that our CPMT chapter – as financial sponsor of the award – transfer the funds for the award to the Region 6 treasurer at the beginning of the 2007 fiscal year so they would be available for the competition in Spring 2007.

Since the first intra-school Micromouse competition is held at the Area-level – with the winner going on to compete at the Region-level, our chapter decided to sponsor the award for our Area, the Region 6-Central Area. The Best Packaging Award would, therefore, be an additional prize for the Area competition only. After all, we are only a local chapter. There are 23 universities in the Region 6-Central Area that have active IEEE Student Branch Chapters. And more than one team can compete from each school. So, the potential for a large field of entries was high. The next step was to *get-the-word-out* to the Central Area schools. Initially, the Region 6 officers said that our Contest Guidelines and Entry Form would be posted on the Region 6 Student Activities webpage.

Early March 2007: Eight weeks to the Central Area Spring Meeting. And no posting of the Best Packaging Award information on the Region 6 webpages. Panic starts to set in!

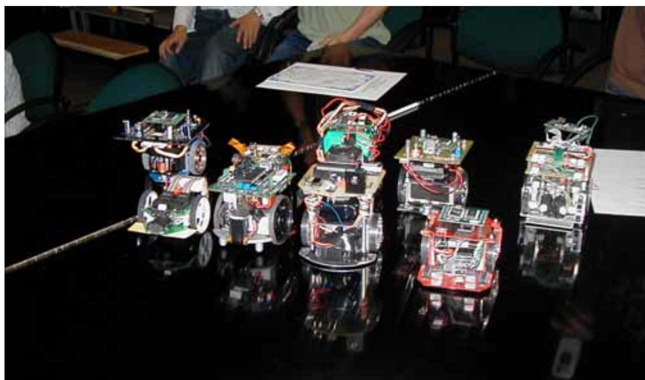
A few more e-mail messages later and I discover that Region 6 leaves these things up to the Area Chairs. A quick search for the Central Area webpage yields a single, short, unadorned page that simply notes the date and location for the Spring Area meeting. Well, at least now I know it will be held at Cal-State Chico! But, how do we get the word out for this new contest? To my rescue – and the rescue of the Best Packaging Award for 2007 – is the Region 6 Regional Student Representative, Lise Johnston. Lise led me through the learning curve for the IEEE e-Notice announcement tool and provided me with the full list Central Area Student Branch Chapters. With this new tool in hand, I quickly distributed the Best Packaging Award Guidelines and Entry Form to all of the Student Branch members in the Central Area of Region 6 – to 14,986 student members!

Mid-April 2007: Less than two weeks to go. Time to start thinking about the logistics of judging the competition. I had generated a Judges Form for scoring the contestants back in the Fall of 2006 along with the Contest Guidelines. And the Guidelines spelled out the evaluation criteria and scoring in detail. Power consumption would be derived from the Micromouse battery configuration – number of cells and rated capacity (Ampere-hours) per cell. Special Bonus points would be awarded for use of rechargeable and recyclable batteries. Thermal management would be evaluated by measuring the hot-spot temperature of the Micromouse with an infrared temperature probe. Initially, we would measure the Micromouse at both quiescent (on, but not running), and op-

erational (on, and running) conditions. However, at the actual competition we discovered that several of the Micromouse devices only functioned in the "run" mode – as soon as they were turned on, they would start moving and try to navigate the maze. So, we dropped the quiescent temperature measurement. Micromouse size and weight would be measured with tape-measure and scale.

The two more complex measurements would be RFI/EMC and audible noise level. These would require additional test equipment such as a digital oscilloscope and a sound level meter. Quality evaluation would be subjective by the judges based on workmanship of the assembled Micromouse – was it well layout, good assembly, etc. Finally, we included a Product Design category in which we would evaluate each Micromouse device on the aesthetic design appearance, creativity, markings (branding), and human-factors such as ease of use and location and accessibility of controls.

Our CPMT chapter decided to send two of us to be judges for the contest – an excellent idea as I will explain shortly. Luu Nguyen, CPMT Fellow and active member of our chapter, had been our *forward scout* and attended the Central Area meeting and Micromouse competition in 2006 at Cal-State Fresno. Luu brought back valuable information on the schedule of events and the modern Micromouse devices. Luu and I assembled our test equipment for the task: a Tektronix digital hand-held oscilloscope with RF antenna, hand-held infrared temperature probe with laser targeting, Extech hand-held digital sound meter with background rejection and peak-hold, notebook PC, digital camera, tape-measure, and bathroom scale (for Micromouse weight measurements). Since we were venturing into an unknown venue, we also included a workshop AC power strip and heavy-duty extension cable, a folding PC table and folding chair, small hand tool set, extra batteries, and a rolling, collapsible crate to carry all the gear. Almost all of which we used – we did not need the extra batteries after all. Also, I created an Excel spreadsheet for recording and tabulating the scores for the contestants that calculated the overall scoring results and gave us the winner as soon as we had entered the data form the last contestant.



Eight Micromouse Contestants sitting on the baby grand piano in the Performing Arts Hall

Competition Day, April 28, 2007, Chico California: Luu and I arrived at the Central Area meeting with our crate of equipment in tow. During the morning presentations I gave a brief presentation on the CPMT Best Packaging Award. There were nine Micromouse Teams from five universities: CSU-Chico, University of Hawaii-Honolulu, University of Hawaii-Manoa, UC-Davis, and San Francisco State University. Seven of the nine contestants also entered the Best Packaging Competition. Each of the Micromouse teams had given their Micromice clever names. The Chico State teams were Juanito 5 Jr., and Remington Plastic. The University of Hawaii fielded Ramrod, The Prodigy, and A.I. from Manoa. The SFSU entry was Gold Digger and the UC-Davis Micromouse was Rat-Zilla.

Following the morning presentations, the Micromouse teams were allowed to go to the competition hall where the maze was set up for some practice and last minute adjustments before lunch. During lunch the maze would be reconfigured for the actual competition that would start right after lunch. So, off the teams went across campus to the competition hall in the Performing Arts building, along with Luu and myself – and our crate of equipment. Once there, we had about one hour to set up our equipment and judge seven contestants on seven areas – while the teams tried out their Micromice in the practice maze and not a few people tried to figure out what Luu and I were doing with all this equipment. We struggled a bit with the first two contestants – such as discovering that the Micromouse would not just sit there once it was turned on – it would run toward the edge of the table, looking for the maze. We quickly found a few excess maze-wall segments to use as *blocks* to lift the Micromouse wheels off the table for the evaluations. We sadly discovered that our bathroom scale had a minimum weight that exceeded the typical weight of the Micromice – leaving us no means of weighing the contestants. We also discovered that the background rejection feature in our digital sound meter proved exceptionally useful as the crowd of curious onlookers kept the ambient sound level at a consistent 36 dBA.

A practice run through the Maze

By the third contestant Luu and I got the hang of the procedure: I would photograph the Micormouse and measure the dimensions while Luu checked on the battery configuration and rating. I would measure the frequency and amplitude of the RF emissions while Luu measured the hot-spots with the infrared probe and the Micromouse on blocks. I would measure the audible noise level and Luu would inspect the workmanship and product design aspects while I entered the data in the spreadsheet. As the teams were ushered out of the room promptly at noon so that the final maze configuration could be assembled, we had just completed the sixth Micromouse. We had to wait until the beginning of the Maze Competition after lunch to judge the seventh and final Micromouse.

All of our category scoring was relative. The measurements were rank ordered and the top three contestants received 5, 3, and 1 points – or, 3, 2, and 1 points, depending on the category weighting. The rest of the contestants received zero points. The final, overall scores ranged from 4 points to 18 points, with the top three finishers scoring 18, 14, and 13 points. We had clear Win, Place, and Show finishers. For the next couple of hours, we got to sit back and enjoy the Maze Competition.

The heat of competition

The meeting reconvened back in the original meeting room for the awarding of the prizes. The Maze winner was the UC-Davis team with Rat-Zilla – successfully navigating the maze in 38.9 seconds on it s first attempt! Interestingly, the same UC-Davis team won the Maze Competition in Fresno in 2006. Could this be the start of a dynasty? To the surprise of the attendees – and to the teams – Rat-Zilla also took the Best Packaging Prize with Juanito 5 Jr. and Ramrod taking second and third. Rat-Zilla excelled at having the smallest volumetric envelope, lowest RF emission, and the second-lowest audible noise level. Rat-Zilla was unique in its use of AC pancake motors (used in magnetic disk drives) for its main drive. These motors were exceptionally quiet and very fast. Many of the other contestants used noisy stepper motors to move the Micromouse from square-to-square in the Maze. Also, the UC-Davis were the only team to "brand" their Micromouse with the Rat-Zilla name and UC-Davis emblazoned on the unit – thus earning themselves sole points for Product Design Markings. With First Place in the Maze competition and the Best Packaging award, the UC-Davis team went home with an extra $1,000 for their student chapter.

The overall Winner of both Maze and Best Packaging, Rat-Zilla from UC-Davis

Following a few concluding remarks from the Central Area Chair, Ron Kane, Luu and I packed up our crate of equipment and headed off across the Central Valley back to the Bay Area and Santa Clara with a full list of successes & opportunities for next year's judges – and a lot of memories. After 16 months of development from initial idea to implementation and the first award, we were quite satisfied in the results. All of the student teams were very interested in our evaluation process, the methods and equipment we used, and the scoring criteria. Why were these particular measurements important? Do all new products go through this type of testing? For us, the real question was, "Did we succeed at our original goal – the engagement of IEEE students in the fundamentals of packaging design, design for manufacturing, design for reliability, and product design?" Undoubtedly, there was the spark of interest in the Micromouse teams. The design project criteria for the Micromouse just expanded from performance capability to product design and reliability – from circuits, software, and feedback loops to power consumption, heat dissipation, and RF and audible noise – to packaging, manufacturability, and reliability – to the CPMT Society.

Bill Allan and Michael Cheng from UC-Davis accepting the First CPMT Micromouse Best Packaging Award from Allen Earman from CPMT-Santa Clara Valley

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IEEE CPMT Society Newsletter

Send inputs, suggestions, and articles by email to nsltr-input@cpmt.org

….. Editor

OUR SINCERE THANKS TO ALL CONTRIBUTORS TO THIS ISSUE

DEADLINE FOR SUBMITTING ARTICLES FOR SEPTEMBER, 2007 ISSUE AUGUST 25TH, 2007

Newly Published Papers … a profile

The June issue of the Transactions has a Special Section that reflects the current challenges faced by the industry in microscale liquid cooling, thermal interface material development, interface resistance minimization, and stacked die.

I've included Guest Editor John Parry's summarizations below:

Thermal Metrology of Silicon Micro-Structures Using Raman Spectroscopy

As integrated circuit (IC) feature sizes continue to reduce, so the challenge of measuring their temperature increases. Abel et al. used Raman spectroscopy to measure temperature and thermal stress of an electrically active silicon cantilever and polysilicon micro-beams with a resolution of close to 1 m, with results within 10% of the finite element model predictions.

On-Chip Liquid Cooling With Integrated Pump Technology

Oprins et al. introduce an on-chip liquid cooling system for microchannels with integrated pump, using an applied ac signal to cause a droplet to fill and empty a 100- m microchannel. Having found a critical filling period, the authors conclude the proposed novel electrowetting system is promising, enhancing cooling capacity by more than 50%.

A Practical Implementation of Silicon Microchannel Coolers for High Power Chips

Colgan et al. describe the design, fabrication, and testing of a practical implementation of a single-phase silicon microchannel cooler for bonding to high power chips. Being fabricated in silicon it can be rigidly bonded to an active die, for example with solder. The authors demonstrated its ability to cool a 300 Wcm thermal test chip.

Hierarchically Nested Channels for Fast Squeezing Interfaces With Reduced Thermal Resistance

Brunschwiler and co-workers at IBM have found a method to reduce the thermal resistance of thermal interface materials by the use of a hierarchy of grooves cut into one of the surfaces, reducing bond line thickness and dry-out, by allowing the paste or grease to flow under thermal cycling.

Rudimentary Finite Element Thermal Modeling of Platelet-Filled Polymer-Ceramic Composites

To investigate the influence of filler geometry on interface material performance, Hill and Strader have modeled polymers loaded with platelet-shaped titanium diboride and boron nitride fillers, providing insight into the observed behavior of these materials, which exhibit a sharp increase in thermal conductivity as their volume fraction is increased.

You may quickly access these 5 papers, and others from the June 2007 issue, at:

ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=6144

(Bookmark this URL.) Select Volume 30, Issue 2. You can also elect to scan earlier Tables of Contents for papers that lend important context to the work you are currently doing. Or use XPLORE's full-text search capability to scan across the full IEEE collection of 1.2 million articles.

Most of our Members belong to institutions or companies with full subscriptions to the **IEL/XPLORE** system, and so can download any papers of interest without additional cost. If your company does not have IEL access, please contact **Paul Wesling** for information on the various subscription plans that are available: **p.wesling@ieee.org**

Invitation to Attend the combined ….

International Symposium on

Advanced Packaging Materials (APM 2007) and the

Int'l Electronics Manufacturing Technology Symposium

October 3-5, 2007 Holiday Inn San Jose/Silicon Valley, CA USA

The **Advanced Packaging Materials Symposium** (APM 2007) is an international premier technical event on electronic packaging materials organized by the IEEE's CPMT Society and its Santa Clara Valley Chapter. APM 2007 features Keynote talks, technical presentations, and exhibits. The Symposium provides leading-edge coverage of developments in all areas of packaging materials and processes. Attendees in the past have included academic researchers, developers, producers, and users of packaging materials from all over the world. APM is also a major packaging materials forum, providing opportunities to network and meet leading experts and exchange up-to-date packaging knowledge in the field.

The 32nd **International Electronics Manufacturing Technology** (IEMT) Conference is the premier IEEE event devoted to the manufacture of electronic, opto-electronic and MEMS/sensors devices and systems. IEMT is an established International conference of long standing organized by the CPMT Society. Through well-mediated technical papers IEMT offers manufacturing technologists as well as designers a single convenient forum to assess new packaging and assembly technologies about to enter production or in production around the world. In addition, IEMT also provides attendees the opportunity to meet leading domain experts and network with colleagues.

Exhibition

A tabletop exhibition featuring suppliers of materials, equipment, components, software, and services to the electronics industry will also be held at the venue of the symposium. Please contact Annette Teng for more details about exhibiting: Annette@corwil.com

Dr. Srinivas Rao, Flextronics, General Chair, IEMT
Dr. Dongkai Shangguan, Flextronics, Gen Chair, APM
Choong Kooi Chee, Intel, Vice General Chair, IEMT
Dr. KRS Murthy, Program Chair, IEMT
Dr. Paul Wang, Microsoft, Program Chair, APM
Azhar Aripin, OnSemi, Vice Program Chair, IEMT
Paul Wesling, Administration Chair, IEMT & APM

Welcome to Silicon Valley and "California Casual," as we gather in the atriums, patios, pool, fitness center and session rooms of the Holiday Inn San Jose. Our venue is a Mediterranean resort-style hotel nestled in a beautifully landscaped 17 acres in the heart of Silicon Valley. So near Silicon Valley's action – so relaxing and informal, for our focus on technical interchange. And you are only steps from the Santa Clara Valley's Light Rail line, for quickly heading downtown or to other destinations. We are minutes (1.6 km / 1 mile) from San Jose International Airport, with complimentary shuttle to/from the hotel.

Professional Development Courses:

Wednesday Oct. 3 is devoted to morning and afternoon PDCs to allow you to quickly master new skills and disciplines that will be useful as you tackle current challenges or new opportunities.

Sessions on:

- **Materials for Electronics**
- **Nano Materials, Nano-Toxicology**
- **Lead-Free Experiences and Challenges**
- **Design for Environment/Recycling**
- **Embedded Passives**
- **Manufacturing Technology**
- **Testing**
- **Packaging Integration Applications (SiP, WLP, etc)**
- **MEMS and Sensors Manufacturing**
- **Display and Opto Manufacturing**
- **Materials for Packaging Applications**
- **Poster Papers**

Register today! Attendance is limited by the nature of the facilities, to allow better sharing and interaction.

Please visit our websites:

www.cpmt.org/iemt or **www.cpmt.org/apm**

One admission allows entry to sessions across both Symposia

EMAP2007 -- **International Symposium on Electronic Materials and Packaging**

November 19-22, 2007
KAIST (Korea Advanced Institute of Science & Technology), Daejon, Korea

You are invited to submit a paper for the EMAP2007. The EMAP2007 symposium is organized by KAIST in collaboration with the Center for Electronic Packaging Materials (CEPM). It is jointly sponsored by the IEEE CPMT Daejon Chapter, IMAPS-Korea, Korea Society of Mechanical Engineers, Korea Society of Electric Engineers, and ASME Korea Section. The objective of this symposium is to create an international forum for the exchange, dissemination and discussion of state-of-the-art technologies and recent developments in electronic materials, packaging and assembly. Following the tremendous success in the last eight conferences in Singapore, Hong Kong, Korea, Taiwan, Malaysia and Japan, which were attended by delegates from more than 10 major countries, the ninth symposium will be held again at the KAIST campus at Daejon Korea. So come and meet world-renowned authorities from the Asia-Pacific region, USA and Europe. Join us and get in touch with leading-edge electronics packaging technologies, and find out more about Korea's electronics packaging industries. In addition, short courses on current packaging trends and technological issues will be also offered. Papers are invited from industry participants as well as researchers from the academia and government research organizations.

Call for Papers (abstracts due **July 31**)

Major Topics of the Symposium:

- Advanced Electronic Packaging Technologies: WLP, Flip Chip, CSP, SIP, SOP, 3-D
- Packaging Materials and Processes: Lead-free Solders, Adhesives, Underfills, Encapsulants, PCBs
- Interconnect Technologies: Wire bonding, Fine Pitch, Micro via, Build-up Technologies
- Materials Characterization, Testing and Measurements: Electrical, Thermal, Chemical, Mechanical
- Package Design, Modeling and Simulation
- Sensors/Bio/MEMS Packaging
- Reliability and Failure Analysis: Interfacial Phenomena, Delamination, Moisture effects
- Polymers and Ceramics for Electronic Applications, Thin films/coatings, Metallization

Abstracts and Papers

A one-page 300-word abstract should be submitted to the Secretariat of the Symposium, describing the scope, contents and key points of the proposed paper. Instructions for preparing the full paper will be sent to the authors whose abstracts are accepted after review. Participants will be required to register upon notification of acceptance of their full papers. The detailed conference information will be announced later at the website, **emap.kaist.ac.kr**. If you have any questions, please send an e-mail to **emap@kaist.ac.kr**.

Institute of Electrical and Electronics Engineers, Inc. Phoenix Section CPMT Chapter & Waves and Devices Chapter Present an all-day Workshop on:

Emerging Device & Packaging Technologies

The semiconductor industry is entering an era with tremendous opportunities to exploit emerging technologies for the benefit of widely diverse markets. Moore's Law requires increasingly intensive materials innovations to maintain its momentum. Meanwhile, new markets in the areas of bioelectronics, sensors, etc., are leveraging the existing manufacturing infrastructure while incorporating new materials and techniques. This one-day workshop will bring together experts from industry, academia, research labs, and consortia to share their technology roadmaps and visions, novel materials and methods, and discuss technical opportunities. The status and challenges facing device, interconnect, and packaging technologies will be discussed in depth. An expert panel discussion will bring a closure to the day's workshop. Vendors will be on hand to exhibit products and services in all aspects of the supply chain for IC, packaging, and module design and manufacturing.

Date: Friday, November 9th, 2007
Time: 7:00 A.M. – 5:00 P.M.
Location: Arizona State University, Tempe, AZ USA

Topics

- Nanotechnology and Continuum Model Limits
- ITRS Roadmap Challenges
- SiP: 3D, Modules, Discrete Passives Integration
- Flexible Electronics
- Green Materials and Packaging
- Bioelectronics and Sensors Technologies
- General Industry and Technology Visions
- Panel Discussion on Future Challenges and Opportunities for Emerging Technologies

For General Information, visit:

www.ieee.org/phoenix

For Additional Information, contact:
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Dr. Chuck Weitzel (Co-Chair), +1-480-413-5906
For Workshop Registration Forms:
Sergio Pacheco, +1-480-413-3737
For Vendor Registration Forms:
Vladimir Noveski, +1-480-554-2375

International Microsystems, Packaging, Assembly and Circuits Technology (IMPACT) Conference

In line with its very strong IC foundry industry for more than 30 years, Taiwan has also developed into a pivotal position in the world's IC packaging, testing and PCB arena. Considering the global number one revenue generated by Taiwan industries on packaging (44.8%), testing (60%) and PCBs (25%), the **International Microsystems, Packaging, Assembly and Circuits Technology (IMPACT)** conference will take place at Taipei International Convention Center Taiwan on October 1-3, 2007. Original and unpublished papers on all aspects of microsystems, packaging, assembly, and PCBs are solicited.

IMPACT Conference Keynote Speakers

Dr. Michael Pecht, University of Maryland, USA
Dr. C. P. Wong, Georgia Institute of Technology, USA
Dr. Kazuhiko Hashimoto, SONY, Japan
Dr. Dongkai Shangguan, Flextronics, Asia Pacific

Organized by ITRI, IEEE's CPMT-Taipei Chapter, IMAPS-Taiwan and TPCA, and with technical co-sponsorship by the CPMT Society, the **IMPACT** conference and TPCA Show 2007 is expecting to create Packaging and PCB – Taiwan to bring together scientists and engineers actively engaged in research and development on microsystems, IC packaging, assembly and PCBs to discuss current progress and emerging technologies in these fields.

IMPACT Conference: Mon.-Wed, Oct. 1-3, 2007
Taipei International Convention Center
AFEC Conference: Wed, Oct. 3, 2007
Taipei International Convention Center
Exhibition & TPCA Show: Wed.-Fri, Oct. 3-5, 2007
Taipei World Trade Center (Hall I & Hall III)

Vist the IMPACT Website:

impact.itri.org.tw

31st International Spring Seminar on Electronics Technology "Reliability and Life-time Prediction"

7-11 May, 2008
Budapest, Hungary

ISSE is the premier European forum for the exchange of information between young scientists from academic communities and electronic industries from around the world on topics related to their experimental and theoretical work in the very wide-spread field of microelectronics technology and electronics packaging. Based on a unique combination of oral and poster presentations as well as individual meetings, senior and junior researchers can come together to discuss scientific problems and organize international cooperation and student exchanges in a convenient atmosphere during three conference days. It is our pleasure to encourage you to participate in ISSE 2008.

the **International Academic Conference on Electronic Packaging Education and Training** will take place at the same venue on 7th May 2008. The aim of the Academic Conference is to catalyze education innovations by bringing together faculty from around the globe. For this purpose, academic people in the field of Electronic Packaging are invited rom North America, Asia and Europe to exchange their knowledge and experience.

Topics of Interest:

- Reliability physics: analysis and life time-prediction in electronics;
- Non-destructive testing, picture acquisition methods;
- Nanotechnology, nanomaterials and nanoelectronics;
- Advanced packaging, new packages and materials, opto-electronics, optical interconnection technology;
- System on chip, system in package;
- Manufacturing processes, process simulation and optimization;
- Innovations in printed circuit board, thin film and thick film techniques;
- Education and information technology in electronics technology;
- System modeling, CAD/CAE in packaging;
- Bio-compatible electronics packaging, environmental, ecology, and toxicology issues in electronics technology

For more information on ISSE 2008, please visit:

www.isse-eu.net

2007 ASME/CPMT **Interpack Conference** *colocated with the*

JSME Thermal Engineering & ASME Summer Heat Transfer Conference

Vancouver, BC, Canada July 8 – 12, 2007

We are pleased to bring these two premier conferences co-located in beautiful Vancouver, allowing engineers to expand their technical horizons through participation in both conferences under one roof. We hope you will be able to meet with hundreds of colleagues, exchange ideas and technical information, and learn of the latest technical advances in heat transfer and electronic and photonic packaging disciplines and industries. We have designed the conferences to provide you great value - one registration fee covers both conferences.

Highlights of the conferences include:
- Over 250 papers/12 technical tracks for **Interpack**
- Over 400 papers/18 technical tracks for AJTEC/SHTC
- Learn from experts offering 20 tutorials covering a wide range of topics on Sunday
- Hear insights from leaders in the field during keynote and panel sessions every day
- Over 30 exhibitors showing their latest products
- Socialize with colleagues at welcoming reception and everyday food functions

For only $100 you can attend any of 20+ tutorials and obtain all the tutorial materials

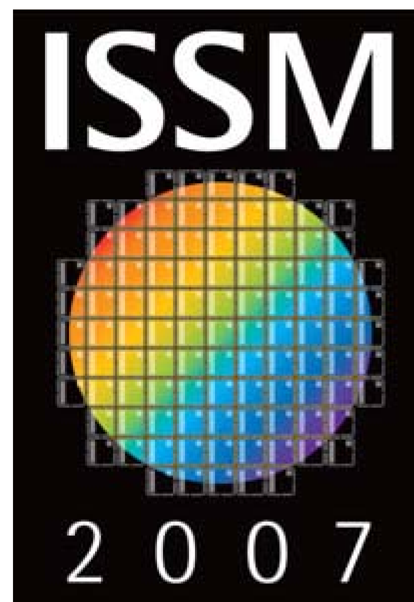
The session schedules for both conferences are posted on the website. Please register today:

www.interpackconference.org

International Symposium on Semiconductor Manufacturing

"Maximizing Operational Efficiencies at the Leading Edge"

October 15-17, 2007
Santa Clara, CA, USA
Marriott Hotel



Featured Keynotes:

Michael Splinter, President and Chief Executive Officer
Applied Materials, Inc

"Optimizing Fab Performance"

An analysis and vision for the next generation of wafer fabs, highly efficient, lower energy and environmentally sound.

Nick Bright, Executive Vice President, Products,
Lam Research Corporation

"Technology and the Equipment Industry"

Historically, Moore's Law has been used as the guiding light for cost and performance in the semiconductor industry. Will this be the case going forward? If not, how will it affect the equipment companies?

Founded in 1992, ISSM is the industry's largest assembly of semiconductor manufacturing professionals dedicated to driving technology innovation and operational excellence within the industry. Currently, ISSM alternates between the US and Japan with the goal of providing an open global forum for the introduction and promotion of new concepts to advance semiconductor manufacturing.

For more information, and to register:

www.issm.com

8th International Conference on Electronics Packaging Technology (ICEPT 2007)

August 14th – 17th, 2007, Shanghai, China

Since 1994, ICEPT has been held seven times in Beijing, Shanghai and Shenzhen, China. Each ICEPT has attracted hundreds of participants from colleges, research institutes, packaging testing manufacturers, packaging testing equipment factories, packaging materials factories including distinguished experts, scholars and enterprises. The conference is highly focused on semiconductor packaging design, semiconductor packaging manufacturing, semiconductor packaging testing, LED packaging, MEMS packaging, system packaging and assembly. We sincerely invite your participation.

Advance Program Now Posted

More information: Visit our website

www.icept.org

Topics for ICEPT'2007:

Advanced Packaging & System Packaging: BGA, CSP, flip chip, WLP, nano-packaging, Cu/low-K packaging, 3D packaging, SiP and other advanced packaging and integration technologies.
High Density Substrate & SMT: HDI, PCB, high performance multi-layer substrate, embedded substrate, micro via, microjoin, stencil print, reflow, and other novel assembly technologies that improve substrate density and performance.
Packaging Design & Modeling: novel designs for various packaging/assembly, modeling, simulation and characterization solutions for electrical, thermal, optical & mechanical properties, multi-function & multi-scale modeling, simulation, validation.
Packaging Materials & Processes: interconnection and encapsulation materials including bonding wires, solder balls, solder pastes, conductive pastes, plastic packaging materials, adhesives, thin-films, dielectric materials, frame materials, green electronics.
Advanced Manufacturing Technology: photolithography, laser processing, novel packaging/assembly technologies, advanced methods/software for modeling and monitoring of process effectiveness and cost analysis, and related manufacturing equipment.
Emerging Technologies: sensors, actuators, MEMS, NEMS and MOEMS, optoelectronics & LED packaging, LCD, solid state lighting, passive and RF devices, power & HV devices, nano dvices based on nanowire, nanotubes and polymers, etc.
Quality & Reliability: Quality monitoring and evaluation for packaging/assembly, advanced methods/technologies/tools for rapid reliability data collection and analysis system, reliability issues in emerging technologies.

Future Directions in IC and Package Design Workshop (FDIP)

October 28, 2007 Atlanta, GA

Organized by the CPMT TC on Electrical Design, Modeling, and Simulation (TC-EDMS)

Held just prior to the
Electrical Performance of Electronic Packaging Conference
October 29-31, 2007

For full information and to register, visit

www.epep.org

CALL FOR PAPERS

58th ECTC

ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE

May 27 – May 30, 2008
Orlando, Florida

OPTOELECTRONICS

Papers are solicited on all topics pertaining to the design, development, and technology of packaging optoelectronics and photonic components, devices, circuitry and systems

Topics of interest include:

- **High Power Optoelectronics and Fiber Laser Packaging:** High-power laser diodes, bars / stacks, and Fiber lasers – including beam combining, coupling, wavelength control, hermetic packaging and thermal issues.
- **High-Brightness LED Packaging for Lighting and Commercial Applications:** Package and optical design, assembly methods, thermal management, reliability, color temperature control, phosphor materials, and volume manufacturing.
- **Optical Component Thermal Management and Reliability:** Optical component thermal management, package design, device performance, failure modes and reliability
- **Micro-optical Packaging and Manufacturing Technology:** Low cost designs, novel optics, assembly methodology and automation technology
- **Silicon Photonics Devices and Packaging:** Optical devices in Silicon, hybrid integration, FR performance, Silicon optical waveguides, photonics circuits and packaging
- **Optical Interconnects:** Integrated optics, high-speed and parallel transceivers, board-level waveguides, optical backplanes, fiber optic connectors and hybrid integration
- **Advanced Materials for Optoelectronics:** Substrates, devices, components and assembly materials

You are invited to submit at 500-word abstract via the ECTC Website http://www.ectc.net

PLEASE SELECT OPTOELECTRONICS AS YOUR PRIMARY COMMITTEE FOR SUBMISSION

(You may also submit directly to the committee chairs below – please include mailing address, telephone number, FAX number and e-mail):

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Abstracts Due: October 15, 2007

Mark your calendars!

9th Electronics Packaging Technology Conference (EPTC 2007)
December 10-12, 2007 Singapore

The 9th Electronics Packaging Technology Conference (EPTC 2007) is an International event organised by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society.

This Conference will bring together researchers, engineers and practitioners involved in the development of integration technologies and packaging. The participants will also have the opportunity to interact with the other delegates by the means of plenary talks. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

The conference program includes full-day short courses which will be conducted by leading experts in the field. Details will be available at a later date.

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference.

Visit www.eptc-ieee.net

IEEE Components, Packaging and Manufacturing Technology Society
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