Components, Packaging, and Manufacturing Technology Society

Newsletter

The Global Society for Microelectronics Systems Packaging

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www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

President's Column…..

Dr. William T. Chen
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President, IEEE CPMT Society
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Greetings!!!

Thoughts at the Sixtieth Anniversary

The year 2007 marks the 60th year anniversary of the singular invention that ushered in the electronics age. On December 23rd 1947, Walter Brattain and John Bardeen, two scientists in Bell Telephone Laboratory in New Jersey, demonstrated point-contact germanium transistor operated as a speech amplifier with a power gain of 18. In January 1948, William Shockley, another Bell Lab scientist leading the semiconductor research group, documented his invention for the Junction Transistor. The 1956 Nobel Prize for Physics was awarded to William Shockley, John Bardeen and Walter Brattain for their discovery of the transistor effect. Over ten years later, Texas Instrument engineer Jack Kilby successfully demonstrated a speech amplifier with his integrated circuit invention in 1959. Robert Noyce at Intel, independently invented the integrated circuit around the same time. In the short history of our industry these scientists and engineers and their inventions laid the foundations for the electronic age.

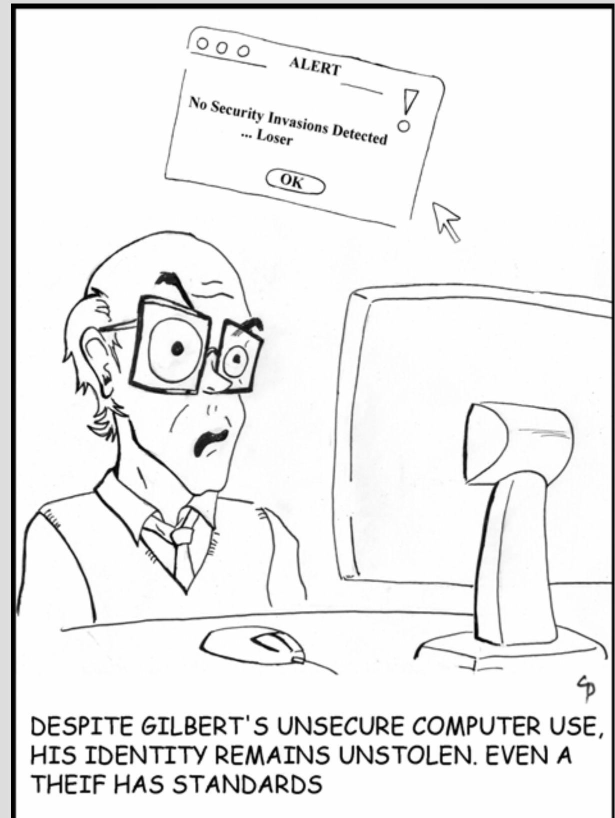
At the 60th year anniversary of the discovery of transistor, I would like to offer some thoughts on the technology, the market, the profession and us.

Technology

It was Gordon Moore, in his 1965 article in Electronics Magazine, April 19, 1965 "Cramming more components onto Integrated Circuits", who set the stage and ground rule for periodic invention and innovation for our industry with the prescient prediction of doubling the amount of transistors on an integrated circuit device every 12 months. Moore later modified the doubling period to 18 months. The 40-year track record following "Moore's Law" to the 65 nm node today testifies to the numerous inventions and innovations in many branchs of science and technology that made up our industry, as well as to the achievements of the men and women behind these inventions and innovations.

(Continued on Page 3)

Cartoon of the Month:



… By Dave Palmer

IEEE CPMT Society Newsletter
September, 2007

Index

- CPMT Society News 3
- Fellows Nominations; Senior Member upgrades 4
- Dr. Arthur Murray (obituary) 6
- Chapter Reports 7
- Conference Reports, Workshop Reviews 8
- Future Conferences and Workshops 11-23

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Refer to **www.cpmt.org** for CPMT Society Chapters and Student Branches list

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2007 Deadlines for Submitting Articles:
November 25th, 2007
Only Articles Sent to nsltr-input@cpmt.org will be included in the newsletter
Members-only Web (www.cpmt.org/mem/)
UserName: [available to Members --
Password: join CPMT!]

President's Column (Continued from Page 1)

There is belief that the traditional Moore's Law Scaling will become more difficult in the outer technology nodes, and Packaging Technologies will play a strong role to take up the slack. The ITRS More than Moore initiative shows the importance of broadening innovations and inventions in Packaging and other Technologies to keep the industry moving ahead in the long run.

Market

Sixty years ago the standard electronic component was the vacuum tube. In application it was bulky, expensive, power hungry, very hot and had limited wear-out life. The market challenge that the Bell Lab research team set out to solve was for the growing interstate long distance telephone communication market requiring reliable solid state components for telephone switch systems. We have come a long way in product applications, markets and technology. Consumer applications dominate the market. From telephone communication alone, over a billion cell phones were sold in 2006. And those cell phones have many more functions than the landline phone of 60 years ago. At a tap of the key, we play music, shoot video and connect to the internet.

Profession

In my last message I mentioned that the traditional roles for an electronic packaging engineer have been: signal integrity, power delivery, heat removal and mechanical reliability. Today our profession is broadening beyond the traditional roles. We are covering all those roles and much more. From technological perspective, the traditional Moore's Law Scaling is becoming more difficult, and packaging professionals are stepping up to take up the slack. The consumer market imperatives - cost, time to market, function, weight, size and look - add new dimensions to the electronic packaging profession. The packaging community is experiencing a rich outpouring of "out of box thinking " from industry, academia, and research institutes. At conferences, trade shows, and other industry gatherings in US, Europe and Asia, new ideas and fresh concepts – coined in phrases such as System in Package (SiP), Wafer Level Packaging, and 3D Packaging – are being hotly debated and tested.

The ways that engineering is being done - from research, development, quality, manufacturing, marketing and sales - are very much collaborative in a competitive environment. Internet enables working across geographical lines. Business models require collaborative engineering across traditional business boundaries.

A Global Community

In the early 1950's Western Electric (the manufacturing arm of AT&T) set up the first factory to build transistors in Allentown, Pennsylvania. Fifty plus years later the semiconductor and electronic industries are spread worldwide.

With the global industry, IEEE CPMT professionals are everywhere around the globe: some are IEEE CPMT members, some are IEEE members, some belong to other professional societies or belong to none at all. Recently I was greatly encouraged to learn of the formation of the CPMT Chapter in Poland, and of the initiative to form a chapter in Austin, Texas. I attended the ICEPT conference in Shanghai last month meeting many fellow electronic packaging professionals from industry, academia, and research institutes.

We are a truly global community.

A Vital and Dynamic Global Professional Society

At the 60th anniversary of the discovery of the transistor, it is time to reflect on the science and technology created from this remarkable discovery; the globally based profession that has risen from it. Today we stand st the cusp of more changes in technology, market and the profession itself. How do we shape and grow the IEEE CPMT Society and the value propositions to be a vital and dynamic force for our membership and for our professionals at this time of change?

We are scheduling some workshops prior to the November CPMT Board of Governor's meeting to examine, debate and address some of these questions. We are at the planning stage. Your input will be welcome.

CPMT Society News:

IEEE-CPMT Society Awards for Year 2008

(Nomination Due Date: January 31, 2008)

Submitted by Dr. Kitty Pearsall, Strategic Director,
IEEE CPMT Society

The CPMT Strategic Awards Director announces the call for nominations for their five, 2008 Society awards. The CPMT Society offers these awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society. While a nominee may have a specific award in mind when applying, the Awards Recognition Committee reserves the right to consider any nomination for awards other than the award suggested when, in its opinion, the support and justification may more appropriately apply to a different CPMT Society award. Winners will be notified by 28 February 2008 and the awards will be presented at the 58th Electronic Components and Technology Conference, May 27- My 30th, 2008, in Lake Buena Vista, Florida, USA.

After reviewing the high level summaries presented below, you will find a list of nomination submission requirements. The awards nomination form can be found on the CPMT Society Home page (**www.cpmt.org/awards**).

- **David Feldman Outstanding Contribution Award:** This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
  Prize: $2,500 and Certificate
  Basis for Judging: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.
  Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2007.
- **Outstanding Sustained Technical Contributions Award:** This award recognizes outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.
  Prize: $2,500 and Certificate
  Basis for Judging: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably

ten (10) years. One major contribution ***will not*** qualify. Contributions must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2007.

- **Electronics Manufacturing Technology Award:** This award recognizes major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
  Prize: $2,500 and Certificate
  Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.
  Eligibility: No need to be a member of IEEE and CPMT Society.

- **Exceptional Technical Achievement Award:** This award recognizes an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
  Prize: $2,500 and a Certificate.
  Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution ***will*** qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.
  Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2007. There are no requirements for service to the IEEE or CPMT Society.

- **Outstanding Young Engineer Award:** This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.
  Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.
  Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.
  Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2007, and must be 35 years of age, or younger, on December 31st, 2007. Please provide Date of Birth (Month/Year) to ensure eligibility.

Guidelines for Nominators:

- Minimum three (**3**) reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.
- Past recipients of an award are not eligible to receive that same award a second time. For a list of past awardees, see the CPMT Society Home page (**www.cpmt.org/awards**).
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
- Please send nominations to CPMT Awards Committee Chair by e-mail, fax or mail. If you fax a nomination, please follow-up with an email.

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IEEE Fellow Nomination Process

Dr. David Palmer
IEEE CPMT Fellow Search Committee

March 1st was the deadline for submitting nominations for the next group of IEEE Fellows of the Institute which will be announce at the end of 2007. Thus, it is a good time to remember what the quest for Fellow is about and to get ready to start the process for the next year. To quote from the IEEE web site:

"The grade of Fellow recognizes unusual distinction in the profession and shall be conferred only by invitation of the Board of Directors upon a person of outstanding and extraordinary qualifications and experience in IEEE-designated fields, and who has made important individual contributions to one or more of these fields."

The total number selected in any one year does not exceed one-tenth percent of the total voting Institute membership. For the last few years about 250 new Fellows have been appointed out of about 600 nominations. CPMT averages about 5 new Fellows a year. We have more than 100 Fellows in our current Society membership of 3000.

In addition to professional distinction, the qualifications an IEEE member needs before being nominated are:

- Must be a senior member at time of nomination

- Must be current in dues (yes, even distinguished engineers forget to renew)
- Must be a member for 5 years (Affiliate member does not count)
- Nominator must get all forms to IEEE web site by March 1st

Through this year one could download the forms, fill them out, and mail them to IEEE headquarters. For the coming year the system will be completely electronic, working from the IEEE web site. The new web site is not yet activated for new nominations but in a few months perform a search on "Fellow nomination" from the new www.ieee.org page and you will get the complete process instructions.

If you know someone who qualifies for the Fellow level you can be a nominator. You do not need anyone's permission. If you need more guidance than is on the IEEE web site you can contact anyone on the CPMT board of Governors or talk to Rao Tummala or Dave Palmer on the Fellow Search committee (see contact information on page 2).

The best steps to success are:

1. Have the Fellow candidate write an extensive resume and list all publications and presentations they have made. With this information you complete the IEEE Fellow nomination form on the web (but make a copy that you can send to potential references). It is usually important to focus on the several technical and organizational contributions that distinguish the candidate in their field. This is typically better than to list only a thousand small contributions that total a lot but did not make an obvious big difference in any technology or organization.
2. Line up between 5 and 8 Fellows in related fields that know of the candidates work or can quickly appreciate it. For example, if the candidate contributed in thermal management, there are a number of Fellows in CPMT that would be ideal for reviewing the nomination.
3. Push everyone to submit everything in February at the latest. About half the nominations miss the deadline and must wait for the next cycle. As the nominator you will have access to the IEEE Fellows Application database and be able to see which references have yet to be submitted.
4. Let C. P. Wong on the CPMT Fellows Review Committee know that you are working on a nomination so he lines up enough society reviewers.

Once a nominator has done their job the work load passes on to C. P. Wong's committee. They review all the nominations submitted in the name of the CPMT Society. All nominations must go through a Society or Council. At this point it is important to have a nomination form that clearly states the candidate's service to IEEE, the Society, and the profession. A member that has spent many years organizing CPMT conferences or producing our publications has a natural advantage in the process of winning a professional award compared to an equal technical contributor but a non-participating member.

In a typical year the Fellow review committee will score and rank about 10 nomination packages and forward them to the IEEE Fellow committee. Historically our submitted nominees have about a 50% success rate. Submitting someone for a series of years is common and should not be considered bad luck by either the nominator or the candidate.

The process takes typically about 20 hours by the candidate, 30 hours by the nominator, and 5 hours by each Fellow reference. CP's team spends many days in the process trying to strengthen every package and to get the right feedback to the nomination.

The Fellow Level recognition is among the highest in our engineering profession. Universities and Companies proudly state the number of Fellows in their staff. As CPMT Society members read the list of Fellows they nod knowingly as they see name after name of admired peers. If your time has come, start the nomination process.

CPMT Fellows

Current in Dues as of September, 2006

Submitted by Marsha S. Tickman, Executive Director

Cristina Amon	Yasuhiro Ando	Tawfik Rahal-Arabi
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Ingo Wolff	C. P. Wong	Ralph Wyndrum
Hiroshi Yamada	Naoaki Yamanaka	Qi-Jun Zhang

IEEE Senior Membership

Dr. Vasudeva P. Atluri, Editor-in-Chief, IEEE CPMT Society Newsletter

Grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. Candidate should be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields. Candidate shall have shown significant practice for at least ten years and shall have shown significant performance over a period of at least five of those years.

Benefits of IEEE Senior Membership Include:

- The professional recognition of your peers for technical and professional excellence.
- An attractive fine wood and bronze engraved Senior Member plaque to proudly display.
- Up to $25.00 gift certificate toward one new Society membership.
- A letter of commendation to your employer on the achievement of Senior member grade (upon the request of the newly elected Senior Member.)
- Announcement of elevation in Section/Society and/or local newsletters, newspapers and notices.
- Eligibility to hold executive IEEE volunteer positions.
- Can serve as Reference for Senior Member applicants.
- Invited to be on the panel to review Senior Member applications.

For additional information including requirements and application process refer to IEEE Senior Member Program website located at

www.ieee.org/organizations/rab/md/smprogram.html.

Contact representatives of the section or society you belong to for any further assistance and suggestions.

CPMT Senior Members

Submitted by Ms. MarshaTickman, Executive Director, IEEE CPMT Society

Congratulations to the following CPMT Society members for achieving Senior Member status after December, 2006:

Atlanta Section :	Jianmin Qu
Buenaventura Section:	Roberto Coccioli
	Francis Donohoe
Central Coast Section:	Jianbiao Pan
Central Texas Section:	Paul Harvey
Eastern North Carolina Section:	Christopher Bower
	Jonathan Hinkle
Italy Section:	Silvia Pietralunga
Mid-Hudson Section:	Oliver Patterson
Northwestern Subsection:	Anthony Close
Orange County Section:	Volkan Ozguz
Oregon Section:	Farhad Akhavan
	Paul Crump
Phoenix Section:	Sandeep Tonapi
San Diego Section:	Mikaya Lumori
Tainan Section:	Yi-Shao Lai

IEEE CPMT Society Newsletter

Send inputs, suggestions, and articles by email to nsltr-input@cpmt.org

….. Editor

Obituary:

Dr. Arthur T. Murphy – IEEE Fellow

Submitted by Daniel I. Amey, DuPont Corporation Daniel.I.Amey@usa.dupont.com

Dr. Arthur T. "Murph" Murphy, Jr. passed away peacefully on July 2nd, 2007 after a short illness; he was 78. Born in Hartford, CT he was an only son to Marye (Beakey) and Arthur Thomas Murphy, Sr.

Art worked for E.I. DuPont de Nemours and Co. Inc., and was a DuPont Fellow "Emeritus" the highest technical position in the corporation. Art joined DuPont in 1979 following a distinguished 25-year career in academia. He was Brown Professor and Head of Mechanical Engineering at Carnegie-Mellon University, Vice-president and Dean of Engineering at Widener University, Head of Electrical Engineering at Wichita State University, and Visiting Professor at MIT and University of Manchester (England) and Adjunct lecturer at Penn State University.

Art began his DuPont career working in the Electronics Connector Division where he developed electronic connectors and components and introduced the first 3-D computer aided design system that DuPont had for mechanical design. He developed a unique filter component for control of electromagnetic interference (EMI) and was awarded patents and marketing excellence awards for this work.

In 1986 he moved to the DuPont experimental station in Wilmington in Departmental Research and Development where he established an Electronic Systems Research group with emphasis on Computer Aided Design of interconnections and high frequency applications. He developed a computer software system for the analysis and simulation of electronic packaging and interconnection systems, which was applied to DuPont materials and customer product development. He then accepted an assignment to work for three years in Japan, working for two years at the Sony Research Center in Yokohama, Japan as a Visiting Research Fellow where he developed semiconductor packaging for high speed integrated circuits. This was followed by a one-year position as DuPont's representative to the International Superconductivity Technology Center in Tokyo, Japan where he developed an active superconducting mixer antenna array. Art returned to the US in DuPont Central Research and Development working on business growth initiatives, university liaison and also serving as an internal consultant with various Dupont businesses. He ended his DuPont career in the DuPont Engineering organization.

Art published numerous technical papers on electronic modeling and simulation and component design, was awarded a number of patents and was co-author of a book, *Introduction to System Dynamics*.

He was very active in industry professional organizations, particularly in the areas of professional development and educational activities. He was a member of the American Society of Mechanical Engineers, a Fellow of the Institute of Electrical and Electronics Engineers (IEEE) and a Fellow of the American Association for the Advancement of Science (AAAS). He was life member and Fellow of the American Society of Engineering Education (ASEE) and DuPont's representative to the ASEE. After his re-

tirement he continued to represent DuPont and served for four years as the society's Vice President of Finance. Working with the National Academy of Engineering, he was involved in projects of national scope dealing with the reform of engineering education. In 1998 Art served as acting President of the Pennsylvania Institute of Technology. He was an evaluator for the Accreditation Board for Engineering and Technology
(ABET) evaluating engineering programs at numerous schools of engineering, most recently this past spring at Columbia University. Art received the B.E.E. from Syracuse University and the Ph.D. and M.S. degrees in electrical engineering from Carnegie-Mellon University and was a registered professional engineer. He was a member of seven honor societies; Eta Kappa Nu, Tau Beta Pi, Phi Theta Kappa to name just a few.

Art was a loving husband, father, and grandfather, caring friend, mentor, and inspiration to all who came in contact with him. Art passed away peacefully with his family at his side. He is survived by his loving wife of 54 years, Jane, and seven children: son Thomas (wife Karen and son Patrick), Chattanooga, TN; daughter Patricia (partner Kendra), Stockton, NJ; daughter Mary (husband Karl and son Brendan), Albany, NY; son Jack (wife Trina, and sons Connor, Devon, and Mason), Radford, VA; daughter Sheila, Lahaina, HI; daughter Jane Ann, Drexel Hill, PA; and son Joseph (wife Chanda), Memphis, TN and a multitude of friends around the world. Art spent years researching family geneology; however, his greatest pleasure was time spent with his family as they traveled the world creating lasting memories and lifelong friendships.

Art and Jane would have celebrated their 55th anniversary on August 16th, 2007. They recently established a dual endowment Scholarship for Study abroad in Engineering and Music at Syracuse University, where they met. In lieu of flowers, contributions can be made to this fund:

The Arthur T. and Jane M. Murphy Endowed Scholarship at Syracuse University for Study Abroad

c/o Mr. Steve Savage
Senior Director of Development
Syracuse University
LC Smith College of Engineering & Computer Science
223 Link Hall
Syracuse, NY 13244

Chapter Reports:

Contribution to IEEE CPMT Newsletter by Singapore REL/CPMT/ED Chapter August 2007

Submitted by Alastair Trigg, Chair - IEEE Singapore Rel/CPMT/ED Chapter

In June, Chapter organized three technical talks. On 22th June, Drs Chih-Hsun Chu and Yong-Fen Hsieh a husband and wife team from Taiwan who started, and now run, the company Materials Analysis Technology which specializes in providing failure analysis service to the semiconductor industry gave two talks. In his talk on "Non-Planar Oxidation of Silicon" Dr Chu discussed different scenarios and gave many examples that he has seen over the course of his career. Dr Hsieh spoke on "Ion Implantation and Related Defect Formation by Latent Stress".

On 25th June, an EDS Distinguished lecturer, Prof. Vijay K. Arora of Wilkes University USA, gave a talk entitled "Performance Evaluation of Nano Circuits and Systems with Ballistic Carriers.

In July the Rel/CPMP/ED Singapore Chapter and ED/SSC Hong Kong Chapter jointly organized the 13th Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology (WIMNACT) which was held in Hong Kong on 23rd July and Singapore on 25th. The workshops were co-sponsored by the EDS Distinguished Lecturer (DL) Program.

The Singapore workshop, attracted about 70 people and was opened with a welcome address by the Chapter Chair, Dr. Alastair Trigg, followed by an Introduction to EEE Microelectronics Center, co-organizer of the workshop, by the Director, Prof. Kin-Leong Pey. DLs from Singapore, Hong Kong, Malaysia, USA and India presented talks at the Singapore workshop.

- Prof. Juin Liou from Univ. of Central Florida: "*On-Chip Spiral Inductors in CMOS Technology for RF Applications*"
- Prof. Ramgopal Rao from IIT-Bombay: "*Device Design and Optimization Challenges for Nano-scale Multi-gate MOSFETs*",
- Prof. Kin-Leong Pey: "*Silicided Hyper-shallow p+/n- Junctions Formed by Pulsed Laser Annealing for Nanoelectronic Devices*"
- Prof. Mansun Chan of HKUST: "*Application of Integrated Circuit Technology for Biological Material Analysis*"
- Prof. Xing Zhou from Nanyang Technological Univ.: "*Unified Compact Modeling of Emerging Multiple-Gate MOSFETs*",
- Mr. Chih-Hang Tung from Institute of Microelectronics: "*Advanced Transmission Electron Microscopy for Nano-electronics Device and Process Analysis*".
- Prof. Vijay Arora of Wilkes University and is visiting professor at Universiti Teknologi Malaysia: "*Physics-Based Models for Performance Evaluation of a Nanoscale MOSFET*".

This first attempt at a joint mini-colloquia, proved very successful as well as economical due to shared travel funds.

DL speakers at WIMNACT-Singapore.: *From left to right*: Xing Zhou, Kin-Leong Pey, Vijay Arora, Juin Liou, Mansun Chan, Ramgopal Rao, Chih-Hang Tung.

Further information on the 13th WIMNACT, including past history of WIMNACTs, can be found at the website:
www.ntu.edu.sg/eee/eee6/conf/WIMNACT07.htm

Two of the DLs extended their stay in Singapore. Prof Juin J. Liou gave a one-day short course on "Electrostatic Discharge (ESD) Protection in BiCMOS/CMOS Technology on 26th July and a day later on 27th July, Prof. Mansun Chan gave a talk on "IC Industry in China: Challenges and Opportunities".

This year, the Chapter's flagship conference on failure analysis, the International Symposium on the Physical and Failure Analysis of Integrated Circuits 2007, was held from 11-13 July in Bangalore, India. It was organized by IEEE ED/SSC Bangalore Chapter and co-sponsored by IEEE Rel/CPMT/ED Singapore Chapter. It comprised one day of tutorials and two days of Symposium and equipment exhibition. Full details can be found at:

ewh.ieee.org/reg/10/ipfa/html/2007/index.htm

Planning is now underway for IPFA 2008 which will be held in Singapore from 7th to 11th July 2008. The first call for papers has been issued and will be available on the Chapter website at **www.ewh.ieee.org/soc/cpmt/singapore/**

Chapter's packaging conference, the 9th Electronics Packaging Technology Conference (EPTC 2007) will be held at Grand Copthorne Waterfront Hotel Singapore in Singapore from 10th to 12th December. Full details of EPTC can be found at the website: **eptc2007.confs.org/**.

Newly Approved CPMT-Chapter in Austin

Submitted by Dr. Om P. Mandhana, Netwoking and Computing Systems Group, Freescale Semiconductor, Inc., Austin, Texas

A new CPMT Chapter in Austin, Texas is approved this year by the IEEE.

The first meeting of this Chapter was held on August 9, 2007 at Freescale Semiconductor, Austin, Texas.

The meeting was attended by many CPMT members from various industries in Austin, Texas area. Following office bearers for the CPMT-Austin Chapter were elected:

Chair: Om P. Mandhana, Freescale Semiconductor
Treasurer: Jonathan Burnett, Freescale Semiconductor
Technical Program Chair: Moises Cases, IBM
Technical Program Co-Chair: Paul M. Harvey, IBM

Future monthly meetings of this Chapter will be held on Thursday of the first week.

Conference Reviews:

Conference report from HDP´07

Submitted by Dr. Johan Liu
SMIT Center, Chalmers University of Technology, Sweden, and Shanghai University & SHU-Intel Joint Lab, Shanghai University, China
Email:jliu@chalmers.se

The 2007 International Symposium on High Density Packaging and Microsystem Integration (HDP'07) was successfully held from between 26 and June 28, 2007 in Shanghai, China. This year, the conference was co-located with the EU-China Green Electronics Workshop, an event that was sponsored by then European Commission and the Ministry of Science and Technology (MOST), China through the official 2007 Sino-EU Science Year Program.

The HDP'07 conference was sponsored by The Institute of Electrical and Electronics Engineers and Component, Packaging and Manufacture Technology Society and supported by The Ministry of Science and Technology and Shanghai Science and Technology Commission, Shanghai Municipal Government, China. We are very honored to have the welcome speeches by Mr. Jianfeng Lu, Principal Program Officer of Department of international collaboration, Shanghai Science and Technology Commission, Shanghai Government, Prof. Min Wang, Vice President of Shanghai University, Mr. Stefan Bengtsson, Vice President of Chalmers University of Technology, Sweden, and Mr. Lars Andreasson, General Consul of the Consulate of Sweden in Shanghai. This conference was also supported by several media including China integrated circuit magazine, semiconductor technology magazine, semiconductor industry magazine and electronic assembly magazine.

More than 300 experts and researchers participated in the HDP'07 conference from countries and regions such as U.S.A., U.K., France, Sweden, Japan, India, Germany, Finland, Poland, Norway, Belgium, Korea, Hong Kong and Taiwan. More than 110 papers were presented in terms of oral and poster presentations. Moreover, we are honored to have outstanding keynote and invited speakers such as Prof. C.P. Wong, Member of Academy of engineers, USA, Fellow of IEEE, Prof. Georgia Tech, USA; Prof. James E. Morris, IEEE Fellow, Maseeh College of Engineering and Computer Science, Portland State University, USA; Prof K. Suganuma, Osaka University, Japan; Mr Matsuda, Hitachi Chemicals, Japan, Thomas Oppert, Pac-Tech, Germany; Dr. Tim Chen, General Manager of Henkel Electronics China Ltd; Dr. Dongkai Shangguan, Vice president, Flextronics U.S.A.; Michael, Todd, Technical Director, Henkel Electronics, USA; Dr. Fay Hua, Principal Engineer, Intel, USA; Dr. Daniel Lu, Staff Engineer, Intel Co., USA; Dr Guilian Gao, Tessera, USA; Dr. Ricky Lee, ASME Fellow, Hong Kong University of Science and Technology; Prof Michael Pecht, IEEE Fellow and Director of CALCE, University of Maryland, USA; Chris Bailey, Greenwich University, UK and Philip Pieters, IMEC, Belgium as well as well-known industries like Intel, Henkel, Huawei, Du Pont, Pac-Tech, Hirox, STS, Panasonic, Hitachi Chemical, Asymtek, Sang Yue, and universities such as Shanghai University, Tsing Hua University, Fudan University, Shanghai Jiaotong University, Huazhong University of Science and Technology, Central South University, Dalian University of Technology, Harbin Institute of Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy Science, Hong Kong University of Science and Technology participating in the conference.

Photos from HDP'07

International Symposium on High Density Packaging and Microsystem Integration (HDP'07)
The IEEE Components, Packaging, and Manufacturing Technology Society
Shanghai University
Organized by:

Sponsored by:
Shanghai University
Organized by:
Shanghai Microao Inc.
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2007 International Symposium on High Density Packaging and Microsystem Integration (HDP'07)
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For first time, there was an exhibition taken place during the conference. The following companies participated in the conference exhibition: Hitachi Chemicals, Panasonic, Henkel, STS, Hirox, Pac-Tech and Sang Yuen. Three best Intel student awards were to given to the students from Dalian University of Science and Technology, University of Science and Technology, Beijing and Hua Zhong University of Science and Technology, China. The HDP'07 conference provided an excellent opportunity for the microelectronics and microsystem industries to exchange the latest development in this fascinating field, especially with regard to the rapid growth of electronics industry in China.

In addition to this, three short courses were given by Prof. C.P. Wong, Prof. James Morris, Dr. Shangguan Dongkai, Dr. Fay Hua and Dr. Daniel Lu on nanotechnology as well as on lead free technology including solders and conductive adhesives.

Workshop Reviews:

Call for Participation in the
2007 IEEE/CPMT Workshop on Accelerated Stress Test and Reliability

Greenbelt Marriot in Greenbelt, Maryland
October 31st through November 2nd, 2007
Submitted by Kirk Gray, Dell Reliability Validation Engineer, Tel: 512-723-1374

This year's IEEE/CPMT Workshop on Accelerated Stress Test and Reliability Theme is: "Accelerated Life Testing, it's Role, Challenges, Attributes, and Interaction with Qualification Testing". Over the last few decades, Accelerated Stress Testing (AST) has been embraced by an ever widening array of worldwide companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market. The purpose of the AST Workshop is to share ideas on better ways of accelerated testing, stress margin limit testing and analysis, and detecting hidden defects and weaknesses in electronic and electro-mechanical hardware that would result in failures. The goal of AST is to cost effectively develop mature robust products at market introduction.

You can access all the current Workshop information at our Website at **www.ewh.ieee.org/soc/cpmt/tc7/ast2007**/

Our registration page can be linked from the home page or accessed directly at URL:
icm3.ieee.org/eventmanager/onlineregistration.asp?eventcode=9L6

Just some of the Presentations that are scheduled at this year's event:

Paul Parker	Power Supply Design and Test for Reliability
Ali Shakouri	Reliability and Testing on Nanostructure
Mike Silverman	Early Reliability Testing
Gary M. Hazard	Rapid Reliability Risk Assessment for Fiber Optic Components
Don Gerstle	Power Conversion Reliability
Hong S. Liu	Comparison Testing of Shock vs. Vibration ESS system
R.Zingher et al.	Enhancing Accelerated Life tests with monitoring and prognostication
Gustavo Plaza et al.	Study of Vibration Monitoring and Failure Criteria Definition for Solder Interconnet
Mike Silverman Hass	Profile Fine Tuning Using Field Data
David Francis	Case Study at CNH Case New Holland - HALT of Alternators
Koustav Sinha et al.	Mechanical strength of copper-silicon interface of planar metallization power modules
Gayatri Cuddalorepatta et al.	Durability Assessment of an Advanced Power Electronics Thermal Cooler
Jinsong Xie	A Case Study of Field Life Prediction and Reliability Assessment of Electronics Assemblies
Joey Bernstein et al.	Physics of Failure and Reliability Modeling of Electronic Packages

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2008 IEEE Systems Packaging Japan Workshop

Hotel de YAMA, Hakone, Japan
January 28 - 30, 2008
www.ewh.ieee.org/soc/cpmt/tc14/
Submitted by Evan Davidson, Japanese Liaison for TCSP

Call for Papers and Invitation

The Systems Packaging Japan Committee cordially invites you to participate in the 2008 IEEE Systems Packaging Japan Workshop (2008 SPJW), which will be held during January 28-30, 2008 at the Hotel de YAMA, Hakone, Japan. This workshop is held every other year in Japan and 2008 SPJW will be the twelfth one since the first workshop in 1986. State-of-the-art technologies in all areas of systems packaging from personal systems to high performance systems will be covered. Attendees are expected to be specialists in the field and to actively participate in all discussions. We look forward to meeting many of you at Hakone.

Topics:

- IT Network Systems
- Digital Consumer Products & Mobile Information Systems
- High Performance Servers
- Advanced Packaging & Components
- Bio/Nano Technologies
- Environmental Aspects

For more information about the workshop, please feel free to contact Mr. Kishio Yokouchi, the Program Chair at:

Research & Development Group
Fujitsu Interconnect Technologies Ltd.,
Phone: 26-263-2711
Facsimile: 26-256-3823
E-mail: **yokouchi.kishio@fict.fujitsu.com**

CONFERENCES OF THE CPMT SOCIETY

Calendar

For quick-links, go to our Society Conferences Page:

www.cpmt.org/conf

53rd IEEE Holm Conference on Electrical Contacts, and Intensive Course

September 16-19, 2007; Sheraton Station Square Hotel, Pittsburgh, PA USA
Contact: Elsie Cabrera, IEEE, e.cabrera@ieee.org
www.ewh.ieee.org/soc/cpmt/tc1/h2007/h2007top.html

3D System Integration Workshop – The Future Technology!

October 1-2, 2007; Fraunhofer Gesellschaft, München Germany
Contact: Simone Brand, Fraunhofer IZM, simone.brand@izm-m.fraunhofer.de
www.pb.izm.fhg.de/izm/050_Events/90_single/81_3d.html

Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT) Conference

October 1-3, 2007; Taipei International Convention Center, Taiwan
20% discount through August 31st
Contact: Wendy Huang, Conference Secretariat, impact@itri.org.tw
impact.itri.org.tw

34th Int'l Electronics Manufacturing Technology Symposium (IEMT 2007)

October 3-5, 2007
Holiday Inn, San Jose (Silicon Valley), CA USA
Discount through Sept. 17th
Contact: Paul Wesling, p.wesling@ieee.org
www.cpmt.org/iemt/

Advanced Packaging Materials Symposium (APM 2007)

October 3-5, 2007
Holiday Inn, San Jose (Silicon Valley), CA USA
Discount through Sept. 17th
Contact: Paul Wesling, p.wesling@ieee.org
www.cpmt.org/apm/

16th Annual International Symposium on Semiconductor Manufacturing (ISSM'07)

October 15-17, 2007, Marriott Hotel, Santa Clara, CA USA
Contact: Maria Hess, AMD, maria.hess@amd.com
www.issm.com

2007 IEEE Electrical Performance of Electronic Packaging (EPEP)

October 29-31, 2007
Renaissance Atlanta Hotel Downtown, Atlanta, GA USA
Contact: Kelly Sutton, University of Arizona, epd@engr.arizona.edu
www.epep.org

2007 IEEE/CPMT Workshop on Accelerated Stress Test and Reliability (AST)

October 31 - November 2, 2007; Greenbelt Marriot in Greenbelt, Maryland USA
Contact: Kirk Gray, Dell Computer, Kirk_Gray@Dell.com
www.ewh.ieee.org/soc/cpmt/tc7/ast2007

2007 International Symposium on Electronic Materials and Packaging (EMAP2007)

November 19-22, 2007; KAIST (Korea Advanced Institute of Science & Technology), Daejon, Korea
Abstracts Due July 31, 2007
Contact: For more information, email emap@kaist.ac.kr
emap.kaist.ac.kr

9th Electronics Packaging Technology Conference (EPTC 2007)

December 10-12, 2007; Singapore
Early registration discount thru October 22nd
Contact: Joseph LIM, eptc2007@elite.sg
www.eptc-ieee.net

2007 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)

December 15-17, 2007; Taipei, Taiwan
Contact: Hui-Yun Hu, EDAPS Secretariat, edaps2007@tl.ntu.edu.tw
edaps2007.ntu.edu.tw

2008 Systems Packaging Japan Worshop (SPJW)

January 28-30, 2008 Hotel de Yama, Hakone, Japan
Abstracts Due Nov 20, 2007
Contact: Kishio Yokouchi, Fujitsu Interconnect Technologies Ltd., yokouchi.kishio@fict.fujitsu.com
www.ewh.ieee.org/soc/cpmt/tc14/Japan08/SWJ08call.html

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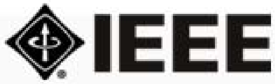
Please cast your vote by mail by signing the ballot sent by IEEE or accessing ballot electronically at www.directvote.net/ieee/
Deadline for casting your vote is 12:00 Noon Central Time in the United States, 17:00 Greenwich Mean Time on 1st November 2007



32nd International
Electronics Manufacturing Technology Symposium

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Advanced Packaging Materials Symposium

October 3-5, 2007 San Jose/Silicon Valley, CA USA

Co-located for the first time!
One registration admits you to all sessions and events.

Summary of the IEMT/APM Symposium (details on website)

SESSIONS

Thursday, October 4
- Stacked Die and Die-Attach Film
- Manufacturing Technology
- Materials for Electronics Packaging
- Imaging, Medical, Embedded Technology
- Materials in Packaging Applications
- Posters Session
- Exhibits, Reception, Evening LEOS Meeting

Friday, October 5
- Materials for Interconnects
- Lead-free Soldering and Bonding
- Packaging for MEMS, 3D, WLP
- Nanotechnology
- Design for Environment

PROFESSIONAL DEVELOPMENT COURSES

Wednesday, October 3

Four Morning PDCs:
- **Nanotechnology Applications in Packaging,** Florin Ciontu, NanoSPRINT
- **Implementing Flip Chip and WLP Technology,** Peter Elenius, E&G Technology Partners
- **Advanced Packaging Technology Solutions for Today's Leading Edge Microelectronics**, Charles B. Woychik, GE Global Research
- **Achieving High Reliability for Lead-Free Solder Joints - Materials Considerations,** Dr. Ning-Cheng Lee, Indium Corporation of America

Three Afternoon PDCs:
- **Polymers & nano-Composites for Electronic and Photonic Packaging: Recent Advances in Materials and Processes,** Prof. C.P. Wong, Georgia Institute of Technology
- **3-Dimensional Semiconductor Packaging & Integration,** Charles E. Bauer, Ph.D., and Herbert J. Neuhaus, Ph.D., TechLead Corporation
- **Failure Modes & Analysis of Flip Chip Assemblies**, Prof. Daniel Baldwin, Georgia Institute of Technology

GALA RECEPTION

Thursday, October 4 Western-themed BBQ and Reception, featuring the Silicon Cowboys rock group (songs from the '60's, '70's and '80's), featuring Tom Tarter, 2005 IEMT General Chair

EXHIBITS

Thursday, October 4 11 AM – 6 PM
and Friday, October 5 10 AM – 3 PM

Register On-line: www.cpmt.org/iemt or /apm Discount through Sept. 17, 2007

2007 combined IEEE Symposium on

Advanced Packaging Materials and Int'l Electronics Manufacturing Technology

October 3-5, 2007
San Jose Holiday Inn
Silicon Valley

Mail/Fax to: **IEMT/APM Symposium.** PO. Box 2110, Cupertino, CA 95015 USA • Phone +1-408-331-0114 • **Fax +1-408-904-6997** • email iemt07@cpmt.org

(*circle*) Dr. Mr. Mrs. Ms. ______________________________

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E-mail ______________________________

(print clearly)

Registration Includes: 2 lunches, Exhibitor Reception/entertainment on Thursday evening, admission to technical sessions, poster session, exhibits, one copy of the printed Proceedings, and a post-conference CD-ROM with final papers, mailed in January.
Paying at the door: Cash, check or credit card.
Cancellation fee: Cancellations are required prior to September 21 for refund (less $75 processing fee). All requests must be in writing (email, FAX). Substitutions accepted at any time.
Persons with a disability: Requests for accommodations for persons with disabilities are due to Paul Wesling, conference administrator, by 24 September. My special needs/requirements include

____

To **exhibit** at APM/IEMT, please see the **EXHIBITORS PAGE** on our website: www.cpmt.org/iemt/ or contact Annette Teng, annetteteng@yahoo.com.

Detach this page, fill in the Registration Form, and FAX it to **+1-408-904-6997**

with credit-card information

Duplicate this Registration Page if extra copies are needed for co-workers.

Register on line:

www.cpmt.org/iemt

This year's Advanced Packaging Materials Symposium (APM) and Int'l Electronics Manufacturing Technology Symposium (IEMT) are completely co-located. One registration entitles the attendee to attend sessions and activities across both events.

Primary Technical Interest: (choose one)

- ☐ **Advanced Packaging Materials**
- ☐ **Electronics Manufacturing Technology**

Circle the appropriate rate: *(all amounts in US dollars)*

SPEAKERS, CHAIRS, COMMITTEE:

Please check: ☐ Speaker ☐ Session Chair ☐ Committee

IEMT/APM Speaker, Chair, Committee **$300**

PRIOR TO SEPTEMBER 17: (save $100)

IEEE Member #____________	Member	Non -member
Advance registration	**$400**	**$475**

AFTER SEPTEMBER 17 and at door:

	Member	Non -member
Regular registration & on-site	**$500**	**$575**

Professional Development Courses *(optional, on Wed Oct. 3)*

Please check:	Member	Non -member
☐ **One Course**	**$300**	**$350**
☐ **Two Courses**	**$450**	**$500**

Mark the Professional Development Courses you are planning to attend: (see descriptions on pages 3-6)

Morning Course (choose no more than one)

- ☐ **Nanotechnology Applications in Packaging**, Florin Ciontu
- ☐ **Implementing Flip Chip & WLP Technology,** Peter Elenius
- ☐ **Advanced Packaging Technology Solutions for Today's Leading Edge Microelectronics**, Charles Woychik, GE
- ☐ **Achieving High Reliability for Lead-Free Solder Joints - Materials Considerations**, Dr. Ning-Cheng Lee, Indium Corp

Afternoon Course (choose no more than one)

- ☐ **Polymers & Nano-Composites in Electronic, Opto-Electronic and Photonic Packaging**, Dr. CP Wong, GaTech
- ☐ **3-Dimensional Semiconductor Packaging & Integration,** Dr. Charles E. Bauer and Dr. Herbert J. Neuhaus
- ☐ **Failure Modes & Analysis of Flip Chip Assemblies**, Prof. Daniel Baldwin, GaTech

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Registrations will be confirmed by email.

IEMT/APM Symposium is sponsored by IEEE, EID #13-1656633

CALL FOR PAPERS

ECTC 2008

May 27 - May 30, 2008
Disney's Contemporary Resort
Lake Buena Vista, Florida USA

The 58th Electronic Components and Technology Conference

Introduction

On behalf of the ECTC Program Committee, it is my pleasure to invite you to submit an abstract for the 58th Electronic Components and Technology Conference (ECTC), to be held May 27 – May 30, 2008, in Lake Buena Vista, Florida. This premier international conference is sponsored jointly by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT) and the Electronic Components, Assemblies, and Materials Association (ECA), the electronic components sector of the Electronic Industries Alliance (EIA). You are not required to be a member of either organization to present a paper or attend the conference.

The ECTC comprises papers covering a wide spectrum of topics, including electronic components, materials, assembly, interconnections, packaging, system packaging, optoelectronics, reliability, and simulation. We have also included a topic on emerging technologies in the program to address exciting new developments and applications in the area of biomedical, nano-scale, organic device packaging and portable power supply. A plenary session and a panel discussion address selected topics each year, in addition to a seminar organized by the IEEE CPMT Society. Authors from companies, research institutes, and universities located around the world presented more than 300 papers and posters at the 2007 ECTC to more than 1,000 conference participants.

Professional Development Courses covering 16 different topics are offered by world-class experts in their fields. Participants can catch up with new technology developments and broaden their technical knowledge base. The technical program and professional development courses are supplemented by the technical exhibition corner. Leading companies primarily in the electronics components, materials, and packaging fields exhibit their latest technologies and products.

The ECTC Program Committee represents a wide range of disciplines and expertise from the electronics industry and is committed to put together an excellent technical program at the ECTC. Please submit an abstract on your recent, previously unpublished work to the 58th ECTC at **www.ectc.net**. In addition to abstracts for papers, I also invite you to submit proposals for Professional Development Courses. The deadline for abstract submission is October 15, 2007. I look forward to seeing you in beautiful Lake Buena Vista, Florida in May 2008.

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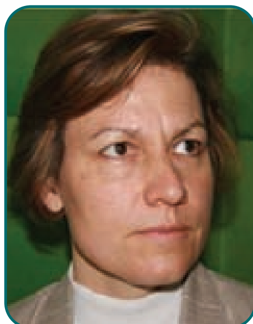
Email: jeanmh@us.ibm.com



Visit the ECTC website (www.ectc.net) for additional conference information.

Major Topics

Papers presenting new developments and knowledge in the following areas are invited. Please select two subcommittees that should consider your paper. ***The work submitted should be original, not previously published, and avoid the inclusion of commercial content.***

- ***Advanced Packaging:*** New packaging technologies, systems packaging, first level thermal solutions for high power applications, designs, materials, and configurations addressing performance, density and cooling for single chip, multichip, 3D, SIP, wafer-level, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA and SMT packages for both Pb-based and Pb-free bumps and package assembly.
- ***Electronic Components & RF:*** Discrete/integrated/embedded passives and passive networks - design, technology and characterization, embedded active components, integrated antennas, RFID/sensors, RF MEMS design & technologies, RF/microwave/millimeter wave components and modules integration in semiconductor, ceramic, organic, glass type substrates, EMI & innovative shielding and isolation techniques for passive components and mixed signal modules, new high frequency characterization methodologies.
- ***Emerging Technologies – Biomedical, Nano-Scale, Organic Device Packaging and Portable Power Supply:*** Packaging of digital health technologies, including biomedical, bioelectronics, bio-sensing devices, micro-fluidic devices, and bio-compatible materials. Nano packaging and electronics, micro-to-nano transition, nano-electro-mechanical systems (NEMS), flexible electronics, nano fluidics, organic electronic devices (active and passive), and systems. Novel emerging technologies for embedded, portable power supplies and RFID. Materials, fabrication, characterization, mechanics, optical properties, packaging, reliability, and applications.
- ***Interconnections:*** Interconnect innovation/design/process on all packaging levels including wire bonding, flip chip, 3D and through Si via connections, first-level package, printed circuit board, and connectors/sockets. Topics may range from bump and under bump metallurgy, electromigration, conductive polymers and nano material based interconnects, novel enabling techniques, electrical performance, to environmental concerns.
- ***Manufacturing Technology:*** Advanced fabrication and assembly process and equipment capability enablement for emerging technologies including: system in package, package on package, wafer thinning, bumping, stacking, low-k chip, Pb-free and MEMS packaging. Product-level integration and system-level optimization of emerging technologies focusing on manufacturability, yield improvement, quality and reliability improvement, electrical/mechanical/environmental performance, supply chain development, and new product introduction.
- ***Materials & Processing:*** Materials and processes for IC and microsystems packaging that enhance mechanical, thermal and electrical performance and cost effectiveness. This includes advances in materials and processing of adhesives, encapsulants, nano-materials, chip underfills, solders and alloys, magnetic and optical materials, thermal interface materials, polymers, ceramics, composites, flexible dielectrics and substrates, thin films, coating, bonding, plating and assembly processes.
- ***Modeling & Simulation:*** Electrical, thermal, optical, and mechanical modeling, simulation, and characterization of packaging solutions including system-level applications. Example topics include - assembly manufacture modeling, Cu low-K interconnects, drop impact models, embedded passives, equivalent circuit models, full-wave modeling, lead-free solders, macromodeling, measurements, and thermo-mechanical reliability.
- ***Optoelectronics:*** Packaging and technology for optoelectronic modules, components and devices including: amplifiers, transmitters, receivers, integrated photonics, passive components, plastics packaging, chip to chip, backplanes and storage. Special interest topics include high power devices, thermal management and reliability, micro-optic packaging & manufacturing technology, silicon photonics devices and packaging, and advanced materials for optoelectronics.
- ***Posters:*** Papers may be submitted on any of the major topics listed by the subcommittees. Presentation of papers in a poster format is highly encouraged at ECTC.
- ***Quality & Reliability:*** Reliability assessment and prediction at the system, PWB or package level; reliability testing and data analysis; failure analysis of field and test failures; reliability modeling of accelerated testing; reliability issues in emerging technologies; testing and predictive simulation; advances in reliability test methods and failure analysis.

Submit your Abstract today, at www.ectc.net

CALL FOR PAPERS

ECTC Components & RF Program Committee
CPMT RF & Wireless Technical Committee

58th ECTC May 27th – May 30th, 2008
Orlando, Florida USA

The CPMT RF & Wireless Technical Committee and the ECTC Electronic Components & RF Program Committee encourage you to submit an abstract in the area of passive components & networks, RF and Microwave components and modules and subsystems.

Discrete Passive Components: Design, materials, processes and manufacturing considerations for discrete passive components- resistors, capacitors, inductors and passive networks.
Integrated and Embedded Passive Components: Design, materials, processing, modeling, manufacturing, and characterization of integrated/embedded passives on silicon, organic, ceramic and glass type substrates for digital, mixed signal, & RF applications
Materials, Processing, Reliability, and Manufacturing of Electronic Components: Design, Materials , Processing, yield and reliability aspects of electronic components
New Technology Development for Electronic Components: Technologies for on chip integration of passive components – silicon through vias, wafer level RDL, nano materials and processes; Technologies for substrate level integration – embedded passive and active components, component integration on ultra thin substrates
RF and Microwave Components: Integrated antennas, filters, baluns, RFID/sensors, RF MEMS, tunable devices and switches, high power and high efficiency RF/Microwave power amplifiers- design, technology and high frequency characterization
RF and Microwave Modules: Module Integration technologies in semiconductor, organic and glass substrates – System in Package, System on Chip, Package on Package, 3D integration

SUBMISSIONS: Please submit abstracts using the ECTC web site: **www.ectc.net** by October 15, 2007. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the "Components & RF" focused sessions **YOU MUST SELECT**
"ElectronicComponents & RF" committee as your PRIMARY subcommittee preference when you submit your abstract.

Craig Gaw, Chair - CPMT RF & Wireless TC, Freescale Semiconductor Inc., c.a.gaw@ieee.org

Mahadevan K. Iyer, Chair - ECTC RF & Components TC, Georgia Institute of Technology, mahadevan.iyer@ece.gatech.edu

CALL FOR PAPERS

ECTC Emerging Technologies Program Committee

58th ECTC May 27th – May 30th, 2008
Orlando, Florida USA

The ECTC Emerging Technologies Program Committee encourages you to submit an abstract to ECTC 2007 in the areas of biomedical, organic, and nanotechnology packaging.

Bio and Biomedical Electronics: - Bio sensors & bio packaging - Microfluidic packaging - Implantable or embedded sensors - Bio compatible materials - Electronic packaging used in medical devices - Biomedical electronics manufacturing - Biomedical electronics design and reliability - Wireless communication for patient monitoring - Remote healthcare management - Reliability of Biomedical Devices - Interface of microelectronics to the neural systems

Organic/Flexible Electronics: - Materials: Active Materials, Encapsulation Materials, Patterning Materials, Thermal/Electrical Rheological Properties, Analysis, Inspection and Measurement Methods - Deposition Methods: Ink-jet, Vacuum, Gravure/Printing, Flexographic Deposition, and Process Integration - Applications: OLED, RFID, wearable, biomedical, passive and active components, design issues

Nano-Electronics: - Nano-Electronics Packaging - Devices, Assembly, Interconnects - Nano-Electronics Materials - Nano-Electronics Applications - Sensors, Actuators, and Detectors - Nano-Electronics Integration - Nano-Electronics Fabrication and Modules - Nano-Electronics Reliability and Failure Analysis - Nano-Electronics Metrology Tools - Nano-Electronics Design and Modeling

SUBMISSIONS: Please submit abstracts using the ECTC web site: **www.ectc.net** by October 15, 2007. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the "Emerging Technologies" focused sessions **YOU MUST SELECT**
"Emerging Technologies" committee as your PRIMARY subcommittee preference when you submit your abstract.

Michael Toepper, Chair – ECTC Emerging Technology PC, IZM, toepper@izm.fhg.com

Debendra Mallik, Assistant Chair – ECTC Emerging Technology PC, Intel Corporation, dmallik@ieee.org

CALL FOR PAPERS

ECTC OPTOELECTRONICS Program Committee

58th ECTC May 27th – May 30th, 2008
Orlando, Florida USA

Papers are solicited on all topics pertaining to the design, development, and technology of packaging optoelectronics and photonic components, devices, circuitry and systems.

Topics of interest include:

- **High Power Optoelectronics and Fiber Laser Packaging:** High-power laser diodes, bars / stacks, and Fiber lasers – including beam combining, coupling, wavelength control, hermetic packaging and thermal issues.
- **High-Brightness LED Packaging for Lighting and Commercial Applications**: Package and optical design, assembly methods, thermal management, reliability, color temperature control, phosphor materials, and volume manufacturing.
- **Optical Component Thermal Management and Reliability:** Optical component thermal management, package design, device performance, failure modes and reliability
- **Micro-optical Packaging and Manufacturing Technology:** Low cost designs, novel optics, assembly methodology and automation technology
- **Silicon Photonics Devices and Packaging:** Optical devices in Silicon, hybrid integration, FR performance, Silicon optical waveguides, photonics circuits and packaging
- **Optical Interconnects:** Integrated optics, high-speed and parallel transceivers, board-level waveguides, optical backplanes, fiber optic connectors and hybrid integration
- **Advanced Materials for Optoelectronics:** Substrates, devices, components and assembly materials

SUBMISSIONS: Please submit abstracts using the ECTC web site by **October 15, 2007**. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the "Optoelectronics" focused sessions **YOU MUST SELECT "Optoelectronics" committee as your PRIMARY subcommittee preference** when you submit your abstract.

Please visit:

www.ectc.net

You may also submit directly to the committee chair below – please include mailing address, telephone number, FAX number and e-mail:

Allen Earman
Novalux LDX
Tel: 408-730-3833
Fax: 408-730-3967
aearman@novalux.com

16th Conference on
Electrical Performance of Electronic Packaging
EPEP 2007

Sponsors:

IEEE Microwave Theory and Techniques Society
IEEE Components, Packaging and Manufacturing Technology Society

October 29-31, 2007

Renaissance Atlanta Hotel
Atlanta, Georgia

The general subject of the meeting is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. This meeting is the premier conference dealing with advanced and emerging issues in electrical design of interconnect structures and assurance of Signal Integrity. EPEP '07 has an outstanding technical program featuring more than 70 technical papers. The conference will feature paper sessions, a poster session and keynote speakers.

For further information, please see the web site at

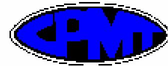
www.epep.org

Final Program

Future Directions in IC and Package Design Workshop (FDIP)

October 28, 2007, Atlanta, GA

sponsored by:



IEEE

COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY SOCIETY

organized by:

CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

1:15pm - 1:30 pm	**Welcome Remarks, Alina Deutsch, IBM, Madhavan Swaminathan, GIT**

SESSION I: SYSTEM DESIGN

1:30pm – 4:00 pm

Session Chair: George Katopis – IBM Corporation

1:30pm – 2:05pm	Signal Bandwidth for High Performance Computing – Dale Becker, IBM Corporation
2:05pm – 2:40pm	Wireless Proximity Communications for 3D System Integration - Tadahiro Kuroda, Keio University
2:40pm – 3:15pm	A Critical Assessment of the State of the Art in Multiscale Multiphysics Modeling of Microelectronics - Jayathi Murthy, Purdue University

3:15 – 4:00 pm - Refreshment Break

SESSION II: POWER DISTRIBUTION

4:00pm – 5:55 pm

Session Chair: Gregory Taylor, Intel Corporation

4:00pm – 4:35pm	Power Delivery Challenges for Mobile Platforms – Tawfik Arabi, Intel Corporation
4:35pm – 5:10pm	Modeling Challenges for Power Distribution Analysis – Madhavan Swaminathan, Georgia Institute of Technology
5:10pm – 5:45pm	Power Delivery System Design Challenges and Explorations on How to Overcome Them - Jiayuan Fang, Sigrity, Inc.
5:45pm – 5:55 pm	**Closing Remarks, Madhavan Swaminathan, GIT, Alina Deutsch, IBM**

Presentations will be posted on the IEEE CPMT Society web page at:
http://www.ewh.ieee.org/soc/cpmt/tc12/

EPTC 2007

9th Electronics Packaging Technology Conference

10th -12th December 2007 • Grand Copthorne Waterfront Hotel, Singapore

IEEE Reliability/CPMT/ED Singapore Chapter

First Call For Registration

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

EPTC 2007 Conference: 10th – 12th December 2007, Singapore

EPTC 2007 will feature 35 technical sessions with nearly 200 paper presentations by researchers from 19 countries; 7 invited papers by technical leaders in various categories; 6 short courses to be conducted by international experts and exhibition with participation of over 20 companies. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation to reliability. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

KEYNOTE ADDRESSES - 11TH DEC 2007

"Package Trends for Mobile & Communication Platforms" - Dr. Ralf Pleininger*, Senior Director, Infineon Technologies, Germany*

"Trends of Technologies for Heterogeneous Integration" - Prof. Herbert Reichl*, Director, Fraunhofer Institute of Micro integration & Reliability, IZM, Germany*

LUNCHEON TALKS - 11TH & 12TH DEC 2007

"Global Packaging Challenges" - Prof Rao Tummala*, Founding Director, Packaging Research Center, Georgia Institute of Technology, USA*

"Market and Technological Trends in Silicon IC and its Impact on Packaging Assembly" - Dr Sanjay Singh*, Director - Industrial Technologies, Frost & Sullivan Asia Pacific.*

INVITED PAPERS:

- **Package-On-Package Mechanical Reliability Characterization - *Masazumi Amagai***, *Texas Instruments, Japan*
- **Advances in Embedded Chip Packaging - *Charles Bauer***, *Tech Lead, USA*
- **Lasers for Packaging Applications - *Nick Konidaris***, *Electro Scientific Industries, USA*
- **Interfacial Reliability of SnAgCu Solder Joints - *Kejun Zeng***, *Texas Instruments, USA*
- **Testing Interface Thermal Resistance - *Marta Rencz***, *MicReD, Hungary*
- **Building Accuracies in Finite Element Models for Life Prediction of Solder Joints - *Ahmer Syed***, *Amkor, USA*
- **Electromigration and Sn Whisker Growth in Flip Chip Pb-Free Solder Joints - *King Ning Tu***, *UCLA, USA*

SHORT COURSES – 10 DEC 2007

Morning Session	Afternoon Session
Emerging Trend to SOP after SIP and 3D Packaging **Prof. Rao Tummala,** *Georgia Tech, USA*	**Signal Integrity and Embedded Passives** **A/Prof. Joungho Kim,** *KAIST, Korea* **Dr. Albert Lu,** *SIMTech, Singapore*
Design For Reliability and Reliability Testing & Statistical Analysis of Lead-Free Solder Joints **Dr. John Lau,** *IME, Singapore*	**Electromigration in Interconnect and Packaging Technologies** **Prof. King Ning Tu,** *UCLA, USA*
Analysis of Delamination in IC Packages Using the Fracture Mechanics Approach **Prof. Andrew Tay,** *NUS, Singapore*	**Dynamic Response of Micro- and Opto- Electronic Systems to Shocks and Vibrations** **Prof. Ephraim Suhir,** *UC Santa Cruz, USA*

More & More - it for - More Than Moore
Technology Exhibits, Poster Presentations, Industry Networking,
Parallel Technical Sessions & Industry Panel Discussion

EPTC 2007 REGISTRATION

http://www.eptc-ieee.net/registration/ Email: **secretariat@eptc-ieee.net / ivan@inmeet.com.sg**

General Chair	Technical Chair	Program Chair
Dr. Kripesh VAIDYNATHAN **Institute of Microelectronics, Singapore** **Email: kripesh@ime.a-star.edu.sg**	**Dr. Tong Yan TEE** **Amkor Technology, Singapore** **Email: tytee@amkor.com**	**Dr. Teck Kheng LEE** **Micron Semiconductor Asia, Singapore** **Email : leetk@micron.com**

2007 Electrical Design of Advanced Packaging and Systems

EDAPS-2007

15th and 17th, Dec. 2007

Taipei, Taiwan

http://EDAPS2007.ntu.edu.tw

ANNOUNCEMENT

The international workshop of EDAPS-2007 will be held in Taipei, Taiwan, R.O.C., on Dec.15-17, 2007. This workshop is the sixth EDAPS and is organized this year by the Department of Electrical Engineering of National Taiwan University, technically sponsored by IEEE CPMT Subcommittee on Electrical Design, Modeling and Simulation (TC-EDMS).

Objective The EDAPS-2007 International Workshop is to enhance the technical awareness in the Asia region specifically in the area of package and on-chip system electrical design concepts, issues, and challenges ahead for next generation electronic products.

International Advisory Committee

Alina Deutsch : IBM Corp., USA	Andreas Cangellaris : Univ. of Illinois, USA
Andreas Weisshaar : Oregon State Univ., USA	Ho-Ming Tong: ASE, Taiwan
F. G. Canavero : Univ. of Torino, Italy	James Libous : IBM Corporation, USA
José Schutt-Ainé : Univ. of Illinois, USA	Madhavan Swaminathan: Georgia Tech.,USA
Ravi Kaw : Avago Technologies, USA	Robert Jackson : Univ. of Massachusetts, USA
Yuan-Liang Li : Intel Corp., USA	Joungho Kim : KAIST, Korea
T. Sudo : Toshiba Company, Japan	E. P. Li : IHPC, Singapore

Topics :

Computer-Aided Design for SoC and SoP Modeling and Design	Interconnect Modeling, Design, Measurement , and Testing for SoC and SoP
EM and Thermal Modeling for SoC and SoP	EMC and EMI on SoC and SoP
RF, Microwave, Millimeter-Wave Circuit Packages	System-on-Packaging (SoP) Testing Strategies and Techniques
Package Reliability	RF-SoP on LTCC
Signal Integrity and Power Integrity	

Speakers The speakers consist of experts in the system integration field from around the world

Technically sponsored by IEEE CPMT Subcommittee on Electrical Design, Modeling and Simulation (EDMS)

Contact Details

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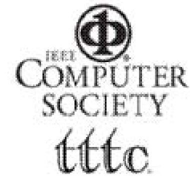
Email: wtl@cc.ee.ntu.edu.tw

National Taiwan University

http://www.ntu.edu.tw



CALL FOR PAPERS

12th IEEE WORKSHOP ON

SIGNAL PROPAGATION ON INTERCONNECTS

Pending Sponsorship by the IEEE Computer Society – Test Technology Technical Council (TTTC) and by the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society

First time in France!

May 12-15, 2008 -*"Pope's Palace", Avignon, France*
http://spi.univ-brest.fr

During the last ten years, the IEEE Workshop on Signal Propagation on Interconnects has been developed into a forum of exchange on the latest research and developments in the field of interconnect modeling, simulation and measurement at chip, board, and package level. The event is also meant to bring together developers and researchers from industry and academia in order to encourage cooperation. In view of the last years success the committee is looking forward to the 12th IEEE Workshop on Signal Propagation on Interconnects where world class developers and researchers will share and discuss leading edge results in Avignon, France. The workshop will be held in English. Detailed information about the workshop and its location are available on the website spi.univ-brest.fr. The committee is looking forward to your participation.

Main topics of the workshop will include, but are not limited to:

- Frequency Domain Measurement Techniques
- Time Domain Measurement Techniques
- Modeling Techniques of Package % On-Chip Interconnects
- Macro-Modeling
- Simulation Techniques for Interconnect Structures
- Electromagnetic Field Theory
- Analysis and Modeling of Power Distribution Networks
- Propagation Characteristics on Transmission Lines
- RF and Microwave Interconnects
- Coupling Effects on Interconnects
- Substrate Effects
- Guided Waves on Interconnects
- Radiation & Interference
- Electromagnetic Compatibility
- Power/Ground-Noise
- Testing & Interconnects
- Optical Interconnects
- Wireless Interconnects

Visit :
spi.univ-brest.fr

Submission of abstracts:

Those who wish to contribute to the workshop should send (by e-mail only) a formatted two-page or four-page paper to the Program Chair **by February 8, 2008** (please see the submission instruction on our website **http://spi.univ-brest.fr**). If the paper is accepted, it will be reproduced, as is, in the workshop proceedings. Notification about acceptance will be given by March 15, 2008.

Workshop Standing Committee:

Uwe Arz, Physikalisch-Technische Bundesanstalt, Braunschweig (Germany) *uwe.arz@ptb.de*
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Co-Chair: Prof. Fabrice HURET, LEST UMR CNRS 6165 – Université de Bretagne Occidentale (France) - Tel. +33 2 98 01 62 75; Fax +33 2 98 01 61 31; email Fabrice.Huret@univ-brest.fr
Program Chair: Prof. Michel NEY, LEST UMR CNRS 6165 – ENSTBretagne (France) - Tel. +33 2 29 00 13 09; Fax +33 2 98 01 63 95; email Michel.Ney@enst-bretagne.fr
Associate Program Chair: Dr Noël TANGUY, LEST UMR CNRS 6165 – Université de Bretagne Occidentale (France) - Tel. +33 2 98 01 71 57; Fax +33 2 98 01 63 95; email Noel.Tanguy@univ-brest.fr
Program Co-Chairs: Prof. Flavio CANAVERO and Prof. Hartmut GRABINSKI.

Technical Program Committee:

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T.R. Arabi, Intel (USA)
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A. Rubio, Univ. UPC Barcelona (E)
A.E. Ruehli, IBM, Yorktown Heights (USA)
W. Samaras, Intel (USA)
G. Sommer, Infineon, Munich (D)
N. van der Meijs, Univ. Delft (NL)
A. Weisshaar, Oregon State Univ. (USA)
T.M. Winkel, IBM, Boeblingen (D)

Institute of Electrical and Electronics Engineers, Inc.

Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter & Waves and Devices Chapter

PRESENT AN ALL-DAY WORKSHOP ON

Emerging Device and Packaging Technologies

Date: Tuesday, December 11th, 2007 **Time: 7:00 A.M. – 5:00 P.M.**
Location: Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

The semiconductor industry is entering an era with tremendous opportunities to exploit emerging technologies for the benefit of widely diverse markets. Moore's Law requires increasingly intensive materials innovations to maintain its momentum. Meanwhile, new markets in the areas of bio-electronics, sensors, etc., are leveraging the existing manufacturing infrastructure while incorporating new materials and techniques. This one-day workshop will bring together experts from industry, academia, research labs, and consortia to share their technology roadmaps and visions, novel materials and methods, and discuss technical opportunities. The status and challenges facing device, interconnect, and packaging technologies will be discussed in depth. Vendors will be on hand to exhibit products and services in all aspects of the supply chain for IC, packaging, and module design and manufacturing.

Topics

- Nanotechnology and Continuum Model Limits
- ITRS Roadmap Challenges
- SiP: 3D, Modules, Discrete Passives Integration
- Flexible Electronics
- Green Materials and Packaging
- Bioelectronics and Sensors Technologies
- General Industry and Technology Visions
- Panel Discussion on Future Challenges and Opportunities for Emerging Technologies

For General Information: **www.ieee.org/phoenix**

For Registration Forms: Sergio Pacheco (480) 413-3737

For Vendor Forms: Vladimir Noveski (480) 554-2375

CALL FOR PAPERS – **Semi-Therm 24**

ABSTRACT DEADLINE **October 20**

Abstracts for **Semi-Therm 24** are due on **October 20**, 2007. We are expecting an exciting list of sessions this year with several special sessions planned, so get your abstract in on time. We will be notifying accepted authors by December 1, 2007,and full manuscripts are due January 12, 2008.

Semi-Therm is soliciting papers on current thermal management technologies, practical application issues, modeling and measurement of electronic components and systems, including the following areas:

- Packaging Level
- Materials
- Modeling and Analysis
- Cooling Technologies
- Applications

The abstract should be between two and five pages of single-spaced text giving the key results, findings and conclusions, and should be supported by additional pages of figures tables and references as appropriate. Abstracts must demonstrate that proposed papers are appropriate for Semi-Therm and of high technical quality.

Semiconductor Thermal Measurement and Management Symposium
March 16-20, 2008,
San Jose, California USA

See full Call for Papers, other information on our website:

www.semi-therm.org

For further information, please contact the program chair via e-mail:

George Meyer
Celsia Technologies
meyer@celsiatechnologies.com
408-577-1407 office, 408-505-7921 cell

ESTC 2008

2nd Electronics System-Integration Technology Conference
1st – 4th September 2008, Greenwich, London, UK

Call for papers

Authors from industry and academia with innovative research or developments are invited to submit Abstracts for this forthcoming major international Conference. Papers from industry are especially important. Such papers will necessarily have product content. However, commercially oriented material and descriptions are not permitted either in the paper or in the presentation or poster. Authors will also benefit from the opportunity for papers to be selected from the Conference Proceedings for publication in IEEE CPMT themed journals. Poster papers will have specific scheduled presentation slots. Proposals for short-course Master Classes are also invited.

Themed topics of ESTC 2008 include:

- **Advanced Packaging**
- **Modeling, Simulation and Design**
- **Emerging Technologies**
- **Manufacturing Technology**
- **Assembly of Photovoltaics**
- **New Materials and Processes**
- **Power Electronics**
- **Reliability for Micro and Nano Systems**
- **Optoelectronics**

Special Sessions with invited speakers:

- **Green Electronics** • **Standards**
- **Prognostics and Health Management**
- **Photovoltaics – Asia Pacific**
- **European Business Global Council**

Call for Exhibitors

The ESTC 2008 exhibition will be based on a 3m x 3m shell scheme in an exhibit area which will accommodate more then 40 stands. Early bookings are strongly advised. Early bookers will receive a significant discount on the normal stand price as follows: The full stand price is £1800. A 20% Early Eagle discount is available for bookings made and paid for before **30th September 2007** and a 10% Early Bird discount is available for bookings made before **29th February 2008**.

General Chair Prof. Chris Bailey, University of Greenwich **chris.bailey@estc.biz**
Executive Chair Prof. Nihal Sinnadurai, Yeoman Protex International, **sinnadurai@estc.biz**
Programme Chair Rolf Aschenbrenner Fraunhofer IZM, **aschenbr@izm.fraunhofer.de**

The 2nd ESTC **Electronics Systems-Integration Technology Conference** (ESTC 2008) follows the very successful first ESTC held in Dresden in 2006. ESTC 2006 comprised over 200 technical papers, outstanding Invited Speakers and an attendance exceeding 400 from across the globe, supplemented by 6 short courses with over 50 attendees. A major technical exhibition was held alongside the Conference - an excellent opportunity for suppliers of materials, design houses, circuit manufacturers to promote their products and reach potential customers.

ESTC 2008 will be held at Greenwich, a World heritage site and major maritime site on the banks of the River Thames in the magnificent city that is London. The Conference and Exhibition will be hosted by the University of Greenwich in the buildings of the former Royal Naval College. Plenary sessions will be in the Great Painted Hall - providing a wonderful ambience for the technical presentations. The exhibition will accommodate more than 40 stands and aims to be the quality event in microelectronics and micro-systems in Europe.

Abstract Guidelines

An abstract means abstracting a summary of the whole paper, presentation, or research project. This includes a summary of the purpose of the research or activity (i.e. what was the problem), followed by a summary of the method used to solve the problem and finally a summary analyses and conclusions including summarising actual data. The skill of an author is in being able to convey summary information concisely and imformatively. The adjunction process may remove authors' names and affiliations. So, well known authors as well as new authors are urged to respect the request to submit a full and true abstract.

- Deadline for receiving Abstracts is **31st January 2008**
- Successful and Unsuccessful authors will be notified no later than 31st March 2008
- Publication-ready full papers are required no later than 31st May 2008 for final adjunction on compliance with the approved Abstract and technical requirements of the Conference.

More information: **www.estc.biz**

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Call for Papers – Abstracts Due January 31, 2008

See Page 23, inside

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