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The Global Society for Microelectronics Systems Packaging

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www.cpmt.org
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VP-Publications Column…..

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VP-Publications, IEEE CPMT Society
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After 22 years (11 terms) as the head of CPMT's Publications function, I concluded my final term in December. Your new VP of Publications is Prof. Wayne Johnson of Auburn University.

I've certainly enjoyed the confidence that the Society has placed in me. During my terms our Transactions have grown from about 800 pages/year to over 2000 (or about 300 papers), with two of the three journals now having an impact factor of 1.0 or higher (our target for 2007). A number of years ago I moved our review tracking system to the beta version of Manuscript Central, for better centralization of paper flow and control, and this has been a key enabler for the expansion. When I started there was one Editor in Chief; now we have 5 EICs covering our wide range of technical fields in our three journals. All of the EICs are recent appointments and are serving ably.

During the early part of my tenure, the Society was running annual deficits and was rapidly depleting its reserves. With changes that I implemented, the Transactions is now generating about US$370k in yearly surplus as I turn them over to my successor, with another $500k/year in conference publications income that I have grown and supervised. We are now a rich Society, and a very careful one in using these resources generated by the work of our volunteers over the past years. In contrast to the near-zero reserves in the early '90's, we now have reserves of about $3.5 million.

As I step down, I feel that the Transactions portion of my responsibilities is in good hands, with Prof. Avram Bar-Cohen at the University of Maryland as our Director of Transactions. With approval at last June's BOG meeting of temporary funding for one year of staff support, he is working on two current projects: to assure that all Reviewers have keywords entered into MC so that Associate Editors can better locate strong reviewers for specific papers; and to find those papers that are lagging in the MC system waiting for their next steps to be taken.

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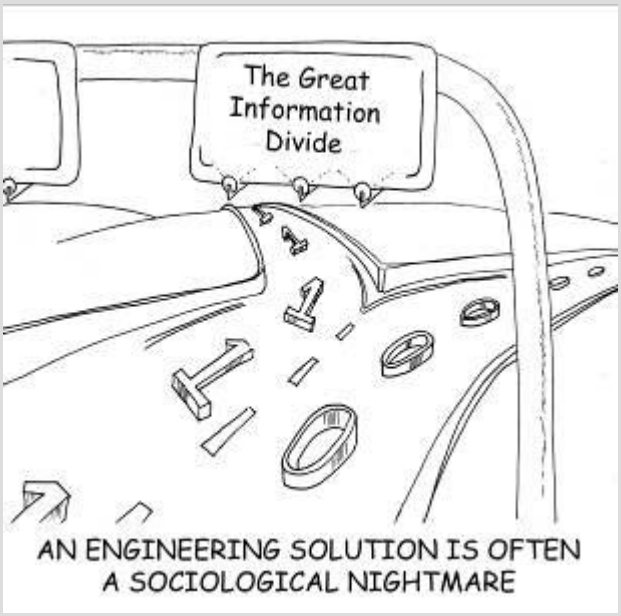
Cartoon of the Month:



… By Dave Palmer

IEEE CPMT Society Newsletter
September, 2007

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Philip C.H. Chan, Paul D. Franzon, R. Wayne Johnson, Kwang-Lung Lin, Petri Savolainen, and Leonard W. Schaper

2008:
Vasudeva P. Atluri, Li Li, Dongkai Shangguan, Patrick Thompson, Klaus-Jürgen Wolter, and Kishio Yokouchi

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Chapters and Student Branches

Refer to **www.cpmt.org** for CPMT Society Chapters and Student Branches list

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2008 Deadlines for Submitting Articles:
February 25th, 2008 **May 25th, 2008**
August 25th, 2008 **November 25th, 2008**
Only Articles Sent to nsltr-input@cpmt.org will be included in the newsletter
Members-only Web (www.cpmt.org/mem/)
UserName: **(available only**
Password: **to members)**

VP-Publications Column *(Continued from Page 1)*

I believe that the Manuscript Central reviewing function will be made much better for the Associate Editors, and that timely intervention in lagging papers is a good step in the direction of the 90-day average turn-around time (from author submittal to return of reviews to the author) that IEEE wishes.

One of the goals that CPMT president Bill Chen has articulated is for each functional area of the Society to work proactively with other CPMT entities and with our stakeholders – authors, researchers, volunteers, institutions. I began a project in the 1990's to building relationships with our various journal stakeholders – Editors, Reviewers, Authors, and corporate/university subscribers – through Editorial Board meetings at major and mid-sized conferences. These will continue under Wayne Johnson's leadership, and I may assist in some of them for the next year or so.

In 2007 I began a series of workshops at our major conferences to serve as training sessions with guidelines for writing high-impact papers for our Transactions. Avi Bar-Cohen was instrumental in gathering much of the content, with Ricky Lee monitoring the Impact Factors for us. The first Workshop was at ECTC in Reno, with the second at EPTC in Singapore. You should be able to attend one during 2008 at ECTC in Orlando and at ESTC in London.

The quarterly CPMT NEWSLETTER continues to be printed and mailed, but in 2007 I began a twice-a-quarter e-Newsletter that is emailed to all members as well as to non-members on our ListServ dlist. This has provided a more timely way to bring current events to our members' desktops. This is a project that I may be continuing as I retire as VP of Publications.

A goal of mine has been to extend the reach of the CPMT Society beyond only our paid members, to include 50,000 or more technical professionals in our fields, through collection of conference, chapter, IEL, and other relationship information. My objective has been to meld them into readers of our e-Newsletter and users of our research results and other publications/conferences products.

I'll continue serving as CPMT's webmaster. My interest/focus for the IEEE's Santa Clara Valley Section and its SF Bay Area Council is the new field of social networking (community forums, blogs, RSS, wiki's, collaborative services), and some of these may be useful to the Society at some point for establishing its own communities around the Technical Committees, Chapters, and conferences. I've set up blogging software (WordPress) on my server, and it automatically sends out RSS feeds; this "subscription" technique seems to be replacing email as a way to distribute news to small communities, and therefore it'll be important for the younger engineers that CPMT wishes to attract, both as members and as customers.

It has been a high honor to serve the CPMT Society over the past decades, and I look forward to some level of continuing engagement with the Society and its members.

Best regards, and best wishes always,
Paul

CPMT Society News:

Results of Election of CPMT Society Officers

Submitted by Ms. Marsha Tickman, Executive Director, IEEE CPMT Society

Twenty-five voting members participated in the election of CPMT Society Officers, including 18 Members-at-Large -- constituting a quorum.

The following candidates were elected:

PRESIDENT: William T. Chen

VICE PRESIDENT, TECHNICAL: N. Rao Bonda (incumbent)

VICE PRESIDENT, CONFERENCES: Rolf Aschenbrenner (incumbent)

VICE PRESIDENT, PUBLICATIONS: R. Wayne Johnson

VICE PRESIDENT, EDUCATION: Albert F. Puttlitz (incumbent)

VICE PRESIDENT, FINANCE: Thomas G. Reynolds III (incumbent)

The terms of office began on 1 January 2008 and run for two years.

Congratulations to all.

*****

Your Board Storms Their Brains

Submitted by Dr. Dave Palmer, IEEE Fellow

Your Board of Governors held a workshop on Friday November 9 until late at night. About 25 volunteers brainstormed on two related topics: How to grow the CPMT Global Community? How to get synergy between the great but independent efforts by many volunteers? First the BOG listed all the stakeholders in the CPMT Global Community so they could see the problems from every perspective.

Examples of individual ideas discussed:

1. What if we had a video made by each CPMT Distinguished lecturer? Perhaps many chapters could use the lectures linked to a telecomm Q & A session without demanding the lecturers to spend days of travel.
2. What if we marketed the Distinguished lecturers to the new chapters. Right now they have a conference emphasis?
3. How can we mutually benefit more from the 500 CPMT *Transactions* authors, 500 reviewers, and 10,000 readers each year? It was pointed out that tech companies pay IEEE $70M each year to get access to the Society electronics library.
4. Can we make an Internet tutorial that teaches our global community to mine the electronic CPMT documents more effectively?
5. Can we start more Technical Committees whenever we suspect about 25-50 people in the world get interested in one of our hot topics? On the other side, we must be willing to let the TC dissolve after a few years to not waste peoples' time on topic with little interest.
6. Can we formally survey our chapters to see what we could be doing better? Could we establish a resource area on the CPMT website for chapters?
7. Do we have a process to obtain Distinguished Lecturers from all over the world?

8. Should we encourage more focused workshops to let engineers from many organizations get together in an unpublished conversation?
9. Don't avoid supporting existing chapters as new ones are created. Remember chapters are 80% the responsibility of their IEEE Section.
10. Is it possible to do a webcast of the BOG so more volunteers can coordinate their efforts, in particular Chapter Chairs?
11. Would virtual attendees to our conferences get more benefit in less time?

About ten Board members signed up to continue working on one of the two questions during the next six months and present proposed actions at the May ECTC Board meeting.

*****

Board of Governors Does Dallas

Submitted by Dr. Dave Palmer, IEEE Fellow

Your Board of Governors showed up 26 strong on November 10th in Dallas Texas for their second business meeting of the year.

President William Chen presented the State-of-the-Society in the morning. The IC industry was down in the first quarter then strongly up in the second. Most predictions are for a strong 2008. A strong market in integrated circuits results in a strong market for components, packaging, and assembly. As a result, many places in Asia are worried about keeping their experienced engineers. In contrast, the North American job market is not so rosy. When he asks universities "Where do graduate students find jobs in our technologies?" they say the students find positions but in unexpected places. Mainframes and PCs are not driving the advanced packaging industry. The Cell phone market is supporting more advanced development than any other. For example, cell phones support much of the through-silicon vias and 3-D chip stacking development. New approaches are being quickly brought to market. This focus and speed suggest we need training in how global industry functions so graduates can perform efficient design and product engineering in today's industry. How to function on an international scale is different from what most of our members' past experiences have been.

President Chen reported that a record number of papers were submitted to the 2008 ECTC. This conference appears to have become a "must" where companies and engineers try to put their best foot forward. In addition, conferences such as IMPACT in Taiwan, ICEPT in Shanghai, and ISEMP in Korea have gained in strength.

CPMT publications have improved with our conference proceedings now available under the IEEE umbrella purchase plan. We have steps in process to increase the "impact" of our *Transactions* resulting in more papers of interest to our members. A "publications workshop" held at CPMT conferences around the globe should continue to increase the worth of our publications.

Technical Committees are the focus for our conferences and workshops. Hot topics, such as 3-D packaging, should be permitted to have a new TC even if the committee will be done with its work in a few years.

Our short professional development courses have been a great success. We must also become creative in helping Universities teach about our technologies and business methods.

We have three new chapters in Poland, Germany, and Austin-Texas. Many of the existing chapters are remaining active. For the last year the CPMT Award and Recognition process has worked very well. Our Society's fellow nominating process has worked very well with a record number being submitted to the IEEE Fellow committee for determination. Because our Society has many members active for the betterment of our profession, CPMT has a high percentage of Fellows.

CPMT financial condition is excellent after a few years of discipline to bring us back from the edge of bankruptcy. We have been frugal so long that now we need to learn to spend the investment money that we vote for. We must use our resources wisely, but we must use them.

The continual question for the Board is "How can we build better value propositions for our community with publications, conferences, chapters, and education?"

Your President's roles are

1. Be an Ambassador of the Society, especially in global areas of growth
2. Work with the Board to provide more value to members
3. Help Finance Vice President commit resources to the right places.
4. Assist Conferences and Publications when needed.
5. Unite the different thrusts in our Society synergistically.

William Chen has agreed to seek continuation of his presidency for another 2 years.

Thomas Reynolds, vice president of finance, presented the details of the CPMT budget. Our conference income is now above $1M/year and still growing. This has allowed us to fund new or expanded meetings during their start-up period. Our reserve funds are put in an investment pool and the income varies greatly from year to year (sometimes becoming a loss). This year our interest income will be over $200K. As always Publications are a large part of our Society income thanks to the many pages of quality papers and the many electronic requests for these papers. Our total income will exceed $2.5M and we will probably have a small excess at the end of the year to add to our reserves.

Tom encouraged all Board members with responsibility to use budgeted money on executing Board plans. Because we can spend 3% of our reserves and 50% of last year's surplus in any given year, we are positioned well for starting new efforts.

Al Puttlitz, Vice President of Education, discussed the 9 formal presentations by CPMT Distinguished Lecturers so far this year. Dr. Ning-Cheng Lee of Indium Corporation of America was elected as a new CPMT Distinguished Lecturer. A long discussion ensued about the many presentations made by the 31 Lecturers in the name of CPMT but where no help from the Board is needed. Al would like more Chapters to use the speakers and will try to make it easier for Chapter Presidents to know who is available and how to make arrangements.

Al also described the large submittal of abstracts aimed at the Motorola/CPMT Ph.D Fellowship and CPMT Ph.D Fellowship at the upcoming ECTC08. There were 93 abstracts for the first and 99 for the second. Several of our other meetings (EMAP) are considering larger best paper awards and best student paper awards in order to bring the best work to our conferences.

Kitty Pearsall, Strategic Program Director of Awards, had her report given by Al Puttlitz. They announced that the IEEE Field Award in Packaging and Manufacturing Technology was given to Dr. Karl Puttlitz and Mr. Paul Totta for developing and perfecting the C4 interconnection Chip to Substrate Bump Technology. The CPMT Awards Committee has an excellent global mix of university and industry members: Charles Lee of Infineon, Ning-Chin Lee of Indium, Kwang-Lung Lin of National Cheng Kung University-Taiwan, Petri Savolainen of Nokia, Ephraim Suhir of University of California, Ralph Russell of Virginia Power, Klaus-Jurgen Wolter of Technische Universitat Dresden, and Kitty Pearsall of IBM. The committee is glad that they have a number of nominees for the IEEE Field Award lined up but is asking for more nomination for all awards. In particular, it was suggested that CPMT Chapters submit nominations.

A discussion over a proposed "CPMT Regional Technical Contribution Award" brought out a number of interesting points on local versus global awards. The decision was delayed until the Award Committee can go through the feedback and make a new proposal.

Phil Garrou's nomination committee report was given by Marsha Tickman. The election results of the Members-at-Large for 2008-2011 were to be announced the following Monday: Steve Bezuk, Kitty Pearsall, Eric Perfecto, Ephraim Suhir, C.P. Wong, and Eric Beyne.

C.P Wong, Chair Fellows Committee, stated that 10 high caliber nominating packets were sent to the IEEE Fellow selection committee. Historically about half the nominees are awarded each year. The fellows committee: Ephraim Suhir, Alina Deutsch, George Harman, Rajen Chanchani, C. P. Wong (chair).

Tony Mak, Constitution and Bylaws Chair, had his report presented by Marsha Tickman. A lot of our Constitution has been mandated to be moved to the Bylaws to make the organization more flexible. IEEE also dictates that some new wording be inserted that prevents problems that have occurred in other Societies. All members will see these changes in an upcoming Newsletter.

C. P. Wong reported on the upcoming ECTC. The organizing committee has lined up 16 leading-edge professional development courses. 616 abstracts were submitted for the meeting. 42% were selected for presentation or poster sessions. An additional student poster session was created. ECA, the cosponsor, will increase their visibility at this conference, however, the ECTC is for the professionals in our technology and is not a marketing venue for industry.

Evening sessions will consist of: Product Development in Semiconductor Industry, 3-D Packaging coming to Reality, and Advanced Embedded Passive and Active device Technology. Itherm is collocated with ECTC.

Rao Bonda, Technical Vice President, presented a proposal for a Task Force on 3-D Electronics. This committee will provide an international forum for researchers and practitioners of 3-D electronics. Paul Franzon of North Carolina State University is taking the organizational lead. The scope will include processes, applications, and design of 3-D electronic systems and sub-assemblies.

Rolf Aschenbrenner, Vice President of Conferences, described the CPMT flagship conferences in 2008: ECTC in May at Disney World, ESTC in September in London, and EPTC in December in Singapore. He listed the 20 conferences that our Society has a major role in. Rolf described the merging of the ICEPT and HDP meetings in 2008. He then summarized the recent direction setting CPMT European meetings: Workshop on 3-D System Integration (Munich, Oct 2007), European Microelectronics and Packaging Conference & Exhibition (Oulu Finland, June 2007), Electronics System-Integration Technology Conference (London, Sept 2008), Electronics System-Integration Technology Conference (Berlin, Sept 2010), Polymers and Adhesives in Microelectronics and Photonics (Garmisch-Partenkirchen, Germany, August 2008), Spring Seminar on Electronics Technology (Budapest, May 2008).

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IEEE-CPMT Society Awards for Year 2008

(Nomination Due Date: January 31, 2009)

Submitted by Dr. Kitty Pearsall, Strategic Director, IEEE CPMT Society

The CPMT Strategic Awards Director announces the call for nominations for their five, 2008 Society awards. The CPMT Society offers these awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society. While a nominee may have a specific award in mind when applying, the Awards Recognition Committee reserves the right to consider any nomination for awards other than the award suggested when, in its opinion, the support and justification may more appropriately apply to a different CPMT Society award. Winners will be notified by 28 February 2008 and the awards will be presented at the 58th Electronic Components and Technology Conference, May 27- My 30th, 2008, in Lake Buena Vista, Florida, USA.

After reviewing the high level summaries presented below, you will find a list of nomination submission requirements. The awards nomination form can be found on the CPMT Society Awards Home page (**www.cpmt.org/awards**).

- **David Feldman Outstanding Contribution Award:** This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
  Prize: $2,500 and Certificate
  Basis for Judging: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.
  Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2007.

- **Outstanding Sustained Technical Contributions Award:** This award recognizes outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.
  Prize: $2,500 and Certificate
  Basis for Judging: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably ten (10) years. One major contribution ***will not*** qualify. Contributions must be documented by open literature publications

such as papers, patents, books and reports (available to the public).
Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2007.

- **Electronics Manufacturing Technology Award:** This award recognizes major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
  Prize: $2,500 and Certificate
  Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.
  Eligibility: No need to be a member of IEEE and CPMT Society.

- **Exceptional Technical Achievement Award:** This award recognizes an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
  Prize: $2,500 and a Certificate.
  Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution ***will*** qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.
  Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2007. There are no requirements for service to the IEEE or CPMT Society.

- **Outstanding Young Engineer Award:** This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.
  Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.
  Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.
  Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2007, and must be 35 years of age, or younger, on December 31st, 2007. Please provide Date of Birth (Month/Year) to ensure eligibility.

Guidelines for Nominators:

- Minimum three (**3)** reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.
- Past recipients of an award are not eligible to receive that same award a second time. For a list of past awardees, see the CPMT Society Awards Home page (**www.cpmt.org/awards**).
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
- Please send nominations to CPMT Awards Committee Chair by e-mail, fax or mail. If you fax a nomination, please follow-up with an email.

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IEEE Fellow Nomination Process

Dr. David Palmer, IEEE CPMT Fellow Search Committee

March 1st was the deadline for submitting nominations for the next group of IEEE Fellows of the Institute which will be announced at the end of 2008. Thus, it is a good time to remember what the quest for Fellow is about and to get ready to start the process for the next year. To quote from the IEEE web site:

"The grade of Fellow recognizes unusual distinction in the profession and shall be conferred only by invitation of the Board of Directors upon a person of outstanding and extraordinary qualifications and experience in IEEE-designated fields, and who has made important individual contributions to one or more of these fields."

The total number selected in any one year does not exceed one-tenth percent of the total voting Institute membership. For the last few years about 250 new Fellows have been appointed out of about 600 nominations. CPMT averages about 5 new Fellows a year. We have more than 100 Fellows in our current Society membership of 3000.

In addition to professional distinction, the qualifications an IEEE member needs before being nominated are:

- Must be a senior member at time of nomination
- Must be current in dues (yes, even distinguished engineers forget to renew)

- Must be a member for 5 years (Affiliate member does not count)
- Nominator must get all forms to IEEE web site by March 1st

Through this year one could download the forms, fill them out, and mail them to IEEE headquarters. For the coming year the system will be completely electronic, working from the IEEE web site. Perform a search on "Fellow nomination" from the new www.ieee.org page and you will get the complete process instructions.

If you know someone who qualifies for the Fellow level you can be a nominator. You do not need anyone's permission. If you need more guidance than is on the IEEE web site you can contact anyone on the CPMT board of Governors or talk to Rao Tummala or Dave Palmer on the Fellow Search committee (see contact information on page 2).

The best steps to success are:

1. Have the Fellow candidate write an extensive resume and list all publications and presentations they have made. With this information you complete the IEEE Fellow nomination form on the web (but make a copy that you can send to potential references). It is usually important to focus on the several technical and organizational contributions that distinguish the candidate in their field. This is typically better than to list only a thousand small contributions that total a lot but did not make an obvious big difference in any technology or organization.
2. Line up between 5 and 8 Fellows in related fields that know of the candidates work or can quickly appreciate it. For example, if the candidate contributed in thermal management, there are a number of Fellows in CPMT that would be ideal for reviewing the nomination.
3. Push everyone to submit everything in February at the latest. About half the nominations miss the deadline and must wait for the next cycle. As the nominator you will have access to the IEEE Fellows Application database and be able to see which references have yet to be submitted.
4. Let C. P. Wong on the CPMT Fellows Review Committee know that you are working on a nomination so he lines up enough society reviewers.

Once a nominator has done their job the work load passes on to C. P. Wong's committee. They review all the nominations submitted in the name of the CPMT Society. All nominations must go through a Society or Council. At this point it is important to have a nomination form that clearly states the candidate's service to IEEE, the Society, and the profession. A member that has spent many years organizing CPMT conferences or producing our publications has a natural advantage in the process of winning a professional award compared to an equal technical contributor but a non-participating member.

In a typical year the Fellow review committee will score and rank about 10 nomination packages and forward them to the IEEE Fellow committee. Historically our submitted nominees have about a 50% success rate. Submitting someone for a series of years is common and should not be considered bad luck by either the nominator or the candidate.

The process takes typically about 20 hours by the candidate, 30 hours by the nominator, and 5 hours by each Fellow reference. CP's team spends many days in the process trying to strengthen every package and to get the right feedback to the nomination.

The Fellow Level recognition is among the highest in our engineering profession. Universities and Companies proudly state the number of Fellows in their staff. As CPMT Society members read the list of Fellows they nod knowingly as they see name after name of admired peers. If your time has come, start the nomination process.

CPMT Fellows

Dr. Vasudeva P. Atluri, Editor-in-Chief,
IEEE CPMT Society Newsletter

Daniel Ammey	Cristina Amon	Yasuhiro Ando
Inder Bahl	Henry Baltes	Diana Bendz
D. Berlincourt*	Gary Bernstein	Joe Brewer*
David Blackburn	William Brown*	L. Burrage*
C. Campbell*	Flavio Canavero	Andreas Cangellaris
Zoltan Cendes	H. Anthony Chan	Yan Chan
Rajen Chanchani	Harry Charles	William Chen
Fan-Tien Cheng	George Chiu	Kenneth Clarke*
Evan Davidson	Alina Deutsch	James Drewniak
Charvaka Duvvury	Charles Eldon*	Aicha Elshabini-Riad
Irving Engelson*	Leslie T. Falkingham	Leonard Feinstein
Wolfgang Fichtner	Paul Franzon	Daniel Gamota
Philip Garrou	Ronald Gedney*	Randy Geiger
Stanley Gershwin	Barry Gilbert	Bernard Gordon
Dimitry Grabbe	Martin Graham	Aditya Gupta
Ronald Gutmann*	George Harman*	J. Harnden*
Erik Heijne	Eric Herz*	J. Hilibrand*
Philip Ho Chan	Todd Hubing	K. Irani*
Rolf Jansen	R. Wayne Johnson	Nan Jokerst
George Katopis	Ravindhar Kaw	Jorma Kivilahti
Harry Kroger*	R. Lafferty*	Kanneth Lakin*
John Lau	Chin Lee	Shi-Wei Lee
Er Li	Johan Liu	Jusheng Ma
Gary May	Michael McShane	James Meindl*
Robert Mertens	James Morris	George Moschytz*
Arthur Murphy	Khalil Najafi	Wataru Nakayama
Michel Nakhla	Luu Nguyen	Istvan Novak
Antonio Orlandi	Kanji Otsuka	David Palmer
Michael Pecht	S. Pookaiyaudom	W. Arthur Porter*
John Powers	Karl Puttlitz	Tawfik Rahal-Arabi
Herbert Reichl	Hugh Ross*	A. Ruehli*
Leonard Schaper	Jose Schutt-Aine	Dongkai Shangguan
John Segelken	Gustave Shapiro*	B. Siegel*
Nihal Sinnadurai	Paul Slade*	John Stafford
D. Strain	Yan-Kuin Su	Toshio Sudo
Ephraim Suhir	Madhavan Swaminathan	Tasuku Takagi
Stuart Tewksbury	Ho-Ming Tong	W. Trybula*
Leung Tsang	Tseung Tseng	Rao Tummala
Yonhua Tzeng	Ifeanyi Ume	Jacobus Vanwyk
Kikuo Wakino*	Mauro Walker*	Andreas Weisshaar
Paul Wesling	O. Winn*	Ingo Wolff*
C. P. Wong	Ralph Wyndrum*	Hiroshi Yamada
Naoaki Yamanaka	Qi-Jun Zhang	Bin Zhao

*Life Fellow

IEEE Senior Membership

Dr. Vasudeva P. Atluri, Editor-in-Chief,
IEEE CPMT Society Newsletter

The Grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. The candidate should be an engineer, scientist, educator,

technical executive, or originator in IEEE designated fields. Candidate shall have shown significant practice for at least ten years and shall have shown significant performance over a period of at least five of those years.

Benefits of IEEE Senior Membership Include:

- The professional recognition of your peers for technical and professional excellence.
- An attractive fine wood and bronze engraved Senior Member plaque to proudly display.
- Up to $25.00 gift certificate toward one new Society membership.
- A letter of commendation to your employer on the achievement of Senior member grade (upon the request of the newly elected Senior Member.)
- Announcement of elevation in Section/Society and/or local newsletters, newspapers and notices.
- Eligibility to hold executive IEEE volunteer positions.
- Can serve as Reference for Senior Member applicants.
- Invited to be on the panel to review Senior Member applications.

For additional information including requirements and application process refer to IEEE Senior Member Program website located at **www.ieee.org/web/membership/senior-members**.

Contact representatives of the section or society you belong to for any further assistance and suggestions.

CPMT Senior Members

Dr. Vasudeva P. Atluri, Editor-in-Chief, IEEE CPMT Society Newsletter

Congratulations to the following CPMT Society members for achieving Senior Member status during 2007:

Atlanta Section :	Jianmin Qu
Buenaventura Section:	Roberto Coccioli
	Michael Ingham
	James Schlaffer
Boston Section:	Jilin Tan
Central Coast Section:	Jianbiao Pan
Central Texas Section:	Paul Harvey
	Ramakrishna Koneru
Central Washington Section:	Howie Johnson
Cincinnati Section:	Clayton Sippola
Dayton Section:	Ronald Coutu
Eastern North Carolina Section:	Robert Evans
	Jonathan Hinkle
	Alan Huffman
France Section:	Richard Perdriau
	Tan Phu Vuong
Germany Section:	Hubert Harer
Madras Section:	Subha Rani
Malaysia Section:	Azhar Aripin
Mid-Hudson Section:	Oliver Patterson
Milwaukee Section:	Jeffrey Kautzer
Montreal Section:	Ramesh Abhari
Northwestern Subsection:	Janice Danvir
Orange County Section:	Wei Koh
	Volkan Ozguz
Oregon Section:	Farhad Akhavan
	Paul Crump
Phoenix Section:	Xuejun Fan
	Subhadarshi Nayak
	Chandrasekhar Ramaswamy
	Ioan Sauciuc
	Sandeep Tonapi
San Diego Section:	Mikaya Lumori
Santa Clara Valley Section:	E. Aoki
	R. Kollipara
	Kyung Oh
	Michael Skinner
	Ji Zheng
Singapore Section:	Charles Lee
Tainan Section:	Yi-Shao Lai

Member Recognition:

Dr. Kitty Metcalfe Pearsall Named Distinguished Engineering Graduate

Dr. Vasudeva P. Atluri, Editor-in-Chief, IEEE CPMT Society Newsletter

The Cockrell School of Engineering, University of Texas, located in Austin, Texas, announced 2007 Distinguished Graduates on December 7th, 2007. Four alumni were elected Distinguished Engineering Graduates of The University of Texas at Austin and were honored at fall commencement ceremonies on December 8th, 2007.

The annual selections, made by the Cockrell School's Engineering Advisory Board, are based on outstanding professional records, public service, support of education, and other significant achievements.

The 2007 Distinguished Engineering Graduates are: Portland State University Emeritus Dean Chik Erzurumlu, IBM Distinguished Engineer **Kitty Pearsall,** consultant, inventor and California Insurance Commissioner Steve Poizner, and owner and manager of HAT Resources Harry Trueblood Jr.

Dr. Kitty Metcalfe Pearsall earned a bachelor's degree in metallurgical engineering in 1971 from the University of Texas at El Paso. In 1972 she joined IBM as a materials engineer, but took an educational leave of absence in 1976. She earned her master's and doctoral degrees in mechanical engineering with a materials option from The University of Texas at Austin in 1979 and 1983 respectively. Since returning to IBM in 1983, she has been a technical resource in materials/package engineering in manufacturing, procurement and development environments with 12 years spent in technical management focusing on the qualification of various commodities.

In 2005 Pearsall was appointed an IBM Distinguished Engineer (DE) and elected into the IBM Academy of Technology. As a DE in IBM's integrated supply chain, she serves as a process consultant and subject matter expert working on strategic initiatives impacting qualification and end quality of procured commodities. She is engaged with world wide teams implementing cross-brand, cross commodity processes/products.

Pearsall has been a licensed professional engineer in Texas since 1993. She is the holder of one U.S. patent, four patents pending and several patent disclosures that have contributed to the IBM patent portfolio. She has authored numerous internal publications as well as 17 external publications for the Institute of Electrical and Electronics Engineers' conferences and journals.

She is a role model to others both technically and professionally, and embraces her role as mentor. She devotes endless time to mentoring – and promoting the engineering career path to technical women professionals – by providing career guidance, engineering advice, and "lessons learned." She actively supports the development, advancement, and recognition of IBM's technical talent. She was recognized this year for her endless drive and passion for mentoring and people development and presented with the Women in Technology "Frances E. Allen Mentoring Award."

Her work with the Society of Women Engineers has had an inspirational effect on today's female engineering students, and she continues to promote engineering as a superb profession for young women to enter.

Pearsall continues to support the Cockrell School of Engineering with contributions to the Friends of Alec spanning more than 20 years.

About UT's Cockrell School of Engineering:

The University of Texas at Austin's Cockrell School of Engineering ranks among the top six public engineering schools in the United States. With the nation's fourth highest number of faculty elected members of the National Academy of Engineering, the School's more than 7,000 students gain exposure to the nation's finest engineering practitioners. Appropriately, the School's logo, an embellished checkmark used by the first UT engineering dean to denote high quality student work, is the nation's oldest quality symbol. The School maintains a Web site at www.engr.utexas.edu.

Chapter Reports:

Singapore REL/CPMT/ED Chapter Update

Submitted by Alastair Trigg, Chair - IEEE Singapore Rel/CPMT/ED Chapter

On 30th October the chapter organised a technical talk on "Thermal Microsystems for Electronics Thermal Management across Multiple Scales" by Professor Suresh V. Garimella, Director of NSF Cooling Technologies Research Center at Purdue University.

Mr Li Wei a student from the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU) in Singapore won the inaugural prestige 2007 IEEE Electronic Device Society Masters Student Fellowship. Only five awards, each worth US$2000, are given worldwide per year.

The final preparations are underway for the CPMT flagship packaging conference in Asia, the 9th Electronics Packaging Technology Conference (EPTC 2007). This is being held in Singapore 10th to 12th December. Over 250 abstracts were submitted from 19 countries, and from those the EPTC Technical Committee selected 175 papers to be presented in 34 oral and 1 poster session. On 10th December there are six short courses and two technical forums. The Conference sessions begin on 11 December with two keynote presentations by Dr Ralf Plieninger, Senior Director, Packaging at Infineon and Prof. Herbert Reichl, Director of the Fraunhofer Institute for Reliability and Microintegration. Together with the contributed papers, there are two luncheon talks and seven invited talks. There is an equipment exhibition in conjunction with the conference Full details of EPTC can be found at the website: www.eptc-ieee.net. During the course of EPTC, IEEE Singapore REL/CPMT/ED Chapter awards will be presented to outstanding students from Nanyang Technological University and Temasek Polytechnic.

Prof. Yeo, HOD of Circuits and Systems presenting the certificate to Mr. Li Wei on September 18th, 2007

From left: Prof. Yeo, Prof. Tan Cher Ming (Li Wei's supervisor), Li Wei and Prof. Pey Kin Leong who nominated Li Wei for the award.

The chapter's flagship conference on failure analysis, the International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2008) will be held in Singapore from 7th to 11th July 2008. The call for papers is available at ewh.ieee.org/reg/10/ipfa/ The deadline for abstracts is **18th January 2008.** In 2008 IPFA will be holding its first Photo Contest – *the Art of Failure Analysis 2008*. In addition to the popular IPFA equipment exhibition, there will an additional opportunity for company promotion through sponsorship packages. Information on all aspects of IPFA is available on the website.

Download the PDF version of this NEWSLETTER, to circulate to other professionals

www.cpmt.org/newsletter/

CPMT United Kingdom & Republic of Ireland (UK & RI) News

Submitted by Nihal Sinnadurai, Chapter Chair CPMT UK & RI
& Executive Chair ESTC-2008

In the UK & RI we have worked with a clear focus on the "customers" i.e. the members and engineers in our field who are interested in the activities we have planned over the years. To this end, we have worked with like-minded institutes in arranging conferences, seminars, tutorials and events in support of students. We have co-sponsored the many annual MicroTech events and Electronics Manufacturing Forums held in the UK.

The most constructive regional development which also benefits other Chapters in Region 8, is the collaboration agreement reached with IMAPS-Europe, whereby CPMT runs a biennial conference namely the Electronics System-Integration Technology Conference (ESTC-2008) in odd years, and IMAPS-Europe runs its European Microelectronics Packaging Conference (EMPC) biennially in the even years, with both being co-sponsored. This deal is now actively running and ESTC-2008 - to be held during 1-4 September 2008 at Greenwich, London - will be the first such collaborative CPMT Conference. CPMT UK&RI, which provided leadership as architect of the collaboration agreement, is in the heart of ESTC-2008.

We would like to see whole-hearted participation by Electronics Engineers and especially CPMT members in ESTC-2008.

ESTC-2008 will be held at Greenwich, the Prime Meridian and magnificent World Heritage and major maritime site on the banks of the River Thames in the great city that is London. The Conference and Exhibition will be hosted at the University of Greenwich in the buildings of the former Royal Naval College – which has a tremendous heritage: the Exhibition Hall will be immediately over the former palace of King Henry the Eighth, and the Queens House is where Sir Walter Raleigh placed his cloak over a puddle for Queen Elizabeth the First to step onto. Plenary sessions will be in the Great Painted Hall – providing a wonderful ambience for the technical presentations. The exhibition will be the quality event in microelectronics and micro-systems in Europe in 2008.

Greenwich, Prime Meridian and World Heritage Site

The Technical themes of ESTC-2008 are: • Advanced Packaging • Emerging Technologies • Manufacturing and Test Technology • Modelling, Simulation and Design • New Materials and Processes • Power Electronics • Technology & Reliability for Micro and Nano Systems • Assembly of Alternative Energy Sources • Optoelectronics • Electronics system-integration for healthcare.

There will be Special Sessions on:
• Greening the Blue Planet • Standards • Prognostics and Health Monitoring • Asia-Pacific Photovoltaics Developments • European Global Business Council

The Technical Committees are in place, the Call for Papers has been widely disseminated, invitations to exhibit have been sent to many companies globally and a brand new enduring website created. Please check out the website **www.estc.biz**. For General information contact: **info@estc.biz** or **sinnadurai@estc.biz**. For Exhibition and R&D Village bookings contact Carole Franks or Susanne Wolf at **intercomm@dial.pipex.com**.

Conference Reviews:

EDAPS 2007: A Workshop on Electrical Design of Advanced Packaging and Systems

Prof. Tzong-Lin Wu, National Taiwan University, Taipei, Taiwan

The 2007 EDAPS conference was held at National Taiwan University, Taipei, Taiwan from Dec. 15th to 18th, 2007. The conference was hosted by the Department of Electrical Engineering, Graduate Institute of Communication Engineering, and Center of Information and Electronics Technology, National Taiwan University, and was sponsored by the National Science Council, IEEE, IEICE, and leading companies in advanced packaging. The participants came from Canada, Hong Kong, Italy, Japan, Korea, Singapore, Taiwan, and the US (in alphabetical order). The number of attendees reached 271, including 27 invited speakers, which is a new record for EDAPS. Among the attendees, 49% are from academia and 51% from industry, which marks a great success in bridging academia and industry together.

The first day started with three tutorials on Signal Integrity, Power Integrity, and SiP Design, given by Mr. Moises Cases (IBM, USA), Prof. Madhavan Swaminathan (Georgia Tech, USA), and Prof. Joungho Kim (KAIST, Korea), respectively. Totally, 146 attendees signed in, including around 70 students and 60 engineers from local industry. On the second and third day, there were three featured keynotes, one luncheon talk, and twenty-three invited talks. The three talks were: "Global Paradigms, Models & Challenges" by Prof. Rao R. Tummala (Georgia Tech, USA), "3D Package Technology Integration" by Dr. Ho-Ming Tang (ASE Group, Taiwan), and "Meeting the Design Challenges Associate with SIP and IC/Package/PCB Co-Design" by Dr. Zoltan Cendes (Ansoft, USA). The luncheon talk was "Academic and Industrial Research: Using the IEEE's XPLORE Database" by Dr. Paul Wesling. The invited talks covered the hottest topics including chip/system level design, electromagnetic simulation, electro-thermal analysis, integrated passive devices, as well as efficient yet accurate modeling techniques. On the fourth day, the invited speakers took the Taiwan High-Speed-Rail train (300 Km/hr at its highest speed) to Kaohsiung to visit ASE groups, which is the largest provider in assembly and test in the world. The feedback to the EDAPS 2007 committee were very positive. Many partici-

pants would like to attend EDAPS again in the future and will recommend EDAPS to their colleagues.

The chairman of EDAPS 2007, Prof. Ruey-Beei Wu, on behalf of the executive committee, would like to thank all the attendees, especially Dr. Alina Deutsch and Prof. Madhavan Swaminathan, the TC-12 EDMS Committee co-Chairs of IEEE CMPT Society, for their kind support in every aspect, which made EDAPS 2007 a wonderful experience. Meanwhile, Prof. Joungho Kim assumes the chairmanship of EDAPS 2008, which will be held in Seoul, Korea from Dec. 10th to 12th, 2008. Regarding the EDAPS 2008 information, please visit **www.edaps2008.org** for details.

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Technical Committee Reports:

TC-1 News from 2007

TC-1: Technical Committee on Electrical Contacts, Connectors, and Cable

Submitted by Dr. Dave Palmer, IEEE Fellow

The scope of this Committee is to be the focal point within the IEEE CPMT Society for electrical contacts, electrical connectors, and interconnecting cable. Its membership consists of individuals having an interest in the research, development, manufacture, and utilization of electrical contacts and devices that contain them. The Committee holds regularly scheduled meetings and functions through the Holm Organization and through task forces having specific objectives. The Committee sponsors or supports conferences, publications, educational, standardization, and other activities.

The 2007 IEEE Holm Conference on Electrical Contacts was held in Pittsburgh, September 17-19. This was the 53rd Annual conference in North America where professionals presented and discussed the latest developments in the field of electric contacts. This year there were 130 attendees and this resulted in a very successful conference.

The technical program had 35 presented papers in 9 sessions, the Ragnar Holm Award Lecture and the Mort Antler Invited Lecture. Papers were presented on electric contacts in switches, relays and connectors, new contact materials and coatings, arc fundamentals, thermal models, finite element analysis and corrosion. A special session was organized on Arc Fault Circuit Interrupter (AFCI). This is a new NEC standard to be implemented in all new residential house constructions in 2008. More details of the program and abstracts can be found in our web site.

On Monday night (9/17), we also had a successful social event at the Pittsburgh Grand Concourse, a restored train station with perfect atmosphere for friendly discussions while dining. The annual Monday social event is becoming a tradition when the conference attendees get to chat more freely with their conference friends. We had 96 attending the dinner social.

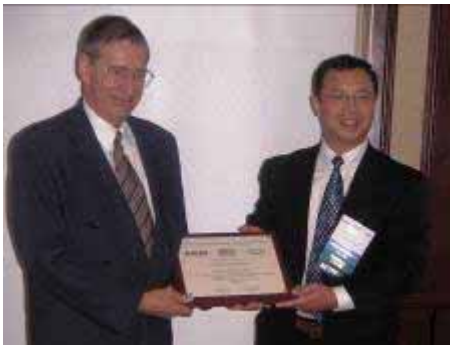
This year, the conference presented 3 awards:

a. The 2007 Ragnar Holm Scientific Achievement Award to Professor Ji Gao Zhang, Beijing University of Posts & Telecommunication, for his life time work on dust and electrical contact reliability, as well as his teaching contributions in China. He gave an award lecture "Effect of Dust Contamination on Electrical Contact Failure".
b. The 2007 Mort Antler Lecture Award to Professor Joachim Heberlein, University of Minnesota, who was the invited speaker to stimulate work on hot topics. His lecture was titled "The Characterization of the Dynamic Arc-Anode Interaction and Using Plasma Deposition of nanocomposites to Tailor Material Properties.
c. The 2006 IEEE Erle Shobert Prize Paper to Dr. John Shea, Eaton Corporation, for his paper "Glowing Contact Physics" being selected as the best out of 43 papers presented in the 2006 conference in Montreal.

TC-1 also runs a 3 day intensive course on electrical contacts bi-annually. The course has been very successful in teaching engineers the physics and practice of contact designs and selections. It is a favorite for switch, relay, circuit breaker, contactor, and connector engineers from automotive, power distribution and telecommunication fields. The 2006 course was held in Montreal and the 2008 course will be held in Orlando just before the Holm Conference.

The 2008 IEEE Holm Conference will be October 27-29 in Orlando. For more information on many special events organized by this committee such as annual IEEE Holm conference, conference presentation downloads, intensive course, international conference, CD-ROM library and link to other societies, please visit our web site at **www.ewh.ieee.org/soc/cpmt/tc1**.

Photo Gallery from 2007 IEEE Holm Conference ===>



Mort Antler Lecturer Prof. Heberlein and Tech. Comm. Chair Dr. Zhou

2007 Holm Award Prof. Zhang (L) & Conference Chair Dr. Shea (R)

2006 Prize paper Dr. Shea (L) & Prize Paper Chair Dr. Taylor (R)

ASTR 2007 Review

Submitted by Mark R. Chrusciel, ASTR Publicity Chair

The ASTR 2007 workshop on Accelerated Stress Testing and Reliability was recently held in the Washington DC area. This years theme was "Accelerated Life Testing, it's Roles, Challenges, Attributes, and Interaction with Qualification Testing".

Over the last few years, Accelerated Stress Testing (AST) has been embraced by an ever widening array of worldwide companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market. The purpose of the AST Workshop is to share ideas on better ways of accelerating and detecting hidden defects, flaws, and weaknesses in electronic and electro-mechanical hardware that would result in failures during usage. Feedback from this years conference was very positive.

Plans are being made for ASTR 2008 to be held in Portland, Oregon in October of 2008. Theme and call for papers to be issued in the spring. Visit the website (link)

ASTR 2007 Committee

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58th Electronic Components and Technology Conference (ECTC) Update

Submitted by Dr. Rajen Dias, Asst. Program Chair

The 58th ECTC that will be held at Disney's Contemporary Resort in Lake Buena Vista, Florida, USA May 27 to 30, 2008, has received 616 technical abstracts, a record number. The technical program will feature over 300 high quality technical papers, presented in 36 oral sessions, two poster sessions and a special student poster session. The papers cover a wide spectrum of topics: advanced packaging, interconnections, electronic components, materials, processing, assembly, manufacturing, optoelectronics, quality and reliability, modeling, simulation and emerging technology that focuses on nano-technology, biomedical and flexible electronics.

The technical program is complemented by 16 professional development courses, a plenary session, a panel discussion session and a CPMT seminar session. In addition, there is a technical exhibit corner where over 50 leading companies, primarily in the electronics components, materials, thermal and packaging fields exhibit their latest technologies and products. The conference allows ample opportunities to network and meet leading experts in the field.

For more information on 58 ECTC, please visit **www.ectc.net**

Workshop Reviews:

6th Future Directions in IC and Package Design (FDIP 2007) Workshop

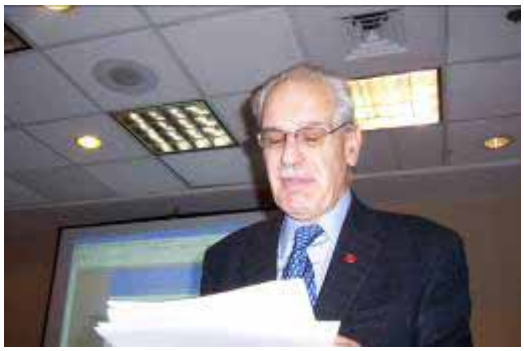
Organized by CPMT Technical Committee on Electrical Design, Modeling, and Simulation, TC-EDMS

October 28, 2007, Atlanta, Georgia

Submitted by Alina Deutsch, IBM T. J. Watson Research Center, Tel: 914-945-2858, email:deutsch@us.ibm.com, co-chair

Madhavan Swaminathan, Georgia Institute of Technology, email: madhavan.swaminathan@ece.gatech.edu, co-chair

This year's workshop was held on October 27, 2007, in Atlanta, Georgia. This was the sixth year for the meeting but it was still very well attended, with 60 participants. The workshop was divided into two sessions, namely System Design, and Power Distribution. The two sessions were chaired by George Katopis from IBM and Gregory Taylor from Intel. As in years past, the presenters were all invited distinguished experts in the field and this year's contributors gave excellent presentations.



George Katopis, IBM

Gregory Taylor, Intel

The System Design session was opened by **Dale Becker** from IBM who presented the talk "Signal Bandwidth for High Performance Computing". Dale defined a new system performance metric, the product of the number of bits in the off-chip signal bus and the data rate. Key issues he foresaw were the need for memory bandwidth increases, a factor of ten increase in Gbps/cm^2 due to increase in density of pins and data rate; power delivery and heat removal become more challenging; containing power distribution effective impedance and signal integrity in the presence of multiple power domains; self heating in I/O pins; importance of core noise in addition to Delta-I noise; ability to design advanced analog loss compensating circuits for drivers and receivers; and time and frequency domain analysis capability for jitter assessment for full channel. Dale saw processor clock frequencies leveling off, off-chip frequencies increasing as number of cores is go-

ing up, ASIC clock frequencies rapidly increasing. Designers need to use full-wave analysis for power distribution and via stub reflections, careful DC analysis to control electromigration, have good understanding of compensating receiver circuits, have good tools to perform optimal chip-package co-design and use common interfaces across companies to reduce cost per pin. Dale saw the cost per pair of differential I/O increasing by a factor of two when going from 3 Gbps to 10 Gbps.

Dale Becker, IBM

Prof. Tadahiro Kuroda from Keio University presented a very nice overview of 3D package interface methods, "Wireless Proximity Communications for 3D System Integration". He made a very compelling argument why inductive coupling is superior to capacitive and TSV (through silicon via) approaches. Inductive coupling has been successfully shown for 1000 I/O's with 1 Gbps data rate and 1 TBps total throughput and only 0.14 pJ per bit. Inductive coupling can be used through the silicon substrate even for thickness as high as 60um and thus multiple chips can be easily stacked without restriction on chip face orientation as found in capacitive coupling.

Capacitive coupling relies on a single metal layer while L-coupling inductors can utilize several on-chip layers and thus have higher efficiency. Prof. Kuroda indicated that this is a much lower energy solution (2 mW) than wire bonding (200 mW) or micro-bumping (20 mW) and still can have very high density of 1 mm^2/Tbps. TSV needs much higher real estate due to the use of ESD protection that is not needed by L-coupling. The resultant 3D stack is much thinner than when using TSV and has very high reliability of 10^{-13} BER. Alignment tolerances are not critical and the cost of L-coupling versus TSV development is much lower since no new technology is needed. L-coupling allows non-contact testing and AC coupling across various power levels. Extendability of this technology is gated by ability to thin the stacked chips and placement of the I/Os with respect to power mesh and density inside the on-chip wiring that could cause some interference. Time interleaving can be used for thicker chips or to increase effective I/O density.

Prof. Kuroda, Keio University

Professor Jayathi Murthy from Purdue University introduced the audience of electrical engineers to the modeling of thermal effects on-chip with her presentation "A Critical Assessment of the State of the Art in Multiscale Multiphysics Modeling of Microelectronics". She indicated that sub-micron thermal physics are generally not included in present day electro-thermal device simulations. When phonons' mean free path becomes comparable to transistor channel dimension, ballistic phonon effects become critical for hot-spot prediction. Thermal resistance of interfaces and surface physics are dominating as device sizes are dropping. Electro-thermal-mechanical analysis is becoming increasingly important but is currently not available. The solution she offered is to create compact models that account for local effects accurately that can be then included in CAD tools and allow to bridge from microscale to macroscale analysis. Such new tools are absolutely necessary as leakage may account for as much as 40% of total power dissipation. Sub-threshold leakage currents increase exponentially with temperature and can lead to thermal runaway. For every 10°C increase in temperature, a MOSFET's drive current decreases about 4% and interconnect delay increases approximately 5%. Because of all these penalties, electronics thermal management is emerging as a critical bottleneck that dictates the need for new tool development.

Prof. Murthy, Purdue University

Tawfik Arabi from Intel presented "Designing for Energy Efficient Mobile Platforms". He indicated that for laptops, Intel's goal is to reduce power by 10W between generations of products. Designers have made good progress in containing the CPU power which is 47% of total but then other factors such as voltage regulator, memory, power delivery are affecting the total power of the platform. A 10 W reduction can allow a 0.1 inch reduction in laptop thickness and Tawfik thought this was significant. He also noted that a 20% reduction in clock frequency leads to a 50%

drop in power consumption. The newer device technologies with metal gate and high *k* such as the 45 nm node show a reduction in f_{max} tolerance for the device. A large improvement in processor power reduction was obtained by introducing temperature gradient distribution across the die in the timing CAD tools. This was doable by partitioning the die into mega-blocks and then performing accurate modeling within the blocks and only global analysis at the chip level.

The remaining challenges are primarily at the platform level, such as the I/O power delivery sub-systems, I/O signaling, voltage regulators, that show impact for light load conditions, such as in idle state.

Dr. Tawfik Arabi, Intel

Prof. Swaminathan, GIT

Professor Madhavan Swaminathan from Georgia Institute of Technology presented "Modeling Challenges for Power Distribution Analysis". He traced the modeling activities from the early 1990's to today. He reviewed the various techniques used, how the simple effective impedance analysis of yesterday needs to be extended to a multi-scale chip-package co-design capability. He felt that low K material use results in increased electromigration exposure, especially at the interposer interface, managing coupling from high density digital circuits into the sensitive analog circuits is increasingly difficult, modeling of frequency dependent losses while predicting time-domain jitter needs new tool development. A new approach to solving the Courant condition was found at GIT by using Laguerre FDTD. This allows to easily handle scale ratios of $1{:}10^6$. Small 3D package vias show significant current density variation due to skin effect and proximity effect. Mobile platforms that use embedded passives encounter large vertical coupling through the partitioned power system. It was felt that many modeling tools are not addressing the issue of causality and this effects the timing prediction for fast signal propagation on long interconnects.

The last talk was given by the founder of Sigrity, **Prof. Jiayuan Fang**, "Power Delivery System Design Challenges and Explorations on How to Overcome Them". Prof. Fang felt that power distribution systems, PDS, modeling tools are now used by over 100 companies. There are still a lot of challenges, however. Most companies do not have design specifications for the power delivery systems. The designers cannot formulate the needed voltage fluctuations, the available chip current, the target impedance for PDS, the current switching conditions, the applicable frequency range. It is then hard to define the optimal location and number of power and ground vias, location and types of decoupling capacitors needed. This can lead to product failures or gross over-design with unnecessary cost.
Guidelines were given on how to establish design specifications for PDS, such as the use of a database storing previous generation product characteristics. New optimization facilities were also shown for best selection and placement of decaps to improve performance and reduce cost.

Prof. Fang, Sigrity

*****

2nd International Workshop on 3D System Integration Munich, Bermany

Submitted by Mr. Rolf Aschenbrenner, VP Conferences, IEEE CPMT Society

The 2nd International Workshop on 3D System Integration took place on 1-2 October 2007 at the Fraunhofer-Society, Munich, co-organized by IEEE CPMT. More than 90 engineers, scientists and entrepreneurs attended the 2-day workshop and discussed worldwide R&D activities, perspectives and challenges of 3D integration.

After the welcome and introduction by Peter Ramm, Fraunhofer Munich, the keynote address was given by Sitaram Arkalgud, director of SEMATECH (US), on "Paving the Roadmap For Through Silicon Vias". The first day continued focussing on Si-based technologies for 3D IC integration with excellent talks by speakers from ZyCube (Japan), STMicroelectronics (Italy) , EPFL (Switzerland), NXP (Netherlands), SINTEF (Norway), Semitool (US), IBM (Switzerland), CEA-Leti (France) and Fraunhofer IZM (Munich). After the opening talk of Robert Darveaux, Amkor (US), on "Developments of 3D Packaging" the second day´s talks

were given by speakers from AT&S (Austria), Techlead (US), Imbera (Finalnd), ASE (US), IMEC (Belgium), Schweizer Electronic (Switzerland), Panasonic (Japan) and Fraunhofer IZM (Berlin).

Picture: Speakers and chairs at the IEEE Workshop on 3D System Integration Munich 2007 (sitting right: Keynote speaker Dr. Sitaram Arkalgud (SEMATECH); row left and center, respectively: Chairman Dr. Peter Ramm and co-chair Rolf Aschenbrenner (Fraunhofer IZM))

2nd IEEE International Workshop On
Advances in Sensors and Interfaces
IWASI 2007

Held 26/27 June 2007 - Bari, Italy

IWASI is a sensors interfaces conference, aimed at bridging the gap between sensor devices and their integration with electronics using newly developed technologies. The workshop focus is on the development of the electronics around the sensors so that efficient sensors can create a system that can easily be placed in the home, the car, or on the human body to improve the quality of life.

The Workshop provides a forum for the exchange of ideas and results in critical areas of design for quality in deep submicron era. Focus areas: • Sensor interfaces • New materials and new technologies for sensors • Sensor modeling and design techniques • Sensors for space, nuclear and particle physics, biomedical, automotive, environmental and other applications • Optoelectronic and photonic sensors • MEMS and MOEMS-based sensors • Post-processing electronics • Noise reduction techniques in sensors interfaces • Testing techniques for sensors systems • Sensor networks.

Photos from the 2007 IWASI

Prof. Daniela De Venuto being interviewed (left) and with the Mayor of the City and the Chancellor of the Politecnico of Bari (below)

Please review the papers from the 2007 IWASI in IEEE's IEL/Xplore system:

ieeexplore.ieee.org/xpl/RecentCon.jsp?punumber=4419989

*****

2008 IEEE
Systems Packaging Japan Workshop

Hotel de YAMA, Hakone, Japan
January 28 - 30, 2008
www.ewh.ieee.org/soc/cpmt/tc14/
Submitted by Evan Davidson, Japanese Liaison for TCSP

Call for Papers and Invitation

The Systems Packaging Japan Committee cordially invites you to participate in the 2008 IEEE Systems Packaging Japan Workshop (2008 SPJW), which will be held during January 28-30, 2008 at the Hotel de YAMA, Hakone, Japan. This workshop is held every other year in Japan and 2008 SPJW will be the twelfth one since the first workshop in 1986. State-of-the-art technologies in all areas of systems packaging from personal systems to high performance systems will be covered. Attendees are expected to be specialists in the field and to actively participate in all discussions. We look forward to meeting many of you at Hakone.

Topics:

● IT Network Systems ● Digital Consumer Products & Mobile Information Systems ● High Performance Servers ● Advanced Packaging & Components ● Bio/Nano Technologies ● Environmental Aspects

For more information about the workshop, please feel free to contact Mr. Kishio Yokouchi, the Program Chair at:

Research & Development Group
Fujitsu Interconnect Technologies Ltd.,
E-mail: yokouchi.kishio@fict.fujitsu.co

PORTABLE 2008

Second IEEE International Interdisciplinary Intersociety Conference on

Portable Information Devices (PIDs)

Jyväskyla, Finland August 10 – 14, 2008

Portable Information Devices (PIDs) have revolutionized our lives including the way we work, play, and stay informed. In our decade PIDs have become essential to everyday life and business culture. Emergence of PIDs has vastly enhanced such basic activities as like reading, taking notes, enjoying music, crunching numbers, watching videos, and keeping up with news and sports on the go. Today's PIDs include: mobile phones, palm-sized personal digital assistants, medical devices, intelligent clothing, iPODs, and many more. Wearable computers might become PIDs in the foreseeable future. Some devices contain built-in organizers for to-do and shopping lists, scheduling appointments, phone numbers, address books, customer contacts, and games. Hardware and software, both electrical and non-electrical (e.g., materials, mechanical, thermal, environmental, etc.), must be designed to be reliable, user-friendly, lightweight, and durable.

PORTABLE 2008 brings together 150-200 electrical, materials, mechanical, optical, reliability, industrial and manufacturing engineers and business leaders involved or interested in various types of PIDs, to address and discuss the state-of-the-art, challenges, attributes and pitfalls in PID-related areas of engineering and applied science, with an emphasis on the interaction of the hardware and software in the PIDs, as well as on their functional and physical (mechanical) performance, reliability and durability.

PORTABLE 2008 is sponsored by the IEEE Vehicular Technology Society (VTS), IEEE Electron Devices Society (EDS), Components Packaging and Manufacturing Technology Society (CPMT), and IEEE Systems, Man, and Cybernetics Society (SMCS). It is technically co-sponsored by the Nokia Corp., University of California at Santa Cruz (UCSC), the University of Maryland at College Park (UMD), the IEEE Engineering in Medicine and Biology Society (EMBS) and IEEE Women in Engineering Group (WIE).

Website: **www.portable2008.com**

IEEE

IEEE Semiconductor Wafer Test Workshop

June 8-11, 2008 Paradise Point Resort San Diego, CA USA

The IEEE **SW Test Workshop** is the only IEEE CPMT Society event that focuses on all the aspects associated with microelectronic wafer and die-level testing. The conference has a mixture of manufacturer and vendor presentations. It is not a sales show, nor an academic or theoretical conference. It is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas. There is a relaxed atmosphere with social activities and plenty of time for informal discussion and networking.

Conference registration includes all meals, refreshments, social activities, the technical program and exhibit attendance, as well as the printed Proceedings distributed at the Workshop.

Technical sessions include:

- New probe card and contactor technologies
- Challenges of 300-mm wafer probing
- Monitoring and reduction of chip I/O pad damage
- Area array and C4 solder bump probing
- Parallel, multi-site probing
- Probe Card PCB Characterization
- Productivity improvements for high volume production
- Probe data collection, analysis, and management
- Addressing unique probing requirements: ● Copper I/O pads ● RF and microwave ● Mixed signal, low noise, and parametric ● Low-k dielectric and Probe Over Active Circuitry ● Probing for Known Good Die ● High power devices

More information, and to register:

www.swtest.org

ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE

May 27th – May 30th, 2008
Orlando, Florida USA

Advance Program: see the website **www.ectc.net**
Plan **now** to attend!

Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS

- DTIP 2008
09-11 April 2008
Boscolo Plaza Hotel Nice, France
Website: cmp.imag.fr/conferences/dtip2008/

CAD, Design and Test
Chair: Marc DESMULLIEZ, Heriot-Watt Univ., Edinburgh, UK; Co-chair: Tarik BOUROUINA, ESIEE, Paris, France

Microfabrication, Integration and Packaging
Chair: Gou-Jen WANG, National ChungHsing Univ., Taiwan; Co-chair: Victor M. BRIGHT, Univ. of Colorado at Boulder, USA

PLENARY INVITED TALKS

* **Integrative MEMS/NEMS Technology for Micro and Nano Systems** Reza GHODSSI, Univ. of Maryland, USA
Materials technology and process integration are the key enabling tools for novel advances in MEMS/NEMS for future biological and chemical micro and nano systems applications. The talk presents an overview of various building block materials and process technologies.

* **MEMS-Enabled Smart Autonomous Systems** Chris Van HOOF, IMEC, Leuven, Belgium
A smart environment will be enabled by miniaturized sensor systems. MEMS technology is providing both sensing and actuating solutions and energy scavenging solutions. State-of-the-art and IMEC solutions will be presented.

PANEL on **Success Stories in MEMS-based Systems**
MEMS make it possible for systems of all kinds to be smaller, faster, more energy-efficient and less expensive. The panel will be the occasion to present complete innovative systems making use of micro- and nanotechnologies, integration, interconnection, and packaging to become major business success stories in various applications and market segments.
The panel is chaired by Anne-Françoise PELÉ, EETimes

SPECIAL SESSIONS

* **Micro Power Generators and Micro Energy Sources** The objective of this special session on Micro Power Generators is to catalyze innovation in microtechnologies for power generation and energy conversion applications by providing researchers with a forum for discussing latest research results. This special session is organized by Skandar BASROUR, TIMA, Grenoble, France.

* **3D TSVs** Through-Silicon Vias are the new favourites for ultra-high density system integration. While driven mostly be the memory industry, the technology is also suitable for complex systems and MEMS devices. This session showcases technological developments that enable the technology as well as application scenarios and perspectives for 3D system integration. This special session is organized by Erik JUNG, IZM, Berlin, Germany.

* **Bio-MEMS** The Special session on bio-MEMS puts together papers on both theoretical analysis and on practical applications of MEMS and NEMS in biomedicine and biochemistry. General topics of interest include design, characterization, modeling, and fabrication of biomedical devices, miniaturized analytic devices, dynamics of fluids in micro channels, Tissue engineering, and others. This special session is organized by Gou-Jen WANG, National ChungHsing Univ., Taiwan.

REGULAR SESSIONS

Reliability and Failure Analysis: 3 papers
Assembly and Packaging: 3 papers
Devices and Components: 16 papers
Structured Design Methodologies and CAD: 6 papers
Multiphysics Modeling and Simulation: 4 papers
Integrated Processes: 4 papers
Characterization: 4 papers
Manufacturing: 4 papers
19 posters, to be introduced by a 3 minutes oral talk.

10th Year Anniversary Celebration!

CALL FOR PAPERS

BIGGER Event! 4 Days Conference

ABOUT EPTC

The 10th Electronics Packaging Technology Conference (EPTC 2008) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter, sponsored by IEEE CPMT Society.

EPTC 2008 is a 4-day event in conjunction with 10th year conference anniversary celebration. It will feature technical sessions, short courses/forums, exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- Advanced Packaging & Emerging Technologies: *Wafer level packaging, 3D integration, embedded passives & actives on substrates, high power modules, high pin count flip chip packaging, RF-ID, SiP and other system integration technologies. Packaging solutions for MEMS, Bio-electronics, Automotive electronics, optoelectronics, organic and printable electronics.*
- Interconnection Technologies: *Gold and copper wire bonding and flip chip (eutectic/lead-free solders) on standard and copper low-k wafers, solder replacement flip chip (ICP, ACP, ACF, NCP), under bump metallurgy, 3D and through Si via connections, microvia and build-up technologies, fine pitch interconnects, nano interconnects.*
- Manufacturing Technologies: *Sustainable volume production of advanced packages and emerging technologies. New manufacturing technologies focusing on incorporating rapid product changes, cost, yield improvement, electrical/mechanical and environmental performance.*
- Materials & Processes: *Advancements in adhesives, encapsulants, underfills, solder alloys, ROHS compliant materials, flexible dielectrics, ceramics, composites, thin film processes on laminates, nano-materials and assembly processes, advanced material characterization techniques.*
- Electrical Modeling & Signal Integrity: *Modeling simulation & measurement for coupling, signal Integrity, power integrity & decoupling scheme analysis reflection, switching noise, EMI/EMC analysis on package & subsystems, RF modules, time & frequency domain measurements for advanced modules.*
- Thermal Characterization & Cooling Solutions: *Modeling & simulation methodology for thermal characterization of advanced packaging, modules & systems. Novel thermal management solutions. Enhanced air & liquid cooling techniques, Hot-spot management.*
- Mechanical Modeling & Structural Integrity: *Thermo-mechanical modeling at package, board & system levels. Modeling of delamination, moisture diffusion, hygrostress, thermal cycling, drop impact, bend, vibration, solder joint reliability and life prediction, measurement of material & interface properties, experimental verification.*
- Quality & Reliability: *Component, board and system level reliability assessment, interfacial adhesion, accelerated testing and models, advances in reliability test methods and failure analysis.*

Important Dates

15th May 2008	**Submission of abstract**
30th June 2008	**Notification of Acceptance**
30th August 2008	**Submission of manuscript**

Abstract and Paper Submission

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories for abstract review. All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 15th May 2008. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Special gift (webcam) will be given to the first 20 submitted abstracts which are subsequently accepted and published. Authors will be notified of paper acceptance and publication instruction by 30th June 2008. The final manuscript for publication in the conference proceedings is due by 30th August 2008. Selected papers will be published in IEEE/CPMT journals.

Outstanding Technical Papers

The conference proceedings is an official IEEE publication. Author(s) of Outstanding Technical Paper(s) and Best Student Paper will receive an award at the next conference.

Call for Short Courses

The conference program includes half and full-day short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings. Proposals for short courses can be submitted to techchair@eptc-ieee.net.

Call for Exhibition / Sponsorship

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. Potential exhibitors and sponsors may email secretariat@eptc-ieee.net for details.

Organized by

IEEE Reliability/CPMT/ED Singapore Chapter

General Chair	Technical Chair
Dr. Tong Yan TEE Amkor Technology, Singapore Email: tytee@amkor.com Tel : +65-62113403	**Dr. Teck Kheng LEE** Institute of Technical Education, Singapore Email : techchair@eptc-ieee.net Tel: +65-65805007

Sponsored by

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Conference information & contacts: Website: http://www.eptc-ieee.net Email: secretariat@eptc-ieee.net

12th IEEE WORKSHOP ON

SIGNAL PROPAGATION ON INTERCONNECTS

May 12-15, 2008 Avignon, France

Sponsored by
the IEEE Computer Society - Test Technology Technical Council (TTTC) and by
the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society

SPI is a forum for the latest research and developments in the field of interconnect modeling, simulation and measurement at chip, board, and package level. The event also brings together developers and researchers from industry and academia in order to encourage cooperation.

For Advance Program (posted March 17) and registration information:

www.univ-brest.fr/spi

10th Academic Conference on Electronic Packaging Education

Budapest, Hungary 7-8th May 2008

Before and jointly with ISSE 2008 (at right), the International Academic Conference on Electronic Packaging Education and Training will take place. The aim of the Academic Conference is to catalyze education innovations by bringing together faculty from around the globe. Academics in the field of electronics packaging education are invited from the USA, Far East and Europe to exchange their knowledge and experience.

General Chair:
Rao R. Tummala, Pettit Chair Professor & Director, Georgia Tech, Packaging Research Center, USA

European Chair:
Klaus Jürgen Wolter, Professor & Director, Dresden University of Technology, Germany

Conference Chair:
Gábor Harsányi, Professor & Head of Department, BME-ETT, Budapest, Hungary

We invite you to request the Advance Program from the Gábor Harsányi at **harsanyi@ett.bme.hu**

Please visit:

www.ett.bme.hu/isse/isse2008/

EuroSimE

Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems

April 20-23, 2008 Freiburg, Germany

EuroSimE addreses the results of both fundamental research and industrial application for thermal and mechanical solutions of (micro)-electronics, focusing on advanced simulation and experiments/technologies.
The aims of this conference are to

- Promote further development and application of advanced simulation methodology and experiment technology for electronic industry
- Disseminate competence and results obtained from relevant research projects
- Promote the integration and co-operation of competencies at international level
- Strengthen communication and co-operation between industry, universities, and research institutes

See the Advance Program now:

www.eurosime.org

31st International Spring Seminar on Electronics Technology (ISSE 2008)

May 7-11, 2008 Budapest, Hungary

Theme: Reliability and Life-time Prediction

ISSE is the premier European forum for the exchange of information between senior and young scientists from academic communities and electronic industries from around the world on topics related to their experimental and theoretical work in the very wide-spread field of electronics and microelectronics technology and packaging. Based on a unique combination of oral and poster presentations as well as individual meetings, professors and students, senior and junior researchers can come together to discuss scientific and educational topics and organize international cooperation in a convenient atmosphere during three conference days. It is our pleasure to encourage you to participate in ISSE 2008, organized in Budapest, the beautiful capital of Hungary.

www.ett.bme.hu/isse/isse2008/

ITherm 2008

May 28 - 31, 2008
Orlando, Florida, USA

ITherm 2008 is an international conference for scientific and engineering exploration of **thermal, thermomechanical and emerging technology issues associated with electronic devices, packages and systems.** ITherm 2008 will be held along with the 58th Electronic Components and Technology Conference (ECTC 2008 - **www.ectc.net**), the premier electronics packaging conference. In addition to paper and poster presentations and vendor exhibits, ITherm 2008 will include panel discussions, keynote lectures by prominent speakers, and professional short courses.

Thermal Management:
• Thermal Vias, Heat Spreaders and Thermal Interface Materials
• Advances in Compact Air Movers
• Single Phase Liquid Cooling
• Novel Phase Change Cooling Techniques
• Microfabricated Thermal Management Devices and Systems
• Thermal and Energy Management in Data Centers
• Advances in Experimental Characterization

Mechanics:
• Modeling and Simulation at Package, Board, and System Levels
• Failure Mechanics and Damage Modeling
• Experimental Techniques
• Material Interfaces: Characterization and Simulation

Emerging Technologies:
• Sensors
• Nanotechnology
• Micro-Fluidics
• Fiber-Optics Interconnect Systems
• MEMS: Device and Package Level Reliability Issues

Visit our website for the complete program:

www.ithermconference.org

IEEE

Polytronic '08

7th International IEEE Conference on

Polymers and Adhesives in Microelectronics and Photonics

Garmish-Partenkirchen, Germany 17-22 August, 2008

Please join researchers, engineers and scientists from around the world in mid-August 2008 to share knowledge and experience in Polymeric Materials for Microelectronic & Photonic Applications (POLY), Adhesives in Electronics, and Polymeric Electronics Packaging (PEP). The program will include keynote, invited and contributed presentations, as well as panel discussions. There are eight half-day tutorials and an IEEE Pavilion featuring technology exhibits and demonstrations.

For the Program and registration details, visit:

www.polytronic2008.com

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For more details:

www.cpmt.org/trans/

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Access papers from the 2007 ECTC, IWASI, EPTC and IEMT:

Visit **ieeexplore.ieee.org** and download them

Purchase the CD-ROM at

www.cpmt.org/proceedings

Call for Papers

Transactions on Electronics Packaging Manufacturing

Special Call for Manuscripts

The IEEE Transactions on Electronics Packaging Manufacturing (T-EPM) is issuing a **Special Call for Manuscripts on 3-D Electronics**. This topic area encompasses a wide range of 3-D manufacturing technologies from stacking die, to stacking packages to stacking wafers. The objective of this Special Section of T-EPM is to collect in one place the most significant archival work in 3-D electronics. To be considered for inclusion in the Special Section, please submit your manuscript **by May 15, 2007**.

Correspondence to Wayne Johnson, Editor in Chief, at **johnson@eng.auburn.edu**

General Call for Manuscripts

The IEEE Transactions on Electronics Packaging Manufacturing (T-EPM) would like to solicit previously unpublished manuscripts for review and possible publication. The focus of T-EPM is on the **manufacture of electronics parts and assemblies**, with broad coverage of **design, factory modeling, assembly methods, quality, product robustness, and design-for-environment. Lead free electronics** has been a recent focus of T-EPM.

Manuscripts may be submitted at:

mc.manuscriptcentral.com/cpmt-trans-ieee

Select "Transactions of Electronics Packaging Manufacturing"

Joint International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)

Call for Papers **July 28 – 31, 2008** **Shanghai, China**

During the last decade, both the International Conference on Electronic Packaging Technology (ICEPT), organized by the China Electronic Packaging Society, Chinese Institute of Electronics (CIE-CEPS), and the International Symposium on High Density Packaging (HDP), organized by Shanghai University, have provided a great technical platform for both researchers both abroad and domestic, scholars and researchers from academia and industries to exchange ideas in new developments in electronics packaging. It has been decided, by IEEE-CPMT and CIE-CEPS, that ICEPT and HDP be merged as the **International Conference on Electronic Packaging Technology & High Density Packaging** (ICEPT-HDP) this year in order to meet the requirements of the rapidly growing packaging industry in China. The ICEPT-HDP 2008 is a 4-day event which will be held from July 28 to July 31 of 2008 in Shanghai, China. The conference will feature short courses, keynotes and technical sessions to widely cover the technological developments in all the areas of electronics packaging.

General Chair:
Prof. Keyun BI, China Electronic Packaging Society
Technical Chair:
Dr. Tom Chung, ASTRI
Organizing Chair:
Prof. Xiaojing WU, Fudan University of China
Co-chairs:
Willian T. Chen, President of IEEE-CPMT
Johan LIU, Professor, Shanghai University

IMPORTANT DATES

April 11, 2008 – Submission of Abstract
April 25, 2008 – Notification of Acceptance
June 20, 2008 – Submission of Manuscript

Further information, and full Call for Papers:

Conference Contact: **icept2008@fudan.edu.cn**

Conference Website: **www.icept.org**

1ST ANNOUNCEMENT AND CALL FOR PAPERS

IEMT 2008

33rd International Electronics Manufacturing Technology Symposium

4th-6th November, 2008 Penang, Malaysia

ABOUT IEMT

The 33rd International Electronics Manufacturing Technology Symposium (IEMT 2008) is an international event organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from CPMT Santa Clara Chapter and the CPMT Society. IEMT 2008 will feature short courses, technical sessions, and exhibitions. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation. IEMT 2008 is an international forum, providing opportunities to network and meet leading experts. Since the late 1980's, IEMT has gained a reputation as a premier electronics materials and packaging conference and is well attended by experts in the field of manufacturing technology from all over the world.

CONFERENCE TOPICS

The topics of interests are specific to electronics packaging, electronics materials, electronics manufacturing technology and reliability issues. Extended abstracts are being sought from, but not limited to, the following areas:

- Emerging Packaging Technologies
- Advanced Packaging
- Interconnection Technologies
- Manufacturing Technologies
- Surface Mount Technology
- IC Testing Technology
- Materials & Processes
- MEMS Packaging
- Electrical Modeling & Signal Integrity
- Thermal Characterization & Cooling Solutions
- Mechanical Modeling & Structural Integrity
- Quality and Reliability
- Chip-Scale Packaging/Flip Chip
- Wafer Fabrication Manufacturing

IMPORTANT DATES

Submission of Abstract	**15th April 2008**
Notification of Acceptance	20th May 2008
Submission of Manuscript	20th July 2008

ABSTRACT AND PAPER SUBMISSION

Extended abstracts are invited to describe original and unpublished work. They should be about 500 words stating clearly the purpose, methodology, results, and conclusions of the work. Key references to prior publications and how the work enhances the existing knowledge should be included in the extended abstract. Authors are requested to designate appropriate areas for the purpose of abstract review. All submissions must be in English and should be made via electronic mail to conference secretariat. Author may send their abstract either in MS Word or AdobeAcrobat© PDF format with only one single file for each submission.

The abstracts must be sent to the secretariat via email by **15th April, 2008**. Authors are requested to include their affiliation, mailing address, telephone and fax numbers, and e-mail addresses. Authors will be notified of paper acceptance and instruction for preparing final papers by **20th May 2008**. The final manuscript for publication in the conference proceedings is due by **20th July 2008**.

EXHIBITION

A tabletop exhibition from suppliers of materials, equipment, components, software, and service providers of electronics industries will also be held at the venue of the conference. Potential exhibitors may email to the conference secretariat.

KEYNOTES AND SHORT COURSES

The conference will have attractive keynotes and short courses on the latest manufacturing technology and advanced packaging from experts in the field. Details will be posted on conference website and subsequent mailings.

BEST PAPER AWARDS

Conference best paper, student best paper and best poster paper will be awarded to outstanding papers at the end of the conference. The awards will be given to the selected papers in the form of certificate and cash. Participants will also be taken to a short tour around the beautiful island of Penang and enjoy the varieties of Malaysian food and cultural shows.

Full Information: **www.cpmt.org/iemt**

Attend the 58th Electronic Components and Technology Conference
May 27 - 30, 2008 Orlando, FL USA

Our industry's premiere event!

Download the Advance Program from the website:

www.ectc.net

Visit us on our website: www.estc.biz

We invite participation by all engineers (and especially CPMT members) in ESTC-2008.

We have had 263 abstract submissions so far (March 5), plus those for the special sessions. The adjudication process will be just about complete by the end of March. 13 Short Course submissions have been received and Exhibition bookings are coming in. The Conference will have 6 parallel sessions, including Special Sessions, and more than 500 international attendees.
Now is the time for companies to take the opportunity to book a valuable exhibition slot (**www.estc.biz/call_for_exhibitors**). You can also gain a place in the event publicity and programmes by sponsoring segments of ESTC-2008 (email: **sinnadurai@estc.biz**)

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