Components, Packaging, and Manufacturing Technology Society Newsletter

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CPMT

The Global Society for Microelectronics Systems Packaging

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www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

President's Column…..

Dr. William T. Chen
IEEE Fellow
President, IEEE CPMT Society
Santa Clara, CA, USA
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Greetings!!!

CPMT Society Review

As many of you know, the CPMT Society is one of the 38 Technical Societies in IEEE. The activities of the Technical Societies come under the jurisdiction of the IEEE Technical Activities Board (TAB) where representatives from all the Societies come together to work on areas of common interest.

One of the functions of TAB is to have an in-depth review of each of the 38 Societies every five years. The stated purpose of the Review Process is: to listen, learn, discuss and comment with a view to helping all the Societies and Councils exchange practices to better serve their members and the profession. The TAB Society Review Committee (SRC) is composed of members with years of experience as Society volunteer leaders.

The CPMT Society was first reviewed in 1997 (the Society Review Process began in the 1990's) and again in 2002.

CPMT was originally scheduled for review in November 2007. This review was postponed to February 2008 to allow for revisions to and updates of the Society Review process. We were anxious for this review because we strongly feel that the review process provides for a rigorous critical examination by our own peers in the IEEE Technical Society Community.

How did this Society Review process work? Last December a self-review questionnaire was sent to CPMT which covered every operational aspect of the CPMT Society, including Vision, Mission, membership, chapters, finance, conferences, education, publications, awards, constitution, and many others.. Marsha Tickman, CPMT Executive Director, and myself organized a team from among the Vice Presidents and Strategic Directors to respond to this questionnaire and compile the statistics and data required by the Society Review Committee. The completed document was submitted to the SRC by mid January, and on February 14th, Valentines Day 2008, we had a formal review session with members of the SRC during the IEEE Board Series in Louisville, Kentucky.

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Cartoon of the Month:

… By Dave Palmer

IEEE CPMT Society Extends a Hearty Welcome to Dr. Wayne Johnson, Professor at Auburn University, as the newly elected Vice President for Publications for the IEEE CPMT Society. In this role, Dr. Johnson will be responsible for the society's transactions and newsletter. Dr. Johnson is suceding Mr. Paul Wesling who has served as the society Vice President for Publications for more than twenty five years.

… By Vasu Atluri

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Chapters and Student Branches

Refer to **www.cpmt.org** for CPMT Society Chapters and Student Branches list

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2008 Deadlines for Submitting Articles:
February 25th, 2008 **May 25th, 2008**
August 25th, 2008 **November 25th, 2008**
Only Articles Sent to nsltr-input@cpmt.org will be included in the newsletter
Members-only Web (www.cpmt.org/mem/)
UserName: [available to Members --
Password: join CPMT!]

President's Column (Continued from Page 1)

The results of the meeting were then written up by a member of the SRC and returned to CPMT for final comment. Any comments from CPMT are included in the document which then goes forward to TAB for final approval.

We expect that the formal review process will be completed in the next couple of months. Has the SRC review process been worthwhile? While we are looking forward to the formal report, we have found the review process itself to be very much worthwhile. The review process provided us with an opportunity to give a thoughtful look of our society: its mission, vision, value propositions and operations. The review process itself allowed us to look at ourselves with all our strengths and weaknesses. To quote Paul Keating, "nothing is more important to a country than the way it thinks about itself." To paraphrase this quote in the context of the IEEE/CPMT society, how do we think about the CPMT Society? In this column we had talked about the various CPMT value propositions: membership and chapters, conferences, publications, technical committees, awards and recognitions, education and others. The world is continuously changing. Our industry, our technology and our profession are changing, perhaps, at a faster pace. The Society Review gave us the opportunity to make a critical self examination. How do we think about ourselves? Are we the CPMT Society that we want to be?

Your comments are welcome.

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CPMT Society News:

Notification of Proposed Changes to CPMT Society Constitution and Bylaws

Submitted by Ms. Marsha Tickman, Executive Director, IEEE CPMT Society

The IEEE Technical Activities Board approved the required incorporation of several items into Society and Council Governing Documents, in order to be in compliance with IEEE Governance Documents.

The key issues include: to define a quorum; action of the governing body - with or without a meeting (e.g., e-mail voting); voting rights of the governing body's presiding officer; nominations and appointments committee operating requirements; and nominations and petition signature requirements.

The changes (shown below), have been approved by the CPMT Board of Governors and the IEEE Technical Activities Board. They are now presented to CPMT members as required.

Amendments to the Constitution (Article VII only, below) will go into effect unless 40 or more Society members object in writing within 30 days of publication to Society Members. Amendments to the Bylaws go into effect following approval by the CPMT Board of Governors and the IEEE Executive Director.

If you wish to register objection to the proposed amendment to Constitution Article VII, please send the objection by e-mail, fax or hard copy by no later than 1 May to:

Marsha Tickman
IEEE CPMT Executive Office
445 Hoes Lane
Piscataway, NJ 08854 USA
m.tickman@ieee.org
fax: 1 732 465 6435

Deletions = ~~strike-through~~

Additions = <u>underline</u>

1. Quorum; action of governing body; voting rights of the governing body's presiding officer:

Proposed Action and rationale:

Delete sections with strike-through from Constitution and insert (with appropriate revisions in accordance with "must haves") in Bylaws, as per format of respective IEEE governing documents.

Add sections to Bylaws as required for compliance.

Items in parentheses, labeled as "clarification" are provided as explanation and will not appear as part of final document.

Constitution

Article VII Meetings

Section l. The Society may hold meetings, conferences, symposia, or conventions either alone or in cooperation with Sectional, Regional, or other Convention Committees of the IEEE or other technical organizations, subject to IEEE rules and regulations. The Society should sponsor at least one technical conference of international scope each year.

Section 2. The BOG shall hold at least two meetings each year, one of which shall be designated the Annual Meeting at a time specified in the Bylaws. Other meetings of the BOG shall be held at such times as are found necessary and/or convenient. Special meetings of the BOG may be called by the President of the Society at his own discretion or upon request f three other members of the BOG with at least 30 days notice.

~~**Section 3.** A quorum of the BoG shall consist of at least 50% of the Elected Members At Large and at least 50% of the total BoG members with Complete Voting Rights.~~

~~**Section 4.** A majority vote of those elected members and "ex-officio with limited vote" members of BOG attending a meeting in which a quorum is present shall be necessary for the approval of actions except as otherwise provided in the Bylaws. If the issue requires a decision by complete voting rights individuals only, then only a majority of attendees with these rights is needed.~~

~~**Section 5.** Business of the BOG may be handled by correspondence, telephone, or any standard business communication medium as appropriate in the opinion of the officer concerned. When such business involves actions not having the prior approval of the BOG, or is outside its normal policy, approval by majority vote is necessary, unless otherwise provided. Telephone acts are to be confirmed promptly in writing.~~

Bylaws

10. ~~Society Business~~ Actions of Board of Governors and Committees thereof: The President and other officers shall conduct Society affairs subject to the Constitution Articles I and VII, these Bylaws, and the advice and consent of the BOG. No BOG meetings shall be held for the purpose of transacting business unless each member shall have been sent notice of the time and place of such meeting at least 30 days in advance of the meeting.

~~10.1 No BOG meetings shall be held for the purpose of transacting business unless each member shall have been sent at least 30 days notice of the time and place of such meeting. Any voting member of the BoG unable to attend a meeting may submit a written or email proxy to the Secretary, President, or Executive Director in advance of the meeting giving notice of their intended vote on matters to come before the BoG.~~

~~10.2 If less than a quorum physically attend or virtually attend (phone, video, internet) a duly called meeting, tentative actions may be taken which will become effective upon subsequent written ratification by other members needed to achieve quorum. Minutes of such meeting shall be expeditiously mailed by the Executive Director to each BOG member.~~

10.1 A quorum of the BoG shall consist of a majority of the total BoG members with Complete Voting Rights and include at least 50% of the elected Members-At-Large.

10.2. A majority vote of those elected members and "ex-officio with limited vote" members of BOG attending a meeting in which a quorum is present shall be necessary for the approval of actions except as otherwise provided in the Bylaws. If the issue requires a decision by complete voting rights individuals only, then only a majority of attendees with these rights is needed.

10.3 The BOG or any committee thereof may meet and act upon the vote of its members by any means of telecommunication. The normal voting requirements shall apply when action is taken by means of telecommunications equipment allowing all persons participating in the meeting to hear each other at the same time. 10.4 The BOG or any committee thereof may take action without a meeting if applicable (e.g. email voting). An affirmative vote of a majority of **all** the voting members of the BOG or any committee thereof shall be required to approve the action. The results of the vote shall be confirmed promptly in writing or by electronic transmission. The writings and/or electronic transmissions shall be filed with the minutes of the BOG or any committee thereof. "Electronic transmission" means any form of electronic communication, such as e-mail, not directly involving the physical transmission of paper, that creates a record that may be retained, retrieved and reviewed by a recipient thereof, and that may be directly reproduced in paper form by such a recipient. *(Clarification: When the Governing Body or any of its committees takes any kind of action such as email voting or mail balloting, without a formal meeting, a minimum of a majority of all of the body's voting members is required to pass the motion/action. For example, if there are 20 voting members of the body, the vote will pass if at least 11 or more vote affirmatively. All 20 voting members are not required to vote in order for the motion to pass; however all 20 members must be sent the email vote and given the opportunity to cast their vote).*

10.5 Voting. Individuals holding more than one position on the BOG or any committee thereof, shall be limited to one vote on each matter being considered by the BOG or committee.

10.6 Proxy voting is not allowed.

10.7.The presiding officer of the BOG shall have no vote on the BOG except if the vote is by secret ballot or unless the Chair's vote can change the outcome of the vote.

10.8 An appropriate order of business at an Annual Meeting of the BOG shall be:

(a) Roll call (b) Ratification of Minutes of previous meeting (c) Reading of report on business transacted other than at meeting (d) Report of Communications (e) Reports of Officers (f) Reports of all Committees (g) Unfinished Business (h) New Business (i) Elections, if not otherwise provided for (j) Adjournment

10.9 All Chapter and Committee Chairpersons shall be invited to BOG Meetings, plus other persons at the discretion of the President.

10.10 Technical and Standing Committee Chairpersons are appointed annually and may be reappointed by the President with the advice and consent of the BOG. They shall be ex-officio members of BOG.

2. Nominations and Appointments Committee operating requirements; nominations and petition signature requirements:

Proposed Action and rationale:

Add sections to Bylaws as required for compliance.

Bylaws

4. Nomination and Election of the Members at Large: The geographic composition of BoG Members-At-Large will reflect the geographic composition of Society membership.

4.1 The Nominating Committee shall be reconstituted and instructed by the President on or before the Spring BOG Meeting of each year. It shall have a chairperson and four or more members of the Society, at least one of whom shall be a member of the BOG.

(a) The Chair of the Nominating Committee shall be the immediate past chair of the BOG. In the event of the incapacity or conflict of interest of the Chair, the most recent Past Chair of the Nominating Committee available shall be the Chair of the Nominating Committee. With extenuating circumstances, a different individual may be appointed to this position.)

(b) Chairs shall not be eligible to be elected to the BoG during their term of service.

(c) At least two-thirds of the voting members of the Nominating Committee shall be elected or appointed by the BoG.

(d) A member of a Nominating Committee may be nominated and run for a position for which such member's respective Nominating Committee is responsible for making nominations only on the following conditions: (i) the nomination is not made by a member of the same Nominating Committee and (ii) the member resigns from the Nominating Committee prior to its first meeting of the year in which the nomination shall be made.

4.2 Annually, prior to formulating the slate of candidates, the Nominating Committee, using IEEE Region definitions and Society membership statistics as of 31 December of the preceding year, will determine the proportion of Society members in each of

the following Regions/grouping of Regions: 1-6 (US), 7 (Canada), 8 (Europe, Africa, Middle East), 9 (Central and South America), 10 (Asia, Pacific). Any Region/grouping of Regions determined to have at least 10% of CPMT total members will have the proportional number of Member-at-Large positions designated to it for representation on the BoG. The slate of candidates for each year's election will be constructed to ensure that the resulting total of newly elected Members-at-Large plus continuing Members-at-Large has the proper proportion of representatives from each Region/grouping of Regions.

4.3 Candidates will be solicited and selected by the Nominating Committee from among members of the respective Regions/grouping of Regions, by a process that ensures input from Society volunteers in the respective Regions/grouping of Regions, as well as from members of the BOG, and chairpersons of all other organizational entities of the Society. The slate will contain at least 1.5 candidates for each forthcoming vacancy.

4.4 Society members in each Region/grouping of Regions with designated BoG positions will vote for their Region/grouping of Regions' respective positions only. That is, members in Region 8 will vote for Members-at-Large for Region 8 only. Society members in Regions without designated BoG positions will vote with the Region/grouping of Regions with the majority of members.

4.5 The Nominating Committee shall cause to be published for the Society membership a call for nomination by petition, such petitions ~~including~~ to include statements of nominees' qualifications and willingness to serve if elected, to be received by the Chairperson before a specified date. A petition nominating a Society member in good standing and supported by the identifiable signatures of at least ~~25 Society members~~ 2% of the eligible voters shall automatically place that member's name on the slate. Signatures can be submitted electronically through the official IEEE society annual election website, or by signing and mailing a paper petition. The name of each member signing the paper petition shall be clearly printed or typed. For identification purposes of signatures on paper petitions, membership numbers or addresses as listed in the official IEEE membership records shall be included. Only
signatures submitted electronically through the IEEE society annual elections website or original signatures on paper petitions shall be accepted. Facsimiles, or other copies of the original signature, shall not be accepted.

4.6 The Chairperson shall ensure that all candidates are properly qualified. The ballot shall provide for write-in candidates. The ballots should be mailed to the entire Society membership including Society affiliates. The results of the vote shall be transmitted to the President and Nominating Committee Chair prior to the date of the new calendar year meeting of the BOG. Newly elected BOG members assume their positions on the first day of the year.

4.7 Those candidates having a plurality of votes will be declared to be elected. Ties shall be broken by the BOG. If an elected member fails to accept the office, the candidate receiving the next highest number of votes will be certified elected. If the vacancy cannot be filled in this manner, the President shall make appointments in cooperation with the Nominating Committee Chairperson.

4.8 The Nominations Committee and the BOG should provide names periodically to the CPMT President for consideration to Divisional Director positions and other IEEE posts.

*****

IEEE Mentoring Connection Program

Interview by Eric Perfecto, BOG member, with Cathy Downer,
Project Manager of IEEE Mentoring Connection
Program Coordinator
Published with prior permission from both Eric Perfecto
and Cathy Downer

When was the TMC instituted as the preferred IEEE mentoring site?

We conducted focus groups with IEEE GOLD members to find out what they were looking for in a mentoring program. We wanted to make sure there was a need and to find out who or what type of IEEE member they were looking for as a mentor. We wanted to propose a unique membership benefit to this group to help with retention. Our focus group participants (3 focus groups held via internet) consisted of one with US/Canada members, second with European members, and third with Asia, South Pacific (Australian area) members – all working within their time zones. Members within these focus groups told us they would value another IEEE member as a mentor – in fact they valued that relationship very highly.

While we ran these focus groups, I searched the web for an online mentoring program that was user friendly, worked within our parameters (less focused on staff administrative) and one that the mentee or protégé searched for their mentor. Not the type of matching that staff reviewed files and matched the individuals up. I also did research with other membership organizations to find out who they used and how they ran their member mentoring programs.

When I came across The Training Connection, I talked with them and asked for references. They offered information on how to help with setting up a program and on the issues we had. They offered a demo site that helped us make a decision. The people running the company were skilled in coaching, training, and running mentoring programs.

We ran a pilot program that began in 2005 with Region 1 and in August opened to Regions 2 and 3 to increase the pool of participants. We selected this area because of the larger cities, larger number of IEEE members in those cities to help with mentoring partnerships that would be close. After a six-month and year-end evaluations, we opened the program in 2006 to IEEE members.

Who and how can apply to be a mentor or to find a mentor?

IEEE members above the grade of Student Member can participate in the program as a mentor or mentee. We made the decision early not to include Students so we could offer a specific and unique program after they graduate to help with the transition into the professional fields and with career development. We did not want the program and the members participating to be used as an employment resource.

When entering the program for the first time you are asked how you are participating – as a mentor or mentee.

Why is this mentoring limited to professionals to professionals?

We wanted a unique membership benefit to offer to those members transitioning from student to the engineering professional fields. Our research told us that the members valued another IEEE member with more experience in the profession as an ideal mentor. IEEE is known as a professional membership organization.

In December 2007, we invited IEEE Graduate Student Members (GSM) to join the program. These members have graduated with their first degree and are in advanced degree programs.

Where can IEEE students go to get matched with professionals?

Many colleges and universities have their own mentoring programs for students who are matched with the college's alumni. MentorNet is an online program designed to match female students with professionals from various professional organizations within the U.S.

How does the mentor to protégé match occur?

When you enter the program as a mentor or mentee, you will complete a User Profile form with basic information. Next, the application form will ask for information that will assist in identifying and requesting the search for a match. The program will prompt you to each step. In the application form, the mentor's questions are a bit different than those of the mentee. The mentee will be asked to define their goals, while a mentor will be asked to

- check off skill competencies that you will bring to a mentoring partnership;
- provide a short biographical summary (can be pasted in from Word);
- check off your technical background based on the IEEE technical societies;
- reply to some short questions on what you would bring to a mentoring partnership as a mentor.

The next step is in the hands of the mentee as they decide who their ideal mentor will be. The mentee will decide if they want a mentor to be close geographically (by country, state/province, and city) so a face-to-face meeting can take place. If close proximity to the mentor is not the primary search criteria, the mentee can search based on skill competencies or gender. Whichever type of search is conducted, a list of potential mentors will be provided to the mentee. The mentee will review the list, along with access to their application, and then decide who they would like to contact through the system (via email) to initiate a mentoring partnership.

Once the mentee and mentor have decided to become partners, they will be encouraged to complete the mentoring agreement to help clarify expectations and define boundaries in their partnership. The IEEE Mentoring Connection Program also has a Mentoring Action Plan for the mentee to work on based on the agreed upon expectations. The Mentoring Action Plan will be reviewed at intervals by both the mentor and mentee.

What is the communication medium: email, phone, face to face?

Communication among the mentoring partners usually originates via email with the request to enter into a mentoring partnership and then each partnership decides how they will communicate. Most use email and phone. Some who are close enough meet face-to-face and also communicate via email.

Can you provide some statistics?

Presently we have 1176 mentees in the program with 540 mentors with over 80 countries represented. We have 256 active mentoring partnerships. Some mentees have more than one mentor. Since the inception of this program we have had twice as many mentees as mentors. We also have over 240 open requests for mentoring partnerships – something I try to work to close up and move over to our active partnerships.

What is the average connection (mentor to protégé relationship) time?

The mentoring partnerships run for one year. If a partnership is not working and both partners have decided to end it, we will close their partnership. Each is open to form new partnerships after one closes.

Can one have more that one mentor?

Yes, we have many mentees who have more than one mentor. We have asked that mentors have no more than two mentoring partnerships at one time. This is to allow time and effort for each partnership to grow and be successful, without causing stress on the mentor's schedule.

What is the average time required per month for a useful relationship?

We ask that mentoring partnerships use a minimum of two hours each month to communicate and discuss goals and issues.

How do you measure the success of the program?

I consider the active partnerships as success. This means that members have found a mentoring partner and are working to reach goals set by the mentee in discussion with their mentor.

What kind of resources does the program provide?

The Training Connection mentoring website has a section, "Library", which has a mentoring guide, newsletters, documents, presentations and other files related to mentoring and its partnerships. The site also has an active Discussion Forum where participants respond to questions posted by myself or our vendor. We also have a mentoring website on the IEEE site, **www.ieee.org/mentoring** which may have additional information you are looking for.

Can we find testimonials on the effectiveness of the program?

Craig Chatterton (mentor)

"Participating in the IEEE Mentoring program has been very rewarding and educational. It has given me the opportunity to share some of my experiences with younger engineers…I have participated in other long-distance mentoring programs and enjoyed them. However, the IEEE program stands out due to the focus on engineering backgrounds and professional careers. I look forward to these new and ongoing relationships."

Jamie Garcia (mentee)

"I went to the site and found it easy to navigate, searched by location, and was astounded to have such a wide selection of local

potential mentors. I contacted by current mentor and arranged a meeting. I immediately received suggestions on how to best position myself for my upcoming performance review."

"It is a pleasure to have made such as strong connection, IEEE has honed a valuable service and whether you are a mentor or mentee, there is a great deal of value in this program."

Gary C. Hinkle (mentor)
"Helping young engineers develop in their careers is very rewarding. Working with some of these individuals has proven to be quite a challenge, because of the diversity among those seeking mentors. I'm glad to be contributing to this program."

I have been interviewing mentors and mentees in active mentoring partnerships! We have filmed half of them for the purpose of creating a mentoring product commercial. The mentors interviewed and filmed so far are from Pittsburgh, Ireland and Canada. Our mentees we will be interviewing and filming are from Cairo, Japan, Saudi Arabia. One mentee we interviewed and filmed is in Pittsburgh. This has been a lengthy process in finding members who wanted to participate, agreeable to be filmed and to use their comments on the program. I am also planning to hold an online forum with this group of participants so they can discuss their partnerships, successes, and how they worked through their partnerships – while attendees can send in questions for responses.

We are also working with The Training Connection for an online mentoring orientation program on 22 May 2008 at 7:00am and again at 4:00pm Eastern. A brief announcement will be placed in The Institute Online Alert for early April. We are not ready yet for registration, but will take any questions early for the program.

Thanks you very much for your time. My hope is that by publicizing this IEEE resource more people will use it.
Visit **www.ieee.org/mentoring**

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Member Recognition:

Society of Manufacturing Engineers Recognizes Dr. C.P. Wong's Contributions

Dr. Vasudeva P. Atluri, Editor-in-Chief,
IEEE CPMT Society Newsletter

The Society of Manufacturing Engineers has selected Dr. C.P. Wong to receive its 2008 Total Excellence in Electronics Manufacturing (TEEM) award. This prestigious, annual award is in recognition of his extraordinary dedication to setting new or higher standards of achievement in electronics manufacturing. The nominating committee, which is comprised of leaders from SME's Electronics Manufacturing Tech Group, is deepely impressed by Dr. Wong's research accomplishments and selected him out of dozens of nominations to be the 2008 recipient. The award will be presented at the SME Member Luncheon, June 1st, 2008, from Noon to 1:30 PM at the Marriott Renaissance Hotel in Detroit, Michigan. Up to 100 industry leaders and professionals representing SME's Board of Directors, Member Council and Manufacturing Enterprise Council along with members and member leaders will be in attendance to applaud Dr. Wong's efforts.

Congratulations to Dr. C. P. Wong on being selected as a well-deserving recipient of the SME's 2008 TEEM award!!!

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IEEE News:

Seeking Nominations for IEEE Medals and Recognitions

Submitted by Leslie Russell, Awards Presentation Program Manager, IEEE Awards

The IEEE Awards Board is seeking nominations for IEEE Medals and Recognitions and encourages the use of its online Potential Nominee Form. This form allows a preliminary review of a nominee by the selection committee and an opportunity to obtain feedback prior to submitting an official nomination form. The Potential Nominee Form is available on the IEEE Awards Web Page at **www.ieee.org/portal/pages/about/awards/noms/potnomform.html**.

The deadline for submission of an official nomination form for any of the IEEE Medals and Recognitions is 1 July 2008. For questions concerning the Potential Nominee Form, please contact awards@ieee.org.

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Chapter Reports:

Singapore REL/CPMT/ED Chapter Update

Submitted by Alastair Trigg, Chair - IEEE Singapore Rel/CPMT/ED Chapter

In February 2008 Chapter organised a DL talk by Prof. JJ Liou of University of Central Florida, USA on Electrostatic Discharge (ESD) Protection for RF ICs.

Planning is well underway for Chapter's flagship packaging conference, EPTC 2008 which will be held in Singapore from 9 to 12 December 2008. The abstract submission deadline is 15 May 2008. Full details of EPTC can be found at the website: **www.eptc-ieee.net**

Chapter's other flagship conference The International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) will be held in Singapore on 7-11 July 2008 and will comprise two days of tutorials followed by three days of technical sessions. An equipment exhibition will be held in conjunction with the technical sessions.

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CPMT United Kingdom & Republic of Ireland (UK & RI) News

Submitted by Nihal Sinnadurai

Nihal Sinnadurai
Chapter Chair CPMT UK & RI
Executive Chair, ESTC 2008
sinnadurai@aol.com

We are delighted to have completed the adjudication of the many high quality Abstracts submitted to the Electronics System-Integration Technology Conference (ESTC-2008). The result is 184 oral papers structured into six parallel tracks and 77 Poster displays which will also have scheduled short presentation slots in the Conference.

We expect over 500 international delegates which will contribute to a lively conference and a very healthy attendance at the exhibits. I encourage CPMT members globally to attend ESTC-2008 and companies to exhibit.

This will be a fulfillment of the active collaboration with IMAPS-Europe and CPMT HQ which was initiated from here, and a gratifying outcome of the efforts to architect both this collaboration and the involvement of national and regional chapters in such international events.
Visit us: **www.estc.biz** for a full advance program.

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Student Chapter Reports:

Chalmers University of Technology
IEEE CPMT Student Chapter

Submitted by Sijia Jiang, IEEE CPMT Student Chapter Chair for 2008, Chalmers University of Technology, Göteborg, Sweden
Email:sijia@student.chalmers.se

The Chalmers University of Technology IEEE CPMT Student Chapter mainly focuses on electrical packaging, but also including other electronics fields of knowledge such as MEMS and displays. The members in the chapter, who mostly are the students of the international master's program in microtechnology supervised by Professor Johan Liu in Chalmers University of Technology, come from multiple cultures and knowledge backgrounds, and gather here in the group to share their knowledge such as electronics, physics and materials science to acquaint with the interesting and promising technology of packaging.

During the study year 2007/2008, we opened the door of electrical packaging when attending the lecture of introduction of microsystem packaging, where the lecturers Johan Liu and Cristina Andersson brought the whole group to enjoy a funny journey into the filed. And in October 2007, we paid a visit to the SAAB Space AB, which is a distinguished company in Sweden, famous with its aircrafts, automobiles and so forth. Following the presentation about the company by the Technical Manager Dr Stanley Mattson, we were guided around to see the testing and analysis facilities.

Apart from the lectures and SAAB visit, there were two fascinating guest lectures, one was about the optical products and packaging of optical devices by Dr Arne Alping at Ericsson and another was about the conductive adhesives and MEMS packaging, by Dr Masahiro Inoue, Osaka University, Japan and Katrin Persson, Iomego, respectively.

As to the social activities, a dish party as a tradition in the chapter was held in MC2 building, Chalmers University during which everybody brought diversified food prepared by ourselves and enjoyed the beverage "sponsored" by Chalmers University of Technology. Additionally, our chapter members organized a "movie and culture" party to communicate the different cultures in our respective home countries and also other activities to enhance our friendship.

So far, the members in the chapter have gained rather enough knowledge of packaging, in the upcoming autumn, it is the time we are going to participate in some projects with more practical experiments, which are believed to make us more engineer-like and put the theory into practical challenges.

Dish Party as a Student Chapter Tradition of Our Chapter

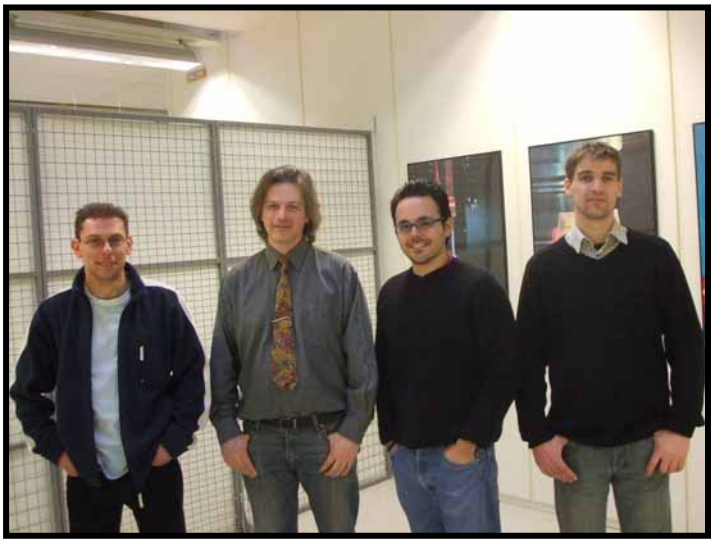
Dish Party as a Tradition of Our Chapter in MC2 Building (Year 2005 ~ 2007)

During October, 2007, for the student members of year 2007 / 2008

During November, 2007, for the student members of year 2006 / 2007

Visit to Frontside Electronics AB, during February, 2007

During December, 2005, for student members of the year 2005 / 2006



Visit to MYDATA Automation AB, Bromma, Sweden, March, 2007.

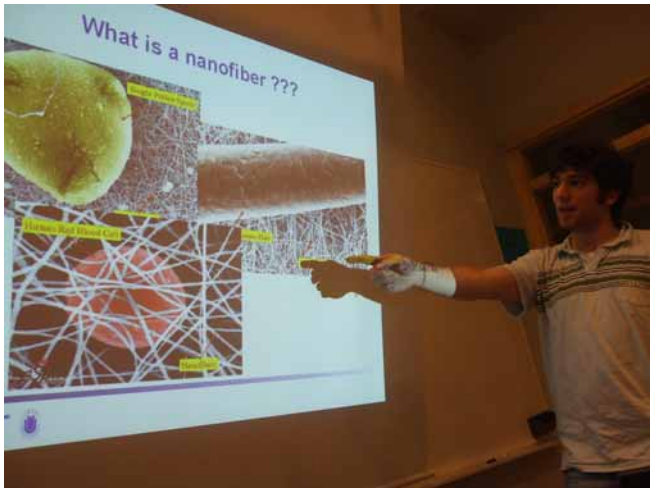
Company Visits

Visit to SAAB Space AB, September, 2006, for the student members of the year 2006 / 2007

Visit to SAAB Space AB, during September, 2005 for the student members of the year 2005 / 2006

Guest lecture about MEMS from Iomega during October, 2007 for the student members of year 2007 / 2008

Project Seminars during January thru April, 2007



Student members of year 2006/2007 are presenting

Professor Johan Liu is discussing with the student members of year 2005/2006 during Project Seminar held in March, 2006

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Conference Reviews:

58th Electronic Components and Technology Conference (ECTC) Update

Submitted by Dr. Rajen Dias, Asst. Program Chair

The 58th ECTC that will be held at Disney's Contemporary Resort in Lake Buena Vista, Florida, USA during May 27 to 30, 2008, has received 616 technical abstracts, a record number for the technical program. The technical program will feature over 300 high quality technical papers, presented in 36 oral sessions, two poster sessions and a special student poster session. The papers will cover a wide spectrum of topics including advanced packaging, interconnections, electronic components, materials, processing, assembly, manufacturing, optoelectronics, quality and reliability, modeling, simulation and emerging technology that focuses on nano-technology, biomedical and flexible electronics.

The technical program is complemented by 16 professional development courses, a plenary session, a panel discussion session and a CPMT seminar session. In addition, there is a technical exhibit corner where over 50 leading companies, primarily in the electronics components, materials, thermal and packaging fields exhibit their latest technologies and products. The conference allows ample opportunities to network and meet leading experts in the field.

For more information on 58 ECTC, please visit **www.ectc.net**

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ECTC 2008 Professional Development Courses Tuesday, May 27, 2008

Kitty Pearsall, Chair ***Jeffrey Suhling, Co-Chair***
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(continued…)

Morning COURSES
8:00 AM - 12:00 PM

1. ACHIEVING HIGH RELIABILITY FOR LEAD-FREE SOLDER JOINTS - MATERIALS CONSIDERATION

Course Leader: Ning-Cheng Lee – Indium Corporation of America

Course Objectives:

This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail, and novel alloys with reduced fragility will be presented. Electromigration, corrosion, and tin whiskering will also be discussed. Furthermore, the reliability of through-hole solder joints will be reviewed, and recommendation will be provided, particularly for thick boards. The emphasis of this course is placed on the understanding of how the various factors contributing to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability. Also will be presented are the desirable future alloys and fluxes in order to meet the challenge of miniaturization.

Course Outline:

- Implementation Status
- Prevailing Materials - Alloys and Finishes
- Surface Finishes Issues - ENIG, ImAg, and ImSn
- Mechanical Properties - Shear, Pull, and Creep
- Intermetallic Compounds - Effect of Cu, Ni, Other Additives, and Heat History
- Failure Modes - Grain Deterioration, Orientation, Mixed Alloys, and Interfacial Voiding
- Thermal Cycle Reliability - Effect of Cycling Condition, Surface Finishes, and Reflow Temperature
- Reliability of Through-Hole Joints - Large and Thick Boards, Partially Filled Through-hole
- Fragility - Effect of Surface Finishes, Alloys, Reflow, Strain Rate, Aging, Cycling, and IMC
- Electromigration - Effect of Current Density, Back Stress, and Cu UBM Thickness
- Corrosion - SAC and Performance of Surface Finishes Under Harsh Conditions
- Tin Whisker - Causes of Formation, Methods for Control

Who Should Attend:

Any one who care about achieving high reliability lead-free solder joints and like to know how to achieve it should take this course.

2. ULTRAHIGH THERMAL CONDUCTIVITY PACKAGING MATERIALS

Course Leader: Carl Zweben – Thermal Materials Consultant

Course Objectives:

This course provides an in-depth discussion of the increasing number of ultrahigh-thermal-conductivity materials that address key packaging problems: heat dissipation, warpage and fracture of low-k dielectric layers, solder joints, etc., arising from differences in coefficient of thermal expansion (CTE). Topics include properties, manufacturing processes, applications, cost, lessons learned, and future directions, including carbon nanotubes. Traditional materials are included for reference.

There are now over 15 low-CTE, low-density materials with thermal conductivities ranging between that of copper (400 W/m-K) and 1700 W/m-K. Thermally conductive carbon fibers allow heat removal from the bottom, as well as the top of a chip, expanding the range of convection cooling. The fibers also can tailor substrate and printed circuit board (PCB) CTE, potentially eliminating the need for underfill. Carbon nanotubes and fibers can greatly increase thermal interface material thermal conductivity. Low-CTE solders under development will provide additional advantages.

Advanced materials are being used in an increasing number of commercial and aerospace microelectronic and optoelectronic applications, including servers, laptops, phased array antennas, telecommunication equipment, laser diodes, solid state lighting, plasma displays, liquid crystal displays, etc. For example, low-CTE diamond particle-reinforced SiC heat spreaders having a thermal conductivity of over 600 W/m-K were used in IBM servers.

Course Outline:

- Key heat dissipation, thermal stress and warping problems
- What is wrong with traditional materials? Overview of their properties
- Classes of ultrahigh thermal conductivity materials: monolithic and composite
- Properties of key monolithic carbonaceous materials
- Properties of key metal matrix composites
- Properties of key ceramic matrix composites
- Properties of key carbon matrix composites
- Properties of key polymer matrix composites
- Thermally conductive, low-CTE printed circuit boards
- Manufacturing methods for advanced materials
- Using advanced materials to improve manufacturing yield
- Lessons learned
- Cost considerations
- Applications of ultrahigh-thermal-conductivity-materials
- Future directions, including carbon nanotubes
- Summary and conclusions

Who Should Attend:

Engineers, scientists and managers involved in microelectronics, optoelectronics and MEMS/MOEMS thermal management and packaging design, production and R&D as well as material suppliers should benefit from this class.

3. VERTICAL (3D) HYPER-INTEGRATION AND PACKAGING OF MICRO-NANO-SYSTEMS

Course Leader: James Jian-Qiang Lu – Rensselaer Polytechnic Institute

Course Objectives:

An overview of vertical (3D) hyper-integration and packaging of micro-nano-systems will be presented, including motivation, key technologies and status towards commercialization. The major motivations discussed include miniaturization of micro-systems; performance increase in speed and data bandwidth due to massive small-sized inter-chip interconnects; heterogeneous system integration of variety of technologies; and lower manufacturing cost for specific applications using particular 3D platforms.

In this course, 3D hyper-integration technologies are divided into 4 categories – transistor build-up, wafer-to-wafer stack, die-on-wafer assembly, and packaging-based 3D. In transistor build-up 3D, active devices are built-up over an IC wafer. In wafer-to-wafer stack 3D,

different systems are first fabricated independently and then stacked and interconnected vertically. The die-on-wafer assembly is similar to SoC approach, but with known-good-dies (KGDs) assembled on an IC wafer, then processed in wafer-level. In the last category, the ICs are packaged vertically in die-to-die, system-in-packaging (SiP) and package-on-package (PoP) fashions.

This course will discuss all these technologies, with emphasis on wafer-to-wafer 3D hyper-integration and potential applications. Sample designs and applications towards commercialization will also be presented. The issues associated with each technology category will be discussed, including integration architecture and design tools, yield and cost, thermal and mechanical constraints, and manufacturing infrastructure. Finally, future directions into micro/nano/electro-opto/bio system hyper-integrations including MEMS will be presented, showing 3D hyper-integration as a very promising emerging architecture for future computer, network, nanotech, and biotech.

Course Outline:

- Challenges of current ICs and packaging
- Why 3D Integration?
- Overview of 3D integration and packaging technologies
- Transistor build-up 3D integration
- Wafer-to-wafer stack 3D hyper-integration: Key unit processes;
- Through-Silicon-Vias (TSV);
- Oxide-to-oxide bonding (via-last);
- Dielectric adhesive bonding (via-last);
- Metal-to-metal bonding (via-first);
- Metal/adhesive redistribute
- Die-on-wafer assembly 3D hyper-integration
- Packaging-based 3D hyper-integration
- Technology status, assessment and challenges/issues
- 3D-enabled designs and applications
- 3D Hyper-integration perspectives and technology projections
- Conclusions

Who Should Attend:

Engineers, managers and executives involved in future R&D investments, assembly and product development of electronic packaging, and wanting a fundamental understanding of 3D technologies, as well as the materials and equipment suppliers wanting to know about the existing and future 3D integration technologies and options, will greatly benefit from this course.

4. FROM THICK WAFERS TO THIN CHIPS - CHALLENGES IN PREASSEMBLY

Course Leader: Werner Kröninger – Infineon Technologies

Course Objectives:

This course introduces the technologies and methods used for thinning wafers down to ultra-thin applications. Preassembly is the main enabler for 3D technologies. Thinning and separation of dice will both be covered, especially chip separation has most interesting new developments which will be discussed in detail. Most logic-ICs are going thin for improved heat-dissipation, reduced electrical resistance or improved mechanical flexibility. Preassembly, linking Front-End and Back-End by transferring the wafers into chips, has two main spheres: wafer-thinning and chip-separation. An overview regarding the different process-flows for thinning chips will be given. Emphasis will also be placed on several processes of back side treatment, improving the mechanical performance of the chips. Potentials and opportunities of these process-flows are discussed. Current and future technologies for chip-separation, including all state-of-the-art flows, will be presented. The various separation-processes and their pros and cons will be covered in detail. Emerging technologies will also be discussed and evaluated. The resulting mechanical properties, important for the performance of many devices, will be presented. Topics and solutions regarding the handling of thin wafers and assembly of thin chips will also briefly be covered. This will help potential users to make decisions about the suitability of these technologies for their applications.

Course Outline:

- Applications for thin dice
- Technologies of wafer thinning: grinding, wet-etch, polish, dry-etch
- Inside silicon: the process of Grinding
- wafer bow and wafer warp
- Stability and flexibility
- Back side treatment, chip-thickness and –strength
- Limits to thinning wafers
- Relevant for dicing and packaging: Surface features
- The general influence of dicing in producing chips
- Combination: separating by thinning
- Ways of separating the dice: Current and emerging technologies
- Shipping & handling and assembly of thinned wafers and dice

Who Should Attend:

The course is intended for technical managers in preassembly and aims at fundamental understanding of thinning and singulation processes. It is also very helpful for staff-and management members in making decisions on what processes to use for their applications. Engineers and managers of die-bonding (back-end) and packaging engineers should also attend to see the increasing influence of preassembly to their field.

5. THROUGH SILICON VIAS AND MICROVIAS FOR HIGH DENSITY INTERCONNECTS IN ADVANCED PACKAGES

Course Leader: Ricky Lee – Hong Kong University of Science and Technology

Course Objectives:

Through silicon vias (TSVs) are one of the major enabling technologies for 3D integration and 3D packaging. In recent years, TSVs have attracted substantial attention in the industry and the academia. This course will elaborate on the latest development and the most important research results of forming and plugging TSVs. In addition, the forming and filling of microvias on organic PCB/substrates with build-up layers will be presented as well. The applications of these two levels of high density interconnects (HDIs) in advanced packaging will be introduced. Some related reliability issues will be addressed. For professionals active in microelectronic packaging research and development, this is a timely summary of progress in all aspects of this fascinating field. The lecture contents are based on the instructor's books, his recent research results, and interactions with the packaging and assembly industries. The scope of this course covers overview of HDI technologies, via forming and plugging processes, insulation/barrier/adhesion and build-up layers, characteristics of copper diffusion, various applications and reliability considerations. With the information provided in this lecture, the attendees will acquire a practical understanding in the design, materials, processes, and reliability issues of high density interconnects in advanced packaging.

Course Outline:

- Overview of high density interconnect (HDI) technologies

- Forming of through silicon vias (TSVs)
- Deposition of interfacial multi-layers on the wall of TSVs
- Plugging of TSVs
- Applications of TSVs
- Organic PCB/substrates with sequential build-up layers
- Forming of microvias on organic PCB/substrates
- Filling of microvias
- Special high density interconnect technologies
- Reliability issues of high density interconnects

Who Should Attend:
This short course is intended for research scientists, professional engineers and technical managers who are involved in IC packaging, component assembly, materials and processing, contract manufacturing and marketing.

6. MOISTURE RELATED RELIABILITY IN ELECTRONIC PACKAGING

Course Leader: Xuejun Fan – Lamar University

Course Objectives:
This course will present a state-of-art and in-depth overview of recent advances in moisture related reliability studies in IC packaging. The course provides fundamental knowledge and understandings on the failure mechanisms associated with moisture such as delamination/cracking during reflow, material and interface degradation during HAST, as well as the electrochemical metal migration and corrosion under biased HAST condition. General reliability test practice, qualification, and the different failure mechanisms will be presented. The accelerated test methodology and experimental validations will be discussed. The course will cover moisture diffusion principles and the characterization of moisture related properties, such as diffusivity, solubility, saturated moisture concentration, and the hygroscopic swelling, and adhesion. The vapor pressure evolution at elevated temperature, especially for lead-free applications and reliability concern, will be discussed. The impact of hygroscopic swelling on copper/low K structures as well as under bump metallurgy (UBM) failures will be described. The key challenges in reliability performance for ultra-thin 3-D stack-die chip scale packages and the selection of wafer level film (WLF) will be discussed. The optimization of reflow profile to reduce the failure rate will be introduced. Several case studies related to moisture-induced failures in different types of packages such as flip chip package, TSOP, QFN, and stack-die chip scale packages will be presented. Course Objectives: 1. Fundamental understanding on moisture-induced failure mechanisms under different accelerated testing conditions; 2. Knowledge on material behaviors in the presence of moisture and the impact on reliability performance; 3. Identification of key material properties related to moisture and material selection guidelines; 4. Familiarity of the existing tools to perform the moisture related modeling and material characterization. 5. Case studies for preventing packages from moisture-induced failures such as flip-chip package, QFN package, Stack-die chip scale packages and TSOP packages.
Course Outline:

- Introduction
- Moisture related reliability test and specifications – MSL, HAST, BHAST etc
- Typical failure modes and failure mechanisms in the presence of moisture
- Moisture diffusion – theory and applications
- Moisture absorption vs. water absorption
- Characterization of moisture related material properties
- Vapor pressure evolution at reflow temperature - what's the impact when lead-free soldering is applied?
- Case study – underfil selection in flip chip BGA applications
- Case study – wafer level film failures in 3-D stacked chip scale packages
- Hygroscopic swelling – the impact on low K/Cu interconnect with silicon-package interaction
- Effect of moisture on material properties
- Accelerated test with moisture - can we further accelerate the test?
- Case studies – QFN, TSOP, Flip-Chip

Who Should Attend:
The course is designed for staff members, technical managers, design and manufacturing personnel, and reliability engineers in microelectronic companies. Although the course reviews most recent advances in moisture related reliability issues, the course does not assume prior knowledge of these issues and hence is of interest for both experts and new actors in this area.

7. DEEP SUBMICRON AND NANOSCALE CMOS PROCESS TECHNOLOGIES

Course Leader: Badih El-Kareh – Independent Consultant

Course Objectives:
Dr. Badih El-Kareh will give an overview of CMOS processes associated with today's semiconductor devices. He will cover CMOS components, conventional CMOS technologies, scaling to deep submicron dimensions and enabling processes, scaling limitations, and enhancements for nanoscale generations, including strained silicon, new gate materials, high-K and low-K dielectrics, and three-dimensional structures.
Course Outline:

- CMOS components, silicon crystal
- Junctions and contacts
- MOSFETs, CMOS
- Conventional CMOS, process technologies, silicon crystal
- Insulators, doping and etch techniques
- Contacts and metallization
- An integrated CMOS process
- Scaling to deep submicron
- Why scaling, scaling scenarios
- Enabling process technologies, copper metallization
- Scaling and limitations
- Nanoscale CMOS
- Mobility enhancement techniques, strained silicon
- New gate material, high-K dielectrics
- Low-K inter-level dielectrics
- Three-dimensional structures, outlook

Who Should Attend:
The course is intended for industrial and academic professionals who need an overview of submicron and nanoscale CMOS process technoligies.

8. FUNDAMENTAL AND RECENT ADVANCES ON POLYMERS AND NANO-COMPOSITES IN ELECTRONIC AN

Course Leaders: CP Wong – Georgia Tech;
Ephraim Suhir – Univ of California

Course Objectives:
Describe the application of polymeric materials in electronic, opto-electronic and photonic packaging (underfills, embedded passives, adhesives, encapsulants, insulators, dielectrics, and even conductive elements for interconnects), indicate the major differences in the

requirements for, and applications of, polymeric materials in microelectronic and photonic packaging, elaborate on the potential of nanomaterials and nanotechnologies in electronics and photonics packaging, Material formulators, suppliers and users should have a thorough understanding of the merits and shortcomings of the existing polymeric materials, as well as of the recent advances in the field, and, first of all, in the area of nano materials and technologies, and what has been achieved and could be expected owing to their applications in components, packaging and manufacturing technologies. What You Will Learn: 1. Fundamental and State-of-the-art and challenges in Polymers in electronic and photonic packaging 2. Materials properties, mechanical behavior and reliability of polymer-coated electronics, optical fibers, and role of predictive modeling 3. What is going on with the nanoscale functionalized materials 4. What could be gained by using nanomaterials and nanotechnologies in microelectronics, opto-electronics, and photonics.

Course Outline:

Brief overview of electronics, opto-electronic and photonics packaging : materials, designs, reliability

Polymeric materials in electronic and photonic packaging

Novel No Flow, Advanced and Reworkable Underfills for Flip-chip Applications

Conductive adhesives and nano-lead-free Alloys for lead-free Interconnects-Fundamentals and Recent Advances

Low-cost High Performance Embedded Passives Materials and Processes

Recent Advances on Low Dielectric(k), Nano- functional Materials(high k polymer-composites).

Polymers use in electronics and coated optical fibers

What are nanomaterials and nanotechnologies?

Some rent and future applications of nanotechnology in micro- and opto-electronic packaging and beyond

Who Should Attend:

Engineers, applied scientists and technical managers involved in the design, processing and manufacturing of micro- and opto-electronic materials and systems, in micro- and opto-electronic packaging and reliability evaluations, as well as material suppliers and users should benefit from taking this course.

AFTERNOON COURSES
1:15 - 5:00 PM

9. DESIGN FOR RELIABILITY AND RELIABILITY TESTING OF LEAD-FREE INTERCONNECTS

Course Leader: John Lau – IME

Course Objectives:

In this course, participants will learn the principles of design for reliability (DFR) and reliability testing and data analysis, and lead-free interconnects. Emphasis is placed on the solder-joint reliability of solder-bumped flip-chip assemblies, solder-balled BGA assemblies, solder-bumped fine-pitch CSP and WLCSP assemblies under thermal fatigue, isothermal fatigue, mechanical bending and shearing, and shock & vibration conditions. Also, up-to-date lead-free solder-joint reliability data of high-density PCA are presented.

Most of the materials are based on the instructor's recently published textbooks, "Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies", "Electronics Packaging", "Chip Scale Packages", "Low-Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies", "Microvias for Low-Cost High-Density Interconnects", and "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive Adhesive Materials". (McGraw-Hill publishes all these books.) Each participant will receive a comprehensive set of handout notes.

Course Outline:

Understand all important aspects of BGA, WLCSP, and flip chip technologies

Know the state-of-art of lead-free soldering

Know the effects of X on the IMC and Cu consumption of SnAgCuX solder joints

Material properties of lead-free solders

Know how to do design for reliability (DFR) of lead-free solder joints

Understand the real meaning of reliability

Know how to do reliability testing and data analysis

Know how to determine the true Weibull Slope and true characteristic life

Help your company to make important decisions on lead-free reliability issues

Identify key parameters that impact the solder joint reliability of your products

Avoid potential reliability problems of your high-density lead-free products

Predict reliability, failure rate, and MTTF of your lead-free products

Who Should Attend:

If you are involved with any aspect of the electronics industry, you should attend this course. The content is recommended for component, packaging, design, material, process, equipment, reliability, product assurance, quality control, manufacturing, vendor, marketing, and sales engineers and managers. It is equally suited for R&D engineers and scientists.

10. ON-CHIP THERMAL MANAGEMENT OF NANELECTRONIC COMPONENTS

Course Leader: Avram Bar-Cohen – University of Maryland

Course Objectives:

The rapid migration of microelectronics into nanoelectronics, with the consequent rise in transistor density and switching speed, has led to steep increases in die heat flux and growing concern over the emergence of on-chip "hot spots". In the absence of new and more aggressive thermal management techniques, nanoelectronic chips can be expected to experience accelerated failure rates and an overall loss in IC reliability and performance. The application of on-chip high heat flux cooling techniques provides a most promising direction for the thermal management of nanoelectronic components and is the focus of this Professional Development course.

Successful development of this cooling strategy requires the integration of thermal management principles and concepts into the design and development process from the earliest stages of chip design. Consequently, the course will begin with a brief review of the iNEMI and ITRS thermal roadmaps and a review of the thermal packaging technology options. Attention will then turn to emerging high flux, on-chip cooling techniques, including solid state thermoelectric coolers-both miniaturized and thin-film TEC's, orthotropic spreaders, and dielectric liquid cooling

Course Outline:

Industry Roadmap for IC technology and packaging

iNEMI thermal management Roadmap

Thermal management options – air, liquid, refrigeration

Emerging high heat flux cooling techniques: solid-state refrigeration – miniaturized and thin-film TEC's, dielectric liquid cooling – spray cooling, pool boiling, two-phase microgap coolers.

Wrap up: What have we learned?

Who Should Attend:

This course is aimed at product managers, research staff, and packaging specialists involved in the design, development, optimization, and testing of advanced micro- and nanoelectronic products. Developers of advanced thermal management technology would also greatly benefit from this course.

11. SYSTEM-ON-PACKAGE (SOP) VS. SYSTEM-IN-PACKAGE (SIP), AND SYSTEM-ON-CHIP (SOC) NE

Course Leaders: Rao Tummala and Mahadevan Iyer – Package Research Center

Course Objectives:

This course presents an overview for highly integrated and microminiaturized convergent systems with consumer, computer, communication and bio-medical functions implementing an integrated approach to digital, analog, RF, optical and sensing technologies. The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market IC-package co-design-centric microsystems packaging design and technology flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP's design flexibility and simplicity, lower cost, and higher electrical performance, and without the intellectual property issues that dominate SOC. To realize these enormous advantages, new SOP sub technology paradigms are required. These include mixed-signal design, ultra high-density embedded digital, embedded optoelectronics and embedded RF component integration as well as wafer level packaging (WLP) and assembly, test and burn-in, thermal management and system reliability. This course makes a compelling case for and presents the status of SOP R&D around the world and compares and contrasts with SOC, SIP and MCM.

Course Outline:

- System trends to convergent micro miniaturized systems
- Semiconductor trends to SOC
- IC and systems packaging evolution
- What is SOP and its Global developments
- SOC, SIP, MCM and SOP – Definitions, Technologies &Applications
- SoP for Digital, RF, Optoelectronic & Sensing Applications
- Technologies & Challenges in SOP Assembly, Thermal Management and Reliability
- Embedded Actives & Passives using SOP Technologies
- Applications of nano materials in SOP
- Convergent Bio SOP Technologies

Who Should Attend:

This course is an overview course and is suitable for all levels of R&D management, senior engineers and executives involved in technical strategy, R&D, design, manufacturing, process and product development of electronic packaging and systems in automotive, consumer, communication, computer, bio-medical, and aerospace industries.

12. WAFER LEVEL – CHIP SCALE PACKAGING

Course Leader: Luu Nguyen – National Semiconductor Corp.

Course Objectives:

Wafer Level-Chip Scale Packaging (WL-CSP) has gained momentum in the small chip arena, driven by needs for cost reduction, form factor shrinkage, and enhanced performance. This course will provide an overview of the WL-CSP technology. The market drivers, benefits, and challenges facing industry-wide adoption will be discussed. The current WL-CSP configurations will be reviewed in terms of their construction, manufacturing process, and published electrical and thermal performance, together with package and board level reliability. Since the technology marks the convergence of fab, assembly, and test, discussion will also address some fundamental issues such as: 1. Does it fit best with front-end or back-end processing?

2. Will it be applicable and cost-effective for memory and other complex devices such as ASICs and microprocessors?

3. Are the current standards for design rules, outline, and reliability applicable? Extensions to higher pin count packages and other arenas such as RF and MEMS will be reviewed.

Course Outline:

- Wafer Level-Chip Scale Packaging (WL-CSP) definition
- Market drivers for WL-CSPs
- Benefits of WL-CSPs
- Barriers and challenges for WL-CSPs
- Review of current WL-CSPs in the industry
- Wafer level testing – status and challenges
- Infrastructure service providers
- Case studies of WL-CSPs (structures, processing, reliability, applications)
- Extension of WL-CSP concept to other arenas (sensors, imaging, MEMS, etc.)
- Future trends: enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra thin WL-CSP, stacked WL-CSP, MCM in "reconstituted wafers," embedded components, etc.)

Who Should Attend:

The course will be useful to the following three groups of engineers and scientists:

1. Newcomers to the field who would like to obtain a general overview of WL-CSP.

2. R&D practitioners who would like to learn new methods for solving CSP problems.

3. Those considering WL-CSP as an alternative for their interconnect systems.

13. EMBEDDED PASSIVE TECHNOLOGY AND COMMERCIALIZATION

Course Leader: Richard Ulrich – University of Arkansas

Course Objectives:

This course will be a comprehensive review of potential applications, commercialized technology, and possible future directions in integrated passive components and processing for organic boards. The organization of the course centers on the benefits and problems with their implementation in order to help potential users make decisions about their applicability in a given situation. Considerable time will also be spent on the candidate materials and processes for integrated resistors, capacitors and inductors in order to help the potential user decide what processes can provide the needed electrical performance while being compatible with their existing substrates and fabrication technology. Emphasis will also be placed on electrical testing, since users of integrated passives will find themselves in the business of producing passive components, not just buying them, and since the electrical performance characteristics of integrated passives can be very different from their surface-mount counterparts, possibly providing significant competitive advantages. Several current potential applications will be described, with particular emphasis on decoupling. The course emphasizes applicability to manufactured microelectronic systems and includes theoretical material necessary to support that purpose.

Course Outline:

- Definitions, Why Use EP's, History
- Substrates of Interest, Thick vs. Thin Film
- Embedded Resistors
- Embedded Capacitors
- Dielectric Choices
- Embedded Inductors
- Electrical Measurement of EP's
- Decoupling
- Filtering
- Termination
- Economic Tradeoffs
- Tolerance, Repeatability and Yield
- Commercialized Systems
- Barriers to Market Penetration
- Where are EP's Going?

Who Should Attend:

Engineers and scientists involved in electronics packaging, circuit board manufacture, electrical design and passive component technologies will benefit from taking this course. The course emphasizes, in order of coverage, motivations for integrated passives, processing, applicability to current systems, materials science, and electrical performance. Anyone in those areas would benefit.

14. ADHESION AND FRACTURE IN MICROELECTRONIC PACKAGING

Course Leader: Mikel Miller – Texas Instruments

Course Objectives:

This short course will explain adhesion, fracture and material concepts as they pertain to microelectronics packaging reliability. Taking a pragmatic rather than esoteric approach, the course is designed to provide a framework for engineers and managers to better understand, solve and potentially avoid adhesion related reliability issues at their respective organizations.

The course will start with an introduction to physical and chemical adhesion, fracture mechanics and material behavior as it pertains to electronic packaging materials. The focus will be to understand what factors play a role in developing interfacial stress and determining interfacial strength. After these fundamentals are discussed, the course will present several adhesion testing techniques germane to microelectronics, discussing what tests are appropriate for each material and the pros and cons of each. This will include interfacial strength testing techniques such as stud pull, button shear and laser spallation and interfacial fracture mechanics techniques such as beam bending tests. Emphasis will be placed on determining which technique is appropriate and feasible for a given situation. Finally, several examples of adhesion related failures in microelectronic components will be discussed and analyzed by applying the earlier learned concepts to each situation. Examples will include issues from flip-chip and leadframe packaging.

Course Outline:

- Adhesion, Fracture and Material Fundamentals
- Chemical Adhesion
- Physical Adhesion
- Fracture Mechanics
- Material Behavior
- Adhesion Measurement Techniques
- Strength of Materials Adhesion Testing
- Fracture Mechanics Adhesion Testing
- Examples of Adhesion-related packaging failures
- Application of adhesion concepts and testing techniques for packaging development

Who Should Attend:

Engineers and technical managers relatively new to thermomechanical reliability of microelectronic packaging, or those wishing to refresh their fundamental understanding of the field will benefit from taking this course.

15. CHALLENGES IN MEMS AND BIO-CHIP PACKAGING

Course Leader: C. S. Premachandran – Institute of Microelectronics

Course Objectives:

Challenges in MEMS and Bio-chip Packaging MEMS is an emerging market in the electronic and medical sector .Many conventional devices are being replaced by silicon based MEMS devices. MEMS devices are manufactured by micromachining silicon for mechanical structures, thin diaphragms, actuators etc. Using silicon process the MEMS devices can be fabricated into tiny chips and is easily integrated into CMOS platform. MEMS devices have wide applications such as mobile phones, hand held devices, automobile, medical products, consumer market etc. So MEMS play a key role in everybody's daily life and has become an indispensable part of the human life.

A final product is realized after packaging the chip. MEMS packaging requires many challenges such as hermetic, vacuum, damping, external access to the media outside etc. Packaging of MEMS device becomes much more challenges than the conventional packaging. To meet the tiny requirement of the package, wafer level packaging, Through silicon via(TSV) ,bumping technologies are aggressively trying to use it to meet the above requirements. Bio chip packaging require more attention than the MEMS packaging because the fluid flow in narrow channels, leakage, evaporation, hydrophobic requirements need to be addressed. Biosensors use MEMS devices to control the body movements, body measurements, imaging etc to understand the body function. Packaging of these devices is a challenge due to the interaction of this packaging with the body.Packaging requirements for implantable chips demands stringent requirements and need to be addressed during the initial product development time.

Course Outline:

- MEMS packaging Introduction
- Wafer to wafer bonding
- Low stress packaging
- Hermetic packaging requirements
- Vaccum packaging requirements and challenges
- wafer level packaging for MEMS
- Microphone, accelorometer, Bolometer ,RF MEMS ,Optical MEMS packaging
- Low temperature wafer-wafer bonding for MEMS
- Biochip packaging requiremnts
- Microfluidic packaging
- Packaging requirement for Lab on a chip(LOC) applicaions
- Thermal considerations for Polymer chain reactions
- Biosensor packaging requirements
- optical Biosensor packaging for bio-imaging
- Implantable sensors
- Reliability requirements

Who Should Attend:

This course is intended for engineers and managers who are involved in the development of MEMS,Bio-chip devices and systems employing sensor,electronic, bio and optical components. This course aims to give an overview and basic packaging requirements on rapidly developing new areas on bio-packaging and mems packaging.

16. TRENDS IN 3D PACKAGING

Course Leaders: Jan Vardaman – TechSearch International, Inc; Phil Garou – TechSerach International, Inc

Course Objectives:

3D packaging is the answer for space constrained applications and products that require greater functionality in a smaller space. 3D packaging offers improved performance for a variety of applications ranging from portable products to space. 3D packaging includes stacked die as well as package on package (PoP) configurations.

Through-hole silicon via (TSV) is the ultimate 3D interconnect. Driven by the need for improved performance and the reduction of timing delays, methods to use short vertical interconnects have been developed to replace the long interconnects found in 2D structures. The industry is moving past the feasibility (R&D) phase for TSV technology into the commercialization phase where economic realities will determine which technologies are adopted.

3D integration with through silicon vias (TSV) includes:

- Through wafer via technologies
- Thinning of wafers
- Wafer-to-wafer and die-to-wafer bonding

This tutorial focuses on the developed of 3D packaging and the current high volume production parts. The tutorial also covers the key enabling technologies for through silicon via formation. Various methods to fabricate vias are described. Enabling unit operations are discussed including:

Course Outline:

- Development of 3D packaging and the current high volume production parts
- Key enabling technologies for through silicon via formation
- Methods to fabricate vias
- Enabling unit operations
- Critical factors limiting the adoption of TSV technology

Who Should Attend:

Packaging engineers that are space constrained in their designs will find the answers that they are seeking by taking this tutorial.

*****

IEEE CPMT Society Newsletter

Send inputs, suggestions, and articles by email to nsltr-input@cpmt.org

….. Editor

Put your Technology Leadership in Writing!

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Additional Information at www.cpmt.org/conf/

CONFERENCES IN 2008:

IEEE Workshop on **Signal Propagation on Interconnects** (SPI 2008) **www.univ-brest.fr/SPI**
May 12-15, 2008 Avignon, France
Contact: Denis Deschacht, Denis.Deschacht@lirmm.fr

58th **Electronic Components and Technology Conference** (ECTC 2008) **www.ectc.net**
May 27 - 30, 2008; Disney's Contemporary Resort Lake Buena Vista, Florida USA
Contact: Jean Trewhella, IBM, jeanmh@us.ibm.com

Intersociety Conference on **Thermal and Thermomechanical Phenomena in Electronic Systems** (I-THERM 2008) **www.ithermconference.org**
May 28-31, 2008 Orlando, FL USA
Contact: Ms. Kelly Sutton, epd@engr.arizona.edu

18th IEEE **Semiconductor Wafer Test Workshop** (SWTW 2008) **www.swtest.org**
June 8-11, 2008 San Diego, CA USA
Contact: Bill Mann, william.mann@ieee.org

International **Conference on Electronics Packaging** (ICEP 2008) **www.jiep.or.jp/icep**
June 10-12, 2008 Tokyo Big Sight, Tokyo, Japan
Contact: ICEP Secretariat at icep@jiep.or.jp

Joint Int'l Conference on **Electronic Packaging Technology & High Density Packaging** (ICEPT-HDP) **www.icept.org**
July 28~31, 2008 Shanghai, China
CFP Abstracts Deadline: April 11, 2008
Contact: ICEPT-HDP Secretariat at icept2008@fudan.edu.cn

Joint Event: 7th Int'l IEEE Conference on **Polymers and Adhesives in Microelectronics and Photonics** (POLYTRONIC 2008) with **PORTABLE 2008**
August 17—22, 2008 Edelweiss Hotel & Conference Center **www.polytronic2008.com**
Garmisch-Partenkirken, Germany
Contact: info@polytronic2008.com

Electronics System-Integration Technology Conference (ESTC 2008) **www.estc.biz**
September 1-4, 2008; University of Greenwich Greenwich, London UK
Contact: Chris Bailey, Greenwich University, chris.bailey@estc.biz

2008 Workshop on **Accelerated Stress Testing & Reliability** (ASTR) **www.ewh.ieee.org/soc/cpmt/tc7/ast2008**
October 1 - 3, 2008 Portland, OR USA
Abstracts Due: April 28, 2008
Contact: Cheryl Tulkoff, National Instruments, cheryl.tulkoff@ni.com

Joint Event: 3rd **Int'l Microsystems, Packaging, Assembly and Circuits Technology** (IMPACT) Conference, with the 10th Int'l Conference on **Electronics Materials and Packaging** (EMAP) **www.impact-emap.org**
October 22 - 24, 2008 Taipei, Taiwan
Abstracts Due: May 31, 2008
Contact: Mr. Long-Shien Lin, tw2008@isu.edu.tw

54th IEEE **Holm Conference on Electrical Contacts** (HOLM 2008) **www.ewh.ieee.org/soc/cpmt/tc1/h2008/h2008top.html**
27-29 October, 2008 Orlando, FL USA
Contact: Chi H. Leung, AMID DODUCO, cleung@amidoduco.com

33rd Int'l **Electronics Manufacturing Technology Symposium** (IEMT 2008) **www.cpmt.ieeemalaysia.org**
November 4-6, 2008; Penang, Malaysia
Contact: Ir. Dr. Cheong Kuan Yew, USM cheong@eng.usm.my

9th **VLSI Packaging Workshop in Japan**
December 1 - 2, 2008; Kyoto, Japan **vlsi-pkg-ws.org**
Abstracts Due: May 31, 2008
Contact: Michitaka Kimura, Renesas Technology Corp, kimura.michitaka@renesas.com

10th **Electronics Packaging Technology Conference** (EPTC 2008) **www.eptc-ieee.net**
December 9-12, 2008; Singapore
Abstracts due June 10, 2008
Contact: Dr. Tong Yan Tee, tytee@amkor.com

Electrical Design of Advanced Packaging and Systems (EDAPS 2008) **www.edaps2008.org**
December 10-12, 2008 COEX Conference Center Seoul, Korea
Papers due: July 31, 2008
Contact: S.M Yang, yangsm@ee.kaist.ac.kr (Office: 82-42-869-5458)

2nd Int'l Conference on **Thermal issues in Emerging Technologies, Theory and Applications** (ThETA2)
December 17-20, 2008 Cairo, Egypt **www.thetaconf.org**
Papers due: July 31, 2008
Contact: thetaconf@gmail.com

CONFERENCES IN 2009:

European Microelectronics and Packaging Conference & Exhibition (EMPC 2009) **www.empc2009.org**
June 14-17, 2009 Rimini, Italy
Abstracts due: December 31, 2008
Contact: Pragma Congressi, segreteria@empc2009.org

ESTC 2008

2nd Electronics System-Integration Technology Conference
1st – 4th September 2008, Greenwich, London, UK www.estc.biz

The IEEE 2nd ESTC Electronics Systems-Integration Technology Conference is on track to be an outstanding technical event and exhibition. ESTC-2008 will comprise 270 themed technical papers in six parallel oral tracks and posters. Posters will be displayed and also be presented.

The Technical themes at ESTC-2008 are: • Advanced Packaging • Emerging Technologies • Manufacturing and Test Technology • Modelling, Simulation and Design • New Materials and Processes • Power Electronics • Technology & Reliability for Micro and Nano Systems • Assembly of Alternative Energy Sources • Optoelectronics • Electronics system-integration for healthcare.

Special invited Sessions:

Asia-Pacific Photo-voltaics *will address: • "Third Generation Photo-voltaics" • "System-integration Strategies for co-Generation of Electricity, Heating and Cooling using Solar Photo-voltaic Modules" • "Building Integrated Photo-voltaics for Maximum Power Generation" • "The Intellectual Property Landscape for Photovoltaic Technologies"*

Standards *will address: "The Critical Standards for BT's 21st Century Network" • "EMC and Functional Safety Requirements for Integrated Electronics Systems" • "The Evolution of Standards in Industry"*

Prognostics and System Health Management for Reliability *will address: "Embedded Prognostics and Health Monitoring Systems" • "Integrated Vehicle Heath Management in the Auto Industry" • Aerospace and Electronics System Prognostic Health Management" • "Detecting Anomalies in Field Returned Laptops using Mahalanobis Distance"*

Greening the Blue Planet (public session): *• "Electronics, Energy and the Environment" Johns Hopkins University • "Interdependence of Marine Ecosystems and Climate Change" WWF • "Future Parks in Future Climates - scalable solutions" Ecologist Brecon National Park • "Talking Green about Nuclear" University of Cardiff*

Short Courses

Eight half-day short courses will be taught on Monday 1st September

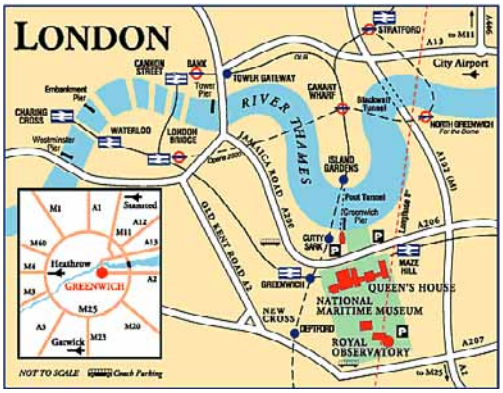
Opening and Keynotes

The Conference will be opened on Tuesday 1st September by Baroness Blackstone, Chancellor of the University of Greenwich. The Keynote Opening Address will be on "**Ambient Assisted Living**" by Dr. Nakita Vodjdani, Vice-President of the European Union AAL Association. The Keynote closing address will be by Prof. Peter Cochrane, entrepreneur and former Chief Technologist of British Telecom

Attendance is expected to exceed 500 international delegates.

The major technical exhibition will be held alongside the Conference – an excellent opportunity for suppliers of materials, design houses, circuit manufacturers to promote their products and reach potential customers.

ESTC 2008 will be held at Greenwich, a World heritage site and major maritime site on the banks of the River Thames in the magnificent city that is London. The Conference and Exhibition will be hosted by the University of Greenwich in the buildings of the former Royal Naval College. Plenary sessions will be in the Great Painted Hall – providing a wonderful ambience for the technical presentations.



Visit: www.estc.biz Information: **sinnadurai@estc.biz**

2nd International Conference on

Thermal issues in Emerging Technologies, Theory and Applications

ThETA2 Cairo, Egypt, December 17th – 20th, 2008

The **ThETA** conference objective is to address the growing impact of thermal issues on most of the advanced technologies including Microelectronics, Nanotechnology, Smart Materials, Micro-Electro-Mechanical Systems, Biomedical engineering, New Energies, Two-phase flow, and more.

Parallel to the conference, a set of workshops will be conducted, aiming at disseminating advances made in different areas to the academic and industrial public in Egypt, fostering network creation with renowned international research centers as well as giving an impulse to academic/industrial cooperation.

DEADLINES

Submitting abstracts:	**June 2nd 2008**
Notification of abstract acceptance:	**June 16th 2008**
Submitting full papers:	**Sep. 8th 2008**
Notification of paper acceptance:	**Oct. 6th 2008**
Camera Ready full paper:	**Nov. 3rd 2008**

Abstracts size: ~1000 words. Required data: Paper title, author(s) name(s) and affiliation(s), contact author email.
File formats: .txt, .doc, .pdf, .sxw
Send to **thetaconf@gmail.com**

CALL FOR PAPERS

Topical Areas:

* Thermal modeling of electronic systems
* Temperature aware computer systems design
* Cooling of electronic systems and data centers
* Micro and Nano scale heat transfer
* Modeling of multiple scale heat transfer problems
* Compact thermal models
* Thermo-mechanical analysis in electronic systems
* MEMS – multiphysical problems
* Computational methods in heat transfer
* Energy conservation
* Fuel cells
* Solid state energy generation / cooling
* Multiphase flow with heat transfer
* Thermal issues in biomedical engineering (diagnosis – therapy)
* Thermal Issues in Microfabrication Technology
* Thermal issues in new materials
* New experimental methods in heat transfer

For full CFP and further information:

www.thetaconf.org

ABSTRACT SUBMISSION DEADLINE EXTENDED TO JUNE 15TH.

33RD INTERNATIONAL ELECTRONICS MANUFACTURING TECHNOLOGY CONFERENCE IEMT 2008

4th-6th November, 2008 **Parkroyal Hotel, Penang, MALAYSIA**

ABOUT IEMT

The 33rd International Electronics Manufacturing Technology Conference (IEMT 2008) is an international event organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from CPMT Santa Clara Chapter. IEMT 2008 will feature short courses, technical sessions, and exhibitions. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation. IEMT 2008 is an international forum, providing opportunities to network and meet leading experts. Since the 1980's, IEMT has gained a reputation as a premier electronics materials and packaging conference and is well attended by experts in the field of electronic packaging and manufacturing from all over the world.

IEMT 2008 will feature short courses, technical sessions, and exhibitions. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation.

CONFERENCE TOPICS

The topics of interests are specific to electronics packaging, electronics materials, electronics manufacturing technology and reliability issues. Extended abstracts are being sought from, but not limited to, the following areas:

- Emerging Packaging Technologies
- Advanced Packaging
- Interconnection Technologies
- Manufacturing Technologies
- Surface Mount Technology
- IC Testing Technology
- Materials & Processes
- MEMS Packaging
- Electrical Modeling & Signal Integrity
- Thermal Characterization & Cooling Solutions
- Mechanical Modeling & Structural Integrity
- Quality and Reliability
- Chip-Scale Packaging/Flip Chip
- Wafer Fabrication Manufacturing

ABSTRACT AND PAPER SUBMISSION

Send 500 words stating clearly the purpose, methodology, results, and conclusions of the work, by **15 JUNE 2008**. Further information on the website:

cpmt.ieeemalaysia.org

10th Year Anniversary Celebration!

CALL FOR PAPERS

BIGGER Event! 4 Days Conference

ABOUT EPTC

The 10th Electronics Packaging Technology Conference (EPTC 2008) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter, sponsored by IEEE CPMT Society.

EPTC 2008 is a 4-day event in conjunction with 10th year conference anniversary celebration. It will feature technical sessions, short courses/forums, exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- Advanced Packaging & Emerging Technologies: *Wafer level packaging, 3D integration, embedded passives & actives on substrates, high power modules, high pin count flip chip packaging, RF-ID, SiP and other system integration technologies. Packaging solutions for MEMS, Bio-electronics, Automotive electronics, optoelectronics, organic and printable electronics.*
- Interconnection Technologies: *Gold and copper wire bonding and flip chip (eutectic/lead-free solders) on standard and copper low-k wafers, solder replacement flip chip (ICP, ACP, ACF, NCP), under bump metallurgy, 3D and through Si via connections, microvia and build-up technologies, fine pitch interconnects, nano interconnects.*
- Manufacturing Technologies: *Sustainable volume production of advanced packages and emerging technologies. New manufacturing technologies focusing on incorporating rapid product changes, cost, yield improvement, electrical/mechanical and environmental performance.*
- Materials & Processes: *Advancements in adhesives, encapsulants, underfills, solder alloys, ROHS compliant materials, flexible dielectrics, ceramics, composites, thin film processes on laminates, nano-materials and assembly processes, advanced material characterization techniques.*
- Electrical Modeling & Signal Integrity: *Modeling simulation & measurement for coupling, signal Integrity, power integrity & decoupling scheme analysis reflection, switching noise, EMI/EMC analysis on package & subsystems, RF modules, time & frequency domain measurements for advanced modules.*
- Thermal Characterization & Cooling Solutions: *Modeling & simulation methodology for thermal characterization of advanced packaging, modules & systems. Novel thermal management solutions. Enhanced air & liquid cooling techniques, Hot-spot management.*
- Mechanical Modeling & Structural Integrity: *Thermo-mechanical modeling at package, board & system levels. Modeling of delamination, moisture diffusion, hygrostress, thermal cycling, drop impact, bend, vibration, solder joint reliability and life prediction, measurement of material & interface properties, experimental verification.*
- Quality & Reliability: *Component, board and system level reliability assessment, interfacial adhesion, accelerated testing and models, advances in reliability test methods and failure analysis.*

Important Dates

10th June 2008	**Submission of abstract**
30th June 2008	**Notification of Acceptance**
30th August 2008	**Submission of manuscript**

Abstract and Paper Submission

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories for abstract review. All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by **10th June** 2008. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Special gift (webcam) will be given to the first 20 submitted abstracts which are subsequently accepted and published. Authors will be notified of paper acceptance and publication instruction by 30th June 2008. The final manuscript for publication in the conference proceedings is due by 30th August 2008. Selected papers will be published in IEEE/CPMT journals.

Outstanding Technical Papers

The conference proceedings is an official IEEE publication. Author(s) of Outstanding Technical Paper(s) and Best Student Paper will receive an award at the next conference.

Call for Short Courses

The conference program includes half and full-day short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings. Proposals for short courses can be submitted to techchair@eptc-ieee.net.

Call for Exhibition / Sponsorship

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. Potential exhibitors and sponsors may email secretariat@eptc-ieee.net for details.

Organized by

IEEE Reliability/CPMT/ED Singapore Chapter

General Chair	Technical Chair
Dr. Tong Yan TEE Amkor Technology, Singapore Email: tytee@amkor.com Tel : +65-62113403	**Dr. Teck Kheng LEE** Institute of Technical Education, Singapore Email : techchair@eptc-ieee.net Tel: +65-65805007

Sponsored by

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Conference information & contacts: Website: http://www.eptc-ieee.net Email: secretariat@eptc-ieee.net

Call for Papers

9th VLSI PACKAGING WORKSHOP in JAPAN (VPWJ)

Dec. 1 - 2, 2008 Kyoto, Japan

Bring your latest research results and share with the participants who are experts from industry and academia, and discuss with them.. The following areas of technology are of primary interest to the participants:

- System in a Package (SiP) - MEMS Packaging Technologies - Advanced Fine Pitch Packaging - Nano-Technology -3D Packaging & COC (Chip on Chip) - Micro Bumping Technology - Wafer Level CSP - Electrical Performance & Thermal Management - Packaging for Optoelectronics - Failure Mechanisms & Reliability Improvement - Packaging for Automobiles - Materials for High Speed Application & Wafer Processing - RF Components & Modules/RF Tags - Green Materials - Integrated Passives/Embedded Components - Assembly and Packaging Challenges for Cu/Low-k Chips - Laminated Materials & Processing - Emerging Technologies

Those who wish to contribute to the workshop should send a two-page abstract of a paper (including figures) to the Program Chair, Hiroshi Yamada at Toshiba, by **May 31, 2008.**

For full Call for Papers, see:

vlsi-pkg-ws.org

Polytronic '08

7th International IEEE Conference on

Polymers and Adhesives in Microelectronics and Photonics

Garmish-Partenkirchen, Germany 17-22 August, 2008

Please join researchers, engineers and scientists from around the world in mid-August 2008 to share knowledge and experience in Polymeric Materials for Microelectronic & Photonic Applications (POLY), Adhesives in Electronics, and Polymeric Electronics Packaging (PEP). The program will include keynote, invited and contributed presentations, as well as panel discussions. There are eight half-day tutorials and an IEEE Pavilion featuring technology exhibits and demonstrations.

For the Program and registration details, visit:

www.polytronic2008.com

Workshop on Accelerated Stress Testing & Reliability

October 29-31, 2008 Portland Oregon

Theme: "**Achieving Cradle to Grave Reliability using DFR and AST**"

The ASTR Workshop is an annual CPMT gathering of test and reliability engineers focused on accelerated stress testing and its relationship to reliability. It provides a forum for people from many different disciplines to network and discuss related issues and methodologies. Over the last few years, Accelerated Stress Testing & Reliability (ASTR) has been embraced by an ever widening array of worldwide companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market.

Completed Presentation Deadline: June 13, 2008

Registration is now open – save through Sept. 30th.

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- Electrical Modeling, Characterization, and Signal Integrity - Thermal-Mechanical Modeling and Characterization - Packaging Technologies for High Brightness LEDs - Flexible Electronics

EMAP 2008:

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Taipei Nangang Exhibition Hall

Joint IMPACT-EMAP Conference

Electronic Circuits Technology (PCBs)

- Material & Processes - Equipment & Processes
- Manufacturing Technology - Test & Inspection Technology - General Topics - Emerging Technology

The 400-500 word abstract should be submitted electronically through the conference website by **May 31, 2008.** Full paper is to be submitted electronically by August 31.

Visit: www.impact-emap.org

Plan to attend and participate!

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