Components, Packaging, and Manufacturing Technology Society Newsletter

IEEE

CPMT

The Global Society for Microelectronics Systems Packaging

Vol. 31 No. 2, June 2008 (ISSN 1077-2999)

www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

President's Column…..

Dr. William T. Chen
IEEE Fellow
President, IEEE CPMT Society
Santa Clara, CA, USA
wt-chen@ieee.org

Greetings!!!

Class of 2008

May and June have been the months to celebrate graduations from high schools and universities. It is the time when young men and women are waiting impatiently for the completion of commencement speeches so they can march to the podium to receive their hard-earned diplomas. For many high school graduates it is a time for selecting a future field of study. For many university graduates it is a time for joining a profession. It is a time of starting careers in a rapidly changing world, of globalization and new waves of growing middle class, of global warming and carbon footprint, of US$140 barrels of oil and competition for natural resources. In short -- it is a world of unprecedented technological revolution and unprecedented challenges.

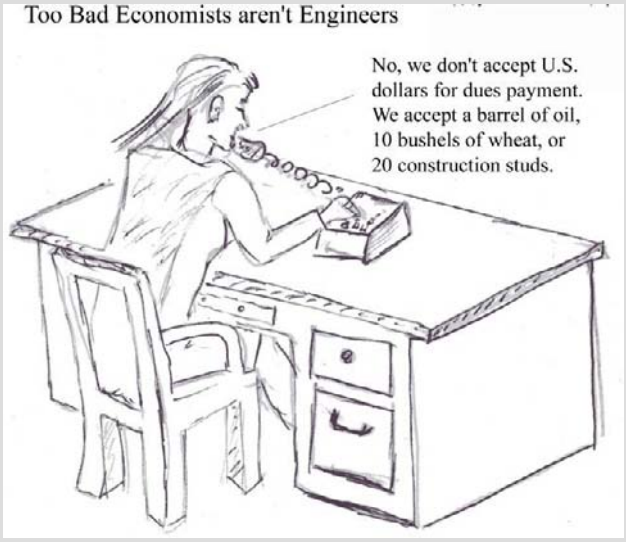
IEEE-USA has been proactive in raising the public awareness as to the importance of encouraging young students to choose science, mathematics, engineering and technology for their future field of study. The Semiconductor Industry Association (SIA) has given much space in its annual report on the need for talent in science and technology. Similar public sentiments and pronouncements have been echoed by the USA National Academies.

Closer to home -- how would one encourage a 2008 graduate to consider the electronics industry and our profession? An equally important question for this Class of 2008 is: once they have joined our profession, how do they prepare themselves to thrive and grow in this profession? What are the tools and knowledge sources to make their jobs fun, interesting, productive, satisfying and worthwhile? How can IEEE/CPMT help the Class of 2008 who are joining our profession?

Frankly I do not have an answer. IEEE and CPMT endeavors to support students and young professionals. Over the years, as they grow in their careers and take on more responsibilities and challenges, naturally their needs will change.

(Continued on Page 3)

Cartoon of the Month:



… By Dave Palmer

Science Fact: The standard Kilogram in France is slowly losing weight

Solution: Send it to America. It will put on some weight.

… By Dave Palmer

IEEE CPMT Society Newsletter
June, 2008
Index

JOIN AND SUPPORT CPMT SOCIETY
WWW.CPMT.ORG

CPMT Officers

President:	William T. Chen	+1-408-986-6505
VP (Technical):	N.Rao Bonda	+1-480-413-6121
VP (Conferences):	Rolf Aschenbrenner	+49-30-46403-164
VP (Publications):	R. Wayne Johnson	+1-334-844-1880
VP (Education):	Albert F. Puttlitz	+1-802-899-4692
VP (Fincance):	Thomas G. Reynolds III	+1-850-897-7323
Sr. Past Pres.:	Rao Tummala	+1-404-894-9097
Jr. Past Pres.:	Phil Garrou	+1-919-248-9261
Executive Director:	Marsha Tickman	+1-732-562-5529

Elected Board Members

2010:
Eric O. Beyne, Steve J. Bezuk, Kitty Pearsall, Eric Perfecto, Ephraim Suhir and C.P. Wong

2009:
Philip C.H. Chan, Paul D. Franzon, R. Wayne Johnson, Kwang-Lung Lin, Petri Savolainen, and Leonard W. Schaper

2008:
Vasudeva P. Atluri, Li Li, Dongkai Shangguan, Patrick Thompson, Klaus-Jürgen Wolter, and Kishio Yokouchi

CPMT Society Newsletter

Editor-in-Chief: Vasudeva P. Atluri, email: vpatluri@ieee.org
Tel: +1-480-554-0360, FAX: +1-480-563-0049
Associate Editor: Li Li, li.li@ieee.org, +1-480-413-6653
Associate Editor: Debendra Mallik, dmallik@ieee.org, +1-480-554-5328
Webmaster & e-Nsltr: Paul Wesling, p.wesling@ieee.org, +1-408-331-0114

CPMT Archival Publications

Publications VP:
R. Wayne Johnson, +1-334-844-1880; johnson@eng.auburn.edu
Editor-in-Chief & Director of CPMT Transactions:
Avram Bar-Cohen, Univ. of Maryland, +1-301-405-3173, abc@eng.umd.edu
Transactions on Components & Pkg. Technologies, Editors in Chief:
Ricky S.W. Lee, Hong Kong Univ of Science & Technology, +852-2358-7203; rickylee@ust.hk
Koneru Ramakrishna, Freescale, Inc., +1-512-933-2555; rama@ieee.org
Transactions on Advanced Packaging, Editor in Chief:
G. Subbarayan, Purdue University, Mechanical Engineering Dept., +1-765-494-9770; ganeshs@purdue.edu
José E. Schutt-Ainé, University of Illinois at Urbana-Champaign, +1-217-244-7279, jose@emlab.uiuc.edu
Transactions on Electronics Pkg. Manufacturing, Editor in Chief:
R. Wayne Johnson, +1-334-844-1880, johnson@eng.auburn.edu

Technical Committee Chairs

TC-Assy - IC and Package Assembly:
Martin Goetz, IBM, +1-919-486-2409, mgoetz@us.ibm.com
TC-ASTR - Environmental Stress & Reliability Test:
John E. Proulx, GM ATC, +1-310-257-3714, john.proulx@gm.com
TC-ECCC - Electrical Contacts, Connectors and Cables:
Jerry Witter, Chugai USA Inc., +1-847-244-6025, g.witter@ieee.org
TC-Ed - Education:
Rao R. Tummala, Georgia Tech., +1-404-894-9097, rao.tummala@ee.gatech.edu
TC-EDMS - Electrical Design, Modeling and Simulation:
Madhavan Swaminathan, Georgia Tech, +1-404-894-3340, madhavan.swaminathan@ee.gatech.edu
TC-EM - Manufacturing - Design & Process:
Walter J. Trybula, SEMATECH, +1-512-356-3306, w.trybula@ieee.org
TC-GEMP - Green Electronics Manufacturing and Packaging:
Nils F. Nissen, IZM, Berlin, +49-30-46403-139, nils.nissen@izm.fraunhofer.de
TC-HDSB - High Density PWB Packaging:
Yoshitaka Fukuoka, Weisti, +81-3-3475-0755, weisti.fukuoka@rose.zero.ad.jp
TC-M - Materials:
Rajen Chanchani, Sandia Labs, +1-505-844-3482, r.chanchani@ieee.org
TC-MEMS - MEMS and Sensor Packaging:
Eric Jung, IZM, Berlin, +49-30-46403-161, email: erju@izm.fhg.de
TC-NANO - Nano Packaging:
Rao Tummala, Georgia Tech., +1-404-894-9097, rao.tummala@ee.gatech.edu
TC-OPTO - Fiber Optics & Photonics:
Susan Law, Australian Photonics/OFTC, +612-9351-1960, Email: s.law@oftc.usyd.edu.au
TC-PEP - Power Electronics Packaging:
Douglas Hopkins, SUNY Buffalo, +1-607-729-9949, d.hopkins@ieee.org
TC-RF+W - RF and Wireless:
Craig A. Gaw, Freescale, +1-480-413-5920, c.a.gaw@ieee.org
TC-SP - Systems Packaging:
Cian O Mathuna, +353-21-4904350, cian.omathuna@tyndall.ie
TC-Test - Electrical Test:
Bruce Kim, Univ of Alabama, +1-205-348-4972, bruce.kim@ieee.org
TC-Therm - Thermal Management & Thermomech. Design:
Tony Mak, Dallas Semiconductor, +1-972-371-4364, t.mak@ieee.org
TC-WLP - Wafer Level Packaging:
Michael Toepper, IZM, Berlin, +49-30-46403-603, toepper@izm.fhg.de

Strategic Program Directors

Awards and Recognition: Kitty Pearsall, kittyp@us.ibm.com
Conferences: Rolf Aschenbrenner, wdb@engr.uark.edu
ECTC Integration: C.P. Wong, cp.wong@ieee.org
Educational Programs: Albert F. Puttlitz, a.f.puttlitz@ieee.org
Global Chapters and Membership: open
Publications: Paul B. Wesling, p.wesling@ieee.org
Student Programs: open
Technical Programs: N.Rao Bonda, r.bonda@ieee.org
Region 8 Programs: Johan Liu, johan.liu@me.chalmers.se
Region 10 Programs: Charles Lee, charles.lee@ieee.org

Standing Committee Chairs

Awards: Kitty Pearsall, kittyp@us.ibm.com
Constitution and Bylaws: Tony Mak, t.mak@ieee.org
Distinguished Lecturers: Albert F. Puttlitz, a.f.puttlitz@ieee.org
Educational Activities: Vacant
Fellows Evaluation: Ching-Ping (C.P.) Wong, cp.wong@ieee.org
Fellows Search: David W. Palmer, d.palmer@ieee.org
Rao Tummala, rao.tummala@ee.gatech.edu
Finance: Philip E. Garrou, pgarrou@rti.com
Long Range / Strategic Planning: Rao Tummala, rao.tummala@ee.gatech.edu
Nominations: Philip E. Garrou, pgarrou@rti.com

Distinguished Lecturers

Program Director: Albert F. Puttlitz
Lecturers: Avram Bar-Chen, H. Anthony Chan, Paul Franzon, George Harman, Badih El-Kareh, George Katopis, John H. Lau, Michael Lebby, Michael Pecht, Lue Martens, James E. Morris, T. Paul Parker, Karl Puttlitz, John M. Segelken, Ephraim Suhir, Paul Totta, Walter Trybula, Rao Tummala, Paul Wesling, C.P. Wong, and Ralph W. Wyndrum, Jr.

Chapters and Student Branches

Refer to **www.cpmt.org** for CPMT Society Chapters and Student Branches list

IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. For circulation information call IEEE Customer Service 800-701-4333, or FAX 908-981-9667.

2008 Deadlines for Submitting Articles:
February 25th, 2008 **May 25th, 2008**
August 25th, 2008 **November 25th, 2008**

Only Articles Sent to nsltr-input@cpmt.org will be included in the newsletter

Members-only Web (www.cpmt.org/mem/)
UserName: [available to Members --
Password: join CPMT!]

President's Column (Continued from Page 1)

Today the CPMT Value Propositions -- Publications, Conferences, Education, Technical Committees, Awards, Membership and Chapters -- are focused more on the needs of all professionals. What are the needs of young scientists and engineers newly entering the profession?

As I look back into the years when I first joined a big corporation with a freshly minted PhD degree, the technology landscape was much simpler and the technology life cycle much longer. Engineering was done in-house. I was fortunate that I found an informal network and support-system which grew with me over the years.

IEEE has the GOLD Program (Graduates of the Last Decade). There is a newly established IEEE Mentoring Connection Program (see the March 2008 Newsletter, page 5). CPMT has a Student Chapters program. Are these programs meeting the needs of the Class of 2008 CPMT Professionals? We do not know. Help us to understand by sharing your input and comments.

Send e-mail to me at **wt-chen@ieee.org** or to the CPMT Executive Office at m.tickman@ieee.org.

*****

CPMT Society News:

CPMT Publications

R. Wayne Johnson
Vice President of Publications

This is my first column as the newly elected Vice president of CPMT Publications. I am excited by this opportunity to serve the members of CPMT. We have a number of activities underway that I would like to outline for you.

1. Formation of a formal Publications Committee: CPMT has operated successfully with an informal publications committee; however, I have formalized this committee. The objectives of the committee are to establish Policies and Procedures so that our Transactions have a common 'rule book' and that we are operating per the policies and procedures required by IEEE. We are also establishing Guidelines to serve as a Best Practice Manual. This will be a valuable training tool for newly assigned Associate Editors and Editors-in-Chief. The Publications Committee will also be a conduit for suggestions from the CPMT membership to improve our publications. The members of the Publications Committee are:

   R. Wayne Johnson, VP Publications
   Avi Bar-Cohn, Society EiC
   Vasudeva P. Atluri, CPMT Newsletter Editor
   Ramakrishna Koneru, EiC T-CPT
   Ricky Lee, EiC T-CPT
   Jose Schutt, EiC T-AdvP
   GaneshSubbarayan, EiCTAdvP
   Ismail Fidan, AE T-EPM (2yr term)
   Ravi V Mahajan, AE TAdvP (2yr term)
   Luu Nguyen, AE T-CPT (2 yr term)

   The committee has three Associate Editors who will serve a two-year term. Through rotation of these three positions, we would like to involve many AEs over the coming years.

2. Publication Timeliness: The time-to-publish is a critical factor in the usefulness of an article and it is important to the authors. IEEE has established three metrics to monitor timeliness based on a two year window:
   a. 80% of papers in each journal have a submission to (electronic) publication time of less than 12 months.
   b. 50% of papers in each journal are reviewed and receive first decision within 120 days of submission. This time window will decrease on a graduated scale to 90 days over a five-year period, beginning January 2009.
   c. No journal will have a mean submission to (electronic) publication time of more than 24 months. This time window will decrease on a graduated scale to 15 months over a five-year period, beginning January 2009.

   We will be work diligently to meet (and exceed) these metrics. To do this, we need the support of everyone in the publication process: Editors-in-Chief, Associate Editors, Reviewers and Authors. The key activities will be for reviewers to return reviews on schedule and for authors to submit revisions and completed, final manuscripts quickly. While this will place additional pressure on CPMT volunteers, the results will be more useful publications. I will talk more about this in a future column.

3. Expand the Newsletter: The CPMT Newsletter is one important way of communicating with our membership. We envision expanding the Newsletter to include 2-4 technical or market-oriented articles per issue. This will provide our members with additional information and authors another opportunity to publish. The Newsletter would still contain all of the current Society information, but would be more 'magazine-like'. We are just beginning to work through the details. Suggestions and comments are welcome.

In closing, I would like to remind you that Publications are part of the communications process and communications should be two-way. If you have any suggestions for CPMT Publications, please feel free to contact me or any member of the Publications Committee.

R. Wayne Johnson, VP Publications, johnson@eng.auburn.edu

*****

Society Board Spends Introspective Evening

Submitted by Dr. Dave Palmer, Contributor,
IEEE CPMT Society Newsletter

About 3 dozen CPMT volunteers met Friday night June1st to review your Society and brainstorm on activities that will improve further your professional network. President William Chen presented the input and output of the February 14th IEEE review of our Society performed by other society presidents. This event occurs every 5 years and helps a society objectively pick future strategies and stop unproductive activities.

Our formal statement of Field of Interest contains all the topics featured at our conferences and in our Transactions. It covers broadly everything component, packaging, and electronics manufacturing engineers need in their career. It was very thoroughly rewritten about 10 years ago and is still relevant. Our core value is to "exercise, nurture, and grow our profession for the benefit of Society through knowledge advancement, innovations and im-

plementation of that knowledge and innovation". Within our mission statement are confirmations of our best opportunities and worst fears: "Our industry is fiercely competitive. Our technologies are advancing at a tremendous pace. The CPMT Society mission is to enable and support our Professionals (members and non-members) to excel." Within our vision is the statement "CPMT is the technical society…trusted and respected within and outside the profession as a premier society."

The review required a close look at any problems. "Declining membership is the major critical issue. … To recruit membership in the US and to grow membership in these fast growing regions of Europe and Asia while serving the global professionals is the critical issue for the CPMT Society."

To set the perspective for decision making, President William Chen pointed out that the CPMT Society participates in the US$250B semiconductor industry and the $1.2T electronics industry. The majority of our member are in companies such as Intel, IBM, Infineon, Motorola, Nokia, NEC, TSMC, QUALCOMM, and Skyworks. Others are in universities and research institutions. Most of our members come from Europe, Asia, and North America.

As a consequence our Society strategy must include:

1. Build and revitalize chapters where there is a good base of electronic and semiconductor industries. This adds to the goal of building a global community of CPMT Professionals. (recent examples include Austin Texas, Germany, pan-Scandinavia, and Poland).
2. Establish flagship conferences in Europe and Asia (such as ESTC and EPTC). Another example is the recent joint meeting announcement with the Chinese Packaging Society.
3. Facilitate Regional Advisory committees chaired by a CPMT Strategic director to focus on regional activities (budget included).
4. Help the many CPMT stakeholders around the globe realize their link to our society's goals so they better benefit and contribute. This can be accomplished through conferences, publications, technical committees, educational offerings, chapter activities, and awards and recognitions. We want all professionals in our technical areas to feel ownership in society activities.

Paul Wesling discussed how many of our activities make a big immediate difference but do not have follow-up attention to result in long range member assistance. For example, we hold a key technical conference but then the society doesn't have any way for attendees or authors to continue participating in the knowledge sharing.

Kitty Pearsall emphasized the special need of the young beginning professionals who don't know yet how to plug into the CPMT network. We should particularly target young professionals in our future activities.

There was a long discussion on how the conference fees (normally paid by the engineer's company) could be used to pay some of the IEEE dues, which is a big hurdle for many professionals. Discussion revealed that there are many ways to "join" CPMT without costing much, but we do not provide an easy way to find out about these ways.

The group then split into regional teams to assembly an action list for making CPMT Society more immediate for members in their region.

*****

IEEE CPMT Society Board of Governors Goes Disney

Submitted by Dr. Dave Palmer, Contributor,
IEEE CPMT Society Newsletter

On the Saturday right after ECTC, 35 of your representatives participated in the Board of Governors meeting at the Disney Contemporary Resort in Orlando, FL USA.

Constitution: Executive Administrator Marsha Tickman announced that the changes to our Bylaws and Constitution had finished their final step of member approval and are now in place.

Appointments: President William Chen announced the appointment of Koneru Ramakirshna as a new Member-at-Large. He replaces Wayne Johnson who has taken the Vice President of Publications position. Steve Bezuk was approved as the next Strategic Director of Membership and Chapters. The President then presented Ralph Russell with an award for his more than a decade of contributions to the Society.

Regional Strategy Reports:
Charles Lee reported for Region 10. They are investigating the use of workshop and conference fees to be used to pay member IEEE/CPMT dues as well as other less expensive forms of affiliation. They are considering more involvement with student groups since this is working well for other engineering societies. A Mandarin version of the CPMT website is being developed. Charles reported that a student reception at one recent Region 10 conference was well received and will be copied at other meetings. Another push will be to have CPMT Technical committees meet in association with some of the meetings to get double value for everyone's travel. In the direction of giving recognition to our members, he reported that the Tokyo Chapter is now recognizing student achievement. The Region 10 advisory committee includes Kishio Yokouchi (Japan), Lin Kwang-Lun (Taiwan), William Chen, Philip Chan, and Ricky Lee (China), Joungho Kim (Korea), Philip Chan (Hong Kong), and Charles Lee (Singapore Malaysia).

Eric Beyne reported for Region 8. In an effort to make new membership less expensive they are trying to find out all the features of affiliate membership which is about half the normal expense. They are also looking into the longstanding Memorandum of Understanding between engineering societies since CPMT is so multi-disciplinary. They suggest we should have a policy to give CPMT speakers at a conference a lower fee than a non-CPMT speaker. They see the best benefits in having local chapters sponsor seminars, workshops and build networking. There is little ex-

pense for professionals in the local area to participate and become involved. Ten chapters already exist in Region 8 with some a mix of IEEE societies. There should also be regional level conferences/workshops that help expand networking but are still not international. Examples mentioned include ESTC and the Eurosime workshop. There are some promising activities in the Middle East: a thermal conference in Egypt and IMP in Israel.

Bahgat Sammakia reported for North America. With a goal of attracting and retaining participating professionals, we must come up with a list of compelling and member-serving reasons to participate in CPMT. We must pick approaches that last beyond any one person's activity. The first action is to define in detail the benefits of both membership and participation not just with a simple list, such as: ECTC, Xplore, Newsletter, access to tech leaders, publication opportunity, leadership training, opportunity to help others, access to restricted web sites, and opportunity for formal peer recognition. It was suggested that this list be sent to members that fail to renew. The next step is to identify the most likely professionals with affinity for CPMT by compiling lists of authors and attendees to our conferences, authors to our Transactions and related magazines, lists from industry and institutions (ECA & EIA), users of our educational material, and member networks. The third priority is to energize the student IEEE chapters with speakers and technical contests.

Finances:
Treasurer Tom Reynolds reviewed the current year budget and the projections for next year. Although our Society has large financial reserves, he did warn that conference attendance in general is trending lower (transportation costs and slow economies) and that conference costs were rising so that parts of our future income are at risk. We have about $3.6M in our reserves but with current financial market performance this is not providing much income.
The subscription price for our Transactions for non-members will go up slightly in accordance with IEEE market survey results. We are spending a bit too slow against our targets this year but there is no reason to panic.

ECTC report:
C. P. Wong and Torsten Wipiejewski reported on the just completed ECTC. Submitted abstracts totaled 621 with 48% from industry and 52% from universities or institutes. This was 25% more than last year. From these abstracts 344 were selected for presentation, 252 oral and 92 with posters. Europe supplied 13%, Asia 28%, and North America 59%. Sixteen professional development courses were given with 340 registered students (up 16% over last year). The technology Corner attracted 83 exhibitors. Three evening panel sessions were held. There were approximately 950 paid attendees from 17 countries.

Education:
Al Puttlitz, VP Education, discussed the results of the Motorola Graduate Fellowship paper, the IEEE-CPMT Ph.D. Student Fellowship paper, and the Intel Best Student Paper competition. He pointed out that 93 student abstracts had been submitted of which 48 were accepted. He was particularly interested in having the Board raise the limit on student travel reimbursement so that more students would have the opportunity to compete.

Al Puttlitz also presented two new CPMT distinguish Lecturer candidates for the Board to vote on. Both Nihal Sinnadurai and R. Wayne Johnson were approved. John Segelken and Paul Totta have announced their departure from the lecture tour.

There was much discussion of possible new corporate sponsorship of prizes and fellowships. A committee with academic experience was set up to propose the best way to use new funding in the student awards area.

Awards:
Kitty Pearsall reviewed our award system and the experience this year. She would always like to have more nominations particularly from Region 8 and 10 but was quite pleased by the choice her committee had this year, with 2-3 candidates for each award. Her committee: Charles Lee, Ning-Chin Lee, Kwang-Lun Lin, Petri Savilainen, Ephraim Suhir, Klaus-Jürgen Wolter, and Ralph Russell. We will try to get the nomination material in the hands of more members sooner this coming year.

There was some discussion on using the evaluation process for the Electronic Manufacturing Technology Award to get visibility from the CEO and result in more industrial activity and keynote addresses.

Kitty presented a plan for CPMT Regional Awards for Society contributions and the Board agreed after much discussion and lunch.

Len Schaper discussed the past year IEEE Field Award process resulting in Karl J. Puttlitz and Paul A. Totta winning for their many years of effort on pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages. The next award deadline is January.

Publications:
Wayne Johnson reviewed the results of the 5-year TAB periodical review of CPMT. Much of the concentration was on the timeliness of publication, mostly the time from paper submittal to publication.

The first response was that CPMT formed a formal publications committee rather than the informal concerned participants of the past. The committee has ten members including the editors of the Transactions and Newsletter. In addition, CPMT is documenting our publication policies particularly for the benefit of new associate editors who may not have a lot of experience in the CPMT culture.

TAB suggested one editor-in-chief in contrast to our shared responsibility approach. We are thinking about that. Remember CPMT does not pay editors; it is an act of love which is best shared.

TAB wanted to make sure that a paper published in one of our conference proceedings does not get republished in a Transaction with no new technology. At first this seems strange since proceedings are not archival even though some of the papers are complete enough to be archived. However, with the new web search capabilities it does not look professional to have two identical papers pop up on the internet with different addresses.

We will start growing more associate editors and promoting them to guest editors for special transactions sections rather than bring-

ing in guest editors from the wilds and then after trial by fire making them associate editors.

In these new times of mostly electronic (not paper) transactions it is no longer clear that 3 Transactions are needed to cover the breadth of CPMT. One no longer worries so much about a thick publication or not being able to find papers of interest to you in a huge table of contents.

Timeliness goals: in looking at papers over 2 years, more than 80% must have been published in less than 12 months. In addition, 50% of submittals must have the first decision (reject or edit) occur within 120 days. For the last year we have had an IEEE staff expert help us monitor the paper flow and push the 113 delinquent papers through the system. Only 17 papers remain in the system that started before 2006.

A workshop to help authors is being offered at some of our conferences. This "Best Practices" workshop was offered at ECTC and attracted about 30 attendees. The newsletter will be expanded to include technical papers and perhaps so advertising of interest to members.

Wayne proposed the Society support a part-time publication expert to work on the newsletter expansion, laggard Transactions papers, and provide communication amongst volunteers. Resolution passed.

Conferences:
Rolf Aschenbrenner, VP Conferences, summarized that CPMT held 26 meeting this year compared to 30 last year. The Polytronic and Portable conferences decided to merge and will meet in Garnisch-Partenkirchen Germany in August.

The ESTC 2008 will be in September in Greenwich, Britain with 270 papers and 16 special presentations.

Phil Garrou and Paul Franzon proposed a new 3-D Silicon international workshop for April 2009. This workshop may rotate to Europe, Asia, and North America. The scope of the meeting is still flexible. The Board approved this initiative.

Technical Committee:
Rao Bonda, Technical VP, reviewed the status and web pages of the various technical Committees. He pointed out that TC-12 has modernized their web presence and is working with all the other committees with this goal. TC-11 has a new title – Electrical Test – Semiconductor Wafer and Packaging.

*****

IEEE CPMT Society Field Award for 2008

Submitted by Dr. Leonard Schaper, Board of Governors – Member at Large, IEEE CPMT Society

The 2008 IEEE CPMT Field Award was presented on May 29, 2008, at the ECTC Conference in Orlando, Florida. The 2008 award was given to:

KARL PUTTLITZ SR. (F'IEEE) - President, Puttlitz Engineering Consultancy, Wappingers Falls, NY USA; and
PAUL A. TOTTA – (non-member) Retired, IBM East Fishkill Facility, East Fishkill, NY, USA,

"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages"

Karl Puttlitz and Paul Totta were part of a small development team at IBM in the early 1960s that initiated the development of the flip-chip interconnection. They established this new interconnection technology in the IBM System 360 computer line. While it has remained the primary interconnection method for IBM, these packaging technologies are found around the world in handheld products, i.e. cell phones, in advanced computer systems from laptop machines to mainframes, and in a wide variety of telecommunication equipment. Flip chip technology developed by this team is now practiced throughout the industry and has been an enabler for advanced systems and miniaturization of electronic packages and handheld systems.

Paul worked on the device side or the interconnection in an effort called Solid Logic Technology (SLT). Key to the advancement of the technology was the concept of using glass passivation on silicon devices. The glass film avoided corrosion and degradation of the device and freed the package from hermetic encapsulations which were expensive and not so reliable. As a young metallurgist entering electronics for the first time, he co-invented the concept and process for creating a metallization pad through the glass, evaporating high-Pb solder and using "homemade" copper balls as contacts and connections between the silicon device and its hybrid, thick film package. The cost of chips was reduced by orders of magnitude and the vibratory-bowl random handling of chips facilitated highly productive, low cost manufacturing. The attached chips were much more rugged and reliable than the hermetically sealed, wire bonded counterparts.

Karl worked on solder-dam development post-fired, glass thick films deposited near the ends of conductor lines forming pads to which the chip solder bumps were reflowed. The dams prevented the molten solder from running down the conductor lines during chip reflow, i.e. prevents solder joint collapse – hence the term "controlled collapse chip connection" or more popularly, C4 joint.

The early ceramic circuit boards required thick-film technology and integrated circuit elements which would be a compatible platform for the C4 devices. Karl developed both the thick-film technology used by IBM and formulations used for its integrated circuits printed on ceramic chip carriers: conductor lines, resistors, capacitors, inductors, humistors, and thermistors.

Thus, IBM's System 360 computer line was very successful because of these packaging and interconnection innovations as well as the system concepts. However, the interconnection system required many innovations on both the device side and carrier

side. As a team, Paul and Karl worked the system out using some of the examples of technology developments below.

Paul's metallurgy background led him to approach problems with semiconductors differently than the EEs and physicists who were on the multidisciplinary team. For instance, the solid-state alloying at the AI contacts, the "penetration problem," was relatively easy for him to understand and explain. It was initially fixed by "doping" AI with Si to satisfy the solid solubility of Si into Al during thermal processing.

As IBM evolved the chip technology from single, discrete devices to integrated circuits, new problems were discovered in the thin film wiring such as electromigration opens of the wires. This problem was solved by colleagues who invented copper doping of the AI. This added orders of magnitude to the current-carrying lifetime of the chip wiring. But then, the Cu-doped AI began disappearing during processing in the line. It was his privilege to determine that the "missing AI" in the line was actually a corrosion phenomenon. The solution to the problem essentially stopped the manufacturing impasse and got him a contribution award as well as reputation of "chief troubleshooter." About this time he was invited to manage the Device Metallurgy Department in the laboratory. One of his first efforts was to replace the AI on AICu-based chip wiring with Ag and Cu wiring. This high conductivity chip wiring was not only more conductive, but more electromigration-resistant as well. IBM's first patent featuring Cu wiring was a Totta/Mutter patent of 1970. Flip chip core drivers were actually made and shipped with this technology, clearly a forerunner of what was to come in the 1990s.

By 1972 Paul took responsibility for chip passivation, and then RF sputtered SiO_2, and multilevel wiring of chips. This included solving via hole problems, planarization techniques and reliability issues. Along with multilayering came the opportunity for "area array". The bump counts rose to about 100 C4s. When flip chips on the alumina substrate grew in size, the low cycle thermal fatigue of the solder became an issue. One of his departments spent much effort in understanding solder fatigue and fracture. This led to shape factors, alloy changes (e.g. Pb In), and other things to extend lifetime.

In the 1970's IBM devised multilayer ceramic (MLC) chip carriers capable of wiring out flip chips with a full array of I/O solder bumps. The chips are directly reflowed to micro sockets formed by co-fired molybdenum vias that intersect the surface, and plated with electroless nickel to render them solderable. However, the electroless nickel, plated from a hypophosphite-based bath, exhibited several unacceptable conditions resulting from phosphorous entrained in the nickel deposits. Cracks occurred due to high internal stresses created; and worse, a nickel phosphide (Ni3P) layer, not wet by solder formed at the solderlmicrosocket interface. This layer caused some solder joints to separate at that interface as identified in Karl's award-winning 1990 IEEE Transaction paper.

His work defined the need for change and he helped provide the innovation with his co-invention of an electroless cobalt plating bath. It demonstrated the feasibility of utilizing an organic boride reducing agent (DMAB), in place of the hypophosphite. Henceforth, a nickel bath was formulated based on DMAB, similar to the cobalt bath. The DMAB-based nickel bath was successfully utilized for several decades for all of IBM's MLC flip chip products.

Karl played a major role in the invention of a method to salvage electrically-good flip-chip devices by restoring the solder bump array subsequent to a reflow attachment and removal from a chip carrier. This was a significant innovation, since electrically-good devices are very scarce in the early development stages of a device program.

Chip replacement capability was a key to IBM's strategy of using highly populated (with 9 to 133 chips) multichip modules (MCMs) for its mainframe computer CPUs. This required the capability to replace one or more chips on these MCMs in order for the computer programs to be economically viable. Replacement allowed meeting yield targets and field upgrades with enhanced chip sets. Karl provided the solution by leading a small development team that invented the flip chip replacement tooling and processes that IBM utilized in its manufacturing plants worldwide for more than 25 years starting in the late 1970s

Replacement consisted of a variety of technologies (e.g. mechanical, ultrasonic, hot gas and infra red heating that allowed individual flip chips to be removed from a closely-spaced array of chips mounted on a MLC MCM, to dress the solder at the removal site, and then, either locally or globally, reflow a replacement chip. These operations were achieved without physical damage or an adverse reliability impact on the replacement chip, neighboring chips, nor the chip carrier.

As a natural result of their collaboration, Paul and Karl co-edited and co-authored a handbook that covers all aspects of area-array interconnects at both the first and second levels of assembly.

Subsequently Paul and Karl worked to continually improve the materials, processes and reliability of the flip chip interconnections system as noted below.

Paul was appointed an IBM Fellow in 1987 in recognition of his many activities in chip and package interconnection technology. The position gave him the freedom to reinvent the C4 process from a metal mask evaporation process to a sputtered seed layer/plating process. The timely reinvention allowed IBM to continue using C4 interconnection because the old process was not extendable to 300mm wafers and fine pitch bumps with counts of up to 10,000 per chip.

All during Paul's time with IBM, from 1971 until retirement, he participated in ECC and ECTC symposia activities. He was a speaker, often session chair, head of interconnections and short course teacher. It was always a rich and rewarding experience. Since retirement from IBM in 1999, he has been invited back to their Corporate Technical Recognition Event three times for recognition:

1. Outstanding Contribution Award for the reinvention of C4 process in the 90s. (2001)

2. A Patent Portfolio Award for multilayered semiconductor wiring which was sputtered and RIE etched; later used extensively throughout the semiconductor world. (2003)

3. A Patent Portfolio Award for a tungsten contact stud structure and process also extensively used by IBM and the world. (2005)

Karl went on to devote his career in providing sustained technical innovations and technical leadership that greatly contributed to the success of this unique interconnection scheme and other packaging innovations. Karl is recognized throughout the world as a lending expert in microelectronic packaging, and particularly for his contributions to area array technology at both the first (chip-to-carrier) and second (carrier-to-card) levels of packaging.

Karl's technical contributions and leadership are widely recognized. IBM honored him with a Corporate Outstanding Innovation Award, and was elected a Fellow of the American Society of Materials (ASM) International and also an IEEE Fellow "-- for developments and leadership in the microelectronic packaging sciences, particularly area array interconnection technology."

Other Achievements: Karl has made numerous contributions to second level (component-to-board) interconnection technology as well, a few examples are noted.

1. CBGA Dual Solder System: Karl led the effort to define and optimize IBM's dual solder system used for ceramic ball grid array components whose fixed standoff height provides greatly enhanced reliability.

2. Replacement of Components Mounted on PCBs: Karl was a key participant in defining a method and tooling to locally remove surface mount (SM) components like CBGAs from even very thin printed circuit boards (PCBs) and locally reflow replacement components.

3. Rework CBGA/CCGA Components: Karl led a team that defined the method and tooling to rework both CBGA and CCGA components allowing one or more balls/columns to be replaced to enhance yields and reduce costs.

4. National Test Specification: Co-authored "The Production Ball Grid Array (BGA) Socket Test Specification," adopted as a national standard by the Electronics Industries Association (EIA): IS- 701, 7/96. Co-author: T. Peel, Contech Research, Inc.

5. Lead-free Technology: Karl had corporate responsibility working with all aspects of the business (development, purchasing, manufacturing, marketing, quality, legal, etc.) for compliance of all IBM products worldwide with Pb-free legislation. He initiated the program at IBM in 1999 and served as Corporate Program Manager until his retirement in 2004. He played a major role in obtaining flip chip and other exemptions from the European Union Commission favorable to the industry. He is the co-editor/co-author of a lead-free handbook, and actively involved in Pb-free solder joint development.

In summary, Paul and Karl made many vital and sustained contributions in advancing the state-of-the-art of flip chip technology in its infancy. They by necessity worked as a very successful team to develop complimentary thin film and thick film technology to make the C4 interconnection system successful for IBM. Now this technology in the form of flip chip interconnection has spread throughout the industry and remains a major driver and enabler for new products and packages around the world.

*****

Call for Candidates

Submitted by Ms. Marsha Tickman, Executive Director, IEEE CPMT Society

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of this Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways: either by the Society Nominating Committee, or by petition.

This year's election is the fourth in which members-at-large will be elected to achieve totals proportionate to the geographic distribution of CPMT members. Voting members will elect members-at-large from within their Region only (that is, members in Region 8 will vote for members-at-large from Region 8, etc.)

Elected Members of the Board of Governors must be willing to attend two annual Board meetings and participate actively in areas of their interest (publications, conferences, membership development, chapter development, etc.) The term of office for this election is 1 January 2009 through 31 December 2011.

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can become a candidate via petition by following the procedures below.

- Prepare a petition that contains your name, member number, and statement of your qualifications for office.
- Provide lines for signatories. Each line should include space for a printed name, member number, and signature.
- Have the petition signed by a MINIMUM of 46 CPMT Society members in good standing (Student grade members are not eligble to sign.)
- Submit your petition by mail no later than Friday, 25 July 2008 to:

CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA

OR

- Request establishment of electronic petition process, allowing signatures to be collected on-line.

You must contact Marsha Tickman to implement electronic petition process.

Membership status of all signatories will be validated. It is suggested that you gather more than 46 signatures in order to assure meeting the minimum required number of valid signatures.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at m.tickman@ieee.org.

*****

Chapter Reports:

IEEE CPMT Polish Chapter

Submitted by Artur Wymyslowski, Secretary of Poland CPMT chapter

The IEEE CPMT Polish Chapter is located on teritory of Poland and its main aim is to bring together different experts and users of electronic packaging for the common benefit. It is the Chapter of IEEE Poland Section. The website for the section can be accessed at www.ieee.pl/index.php?lang=en&MMenu=main.

The IEEE Components, Packaging and Manufacturing Technology (CPMT) Society is the leading international forum for scientists and engineers engaged in the research, design and development of revolutionary advances in microsystems packaging and manufacture. The CPMT Society can help with technical excellence, professional development and international networking opportunities, through its journals, conferences and workshops, committee activities, local chapter events, educational programs and awards.

IEEE CPMT Polish chapter was started in 2007 in Wroclaw, which is located in the south-west part of Poland. Currently the chapter consists of 10 active members from different background and experience.

The current chapter board consists of three persons:

- President: dr hab. eng. Jan Felba prof.
- Vice-president: dr eng. Ryszard Kisiel
- Secretary: dr hab. eng. Artur Wymyslowski

IEEE CPMT-Poland chapter organizes anually a number of events devoted to:

1. Conference organization
2. Lectures and seminars
3. Courses

On 6th of March 2008 an agreement between CPMT-Poland chapter and IMAPS Poland-chapter was signed on bilateral ccoperation. The main goal of the signed agreement is to:

1. expand the knowledge on microelectronics
2. support the acheivements of the both parties
3. organize anually the common scientific-technical Conference

Picture of agreement signing event between officers of CPMT-Poland Chapter and iMAPS-Poland Chapter

On the *21-24th of September 2008* there will be orginized a scientific conference *IMAPS-CPMT poland conference*. The conference will take place at *Warszawa-Pultusk.*

The organizing institutes:

1. IMAPS-Poland chapter (http://www.imaps.org.pl/about/english.php)
2. CPMT-Poland chapter (cpmt-poland.info/)
3. Institute of Electronic Materials Technology (www.imio.pw.edu.pl/en/main.html)
4. Warsaw University of Technology (eng.pw.edu.pl/)
5. Committee on Electronics Telecomunication of Polish Academy of Science (keit.pan.pl/)

The conference topics include:

1. Hybrid and Semiconductor Technology
2. Design Methods and Computer Simulations
3. Electronics Materials and Components
4. Microcircuits Applications
5. Thick-Film and Thin-Film Sensors
6. Packaging and PCB
7. Quality and Reliability Evaluation
8. Thermal Management
9. Optoelectronics and Photovoltaics
10. Education in Electronics

For more information about the conference, access imaps2008.imio.pw.edu.pl/.

In order to contact the IEEE CPMT - Polish chapter, please use the following address:
IEEE CPMT - Polish Chapter
Wroclaw University of Technology
(www.pwr.wroc.pl/en_main.xml)
Faculty of Microsystem Electronics and Photonics
(wemif.net/?c=a&s=0&lng=en)
ul. Grabiszynska 97
53-439 Wroclaw
Poland

or use one of the following e-mail adresses:

- President: dr hab. eng. Jan Felba, prof. - jan.felba[at]pwr.wroc.pl
- Vice-president: dr eng. Ryszard Kisiel - r.kisiel[at]imio.pw.edu.pl
- Secretary: dr eng. Artur Wymyslowski - artur.wymyslowski[at]pwr.wroc.pl

*****

IEEE CPMT Society Phoenix Chapter Update

Submitted by Mr. Victor Prokofiev, IEEE Phoenix CPMT Chair 2007

In the year 2007 IEEE Phoenix CPMT chapter was very rich on events and other activities. The chapter provided very diverse learning opportunities to all engineers in the Phoenix area, which is a very important for member professional development. During the year the chapter held twelve technical presentations, organized one “Backend Wafer Processing Technologies” tutorial, and co-sponsored “Emerging Device and Packaging Technologies” workshop with IEEE WAD (Waves and Devices) Phoenix Chapter. After investing a lot of effort in organizing these events the chapter officers were pleased to learn as more than 400 people

found time in their busy life and attended the chapter events. In addition to that, the chapter also provided technical seminar attendees with free refreshments and hot meal. In order to keep pool of engineering talents sound, the chapter continues to sponsor scholarship program for IEEE Student Members within IEEE Phoenix Region. Special thanks to all IEEE CPMT Phoenix Chapter officers for volunteering, Freescale Semiconductor Corporation for providing Chapter with meeting rooms, and all other people who supported our activities!

*****

IEEE CPMT Society Student Branch at Georgia Institute of Technology

Submitted by Mr. Dean Sutter, Director, Business Operations and Infrastructure, Microsystems Packaging Research Center, Georgia Institute of Technology
dsutter@ece.gatech.edu

The IEEE CPMT Student Chapter at Georgia Institute of Technology (GIT) was the first CPMT Student Chapter formed. It was formed in May 2001 with the support of Professor R. Tummala, Director of the Microsystems Packaging Research Center (PRC), and Professor M. Swaminathan, Deputy Director of the PRC who also serves as the Chapter Faculty Advisor.

The GT Student Chapter leaders are Jin Liu (President), Nevin Altunyurt (Vice President), and Dhanya Athreya (Secretary / Treasurer).

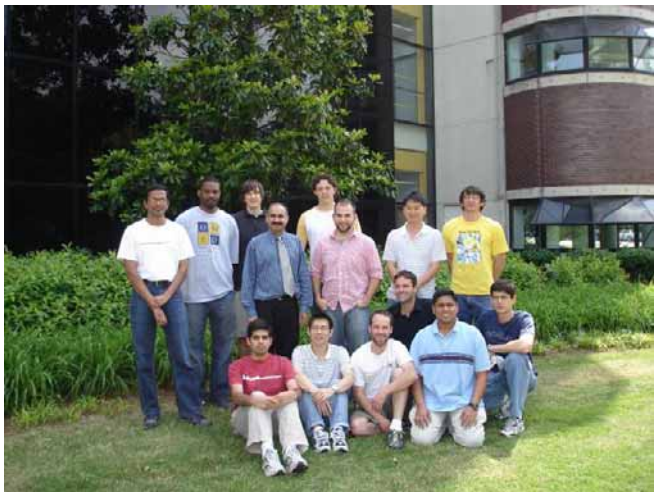
Jin Liu

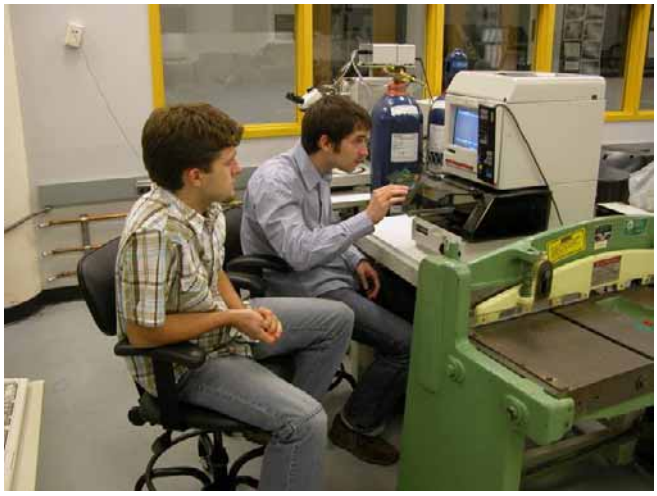
Nevin Altunyurt

Dhanya Athreya

The Chapter co-organizes with the PRC Student Council. The Chapter's charter is to promote the awareness of the various electronics packaging education and research at GIT, while at the same time; it provides a center of gravity for social activities for students in the electronics packaging field.

Based on the broad spectrum of technologies needed to realize electronic packages, the Chapter student body is quite interdisciplinary in its composition. Areas of study and research include electrical and mechanical design, material development, characterization, and synthesis; substrates with high density wiring and microvias, embedded passives components, RF, MEMs, interconnects, optics, thermal management, reliability, and electrical test to name a few. As a result, a majority of the students are from the School of Electrical and Computer Engineering. However, there are many students from the School of Materials Science and Engineering, the School of Mechanical Engineering, as well as the School of Chemical Engineering. Additionally, students are involved with other research centers on the campus such as the Microelectronics Research Center (MiRC), the Interconnect Focus Center (IFC), the Georgia Electronic Design Center (GEDC).





Dr. Sitaraman (ME) and Student Interns from Dresden Germany

Students and Industry attendees at PRC 3DASSM Workshop

ECTC has been a primary vehicle for the Chapter students to get visibility externally of GIT and GIT typically has a strong presence. This year at ECTC 2008, GIT presented 27 papers, had 11 student posters, this in addition to having a student booth for the 2nd consecutive year. Additionally, Mr. Tapobrata Bandyopadhyay has been announced as the winner of the 2008 IEEE-CPMT Ph.D. Student Fellowship.

Mr. Bandyopadhyay's paper, "Microwave Design & Characterization of a Novel Nano-Cu based Ultra-fine Pitch Chip to Package Interconnect" presented, for the first time, the RF/Microwave design, modeling, parametric optimization and characterization of interconnect transitions for a Nano-Cu based chip-to-package interconnect system for microelectronics packaging applications. His work demonstrated lower electrical parasitics and transition losses (for Chip-on-Chip and Chip-on-Package configurations) using Nano-Cu interconnects, as compared to conventional Solder bumps and Gold stud bumps. Congratulations goes out to the co-authors Gaurav Mehrotra, Georgia Tech, Dr. Mahadevan K. Iyer, Infineon Technologies, Dr. P.M. Raj, Georgia Tech, and Profes-

sors Madhavan Swaminathan and Rao R. Tummala, Georgia Tech. Mr. Bandyopadhyay will receive a one-year Fellowship of $10,000 towards his Ph.D. studies in 2008 and 2009 and is eligible for up to $300 towards his travel expenses that are not paid from another source. Congratulations Tapobrata and team!

Student Chapter Booth @ ECTC Conference

To improve promotion of packaging technology awareness, the Chapter established several different lecture series. These included; a student lecture series, a student research promotion program, and a distinguished lecture series.

Several distinguished speakers from industry have been invited to give seminars in the year 2007~2008 to expose the students with the state of the art development in packaging field from the industry. The topics include 3D IC Integration by Dr. Philip Garrou, Electrostatic Protection of Semiconductor Devices by Dr. Duvvury of TI, and Integration of 3D Stacked DRAM and Logic Devices by Mr. Motohashi of NEC. The seminar series greatly broadens the scope of students' packaging knowledge from an industry perspective and it helps students to keep up with the technology developments in industry.

PRC students Nithya Sankaran, Tapobrata Bandyopadhyay, and Guarav Mehrotra tending the PRC booth at ECTC

Student Poster Session

Student Research Opportunities Meeting

Students Participate in Industry Workshop

Dr. Philip Garrou's seminar in 2007

Social events are also an important part of student chapter's activities at GT. Last spring the Chapter invited the faculty, the research staff as well as the students from across the schools to a spring picnic. During the picnic, students had the opportunities to talk with the faculty members as well as the research staff about things they are interested, from research to the life at school. It was a great experience, especially for those who just entered the field of packaging.

Dr. Duvvury's seminar on electrostatic protection of semiconductor devices in 2007

Audience at Dr. Philip Garrou's seminar in 2007

Spring picnic held at Georgia Tech

IEEE CPMT Society Newsletter
Send inputs, suggestions, and articles by email to nsltr-input@cpmt.org
….. Editor

Spring picnic held at Georgia Tech

*****

News from the IEEE CPMT SBC | Politehnica University of Bucharest

Submitted by Alexandra Iulia Potop, Press Officer IEEE CPMT Student Branch Chapter of Politehnica University of Bucharest, Romania—alexa.potop@cetti.ro

University Politehnica of Bucharest, the Faculty of Electronics, Telecommunications and Information Technology, and the Electronics, Telecommunications and Computer Science University of Pitesti organized with great success, between 10 – 12th of April, the 17th edition of The Interconnection Techniques in Electronics professional student contest TIE 2008.

The central objective of the contest was emphasizing the participants' knowledge in the field of computer aided design of electronic modules.

Based on its organizational structure, including public evaluation of technical solutions found by students, the contest promotes, in a total fair-play spirit, competition and professionalism among the participants interested in the area of microsystems and electronic modules packaging.

The poster of the TIE 2008 contest

This year the contest, hosted by the University from Pitesti, gathered nearby 40 students from ten Romanian Universities: "Gh. Asachi" Technical University – Iasi, "Politehnica" University – Timisoara, Technical University – Cluj-Napoca, University – Pitesti, North University – Baia Mare, "Stefan cel Mare" University – Suceava, Politehnica University – Bucharest, "Lucian Blaga" University – Sibiu, "Transilvania" University – Brasov, "Dunarea de Jos" University – Galati.

The opening ceremony took place in a very warm atmosphere with more than 70 attendees. Greetings to the participants were offered by Alexandru Borcea, ARIES Program Manager (Romanian Association for Industry, Electronics and Software), Prof. Ph. D. Gheorghe Serban, Vice Rector, Prof. Ph. D. Gheorghe Barbu, the rector of the University of Pitesti and Prof. Ph. D. Paul Svasta, from University Politehnica of Bucharest and the Chairman of the Steering Committee of TIE.

Prof. Gheorghe Barbu pointed out that the contest is useful for both teaching stuff and students. It gathers the best students in the field and it's a great opportunity for them to evaluate by themselves their level of knowledge, to accommodate with the competition and also to find out the latest news in this field.

The Professor said he would also like to hear opinions from the students in order to develop an open talk between all involved persons.

Opening ceremony - From left to right: Alexandru Borcea, ARIES, Prof. Ph. D. Gheorghe Serban, ViceRector, Prof. Gheorghe Barbu, Ph. D, the Rector of the University of Pitesti and Prof. Ph. D. Paul Svasta, IEEE-CPMT SBC Advisor

Mr. Alexandru Borcea was present at every edition of the contest and mentioned that TIE aligns the universities and the business domain, assuring the competitivity of the industry. The diploma received at the end of the contest is on its way to become a certificate.

This year featured new events on the contest schedule: two workshops based on *Traceability in Electronic Packaging and the Nowadays Solutions for Electronic Modules Development.*

For the participants, and especially for the winners, it is a good occasion to keep in touch with trends and a way to get informed about their future career. Students can now decide if what they learn is what companies ask for.

The first Workshop, presented by Mr Traian Cuhu, Key Account & Distribution Manager Romania & Bulgaria, at Brady Corporation, having as moderator Mr. Alexandru Borcea, had as topics "*Traceability, an Important Key in Electronic Manufacturing*" and draws the steps to follow in manufacturing a ticket for a big variety of products.
The term "traceability" means the steps one should follow in manufacturing the product. Prof. Paul Svasta stated that "a company cannot exist without traceability".

The second Workshop, presented by Radu Serban Ionescu, Ph.D., from the RadioConsult Company and chaired by Prof. Mariana Jurian, Ph. D., had as topic: "*Nowadays Solutions in Electronic Modules Design*".

Dr. Ionescu discussed the problem of planning and manufacturing the components used to create the radio equipment defined through a program or virtually (Software Radio). His presentation ended with an invitation made to the universities who want to improve their lectures and lab platforms to have access at additional material.

And of course, a contest couldn't be without participants and subjects.

The Technical Committee, chaired by Associate Professor Norocel Dragos Codreanu of Politehnica University of Bucharest, was deeply involved in development of the subject for the contest. The developing team gathered teaching staff from each participant university as well the previous winner of the contest, Cosmin Andrei Tamas. As a new comer, Associated Professor Gheorghe Pana Ph.D. from Brasov told us how important the direct involvement in the contest topics development was for him, saying he had a lot to learn from it.

From our SBC there were four participants, one of them (Radu Foti Coleca-SBC Vice-Chairman) obtaining a good result in the final.

The winners of TIE 2008 are students at "Politehnica" University of Timisoara from Professor Horia Carstea, and Assistant Professor Marius Rangu.

Students found the contest a little bit hard, but challenging, and await with great interest next year's edition, which will take place in Galati, hosted by the "Dunarea de Jos" University of Galati, as well as the new ideas (and opportunities) it will bring.

From right to left: Adam Gina, Valentin Nita, Leonard Teasca and Radu Foti Coleca from Politehnica University of Bucharest

The winners of the TIE 2008 contest - From left to right: Trifan Alexandru (third place) Osan Adrian (first place) and Negrea Catalin (second place)

*****

Conference Reviews:

58th Electronic Components and Technology Conference (ECTC) Update

Submitted by Dr. Dave Palmer, Contributor,
IEEE CPMT Society Newsletter

Luncheon Speaker:

Title: The Global Semiconductor Industry Outlook

George M. Scalise, president of the Semiconductor Industry Association, gave the luncheon presentation at this year's ECTC. He used as his theme "creative destruction," a concept from the works of Joseph Schumpeter. As an example, he pointed out that the transistor vastly improved electronics performance over tubes yet none of the successful tube companies made it big in transistors or ICs. He similarly sees the end of the CMOS era in about 10 years with some yet to be defined Nanotechnology taking over. How can a company make the creative leap without the concomitant destruction?

He pointed out that during such a transition it will be necessary to:

- Commit to IP protection amongst the players
- Compete for investment funds

- Rebuild the development and manufacturing infrastructure

He observed that unlike the days of Bell Labs, all research is now conducted in universities. He further observed that education of students from first grade through the universities will have to continue changing with the changing technology and talent needs, and also that the big 'creative destruction' will require wise tax policies for both research and infrastructure changes.

He has been somewhat disappointed that Washington DC has been mostly talk and little action on these issues, but did point out that some countries are taking the lead (Ireland, China, Singapore, and Israel).

The industry is seeing an 8% growth this year. Memory chips are under severe cost pressure. The PC market is still the number one driver at 40% with the cell phones second with 20%. Other consumer products are at 17%. The industry has grown from $40B in 1995 to $400B soon.

Panel Sessions at 58th ECTC:

3D- TSV Packaging Application – Implementation:
On Tuesday evening at this year's ECTC *William Chen*, President of the CPMT Society, moderated the ECTC Panel Discussion focused on TSV (Through Silicon Vias). About 230 conference attendees skipped Disney World to learn and ask many questions.

Peter Ramm of Fraunhofer IZM discussed the advantage of 3-D systems to provide heterogeneous systems. He used as an example the European e-CUBES project focused on self organizing networks of wireless sensors. Infineon Automotive has created a tire pressure measurement system as a 0.3" cube by combining a 'large' MEMs pressure diaphragm with an RF transceiver and antenna. The system used stud bumps as well as hollow vias to connect layers. His advice was "don't use a complex interconnect for all interfaces but use the easiest technology for each layer." Via metal filling is the most expensive step in TSV at $109; the complete TSV is estimated at $400/wafer. Any of the 3-D solutions often answer the challenge of performance draining interconnection in a 2-D design.

Bob Sankman of Intel emphasized the shorter connection lengths of 3-D allowing a high rate of data communication. This would be particularly helpful with memory stacked on a processor chip, or perhaps a multi-sensor chip on a processor or wireless transceiver. In general where the form factor is the most important marketing need, 3-D should be used. Since TSV is a most complex way to stack layers it should only be suggested for the right market. Bob Sankman suggested that the via last approach is more flexible in manufacture. As to whether you should do wafer stacking or die stacking depends on the application and unit volume. Intel will not go to TSV until they "have to".

Hirofumi Nakajima of NEC Electronics Company mentioned that Japan has been working on TSV intensively since 1990. They use Cu, W, and poly-Si to fill the vias, but contamination must be monitored with copper. Tungsten has lower resistance and finer pitch than poly-Si. They have found chip to wafer bonding as the most cost effective approach for their applications. He showed an image sensor as an example resulting in 0.64 mm package heights. Their target is to perform TSV at $200/wafer. Sony is using face-to-face with 25 micron pitch. He agreed that you need a significant form factor or performance advantage to compensate for the extra cost of TSV. This suggests that a break-through is needed in TSV processes.

Tom Gregorich of Qualcomm says that it is time for each company to either ante-up for TSV or to pass. Qualcomm motivation for TSV process is to include more consumer functions in the same form factors of today's slim units. Unfortunately the consumer judges the product by cost and form factor and performance. The wide ranges of technology in the cell phones make it hard to put everything into one package. The question they ask regularly is "what is next in cell phone packaging." With TSV one must also ask who performs the extra steps, the wafer fab or the assembly line. Tom predicts that TSV will keep improving every year just like wire bonding has just kept going.

Under questioning the panel stated that design for TSV is behind the fab process at this time. There are rules of thumb for TSV design but no automated computer tools. In conclusion, it appears that TSV is something everyone is getting familiar with just in case one more manufacturing breakthrough occurs.

ECTC Panel – Product Development in the Semiconductor Industry:
Senol Pekin, Intel, chaired a packed evening session on Wednesday at the just completed ECTC in May. The perspective for the discussion was set.

- Originator company of new tech bears most of the cost
- Copy-cat companies get higher profits initially
- Profit margins decrease in time

Lesson learned: one needs a series of great ideas to sustain a company. Examples used include Disney domination of animation in the 20s and 30s only to have other companies originate super-hero cartoons and expand the pie of acceptability. Senol Pekin also pointed out that the nylon industry often threatened to stop growing but new markets kept being discovered. The Semiconductor industry is $250B/year today, how will it keep growing?

Jerry Bautista of Intel insisted that an increase of digital power in an IC will continue to double every two years. However, the advance will not depend on diminishing feature size or higher clock rate as much as by architecture such as multicore, and high bandwidth connections to memory and between cores. Application trends will continue to see data bases get more massive: from the 3-D and video streaming of today to some complex sensing and perception applications in the future, e. g. virtual surgery.

Philip Damberg of Tessera discussed how IP based companies can keep growing using Tessera's history to prove his point. Growth comes from anticipating trends before large companies, and buying up small companies that are headed in the right direction.

Hamza Yilmaz of Alpha and Omega enumerated the steps for successful product development and then suggested general rules of thumb.

- Examine new concept and market
- Define initial spec and flesh out justification for investment

- Detailed design resulting in full specification – start system level evaluation
- Customer sampling – system characterization
- Release to manufacture

Success of a Technology company depends on having many products in the development pipeline. Must maintain a process R&D effort separate from specific product R&D or your strength will ebb. When a crisis develops it is important to immediately dig for the root cause reason and not play palace politics. Hamza Yilmaz suggested that we should now use the many computer simulation tools that exist for each step of development.

Ken Williams of Applied Materials explained that every step in the product development pipe sees a reduction of options by 10, thus develop something with lots of options in the design stage. He suggested that the low-K quest has been delayed by 7 years because the initial scope of the development had too few options. He sees "solid state drives" as a new inflection point. If the trends continue 7 new fabs will be needed just to make enough flash memory. The cost of these memories must drop (do we have any technology options lefts?), we need 32nm litho but it doesn't exist realistically in the pipeline (Intel cancelled the Extreme UV litho effort because it couldn't keep on schedule).

Raj Masters of Advanced Micro Devices discussed efficient product development. He added a new rule of thumb – "never have more than 100 check points / milestones on even the most complex project or you will never finish." He suggested it is most important in the production facilities to carefully separate value added steps from waste steps. Some waste steps may be mandated for historic reasons but many can be designed out of the flow. He mentioned that when he enters a plant announcing that he is there to make them "lean" that most engineers mumble "leave us alone, we know what we are doing," but by the time the process is over everyone is lean and mean.

In response to audience questions the following consensus was projected. It doesn't make sense to go to 450mm at this point since there are still other ways to get more ICs out of existing wafers. Companies can grow revenue by going into related markets that benefit from their strengths – ICs to large panel displays to solar cell panels was an example. (so companies can grow fast even if the IC business does not). They predicted the semiconductor industry would continue to grow faster than the world economy. Most were lukewarm toward stacking chips using TSV but they all are developing the technology in case there is a more prime time. Intel may have been bluffing, but suggested that the need to marry external memory at high bandwidth to processors may push TSV for them.

Advanced Embedded Passive and Active Device Technologies:

On Thursday evening of ECTC *Yoshitaka Fukuoka* of Weisti led the CPMT Seminar on embedded components.

Osamu Nakao of Fujikura entitled his presentation "IC Chip-Embedded Polyimide Multi-layer Circuit Board." The original motivation was to make flexible and foldable multi-layer polyimide circuit boards with embedded chips. This approach gave higher density, easier handling, high performance, good reliability, allowed surface mounting if needed, and could conform to system package. The IC interconnections are formed on some foundation polyimide layers to which the ICs are mounted face-down. Face up can also occur but requires vias to be accurately placed in a polyimide layer. It is sometimes necessary to reposition the pads on an IC from dense edge pads to less dense area distributed pads using wafer steps. A pitch of 300 microns is reasonable, allowing a 8x8mm chip to have 600 I/O. The silicon die are typically thinned to 80-100 microns before embedding. Conductive paste has been used to fill vias in polyimide. Particle size is 5-10 microns.

Atsushi Kobayashi of Dai Nippon Printing discussed "The superiority of Buried Bump Interconnection Technology in EPD & EAD PCB manufacturing. The standard BBit process uses 180 micron bump spacing, the advanced is at 130 microns, and the super to be released in one year will be at 80 microns. The embedding is in 6-8 layers with bumps on Cu foil layered with Prepreg. The embedding of components results in shorter interconnect lines and lower cross talk and noise pickup. Bumps are made with screen printing of custom Ag paste. An example was a wrist watch with memory chip. 10 million unit are made a month with 95% yield using Know Good Die.

Yasuhiro Sugaya of Panasonic Electronic Devices presented "Embedded Capacitor Interposer by using SIMPACT. The goals for their embedding were (1) a multi-functional terminal that was smaller but fully functional, and (2) a high speed CPU package with low ESR and ESL. A new paste was develop to act like a via post when attaching the components. Module size reduction was 45 – 60 %. One particular advantage was to bring the bypass capacitors to be right beneath the LSI chip rather than having surface mount caps on other side of mother board. The embedded capacitor sheet is only 100 microns thick instead of the original discrete 1.8mm thickness. A clock rate of 400 MHz was achieved with much reduced power usage. Clock jitter went from 133 to 65 psec.

Akinobu Shibuya of NEC focused on "Si Interposer Integrated with SrTiO3 thing Film Decoupling Capacitors and TSVs." He pointed out that as the speed of ICs keeps increasing, the capacitors must get faster and larger. A goal of one microfarad with short leads is set for any technology. They place a thin film capacitor between the IC and the package/board. The capacitor and the needed interconnections becomes the silicon interposer. An STO sputtered thin film is used to get a dielectric of over 100. This capacitance layer is carpeted everywhere and then patterned so through vias can be made. An IR laser beam is used to find weak points in the capacitor by noticing the increase in leakage due to local heating. Hillocks often correspond to leakage points. They discovered if the film deposition takes place at less than 400 C then no hillocks form. The through silicon vias are 50 micron thick with smooth side walls. Copper is the fill leaving a pad on the top of the via. The STO capacitor wafer is married to the LSI wafer and then dicing is one. Capacitance range depends partly on LSI size and has been 1-7 microfarad.

Ichiro Koiwa of Kanto Gakuim University discussed "Fabrication and Embedding the Thin Film Capacitor Array Prepared by Semiconductor Technology." The driving need is that there was no surface area for capacitors so they had to be embedded. He discussed two dielectric types. One gives large area capacitors with

medium loss: dielectric = 51, delta = .03, Ba0.6Sr0.4TiO3. the second gives medium capacitors and at low loss: dielectric =350, delta = .001, Sr0.9Bi2.1 Ta2.0O9. Platinum films were used as the plates. A master pattern of capacitor sizes was used so that any particular value can be reached by connecting the correct plates. These designs self resonate at 10 GHz for the 65 pF size. There is only a 1% change from 25-150 C. The low K capacitors survive soldering steps on the board.

Many different embedding technologies are being actively used in commercial product manufacturing.

Presentations at 58th ECTC:

Since many Society members were unable to make the ECTC in May a brief summary of some of the talks are below so you can consider ordering a Proceedings CD or search Xplore for more of the presentations.

Session 4 RF components:

1. Sandia Labs describe 3 components developed to allow a portable real-time spectrum analyzer: SiGe RF power divider, monolithic frequency stepped SAW filter, and integrated RF detectors.
2. Sasumu Obata of Toshiba discussed the use of low outgassing polymer used to make adjustable capacitors "hermetic" with wafer processing.
3. Geert Carchon of IMEC described post processing of state-of-the-art CMOS wafers with BCB and Copper to make high Q inductors for high frequency circuits.
4. Emile Davies-Venn of Intel described in detail the circuit design and FCBGA processing to achieve Q~30 for capacitors and inductors used on a WiFi Balun.
5. David Chung of Georgia Tech describes an antenna module for 14 GHz satellite use that can be stacked like LEGOS TM. Liquid Crystal Polymer was the material used.
6. Lianjun Liu of Freescale Semiconductors gave an expansive talk on RF MEMS switch designed for many cycles and low price. The goal is to integrate the switches into a cell phone module so a minimum of components can serve the many bands a phone must respond to.
7. Guoan Wang of IBM discussed board patterning techniques to produce slow wave behavior of 60 GHz circuits. This will allow compact components.

Session 10 Nanotechnology:

1. Yang Chai of Hong Kong University of Science and technology presented development using carbon nanotubes to minimize electromigration of Cu lines on ICs. The resistivity increased by 14% when tubes are include in the electroplating solution. However the electromigration is suppressed.
2. Wei Lin of Georgia Tech described taking aligned nanotubes carpets grown at high temperature but then transferred at low temperature to an assembly. The presentation included a movie showing transfer in an SEM.
3. Jin-Chen Chiu of National Sun Yat-Sen University discussed making a liquid of nanotubes in a polyimide matrix using an ionic liquid to keep the tubes from clumping. This material is applied as EM shielding on a module.
4. Po-Chun Huang of National Tsing Hua University produced nano particles of Tin by evaporating into a gas and used metal salt in liquid to prevent aggregation and oxidation. This paste could fill micro vias on the smallest scale.
5. Trang T. Thai of Georgia Tech described wireless sensors based on nanotubes. This is a simulation study aimed at using them as gas sensors in composites or structures.
6. Shin-Bok Lee of Seoul National University proposed Pd-Ag dendrites at hydrogen sensors. These filaments are more stable than a thin film of Pd which is the current technology.
7. Rabindra Das of Endicott Interconnect Technologies used a raster laser to process dielectric films to make adjustable capacitors. Also, deep channel etching to allow x10 density capacitors was presented.

***Session 16 Integrated Passives*:**

1. Arun Chandra Kundu of Intel compared passives for silicon, glass, and LTCC for a wireless module. All were suitable for production with LTCC being thicker and more expensive and glass allowing smallest form factor.
2. P. Markondey Raj of Georgia Tech discussed dielectric films that give TCC< 30 ppm. They developed low temperature ways to get the right crystal structure from BaTaZno3 and CuZrO3 films.
3. Li Li of Freescale Semiconductor discussed a trade-off study of technology for making Baluns. After succeeding with GaAs they wanted to lower costs by using high resistivity Si wafers.
4. Don Won Lee of Stanford University presented methods to make solenoid inductors with magnetic cores using IC processing. An amorphous CoTaZr film was used as the core.
5. Clemens Ruppel of EPCS AG discussed the high Q filters needed to provide a 55 dB duplexer for cell phones to isolate transmitter from receiver. SAW and BAW devices still win in design and expense over MEMs type designs.
6. Goerge Ponchek of NASA discussed resistors embedded in a Liquid Crystal Polymer. The study characterized the resistors to determine the highest power for which they remain reliable.
7. Kai Liu of STATS ChipPAC compared many substrates for filter and Balun construction. They chose a silicon substrate using IPD technology and made it x6 smaller area and x10 volume. Qualification was performed.

Mahadevan Iyer and Amit Agrawal prepare before the breakfast meeting begins

Electronic Components & RF Committee meeting:

Mahadevan Iyer of Infineon chaired a Friday 7am breakfast meeting for the Electronic Components & RF committee at ECTC. Fourteen conference attendees showed upin addition to two persons calling in. Mahadevan reported that 54 abstracts were received with the right technology focus. Of these 42 were submitted directly to the committee and 18 papers scheduled for presen-

tation. This represented 2.5 sessions at the conference plus one of the evening panels which was completely dedicated to embedded components.

Len Shaper suggested that we include in our next request for papers a focus on high speed digital components (terminations and decoupling caps) and stress was added for papers on wireless sensors. Variations on the committee name were considered to make sure RF and Components were both recognized; the leading contender is "electronic components and RF technology." New names of stakeholders were gathered for next year's e-mailing request. There was a suggestion to mine the names of all authors of papers and presentations of RF and component papers.

Amit Agrawal of Cisco was voted the new chair of the committee. If you want to help grow these technical topics for ECTC and for the CPMT Society contact Amit at ap_agrawal@yahoo.com

Part of committee preparing for next year's ECTC abstract hunt

*****

2nd International Workshop on 3D System Integration

Submitted by Rolf Aschenbrenner, VP Conferences, IEEE CPMT Society

The 2nd International Workshop on 3D System Integration took place on 1-2 October 2007 at the Fraunhofer-Society, Munich, co-organized by IEEE CPMT. More than 90 engineers, scientists and entrepreneurs attended the 2-days workshop and discussed about world-wide R&D activities, perspectives and challenges of 3D integration.

After the welcome and introduction by Peter Ramm, Fraunhofer Munich, the keynote address was given by Sitaram Arkalgud, director of SEMATECH (US), on "Paving the Roadmap for Through Silicon Vias". The first day continued focussing on Si-based technologies for 3D IC integration with excellent talks of speakers from ZyCube (Japan), STMicroelectronics (Italy) , EPFL (Switzerland), NXP (Netherlands), SINTEF (Norway), Semitool (US), IBM (Switzerland), CEA-Leti (France) and Fraunhofer IZM (Munich). After the opening talk of Robert Darveaux, Amkor (US), on "Developments of 3D Packaging" the second day´s talks were given by speakers from AT&S (Austria), Techlead (US), Imbera (Finalnd), ASE (US), IMEC (Belgium), Schweizer Electronic (Switzerland), Panasonic (Japan) and Fraunhofer IZM (Berlin).

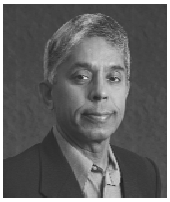
Speakers and chairs at the IEEE Workshop on 3D System Integration Munich 2007 (sitting right: Keynote speaker Dr. Sitaram Arkalgud (SEMATECH); row left and center, respectively: Chairman Dr. Peter Ramm and co-chair Rolf Aschenbrenner (Fraunhofer IZM)

*****

Enabling Technologies for Green Electronic Packaging

Submitted by Dr. Mali Mahalingam, Tutorial Committee Chair, IEEE CPMT Society Phoenix Chapter
mali.mahalingam@freescale.com

In our modern day living we are all very much aware of the waste materials we create, improper disposal of products at the end-of-life and many health and environmental consequences resulting from such actions. According to the UN Environment Programme, electronic waste totals 50 million tons a year worldwide ["High Tech Trash", National Geographic, Jan. 2008]. In the electronics industry this is a growing problem due to "rapid technology changes" and the practice of "planned obsolescence" in consumer electronic products. If the waste material is not properly recycled and treated, they become major sources of toxins and carcinogens. To combat the situation, RoHS (Restriction of Hazardous Substances) Directive came into effect in 2003 and this directive restricts the use of six hazardous materials in the manufacture of electronic and electrical equipment. We need to be more thoughtful and creative in the future in reducing and/or eliminating the use of harmful materials as we develop new materials, new assembly/manufacturing processes and new products.



IEEE CPMT Society Phoenix Chapter is organizing a half-a-day technical tutorial under the leadership of Dr. Mali Mahalingam of Freescale Semiconductor Inc., Tempe, Arizona, to focus on the theme of "Enabling Technologies for Green Electronic Packaging". It is planned for mid Sept. 2008, at Amphitheater, Airport Hilton, Phoenix. Following four topics are planned: (i) Pb free solders (ii) Green polymers for electronic packaging (iii) Environmentally friendly assembly/manufacturing processes and (iv) recycling/ environmentally friendly disposal. Dr. Darrel Frear (Freescale Semiconductor Inc.), Prof. C.P. Wong (Georgia Tech.), Dr. Luu T. Nguyen (National Semiconductor Inc.) have commit-

ted to be presenters. Commitment from a fourth speaker is shortly expected.

*****

Summary Report on ITHERM 2008

Yogendra Joshi, Program Chair

The ITherm 2008 conference was held at the Hilton at Walt Disney World Resort in Orlando, Florida during May 28-31, 2008. The Conference General Chair was Dr. Tom Lee from TSMC, Inc. and Program Chair was Prof. Yogendra Joshi from Georgia Institute of Technology. The conference was attended by approximately 260 registered attendees and included nearly 170 technical paper presentations.

The conference began on May 28 with a total of thirteen advanced short courses (4 hours each) and tutorials (2 hours each) presented by expert instructors in morning and afternoon sessions. In general, the short courses covered established topics of general interest, whereas the tutorials covered emerging themes. During May 29-May 31, the technical papers were presented in 38 sessions covering four Tracks: Thermal Management, Mechanics and Materials, Emerging Technologies, and Energy Efficient Electronics. The last of these, is a newly established topic of significant current interest. All papers in this Track were presented in the form of posters in a single dedicated session on May 30. In all, 18 technical sessions were held in Thermal Management, 8 in Mechanics and Materials, 6 in Emerging Technologies, and 6 in Energy Efficient Electronics.

In addition to the technical papers, there were three Keynote/Invited presentations. The opening Keynote titled, "Emerging Systems Packaging Technologies", was delivered on the morning of May 29 by Prof. R.R. Tummala from Georgia Institute of Technology. The ITherm Achievement Award Luncheon talk titled," IBM, Mainframes, and Environmentals", was delivered by Dr. R.R. Schmidt from IBM. There were four panel sessions during the conference. These included: "Thermal Management Challenges for Military Electronics", "Cooling Challenges and Energy Efficiency in Low Form Factor Electronics", "Cyber Infrastructure Resources for Thermal Management", and ""Energy Efficient Data Centers".

A key feature of the ITherm conference has historically been the link with the Electronics Components and Technology Conference (ECTC) through the joint Exhibits program. This year the distance between the two venues required the use of shuttle buses. Visits to the Exhibit were arranged for the evening reception on May 28, and during the afternoon of May 29. For ITherm 2010, the proximity of the two conference venues will make this linkage even stronger.

The Awards Luncheon was the final event of the conference, held on May 31. At this event, Best Paper Awards to the authors of the highest rated paper from each of the four Tracks were presented. In addition, two papers from the Thermal Track and one from the Mechanics Track received the Outstanding Paper Awards.

SCV CPMT Chapter – Aaargh!

The theme of CPMT's luncheon at ECTC this year was "Pirates!" with the idea that there is treasure buried within the Society's services and networking. After returning to the Santa Clara Valley (CA), several of the ECTC attendees (along with others from the chapter's operating committee) celebrated by donning some of the booty brought back from the Conference.

SCV Chapter OpCom members (from left): Valerie Pilloud (treasurer), Allen Earman, (vice-chair), Paul Wesling (chapter advisor), Mudasir Ahmad (secretary), Janis Karklins (membership development), Bernie Siegal (SEMI-THERM liaison); front row: Ed Aoki (program co-chair), Sandra Winkler (program co-chair)

The SCV Chapter is holding their summer planning meeting/picnic at the home of Bernie Siegal in July to structure another active program for 2008-2009.

Put your Technology Leadership in Writing!

Publish in our IEEE Transactions

Figures in full color; worldwide access to results.

For more details:

www.cpmt.org/trans/

Watch for the September, 2008, Newsletter Issue
IEEE CPMT Society News

Send Your News Articles to the Editor at
nsltr-input@cpmt.org

Access papers from the 2008 ECTC, EPTC, and others:

Visit ieeexplore.ieee.org and download them

Purchase the CD-ROM at www.cpmt.org/proceedings

ACCESS A WEALTH OF KNOWLEDGE AT WWW.CPMT.ORG
JOIN THE IEEE CPMT SOCIETY

ACCESS PREVIOUS ISSUES OF NEWSLETTER AT WWW.CPMT.ORG

SUPPORT THE CPMT SOCIETY
RECRUIT A NEW MEMBER
ADDITIONAL INFORMATION AT WWW.CPMT.ORG and WWW.IEEE.ORG/mgm/

Support IEEE CPMT Society and Chapters

Participate in Seminars, Workshops, and Conferences by Organizing and Attending

Additional Information at www.cpmt.org/conf/

CONFERENCES IN 2008:

Joint Int'l Conference on **Electronic Packaging Technology & High Density Packaging** (ICEPT-HDP) **www.icept.org**
July 28~31, 2008 Shanghai, China
Contact: ICEPT-HDP Secretariat at icept2008@fudan.edu.cn

Joint Event: 7th Int'l IEEE Conference on **Polymers and Adhesives in Microelectronics and Photonics** (POLYTRONIC 2008) with **PORTABLE 2008**
August 17—22, 2008 Edelweiss Hotel & Conference Center **www.polytronic2008.com**
Garmisch-Partenkirken, Germany
Contact: info@polytronic2008.com

Electronics System-Integration Technology Conference (ESTC 2008) **www.estc.biz**
September 1-4, 2008; University of Greenwich Greenwich, London UK
Contact: Chris Bailey, Greenwich University, chris.bailey@estc.biz

4th Int'l **Workshop on Thermal Investigations of ICs and Systems (THERMINIC)**
September 24-26, 2008 Rome, Italy
Contact: Chantal Bénis-Morel, CMP, chantal.benis@imag.fr

2008 Workshop on **Accelerated Stress Testing & Reliability** (ASTR)
www.ewh.ieee.org/soc/cpmt/tc7/ast2008
October 1 - 3, 2008 Portland, OR USA
Contact: Cheryl Tulkoff, National Instruments, cheryl.tulkoff@ni.com

Joint Event: 3rd **Int'l Microsystems, Packaging, Assembly and Circuits Technology** (IMPACT) Conference, with the 10th Int'l Conference on **Electronics Materials and Packaging** (EMAP)
www.impact-emap.org
October 22 - 24, 2008 Taipei, Taiwan
Contact: Mr. Long-Shien Lin, tw2008@isu.edu.tw

54th IEEE **Holm Conference on Electrical Contacts** (HOLM 2008)
ewh.ieee.org/soc/cpmt/tc1/h2008/h2008top.html
27-29 October, 2008 Orlando, FL USA
Contact: Chi H. Leung, AMID DODUCO, cleung@amidoduco.com

Electrical Performance of Electronic Packaging (EPEP 2008)
27-29 October, 2008 San Jose, CA USA
Contact: Kelly, Univ of Arizona Professional Development, epd@engr.arizona.edu

33rd Int'l **Electronics Manufacturing Technology Symposium** (IEMT 2008) **www.cpmt.ieeemalaysia.org**
November 4-6, 2008; Penang, Malaysia
Contact: Ir. Dr. Cheong Kuan Yew, USM cheong@eng.usm.my

9th **VLSI Packaging Workshop in Japan**
December 1 - 2, 2008; Kyoto, Japan **vlsi-pkg-ws.org**
Contact: Michitaka Kimura, Renesas Technology Corp, kimura.michitaka@renesas.com

10th **Electronics Packaging Technology Conference** (EPTC 2008) **www.eptc-ieee.net**
December 9-12, 2008; Singapore
Contact: Dr. Tong Yan Tee, tytee@amkor.com

Electrical Design of Advanced Packaging and Systems (EDAPS 2008) **www.edaps2008.org**
December 10-12, 2008 COEX Conference Center Seoul, Korea
Papers due: July 31, 2008
Contact: S.M Yang, yangsm@ee.kaist.ac.kr

2nd Int'l Conference on **Thermal issues in Emerging Technologies, Theory and Applications** (ThETA2)
December 17-20, 2008 Cairo, Egypt **www.thetaconf.org**
Papers due: July 31, 2008
Contact: thetaconf@gmail.com

CONFERENCES IN 2009:

2009 Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM 25)
March 15-19, 2009 San Jose, CA USA
Abstracts due: October 15, 2008
Contact: Tom Tarter, ttarter@ieee.org

59th Electronic Components and Technology Conference (ECTC 2009)
May 25-29, 2009 San Diego, CA USA
Abstracts due: October 15, 2008
Contact: Jean Trewhella, jeanmh@us.ibm.com

European Microelectronics and Packaging Conference & Exhibition (EMPC 2009) **www.empc2009.org**
June 14-17, 2009 Rimini, Italy
Abstracts due: December 31, 2008
Contact: Pragma Congressi, segreteria@empc2009.org

IEEE **Int'l Workshop On Advances in Sensors and Interfaces** (IWASI'09)
June 25-26, 2009 Trani, Italy
Papers due: February 28, 2009
Contact: Prof. Daniela De Venuto, d.devenuto@poliba.it

ESTC 2008

2nd Electronics System-Integration Technology Conference
1st – 4th September 2008, Greenwich, London, UK www.estc.biz

The IEEE 2nd ESTC Electronics Systems-Integration Technology Conference is on track to be an outstanding technical event and exhibition. ESTC-2008 will comprise 270 themed technical papers in six parallel oral tracks and posters. Posters will be displayed and also be presented.

The Technical themes at ESTC-2008 are: • Advanced Packaging • Emerging Technologies • Manufacturing and Test Technology • Modeling, Simulation and Design • New Materials and Processes • Power Electronics • Technology & Reliability for Micro and Nano Systems • Assembly of Alternative Energy Sources • Optoelectronics • Electronics system-integration for healthcare.

Special invited Sessions:

Asia-Pacific Photo-voltaics *will address: • "Third Generation Photo-voltaics" • "System-integration Strategies for co-Generation of Electricity, Heating and Cooling using Solar Photo-voltaic Modules" • "Building Integrated Photo-voltaics for Maximum Power Generation" • "The Intellectual Property Landscape for Photovoltaic Technologies"*

Standards *will address: "The Critical Standards for BT's 21st Century Network" • "EMC and Functional Safety Requirements for Integrated Electronics Systems" • "The Evolution of Standards in Industry"*

Prognostics and System Health Management for Reliability *will address: "Embedded Prognostics and Health Monitoring Systems" • "Integrated Vehicle Heath Management in the Auto Industry" • Aerospace and Electronics System Prognostic Health Management" • "Detecting Anomalies in Field Returned Laptops using Mahalanobis Distance"*

Greening the Blue Planet (public session): *• "Electronics, Energy and the Environment" Johns Hopkins University • "Interdependence of Marine Ecosystems and Climate Change" WWF • "Future Parks in Future Climates - scalable solutions" Ecologist Brecon National Park • "Talking Green about Nuclear" University of Cardiff*

Short Courses

Eight half-day short courses will be taught on Monday 1st September

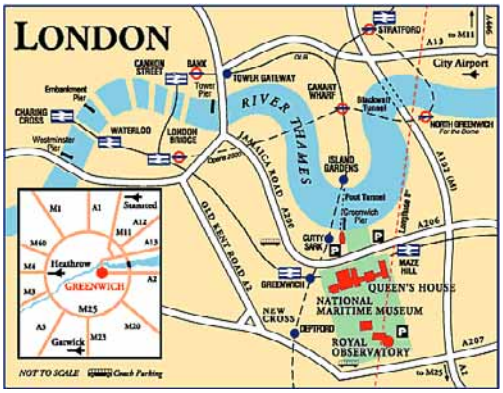
Opening and Keynotes

The Conference will be opened on Tuesday 1st September by Baroness Blackstone, Chancellor of the University of Greenwich. The Keynote Opening Address will be on "**Ambient Assisted Living**" by Dr. Nakita Vodjdani, Vice-President of the European Union AAL Association. The Keynote closing address will be by Prof. Peter Cochrane, entrepreneur and former Chief Technologist of British Telecom

Attendance is expected to exceed 500 international delegates.

The major technical exhibition will be held alongside the Conference – an excellent opportunity for suppliers of materials, design houses, circuit manufacturers to promote their products and reach potential customers.

ESTC 2008 will be held at Greenwich, a World heritage site and major maritime site on the banks of the River Thames in the magnificent city that is London. The Conference and Exhibition will be hosted by the University of Greenwich in the buildings of the former Royal Naval College. Plenary sessions will be in the Great Painted Hall – providing a wonderful ambience for the technical presentations.



Visit: www.estc.biz Information: **sinnadurai@estc.biz**

Joint International Congress and Exhibition
In Conjunction with the 1st World ReUse Forum

EGG ELECTRONICS GOES GREEN 2008+

Merging Technology and Sustainable Development

September 07-10, 2008 Berlin, Germany
Organized by Fraunhofer IZM
Technical Co-sponsor: CPMT Society
Industrial sponsors: DELL, Intel, Panasonic

Building on the tradition of the extremely successful conferences **Electronics Goes Green 2000** and **2004**, **Electronics Goes Green 2008+** will again be the meeting point for specialists from all over the world working in the realm of electronics and the environment. This year's presentations will focus on the following main topics:

- Legislation: Impacts, Improvements & Harmonization
- Products, Systems & Sustainable Technologies
- Management & Social Responsibility

If you have a professional interest in the best environmental solutions already or if you are increasingly forced into dealing with topics like energy efficiency, carbon footprints, toxic substances or recycling, then the Electronics Goes Green 2008+ is the place to come for updates and international exchange.

Visit our website for the Preliminary Program or subscribe for conference newsletter:

egg2008.izm.fraunhofer.de

Polytronic '08

Co-located with
PORTABLE'08

7th International IEEE Conference on

Polymers and Adhesives in Microelectronics and Photonics

Garmish-Partenkirchen, Germany 17-22 August, 2008

Please join researchers, engineers and scientists from around the world in mid-August 2008 to share knowledge and experience in Polymeric Materials for Microelectronic & Photonic Applications (POLY), Adhesives in Electronics, and Polymeric Electronics Packaging (PEP). The program will include keynote, invited and contributed presentations, as well as panel discussions. There are eight half-day tutorials and an IEEE Pavilion featuring technology exhibits and demonstrations.

For the Program and registration details for both Polytronic and PORTABLE, please visit:

www.polytronic2008.com

Call for Papers posted .... **EDAPS 2008**

Electrical Design of Advanced Packaging and Systems Symposium

- Seoul, Korea - December 10-12, 2008
- Abstracts Due July 31

Technologists are requested to submit papers in the areas of Modeling, Design, and Measurement of:

- High-speed Digital Signal Integrity
- Power Distribution Network
- High-speed Channels and Interconnect
- Embedded Passives - EMI/EMC
- System in Package (SiP) / System on Package (SoP)
- RF/Microwave Packaging

For more information, please visit our website:

edaps2008.org

Contact: Prof. Dr. Joungho Kim, KAIST, Symposium Chair, joungho@ee.kaist.ac.kr

Workshop on Accelerated Stress Testing & Reliability

October 29-31, 2008 Portland Oregon

Theme: "**Achieving Cradle to Grave Reliability using DFR and AST**"

The ASTR Workshop is an annual CPMT gathering of test and reliability engineers focused on accelerated stress testing and its relationship to reliability. It provides a forum for people from many different disciplines to network and discuss related issues and methodologies. Over the last few years, Accelerated Stress Testing & Reliability (ASTR) has been embraced by an ever widening array of worldwide companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market.

Registration is now open – save through Sept. 30th.

Please visit:

www.ewh.ieee.org/soc/cpmt/tc7/ast2008

IEEE COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY SOCIETY

Final Program

Future Directions in IC and Package Design Workshop (FDIP)

October 26, 2008, San Jose, CA

sponsored by:

organized by:

CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

SESSION I: SYSTEM DESIGN

Session Chair: Paul D. Franzon, – North Carolina State University

Architecture Implications of 3D Integration Technology – Michael Ignatowski, IBM Corporation
Design Considerations for Highly Integrated 3D SiP for Mobile Applications – Joungho Kim, KAIST Korea
Design of Through-Silicon Vias and Vertical Shielding for 3D Integration - Ivan Ndip, Fraunhofer IZM, Germany
Tb/s-Class Module-to-Module Optical Data Buses on Printed-Circuit Boards - Fuad Doany, IBM Corporation

SESSION II: MODELING

Session Chair: Albert E. Ruehli, IBM Corporation

Electromagnetic Solvers for Interconnect and Package Modeling – New Developments – Sadasiva M. Rao, Auburn University
Accelerated Parallelized Integral Equation Techniques for Packaged Microelectronics – Vikram Jandhyala, Univ of Washington
Benefits of Surface Integral Equation Modeling Leveraging Massively Parallel Advanced Techniques – Jason D. Morsey, IBM

Workshop will be held at the Wyndham Hotel, 1350 N. 1st Street, San Jose, California 95112, (408) 453-6200. The hotel is holding a block of rooms for participants at a special rate of $119.00 plus tax. Room reservations must be made by **September 25, 2008** to guarantee this rate. After that time rooms will be on a space and rate available basis only. *Be sure to mention that you are attending the Electrical Performance of Electronic Packaging conference. R*ooms are limited so make your reservations early. Additional information can be obtained at **www.epep.org**

Additional information may be obtained from the workshop chairs:

Alina Deutsch
deutsch@ieee.org
phone: (914) 945-2858
fax: (914) 945-2141

Madhavan Swaminathan
madhavan.swaminathan@ece.gatech.edu
phone: (404) 894-3340
fax: (404) 894-9959

and the workshop administration:

epd@engr.arizona.edu
phone: (520) 621-3054
fax: (520) 621-1443

Attendees interested in the workshop will be charged a $60.0 fee that will cover afternoon refreshments, digest of abstracts, and posting of the foils on the CPMT Society TC-EDMS web site. All attendees must register by September 12, 2008 using the EPEP'08 website at **www.epep.org** in order to assure that the workshop is being held. On-site registrants will be admitted depending on availability of seating.

First Call For Papers

59th Electronic Components and Technology Conference

www.ectc.net

To be held in San Diego, California, USA, May 26 - May 29, 2009

The Electronic Components and Technology Conference is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. The ECTC is jointly sponsored by the Components, Packaging and Manufacturing Technology Society of the IEEE and the Electronic Components Association. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the following areas:

Advanced Packaging:
New packaging technologies, systems packaging, first level thermal solutions for high power applications, designs, materials, and configurations addressing performance, density and cooling for single chip, multichip and SIP, waferlevel, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA and SMT packages for both Pb-based and Pb-free bumps and package assembly.

Electronic Components & RF:
Discrete Passive Components; integrated and embedded passive and active components integration on silicon ceramic, organic substrates; electronic components-design, materials, processing, test, characterization; new technology development for components - silicon through vias, wafer level RDL, nano materials and processes; tunable materials, structures, devices and switches; RFID/sensors, RF MEMS, integrated antennas, filters, baluns; components and modules for WLAN, UWB, mobile PC and multi band radio applications.

Emerging Technologies – Biomedical, Nano-Scale and Organic Devices Packaging & Portable Power Supply:
All design, fabrication, modeling, and performance aspects of materials, devices, systems, and packaging in the areas of: (1) Nanoelectronics including <90nm Si device technology, Single Electron Transistors (SETs), Carbon Nano Tube (CNT)/nanowire and molecular devices, spintronics, etc., (2) Bioelectronics such as biomedical, bioengineering, biosensors and electronics for medical devices, and (3) Organic /Printable Electronics.

Interconnections:
Interconnect innovation/design/process on all packaging levels including wire bonding, flip chip, 3D and through Si via connections, first-level package, and printed circuit board. Topics may range from bump and under bump metallurgy, electromigration, conductive polymers and nano material based interconnects, novel enabling techniques, electrical performance, to environmental concerns.

Manufacturing Technology:
Advanced process and equipment improvement for volume production of emerging technologies including: system in package, package on package, wafer thinning, bumping, stacking; low-k chip, Pb-free and MEMS packaging. Product level rapid integration and system level optimization of new packaging technologies focusing on cost, yield, electrical/mechanical/environmental performance, supply chain development, and product ramp.

Materials & Processing:
Materials and processes for IC and microsystems packaging that enhance mechanical, thermal and electrical performance and cost effectiveness. This includes advances in materials and processing of adhesives, encapsulants, nanomaterials, chip underfills, solders and alloys, magnetic and optical materials, thermal interface materials, polymers, ceramics, composites, flexible dielectrics and substrates, thin films, coating, bonding, plating and assembly processes.

Modeling & Simulation:
Electrical, thermal, optical, and mechanical modeling, simulation, and characterization of packaging solutions including system-level applications. Example topics include - assembly manufacture modeling, Cu low-K interconnects, drop impact models, embedded passives, equivalent circuit models, fullwave modeling, lead-free solders, macromodeling, measurements, and thermomechanical reliability.

Optoelectronics:
Packaging and technology for fiber-optic modules, components and devices including: amplifiers, transmitters, receivers, integrated photonics, passive components, plastics packaging, chip to chip, backplanes and storage. With special emphasis on transceivers, optical inter-connects, high power lasers, advanced processes, manufacturing technology, micro-optical packaging, LED/laser projection displays and solid state lighting.

Posters:
Papers may be submitted on any of the major topics listed by the subcommittees. Presentation of papers in a poster format is highly encouraged at ECTC.

Quality & Reliability:
Reliability assessment and prediction at the system, PWB or package level; reliability testing and data analysis; failure analysis of field and test failures; reliability modeling of accelerated testing; reliability issues in emerging technologies; interconnect reliability physics, testing and predictive simulation; advances in reliability test methods and failure analysis.

At the discretion of the program committee, submitted abstracts may be considered for poster presentation.

You are invited to submit a 750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

Rajen Dias
Intel Corporation
MS – CH5-263
5000 W. Chandler Blvd., Chandler, AZ 85226
Phone: +1-480-554-5202
Fax: +1-480-554-7171
Email: rajen.c.dias@intel.com

Abstracts must be received by October 15, 2008.
All abstracts must be submitted electronically at **www.ectc.net**. You must include the mailing address, business telephone number, FAX number and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses
In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200 word proposals must be submitted via the website at **www.ectc.net** by **October 15, 2008**. If you have any questions, contact:

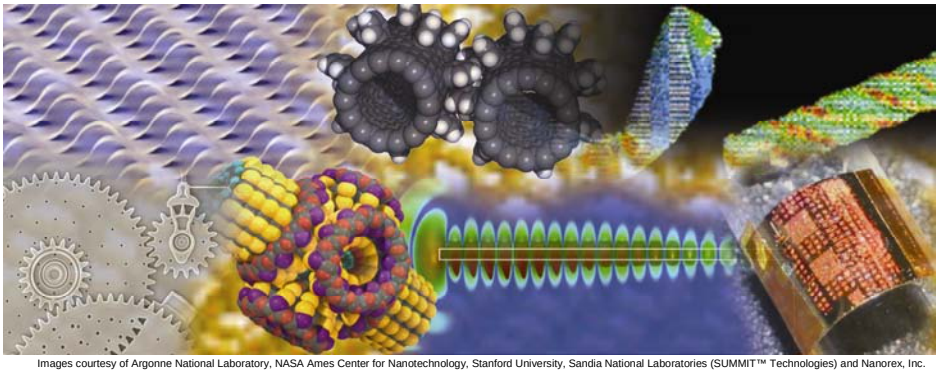
Kitty Pearsall, ECTC Professional Development Courses Chair
IBM Corporation
IMAD 2C-40/Bldg 045
11400 Burnet Road, Austin, Texas 78758
Phone: 1-512-838-7215
Fax: 1-512-823-7004
Email: kittyp@us.ibm.com

Institute of Electrical and Electronics Engineers, Inc.

Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter
&
Waves and Devices Chapter

PRESENT AN ALL-DAY WORKSHOP ON



Images courtesy of Argonne National Laboratory, NASA Ames Center for Nanotechnology, Stanford University, Sandia National Laboratories (SUMMIT™ Technologies) and Nanorex, Inc.

Emerging Device and Packaging Technologies

Friday, November 14th, 2008 7:00 A.M. – 5:00 P.M.

Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

EXECUTIVE COMMITTEE

Workshop Chair
Vasu Atluri, Intel
vpatluri@ieee.org

Workshop Co-Chair
Chuck Weitzel, Freescale
c.weitzel@ieee.org

Registration Chair
Sergio Pacheco, Freescale
sergio.pacheco@ieee.org

Vendor Committee Chair
Steve Rockwell, Motorola
steve.rockwell@ieee.org

Electronic Media Chair
Qing A. Zhou, Intel
qzhou@ieee.org

Arrangements Chair
Samir Pandey, Intel
samir.pandey@ieee.org

TECHNICAL COMMITTEE
Co-Chair: Debendra Mallik, Intel
dmallik@ieee.org
Co-Chair: Mel Miller, Freescale
melmiller@ieee.org
Henning Braunisch, Intel
Shahin Farahani, Freescale
Sanka Ganesan, Intel
Steve Goodnick, ASU
Vivek Gupta, Freescale
Sunit Mahajan, Intel
Steve Rockwell, Motorola
Kalluri Sarma, Honeywell
Sudhama Shastri, CMD
Sandeep Tonapi, Anveshak

Call for Papers

The continued scaling of microelectronics for mainstream applications such as computing and communications on one hand has been enabled by newly developed materials, tools, and techniques; on the other hand the associated capabilities are spawning novel applications and market opportunities. This year's one-day workshop focuses on the topics of nanotechnology, bioelectronics, and energy. Invited experts from industry, academia, research labs, and consortia will share their vision of technical challenges and opportunities in these areas. Current and emerging device, interconnect, and packaging technologies will be discussed in depth. A poster session on the broader workshop topic of emerging device and packaging technologies has been added this year to provide additional presentation and discussion opportunities. Select vendors will exhibit products and services related to all aspects of the supply chain for microelectronics design and manufacturing.

Invited Speaker Topics

Nanotechnology
- Nanofabrication
- Nanoelectromechanical Systems
- Nanofluidic Devices

Bioelectronics
- Biochips
- Biosensing
- Biosecurity

Energy
- Solar Cells
- Energy Harvesting
- Micro Power Generators

Poster Session

Abstracts are invited for consideration to the poster session in emerging device and packaging technologies (not limited to nanotechnology, bioelectronics, or energy).

Poster Abstract Submissions: Two pages (topic, summary of significant results and conclusions – WORD or PDF files only). Abstract must include author names, affiliations, addresses, and e-mail address of lead author.

Submission Deadline:	August 29, 2008
Submitting Address:	melmiller@ieee.org
Acceptance Notification:	September 19, 2008
Final Presentation Due:	November 5, 2008

Sponsporships and Vendor Displays: This is a great opportunity to promote your company or product. For more information, contact Vasu Atluri vpatluri@ieee.org or Chuck Weitzel c.weitzel@ieee.org (sponsors) and Steve Rockwell steve.rockwell@ieee.org (vendors).

Workshop Registration: On-line registration will open in August at *www.acteva.com/go/ieeephxsecworkshop2008*

33RD INTERNATIONAL ELECTRONICS MANUFACTURING TECHNOLOGY CONFERENCE IEMT 2008

4th-6th November, 2008 **Parkroyal Hotel, Penang, MALAYSIA**

The 33rd International Electronics Manufacturing Technology (IEMT) Conference is the premier IEEE event devoted to the manufacture of electronic, opto-electronic and MEMS/sensors devices and systems. IEMT is an established International conference of long standing organized by the Components Packaging and Manufacturing Technology (CPMT) Society of IEEE. IEMT 2008 is being organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from CPMT's Santa Clara Valley Chapter.

IEMT 2008 will feature short courses, technical sessions, and exhibitions. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation. IEMT 2008 is an international forum, providing opportunities to network and meet leading experts. Since the 1980's and 1990's, IEMT has gained a reputation as a premier electronics materials and packaging conference and is well attended by experts in the field of electronic packaging from all over the world.

Visit our website: cpmt.ieeemalaysia.org

SEMI-THERM®

Semiconductor Thermal Measurement and Management Symposium

Fairmont Hotel, San Jose CA USA March 15th-19th, 2009

CALL FOR PAPERS

SEMI-THERM is the world's premier forum specifically dedicated to thermal management of electronics. The symposium fosters the exchange of knowledge between industry academics, experts and practitioners on the latest advances in electronics thermal management.

SEMI-THERM is soliciting papers on current thermal management technologies and practical application issues, modeling and measurement of electronic components and systems in the following areas:

Component to System level thermal management:
Die, Package, Board and Systems Level

Packaging Materials:
Interface, Spreading, Nanotechnology, Material Characterization, Composites

Modeling and Analysis:
CFD, Compact, Finite element, Thermal Limitations

Cooling technologies:
Conduction, Convection, Radiation, Air, Liquid, Two Phase, Fans and Blowers, and Solid State

Applications:
Consumer, High Volume, Harsh Environments, LED, Medical, Telecom, Portable, Automotive, Solar Photovoltaic, Military, Power and Storage Systems

Selection of papers for presentation is solely based on the extended abstract. The abstract should provide a complete summary of the proposed paper comprising work or result not previously presented or published.

The abstract should be between 2 and 5 pages of single spaced text giving the key results, findings and conclusions, supported by additional pages of figures, tables and references as appropriate. Abstracts must demonstrate that proposed papers are appropriate for SEMI-THERM and of high technical quality.

Author Deadlines
Abstract Deadline: **September 15, 2008**
Abstract Acceptance Notification: **November 1st, 2008**
Photo-ready Full Manuscript Due: **December 15th, 2008**

Plan to attend and consider giving a paper –

Visit our website:

www.semi-therm.org

IMPACT 2008:

3rd International Microsystems, Packaging, Assembly and Circuits Technology

held jointly with **EMAP 2008:**

10th International Conference on Electronics Materials and Packaging

October 22 to24, 2008
Taipei Nangang Exhibition Hall

"Creative Collaboration, More Than Packaging"

Organized by IEEE CPMT-Taipei, ITRI, IMAPS-Taiwan, ISU University, SMTA and TPCA, the 3rd IMPACT and the 10th EMAP Joint Conference and TPCA Show 2008 are expected to bring together scientists, engineers and experts actively engaged in research and development on Microsystems, IC Packaging, Assembly, Materials and PCBs to discuss the current progress and emerging technologies in the fields

Plan now to attend. Visit:

www.impact-emap.org

2nd Int'l Conference on Thermal issues in Emerging Technologies, Theory and Applications (ThETA2)

December 17 – 20, 2008 Cairo, Egypt

Papers due: July 31, 2008

Emerging Technologies in various domains, including Microelectronics, Nanotechnology, Smart Materials, Micro-Electro-Mechanical Systems, Biomedical engineering as well as New Energies, all raise many issues related to thermal effects and interactions. The importance of such effects is continuously increasing to a point where they become a dominant factor in determining the performance of such technologies.

Parallel to the conference, a set of workshops will be conducted, aiming at disseminating advances made in different areas to the academic and industrial public in Egypt, fostering network creation with renowned international research centers as well as giving an impulse to academic/industrial cooperation.

Find out more! **Contact:** **thetaconf@gmail.com**

IEEE Components, Packaging and Manufacturing Technology Society
Marsha Tickman, Executive Director
PO Box 1331 / 445 Hoes Lane
Piscataway, NJ 08855 USA

Visit our website
www.cpmt.org

Download the PDF version of this NEWSLETTER, to circulate to other professionals

www.cpmt.org/newsletter/