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www.cpmt.org
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President's Column…..

Dr. William T. Chen
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President, IEEE CPMT Society
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Greetings!!!

The world is going through the worst economic recession of all times. The electronic industry -- our industry -- is suffering together with many industries. Cutbacks are affecting research and educational institutions alike. Almost daily we read or hear of companies retrenching, implementing layoffs and job cuts. We expect that many in our profession are in the jobless situation or are facing such prospects. In my contacts with the CPMT community we learn and share a sense of this changing reality – a new reality.

What is our society vision and strategy going forward? We have had good discussions on the CPMT value propositions in previous President's Messages in this newsletter. The value propositions for our society – publications, conferences, education, technical committees, membership and chapters, recognitions and awards – are well understood. As professional engineers, these CPMT value propositions revolve around some simple words describing tools of our trade: knowledge and learning, experience and judgment, and networking. In this changing reality, all of us need to sharpen and empower our tools of trade at all times.

One important topic that concerns all of us in the Society will be to broaden our professional and technology reach for our conferences, publications, technical committees, education, membership and chapter activities. While our nucleus has been electronic components technology and manufacturing, our CPMT Society Field of Interest is much broader. Our VP for Publications Wayne Johnson and his publications committee have been talking to me about increasing the journal coverage to electronic manufacturing. Rolf Aschenbrenner, VP Conferences, Rao Bonda, VP Technical and Al Puttlitz, VP Education are working towards organizing workshops, forming new technical committees and educational courses in new and emerging areas such as flexible electronics and print electronics, in medical and health electronics, and solar packaging. Our Strategic Director for Awards Kitty Pearsall has been exploring with her committee recognition of exceptional achievement outside the traditional CPMT community. The Regional Strategic Directors and Strategic Director for Chapters and Membership have brought focus to CPMT activities across the globe.

For all of us, volunteers in the CPMT Society -- we have been held together by a strong tie -- belonging to and pride in the CPMT community, and commitment in the volunteer service. We have shared ideas, argued and fought over them over the years. We see that 2009 may be a changing period for our profession and our industry. An important question that we will need to address is how would IEEE and CPMT change to meet the changing times for our membership, our profession and our industry? How do we plan for this change together, in our vision, and direction for the coming years?

I expect that there will be downward trends for membership renewal and for new membership. I do want to pass the word out that those of our members who have become unemployed are eligible for 50% off IEEE and CPMT dues and subscriptions. They will be able to exercise this discount when it comes time to renew for 2010. This discount also applies to new membership as well. Additionally, IEEE has a number of career resources, including a job site listing to connect those who have jobs and who need jobs:

www.ieee.org/careers

As always, I welcome and encourage your feedback.

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IEEE CPMT Society Newsletter
Spring 2009
Index

Circulate your printed or PDF copy of this NEWSLETTER to co-workers.

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Chapters and Student Branches

Refer to www.cpmt.org for CPMT Society Chapters and Student Branches list

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2009/2010 Deadlines for Submitting Articles:
May 25th, 2009 **August 25th, 2009**
November 25th, 2009 **February 25th, 2010**

Only Articles sent to nsltr input@cpmt.org will be included in the newsletter

Members-only Web (www.cpmt.org/mem/)
UserName: [available to Members --
Password: join CPMT!]

CPMT Society News:

CALL FOR CANDIDATES

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of this Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways -- either by the Society Nominating Committee, or by petition.

This year's election is the fourth in which members-at-large will be elected to achieve totals proportionate to the geographic distribution of CPMT members. Voting members will elect members-at-large from within their Region only (that is, members in Region 8 will vote for members-at-large from Region 8, etc.)

Elected Members of the Board of Governors must be willing to attend two annual Board meetings and participate actively in areas of their interest (publications, conferences, membership development, chapter development, etc.) The term of office for this election is 1 January 2010 through 31 December 2012.

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can become a candidate via petition by following the procedures below.

- Prepare a petition that contains your name, member number, and statement of your qualifications for office.

- Provide lines for signatories. Each line should include space for a printed name, member number, and signature.

- Have the petition signed by a MINIMUM of 46 CPMT Society members in good standing (Student grade members are not eligible to sign.)

- Submit your petition by mail no later than Friday, 25 July 2008 to:

CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA

OR

- Request establishment of electronic petition process, allowing signatures to be collected on-line.

You must contact Marsha Tickman to implement electronic petition process.

Membership status of all signatories will be validated. It is suggested that you gather more than 46 signatures in order to assure meeting the minimum required number of valid signatures.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at m.tickman@ieee.org.

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Congratulations to IEEE CPMT Fellows Class of 2009

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Moises Cases
USA
for contributions to design and noise control for power and signal distribution in digital systems

Shen-Li Fu
Taiwan
for contributions to electronic packaging research and education

Yoshitaka Fukuoka
Japan
for development of multichip module and high density substrate technologies

Lih-Tyng Hwang
USA
for contributions to System-in-a-Package technologies

Sung Kang
USA
for contributions to lead-free solders in microelectronics

James Knighten
USA
for contributions to understanding electromagnetic noise coupling paths for product compliance with regulatory standard

Mali Mahalingam
USA
for contributions to packaging and thermal performance of semiconductor electronics

Timothy Maloney
USA
for contributions to electrostatic discharge protection of semiconductor components

Chandrakant Patel
USA
for leadership in thermal and energy management in data centers

Omar Ramahi
Canada
for contributions to computational electromagnetics in electromagnetic compatibility

Gregory Taylor
USA
for contributions to mixed signal circuit technology for microprocessors

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New IEEE CPMT Senior Members

The members listed below were recently elevated to the grade of Senior Member.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields for a total of 10 years and have demonstrated 5 years of significant performance. Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html.

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Belarus Section, Belarus

Steve Bezuk
San Diego Section, USA

W Bottoms
Santa Clara Valley Section, USA

Antonio Ciccomancini-Scogn
Boston Section, USA

Joseph Diepenbrock
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Ezra Gershon
Long Island Section, USA

Stephen Hellriegel
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Tuula A Ilmorinne
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Toronto Section, Canada

N Slater
Toronto Section, Canada

Yuming Tao
Ottawa Section, Canada

Klaus-Juergen Wolter
Germany Section, Germany

Xin Wu
Central Texas Section, USA

Luhua Xu
Coastal Los Angeles Section, USA

John Zhang
Northern Virginia Section USA

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Student Branch News:

Interconnection Techniques in Electronics (TIE)– Professional Student's Contest

submitted by Cocoru Vlad, Chair of IEEE CPMT Student Branch Chapter of University Politehnica of Bucharest, Romania— vlad.cocoru@cetti.ro

At the beginning of April, between 9th and 12th, Galati, Romania, was home of the XVIIIth edition of an increasingly popular students' contest: **Interconnection Techniques in Electronics (TIE- www.tie.ro)**. The main organizer of the event was "Dunarea de Jos" University, Faculty of Electric and Electronics Engineering leaded by Prof. Dorel Aiordachioaie. The core of this

event is to test the participants' ability to find a professional solution to a real electronics interconnection problem.

The Romanian Student Branch Chapter is involved together with the IEEE-CPMT Hu&Ro Joint Chapter (Chair Professor Dan Pitica) in organizing this event and takes full credit for training the participants.

This competition gathers the most skilled and trained undergraduate students from the majority university campuses across Romania.

The main difference for this edition, compared to the past ones, is that we have invited our Hungarian colleagues from the Budapest University of Technology and Economics, Department for Electronic Technology (Head of the Department Professor Harsany Gabor). The students were accompanied by Professor Illyefalvi-Vitez Zsolt and Ms. Batorfi Reka. This was also the first edition to be held in English.

Professor Nihal Sinnadurai, IEEE Fellow, IEEE Distinguished Lecturer has presented to the participants the place of IEEE in the professional world and how important is for the young students to join a.s.a.p. this community.

The sole participation to this contest as a student implies that you have the required skills of a CAD designer. This competition is recognized by employers as a real certification of participants' knowledge level.

The subjects are created by a team of professionals who deal with CAD topics and winners from past editions of the TIE contest.

Fig. – Brainstorming session for creating the proposed subject for this edition

The topic purposed this time refers to the command of an integrated video camera and signal transmission though USB port. The design in Schematics and in Layout is highlighted: The correct implementation of decoupling capacitors, the separation of analog and digital ground layers are important issues, but special attention is paid to the problems that could appear in the actual practical PCB design phase: the signals and high speed routes integrity for multiple layers in printed circuit boards.

The real issue is not the difficulty of the problem (at this level, all participants are likely to be able to fully answer the given problem), but to do that in a very short time (only 3 hours, when the required time to fully solve the problem would be above 5). Therefore, no one is able to achieve the maximum available score, and the winners are expected to resolve as many problems as possible in the given time.

The first three ranked students receive a 10 month scholarship. Additionally, the winner of the TIE contest, Bogdan Raducanu, was awarded by CPMT Society with a full year IEEE CPMT Membership**.**

Figure – awarding the winners. From right to left: ***Prof. Paul Svasta*** *(SBC Advisor),* ***Bogdan Raducanu*** *(TIE 2009 winner, 3rd year student at Electronics, Telecommunication and Information Technology, Bucharest), Adrian Petrariu (TIE 2009 first runner-up, "Stefan cel Mare" University of Suceava),* ***Alexandru Coman*** *(TIE 2009 second runner-up, "Dunarea de Jos" University of Galati).*

All the participants expressed their interest for the TIE event and many of them, including our Hungarian friends, claimed their intention to attend the next year edition, which will take place in Cluj Napoca.

At the end, there was a very pleasant social event (boat trip on the Danube) and a closing ceremony in the last afternoon of staying in Galati. With this occasion, many contacts have been made which are likely to turn up into future collaborations and even friendships. Professor Paul Svasta, the SBC Advisor, pointed out the importance of IEEE-CPMT Politehnica University of Bucharest Student Branch Chapter to promote round of our country the aim of IEEE-CPMT Society.

We wish to all the participants all the best until the next year!

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IEEE CPMT Society Newsletter
Send inputs, suggestions, and articles by email to
nsltr-input@cpmt.org
….. Editor

Publications News:

Announcing Upcoming Special Sections
Transactions on Advanced Packaging

May 2009
ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=6040

Special Section on High-Speed I/O Channels

Wendem T. Beyene, Guest Editor
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Increase in integrated circuit data processing capabilities has driven the need of faster data transmission between chips and subsystems. As transistor technology has scaled and data rates gradually exceeded several gigabits per second, the high-speed I/O channels have limited the performance of digital computers and communication networks. Consequently, researchers with expertise in board and packaging, transceiver design, signal processing, and communications have worked hard to mitigate the signal degradation caused by the channel. As a result, there has been significant improvement, over the last decade in the design, analysis and optimization of high-speed I/O channels. More than ever now, researchers from various fields need to readily communicate and collaborate to further improve the performance of high-speed I/O channels.

This Transactions' "**Special Section on High-Speed I/O Channels**" has a twofold purpose. First, the section presents a review and a snapshot of the latest work on high-speed I/O channels by researchers from both academia and industry. I hope the section will be of interest to the IEEE Advanced Packaging community and will inspire further study and research in this exciting topic. Second, this section seeks to encourage readers and researchers from various disciplines, including circuit and systems, architecture and communications, to contribute papers that describe their research on this topic to the Transactions of Advanced Packaging.

The special section is organized around **10 invited papers** that are grouped into four main areas. The first group of papers deals with the modeling and analysis as well as power integrity characterization arising in the design of high-speed links. The paper entitled "*Modeling and analysis of high-speed I/O links*" gives comprehensive review of modeling and analysis of high-speed I/O channels and presents techniques to co-optimize the link architecture, circuit and interconnect as well as to establish the power-performance tradeoffs. The second paper is "*On-die power supply noise measurement techniques*" and focuses on the latest methods in characterization and analysis techniques of power supply noise that has become increasingly useful in the characterization of on-chip signal and noise to improve the robustness of the high-speed I/O circuitry.

The second group of papers is on statistical system simulation techniques. The paper entitled "*Statistical simulation of physical transmission media*" reviews the basic theory of statistical modeling and simulation methods used in design optimization of high-speed links and presents methods to include correlated jitter and data in the system simulation. The next paper is dedicated to "*Channel coding for high-speed links: A systematic look at code performance and system simulation*". The paper analyzes error correction coding in high-speed links based on the system's error regions and channel's pulse response and provides techniques to extend the statistical simulation methods for coded high-speed links.

The papers in the third group concern link eye closure prediction and jitter analysis. The paper entitled "*Predicting microwave digital signal integrity*" develops the fundamental relationships between signal integrity and the bandwidth and reflections and gives a fast analytical method to derive the eye closure and to predict link jitter caused by the impedance discontinuities in the interconnects. The second paper, "*Jitter challenges and reduction techniques at 10 Gbps and beyond*" reviews the jitter challenges as the data increases and discusses jitter reduction techniques, including tracking via clock recovery, equalizations, DCD cancellation to avoid jitter amplification.

The fourth group of papers is on design, analysis, and characterization of high-speed links using four different channels: AC/DC bidirectional link, parallel interfaces, serial link, and fiber optics channels. The paper entitled "*Frequency-division bidirectional communication over chip-to-chip channels*," presents techniques for frequency-division bidirectional communication over chip-to-chip channel using both AC and DC links on the same physical channel. The next paper is "*Advanced modeling and accurate characterization of 16Gb/s memory interference*" and discuss the modeling and characterization of a complete link running at *16 Gb/s* and presents correlations between system simulation results and data from on-chip and off-chip measurements. The following paper is "*Is 25 Gb/s on-board signaling viable?*" and presents a study of distance and speed limits of electrical link and discuss the design, modeling, and simulation of a *25 Gb/s* on-board signaling. The final paper entitled "*160 Gb/s bidirectional polymer-waveguide board-level optical interconnects using CMOS-based transceivers*" presents the development of parallel optical interconnect technologies using polymer waveguide integrated in PCBs and demonstrates the performance of the complete link using *32* polymer waveguides achieving a *160 Gb/s*.

It is a great honor for me to be the editor of this special section. I wish to express my gratitude to the authors who contributed excellent research papers. Although the papers were invited, two or three specialists nevertheless reviewed each paper. I am grateful to all the referees and especially to those who were kind enough to review and give their valuable suggestions and feedbacks to the authors to make this special section possible

I would like to thank J. Schutt-Ainé and G. Subbarayan for their continued support with the special section. I also want to acknowledge M. Tickman for her editorial and coordination efforts throughout this project.

Download these papers today, from IEEE's Xplore database:

ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=6040

Special Section on Packaging for Micro/Nano-Scale Systems

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It has been said for years that the 21st century should be the MEMS/NEMS century – as the 20th century has been labeled the IC century. However, this may not come true if packaging issues cannot be resolved physically and economically. Furthermore, the complex MEMS/NEMS packaging is often application-specific and there is still no standard to follow. With two former well-received special issues on MEMS/NEMS Packaging published in IEEE Transactions on Advanced Packaging in 2003 and 2005, we are honored to continue organizing this special section on packaging for micro/nano-scale systems. As the existing MEMS/NEMS products grow rapidly and new applications emerge constantly, the MEMS/NEMS industry has been continuously facing tremendous challenges due to more rigorous device performance specifications, harsher operating environments, and lower price requirements. Micro/nano-scale packaging is crucial to device interconnection and system integration and usually is a roadblock to overall product cost savings. Therefore, it is becoming more and more critical to all the industry sectors including automotive, heavy duty, aerospace, healthcare, consumer electronics, and many others involved in MEMS/NEMS production or applications.

This special section brings together 11 papers. In addition to the topics on specific MEMS/NEMS device interconnection and system integration, this special section also includes interesting and exciting studies in thermoelectric refrigeration and leakage characterization. The first paper is related to micro-interconnection. K. Chen, J. Salvia, R. Potter, R. T. Howe, and T. W. Kenny present a novel packaging technology for RF MEMS devices and evaluate the utility of silicon interconnects for RF applications. They evaluated performance and created an equivalent lumped-element model for silicon interconnects for fully-encapsulated RF MEMS devices. The next two papers are about biochemical and optical sensors. E. Ghafar-Zadeh, M. Sawan, and D. Therriault proposed a microfluidic packaging technique for lab-on-chip applications. The simulation, fabrication and chemical testing results of the implemented hybrid system incorporating microelectronics and microfluidics are presented to prove their novel concept. In the following paper, C. X. Premachandran, K. Chen, J. Singh, J. Teo, Y. Xu, N. Chen, and C. Sheppard developed a miniaturized optical bioprobe package using a 3D micro mirror and tested it for bio-imaging applications.

The last eight papers are related to technology development and characterization including thermoelectric refrigeration, cooling, leakage measurement, sealing, a burn-in testing device, electromigration and thermomigration. Thermoelectric refrigerators offer several advantages over vapor-compression refrigerators but past work in this area has neglected the impact of thermal and electrical contact resistances. A. Pettes, M. Hodes, and K. E. Goodson presented an innovative methodology to optimize thermoelectric refrigeration in the presence of thermal boundary resistance. In the sixth paper, D. Gerlach, D. Gerty, R. Mahalingam, Y. Joshi, and A. Glezer proposed a design for cooling 3D stacked chip electronics by interleaved solid spreaders and synthetic jets. The velocity field of the active heat sink is mapped using particle image velocimetry and the thermal performance is characterized using a surrogate heater and embedded thermocouple sensors. To quantify the true leak rate of micro to nano-liter packages, A. Goswami, B. Han, S.-J. Ham, and B.-G. Jeong proposed a new method using a helium mass spectrometer. The next three papers are related to sealing technology, although each one demonstrated a different approach. I. Zine-El-Abidine and M. Okoniewski developed a novel all SU-8 packaging method for MEME devices. The low-temperature and low-cost process allows for non-hermetic as well as hermetic packaging. In the next paper concerning the cost for mass production, J. S. Lee, F. Faheem, J. T. Kim, J. D. Jung, J. Y. Kim, J. D. Kim, and C H. Lee proposed an innovative cost-effective MEMS packaging using copper lead frames as a pre-plated frame. The paper by J. Kim, B. Jeong, M. Chiao, and L. Lin demonstrated the feasibility of ultrasonic bonding for hermetic MEMS packaging at low temperature. They describe the ultrasonic bonding and hermetic sealing processes as well as the characterizations of bonding tools and equipment setups. For wafer-level burn-in testing, F. Wang, X. Li, and S. Feng designed and fabricated a new type of probe card using a silicon and nickel composite micromachining technique. The last paper concerns electromigration and thermomigration because they are critical to the reliability of next generation nanoelectronics. S. Li, M. Abdulhamid, and C. Basaran developed a model and simulated electromigration and thermomigration to evaluate degradation in the solder joints under high current densities and temperature gradients.

Finally, we would like to thank all the authors, reviewers, and editing staff for their hard work to get this special section published successfully.

J. Albert Chiou, Associate Editor
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Download these papers soon, from IEEE's Xplore database:

ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=6040

Special Section on Wafer Level Packaging: Interconnects for Enhanced Reliability

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Wafer Level Chip Scale Packaging (WLCSP) has seen wide spread acceptance in the portable industry in the past few years. In fact, take apart any cell phone nowadays, and one would be hard pressed not to find at least one such package form factor tucked away somewhere on the high density PCB.

In order to get an update on the status of the WLCSP technology across the industry, the WLCSP Forum (www.wlcspforum.org/) conducted an industry-wide survey during the Spring and Summer of 2008, to establish a more comprehensive view of WLCSP technologies, especially in the area of reliability requirements. Half of the companies surveyed were IDMs, and the other half split between fabless semiconductor companies and OEMs. The results indicated that configurations of bump on pad and bump on redistributed layers were common, with sizes expanding up to 225 I/O at 0.4mm pitch. High silver solder alloys with SAC405 and SAC305 were used for applications where thermal cycling performance requirements were critical. However, there was a growing interest in low Ag alloys, namely, SAC105, SAC125, and doped variants of SAC105 solder alloys. Close to 1/3 of the respondents were currently using this solder alloy for drop test sensitive applications. End users cited low-cost, small footprint, and high reliability as three key factors in their selection of the package form factor. A ball pitch of 0.5 mm was predominant, but 0.4 mm will likely take over within the next two years. Over 1/3 of the users were already developing or have already qualified 0.3 mm pitch.

This fourth Special Section on Wafer Level Packaging adds to the considerable body of peer-reviewed papers in this area. The first paper from IME (C.S. Premachandran *et al.*) describes a 3D wafer level package containing an accelerometer. Proper sealing is required to ensure hermeticity. The second paper from NUS and U. Arkansas (E. Liao *et al.*) discusses about the design, fabrication, and characterization of a novel chip-to-package interconnect - the planar microspring. In the third paper, the folks at PARC (E. Chow *et al.*) show their microspring compliant interconnects enabling a large die to be soldered to an organic board without the use of underfill. And, the fourth paper from NTHU and ASE (M.C. Yew *et al.*) proposed a solder on rubber concept to minimize joint stresses for enhanced board level reliability.

I would like to thank all the reviewers for this special issue. Many thanks also to Marsha Tickman of IEEE for her support.

IEEE Xplore® Table of Contents Alert

Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our CPMT *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is:

ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

If you already have an IEEE web account, you may sign in and select those journals you wish to track. If you don't have an account, all it takes is your name and email address!

Then simply click the Alert Status box next to the journals you wish to monitor. You will receive an email each quarter when that journal is posted to Xplore.

Similarly, if you prefer to receive information by RSS feed, you may add our journals' feeds to your Reader. You'll get a listing of the papers in that issue, along with full abstracts and a link for downloading the paper. The RSS links are shown on this same web page.

Here are the journals we suggest you select for monitoring:

- Advanced Packaging, IEEE Trans on
- Components and Packaging Technologies, IEEE Trans on
- Electronics Packaging Manufacturing, IEEE Trans on

*****

Visit CPMT on the Web at: **www.cpmt.org**

CALL FOR PAPERS

Special Section on Solid-State Lighting Technologies

IEEE Transactions on Components and Packaging Technologies

In the 19th century, one of the most important inventions in terms of changing how people lived and worked was the incandescent light bulb. Starting in 1802 with Sir Humphry Davy's first demonstration of incandescent light, it took over 100 years of research before evolving into the incandescent light bulbs that we have today, and there are countless numbers of them in use in homes, cars, traffic lights, and commercial buildings all around the world and in outer space. As the world becomes more conscious of energy usage, with lighting accounting for approximately 20% of the electricity use in developed countries, the inefficiencies of incandescent bulbs have led to significant governmental support for energy-saving alternatives. The U.S. Department of Energy hopes to reduce electrical consumption for lighting across the country by 50 percent by the year 2025. Some of the most recent LED technologies are given below.

www.lumination.com

www.cree.com www

lumileds.com

The future seems bright for solid-state lighting technologies. With lifetimes of 50,000 to 60,000 hours and light outputs of over 100 lumens per watt, solid-state lighting offers better performance than many other lighting technologies. It is expected that it will replace all of the lighting technologies during next decade. Their lack of hazardous materials, such as mercury or halogen gases, makes them a more environmentally friendly alternative to fluorescent lamps. However, they are currently high cost and unable to match the light output of high-wattage light bulbs due to temperature limits on the materials. Global efforts to make SSL technology affordable are underway. This includes LED chips, packaging, thermal management, driver electronics, fixtures, and integration.

While the 19th century was the time for development of the incandescent light bulb, the 21st century is the time for development of solid-state lighting for residential, commercial, and industrial applications. We would like to draw attention to the recent efforts in this technology by publishing a special section in the *IEEE Transactions on Components and Packaging Technologies*, dedicated to solid-state lighting.

Topics of interest include, but not limited to:

- LED chip/substrate technology
- Semiconductor material development
- Packaging
- Thermal management
- Light quality (CRI, CCT) improvement techniques
- Efficiency improvements
- Fixture technologies
- System electrical efficiency and ROI (return on investment)
- Reliability

These developments can be in any solid-state lighting technology field. Both academic and industrial scientists are encouraged to submit their recent findings relevant to SSL technology. Papers will go through a rigorous review process based on IEEE guidelines and selected papers will be published in the CPT Transactions. Manuscripts are to conform to the standard IEEE transactions format, which can be found at www.cpmt.org/trans/transepm-auth.html.

Manuscripts must be submitted on line at ScholarOne Manuscripts: mc.manuscriptcentral.com/tcpt-ieee:

1. If you have not submitted a manuscript to the CPMT Transactions before -- create a user account for yourself.
2. Enter your Author Center and follow steps for submitting your manuscript.
3. *IMPORTANT:* In the Cover Letter window – note "Manuscript is submitted for Special Section on Solid-State Lighting Technologies.

To be considered for this Special Section, papers should be submitted by no later than **June 20, 2009.**

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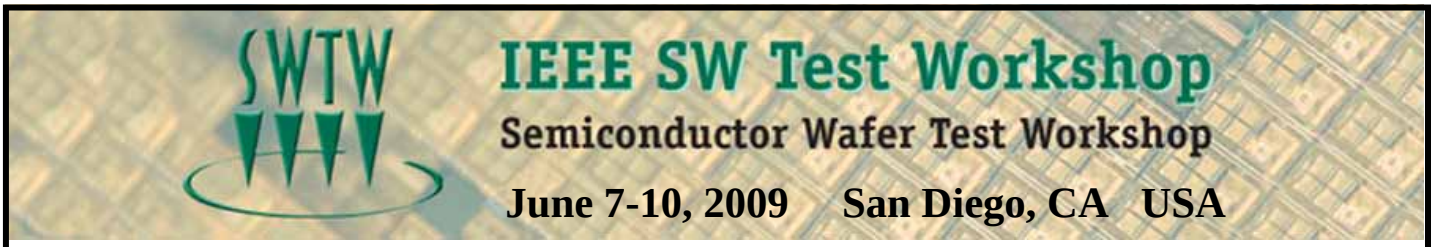


The Workshop begins on Sunday afternoon with a topical tutorial, followed by a welcome reception, dinner, and a Keynote Speaker. The Technical Program starts Monday morning with 30-minute presentations in theme-oriented sessions. SW Test EXPO 2009 will showcase many of the key suppliers to the wafer probe industry and, as always, there will be ample opportunities for networking. The workshop concludes on Wednesday at Noon after an awards presentation and luncheon.

SWTW is a probe technology forum with a relaxed atmosphere held at a beautiful resort hotel and has ample time dedicated to informal discussions and networking. This year's special social activities a Casino Night at the Resort. Dinner will begin at 6:00 PM with the tables opening for play at 7:00 PM going until the closing raffles at 10:00 PM. It's fun times with fun money for all!

Conference registration includes all meals, refreshments, social activities, and technical program and exhibit attendance, as well as the printed proceedings distributed at the Workshop.

TOPICS:

- New probe card and contractor technologies
- Challenges of 300-mm wafer probing
- Monitor and reduction of chip I/O pad damage
- Area array and C4 solder bump probing
- Parallel, multi-site probing
- Probe Card PCB Characterization
- Productivity improvements for high volume production
- Probe data collection, analysis, and management
- Probe Card cleaning, extending card life, improving cost of ownership
- Advances in Probe Card Analyzers and metrology tools
- Addressing unique probing requirements:

  - Copper I/O pads - RF and microwave - Mixed signal, low noise, and parametric - Low-k dielectric and Probe Over Active Circuitry - Probing for Known Good Die - High power devices - Probe Potpourri (anything goes)

Visit **www.swtest.org**

Dec. 1-3, 2009

Call for Papers

The 11th Electronic Material and Packaging Conference (EMAP 2009) is an international event organized by the School of Mechanical Engineering, Universiti Sains Malaysia (USM), with technical co-sponsorship from the CPMT Society of IEEE. EMAP 2009 will feature short courses, technical sessions, and an exhibition.

This conference is an international forum of experts and researchers for the exchange, dissemination and discussion of state-of-the-art technologies and recent developments in electronic materials, packaging, manufacturing and assembly. Since 1999, EMAP has gained a reputation as a premier electronic materials and packaging conference in the Asia-Pacific region where most of the electronic packaging activities are taking place.

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work.

The abstracts must be received by **June 15, 2009**. The final manuscript is due by October 1, 2009.

For more information, and the full Call for Papers, visit:

mechanical.eng.usm.my/EMAP2009

Visit EMAP the week before EPTC, in Singapore!

15th International Workshop on Thermal investigations of ICs and Systems

Leuven, Belgium -- 7-9 October 2009

THERMINIC Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. These questions are becoming more and more crucial with the increasing element density of circuits packaged together and with the move to nanotechnology. These trends are calling for thermal simulation, monitoring and cooling. Thermal management is expected to become an increasingly dominating factor of a system's cost. The growing power dissipated in a package, and the mobile parts of Microsystems, raise new thermal problems to be solved in the near future necessitating the regular discussion by the experts in these fields. Finally, there is an increasing need for accurate assessment of the boundary conditions used in the analysis of electronic parts, which requires a concurrent solution of the thermal behaviour of the whole system.

This year THERMINIC will address in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomena in "high-tech" systems.

Leuven is a university town located 30km to the east of Brussels. The workshop is hosted at the Faculty Club, a unique conference and banqueting centre, welcoming guests to the calm and tranquility of the 13th century Infirmerie of the Grand Beguinage and the Convent of Chièvres, built in 1561.

For information, and to register:

cmp.imag.fr/conferences

IEEE NANO 2009
July 26-30, 2009
Genoa, Italy

The conference brings together researchers, industry workers, entrepreneurs and funding agency leaders. It provides a forum for exchange of ideas, interaction, networking and collaboration for research and development in nanotechnology with special reference to the latest advances in nanotechnology.

CPMT's James Morris plans to have two sessions on nanotechnology in packaging applications.

For further information, and to register:

www.medinfo.dist.unige.it/ieeenano2009

Joint, with ACS and MRS, and IEEE-SSCS

Organic Microelectronics & Optoelectronics Workshop V

July 6-9, 2009
San Francisco

The workshop brings together a broad spectrum of chemists, materials scientists, physicists, and engineers from both industry and academia in a stimulating forum to share information and ideas in the emerging fields of Organic Microelectronics and Optoelectronics. The goal is to build an interdisciplinary community working on applications such as RFIDs, displays, sensors, photovoltaics and optical devices while addressing some of the common scientific and manufacturing challenges to help these technologies advance in a more rapid, effective, and economical manner.

The technical program focuses on the areas of synthesis, theory, novel processing/ patterning/fabrication and device physics through a series of presentations by renowned invited speakers and poster sessions.

Early-registration discounts through June 1.

Visit our website:

www.organicmicroelectronics.org

JUNE 15TH-18TH, 2009 IN RIMINI - ITALY

EMPC2009 EUROPEAN MICROELECTRONICS and PACKAGING CONFERENCE

The IMAPS EMPC, alternating annually with CPMT's ESTC, is Europe's premier conference planned every two years in a different European country, bringing together specialists from industry and academia.

The EMPC addresses "everything in electronics between the chip and the system".

TUTORIALS:

- Emerging Needs and Trends from 3D ICs to 3D Systems
- Physical and Electrical Design Modelling
- Electronics Reliability
- Recent trends in MEMS and BioMEMS packaging
- Advanced materials for High Power Electronics packaging

SEMINARS:

- Latest Advances in TSV Technology for 3D Integration
- Wirebonding

Exhibitors display equipment and programs.

EMPC is being held in Rimini, one of the most renown bathing resort towns in Italy,

TECHNICAL PROGRAM:

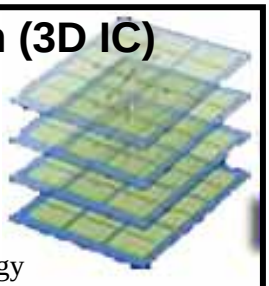
28 Sessions, plus Poster Sessions

Download the Advance Program – visit the website:

www.empc2009.org

IEEE International Conference on 3D System Integration (3D IC)

September 28-30, 2009 San Francisco



This conference combines the previous ASET and IEEE EDS Society sponsored **International 3D System Integration Conference**, held in Tokyo in 2007 & 2008, and the IEEE CPMT sponsored **3D System Integration Conference** held in 2005 & 2007 in Munich. The new, combined Conference will be held in San Francisco.

3D IC will cover all 3D IC topics, including 3D process technology, materials, equipment, circuits technology, design methodology and applications. The conference invites authors and attendees to submit and interact with 3D researchers from all around the world.

TOPICAL AREAS:

- 3D IC Technology
- 3D IC Circuits Technology
- 3D Applications
- 3D Design Methodology
- Test and Reliability of 3D Systems

To receive further information about 3D IC, or to register:

www.3dic-conf.org

ASTR 2009 Workshop on Accelerated Stress Testing & Reliability

October 7-9, 2009 Jersey City, NJ USA

The purpose of the ASTR Workshop is to share ideas on better ways of accelerating and detecting hidden defects, flaws, and weaknesses in electronic and electro-mechanical hardware that would result in failures during usage.

For more information:

www.ewh.ieee.org/soc/cpmt/tc7/ast2009

EPTC 2009 Singapore

11th Electronics Packaging Technology Conference
9th – 11th December 2009
Shangri-La Hotel Singapore

Mark Your Calendar for EPTC 2009

CALL FOR PAPERS

Selected Publication in IEEE

ABOUT EPTC

The 11th Electronics Packaging Technology Conference (EPTC 2009) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society.

EPTC 2009 will feature technical sessions, short courses/forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- **Advanced Packaging:** Wafer level packaging, 3D integration, TSV (through Silicon Via), embedded passives & actives on substrates, flip chip packaging, RF-ID, 3D SiP, Packaging solutions for MEMS, MOEMS, NEMS, Automotive electronics, optoelectronics
- **Interconnection Technologies:** wire bonding technology, flip chip technology, solder alternatives (ICP, ACP, ACF, NCP), under bump metallurgy, 3D and TSV connections, microbump, substrate technology,
- **Materials & Processes:** Materials and processes for traditional and advanced microelectronic systems, 3D packages, MEMS, solar, green and biomedical packaging that enhance mechanical, thermal, electrical and optical performance as well as cost effectiveness.
- **Modeling & Simulations:** Electrical Modeling & Signal Integrity, Thermal Characterization & Cooling Solutions: Mechanical Modeling & Structural Integrity
- **Quality & Reliability:** Component, board and system level reliability assessment, interfacial adhesion, accelerated testing and models, advances in reliability test methods and failure analysis.
- **Emerging Technology:** Packaging solutions for solar photovoltaic applications, systems and packaging in the areas of bioelectronics such as biomedical, bioengineering, biosensors and electronics for medical devices; wearable electronics, organic/printable electronics; portable power supplies such as fuel cells; and other novel packaging.

IMPORTANT DATES

Submission of abstract	**15th June 2009**
Notification of Acceptance	**1st August 2009**
Submission of manuscript	**1st October 2009**

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories (found under CONFERENCE TOPICS) for abstract review. All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 15th June, 2009. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance and publication instruction by 1st August 2009. The final manuscript for publication in the conference proceedings is due by 1st October 2009. Selected papers will be published in IEEE/CPMT journals.

OUTSTANDING TECHNICAL PAPERS

The conference proceeding is an official IEEE publication. Author(s) of Best Technical Paper and Best Student Paper will receive an award at the next conference.

CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings. Proposals for short courses can be submitted to seungwook.yoon@statschippac.com.

CALL FOR SPONSORSHIP / EXHIBITION PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. Potential exhibitors and sponsors may email secretariat@eptc-ieee.net for details.

General Chairs: Mr. James HOW / Mr. Yew Cheong MUI
Technical Chair: Dr. Seung Wook YOON

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UNIQUELY Singapore
www.visitsingapore.com

Conference information & contacts: Website: http://www.eptc-ieee.net Email: secretariat@eptc-ieee.net

Conference News:

CONFERENCES IN 2009:

2009 59th Electronic Components and Technology Conference (ECTC 2009)
May 25-29, 2009 San Diego, CA USA www.ectc.net
Contact: Jean Trewhella, jeanmh@us.ibm.com

2009 19th IEEE Semiconductor Wafer Test Workshop (SWTW 2009)
June 7-9, 2009 Paradise Point Resort, San Diego, CA USA
www.swtest.org
Contact: Maddie Harwood, maddie@cemamerica.com

2009 17th European Microelectronics and Packaging Conference and Exhibition (EMPC 2009)
June 15 -18, 2009 - Rimini – Italy www.empc2009.org
Contact: Pragma Congressi segreteria@empc2009.org

2009 3rd IEEE International Workshop on Advances in Sensors and Interfaces (IWASI 2009)
June 25-26, 2009 Trani, Italy
iwasi.poliba.it/iwasi2009
Contact: **Prof. Daniela De Venuto, d.devenuto@poliba.it**

2009 5th Annual Organic Microelectronics and OptoelectronicsWorkshop
July 6-9, 2009, San Francisco CA, USA
acswebcontent.acs.org/organicmicroelectronic
Contact: organic_microelectronics@acs.org

2009 International Conference on Electronics Packaging Technology/ High Density Design, Packaging and Microsystem Integration (ICEPT/HDP 2009)
August 10-13, 2009 Beijing, China
Contact: icept2009@tsinghua.edu.cn

2009 IEEE International Conference on Portable Information Devices (PORTABLE)
September 21-22, 2009 Anchorage, AK USA
www.ieeevtc.org/portable2009
Contact: Ephraim Suhir suhire@aol.com

2009 3rd International Conference on 3D System Integration (3DIC 2009)
September 28 – 30, 2009 San Fancisco, CA, USA
www.3dic-conf.org
Contact: P. Garrou pgarrou@rti.org

2009 31st Annual Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2009)
30 August – 4 September 2009 Anaheim, CA, USA
www.esda.org
Contact: Lisa Pimpinella lpimpinella@esda.org

2009 15th Int'l Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2009)
October 7 – 9, 2009 Leuven, Belgium
cmp.imag.fr/conferences/therminic/therminic2009
Contact: Chantal Bénis-Morel, chantal.benis@imag.fr

2009 4th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2009)
October 21-23, 2009 Taipei, Taiwan
www.impact.org.tw/2009/General
Contact: Ms.Yaffy Liu service@impact.org.tw

2009 55th IEEE Holm Conference on Electrical Contacts (HOLM 2009)
Sept. 14-16, 2009 Vancouver, BC, Canada
www.ewh.ieee.org/soc/cpmt/tc1
Contact: Alicia Zupeck a.zupeck@ieee.org

2009 18th IEEE Electrical Performance of Electronic Packaging (EPEP 2009)
October 19-21, 2009 Portland, OR, USA
www.epep.org
Contact: Kelly Sutton epd@engr.arizona.edu

2009 IEEE/CPMT Workshop on Accelerated Stress Test and Reliability (ASTR 2009)
October 7-9 2009 Jersey City, NJ USA;
www.ewh.ieee.org/soc/cpmt/tc7/ast2009
Contact: Cheryl Tulkoff ctulkoff@austin.rr.com

2009 11th Electronics Packaging Technology Conference (EPTC 2009)
9-11 December 2009, Singapore
www.eptc-ieee.net

2009 IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS 2009)
December 2-4, 2009 Hong Kong, China
www.edaps2009.org
Contact: edaps2009@ee.cuhk.edu.hk

CONFERENCES IN 2010:

2010 60th Electronic Components and Technology Conference (ECTC 2010)
June 1 - 4, 2010 Las Vegas, NV, USA
www.ectc.net
Contact: Jean Trewhella, jeanmh@us.ibm.com

3nd Electronics Systemintegration Technology Conference (ESTC 2010)
September 13-16, 2010 Berlin, Germany
www.estc.biz/outlook_estc_2010
Contact: Rolf Aschenbrenner,
rolf.aschenbrenner@izm.fraunhofer.de

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www.cpmt.org/conf

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Visit ieeexplore.ieee.org and download them

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Participate in Seminars, Workshops, and Conferences by Organizing and Attending

Additional Information at www.cpmt.org/conf/

Future Directions in IC and Package Design Workshop (FDIP)

October 18, 2009, Portland, OR USA

Special Topic: What Research is Planned for EM Tools and How Are They Made Available to Computer Designers

FDIP includes 7 talks on key topics; see the Advance Program for the listing. FDIP is held immediately before EPEP – be sure to schedule this extra day into your travel plans! Register by September 20th.

More information: **www.epeps.org**

CPMT and MTT Societies

18th Conference on

Electrical Performance of Electronic Packaging (EPEP 2009)

October 19-21, 2009
Portland, Oregon USA

Abstracts Due: July 18, 2009

The general subject of EPEP is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. The goal is to be the leading conference dealing with advanced and emerging issues in electrical design of interconnect structures and assurance of Signal Integrity. Authors are invited to submit papers describing new technical contributions.

For full submittal details, please visit:

www.epep.org

IEEE Components, Packaging and Manufacturing Technology Society
Marsha Tickman, Executive Director
PO Box 1331 / 445 Hoes Lane
Piscataway, NJ 08855 USA

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