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Transactions on Advanced Packaging

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Special Section on High-Speed I/O Channels

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Increase in integrated circuit data processing capabilities has driven the need of faster data transmission between chips and subsystems. As transistor technology has scaled and data rates gradually exceeded several gigabits per second, the high-speed I/O channels have limited the performance of digital computers and communication networks. Consequently, researchers with expertise in board and packaging, transceiver design, signal processing, and communications have worked hard to mitigate the signal degradation caused by the channel. As a result, there has been significant improvement, over the last decade in the design, analysis and optimization of high-speed I/O channels. More than ever now, researchers from various fields need to readily communicate and collaborate to further improve the performance of high-speed I/O channels.

This Transactions' "**Special Section on High-Speed I/O Channels**" has a twofold purpose. First, the section presents a review and a snapshot of the latest work on high-speed I/O channels by researchers from both academia and industry. I hope the section will be of interest to the IEEE Advanced Packaging community and will inspire further study and research in this exciting topic. Second, this section seeks to encourage readers and researchers from various disciplines, including circuit and systems, architecture and communications, to contribute papers that describe their research on this topic to the Transactions of Advanced Packaging.

The special section is organized around **10 invited papers** that are grouped into four main areas. The first group of papers deals with the modeling and analysis as well as power integrity characterization arising in the design of high-speed links. The paper entitled "*Modeling and analysis of high-speed I/O links*" gives comprehensive review of modeling and analysis of high-speed I/O channels and presents techniques to co-optimize the link architecture, circuit and interconnect as well as to establish the power-performance tradeoffs. The second paper is "*On-die power supply noise measurement techniques*" and focuses on the latest methods in characterization and analysis techniques of power supply noise that has become increasingly useful in the characterization of on-chip signal and noise to improve the robustness of the high-speed I/O circuitry.

The second group of papers is on statistical system simulation techniques. The paper entitled "*Statistical simulation of physical transmission media*" reviews the basic theory of statistical modeling and simulation methods used in design optimization of high-speed links and presents methods to include correlated jitter and data in the system simulation. The next paper is dedicated to "*Channel coding for high-speed links: A systematic look at code performance and system simulation*". The paper analyzes error correction coding in high-speed links based on the system's error regions and channel's pulse response and provides techniques to extend the statistical simulation methods for coded high-speed links.

The papers in the third group concern link eye closure prediction and jitter analysis. The paper entitled "*Predicting microwave digital signal integrity*" develops the fundamental relationships between signal integrity and the bandwidth and reflections and gives a fast analytical method to derive the eye closure and to predict link jitter caused by the impedance discontinuities in the interconnects. The second paper, "*Jitter challenges and reduction techniques at 10 Gbps and beyond*" reviews the jitter challenges as the data increases and discusses jitter reduction techniques, including tracking via clock recovery, equalizations, DCD cancellation to avoid jitter amplification.

The fourth group of papers is on design, analysis, and characterization of high-speed links using four different channels: AC/DC bidirectional link, parallel interfaces, serial link, and fiber optics channels. The paper entitled "*Frequency-division bidirectional communication over chip-to-chip channels*," presents techniques for frequency-division bidirectional communication over chip-to-chip channel using both AC and DC links on the same physical channel. The next paper is "*Advanced modeling and accurate characterization of 16Gb/s memory interference*" and discuss the modeling and characterization of a complete link running at *16 Gb/s* and presents correlations between system simulation results and data from on-chip and off-chip measurements. The following paper is "*Is 25 Gb/s on-board signaling viable?*" and presents a study of distance and speed limits of electrical link and discuss the design, modeling, and simulation of a *25 Gb/s* on-board signaling. The final paper entitled "*160 Gb/s bidirectional polymer-waveguide board-level optical interconnects using CMOS-based transceivers*" presents the development of parallel optical interconnect technologies using polymer waveguide integrated in PCBs and demonstrates the performance of the complete link using *32* polymer waveguides achieving a *160 Gb/s*.

It is a great honor for me to be the editor of this special section. I wish to express my gratitude to the authors who contributed excellent research papers. Although the papers were invited, two or three specialists nevertheless reviewed each paper. I am grateful to all the referees and especially to those who were kind enough to review and give their valuable suggestions and feedbacks to the authors to make this special section possible

I would like to thank J. Schutt-Ainé and G. Subbarayan for their continued support with the special section. I also want to acknowledge M. Tickman for her editorial and coordination efforts throughout this project.

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Special Section on Packaging for Micro/Nano-Scale Systems

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It has been said for years that the 21st century should be the MEMS/NEMS century – as the 20th century has been labeled the IC century. However, this may not come true if packaging issues cannot be resolved physically and economically. Furthermore, the complex MEMS/NEMS packaging is often application-specific and there is still no standard to follow. With two former well-received special issues on MEMS/NEMS Packaging published in IEEE Transactions on Advanced Packaging in 2003 and 2005, we are honored to continue organizing this special section on packaging for micro/nano-scale systems. As the existing MEMS/NEMS products grow rapidly and new applications emerge constantly, the MEMS/NEMS industry has been continuously facing tremendous challenges due to more rigorous device performance specifications, harsher operating environments, and lower price requirements. Micro/nano-scale packaging is crucial to device interconnection and system integration and usually is a roadblock to overall product cost savings. Therefore, it is becoming more and more critical to all the industry sectors including automotive, heavy duty, aerospace, healthcare, consumer electronics, and many others involved in MEMS/NEMS production or applications.

This special section brings together 11 papers. In addition to the topics on specific MEMS/NEMS device interconnection and system integration, this special section also includes interesting and exciting studies in thermoelectric refrigeration and leakage characterization. The first paper is related to micro-interconnection. K. Chen, J. Salvia, R. Potter, R. T. Howe, and T. W. Kenny present a novel packaging technology for RF MEMS devices and evaluate the utility of silicon interconnects for RF applications. They evaluated performance and created an equivalent lumped-element model for silicon interconnects for fully-encapsulated RF MEMS devices. The next two papers are about biochemical and optical sensors. E. Ghafar-Zadeh, M. Sawan, and D. Therriault proposed a microfluidic packaging technique for lab-on-chip applications. The simulation, fabrication and chemical testing results of the implemented hybrid system incorporating microelectronics and microfluidics are presented to prove their novel concept. In the following paper, C. X. Premachandran, K. Chen, J. Singh, J. Teo, Y. Xu, N. Chen, and C. Sheppard developed a miniaturized optical bioprobe package using a 3D micro mirror and tested it for bio-imaging applications.

The last eight papers are related to technology development and characterization including thermoelectric refrigeration, cooling, leakage measurement, sealing, a burn-in testing device, electromigration and thermomigration. Thermoelectric refrigerators offer several advantages over vapor-compression refrigerators but past work in this area has neglected the impact of thermal and electrical contact resistances. A. Pettes, M. Hodes, and K. E. Goodson presented an innovative methodology to optimize thermoelectric refrigeration in the presence of thermal boundary resistance. In the sixth paper, D. Gerlach, D. Gerty, R. Mahalingam, Y. Joshi, and A. Glezer proposed a design for cooling 3D stacked chip electronics by interleaved solid spreaders and synthetic jets. The velocity field of the active heat sink is mapped using particle image velocimetry and the thermal performance is characterized using a surrogate heater and embedded thermocouple sensors. To quantify the true leak rate of micro to nano-liter packages, A. Goswami, B. Han, S.-J. Ham, and B.-G. Jeong proposed a new method using a helium mass spectrometer. The next three papers are related to sealing technology, although each one demonstrated a different approach. I. Zine-El-Abidine and M. Okoniewski developed a novel all SU-8 packaging method for MEME devices. The low-temperature and low-cost process allows for non-hermetic as well as hermetic packaging. In the next paper concerning the cost for mass production, J. S. Lee, F. Faheem, J. T. Kim, J. D. Jung, J. Y. Kim, J. D. Kim, and C H. Lee proposed an innovative cost-effective MEMS packaging using copper lead frames as a pre-plated frame. The paper by J. Kim, B. Jeong, M. Chiao, and L. Lin demonstrated the feasibility of ultrasonic bonding for hermetic MEMS packaging at low temperature. They describe the ultrasonic bonding and hermetic sealing processes as well as the characterizations of bonding tools and equipment setups. For wafer-level burn-in testing, F. Wang, X. Li, and S. Feng designed and fabricated a new type of probe card using a silicon and nickel composite micromachining technique. The last paper concerns electromigration and thermomigration because they are critical to the reliability of next generation nanoelectronics. S. Li, M. Abdulhamid, and C. Basaran developed a model and simulated electromigration and thermomigration to evaluate degradation in the solder joints under high current densities and temperature gradients.

Finally, we would like to thank all the authors, reviewers, and editing staff for their hard work to get this special section published successfully.

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Special Section on Wafer Level Packaging: Interconnects for Enhanced Reliability

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Wafer Level Chip Scale Packaging (WLCSP) has seen wide spread acceptance in the portable industry in the past few years. In fact, take apart any cell phone nowadays, and one would be hard pressed not to find at least one such package form factor tucked away somewhere on the high density PCB.

In order to get an update on the status of the WLCSP technology across the industry, the WLCSP Forum (www.wlcspforum.org/) conducted an industry-wide survey during the Spring and Summer of 2008, to establish a more comprehensive view of WLCSP technologies, especially in the area of reliability requirements. Half of the companies surveyed were IDMs, and the other half split between fabless semiconductor companies and OEMs. The results indicated that configurations of bump on pad and bump on redistributed layers were common, with sizes expanding up to 225 I/O at 0.4mm pitch. High silver solder alloys with SAC405 and SAC305 were used for applications where thermal cycling performance requirements were critical. However, there was a growing interest in low Ag alloys, namely, SAC105, SAC125, and doped variants of SAC105 solder alloys. Close to 1/3 of the respondents were currently using this solder alloy for drop test sensitive applications. End users cited low-cost, small footprint, and high reliability as three key factors in their selection of the package form factor. A ball pitch of 0.5 mm was predominant, but 0.4 mm will likely take over within the next two years. Over 1/3 of the users were already developing or have already qualified 0.3 mm pitch.

This fourth Special Section on Wafer Level Packaging adds to the considerable body of peer-reviewed papers in this area. The first paper from IME (C.S. Premachandran *et al.*) describes a 3D wafer level package containing an accelerometer. Proper sealing is required to ensure hermeticity. The second paper from NUS and U. Arkansas (E. Liao *et al.*) discusses about the design, fabrication, and characterization of a novel chip-to-package interconnect - the planar microspring. In the third paper, the folks at PARC (E. Chow *et al.*) show their microspring compliant interconnects enabling a large die to be soldered to an organic board without the use of underfill. And, the fourth paper from NTHU and ASE (M.C. Yew *et al.*) proposed a solder on rubber concept to minimize joint stresses for enhanced board level reliability.

I would like to thank all the reviewers for this special issue. Many thanks also to Marsha Tickman of IEEE for her support.

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Special Section on Solid-State Lighting Technologies

IEEE Transactions on Components and Packaging Technologies

In the 19th century, one of the most important inventions in terms of changing how people lived and worked was the incandescent light bulb. Starting in 1802 with Sir Humphry Davy's first demonstration of incandescent light, it took over 100 years of research before evolving into the incandescent light bulbs that we have today, and there are countless numbers of them in use in homes, cars, traffic lights, and commercial buildings all around the world and in outer space. As the world becomes more conscious of energy usage, with lighting accounting for approximately 20% of the electricity use in developed countries, the inefficiencies of incandescent bulbs have led to significant governmental support for energy-saving alternatives. The U.S. Department of Energy hopes to reduce electrical consumption for lighting across the country by 50 percent by the year 2025. Some of the most recent LED technologies are given below.

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The future seems bright for solid-state lighting technologies. With lifetimes of 50,000 to 60,000 hours and light outputs of over 100 lumens per watt, solid-state lighting offers better performance than many other lighting technologies. It is expected that it will replace all of the lighting technologies during next decade. Their lack of hazardous materials, such as mercury or halogen gases, makes them a more environmentally friendly alternative to fluorescent lamps. However, they are currently high cost and unable to match the light output of high-wattage light bulbs due to temperature limits on the materials. Global efforts to make SSL technology affordable are underway. This includes LED chips, packaging, thermal management, driver electronics, fixtures, and integration.

While the 19th century was the time for development of the incandescent light bulb, the 21st century is the time for development of solid-state lighting for residential, commercial, and industrial applications. We would like to draw attention to the recent efforts in this technology by publishing a special section in the *IEEE Transactions on Components and Packaging Technologies*, dedicated to solid-state lighting.

Topics of interest include, but not limited to:

- LED chip/substrate technology
- Semiconductor material development
- Packaging
- Thermal management
- Light quality (CRI, CCT) improvement techniques
- Efficiency improvements
- Fixture technologies
- System electrical efficiency and ROI (return on investment)
- Reliability

These developments can be in any solid-state lighting technology field. Both academic and industrial scientists are encouraged to submit their recent findings relevant to SSL technology. Papers will go through a rigorous review process based on IEEE guidelines and selected papers will be published in the CPT Transactions. Manuscripts are to conform to the standard IEEE transactions format, which can be found at www.cpmt.org/trans/transepm-auth.html.

Manuscripts must be submitted on line at ScholarOne Manuscripts: mc.manuscriptcentral.com/tcpt-ieee:

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To be considered for this Special Section, papers should be submitted by no later than **June 20, 2009.**

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