President's Column (cont.):

Traditionally the CPMT Luncheon recognizes of achievements of many of our peers in the profession. We presented IEEE and CPMT Society awards recognized important and significant achievements and great contributions within our own community. We recognized best papers from CPMT transactions. This year, the Society created a new award, the CPMT Student Travel Award, which enabled sixteen students to participate in the ECTC Conference. It is an important message to the younger generation in our midst: the CPMT Society is their society and the ECTC conference is their conference.

This year we have started a tradition to honor and recognize the many dedicated volunteers in the ECTC program committees. Volunteers are the backbone of the ECTC, our Society and our profession. In this very difficult year, with the economy in trouble and the success of the ECTC in jeopardy, each and every one of the teams have worked long and hard to make this 59th conference the best ever.

Besides the professional development courses, panel sessions and technical programs, what does one do during ECTC? One of my favorite activities was the Best Practices Publication Workshop. It was held two times during the ECTC week. The workshop was led by Wayne Johnson, CPMT VP for Publications. The workshop is designed for those in our midst who do great research, make great presentations, and now want to write great technical papers and get them published in CPMT Transactions. In the workshop Wayne described the key attributes in a great journal paper and the best practices to achieve them. Developments in the electronic packaging industry are moving at a rapid and accelerating pace. It is crucially important to put one's significant research contribution into the best technical publications in our profession. Wayne will be holding the workshop at other CPMT Technical Conferences. Please be on the lookout for it.

ECTC is one of the many technical conferences in our global CPMT community. In my list of things to do is to complete the paper review assignment for EPTC conference in Singapore in December. In my own calendar for the month of August , there will be the ICEPT – HDP conference in Beijing, China, and the flexible electronics workshop in Binghamton NY. Please review the newsletter and the CPMT website for the complete listing.

The employment picture continues to be severe and daunting. In the spring message I mentioned that I expected deep downward trends for membership renewal and for new membership. Please pass the word out that for those of our members who have become unemployed they are eligible for 50% off IEEE and CPMT dues and subscriptions. They will be able to exercise this discount when it comes time to renew for 2010. This discount also applies to new membership as well. Additionally, IEEE has a number of career resources, including a job site listing to connect those who have jobs and who need jobs.
http://www.ieee.org/web/careers/home/index.html.

CPMT Society News:

Congratulations to IEEE CPMT Society Award Winners Presented at 59th ECTC in San Diego, CA

Submitted by Leonard W. Schaper, Kitty Pearsall, and Wayne Johnson

CPMT Field Award:

The 2009 IEEE CPMT Award, the most prestigious award in the CPMT fields of study, was presented to GEORGE G. HARMAN (LF'IEEE) - NIST Scientist Emeritus (Retired NIST Fellow), Consultant, Gaithersburg, MD, USA, at the 2009 ECTC Conference.

The citation reads: "For pioneering achievements in wire bonding technology."

George Harman was hired at NBS/NIST in 1950 as an Electronic Scientist. In 1955, he filed for a patent on an electroluminescent microwave detector (# 2,928,937). He then studied the high frequency properties of various electroluminescent materials and discovered a new class of ferroelectric electroluminescent materials. His first 15 papers were generally in the area of applied physics and were published in the J. Appl. Physics, and similar journals. He studied contacts and surface states of several new unstudied (at that time) semiconductors (SiC, BC, etc.) and in the process obtained several US semiconductor device patents.

In 1968, a Navy strategic missile under development (Poseidon) had major reliability problems in its wire bonded interconnections. The urgency resulted in Harman being assigned to help solve that problem. This led to an extensive laboratory investigation designed to understand ultrasonic bonding and its evaluation. He developed a 25 µm diameter constricted, floating-cone capacitor microphone to plot the ultrasonic vibration modes of tools at 60 kHz, and applied those measurement methods to understanding and solving other problems in ultrasonic bonding machines and processes. Later, he used a laser interferometer to refine those earlier measurements. In 1971 he started the ASTM F-01.07 committee to standardize wire bond testing methods, which included pull test, nondestructive test, and ball bond shear test. Also, standards for bonding wire inspection methods, etc., were developed during that period. Harman, who currently chairs ASTM Committee F-01.07 (Wire Bonding, Flip Chip, and Tape Automated Bonding), updated and re-balloted the original wire bonding standards in 2005-06. Note that Harman's IEEE fellow citation (in 1982) was "for development of process control and screening procedures for microelectronic welding and bonding". He continues to contribute to the wire bonding area. Recently, an extension of his laboratory work and publications on wire bonding to soft substrates led to applying those principles to wire bonding on Cu-LoK chips. Other recent publications discussed projected metallurgical wire bond problems in NASA extreme temperature planetary exploration probes.

During the 1970's, Harman contributed to the military standards for testing wire bonds (at that time these were the only semiconductor/packaging standards publicly available and in general use), attended JEDEC meetings, and contributed data to be incorporated in their standards. He wrote the bond pull test method for MIL-S-19500 which was subsequently added to MIL-STD-750C, and supplied data and curves for the most used wire bond pull test in MIL-STD-883. He wrote the first version of the nondestructive bond pull test in MIL-STD-883 and has defended its use numerous times, and his paper on that subject in the IEEE IRPS stands alone for the statistical and metallurgical understanding of that test method. Currently, that test is required for most critical parts flown by NASA.

In his NIST Fellow position, George Harman has served as a national and international consultant in the field of wire bonding, advising and solving problems in chip-package interconnections for numerous organizations each year. He has taught most US and many foreign engineers both metallurgical and practical aspects of wire bonding in the 8-hour short-courses sponsored by UAZ, IMAPS, HKUST, and many others organizations for 20 years. He used the well developed and organized content of such lectures, in 1989, and published the first edition, and in 1997 the second edition of the only book(s) on that subject. It is frequently referred to as "the wire bond bible" and has been used by thousands of engineers (over 5000 copies of second edition have been sold by McGraw Hill). Two wire bond manufacturers have given a copy with each major machine purchased ("to educate and save us time and service calls to our customers"). These books have been a major world-wide contribution to the field by Harman.

Most of George Harman's career has been engaged in understanding, standardizing, implementing improvements into the industry's tooling, and disseminating wire-bond technology. He is the individual most responsible for transforming a labor-intensive manual bonding technology whose results depended upon an operator's skill, with attendant poor reliability, to a well-understood, highly automated (>8 bonds per second) method with an outstanding reliability record. As a result of Mr. Harman's work, wire bonding has become the industry standard. It accounts for more than 95 percent of the interconnections made between chips and the next level of assembly in electronic products manufactured worldwide. Approximately 7x10(+12) wire bonds are created each year. George Harman's work has had a profound impact on the industry, and likely benefited anyone utilizing an electronic product.

CPMT Society Awards:

The CPMT Award Committee is made up of a 7 cross-geographic members chaired by Kitty Pearsall. Team members are Charles Lee, Ning-Cheng Lee, Ralph Russell, Kwang-Lung Lin, Klaus-Jürgen Wolter, Petri Savolainen and Ephraim Suhir. As you can imagine there are many challenges in selecting the single, "BEST" candidate for each of the 5 CPMT Categories: Outstanding Young Engineer, Electronics Manufacturing Technology, Exceptional Technical Achievement, Outstanding Sustained Technical Contribution and the David Feldman Awards. This year awards were once again presented at the CPMT Luncheon at the 59th ECTC Conference held in San Diego. We were fortunate to have his son and daughter receive his award in his absence. Congratulations to all the winners!!! Job well done!

Outstanding Young Engineer Award:

The Outstanding Young Engineer Award is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation. This year's award is being presented to **Dr. Madhusadan K. Iyenger** for his exceptional and sustained technical innovation over the last 5 years that has resulted in cutting edge cooling technology and products with realizable benefits to the IT industry and its' customers which has resulted in several patents and refereed publications. Dr Avi Bar-Cohen presented Madhusadan's award personally since he was his Graduate Studies Professor.

IEEE Mission

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity

Electronics Manufacturing Technology Award:

The Electronics Manufacturing Technology Award is given to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society. This year's award is being presented to **Ho-Ming Tong**. Dr Ho-Ming is known world wide for his pioneering development, manufacturing and implementation work in flip chip packaging in applications that spanned from high-end computing at IBM to cost sensitive applications covering computing, communications, consumer and car electronics at ASE, the world's largest IC assembly and test service provider. The award was accepted on behalf of Ho-Ming Tong by his son Carl Tong and daughter Irene Tong.

Exceptional Technical Achievement Award:

The Exceptional Technical Achievement Award is given to recognize an individual, or group of individuals for exceptional technical achievement in the fields encompassed by the CPMT Society. This year's award is being presented to **Dr. Sheng Liu** for his pioneering work on multi-physics and multi-scale modeling for manufacturing process modeling and reliability qualification coupled with the development of various validation tools. His work has resulted in many papers and publications in conference proceedings, 3 book chapters, 2 books (in preparation), over 300 technical papers, more than 70 patents filed or granted, and many keynote and invited talks. The award was accepted on behalf of Dr. Sheng Liu by his colleague.

Outstanding Sustained Technical Contribution Award:

The Outstanding Sustained Technical Contribution Award is given to recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society. This year's award goes to **Moises Cases**. He is a renowned expert in system level electrical packaging design and integration including system level timing for high performance digital systems encompassing multiple boards and cable subsystems which is noted by his numerous IBM and Professional awards, 50 issued patents as well as more than 92 publications in refereed journals.

David Feldman Award:

The David Feldman Award is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions. This year's award is being presented to **CP Wong**. Dr Wong has been untiring in his passion and dedication to the IEEE and CPMT Society by serving in various CPMT leadership roles for the last 22 years that include serving as President, CPMT BoG (numerous terms), Chair/Member of the CPMT Fellow Committee and several Executive ECTC roles, such as General Chair of ECTC, Materials and Process Technical Sub Committee, CPMT ECTC Rep for 16 continuous years, as well as numerous IEEE roles. All of this in addition to having been recognized in 2002 as the first recipient of the CPMT Exceptional Technical Award highlight CP as an excellent David Feldman recipient.

CPMT Transactions – Best Paper Awards:

At the ECTC CPMT Award luncheon, awards were presented for the best 2008 papers published in the Transactions on Advanced Packaging and in the Transaction on Components and Packaging Technologies. The top papers were selected based on reviewer

comments during the peer review process and then the Associate Editors voted to select the winners. The objective of these awards is to recognize excellence and foster continuous improvement in our Transaction.

The winners were:

Transaction on Components and Packaging Technologies (TCPT):

Xuejun Fan, G. Q. Zhang, Willem D. van Driel, and Leo J. Ernst
"Interfacial Delamination Mechanisms during Reflow with Moisture Preconditioning"
T-CPT, Volume 31, Issue 2, June 2008

TCPT presentation: left to right: Wayne Johnson, Coauthors Leo Ernst and Xuejun Fan, William Chen

Abstract
This paper first examines the commonly-used thermal-moisture analogy approach in thermal-moisture analogy approach. We conclude that such an analogy using a normalized concentration approach does not exist in the case of soldering reflow, when the solubility of each diffusing material varies with temperature or the saturated moisture concentration is not a constant over an entire range of reflow temperatures. The whole field vapor pressure distribution of a flip chip BGA package at reflow is obtained based on a multiscale vapor pressure model. Results reveal that moisture diffusion and vapor pressure have different distributions and are not proportional. The vapor pressure in the package saturates much faster than the moisture diffusion during reflow. This implies that the vapor pressure reaches the saturated pressure level in an early stage of moisture absorption, even the package is far from moisture saturated. However, the interfacial adhesion degrades continuously with moisture absorption. Therefore, the package moisture sensitivity performance will largely reply on the adhesion strength at elevated temperature with moisture. A specially designed experiment with a selection of six different underfills for flip chip packages was conducted. Results confirm that there is no correlation between moisture absorption and the subsequent interface delamination at reflow. The adhesion at high temperature with moisture is the only key modulator that correlates well with test data. Such a parameter is a comprehensive indicator, which includes the effects of thermal mismatch, vapor pressure, temperature and moisture. In this paper, a micromechanics based mechanism analysis on interfacial delamination is also presented. With the implementation of interface properties into the model study, it shows that the critical stress, which results in the unstable void growth and delamination at interface, is significantly reduced when the effect of moisture on debonding is considered.

Transactions on Advanced Packaging (TADVP):

Kyung Suk (Dan) Oh, Frank Lambrecht, Sam Chang, Qi Lin, Jihong Ren, Chuck Yuan, Jared Zerbe, and Vladimir Stojanovic
"Accurate System Voltage and Timing Margin Simulation in High-Speed I/O System Designs"
T-AdvP, Volume 31, Issue 4, November 2008

TADVP presentation: left to right: Wayne Johnson, Coauthor Dan Oh, William Chen

Abstract
Accurate analysis of system timing and voltage margin including deterministic and random jitter is crucial in high-speed I/O system designs. Traditional SPICE-based simulation techniques can precisely simulate various deterministic jitter sources, such as intersymbol interference (ISI) and crosstalk from passive channels. The inclusion of random jitter in SPICE simulations, however, results in long simulation time. Innovative simulation techniques based on a statistical simulation framework have been recently introduced to cosimulate deterministic and random jitter effects efficiently. This paper presents new improvements on this statistical simulation framework. In particular, we introduce an accurate jitter modeling technique which accounts for bounded jitter with arbitrary spectrum in addition to Gaussian jitter. We also present a rigorous approach to model duty cycle distortion (DCD). A number of I/O systems are considered as examples to validate the proposed modeling methodology.

E-MAIL ALIAS AND IEEE WEB ACCOUNT NEEDED

2009 CPMT Society Board of Governors Election Goes Web-Based

Submitted by Marsha Tickman, Executive Director, IEEE CPMT Society

This year marks the implementation of a web-based balloting process for the CPMT Board of Governors election.

Eligible voting members will receive notification by e-mail in the Fall of this year with instructions for voting on-line. You will need an IEEE Web Account to access the ballot and cast your vote. This Web Account is the same one you may use for IEEE services such as renewing membership and accessing IEEE Xplore.

If you do not recall your Web Account username and password, or aren't sure whether you have established an account, please go to http://www.ieee.org/web/accounts to recover your password or establish a new account.

Please be sure to update your IEEE membership record with you current e-mail alias. If you DO NOT HAVE AN E-MAIL address or would prefer to receive a paper ballot by mail, please send your name, mailing address and IEEE Member Number by Tuesday 1 September to:

Marsha Tickman
IEEE CPMT Executive Office
445 Hoes Lane
Piscataway, NJ 08854 USA

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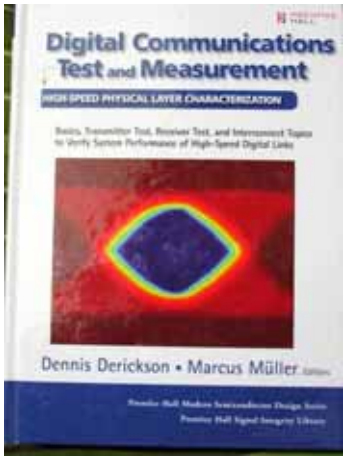
Book Reviews:

Submitted by Dr. David Palmer, IEEE Fellow

Digital Communications Test and Measurement High-Speed Physical Layer Characterization

Edited by Dennis Derickson and Marcus Muller

Price: $83.20 (Amazon)



This book is an excellent tutorial and guide for making high-speed measurements on communication hardware. The measurement set-ups are described in detail including cautions against common errors. Motivation for each measurement is given. This book is almost 1000 pages and could be used in a university laboratory class for in depth understanding if specific communication systems are provided to measure.

The first chapter reviews the digital communication system on a functional block level and Chapter three presents specific communication links so all measurements in the book have a focus.

For CPMT society members chapter 13 on physical interconnection measurements and modeling and appendix C detailing coaxial cables and connectors will be the most useful, but all the rest will be needed to allow efficient trade-offs on the system level. The book has five areas of concentration: bit error ratio measurements, high-speed digital waveform analysis, jitter in digital data stream, receiver testing, and characterization of the physical interconnection structures.

I was particularly impressed with the Time domain reflectometry discussion as applied to interconnections. Many issues confusing to the occasional lab user were clearly presented and made simple in execution.

The editors integrated the many author contributions in an efficient way so that each chapter can be used in isolation yet the user feels there is little duplication within the book.

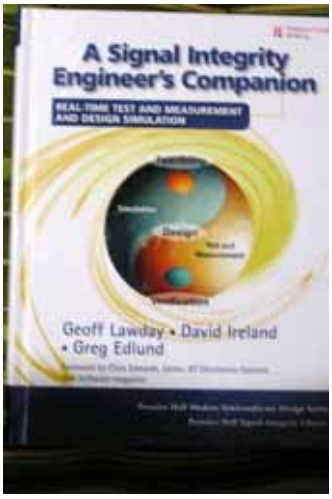
This book will find use in any cross-discipline design team. In particular, it will allow the package integration expert to understand the jargon and the trade-off pressures felt by others on the team.

A Signal Integrity Engineer's Companion Real-Time Test and Measurement and Design Simulation

By Geoff Lawday, David Ireland, and Greg Edlund

Prentice Hall Modern Semiconductor Design Series

Price: $80.00 (Amazon)



This book does a great job of teaching an approach to going from concept to product for high-speed digital systems. New design methods depending on complex signal integrity tests and measurements are presented. The presentation assumes a team is working on a complex design. However, considerable course or hardware experience is needed to gain the maximum from this text. This reader would have been helped by a glossary of all the initials used (apparently with the assumption that the reader already used them daily).

The writing is first class with catchy phrases like "probing has been the Cinderella of instrumentation" and "adequate instruments are only half the (troubleshooting) story, the partner in their work is the stimulation instrument – the signal source." Humor is used to keep the reader engaged while grappling with difficult concepts. The major concerns of reflections, attenuation, crosstalk, poor grounding, timing errors, and EM radiation are addressed from specifications to hardware testing.

Chapter five on the need, fundamentals, and subtleties of probes proved very important and is not included in many similar topic books. Each chapter has a motivational introduction and often a wise conclusion that underlines important lessons. The complete book integrates the analog perspective needed with the digital design process so robust at low frequencies. The book treats the importance of fixtures lightly despite a history of precision fixtures being used to test blocks/modules of the system when they are independently finished.

The last chapter brings in the perspective and tools (SPICE & ADS) needed for the many systems that now have wireless features in addition to the high-speed digital complexity. This chapter sets the