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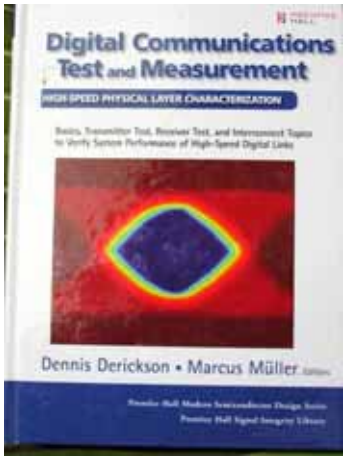
Book Reviews:

Submitted by Dr. David Palmer, IEEE Fellow

Digital Communications Test and Measurement High-Speed Physical Layer Characterization

Edited by Dennis Derickson and Marcus Muller

Price: $83.20 (Amazon)



This book is an excellent tutorial and guide for making high-speed measurements on communication hardware. The measurement set-ups are described in detail including cautions against common errors. Motivation for each measurement is given. This book is almost 1000 pages and could be used in a university laboratory class for in depth understanding if specific communication systems are provided to measure.

The first chapter reviews the digital communication system on a functional block level and Chapter three presents specific communication links so all measurements in the book have a focus.

For CPMT society members chapter 13 on physical interconnection measurements and modeling and appendix C detailing coaxial cables and connectors will be the most useful, but all the rest will be needed to allow efficient trade-offs on the system level. The book has five areas of concentration: bit error ratio measurements, high-speed digital waveform analysis, jitter in digital data stream, receiver testing, and characterization of the physical interconnection structures.

I was particularly impressed with the Time domain reflectometry discussion as applied to interconnections. Many issues confusing to the occasional lab user were clearly presented and made simple in execution.

The editors integrated the many author contributions in an efficient way so that each chapter can be used in isolation yet the user feels there is little duplication within the book.

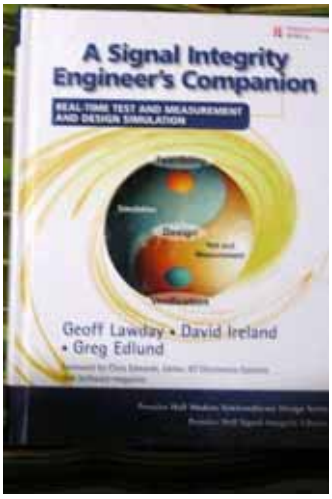
This book will find use in any cross-discipline design team. In particular, it will allow the package integration expert to understand the jargon and the trade-off pressures felt by others on the team.

A Signal Integrity Engineer's Companion Real-Time Test and Measurement and Design Simulation

By Geoff Lawday, David Ireland, and Greg Edlund

Prentice Hall Modern Semiconductor Design Series

Price: $80.00 (Amazon)



This book does a great job of teaching an approach to going from concept to product for high-speed digital systems. New design methods depending on complex signal integrity tests and measurements are presented. The presentation assumes a team is working on a complex design. However, considerable course or hardware experience is needed to gain the maximum from this text. This reader would have been helped by a glossary of all the initials used (apparently with the assumption that the reader already used them daily).

The writing is first class with catchy phrases like "probing has been the Cinderella of instrumentation" and "adequate instruments are only half the (troubleshooting) story, the partner in their work is the stimulation instrument – the signal source." Humor is used to keep the reader engaged while grappling with difficult concepts. The major concerns of reflections, attenuation, crosstalk, poor grounding, timing errors, and EM radiation are addressed from specifications to hardware testing.

Chapter five on the need, fundamentals, and subtleties of probes proved very important and is not included in many similar topic books. Each chapter has a motivational introduction and often a wise conclusion that underlines important lessons. The complete book integrates the analog perspective needed with the digital design process so robust at low frequencies. The book treats the importance of fixtures lightly despite a history of precision fixtures being used to test blocks/modules of the system when they are independently finished.

The last chapter brings in the perspective and tools (SPICE & ADS) needed for the many systems that now have wireless features in addition to the high-speed digital complexity. This chapter sets the

stage so the engineer knows what help they may need in this area should it require more depth.

This book will be of great value to many engineers but they will have to self-identify based on their experience and current projects.

Introduction to System-On-Packaging (SOP), Miniaturization of the Entire System,

By Rao R. Tummala and Madhavan Swaminathan

MacGraw-Hill, 2008, pp. 785

This is a complete introduction to the on-going research and development of SOP. The authors have co-authored several chapters and edited the rest written by leaders in the field. The basic theme is that there is plenty of room for further miniaturization even after the IC digital evolution call Moore's Law. There is no question that the many components and boards of a system are undergoing continual miniaturization using techniques other than those from the CMOS juggernaut. However, the transistor count has gone up 9 orders of magnitude and the transistor miniaturization improved by 6 orders, whereas the SOP miniaturization appears limited to 2 orders (may just be the reviewers conservative view). None the less, all this technology will be needed to win in the marketplace over the next decade.

This book describes where SOP technology is being expanded and directions technology may take, but does not really address any economic destiny. Remember CMOS is slowing for economic not technical reasons. The SOP is not an irresistible BORG spaceship assimilating all technology in its integration effort, but one future direction proved plausible by the many great developments discussed in this book. Many university and industrial advances are presented in detail within this book.

Before discussing the details, it is important to note that each section of this book presented new exciting facts and new technology interconnections to any reader except those with many years developing integrated packaging. The large number of "AHAs" is a mark of a great tech book.

The integration of unusual single MEMs or photonic element into a highly integrated system is quite a challenge. The MEMs and Optoelectonics chapters in this book give several options to accomplishing this level of integration in addition to discussing economic packaging of single MEMS and photonic devices. Other chapters address many integration aspects of Biosensor, electrical module testing, thermal management, wirering, RF, mixed signal, and stacked ICs.

The RF chapter uses LTCC and LCP integrated packaging as the basis for SOP creation. Particularly informative discussions occur on how to miniaturize and add gain to module antennas. Discussion of RF MEMs switches and their pros and cons as well as popular RFIDs are also well covered.

One practical aspect of system realization is not discussed in the book (it may be too soon). With the existing system of miniaturizing / integrating the digital and small signal analog signals in integrated circuits and interconnecting them with other components on boards there are well established methods to modify (tweak) the design on the board level when the simulations missed a little in timing or noise levels. The higher level of miniaturization of SOP does not appear to have these options so may require higher fidelity simulations.

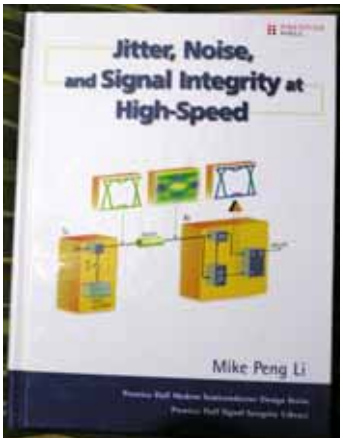
In addition to clear descriptions and explanations, each chapter has extensive references so that the working developing engineer can quickly study the foundation of any aspect of this field before they invest in further efforts. This book is a pleasant necessity for any engineer or manager involved in miniaturization of systems and modules.

Jitter, Noise, and Signal Integrity at High Speed

By Mike Peng Li

Prentice Hall Modern Semiconductor Design Series

Price: $80 (Amazon)



As clock speeds and analog signals frequencies are increasing, the system packaging design becomes the important component to maintaining Signal Integrity. The best system architectures can be sabotaged by not including package design from the very beginning. The author has clearly been involved in many difficult system designs that had noise challenges, some of which were unanticipated at the start.

This book fulfills the need in describing the fundamentals of Noise and Jitter so design tradeoffs can be made with reasonable certainty of eventual performance. Although not directly addressing modern micropackaging, the sources of noise are detailed so the experienced packaging engineer can quantify the contribution of each design choice.

Although this is the best book around for a university course on this material, I suspect that this subject matter can not really be learned

until one is well within a complex industrial design and the slow realization that the margin of signal integrity is shrinking dawns on the team. By analogy, this subject is like a thermodynamics course for an undergraduate; the students will survive and maybe get a good grade but they will never understand until they have faced a few real life designs that depend on true understanding.

Thus I recommend that every design team (including package experts) have this book in their meeting room where they can take turns studying it and trying to tutor each other as the inevitable need arises. For example, the only books on this topic my firm has today were written about 15 years ago when frequencies were gentle and packaging had more margin based just on rules of thumb. Since then I/O frequencies have increased from 1 to 40 Gbs, and at least one designer must really understand the features that increase noise / crosstalk and degrade the Bit Error Rate.

Do not feel neglected if you do not need this book; your designs are probably very challenging on some other basis such as cost or miniaturization. We can't all struggle up the frequency spectrum.

Conference News:

59th ECTC Overview:

Submitted by Eric Perfecto, Senol Pekin, Rao Bonda, Pat Thompson, and Bill Chen – ECTC 2009 Committee

The 59th Electronic Components and Technology Conference was Alive and Well in San Diego, CA

Sheraton San Diego Hotel & Marina was the venue for the 59th ECTC in May 26-29th, 2009.

Although the attendance was not the highest ever due to worldwide recession and the H1N1 flu worries, the 59th ECTC in San Diego was a great success. Thanks to the authors and the ECTC program committee, they presented 336 high quality papers in 38 oral sessions and three poster sessions. About 46% of the papers presented were from North America, 37% from Asia and 17% from Europe. With 551 conference attendees and 185 professional development course (PDC) attendees, the 59th ECTC pulled it through successfully in an industry that is working on rebounding from a worldwide recession. In addition to technical sessions, the conference was enhanced by 16 Professional Development Courses, 14 new exhibitors totaling to 52, luncheons, raffle drawings, evening receptions, best paper awards, ECTC Panel Discussion chaired by William Chain of ASE, and Plenary Session co-chaired by Jie Xue of Cisco and Senol Pekin of Intel. Technical sessions started on Tuesday and continued through Friday.

A Big Thanks to the Executive Committee of the 59th ECTC!

From left to right: David McCann, Rao Bonda, Steve Bezuk, C. P. Wong, Wolfgang Sauter, Lisa Renzi, Glyndwr Smith, Kitty Pearsall, Eric Perfecto, Patrick Thompson, Jean Trewhella, Rajen Dias, and Torsten Wipiejewski (not shown)

Tuesday:

185 attendees attended 16 professional development courses. Eight of these courses were new for this year. The courses were organized by the PDC Committee chaired by Kitty Pearsall of IBM.

ITRS Assemblies and Packaging Technology Committee held its meeting on Tuesday from 8:00 am until 5:00 pm. In parallel, and with increased focus in optical packaging, two special sessions were organized by the Optoelectronics committee.

In the evening, students attended the ECTC Student Reception where they had an opportunity to learn about how the technical subcommittees work to select the abstracts.

The ECTC Student Reception was hosted by Lei Shan of IBM TJ Watson Research Center.

Following the students reception, the 59th ECTC General Chair hosted a reception for the speakers and session chairs.

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IEEE will be essential to the global technical community and to technical professionals everywhere, and be universally recognized for the contributions of technology and of technical professionals in improving global conditions.