until one is well within a complex industrial design and the slow realization that the margin of signal integrity is shrinking dawns on the team. By analogy, this subject is like a thermodynamics course for an undergraduate; the students will survive and maybe get a good grade but they will never understand until they have faced a few real life designs that depend on true understanding.

Thus I recommend that every design team (including package experts) have this book in their meeting room where they can take turns studying it and trying to tutor each other as the inevitable need arises. For example, the only books on this topic my firm has today were written about 15 years ago when frequencies were gentle and packaging had more margin based just on rules of thumb. Since then I/O frequencies have increased from 1 to 40 Gbs, and at least one designer must really understand the features that increase noise / crosstalk and degrade the Bit Error Rate.

Do not feel neglected if you do not need this book; your designs are probably very challenging on some other basis such as cost or miniaturization. We can't all struggle up the frequency spectrum.

Conference News:

59th ECTC Overview:

Submitted by Eric Perfecto, Senol Pekin, Rao Bonda, Pat Thompson, and Bill Chen – ECTC 2009 Committee

The 59th Electronic Components and Technology Conference was Alive and Well in San Diego, CA

Sheraton San Diego Hotel & Marina was the venue for the 59th ECTC in May 26-29th, 2009.

Although the attendance was not the highest ever due to worldwide recession and the H1N1 flu worries, the 59th ECTC in San Diego was a great success. Thanks to the authors and the ECTC program committee, they presented 336 high quality papers in 38 oral sessions and three poster sessions. About 46% of the papers presented were from North America, 37% from Asia and 17% from Europe. With 551 conference attendees and 185 professional development course (PDC) attendees, the 59th ECTC pulled it through successfully in an industry that is working on rebounding from a worldwide recession. In addition to technical sessions, the conference was enhanced by 16 Professional Development Courses, 14 new exhibitors totaling to 52, luncheons, raffle drawings, evening receptions, best paper awards, ECTC Panel Discussion chaired by William Chain of ASE, and Plenary Session co-chaired by Jie Xue of Cisco and Senol Pekin of Intel. Technical sessions started on Tuesday and continued through Friday.

A Big Thanks to the Executive Committee of the 59th ECTC!

From left to right: David McCann, Rao Bonda, Steve Bezuk, C. P. Wong, Wolfgang Sauter, Lisa Renzi, Glyndwr Smith, Kitty Pearsall, Eric Perfecto, Patrick Thompson, Jean Trewhella, Rajen Dias, and Torsten Wipiejewski (not shown)

Tuesday:

185 attendees attended 16 professional development courses. Eight of these courses were new for this year. The courses were organized by the PDC Committee chaired by Kitty Pearsall of IBM.

ITRS Assemblies and Packaging Technology Committee held its meeting on Tuesday from 8:00 am until 5:00 pm. In parallel, and with increased focus in optical packaging, two special sessions were organized by the Optoelectronics committee.

In the evening, students attended the ECTC Student Reception where they had an opportunity to learn about how the technical subcommittees work to select the abstracts.

The ECTC Student Reception was hosted by Lei Shan of IBM TJ Watson Research Center.

Following the students reception, the 59th ECTC General Chair hosted a reception for the speakers and session chairs.

IEEE Vision

IEEE will be essential to the global technical community and to technical professionals everywhere, and be universally recognized for the contributions of technology and of technical professionals in improving global conditions.

Wednesday:
Technical sessions started on Wednesday at 8:00 AM and prior to that in the morning, the speakers and session chairs met at breakfast to prepare for the sessions. Three coffee breaks everyday created the opportunity for networking and exchanging information among the conference attendees.

The 2008 Best and Outstanding papers for the oral presentations and posters were also presented at the ECTC luncheon.

On Tuesday night, ECTC Panel Discussion on "Consumer Electronics and Packaging Technologies in Times of Recession and Recovery" chaired by William Chen of ASE attracted the attention. Conference attendees had an opportunity to listen to Jim Walker, VP of Research at Gartner-Dataquest; Ron Stager, Partner In-charge at KPMG; Mark Brillhart, VP of technology and Quality at Cisco Systems; Joyce Koo, Materials Lab Manager at Research in Motion; Raj Master, General Manager of IC Packaging, Quality and Reliability at Microsoft; and Michael Nealon, Director of Hardware and Design at IBM Server Group.

Jim Clifford, Senior Vice President and General Manager of Operations, Qualcomm CDMA Technologies gave a talk at the ECTC Luncheon. His presentation is posted at the ECTC web site due to popular demand.

Mr. Jim Clifford is the Senior Vice President and General Manager of Operations at QUALCOMM CDMA Technologies (QCT). In this role, Mr. Clifford is responsible for IC and Packaging Technologies, Procurement, Integrated Supply and Demand Planning, and Quality in addition to managing the overall operations functions for the QCT division.

Mr. Clifford has been at QUALCOMM since 1994, when he joined the company as a director of business development and oversaw product development in its OmniTRACS division. In 1996 he moved to QCT as director ASICs, and has focused on sourcing IC chips during the explosive growth for CDMA technology. He was promoted to vice president of operations in 1997, senior vice president in 2000, and GM of Operations in 2003. Prior to his career at QUALCOMM, Mr. Clifford had more than 20 years of experience at Unisys in positions ranging from IC design to vice president and general manager of mainframe computer manufacturing. Mr. Clifford holds a Bachelor's of Science in Physics from San Diego State University, and is a graduate of the Executive Program for Scientists and Engineers offered by the University of California, San Diego.

Mr. Clifford's luncheon presentation at ECTC on "Less and Moore: Wireless, Fabless, Factory-less" covered an overview of the expanding mobile applications that are driving the semiconductor landscape. He talked about the importance of the evolving collaborative models across the value chain to meet product requirements such as low cost, low power, small form factors and high performance. Innovative technology solutions and co-design of architecture, design, silicon and packaging are requirements to meet consumer demand for increased features and capabilities. Mr. Clifford's presentation is posted on the ECTC website www.ectc.net.

In the evening, exhibitor reception provided another opportunity for networking and exchanging information among the conference attendees.

General Chair Rao Bonda hosted the program subcommittee chairs and assistant chairs in his suit and thanked them for their leadership in selecting the 336 technical papers out of 564 abstracts which was the second highest number of abstracts received in the ECTC history.

On Wednesday night, Jie Xue of Cisco and Senol Pekin of Intel Corporation co-chaired the ECTC Plenary Session titled "Product Qualification Strategies in the Semiconductor Industry". Panelists Tin-Lup Wong, DE and Executive Director of Product Q&E at Lenovo; Bruce Euzent, VP of Q&R at Altera; Tom Gregorich, CP of IC Packaging at Qualcomm; Jean Trewhella, Director of packaging R&D at IBM Corporation; and Jim Walker, VP of Research at Gartner-Dataquest concentrated on time-to market, improving innovation, and enhancing customer satisfaction. This panel was held as a continuation in a series that concentrates on critical issues related to the semiconductor industry by bringing the experts and leaders together in the framework of text-book theory, and real life challenges and applications.

Thursday:
The 2009 CPMT Awards were presented at the Luncheon. Madhusudan Iyenger, Ho-Ming Tong, Sheng Liu, Moises Cases, C. P. Wong and George Harman were honored with various awards.

Industry veteran and wire bonding expert, George Harman, was among the ones that were honored due to their contributions. He received 2009 IEEE CPMT Field Award.

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General Chair Rao Bonda of Freescale Semiconductor received an award from CPMT Representative C. P. Wong for contributions to the ECTC conference.

Fifty two exhibitors took part in the Technology Corner Exhibit which continued on Thursday.

On Thursday, ECTC Program Committee met in preparation for the ECTC 2010 in Las Vegas. CPMT Representative C. P. Wong announced that Wolfgang Sauter of IBM Corporation will serve as the Assistant Program Chair for 2010. Senol Pekin of Intel Corporation joined the Executive Committee as the new Web Administrator.

Thursday evening was always fun at the ECTC as the conference attendees and their spouses got plenty of time to talk at the well-catered ECTC Gala Reception.

In the far back of the photo above, Debb Kaller of Parallel Semiconductor and Lee Smith of Amkor can be seen exchanging information.

Shown in the picture above is the "A-Team" for 2010: (from left to right) Assistant General Chair Rajen Dias of Intel Corporation, Program Chair David McCann of Amkor, Assistant Program Chair Wolfgang Sauter of IBM, and 60th ECTC General Chair Jean Trewhella of IBM.

Friday:

Technical sessions continued till 5 PM. Conference attendees enjoyed the Program Chair luncheon at the last day of the conference, thanks to the raffle drawings announced by Thomas Reynolds.

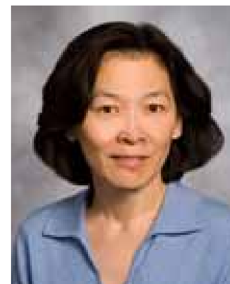
Tin-Lup Wong, DE and Executive Director of Product Q&E at Lenovo, who joined the conference for the first time this year to speak at the ECTC Plenary Session is likely to attend next year also, since he won a free registration for next year's conference.

The First Call for Papers for 60th ECTC is already out and can be found at www.ectc.net. You are invited to submit a 750-word abstract by October 15, 2009. In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses.

See you at the 60th ECTC in Las Vegas, Nevada next year!

59th ECTC 2009 Plenary Session:

Product Qualification Strategies in the Semiconductor Industry was under the Spotlight at the 59th ECTC in San Diego, CA



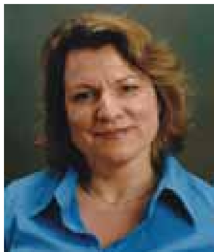
Jie Xue of Cisco and Senol Pekin of Intel Corporation moderated the discussion to highlight the strategies in integrating qualification into product development with emphasis on cost-cutting, time-to-market and improved innovation.

59th ECTC 2009 Plenary Session Participnats

Session Chairs are Jie Xue of Cisco and Senol Pekin of Intel Corporation. Panelists included Tin-Lup Wong, DE and Executive Director of Product Q&E at Lenovo; Bruce Euzent, VP of Q&R at Altera; Tom Gregorich, CP of IC Packaging at Qualcomm; Jean Trewhella, Director of packaging R&D at IBM Corporation; and Jim Walker, VP of Research at Gartner-Dataquest.

Reliability qualification is often the bottleneck in semiconductor product development and can significantly delay deployment. In an industry that is working on rebounding from a world wide recession, high level experts took the stage and discussed product qualification strategies towards enhancing customer satisfaction, at the Plenary Session organized and co-chaired by Jie Xue of Cisco and Senol Pekin of Intel Corporation. The session attracted hundreds of engineers and managers. This panel was held as a continuation in a series that concentrates on critical issues related to the semiconductor industry by bringing the experts and leaders together in the framework of text-book theory, and real life challenges and applications.

Jim Walker, VP of Research at Gartner-Dataquest took the stage first by predicting that Semiconductor Industry will rebound faster from recession than most other industries. The World financial crisis has resulted in chaos and continued downside momentum for most industries. In contrast, the recession of 2001 prepared the semiconductor industry to be more astute in managing capital, inventories and resources in this current economic downturn that began in 2008. As a result, second half of this year should be improved, as seasonal increases in cell phone, PC and even consumer electronic products orders for IC's begin to increase due to inventory replenishment. Mr. Walker further stated that semiconductor packaging will play an important role in this upturn, since increased demand for the next generation of electronic products will result in the adoption of new packaging technologies and qualification schemes. He emphasized the importance of time-to market in revenue generation and margin improvement.



Jean Trewhella, Director of IBM Packaging Research and Development Center, challenged the status-quo by explaining that technology focused development done early can reduce the technical risks and enable truly streamlined qualification testing. However this is becoming increasingly difficult as the demands on packaging to overcome the thermal, bandwidth and chip packaging interaction challenges of semiconductors grow. In order to drive reliable solutions with high value the silicon technology and the packaging technology must be co-developed with target application architecture space in mind. Ms. Trewhella emphasized that collaboration through an eco-system across the value chain can enable non-vertically integrated companies to reap the benefits of end-to-end development.

Tom Gregorich , VP of IC Package Engineering at Qualcomm, stated that new technologies introduce new failure mechanisms. Over the past 20 years the mobile telephone has grown-up from being a trunk-mounted voice-only device to a handheld data portal to the World Wide Web and beyond. During this same time period, the semiconductor technologies used in these devices have evolved at ever-increasing rates. Extrapolating J.M. Juran's definition of quality ("fitness for use") over time, Mr. Gregorich explained that the key to maintaining reliability is by understanding and management of component stresses. He then introduced the time-to-market product development constraint and the challenges of parallel and simultaneous technology deployment. Mr. Gregorich referred to a series of technology changes which have had significant impact on the semiconductor industry. These technology changes include the following transitions: from leaded to SMT components; from trunk to handheld; from SnPb to Pb-free and from wire bond to flip chip. Finally he presented a list of "10 Easy Steps" to better reliability qualification.

Bruce Euzent, VP of Quality and Reliability at Altera, reminded that "one size does not fit all" in reliability qualification. He explained that there are many strategies for qualification of new components other than the traditional 3 lots for 1000 hours qualification exercise. Different applications and market segments introduce time to market and specific failure mechanisms that must be dealt with. Knowledge based qualification and application specific qualification strategies are used to address these concerns. No one methodology is applicable for every product, market, and application. He concluded that a successful qualification methodology requires the intelligent melding of multiple concepts.

Tin-Lup Wong, Distinguished Engineer and Executive Director, Product Engineering & Quality at Lenovo said "what is enough is not enough!" As notebook computer design becomes thinner and lighter, the design consideration and robustness of the second level packaging on Ball Grid Arrays (BGA) become a significant part of the reliability equation. The problem is compounded by highly mobile users, wireless computing and challenging user environment. Dr. Wong explained how the general assumptions and practices in the packaging world were affecting the reliability of ThinkPad notebook design, and how the design team collaborated with industry leaders, drove design innovations and improved on end-to-end process control to deliver reliable products to the market.

59th ECTC 2009 Panel Discussion:

The theme of the Tuesday night ECTC Panel Session was "Consumer Electronics and Packaging Technologies in Times of Recession and Recovery". It was chaired by William Chen, CPMT Society President, and Senior Technical Advisor at ASE. There panel session scheduled from 7:30 pm to 9:00 pm had attendance of about 200 participants.

The eclectic panel was composed of industry leaders, technologists, business consultants, and analysts.Panelists presented different perspectives in the consumer electronics recovery landscape and new opportunities in the new economy.

The panel addressed a number of questions at the crossroads of consumer market, global business and technology innovation including 3D packaging with particular focus of the impact of the deep recession and eventual recovery. Some of the questions addressed by the panelists were: How will the consumer electronics product landscapes look, as the economic recession moves into recovery? What

are the dynamics between market imperatives and technology innovations? How do these trends drive the direction of packaging technologies?

Picture of 59th ECTC 2009 Panel Session Participants - Joyce Koo, Manager, Materials Lab, Research In Motion; Michael Nealon, Director, Hardware and Design, IBM Server Group; Raj Master, General Manager, IC Packaging, Quality & Reliability, Microsoft; Mark Brillhart, Vice President, Technology and Quality, Cisco; William Chen, Senior Technical Advisor (Panel Chair, standing); Ron Steger, Partner in Charge, KPMG; Jim Walker, V.P. of Research, Semiconductor Manufacturing, Gartner/Dataquest.

The following paragraphs provide brief biography of the 59th ECTC 2009 Panel Session participants:

Dr. Y.C. Joyce Koo is currently serving as Material Interconnect Lab Manager at Research in Motion Ltd. He has extensive experience in the field of Microelectronic and Photonics packaging, related to commercial, military and telecommunications. She has held many senior positions at various companies, including Specialty Engineer at Litton System and Staff Engineer position at IBM Canada. Joyce obtained her PhD degree in the field of microcrystalline (nano-crystalline) silicon fabrication and characterization from the University of Toronto, Canada in 1992. Joyce currently is a lab manager at Research In Motion, Material Interconnect Lab.

Mr. Mike Nealon is the Director of System Hardware Design for IBM's Enterprise Systems Development Organization. His present responsibilities include the system design and hardware development of IBM's Enterprise Systems, including the High End zClass Servers, POWER Servers and High End Storage. Mike has been with IBM for 26+ years with assignments in processor and system packaging technology development, microprocessor design and system development serving in a variety of managerial and technical leadership positions.

Mr. Raj Master is currently General Manager of Hardware IC Packaging,Quality and Reliability Engineering for Microsoft. He is responsible for Game console, Keyboard, mouse, webcam, Zune and Surface computing. Raj was at AMD from 1996 to October 2008. At AMD, Raj was a Corporate Fellow and Chief Technologist. Raj is responsible to develop AMD strategy for C4, packaging, assembly and Thermal solutions. He led the Organic packaging development and manufacturing which is now in high volume production. Raj joined AMD after spending 21 years at IBM. He was Senior Technical Staff member at IBM prior to joining AMD. He was responsible for packaging development and manufacturing as related to C4, Ball Grid Array, Column Grid Array, Board Level Reliability and Multi Layer Ceramic Substrate.

Mr. Mark Brillhart leads Cisco's Technology and Quality organization, a global team responsible for delivering customer-driven quality and reliability solutions and infrastructure for Cisco products. With 300+ employees in locations around the world, Brillhart oversees a team responsible for developing industry-leading testing tools and technologies for leading-edge ASICs, PCBs, optical devices, custom memory modules, and complex interconnect technologies. Brillhart joined Cisco in 1999, first as a technical lead and then as manager of the Interconnect Reliability and Electronic Packaging teams. He has also served as Director of Hardware Reliability, Sr. Director of Component Quality and Technology, and Vice President of Manufacturing Operations Engineering. Prior to Cisco, he held a variety of engineering and technical lead positions at HP, as well as research and development positions in the medical products industry.

Mr. Ron Steger began his career with KPMG in 1976, and was admitted into the partnership in 1986. Mr. Steger is one of a select number of partners who has been appointed both an IFRS and U.S. SEC Reviewing Partner, the firm's senior-most technical positions. Mr. Steger has extensive experience serving clients in the technology, food service and consumer products industries. He is the former National Industry Director for Electronics, and currently serves as the leader of KPMG's Global Semiconductor Practice.

Mr. Jim Walker is a vice president of research with the semiconductor manufacturing team at Gartner-Dataquest. His research covers semiconductor packaging and assembly, manufacturing outsourcing services, MEMS and nanotechnology. Before joining Gartner Dataquest, Mr. Walker was the co-founder and vice president of marketing for Hana-USA, a subcontract IC package assembly company. At Dexter Electronic Materials and E.I. DuPont, he performed research, development, quality assurance and technical service utilizing polymeric materials for adhesive, composite, aerospace, electronic and semiconductor applications. At National Semiconductor, Mr. Walker held various roles, including surface mount packaging marketing manager. He is a founding member of the Surface Mount Technology Association (SMTA) and served as the national president.

CPMT ECTC Volunteer Recognition:

More than 200 volunteers that contributed to each ECTC are the key for making the ECTC a premier packaging conference. Many of these volunteers have served ten, twenty or even more years, representing an impressive time and energy contribution. In 2008, the CPMT BOG decided to recognize long-term volunteers, and created the CPMT ECTC Volunteer Recognition Award. The award recognizes two service milestones, 10 and 25 years. The first presentation of awards was made at the 2009 ECTC by Bill Chen, President of the CPMT. Since 2009 was the inaugural year, plaques were presented to "catch up" with volunteers' service. The 10-year plaques were presented to volunteers with 10 to 24 years of service, and the 25-year plaques were presented to volunteers with 25 or more years of service. In all, 56 volunteers received 10-year plaques, and four volunteers received 25-year plaques. The accompanying list contains the names of all recipients. Bill Chen and the entire CPMT BOG thank all ECTC volunteers for their contribution to the ECTC.

10-year recipients were Amit Agrawal, Yasuhiro Ando, Rao Bonda, Jo Caers, Michael Caggiano, Andreas Cangellaris, Moises Cases, Rajen Chanchani, Harry K. Charles, Mario Dagenais, Rajen Dias, Craig Gaw, Lih Tyng Hwang, Masataka Ito, Christine Kallmayer, Sung K Kang, George Katopis, Harry Kellzi, Bruce Kim, Claude

Ladouceur, Pradeep Lall, Michael Lamson, John Lau, Michael Lebby, Chin C. Lee, Timothy Lenihan, Jong-Kai Lin, Johan Liu, Erdogan Madenci, Tony Mak, Raj Master, Goran Matijasevic, David McCann, James E. Morris, Luu Nguyen, Donna M. Noctor, Dennis Olsen, Kyung-Wook Paik, Kitty Pearsall, Raj Pendse, Eric Perfecto, Tom Poulin, Albert Puttlitz, Sudipta Ray, Thomas Reynolds, Bill Ring, Leonard Schaper, Suresh K Sitaraman, Joseph Soucy, Ephraim Suhir, Madhavan Swaminathan, Tom Swirbel, Andrew A.O. Tay, Jan Vardaman, Torsten Wipiejewski, and Ping Zhou.

25-year recipients were DarvinEdwards, George G.Harman, PatrickThompson, and C. P.Wong.

Patrick Thompson receiving 25-year ECTC Volunteer Service award from Bill Chen

C.P. Wong receiving 25-year ECTC Volunteer Service award from Bill Chen

Best of ECTC 2008 Conference Papers:

The best paper awards for ECTC 2008 were presented at ECTC 2009 luncheon on May 27, 2009 in San Diego. Jean Trewhella, the Program Chair for ECTC 2008 coordinated the selection process and the awards were presented by Rao Bonda, the General Chair for the ECTC 2009.

Best Papers - 2008:
The authors of the Best Session Paper shared a check for US$2500 and the authors of the Best Poster Paper shared a check for US$1500.The winning authors also received a personalized plaque commemorating their achievement.

Best Session Paper
"Material Design and Package-Level Reliability of a Novel Low-Temperature Solder Based on Intermetallic-Compound Phases with Superior High-Homologous Temperature Properties" by Daewoong Suh and Chi-Won Hwang – Intel Corporation; Minoru Ueshima and Jun Sugimoto – Senju Metal Industry Company, Limited

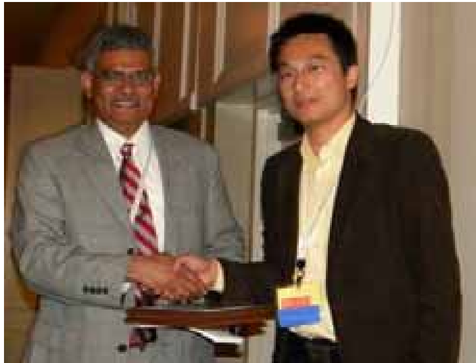
Best Poster Paper
"Development of a 50mm Dual Flip Chip Plastic Land Grid Array Package for Server Applications" by Sylvain Ouimet and Isabelle Dépatie – IBM Canada Limited; Jon Casey, Kenneth Marston, Jennifer Muncy,Virendra Jadhav, and Thomas Wassick – IBM Semiconductor Research and Development Center; John Corbin – IBM Systems and Technology Group

Outstanding Papers – 2008:
The winning authors for Conference Outstanding Session and Poster Papers received a personalized plaque commemorating their achievement and shared a check for US$1000.

Outstanding Session Paper
"Replacement of the Drop Test with The Vibration Test-The Effect of Test Temperature on Reliability" by T.T. Mattila, L. Suotula, and J.K. Kivilahti – Helsinki University of Technology

Outstanding Session Paper
"Replacement of the Drop Test with The Vibration Test-The Effect of Test Temperature on Reliability" by T.T. Mattila, L. Suotula, and J.K. Kivilahti – Helsinki University of Technology

Outstanding Poster Paper
"Interfacial Fracture Properties and Failure Modeling for Microelectronics" by A. Xiao, K.M.B. Jansen, J. de Vreugd, and L.J. Ernst – Delft University of Technology; H. Pape – Infineon Technologies AG; B.Wunderle – Fraunhofer IZM



Motorola Electronic Packaging Fellowship – 2008:
The winning student paper author received a three year fellowship grant of US$21,000 at his/her university. The following paper was selected based on the Motorola Electronic Packaging Fellowship paper competition conducted at 58th ECTC in Lake Buena Vista, Florida:

"3-D Stacking of Chips with Electrical and Microfluidic I/O Channels" by Calvin R. King Jr. (Student Author), Deepak Sekar, Muhannad S. Bakir, Joel Pikarsky, and James D. Meindl – Georgia Institute of Technology; Bing Dang – IBM T. J.Watson Research Center

CPMT Ph.D. Student Fellowship – 2008:
The winning student paper author received a one year Fellowship of $10,000 towards his/her Ph.D. studies in 2008 and 2009.The following paper was selected based on the CPMT Ph.D. student fellowship paper competition conducted at 58th ECTC in Lake Buena Vista, Florida:

"Microwave Design & Characterization of a Novel Nano-Cu based Ultra-fine Pitch Chip to Package Interconnect" by Tapobrata Bandyopadhyay (Student Author), Gaurav Mehrotra, P.M. Raj, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology; Mahadevan K. Iyer – Infineon Technologies

Intel Best Student Paper – 2008:
The winning student received a certificate and a check for $2500.The following paper was selected based on the Intel Best Student Paper competition conducted at 58th ECTC in Lake Buena Vista, Florida:

"Peridynamic Theory for Impact Damage Prediction and Propagation in Electronic Packages Due to Drop" by Abigail Agwai (Student Author), Ibrahim Guven, and Erdogan Madenci – University of Arizona

The awards for ECTC 2009 Best Papers will be presented at ECTC 2010 in Las Vegas, Nevada on June 2, 2010.

Kudos to 59th ECTC General Chair Dr. Rao Bonda:

Dr. Rao Bonda is currently a technology program manager in Freescale Semiconductor, Inc. (formerly known as Motorola's Semiconductor Products Sector) in Tempe, AZ. He received a Ph.D. in Materials Science and Engineering from the University of Pennsylvania, Philadelphia, PA, in 1985. After receiving Ph.D., Rao continued research in materials science at the Ohio State University, Columbus, OH and the University of Wisconsin, Madison, WI until 1989. Prior to joining Motorola in 1994, he was a research member at IBM T.J. Watson Research Center, Yorktown Heights, NY, and IBM Microelectronics Division, Endicott, NY.

Rao has been a member of the Board of Governors for the IEEE CPMT Society for over twelve years. He was the Chair of its Awards Committee from 1997-2005. At present, he is the Vice President-Technical for the Society. He is also an Associate Editor for IEEE Transactions on Advanced Packaging journal. He is very active in CPMT Phoenix Chapter and IEEE Phoenix Section. He has served as the chair and program chair for the Chapter and as the chair for the IEEE Phoenix Section.

Rao has been actively participating in the Electronic Components and Technology Conference (ECTC) for over twelve years. He has served as the chairman of the Components and RF sub-committee and has chaired the sessions at the ECTC. He has chaired the Professional Development Courses committee and served on the committee for three years. He was the Assistant Program Chair for the 2006 ECTC, the Program Chair for 2007 ECTC, Vice General Chair for 2008 and General Chair for 2009. He is currently the Jr. Past General Chair for 2010 ECTC.

Rao is a senior member of the IEEE. In addition to a Ph.D., he holds an MS and a BS in Metallurgical Engineering from Indian Institute of Technology, Kanpur, and Regional Engineering College, Warangal (India), respectively. He also received an MBA from the Arizona State University, Tempe, AZ, in 1998.

SWTW 2009 Update:

Submitted by Jerry Broz, Ph.D., General Chair of SW Test Workshop

The 19th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) was successfully held at the Paradise Point Resort in San Diego, CA, from June 7 to 10, 2009. This yearly workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. The SW Test 2009 agenda consisted of a technical program, supplier exhibits (which ARE NOT open during the technical sessions), and a Casino Royale Social Event as well as plenty of time for informal interaction and networking with colleagues. The total conference and EXPO attendance was 175 with approximately 15% international attendees representing a total of 12 countries. Unfortunately, due to the H1N1 pandemic alert level, many of the usual international attendees were restricted from travelling to the United States.

The workshop began with a Sunday afternoon tutorial session organized by Technical Program Chair Brett Crump in conjunction with Darren James and Jeff Greenberg of Rudolph Technologies. This excellent three part tutorial provided new and experienced technologists key insights into many of the metrology problems facing the wafer test industry. Topics included an introduction into applied metrology concepts; a series of case studies focused on metrology tool capability assessments; and wrapped up with a practical discussion on the metrology approaches used to fix wafer sort floor problems.

After the welcome reception, Jerry Broz, Ph.D., SW Test General Chair, gave a short, "Probe Year In Review" presentation which set the stage for the Keynote Presentation, entitled, "Test Economics Driving Test Technology", made by Risto Puhakka, President of VLSI Research, Inc.

Mr. Puhakka discussed the key metrics tracked by VLSI which showed that the overall semiconductor industry was relatively healthy as the global recession began. Interestingly, these metrics demonstrated that half of the global chip recession was caused by overspending within the Taiwan memory sector. VLSI's global chip making climate trend index showed that the semiconductor industry has started slowly moving out of the "deep freeze". The data provided also showed that the general semiconductor business and capacity utilization rates are basically returning to normal but at an overall lower operating level.

The probe card market experienced a reduction in revenue of approximately 30% from 2008; with the most dramatic changes occurring in the advanced probe card technologies primarily used for memory test. FormFactor, Micronics Japan (MJC), and Japan Electronic Materials (JEM), respectively, remained as the top three probe card suppliers world-wide; however, the rest of the top ten saw a major reshuffle. Mr. Puhakka stated that VLSI has already seen that the back-end consumables and materials are bouncing back and expects the probe card and socket businesses to recover sooner than ATE. ATE is forecasted to remain less than half of total test hardware spending. Overall, VLSI's outlook for the semiconductor industry was very positive for the rest of 2009 and into 2010. Risto's keynote presentation will be available on the SW Test website (http://www.swtest.org) in July; in the meantime, it can be downloaded from the weSRCH.com website at http://electronics.wesrch.com/pdfEL1SE1ZTZAAXK.

The 2009 SW Test technical program began on Monday morning with the Welcome session by Dr. Jerry Broz. Dr. Broz gave a positive update on Bill Mann, Chair Emeritus, who is battling cancer and recognized the passing of long time SW Test contributor and Steering Committee member, Frank Pietzschmann (Qimonda-Dresden). Dr. Jerry Broz, Ph.D., was selected as a recipient for the IEEE Computer Society's Golden Core award, given for long-standing service to the society. Each year the IEEE Awards Committee selects up to a maximum of 50 recipients out of the more than 100,000 current IEEE Computer Society members and permanently includes the names in the Golden Core Member master list. The Golden Core is the highest level of membership designation in the IEEE Computer Society.

The next two and a half days were filled with a wide variety of technical presentations covering every facet of the wafer test process from *Large Area Array Probing Challenges* to *Damage Control and Low Force Probing*. Some individual highlights from the technical program included Michael Huebner, Ph.D., (FormFactor) and Scott Lindsey, Ph.D. (Aehr Test), discussing the future of increased pin counts and two different full wafer probing methods. The importance of consistent and accurate data tracking methods in the sort environment was detailed by Mark Winn (Intel) and Rob Marcelis (Salland Engineering). Jan Martens (NXP-Hamburg) discussed contact mechanisms behind copper metallurgy effects for sort process and cleaning performance. The technical hurdles experienced during an RF-probe card and ATE hardware qualification were discussed by Mike Slessor, Ph.D., (MicroProbe); Mark Roos (Roos Instruments) with Roger Hayward (Cascade Microtech); and Daniel Watson (Teradyne). Several other presentations, such as those by James Tong (Texas Instruments) and Gordon Vinther (Ardent Concepts) reviewed the use of standardized methodologies within the development environment and transitioning to a production test floor. Overall, the technical program had 29 podium presentations with 65% from suppliers, 15% from semiconductor manufacturers, and 20% collaborative presentations from both manufacturers and suppliers.

Best Presentation was awarded to the collaborative team of Yuan Huang, Gary Liu, Thompson Hsu (United Microelectronics Corp.) and Wensen Hung, Cahris Lin, Dean Yang (MPI–Taiwan) for their comprehensive work on vertical cobra probing on low-k wafers; *Best Data Presented* went to the technical team of Wolfgang Schaefer, Ph.D. and Gunther Boehm (Feinmetall GmbH) that discussed various aspects of high temperature probing; *Best Presentation, Tutorial in Nature*, went to Gert Hohenwarter (GateWave Northern) for his overview on key issues for power delivery verification; the *Most Inspirational Presentation* was awarded to Jason Mroczkowski and Ryan Satrom (Everett Charles Technologies) for their detailed work on wafer level test hardware using a signal integrity simulation; and although there were many eligible candidates for the infamous "*Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch*" this award was not inflicted. All the presentations (including the tutorials, keynote, technical program, and posters) from 2009 as well as previous workshops (1993 to 2009), are available on the newly redesigned SW Test website (http://www.swtest.org).

Technology EXPO 2009 had a total of 31 industry exhibitors and five Corporate Supporters (Advanced Probing Systems, Buckling-

Beam Solutions, Electro-Scientific Instruments, International Test Solutions, and JEM). During the EXPO, all aspects of the wafer sort industry and associated infrastructure suppliers were represented with twelve probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers.

The 20th Annual SW Test Workshop and EXPO will be held June 6 to 9, 2010, at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for podium and poster presentations will be open starting January 1, 2010.

Technical Program Pictures:

Technology Expo Pictures:

CONFERENCES IN 2009:

2009 International Conference on Electronics Packaging Technology/ High Density Design, Packaging and Microsystem Integration (ICEPT/HDP 2009)
August 10-13, 2009 Beijing, China
Contact: icept2009@tsinghua.edu.cn

2009 IEEE International Conference on Portable Information Devices (PORTABLE)
September 21-22, 2009 Anchorage, AK USA
http://www.ieeevtc.org/portable2009
Contact: Ephraim Suhir suhire@aol.com

2009 3rd International Conference on 3D System Integration (3DIC 2009)
September 28 – 30, 2009 San Fancisco, CA, USA
http://www.3dic-conf.org
Contact: P. Garrou pgarrou@rti.org

2009 31st Annual Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2009)
30 August – 4 September 2009 Anaheim, CA, USA
http://www.esda.org
Contact: Lisa Pimpinella lpimpinella@esda.org

2009 15th Int'l Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2009)
October 7 – 9, 2009 Leuven, Belgium
http://cmp.imag.fr/conferences/therminic/therminic2009
Contact: Chantal Bénis-Morel, chantal.benis@imag.fr

2009 4th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2009)
October 21-23, 2009 Taipei, Taiwan
http://www.impact.org.tw/2009/General/
Contact: Ms.Yaffy Liu service@impact.org.tw

2009 55th IEEE Holm Conference on Electrical Contacts (HOLM 2009)
Sept. 14-16, 2009 Vancouver, BC, Canada
http://www.ewh.ieee.org/soc/cpmt/tc1
Contact: Alicia Zupeck a.zupeck@ieee.org

2009 18th IEEE Electrical Performance of Electronic Packaging (EPEP 2009)
October 19-21, 2009 Portland, OR, USA http://www.epep.org
Contact: Kelly Sutton epd@engr.arizona.edu

2009 IEEE/CPMT Workshop on Accelerated Stress Test and Reliability (ASTR 2009)
October 7-9 2009 Jersey City, NJ USA;
http://www.ewh.ieee.org/soc/cpmt/tc7/ast2009/
Contact: Cheryl Tulkoff ctulkoff@austin.rr.com