

# EPTC 2009 Singapore

11<sup>th</sup> Electronics Packaging Technology Conference  
9<sup>th</sup> – 11<sup>th</sup> December 2009  
Shangri-La Hotel Singapore

Mark Your Calendar  
for EPTC 2009

## CALL FOR PAPERS

Selected  
Publication in IEEE

### ABOUT EPTC

The 11<sup>th</sup> Electronics Packaging Technology Conference (EPTC 2009) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society.

EPTC 2009 will feature technical sessions, short courses/forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

### CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- ❑ Advanced Packaging: Wafer level packaging, 3D integration, TSV (through Silicon Via), embedded passives & actives on substrates, flip chip packaging, RF-ID, 3D SiP, Packaging solutions for MEMS, MOEMS, NEMS, Automotive electronics, optoelectronics
- ❑ Interconnection Technologies: wire bonding technology, flip chip technology, solder alternatives (ICP, ACP, ACF, NCP), under bump metallurgy, 3D and TSV connections, microbump, substrate technology,
- ❑ Materials & Processes: Materials and processes for traditional and advanced microelectronic systems, 3D packages, MEMS, solar, green and biomedical packaging that enhance mechanical, thermal, electrical and optical performance as well as cost effectiveness.
- ❑ Modeling & Simulations: Electrical Modeling & Signal Integrity, Thermal Characterization & Cooling Solutions: Mechanical Modeling & Structural Integrity
- ❑ Quality & Reliability: Component, board and system level reliability assessment, interfacial adhesion, accelerated testing and models, advances in reliability test methods and failure analysis.
- ❑ Emerging Technology: Packaging solutions for solar photovoltaic applications, systems and packaging in the areas of bioelectronics such as biomedical, bioengineering, biosensors and electronics for medical devices; wearable electronics, organic/printable electronics; portable power supplies such as fuel cells; and other novel packaging.

### IMPORTANT DATES

Submission of abstract	15th June 2009
Notification of Acceptance	1st August 2009
Submission of manuscript	1st October 2009

### ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories (found under CONFERENCE TOPICS) for abstract review. All submissions must be in English and should be made via the online submission system found at <http://www.eptc-ieee.net>. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 15<sup>th</sup> June, 2009. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance and publication instruction by 1<sup>st</sup> August 2009. The final manuscript for publication in the conference proceedings is due by 1<sup>st</sup> October 2009. Selected papers will be published in IEEE/CPMT journals.

### OUTSTANDING TECHNICAL PAPERS

The conference proceeding is an official IEEE publication. Author(s) of Best Technical Paper and Best Student Paper will receive an award at the next conference.

### CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings. Proposals for short courses can be submitted to [seungwook.yoon@statschippac.com](mailto:seungwook.yoon@statschippac.com).

### CALL FOR SPONSORSHIP / EXHIBITION PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. Potential exhibitors and sponsors may email [secretariat@eptc-ieee.net](mailto:secretariat@eptc-ieee.net) for details.

General Chairs: Mr. James HOW / Mr. Yew Cheong MUI  
Technical Chair: Dr. Seung Wook YOON

Organized by



IEEE Reliability/CPMT/ED Singapore Chapter

Sponsored by



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Supported by



SINGAPORE EXHIBITION & CONVENTION BUREAU

Held in



[www.visitsingapore.com](http://www.visitsingapore.com)

Conference information & contacts: Website: <http://www.eptc-ieee.net> Email: [secretariat@eptc-ieee.net](mailto:secretariat@eptc-ieee.net)



# 2009 IEEE Electrical Design of Advanced Packaging & Systems Symposium



December 2-4, 2009 Hong Kong / Shenzhen, China

<http://www.edaps2009.org/>

Email: [edaps2009@ee.cuhk.edu.hk](mailto:edaps2009@ee.cuhk.edu.hk)

Call for Papers

## The 2009 IEEE EDAPS Symposium

The Electrical Design of Advanced Packaging & Systems (EDAPS) has been the premier international signal integrity symposium in Asia region since 2002. The symposium consists of paper presentations, industry exhibitions, workshops and tutorials. The 2009 EDAPS will be jointly sponsored by The Chinese University of Hong Kong, Applied Science and Technology Research Institute (ASTRI), Innovation and Technology Commission of Hong Kong SAR Government and the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).

The purpose of EDAPS Symposium is to enhance the technical awareness and technology collaborations in the Asia region specifically in the electrical designs of chip, package and system levels from design concepts, technical challenges to the modeling and EDA tools. The papers of the symposium not only address the current technical issues but also bring out the challenges facing to IC design, SiP/SoP packaging, EMI/EMC, and EDA tools. The symposium is a major venue for creating the opportunity for the researchers and practitioners from the diverse fields to exchange information and build up the network.

## Venue

The 2009 EDAPS will be held in the spectacular campus of The Chinese University of Hong Kong during December 3-4, 2009. In order to promote the state-of-the-art technologies to the electronics-related industries in China, a one-day session consisting of technical tutorials and workshops will be held in Shenzhen, China on December 2.

## Important Deadlines and Dates:

Print-ready 4-page Full Paper Submission (up to 4 pages in PDF format only)	<b>10 August 2009</b>
Paper Acceptance Notification	<b>14 September 2009</b>
Advanced Program Available on Website	<b>31 October 2009</b>

### Symposium Chair:

Prof. Ke-Li Wu,  
[klwu@ee.cuhk.edu.hk](mailto:klwu@ee.cuhk.edu.hk)

### Symposium Co-Chair:

Prof. Bing Li,  
[leibp@nus.edu.sg](mailto:leibp@nus.edu.sg)

### Technical Program Committee Chair:

Dr. Tom Chung,  
[tomchung@astri.org](mailto:tomchung@astri.org)

### Local Arrangement Committee Chair:

Prof. Kwok Keung, Michael, Cheng  
[kkcheng@ee.cuhk.edu.hk](mailto:kkcheng@ee.cuhk.edu.hk)

### International Steering Committee Members:

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## Organizers/Sponsors:



Innovation and Technology Commission  
The Government of the Hong Kong Special Administrative Region

Call for Papers [www.edaps2009.org](http://www.edaps2009.org)



## Key Topics of the 2009 EDAPS:

- Signal integrity topics including High-speed Digital Signal Integrity Modeling, Design, and Measurement;
- Power Distribution Network;
- System in Package (SiP)/System on Package (SoP) Design;
- High-performance Packaging for System on Chip (SoC);
- RF/Microwave Packaging for Wireless Communication and Mobile Phone;
- Interconnect Modeling, Simulation, and Measurement;
- Embedded Passives Modeling and Measurement;
- High-speed Channels Modeling and Measurement;
- EMI/EMC and Electromagnetic Modeling and Measurement;
- EDA Tools for Chip, Package, and Board Co-design and Simulation.

## Guidelines for Paper Submission:

Authors are requested to submit a preliminary paper up to 4 pages in length, including title, author's affiliation, abstract, figures and references.

All submissions must be made through EDAPS2009 website: [www.edaps2009.org](http://www.edaps2009.org) and must be in electronic format (PDF).

A MS-Word template is available on the symposium website. No hardcopy submission will be accepted.

### Symposium Program:

Tutorials:	2 December 2009
Plenary Speeches:	3 December 2009
Oral Presentations:	3 – 4 December 2009
Poster Presentations:	3 – 4 December 2009
Exhibition:	3 – 4 December 2009
Banquette:	3 December 2009



Call for Papers [www.edaps2009.org](http://www.edaps2009.org)

# 11<sup>th</sup> International Conference on Electronic Materials and Packaging (EMAP 2009) Penang, Malaysia

Dec. 1-3, 2009

The 11th Electronic Material and Packaging Conference (EMAP 2009) is an international event organized by the School of Mechanical Engineering, Universiti Sains Malaysia (USM), with technical co-sponsorship from the CPMT Society of IEEE. EMAP 2009 will feature short courses, technical sessions, and an exhibition.

This conference is an international forum of experts and researchers for the exchange, dissemination and discussion of state-of-the-art technologies and recent developments in electronic materials, packaging, manufacturing and assembly. Since 1999, EMAP has gained a reputation as a premier electronic materials and packaging conference in the Asia-Pacific region

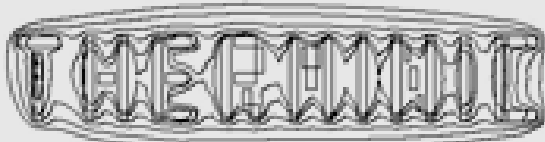
where most of the electronic packaging activities are taking place.

Experts from reputed industries like Intel, Silterra etc. and academicians from major universities will deliver keynote lectures. A tabletop exhibition from suppliers of materials, equipments, components and software, and from service providers of electronics industry will be held at the venue of the conference.

For more information, and the full Advance Program (when posted), visit:

[mechanical.eng.usm.my/EMAP2009](http://mechanical.eng.usm.my/EMAP2009)

Visit EMAP the week before EPTC, in Singapore!



THERMINIC Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. These questions are becoming more and more crucial with the increasing element density of circuits packaged together and with the move to nanotechnology. These trends are calling for thermal simulation, monitoring and cooling. Thermal management is expected to become an increasingly dominating factor of a system's cost. The growing power dissipated in a package, and the mobile parts of Microsystems, raise new thermal problems to be solved in the near future necessitating the regular discussion by the experts in these fields. Finally, there is an increasing need for accurate assessment of the boundary conditions used in the analysis of electronic parts, which requires a concurrent solution of the thermal behaviour of the whole system.

## 15th International Workshop on Thermal investigations of ICs and Systems

Leuven, Belgium -- 7-9 October 2009

This year THERMINIC will address in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomena in "high-tech" systems.

**Leuven** is a university town located 30km to the east of Brussels. The workshop is hosted at the Faculty Club, a unique conference and banqueting centre, welcoming guests to the calm and tranquility of the 13<sup>th</sup> century Infirmerie of the Grand Beuginage and the Convent of Chièvres, built in 1561.

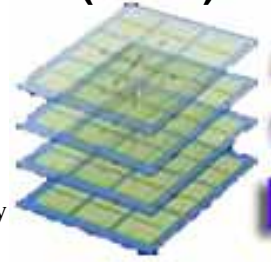
For information, and to register:

[cmp.imag.fr/conferences](http://cmp.imag.fr/conferences)

# IEEE International Conference on 3D System Integration (3D IC)

September 28-30, 2009

San Francisco



This conference combines the previous ASET and IEEE EDS Society sponsored **International 3D System Integration Conference**, held in Tokyo in 2007 & 2008, and the IEEE CPMT sponsored **3D System Integration Conference** held in 2005 & 2007 in Munich. The new, combined Conference will be held in San Francisco.

**3D IC** will cover all 3D IC topics, including 3D process technology, materials, equipment, circuits technology, design methodology and applications. The conference invites authors and attendees to submit and interact with 3D researchers from all around the world.

## TOPICAL AREAS:

- 3D IC Technology
- 3D IC Circuits Technology
- 3D Applications
- 3D Design Methodology
- Test and Reliability of 3D Systems

To receive further information about 3D IC, or to register:

[www.3dic-conf.org](http://www.3dic-conf.org)



## ASTR 2009 Workshop on Accelerated Stress Testing & Reliability

October 7-9, 2009 Jersey City, NJ USA

The purpose of the ASTR Workshop is to share ideas on better ways of accelerating and detecting hidden defects, flaws, and weaknesses in electronic and electro-mechanical hardware that would result in failures during usage.

For more information:

[www.ewh.ieee.org/soc/cpmt/tc7/ast2009](http://www.ewh.ieee.org/soc/cpmt/tc7/ast2009)

## IEEE CPMT Symposium Japan

The VLSI Packaging Workshop in Japan (<http://vlsi-pkg-ws.org/vlsi-pkg.html>) has been held biannually since 1992 in Kyoto, and it has become a well-known international workshop for advanced packaging technologies. Due to ever increasing activities and changing demands, the committee has reviewed its mission, cooperated with the members of IEEE CPMT Japan Chapter, refurbished the workshop, and started the new symposium—IEEE CPMT Symposium Japan. It will provide component, packaging, and manufacturing researchers who are extending their activities beyond borders with opportunities to exchange technical knowledge and perspective. The committee strongly encourages you to attend this symposium and participate in the discussion, to understand the technology trends and find the best targets for your technology/business development. Bring your latest research results and share with the participants who are experts from the industry and the grove of Academe, and discuss with them. Anybody contributing to the achievement of a sustainable society through electronics is very welcome at this symposium.

### Important information

- Submission of abstract: Feb. 15, 2010
- Notification of acceptance: Mar. 31, 2010
- Submission of manuscript: May 15, 2010
- Conference dates: Aug. 24, 25, and 26, 2010.
- Venue: The University of Tokyo, Japan

### Technical area

- + System in a Package (SiP)
- + Advanced Fine Pitch Packaging
- + 3D Packaging & COC (Chip on Chip)
- + Wafer Level CSP
- + Packaging for Optoelectronics
- + Packaging for Automobile
- + RF Components & Modules / RF Tags
- + Integrated Passives / Embedded Components
- + Laminated Materials & Processing
- + Board level reliability
- + MEMS Packaging Technologies
- + Nano-Technology
- + Micro Bumping Technology
- + Electrical Performance & Thermal Management
- + Failure Mechanisms & Reliability Improvement
- + Materials for High Speed Application & Wafer Process
- + Green Material
- + Assembly and Packaging Challenges for Cu/Low-k Chips
- + Emerging Technologies

### Contact person

General Chair: Hirofumi Nakajima, NEC Electronics Co. ([hirofumi.nakajima@necel.com](mailto:hirofumi.nakajima@necel.com))

Vice Chair: Hiroshi Yamada, Toshiba Co. ([hiroshi.yamada@toshiba.co.jp](mailto:hiroshi.yamada@toshiba.co.jp))

Program Chair: Shigenori Aoki, Fujitsu Laboratories Ltd. ([aoki.shigenori@jp.fujitsu.com](mailto:aoki.shigenori@jp.fujitsu.com))



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**[nsltr-input@cpmt.org](mailto:nsltr-input@cpmt.org)**

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**Visit [ieeexplore.ieee.org](http://ieeexplore.ieee.org) and download them**

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**[WWW.IEEE.ORG/mgm/](http://WWW.IEEE.ORG/mgm/)**

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**by Organizing and Attending**  
**Additional Information at [www.cpmt.org/conf/](http://www.cpmt.org/conf/)**



## 2009 IEEE Electrical Design of Advanced Packaging & Systems Symposium

December 2-4, 2009 Hong Kong / Shenzhen, China

The EDAPS has been the premier symposium on electrical designs at chip, module and system levels in Asia since 2002. The symposium consists of paper presentations, industry exhibitions, workshops and tutorials. The purpose of EDAPS is to enhance the technical awareness and technology collaborations in the Asia region specifically in the electrical designs of chip, package and system levels from design concepts, technical challenges to the modeling and EDA tools. The symposium provides a major venue for researchers and practitioners from the diverse fields to exchange information and for networking.

The EDAPS **online paper submission** is NOW on till 31 August 2009! We sincerely invite you and your colleagues or students to submit a paper and participate in this year's EDAPS. For details, please refer to the official website: [www.edaps2009.org](http://www.edaps2009.org)

In this year, EDAPS is to be held on December 2 in Shenzhen, China (for workshops and tutorials) and on December 3 and 4 in the spectacular campus of CUHK, Hong Kong, China.

The EDAPS has a wide technical coverage serving the communities of IC design, SiP/SoP packaging, EMI/EMC, and EDA tools, etc. All accepted papers will be included in IEEE Xplore and indexed by EI. Come to EDAPS 2009 to learn, to do business, to make new acquaintances and to network with old friends. See you in Shenzhen and Hong Kong in December 2009!

### Important Dates:

Print-ready 4-page Full Paper Submission: 31 Aug. 09

Paper Acceptance Notification: 30 Sept. 09

Advanced Program Available on Website: 31 Oct. 09

The 2009 EDAPS is jointly sponsored by The Chinese University of Hong Kong, Hong Kong Applied Science and Technology Research Institute (ASTRI), Innovation and Technology Commission of Hong Kong SAR Government, and the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).

## SECOND FLEXIBLE ELECTRONICS SYMPOSIUM

DATE: Wednesday, August 19, 2009,

TIME: 7:30am - 4:45pm

LOCATION: Traditions at the Glen, Johnson City, NY

**SPONSORS:** BU Center for Advanced Microelectronics Manufacturing (CAMM); IEEE Components, Packaging and Manufacturing Technology Society (CPMT) -- Binghamton Chapter; Sandia National Laboratory; Cornell University

This symposium brings together leading researchers from academia, national labs, and industry in the fields of flexible electronics, functional printing, and emerging electronic materials to review and share new research findings in critical technology areas and identify issues for the rapidly growing flexible electronics field. It provides opportunities for discussion of key research and development areas and sharing of ideas and information. At the close of the technical agenda, attendees may tour the CAMM development facilities, a national research laboratory focusing on roll-to-roll electronics.

### Symposium at a Glance

-- CAMM Research Program -- Industry-Academic Panel Discussion on Materials-Related Challenges in Flexible and Organic Electronics -- Industry Perspectives on Flexible Electronics Initiatives -- Pressure Sensors on Flex -- Stretchable Electronics -- CAMM Facility Tour (5:00-6:30 pm)

Technical events will be followed by an optional, no-host, Networking Dinner on the Binghamton University campus at 6:45pm (\$30 fee). Registration is required for event attendance. No fee is required for attending technical events.

Information: [guest.cvent.com/EVENTS/Info/Agenda.aspx?e=60856a63-5f6b-44f0-addb-39e916f894d2](http://guest.cvent.com/EVENTS/Info/Agenda.aspx?e=60856a63-5f6b-44f0-addb-39e916f894d2)

COMPONENTS, PACKAGING AND  
MANUFACTURING TECHNOLOGY SOCIETY

**ECTC Electronic Components & RF Program Committee**  
**CPMT RF & Wireless Technical Committee**

**60th ECTC June 1 – June 4, 2010**

**Paris Las Vegas Hotel**  
**Las Vegas, Nevada USA**

The ECTC Electronic Components & RF Program Committee and the CPMT RF & Wireless Technical Committee encourage you to submit an abstract to ECTC 2010 in the areas of passive components & networks, RF & Microwave components & modules, and subsystems. ECTC is the premier Electronic Components and Packaging conference held annually and attended by about 1000 delegates with equal participation from companies and academia. As in the past, Electronic Components, RF & Microwave, and MEMS related papers are solicited for focus sessions during this prestigious conference.

**Discrete Passive Components**

Design, materials, processes, and manufacturing considerations for discrete passive components: resistors, capacitors, inductors, and passive networks.

**Integrated & Embedded Components**

Design, materials, processing, modeling, manufacture, and characterization of integrated & embedded passive & active components on silicon, organic, ceramic, ultra-thin, and glass type substrates for digital, mixed signal, and RF applications; metamaterials, component integration for power converter modules.

**RF & Microwave Components**

Integrated antennas, filters, baluns, RFID/sensors, RF MEMS, MEMS, MEMS packaging, tunable devices and switches, high power and high efficiency RF/Microwave power amplifiers – design, technology and high frequency characterization

**RF & Microwave Modules**

Module Integration technologies in semiconductor, organic, and glass substrates – System in Package, System on Chip, Package on Package, and 3D integration; shielding and isolation

**Materials, Processing, Reliability, & Manufacture of Electronic Components**

Design, High permeability and high permittivity materials at high frequencies and their processing, yield and reliability aspects of electronic components, through silicon vias, wafer level RDL, and nanostructured materials and processes,

**SUBMISSIONS:**

Please submit abstracts using the ECTC web site: [www.ectc.net](http://www.ectc.net) by October 15, 2009. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the “Electronic Components & RF” focused sessions

**YOU MUST SELECT “Electronic Components & RF” committee as your PRIMARY subcommittee preference** when you submit your abstract at the ECTC web site. Again, to have your paper considered for the electronic components & RF/microwave sessions, please do the following:

STEP #1: Submit abstract through the ECTC web site ([www.ectc.net](http://www.ectc.net)) and select **“Electronic Components & RF” as PRIMARY subcommittee preference**

STEP #2: Email abstract copy and author’s email & contact information to:  
Craig Gaw at [c.a.gaw@ieee.org](mailto:c.a.gaw@ieee.org) & Amit Agrawal at [amiagra2@cisco.com](mailto:amiagra2@cisco.com)

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# 26

Semiconductor Thermal Measurement and Management Symposium  
Hyatt Hotel, Techmart, Santa Clara, CA, USA  
February 21-25, 2010

## CALL FOR PAPERS

SEMI-THERM is the world's leading forum on the thermal management of electronics. For 25 years it has fostered the exchange of knowledge between practicing thermal engineers, professionals and industry experts, while showcasing the latest academic and industrial advances in electronics thermal management.

In its 26th year, SEMI-THERM will include Invited Speakers, Panel Sessions, Technical Sessions, Short Courses, an Evening Tutorial, Exhibits and dedicated Vendor Workshops. SEMI-THERM actively solicits student papers and awards travel stipends and reduced conference fees to student participants. Those papers deemed to be among the best in the conference will be invited to be published in the *IEEE Transactions on Components and Packaging Technologies*.

### Subjects of Particular Interest

SEMI-THERM is soliciting papers on current thermal management technologies and practical application issues, modeling and measurement of electronic components and systems including, but not necessarily limited to, the following areas:

<b>Component Level Thermal Management</b> Die, Package	<b>Experimental Analysis</b> Liquid Cold Plates, Manifold Microchannels, DOE
<b>System Level Thermal Management</b> Boards, Enclosures	<b>Multidisciplinary Thermal Design</b> Acoustic interactions, Cost Trade-Off, Design for Reliability
<b>Chip &amp; System Packaging Materials</b> TIMs, Heatspreaders, Nanomaterials, Material Characterization	<b>Datacenter Thermal Management</b> Metrics, Best Practices, Efficient Layout, Industry Trends
<b>Modeling</b> CFD, Compact Models, FEM/BEM, Novel Approaches	<b>Thermal-Aware Design</b> Energy Usage-optimized Designs, Leakage Power, CPU Power management, Airmover Control Technologies
<b>Traditional &amp; Enabling Technologies</b> Conduction, Convection, Radiation, Air, Liquid, Two Phase, Vapor Compression/Refrigeration, Fans and Blowers, Solid State Airmovers,	<b>Application Environments</b> Consumer, High Volume, Portable, Harsh Environments, LED, Medical, Telecom, Automotive, Solar Photovoltaic, Military, Power and Storage Systems

The selection of papers for the Symposium is solely based on an extended abstract, which should provide a complete summary of the proposed paper comprised of work or results not previously presented or published. Submitted abstracts should be between 2 and 5 pages of single spaced text giving the key results, findings and conclusions, supported by additional pages of figures, tables and references as appropriate. **Abstracts are expected to demonstrate that the proposed papers are appropriate for SEMI-THERM and of high technical quality.** Abstracts must be submitted electronically in RTF, DOC or PDF formats via the SEMI-THERM web site.

The intent of technical papers is to communicate timely and relevant technical information to a technical audience. The paper should present an unbiased description of a certain method or product, discussing both pros and cons. Both subtle and blatant advertisement of any products or services is in direct conflict with the spirit of the Symposium. Examples of the former include repeated references to products or trade names and excessive use of corporate logos and trademarks in graphic illustrations. Photographs of commercial equipment are not permitted unless they add educational value. The SEMI-THERM Program Committee desires that all authors and presenters understand unambiguously that commercialism is inappropriate and will not be tolerated; authors are asked to abide by these constraints when preparing their abstracts, papers, and presentations.

### Key Dates

**Abstract Deadline**  
August 17, 2009

**Abstract Acceptance Notification**  
October 10, 2009

**Photo-ready Full Manuscript Due**  
December 17, 2009

For further information please contact the Program Chair via email:

[Sai Ankireddi, Sun Microsystems Inc.](mailto:sai.ankireddi@sun.com)

E-mail: [sai.ankireddi@alumni.purdue.edu](mailto:sai.ankireddi@alumni.purdue.edu), Phone: 408-582-2231

Visit the SEMI-THERM web site at: <http://www.semi-therm.org>

**IEEE Components, Packaging and Manufacturing  
Technology Society**

Marsha Tickman, Executive Director  
445 Hoes Lane  
Piscataway, NJ 08854 USA



**Future Directions in IC and  
Package Design Workshop (FDIP)**

**October 18, 2009, Portland, OR USA**

**Special Topic: What Research is Planned for EM Tools  
and How Are They Made Available to Computer De-  
signers**

FDIP includes 7 talks on key topics; see the Advance Pro-gram for the listing. FDIP is held immediately before EPEP – be sure to schedule this extra day into your travel plans! Register by September 20<sup>th</sup>, 2009

More information: [www.epeps.org](http://www.epeps.org)

*CPMT and MTT Societies*

**18th Conference on  
Electrical Performance of  
Electronic Packaging (EPEP 2009)**

**October 19-21, 2009  
Portland, Oregon USA**

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