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From the *Transactions on Components, Packaging and Manufacturing Technology:*

Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring

Jonghyun Cho; Eakhwan Song; Kihyun Yoon; Jun So Pak; Joohee Kim; Woojin Lee; Taigon Song; Kiyeong Kim; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Minsuk Suh; Kwangyoo Byun; Joungho Kim; **Issue Date:** Feb. 2011 Page(s): 220–233

In three-dimensional integrated circuit (3D-IC) systems that use through-silicon via (TSV) technology, a significant design consideration is the coupling noise to or from a TSV. It is important to estimate the TSV noise transfer function and manage the noise-tolerance budget in the design of a reliable 3D-IC system. In this paper, a TSV noise coupling model is proposed based on a three-dimensional transmission line matrix method (3D-TLM). Using the proposed TSV noise coupling model, the noise transfer functions from TSV to TSV and TSV to the active circuit can be precisely estimated in complicated 3D structures, including TSVs, active circuits, and shielding structures such as guard rings. To validate the proposed model, a test vehicle was fabricated using the Hynix via-last TSV process. The proposed model was successfully verified by frequency- and time-domain measurements. Additionally, a noise isolation technique in 3D-IC using a guard ring structure is proposed. The proposed noise isolation technique was also experimentally demonstrated; it provided −17 dB and −10 dB of noise isolation between the TSV and an active circuit at 100 MHz and 1 GHz, respectively.

PDN Impedance Modeling and Analysis of 3D TSV IC by Using Proposed P/G TSV Array Model Based on Separated P/G TSV and Chip-PDN Models

Jun So Pak; Joohee Kim; Jonghyun Cho; Kiyeong Kim; Taigon Song; Seungyoung Ahn; Junho Lee; Hyungdong Lee; Kunwoo Park; Joungho Kim; **Issue Date:** Feb. 2011 Page(s): 208–219

The impedance of a power-distribution network (PDN) in three-dimensionally stacked chips with multiple through-silicon-via (TSV) connections (a 3D TSV IC) was modeled and analyzed using a power/ground (P/G) TSV array model based on separated P/G TSV and chip-PDN models at frequencies up to 20 GHz. The proposed modeling and analysis methods for the P/G TSV and chip-PDN are fundamental for estimating the PDN impedances of 3D TSV ICs because they are composed of several chip-PDNs and several thousands of P/G TSV connections. Using the proposed P/G TSV array model, we obtained very efficient analyses and estimations of 3D TSV IC PDNs, including the effects of TSV inductance and multiple-TSV inductance, depending on P/G TSV arrangement and the number of stacked chip-PDNs of a 3D TSV IC PDN. Inductances related to TSVs, combined with chip-PDN inductance and capacitance, created high upper peaks of PDN impedance, near 1 GHz. Additionally, the P/G TSV array produced various TSV array inductance effects on stacked chip-PDN impedance, according to their arrangement, and induced high PDN impedance, over 10 GHz.

High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)

Joohee Kim; Jun So Pak; Jonghyun Cho; Eakhwan Song; Jeonghyeon Cho; Heegon Kim; Taigon Song; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Min-Suk Suh; Kwang-Yoo Byun; Joungho Kim; **Issue Date:** Feb 2011 Page(s): 181–195

We propose a high-frequency scalable electrical model of a through silicon via (TSV). The proposed model includes not only the TSV, but also the bump and the redistribution layer (RDL), which are additional components when using TSVs for 3-D integrated circuit (IC) design. The proposed model is developed with analytic *RLGC* equations derived from the physical configuration. Each analytic equation is proposed as a function of design parameters of the TSV, bump, and RDL, and is therefore, scalable. The scalability of the proposed model is verified by simulation from the 3-D field solver with parameter variations, such as TSV diameter, pitch between TSVs, and TSV height. The proposed model is experimentally validated through measurements up to 20 GHz with fabricated test vehicles of a TSV channel, which includes TSVs, bumps, and RDLs. Based on the proposed scalable model, we analyze the electrical behaviors of a TSV channel with design parameter variations in the frequency domain. According to the frequency-domain analysis, the capacitive effect of a TSV is dominant under 2 GHz. On the other hand, as frequency increases over 2 GHz, the inductive effect from the RDLs becomes significant. The frequency dependent loss of a TSV channel, which is capacitive and resistive, is also analyzed in the time domain by eye-diagram measurements. Due to the frequency dependent loss, the voltage and timing margins decrease as the data rate increases.

Design, Modeling, and Evaluation of a Multiband MIMO/ Diversity Antenna System for Small Wireless Mobile Terminals

Qinjiang Rao Wilson, K. P.; **Issue Date:** March 2011 Page(s): 410–419

A new multiband diversity antenna is presented, which is suitable for multiband diversity and multiple-input multiple-output antenna systems for small wireless mobile terminals. The antenna consists of two branches of folded monopoles, at least one of which is terminated with a rectangular patch. By slightly tuning the width of the patch, the antenna can simultaneously achieve a flexible frequency ratio and a desired bandwidth. An example design is presented for most application bands, from 890 MHz through

6 GHz, which operates in a real-world cellular phone environment, including near-field interactions with other phone components and a model of a human head (the SAM phantom). The simulated and experimental results, including S-parameters, radiation patterns, signal correlations and mean effective gain, have validated the proposed antenna design as useful for compact mobile devices.

Low Phase Noise and Low Power Consumption VCOs Using CMOS and IPD Technologies

Yuan-Chia Hsu; Hwann-Kaeo Chiou; Hsien-Ku Chen; Ta-Yeh Lin; Da-Chiang Chang; Ying-Zong Juang; **Issue Date:** May 2011 Page(s) 673–680

This paper presents two voltage controlled oscillators (VCOs) operating at 5.42 and 5.76 GHz implemented in 0.18-μm complementary metal-oxide semiconductor (CMOS) technology with integrated passive device (IPD) inductors. One IPD inductor was stacked on the top of the active region of the 5.76-GHz VCO chip, whereas the other IPD inductor was placed on the top of the 5.42-GHz VCO CMOS chip but far from the its active region. The high-quality IPD inductors reduce the phase noise of the VCOs. The measurements of the two VCOs indicate the same phase noise of −120 dBc/Hz at 1 MHz offset frequency. These results demonstrate a 6-dB improvement compared to the VCO using an on-chip inductor. This paper also presents the effect of the coupling between the IPD inductor and the active region of the chip on the phase noise performance.

From the *Transactions on Components and Packaging Technologies:*

Dynamic Lithium-ion Battery Model for System Simulation

Lijun Gao; Shengyi Liu; Dougal, R. A.; **Issue Date:** Sep. 2002 Page(s): 495–505

Presents here a complete dynamic model of a lithium ion battery that is suitable for virtual-prototyping of portable battery-powered systems. The model accounts for nonlinear equilibrium potentials, rate- and temperature-dependencies, thermal effects and response to transient power demand. The model is based on publicly available data such as the manufacturers' data sheets. The Sony US18650 is used as an example. The model output agrees both with manufacturer's data and with experimental results. The model can be easily modified to fit data from different batteries and can be extended for wide dynamic ranges of different temperatures and current rates.

Power and Life Extension of Battery-ultracapacitor Hybrids

Dougal, R. A. Liu, S. White, R. E.; **Issue Date:** Mar. 2002 Page(s): 120–131

The performance of a battery-ultracapacitor hybrid power source under pulsed load conditions is analytically described using simplified models. We show that peak power can be greatly enhanced, internal losses can be considerably reduced, and that discharge life of the battery is extended. Greatest benefits are seen when the load pulse rate is higher than the system eigenfrequency and when the pulse duty is small. Actual benefits are substantial; adding a 23 F ultracapacitor bank (3 × 7 PC10 ultracapacitors) in parallel with a typical Li-ion battery of 7.2 V and 1.35 A hr capacity can boost the peak power capacity by 5 times and reduce the power loss by 74%, while minimally impacting system volume and weight, for pulsed loads of 5 A, 1 Hz repetition rate, and 10% duty.

From the *Transactions on Advanced Packaging:*

Noise Isolation in Mixed-Signal Systems Using Alternating Impedance Electromagnetic Bandgap (AI-EBG) Structure-Based Power Distribution Network (PDN)

Jinwoo Choi Govind, V. Swaminathan, M. Bharath, K.; **Issue Date:** Feb. 2010 Page(s): 2–12

This paper presents efficient noise isolation and suppression method in mixed-signal systems using alternating impedance electromagnetic bandgap (AI-EBG) structure-based power distribution network (PDN). Currently, split planes are used for isolation in mixed-signal systems for isolating sensitive RF/analog circuits from noisy digital circuits. However, split planes show good isolation only at low frequencies due to electromagnetic coupling through the gap. The AI-EBG structure-based PDN presented in this paper provides excellent isolation (−80 dB ~ −100 dB) in the frequency range of interest by suppressing almost all possible electromagnetic modes. The AI-EBG structure has been integrated into a mixed-signal test vehicle to demonstrate the isolation level achievable. The ability of the AI-EBG structure to suppress switching noise has been quantified in this paper. The AI-EBG structure provided greater than 100 dB of isolation in passive S-parameter measurement and suppressed in-band noise down to −88 dBm of isolation in a functional test.

Defect Detection of Flip Chip Solder Bumps With Wavelet Analysis of Laser Ultrasound Signals

Jin Yang Ume, I. C. Lizheng Zhang; **Issue Date:** Feb. 2010 Page(s): 19–29

Microelectronics packaging technology has evolved from through-hole and bulk configuration to surface-mount and small-profile ones. In surface mount packaging, such as flip chips, chip scale packages, and ball grid arrays, chips/packages are attached to the substrates/printed wiring board (PWB) using solder bump interconnections. Solder bumps hidden between the chips/packages and the substrate/board are no longer visible for inspection. A novel solder bump inspection system has been developed using laser ultrasound and interferometer techniques. This system has been successfully applied to detect solder bump defects including missing, misaligned, open, and cracked solder bumps in flip chip packages, chip scale packages and land grid arrays. The system uses a pulsed Nd:YAG laser to induce ultrasound in the thermoelastic regime and the transient out-of-plane displacement response in nanometer scale on the package surface is measured using the interferometer technique. In this paper, wavelet analysis of laser ultrasound signals is presented and compared to previous signal processing methods, such as error ratio and correlation coefficient. The results show that wavelet analysis increases measurement sensitivity for inspecting solder bumps in electronic packages. Laser ultrasound inspection results are also compared to X-ray results. In particular, this paper discusses defect detection for a 6.35 mm ?? 6.35 mm ?? 0.6 mm PB18 flip chip package and flip chip package (??SiMAF??) with 24 lead-free solder bumps. These two types of flip chip specimens are both nonunderfilled.

From the *Transactions on Electronics Packaging Manufacturing:*

Acid Decapsulation of Epoxy Molded IC Packages With Copper Wire Bonds

Murali, S. Srikanth, N.; **Issue Date:** July 2006 Page(s): 179–183

Epoxy molded IC packages with copper wire bonds are decapsulated using mixtures of concentrated sulfuric acid (20%) and fuming nitric acid in an automatic decapping unit and, observed with minimal corrosion of copper wires (0.8-6 mil sizes) and bond interfaces. To attain maximum cross-linking of the molded epoxies, the post mold cured packages (175 °C for 4 h) were further, aged at high temperature of 150 °C for 1000 h. These packages are decapsulated using mixtures of higher ratio of concentrated sulfuric acid (40%) along with fuming nitric acid. The shear strength of copper wire bonds with 1 mil (25 mum) diameter of the decapsulated unit is higher than 5.5 gf/mil^2. The present study shows copper stitch bonds to Au, Cu, Pd, and Sn alloy plated surfaces are less affected on decapping, with a few grams of breaking load on stitch pull test, while stitch bonds on silver plated surfaces reveal lifting of wire bonds on decapping.

Printed circuit board recycling: a state-of-the-art survey

Jianzhi Li Shrivastava, P. Zong Gao Hong-Chao Zhang; **Issue Date:** Jan. 2004 Page(s): 33–42

This survey is done with an intention of providing a clear and comprehensive review of current practices and recent developments in the area of printed circuit board (PCB) recycling. The aim of this paper is to be a reference for research and implementation for the PCB recycling process. Original information is collected from the companies engaged in the PCB recycling industry and articles published after 1990. The paper gives an overview of the PCB structure, material composition and different recycling processes.
