ECTC General Chair Rajen Das (standing, center).

Chris Bower, Semprius - winner of "Introduction to System-on-Package," written and donated by R.Tummala.

discussing the success of the conference while eating good food (and desserts).

On Friday, Technical sessions continued till 5 PM. At the luncheon, General Chair Rajen Dias of Intel received the ECTC General Chair award from CPMT Representative C. P. Wong.

Conference attendees never feel sad at the last day of the conference thanks to the raffle drawings announced by ECTC Treasurer Tom Reynolds at the luncheon.

The First Call for Papers for 62nd ECTC is already out and can be found at www.ectc.net. You are invited to submit an abstract by October 10, 2011. In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses.

See you at the 62nd ECTC in San Diego, CA next year!

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## 2011 IEEE Semiconductor Wafer Test Workshop

***Submitted by Jerry Broz, Ph.D., General Chair of IEEE SW Test and IEEE Senior Member***

San Diego, CA: Wafer level test and probe technologists from around the world met in San Diego, CA, from June 12 to 15, 2011 for 21th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) at the Rancho Bernardo Inn in San Diego, CA. This annual IEEE / CPMT sponsored workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. SW Test 2011 began with a Sunday tutorial from Intel Corporation on the basics of statistical analysis with applicability to wafer level sort and data analysis. Starting Monday morning, the next three days were filled with a broad technical program; 5-hours of supplier exhibits (which did not compete with the technical sessions), and a San Diego Safari Park Social Networking Event.

SW Test 2011 had a total of 305 attendees from 15 countries with 30% of the attendees from outside the US to make the 2011 Workshop a truly global gathering of leading probe technologists. As always, there was a great mix of end-users (~31%) and suppliers / vendors (~69%) that were in attendance during the three day event. This unique workshop provides for plenty of time for informal interaction to discuss problems and promotes a friendly networking environment between colleagues as well as new attendees.

On Sunday night, Dr. William Chen, Sr. Advisor at ASE Group and former President of CPMT, made a thought provoking Keynote Presentation entitled, "*From Backend to Front End*".

Dr. William Chen began with a perspective into device packaging / assembly development that will likely affect wafer level test technologies. He reminded the attendees that Moore's Law is NOT a Law of Nature; it is however, an "expectation of continuity for innovation and invention" and a "promise of innovation and creativity for the semiconductor industry".

Dr. Chen discussed that overall society life experience improvements have been achieved through key product cycles within computing (personal computing), communication (wireless and wired), information (virtual sociality), and life sciences (medical and biotechnologies).

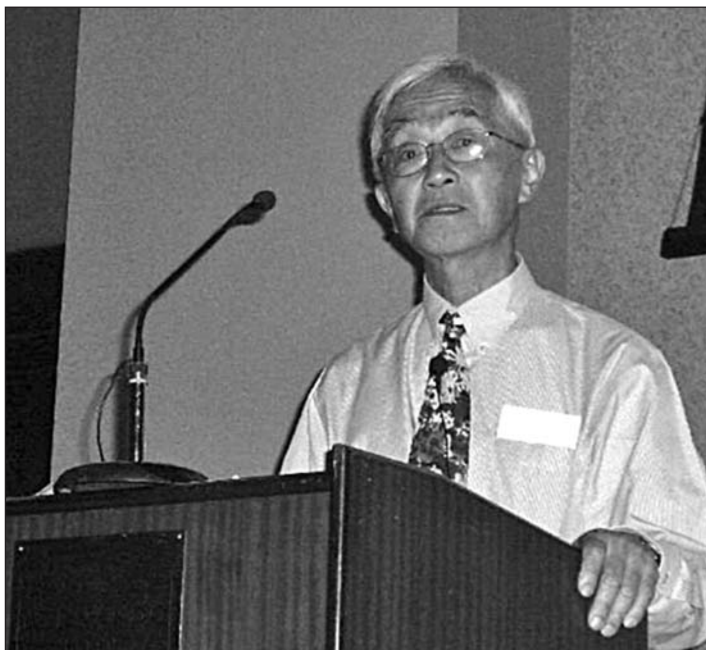
The changing landscape for packaging technologies to support future product life cycles will be driven by the critical integration of an increasing number of semiconductor device types within various electronics. According to Dr. Chen, the concepts of "More Moore" and "More than Moore" are the major trends that are currently driving semiconductor devices and packaging developments and architecture innovation.

"More Moore" can be described by continued shrinking of physical feature sizes of the digital functionalities in order to improve density and performance. It is, however, necessary to move past "More Moore", which works well for the digital world, but not for interfacing with the actual physical world. The "More-than-Moore" approach allows for the non-digital functionalities to

migrate from the system board-level into the package (SiP) or onto the chip (SoC). Incorporation of such functionalities does not scale according to "Moore's Law", but does have potential to provide substantial value to the end user in different ways.

In his opinion, Dr. Chen believes that one of the important trends in packaging includes the incorporation of system level integration through System in Package (SiP). This technology enables equivalent scaling through functional diversification of embedded active and passive components as well as integration of more functionality. The advent of 3D packaging will provide a fundamental paradigm change that will be based upon technology and infrastructure from flip chip and wafer level packaging and test. The speed and power advantages of 3D-TSV allow for a faster circuit speed with reduced power consumption. As an example, standby power can be reduced by 75% when compared to PoP and MCP packages and with a smaller physical size.

Dr. Chen discussed that with current practices, wafer level testing test can clearly identify whether a semiconductor die is "probably good" prior to packaging. Backend test can then determine whether the device is still good after packaging. However, with the advent of 3D packaging and stacked die complexity, it becomes more and more difficult to properly determine if the die has "gone bad" or if the packaging has created a "defective device". Dr. Chen concluded that in our industry the backend (wafer test and package test) will be coming to the forefront of the technology supply chain. He then challenged the wafer test community at SW Test to further promote academic participation, "Without academic participation, where is the future knowledge and innovation for needed for wafer test and packaging going to come from?" To help support academic attendance, Dr. Jerry Broz worked closely with the IEEE Foundation in 2010 for the establishment of the William R. Mann Student Travel Grant for eligible student that are IEEE members.



Dr. William Chen
Sr. Advisor, ASE Group
SW Test 2011 Keynote Presentation

The complete version of Dr William Chen's keynote presentation is available for download on the SW Test website (http://www.swtest.org).

On Monday morning, Dr. Jerry Broz, SW Test General Chair, welcomed the attendees to the 21st Annual SW Test Workshop. Dr. Broz reviewed a number of SIA statistics as well as iSuppli information which showed a general rebound in the semiconductor industry. Not surprisingly, the year of semiconductor sector recovery was reflected in the VLSI Research probe card market overview that had been released in May, 2011. The report showed that total probe card revenue was up in 2010, a gain of ~28% (from ~$750M in 2009 to ~$1040M in 2010). The top three revenue generating probe card suppliers remained unchanged – (1) FormFactor; (2) Micronics Japan (MJC), and (3) Japan Electronic Materials (JEM) – and all three companies experienced increased revenues. Of the top three, MJC was reported to have the greatest percentage of growth.

After the Chairman's Welcome to Attendees, the technical program kicked-off and the excellent podium presentations covered various facets of the wafer test process from *Critical Probe Challenges and Cost of Ownership* to *Methods and Strategies for Addressing Extreme Current Challenges.*

Individual highlights from the program included a discussion of new probe technologies for various bump materials by Amy Leong (MicroProbe). Steven Ortiz (Avago Technologies) discussed probe to pad placement error correction for wafer level S-Parameter measurements. Gert Hohenwarter, Ph.D., (Gatewave Northern) outlined that power delivery network analysis and made a case for true 3D simulations. Wafer probing on fine-pitch micro-bumps for 2.5D- and 3D-SICs was presented by Erik Jan Marinissen, Ph.D., (IMEC Research Institute – Belgium). The importance of a WSP (wafer socket probe) for flip chip applications was detailed by Brandon Mair (Texas Instruments). Marc Knox (IBM) discussed his team's efforts for the development of a flexible and efficient chip thermal imaging capability. Technical hurdles experienced for in the electromechanical design of spring pin based WLCSP contact engine and its effect on signal fidelity were addressed by Mike Fredd (Cascade Microtech). Innovations for wafer map and pad stepping to reduce test time were reviewed by Kevin Fredriksen (SPA GmbH – Germany). Takashi Sugiyama (Hitachi Chemical Co. Ltd. – Japan) discussed high density and high speed approach for probe card PCBs. Doron Avidar (Micron – Israel) introduced the concept of "Ghosting" for touchdown reduction using alternate site sharing. Seenew Lai (MPI – Taiwan) detailed the complex challenges associated with development of high bandwidth (>2.5 Gbps) and fine pitch ($<30\ \mu$m) cantilever probe cards.

Overall, the technical program had 32 podium presentations with 55% from suppliers, 18% from semiconductor manufacturers, and 27% collaborative presentations from both manufacturers and suppliers. All the presentations from SW Test 2011 as well as previous workshops (1993 to 2010) are available at the SW Test website (http://www.swtest.org).

The committee recognized the best podium presentations and Rey Rincon (Technical Program Chair) awarded the authors …

- Best Presentations *(awarded jointly)*:
  1) *Identification, Analysis, and Control of High Temperature on Wafer Test Process*

IEEE SW Test Committee 2011
Front: Fred Taber, Jan Martens, Jerry Broz, Ph.D. (General Chair), Rey Rincon (Program Chair), John Caldwell; Middle: Mark Ojeda, Amy Leong, Roy Swart, Tatsuo Inoue, Darren James, Patrick Mui; Back: Boyd Daniels, Michael Huebner, Ph.D., Gunther Boehm.

Marcel BLEYL and Jan MARTENS (NXP Semiconductors – Germany)
Darren JAMES (Rudolph Technologies – USA)

2) *Contact Formation in Wafer Probing: Fritting, Breakdown, Damage and Conduction*
Jörg SEEKAMP and Gunther BöHM (Feinmetall – Germany)
Jan MARTENS (NXP Semiconductors)
Marcel MITTAG (Fraunhofer Institut für Werkstoffmechanik – Germany)

- Best Data Presented
  *Use of Harsh Wafer Probing to Evaluate Various Bond Pad Structures*
  Stevan HUNTER, Troy RUUD, Bryce RASMUSSEN and Vail MCBRIDE (ON Semiconductor – USA)
- Most "Inspirational" Presentation
  *Novel Carbonaceous Film with High Electrical Conductivity and Super High Hardness for Semiconductor Test Probes*
  Teruyuki KITAGAWA, Ph.D. (Nomura Plating Co., Ltd. – Japan)
- Best Presentation, Tutorial in Nature *(awarded jointly)*

1) *Electromagnetic Analysis and Verification of Probe Card Performance for First Pass System Success*
Cristian GOZZI (TechnoProbe – Italy)

2) *Key Design Parameters to Maximize Probe Current Carrying Capability*
January KISTER (MicroProbe – USA)

After a multi-year hiatus, the infamous "*Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch*" was awarded this year; however, the committee decided to protect the guilty and will keep "*what happens at SW Test AT SW Test*".

During the SW Test Technology EXPO, 35 full size exhibits showcased products for the wafer sort industry and the associated critical infrastructure. The exhibitors represented probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers. SW Test 2011 also had five Corporate Supporters - Acme Technology, Advanced Probing Systems, International Test Solutions, JEM America, Micronics Japan (MJC), and T.I.P.S. Messtechnik.

The 21st Annual IEEE SW Test Workshop and Tech EXPO will be held on *June 12 to 15, 2011* at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for the technical program and exhibitor registration for the Tech EXPO are already open.