2.5D and 3D TSV Products

Phil Marcoux
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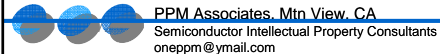
May 2011



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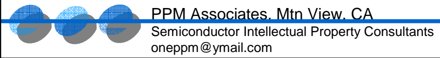
Outline

- Why 2.5D and 3D Products?
- Why TSVs?
- 2.5D/3D Product Examples



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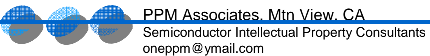
Javier De La Gruz, eSilicon



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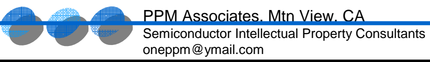
Why 3D and 2.5D?

To Meet the 3 “Givens” of Semiconductor Packaging

- Smaller
  - We are back to thinking of apartment buildings vs. suburban sprawl. (remember MCMs?)
- Faster
  - Shorter signal distances = less obstacles.
- Cheaper
  - Stuff more into one rather than several packages.
  - Better yields from chip partitioning



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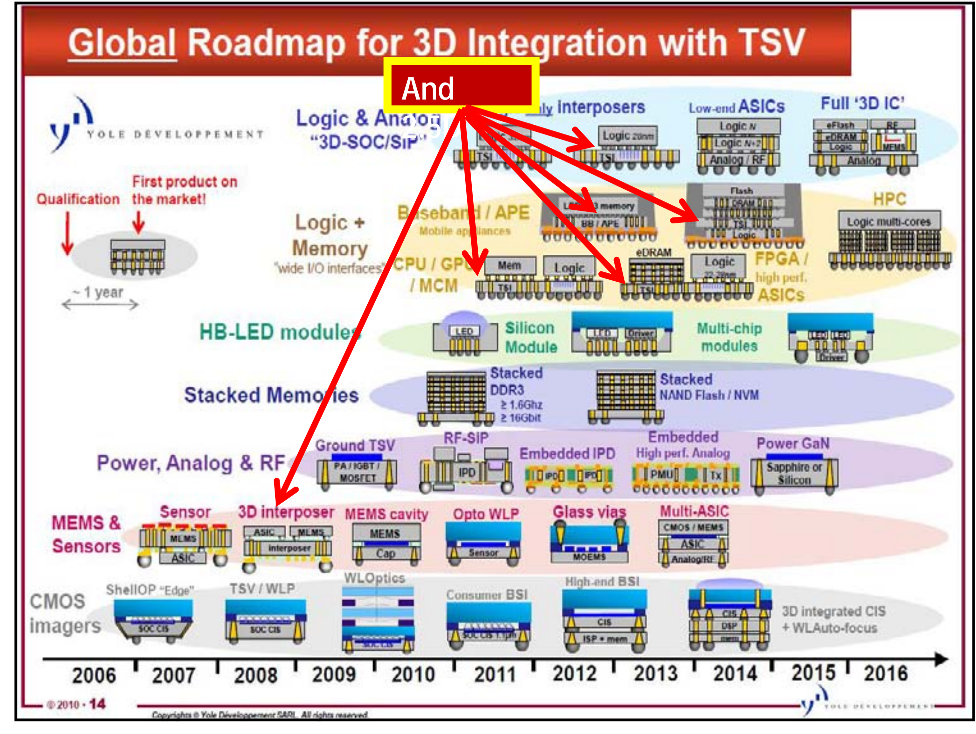
Global Roadmap for 3D Integration with TSV
And
YOLE DEVELOPPEMENT
Logic & Analog "3D-SOC/SiP"
Low-end ASICs
Full '3D IC'
Qualification
First product on the market!
~ 1 year
Logic + Memory
"wide I/O interfaces"
Baseband / APE
CPU / GPU / MCM
HPC
FPGA / high perf. ASICs
HB-LED modules
Silicon Module
Multi-chip modules
Stacked Memories
Stacked DDR3
Stacked NAND Flash / NVM
Power, Analog & RF
Ground TSV
RF-SIP
Embedded IPD
Embedded High perf. Analog
Power GaN
MEMS & Sensors
Sensor
3D interposer
MEMS cavity
Opto WLP
Glass vias
Multi-ASIC
CMOS imagers
ShellOP "Edge"
TSV / WLP
WLOptics
Consumer BSI
High-end BSI
3D integrated CIS + WLAuto-focus
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
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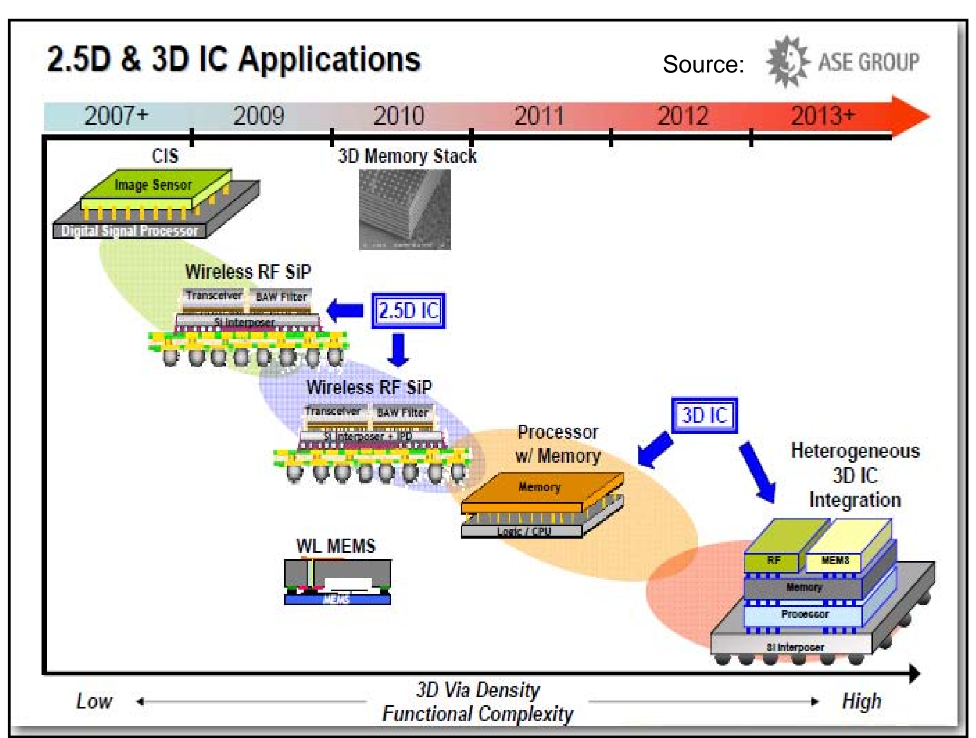
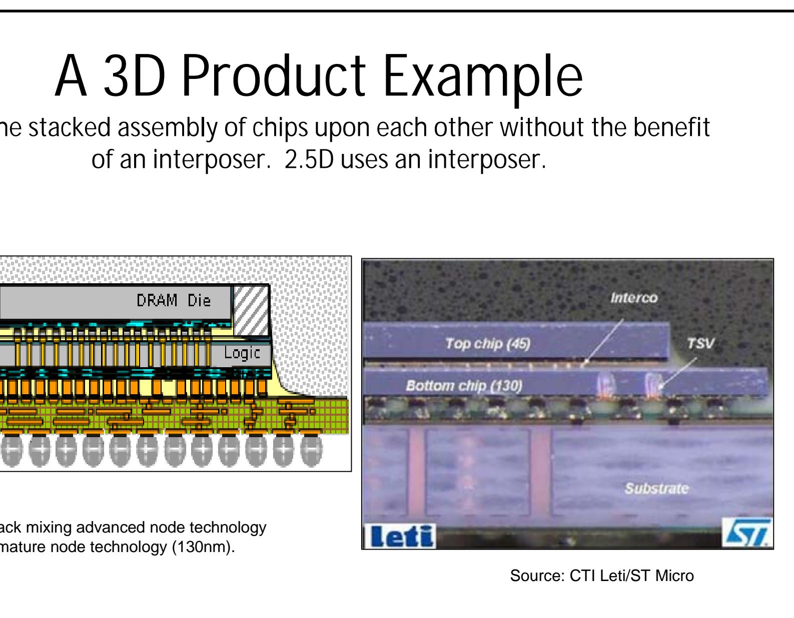

2.5D & 3D IC Applications
Source: ASE GROUP
2007+
2009
2010
2011
2012
2013+
CIS
Image Sensor
Digital Signal Processor
3D Memory Stack
Wireless RF SiP
Transceiver
BAW Filter
Si Interposer
2.5D IC
Wireless RF SiP
Si Interposer + IPD
Processor w/ Memory
Memory
Logic / CPU
3D IC
Heterogeneous 3D IC Integration
RF
MEMS
Memory
Processor
Si Interposer
WL MEMS
MEMS
Low
3D Via Density
Functional Complexity
High

A 3D Product Example

3D is the stacked assembly of chips upon each other without the benefit of an interposer. 2.5D uses an interposer.



A two-die stack mixing advanced node technology (45nm) with mature node technology (130nm).

Source: CTI Leti/ST Micro

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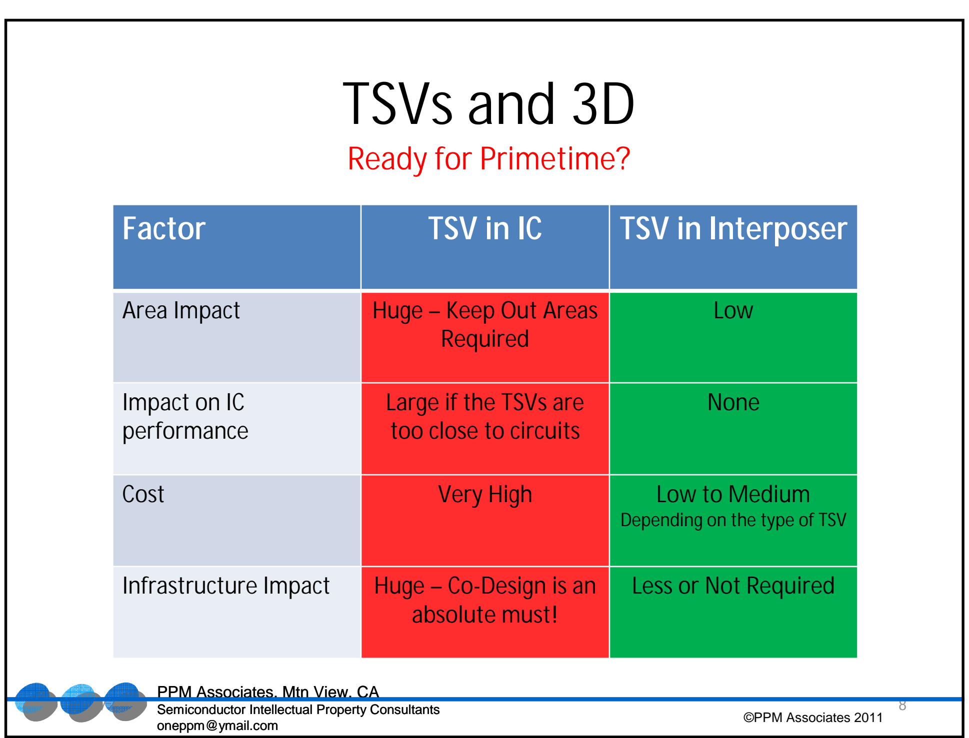

TSVs and 3D

Ready for Primetime?

Factor	TSV in IC	TSV in Interposer
Area Impact	Huge – Keep Out Areas Required	Low
Impact on IC performance	Large if the TSVs are too close to circuits	None
Cost	Very High	Low to Medium Depending on the type of TSV
Infrastructure Impact	Huge – Co-Design is an absolute must!	Less or Not Required

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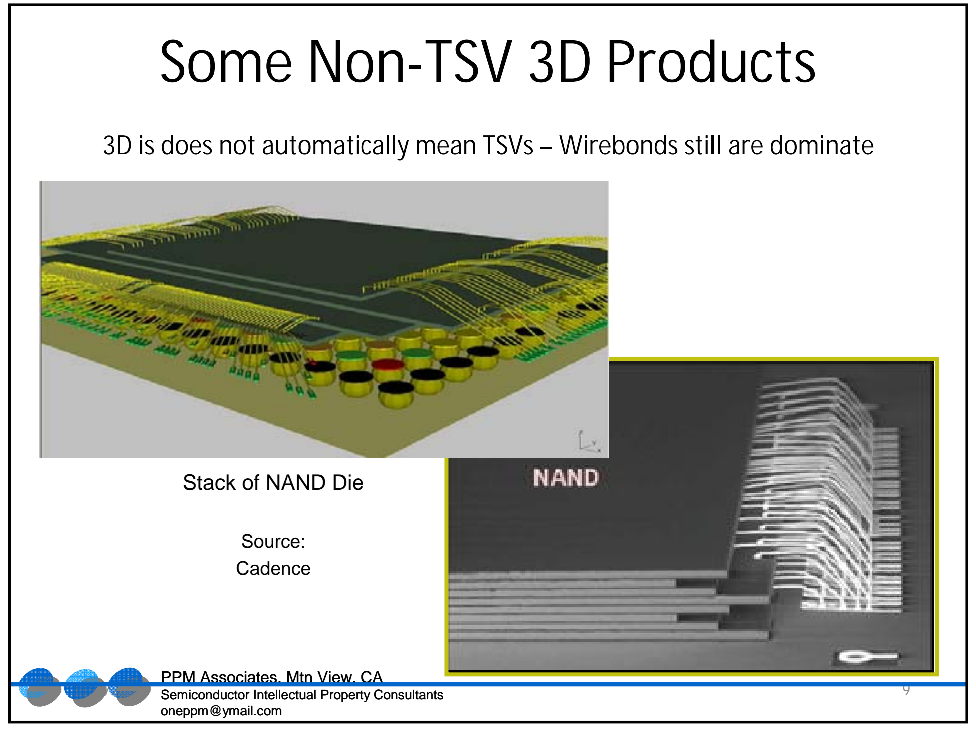
Some Non-TSV 3D Products
3D is does not automatically mean TSVs – Wirebonds still are dominate
NAND
Stack of NAND Die
Source:
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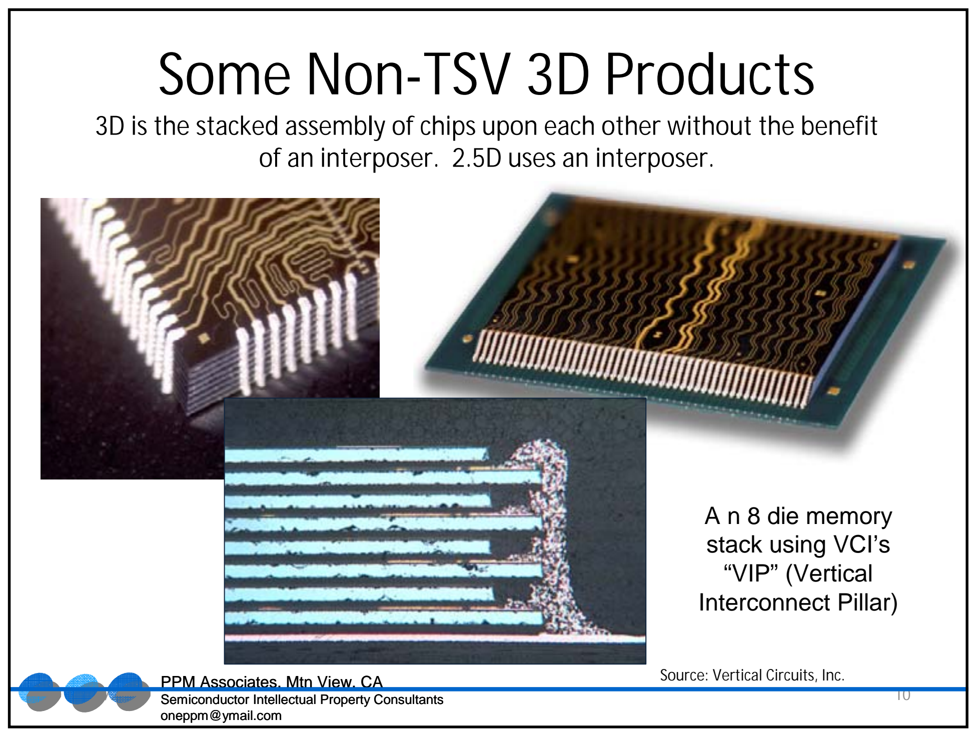
Some Non-TSV 3D Products
3D is the stacked assembly of chips upon each other without the benefit of an interposer. 2.5D uses an interposer.
A n 8 die memory stack using VCI's "VIP" (Vertical Interconnect Pillar)
Source: Vertical Circuits, Inc.
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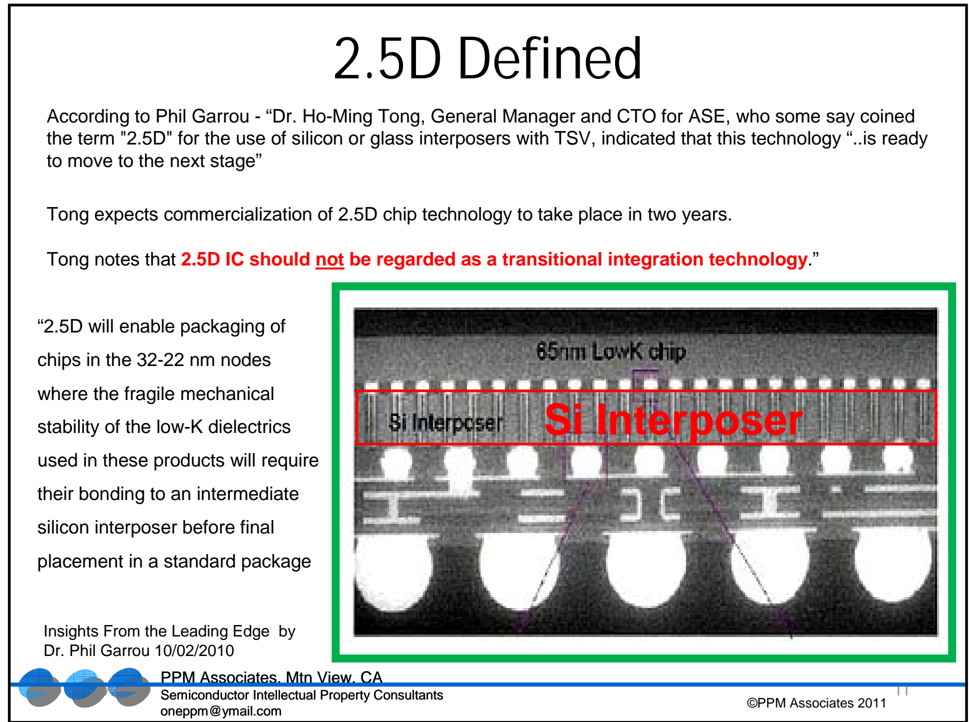
2.5D Defined
According to Phil Garrou - "Dr. Ho-Ming Tong, General Manager and CTO for ASE, who some say coined the term "2.5D" for the use of silicon or glass interposers with TSV, indicated that this technology "..is ready to move to the next stage"
Tong expects commercialization of 2.5D chip technology to take place in two years.
Tong notes that 2.5D IC should not be regarded as a transitional integration technology."
"2.5D will enable packaging of chips in the 32-22 nm nodes where the fragile mechanical stability of the low-K dielectrics used in these products will require their bonding to an intermediate silicon interposer before final placement in a standard package
Insights From the Leading Edge by Dr. Phil Garrou 10/02/2010
65nm LowK chip
Si Interposer
Si Interposer
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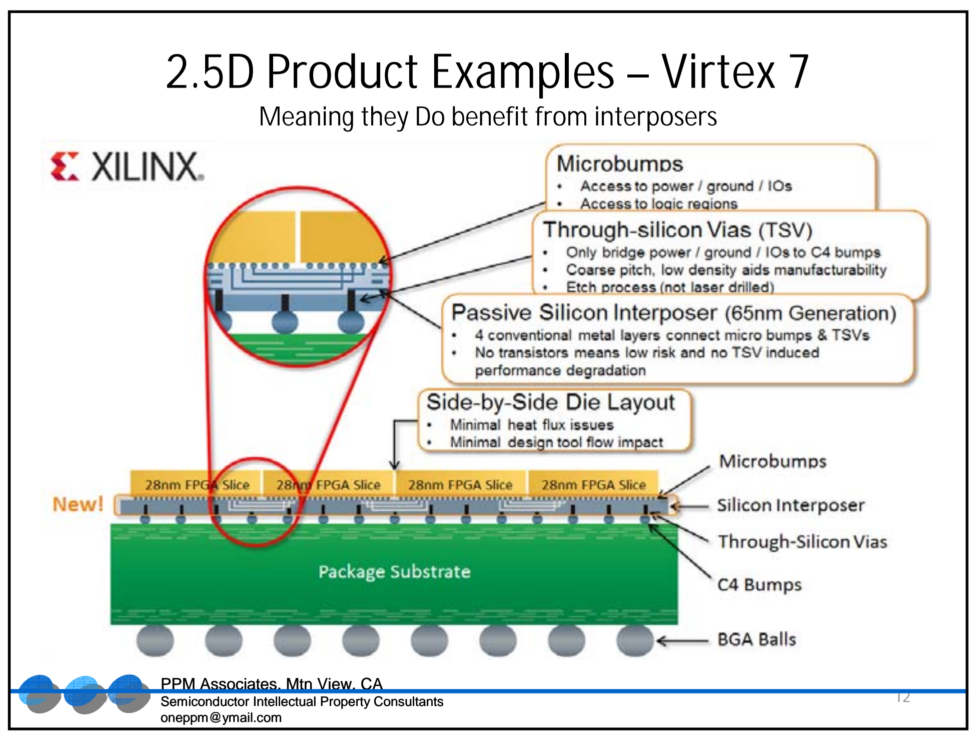
2.5D Product Examples – Virtex 7
Meaning they Do benefit from interposers
XILINX.
Microbumps
Access to power / ground / IOs
Access to logic regions
Through-silicon Vias (TSV)
Only bridge power / ground / IOs to C4 bumps
Coarse pitch, low density aids manufacturability
Etch process (not laser drilled)
Passive Silicon Interposer (65nm Generation)
4 conventional metal layers connect micro bumps & TSVs
No transistors means low risk and no TSV induced performance degradation
Side-by-Side Die Layout
Minimal heat flux issues
Minimal design tool flow impact
Microbumps
28nm FPGA Slice
28nm FPGA Slice
28nm FPGA Slice
28nm FPGA Slice
New!
Silicon Interposer
Through-Silicon Vias
Package Substrate
C4 Bumps
BGA Balls
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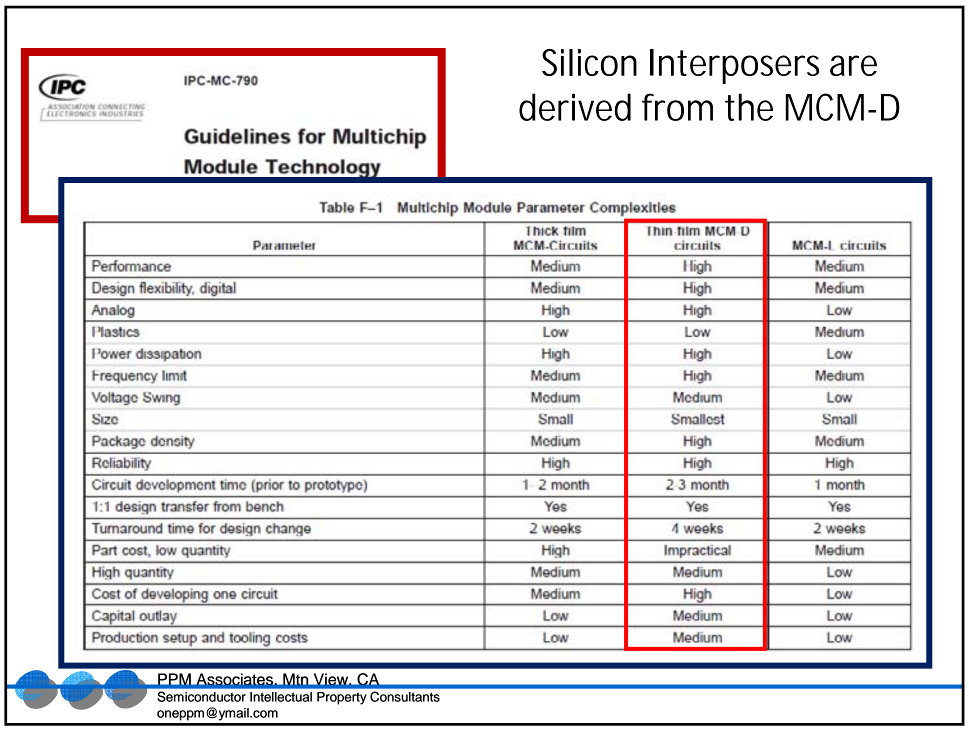
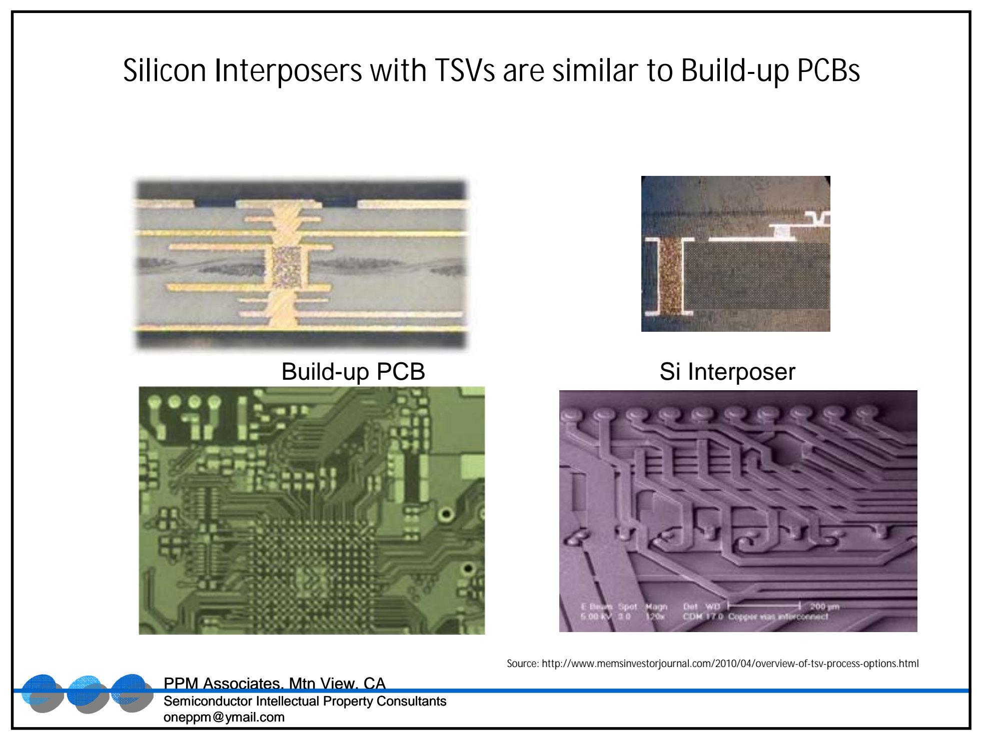
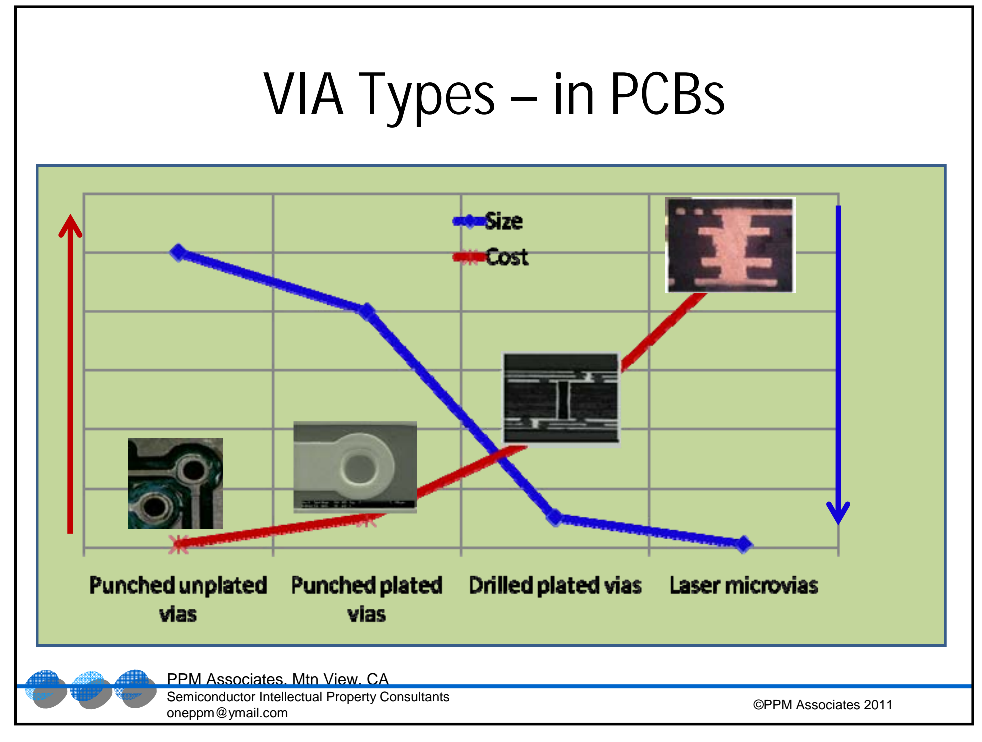


Table F–1 Multichip Module Parameter Complexities

Parameter	Thick film MCM-Circuits	Thin film MCM-D circuits	MCM-L circuits
Performance	Medium	High	Medium
Design flexibility, digital	Medium	High	Medium
Analog	High	High	Low
Plastics	Low	Low	Medium
Power dissipation	High	High	Low
Frequency limit	Medium	High	Medium
Voltage Swing	Medium	Medium	Low
Size	Small	Smallest	Small
Package density	Medium	High	Medium
Reliability	High	High	High
Circuit development time (prior to prototype)	1-2 month	2-3 month	1 month
1:1 design transfer from bench	Yes	Yes	Yes
Turnaround time for design change	2 weeks	4 weeks	2 weeks
Part cost, low quantity	High	Impractical	Medium
High quantity	Medium	Medium	Low
Cost of developing one circuit	Medium	High	Low
Capital outlay	Low	Medium	Low
Production setup and tooling costs	Low	Medium	Low




VIA Types – in PCBs
Size
Cost
Punched unplated vias
Punched plated vias
Drilled plated vias
Laser microvias
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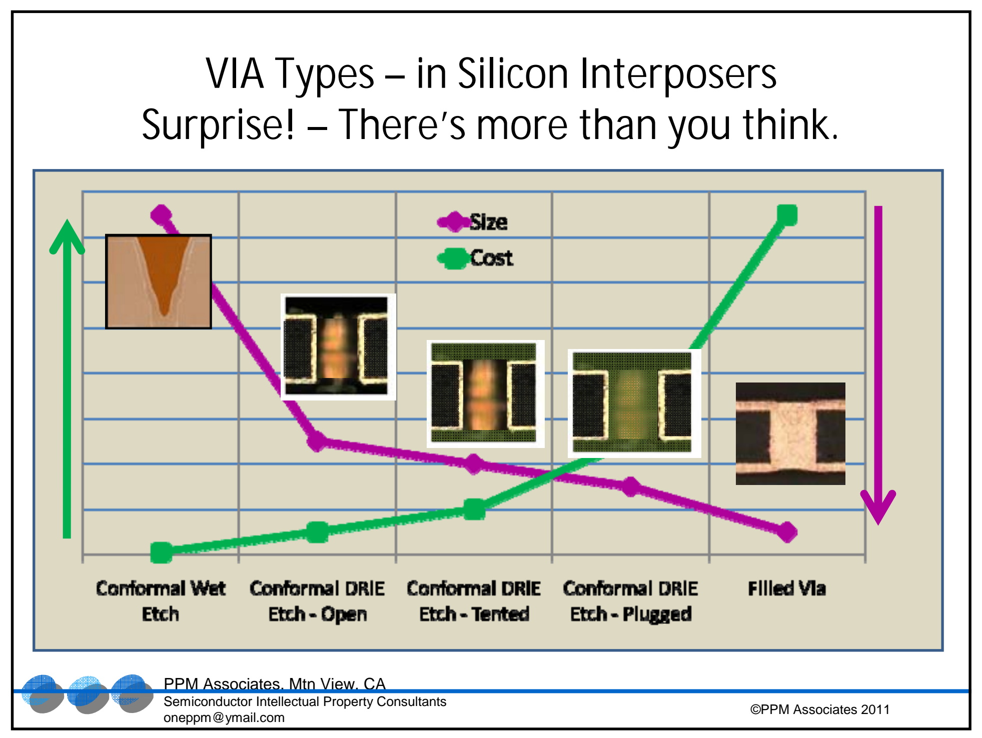
VIA Types – in Silicon Interposers
Surprise! – There's more than you think.
Size
Cost
Conformal Wet Etch
Conformal DRIE Etch - Open
Conformal DRIE Etch - Tented
Conformal DRIE Etch - Plugged
Filled Via
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VIA Types – for Silicon Interposers

Conformal Wet Etch – Large Area, Difficult to Control, Least Expensive

Conformal DRIE Etch – Smaller Area, Controlled Etch, Slightly More Expensive

Conformal Tented– Small Area, Difficult to Control, More Expensive due to polymer cost

Conformal Plugged– Small Area, Challenge to Plug, More Expensive due to polymer and plug cost

Filled Via– Small Area, Plating is long and difficult to Control, Higher Stress, Most Expensive

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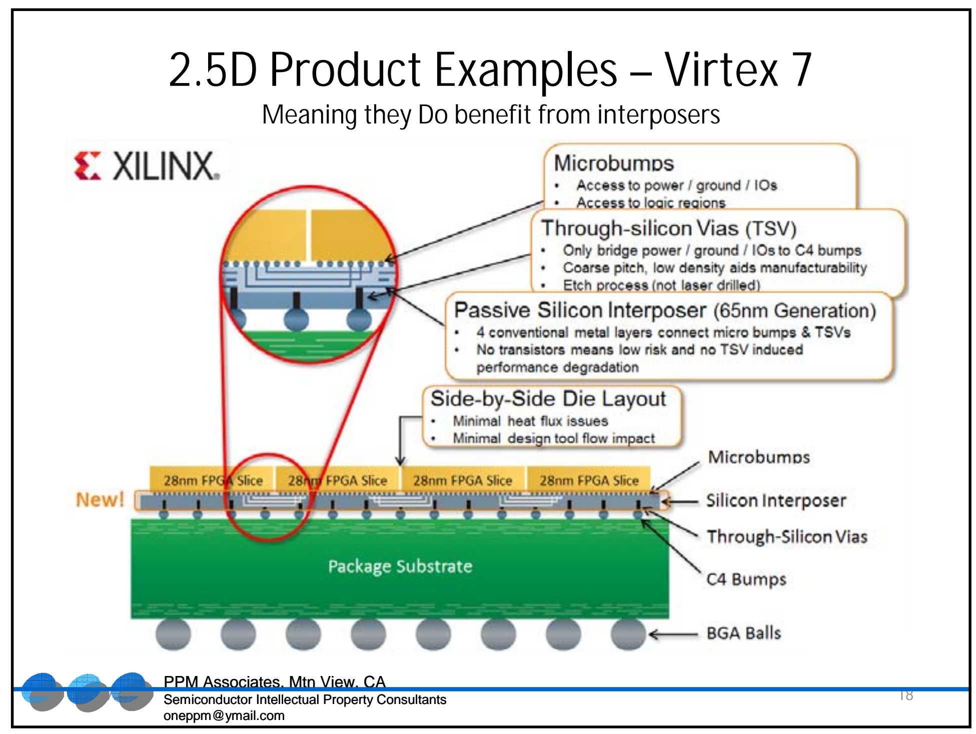
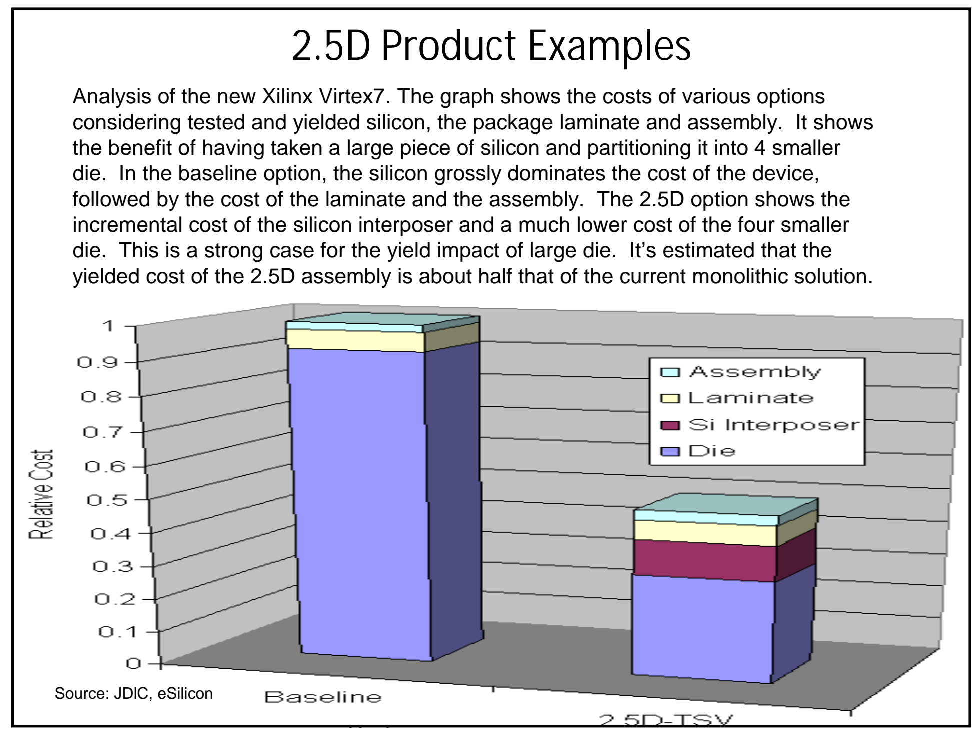
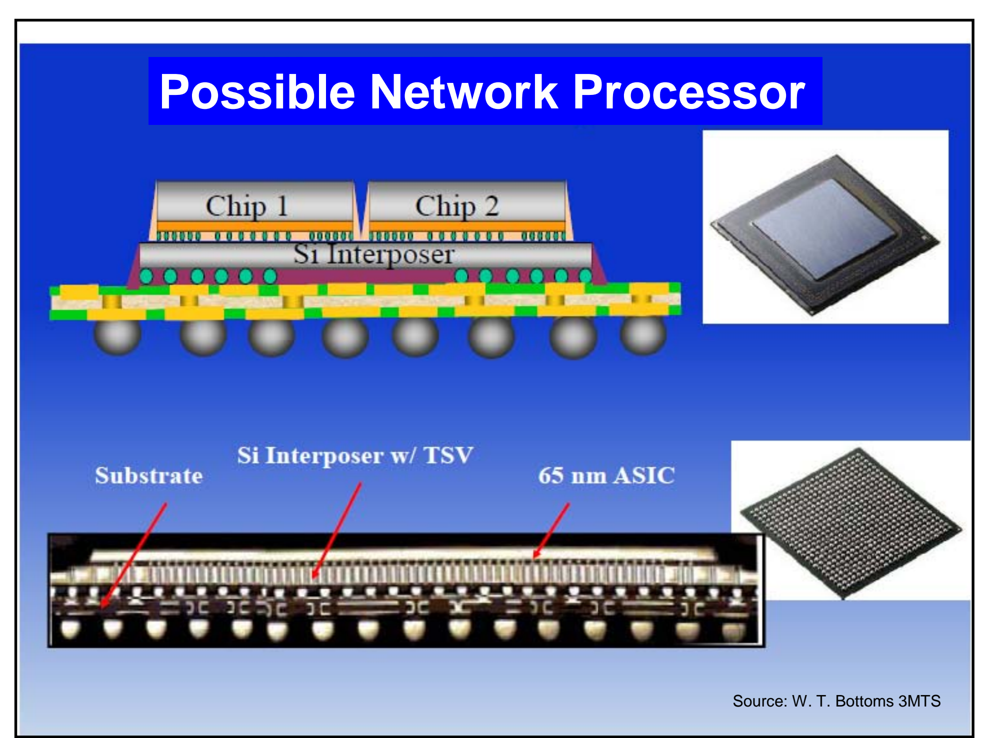
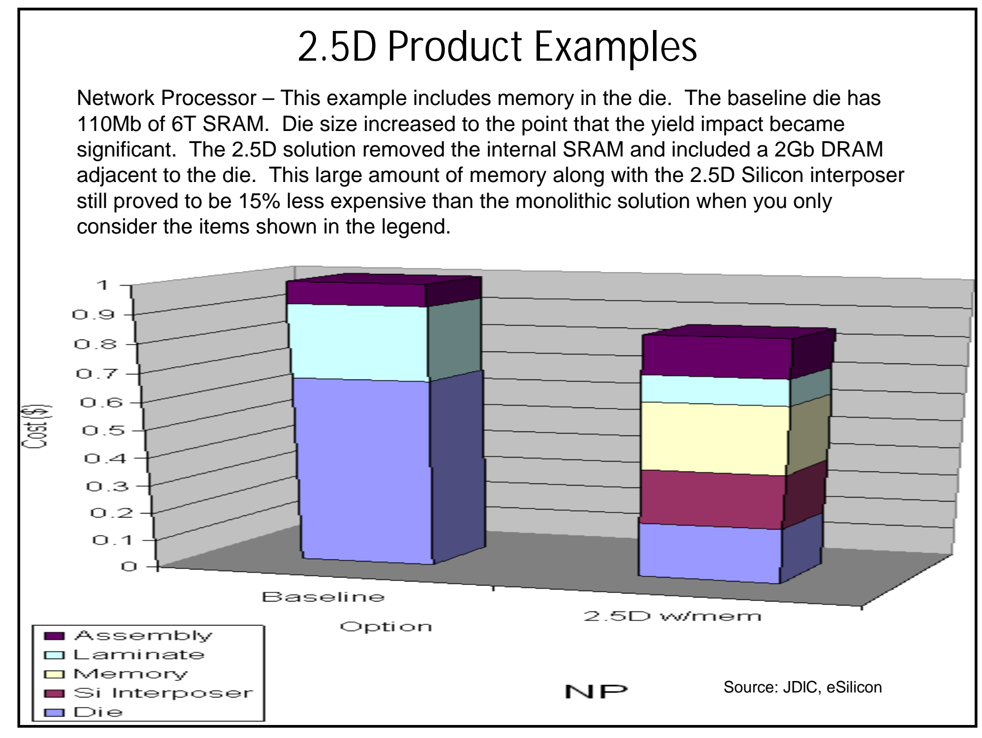



2.5D Product Examples
Analysis of the new Xilinx Virtex7. The graph shows the costs of various options considering tested and yielded silicon, the package laminate and assembly. It shows the benefit of having taken a large piece of silicon and partitioning it into 4 smaller die. In the baseline option, the silicon grossly dominates the cost of the device, followed by the cost of the laminate and the assembly. The 2.5D option shows the incremental cost of the silicon interposer and a much lower cost of the four smaller die. This is a strong case for the yield impact of large die. It's estimated that the yielded cost of the 2.5D assembly is about half that of the current monolithic solution.
Relative Cost
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Assembly
Laminate
Si Interposer
Die
Baseline
2.5D-TSV
Source: JDIC, eSilicon


Possible Network Processor
Chip 1
Chip 2
Si Interposer
Substrate
Si Interposer w/ TSV
65 nm ASIC
Source: W. T. Bottoms 3MTS

2.5D Product Examples

Network Processor – This example includes memory in the die. The baseline die has 110Mb of 6T SRAM. Die size increased to the point that the yield impact became significant. The 2.5D solution removed the internal SRAM and included a 2Gb DRAM adjacent to the die. This large amount of memory along with the 2.5D Silicon interposer still proved to be 15% less expensive than the monolithic solution when you only consider the items shown in the legend.



2.5D Interposer Specs

	Today	In ~ 5 years	Possibly > 5 years
Substrate Mtl.	Silicon	Silicon	Silicon or Glass
Size	200mm	300mm	> 300mm
Thickness	300 – 400um	300 – 400um	200 – 300um
Via Diameter	60 to 80um	40 to 60um	<40um
Aspect Ratios	5 to 1	Range of 5 - 10 to 1	Range of 5 - 10 to 1
Plating	Conformal or Filled Cu	Conformal or Filled Cu	Conformal or Filled Cu
Insulator	Oxide or Poly	Oxide or Poly	Oxide or Poly or NONE
RDLs	1 to 2	2 to 3	>3

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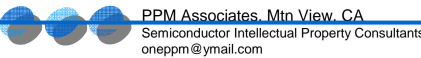
There's Too Many Flavors and Options!

In every transition in technology we suffer a period of
Too Many Options

- Wirebond
- FlipChip – Solder
- Flipchip – Conductive Epoxy
- Flipchip – Copper Pillar
- Wraparound WLP
- Stud Bumping
- Conformal TSV
- Filled TSV



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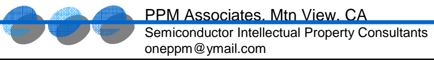
Conclusion

- 3D and 2.5D is an exciting extension to the IC packaging world.
- The roots are with the MCMs of the early '90s
- Which means demons like lack of KGD still lurk
- Too many options exist and the infrastructure still needs growth
- Interposers (2.5D) aren't just a stepping stone to 3D



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