A Comparison of Low Cost Interposer Technologies

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Terry (Teckgyu) Kang & Abraham Yee

Advanced Technology Group

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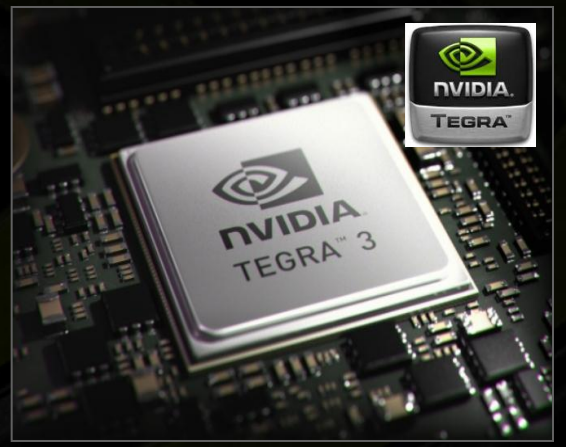
NVIDIA Products and Interposer Drivers

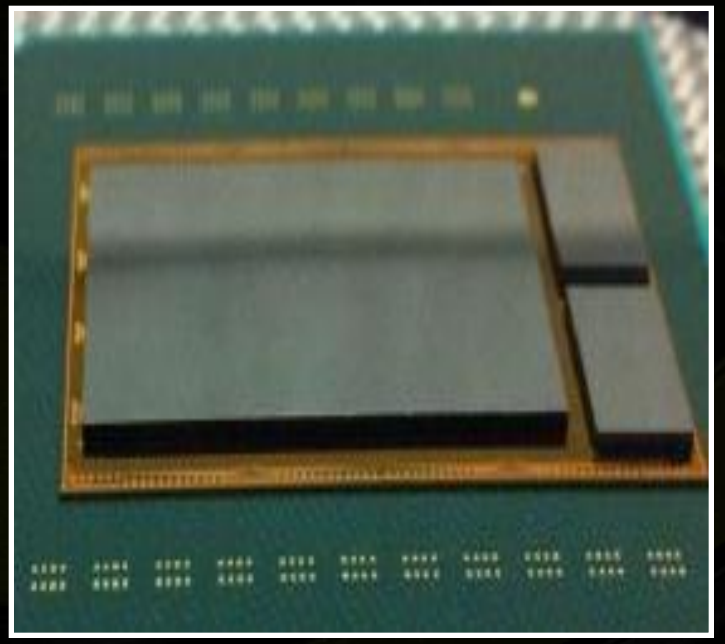
- NVIDIA Products
  - Application processor for mobile phones and tablet PCs (Tegra)
  - Gaming GPU for laptop and desktop PCs (GeForce)
  - High-end digital content creation for workstation (Tesla/Quadro/Volta)



- Interposer Drivers
  - Higher electrical performance
  - Smaller form factor

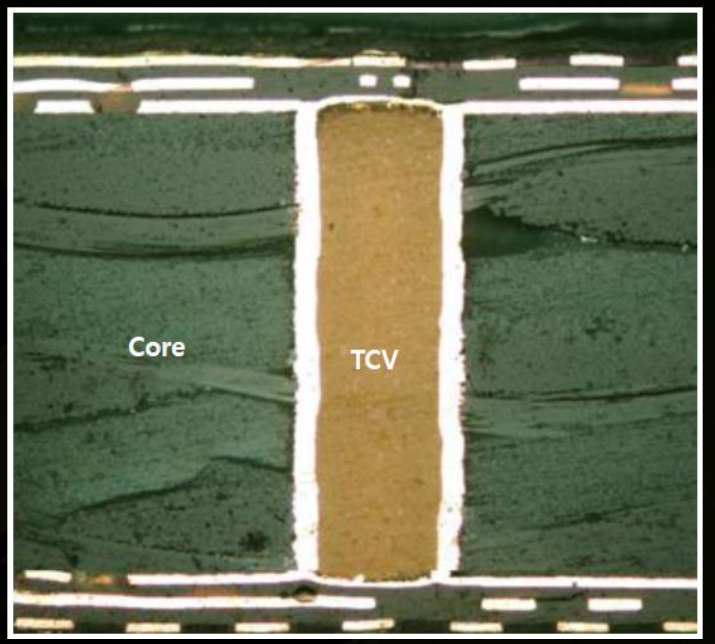
Low Cost Interposer Approaches

Si Interposer



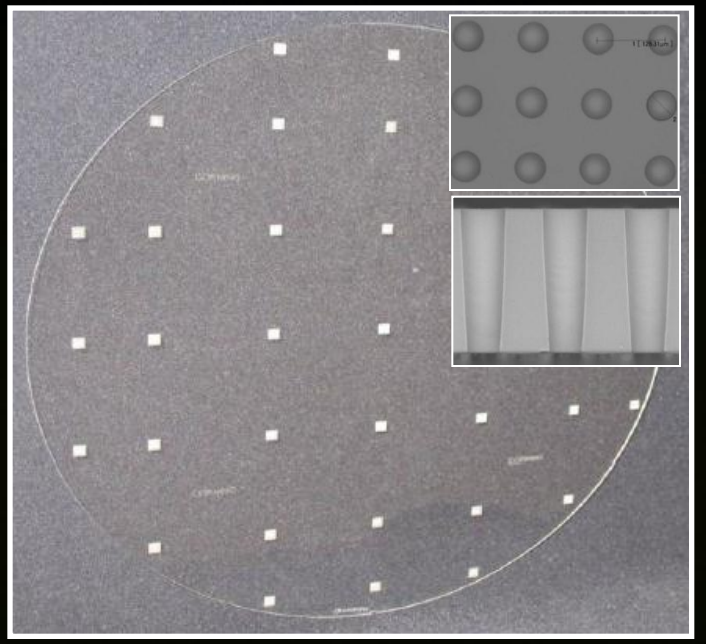
Source: Yole/Global Foundries 2012

Organic Interposer



Source: SEMCO

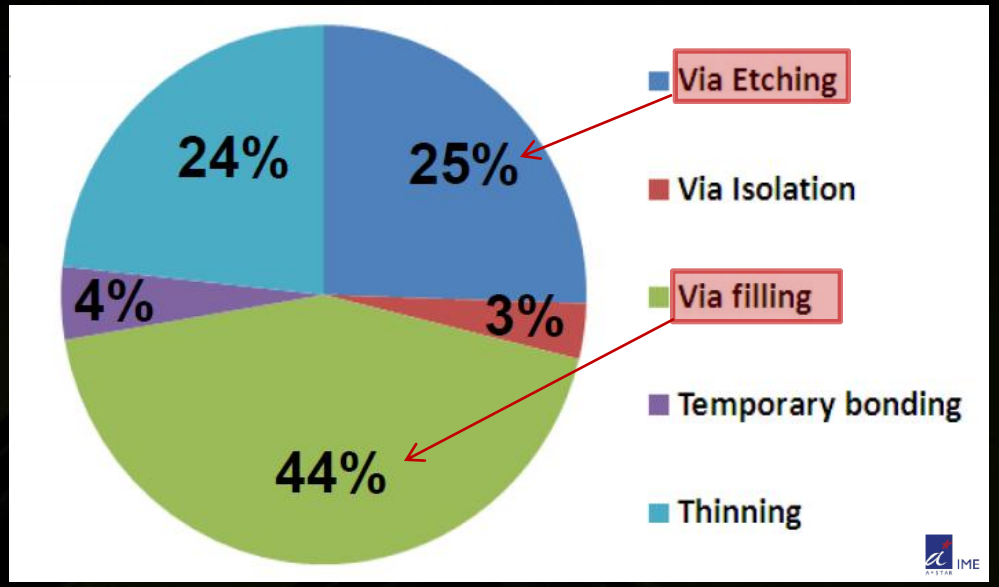
Glass Interposer



Source: Corning (2013 IMAPS)

Si Interposer Process Cost Analysis

Cost Distribution of TSV Processes



Source: IME

- Via etching and filling (69%) processes are major cost factor
- TSV formation is the most expensive cost for interposer fabrication
- Thinner interposer reduces process cost

Assembly Flows for Thinner Interposer

Chip to Chip

Process Thin I/P or Die

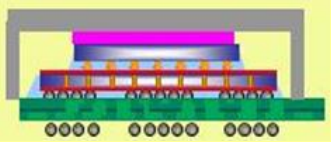
Chip/Wafer Damage

Top Die Attach

uBump Joining Defects

Underfill & Cure

Finish Assembly

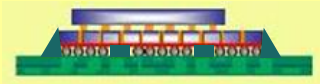


Chip to Sub

Attach I/P & UF on Sub

C4 Bump Joining Defects

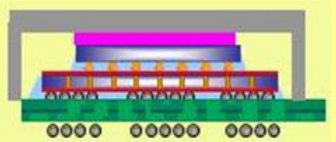
Top Die Attach



uBump Joining Defects

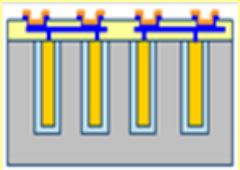
Underfill & Cure

Finish Assembly

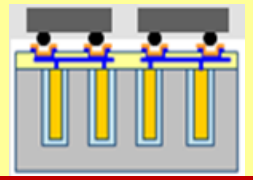


Chip to Wafer

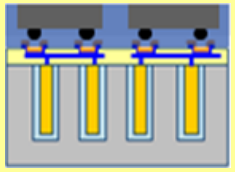
I/P Wafer with full thickness



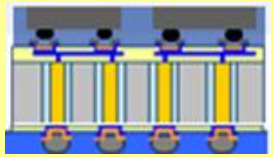
Top Die Attach



Mold & Top Die Exposure



C4 Bump & Singulation



Thin Si Interposer Summary

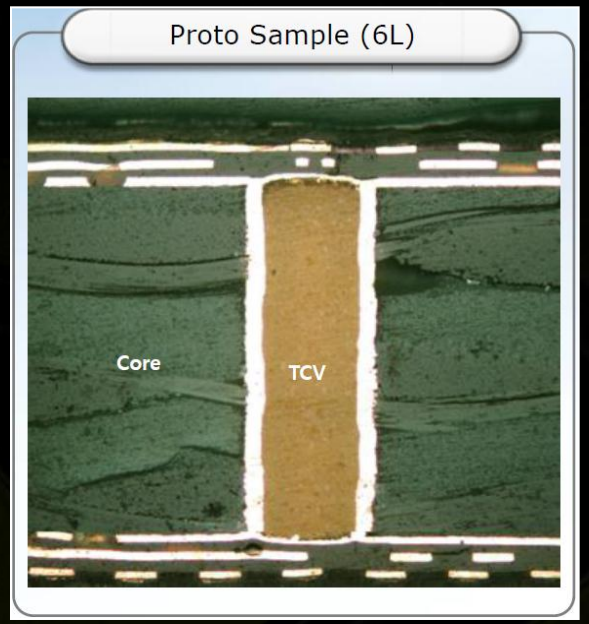
Advantages

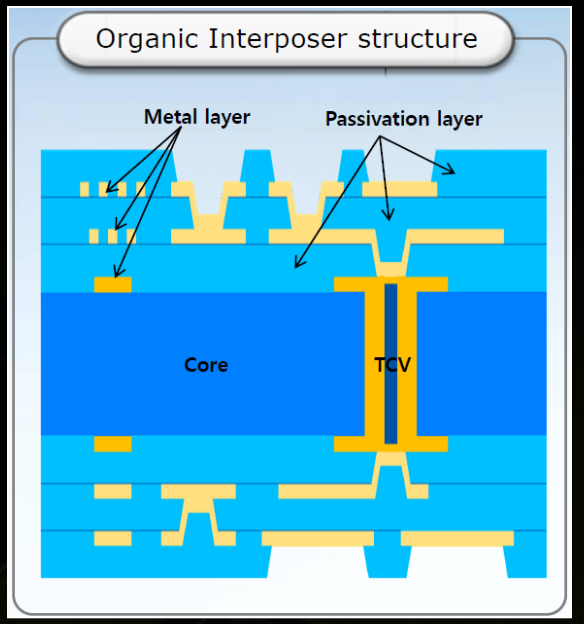
- Reduce interposer process cost
- No warpage concern during top die attach (C2W)
- Tighter design rule
- Better electrical performance

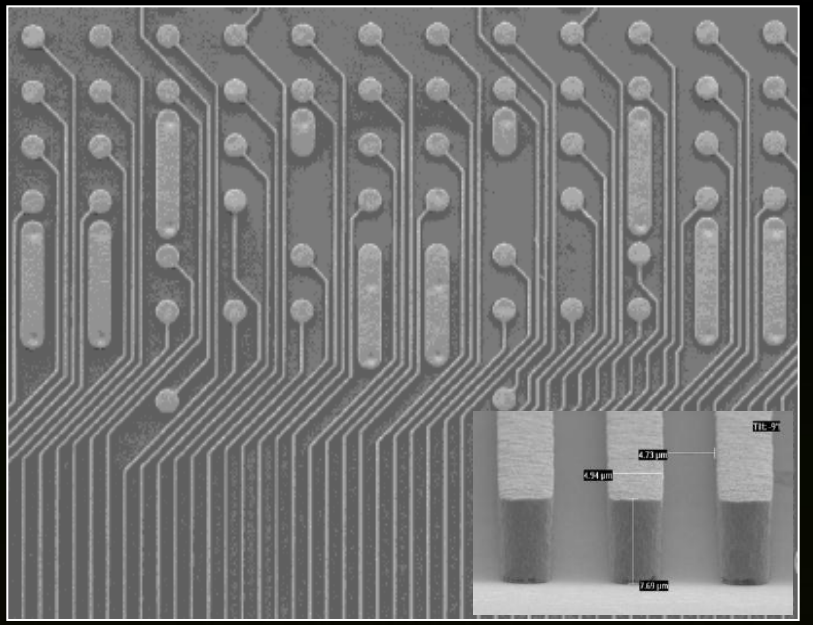
Challenges

- uBump joint reliability
- Higher interposer thickness variation
- New investment for C2W process equipment (OSATs)

Organic Interposer







Source: SEMCO (2012 MEPTEC)

- Use low CTE and high modulus organic materials
- Mechanically symmetric structure
- Offer finer design rule than conventional substrate
- Apply Si fab equipment for manufacturing

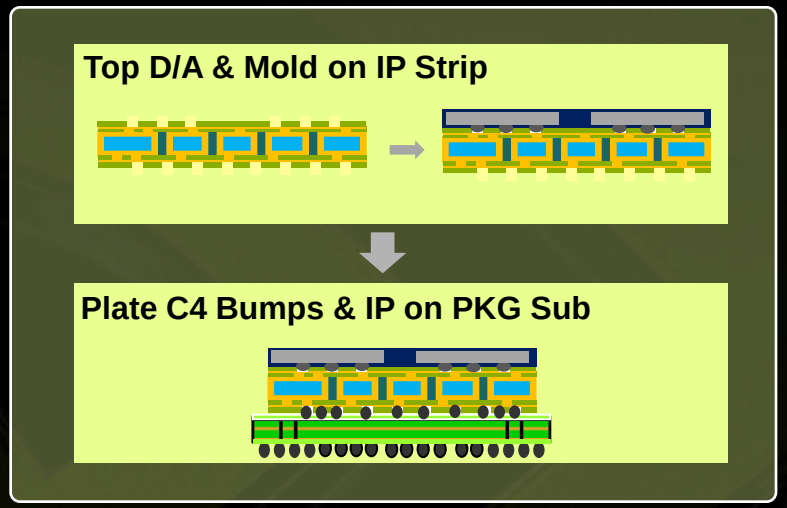
Si vs. Organic Interposer

Si Interposer		Organic Interposer
Wafer	Core Substrate Type	Panel
Silicon (3ppm/K) 100㎛ ※ Handling trouble	Core Material (CTE) Core Thickness	Organic (4ppm/K) 60~450㎛
1㎛	Line Width	3㎛ @2013
Asymmetry (n+1)	Structure (Top+Bottom)	Symmetry (n+n) ※ Warpage Controlable
Dry Etch	Core Through Hole	Laser Via / Mechanical Drill
PECVD + PVD+Cu Plating (Semiconductor Process)	Through Hole Filling	E'less Cu+Cu Plating (PCB Process)
Wafer Thinning	Total Thickness Control	Core Thickness selected
801ea/m^2 (12 inch)	Net Die (25 x 25mm^2)	1260ea/m^2 (200 x 250mm^2)

Source: SEMCO (2012 MEPTEC)

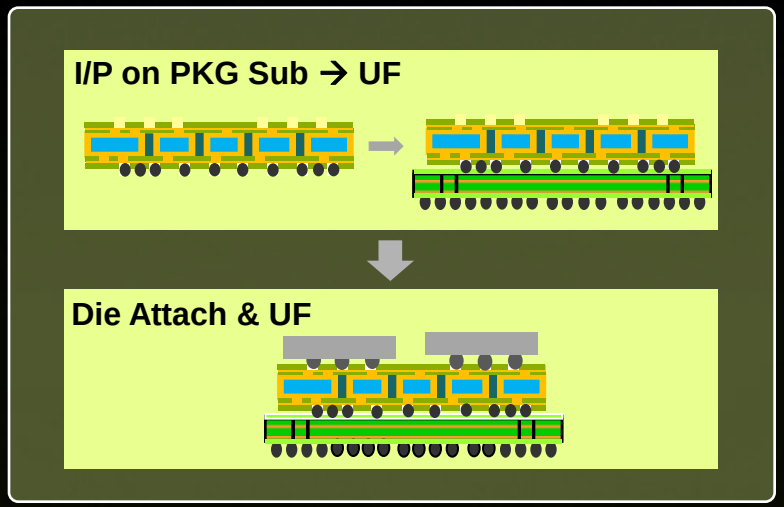
Organic Interposer Assembly Flow

Chip to Strip



- Similar to C2W process flow
- Die attach and mold process
- Thermal compression bonding for D/A

I/P to PKG Substrate



- C2S process flow
- Die attach and mold process
- Mass reflow for D/A

Organic Interposer Summary

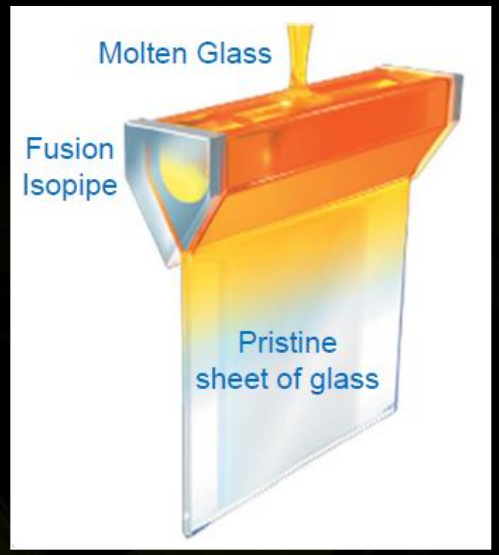
Advantages

- Use low cost process and materials
- Process rectangular panel format
- Utilize existing supply chain
- Extended to interposer embedded substrate
- Potentially lower cost

Challenges

- Looser design rule than Si interposer
- Innovation needed to create robust tight L/S
- Manufacturing and reliability challenges
- Limited suppliers

Glass Interposer

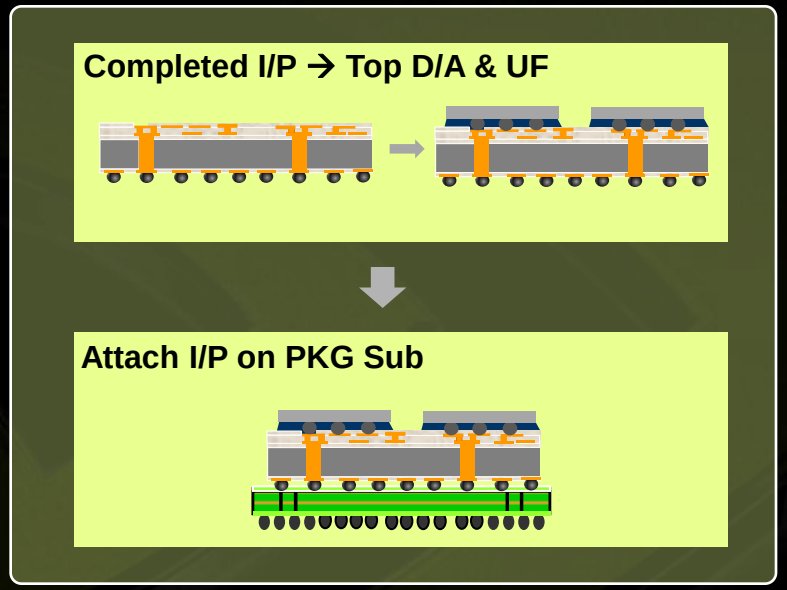


Source: Corning (2013 IMAPS)

- Formed by fusion process
- Applicable for roll to roll process with Cu via filling process
- Material properties can be tailored (CTE: 3~9 ppm/C)
- Via formation processes: Laser or Wet etch
- Similar assembly process steps to Si interposer

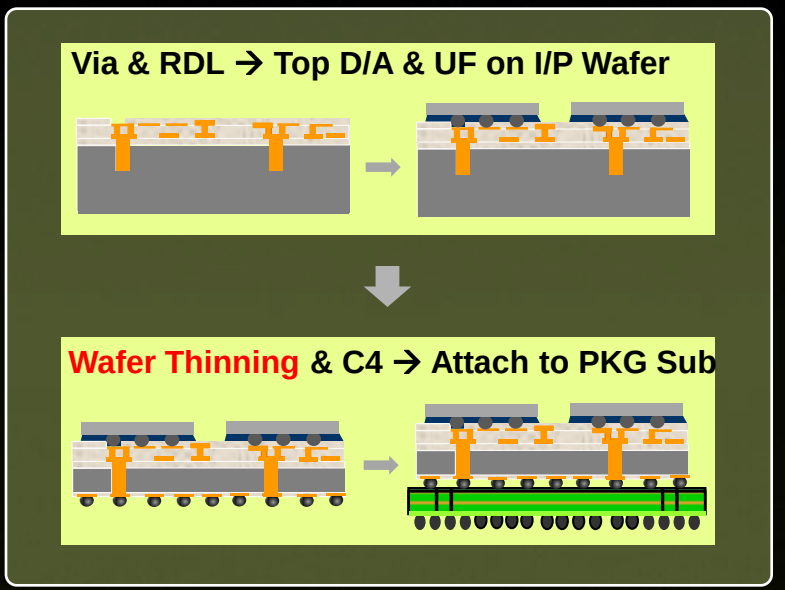
Glass Interposer Assembly Process

Chip to Singulated I/P



- Similar to C2C process flow
- Attach top die on singulated I/P
- Require T/C bonding for thin I/P

Chip to Wafer



- Similar to C2W process flow
- Mass reflow for die attach
- Challenge for glass wafer thinning

Glass Interposer Summary

Advantages

- Use low cost material
- Process rectangular panel format
- Potentially applicable for roll to roll process
- Material properties can be tailored

Challenges

- Supply chain
- Looser design rule than Si interposer
- Cost effective via formation
- Warpage control for large panel

Low Cost Interposer Comparison

	Thin Si Interposer	Organic Interposer	Glass Interposer
Process Format	**Wafer**	**Panel**	**Panel**
Design Rule (L/S & Via Diameter)	**Very Tight**	**Loose**	**L/S: Under development** **Via: Loose**
Assembly Process	**C2W**	**C2SI**	**C2GI**
Supply Chain	**Si Fab or** **Si Fab → OSAT**	**Substrate → OSAT**	**Not defined yet**

Summary

- Current interposer cost is too high
- The cost should be reduced to enable for high volume production
- We need innovation from the industry (Foundries, OSATs, Material/Equipment Suppliers) to implement 2.5D for HVP