Design and Analysis of Chiplet Interfaces for Heterogenous Systems

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1

Headlines with Chiplets

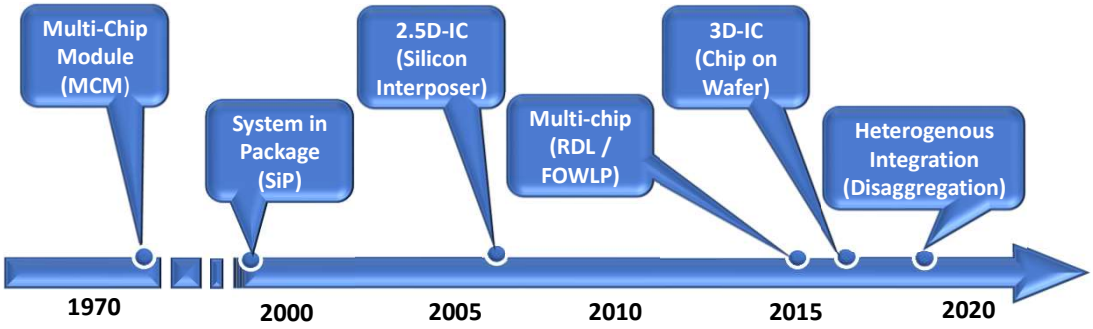
- Chiplets: The new era begins
- To keep pace with Moore's Law, chipmakers turn to 'Chiplets'
- How "Chiplets" may help the future of semiconductor technology
- *Chiplets - Taking SoC design where no monolithic IC has gone before*
- **Chiplet ecosystem slowly picks up steam**
- The good and bad of chiplets
- Chiplets are both solution to and symptom of a larger problem
- ***The benefits of chiplets can't be separated from the difficulties driving their use***

2

2

History of Multi-Chiplet Design

- Chiplets would enable an ASIC partitioned into multiple dies and then interconnected together within a package to make an integrated system



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3

Recent High-Performance Chips

- Heterogeneous integrations on silicon substrates (Chip-on-Wafer-on-Substrate (CoWoS)) or *Embedded Multi-Die Interconnect Bridge (EMIB)*
- Heterogeneous integrations on organic substrates using finer metal line width and spacing (say 5 µm) at high yield
  - Intel Agilex Partitioned FPGA
  - Xilinx *Virtex* Partitioned FPGA
  - AMD *Fiji GPU & HBM* integration
  - Cisco's *ASIC & HBM* integration

IEEE EPS Heterogeneous Integration Roadmap. http://eps.ieee.org/hir 4

4

Outline

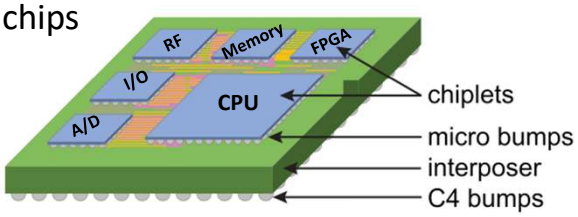
- Introduction
- Chiplets
  - Advantages and disadvantages
- Types of Interposers
  - Channel: signal integrity
  - Power distribution network: power integrity
- Chiplet Interface
  - I/O characteristics
  - Source-synchronous parallel interface
- Supply noise
  - Jitter analysis
- Conclusions

5

5

Chiplets for Heterogenous Systems

- Partitioning a big die into multiple smaller chiplets, then using advanced packaging technology to achieve performance as close as possible to monolithic integration
- Heterogeneous integration uses packaging technology to integrate dissimilar chips
  - Organic Substrates
  - Silicon Substrates (TSV Interposers)
  - Silicon Substrate (EMIB, TSV-less)
  - Fan-Out RDL-Substrates
  - Ceramic Substrates
  - Glass substrate
  - Entirely new architectures using chiplets are possible



J. Kim et al., "*Architecture, chip, and package co-design flow for 2.5D IC design enabling heterogeneous IP reuse,*" in Proc. 56th DAC, Jun. 2019

6

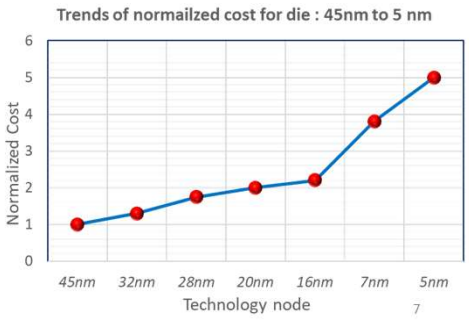
6

Why Chiplets ?

- Moore's Law keeps slowing
  - It is not sufficient to meet compute needs
  - Cannot use bigger chips to offset the slowdown
- How to extend performance gains ?
- Increasing die sizes are economically challenging
- Build multiple smaller chips (chiplets)
  - Not needed for some markets
- A heterogeneous integration solution can move us into the next semiconductor era

https://www.chipestimate.com/Enabling-Cost-Effective-High-Performance-Die-to-Die-Connectivity/Cadence/Technical-Article/2020/07/21

Performance/ Node [nm]	20 → 16	16 → 10	10 → 7	7 → 5
Power	60%	40%	<40%	20%
Performance	40%	20%	30%	15%
Area Reduction	-	50%	37%	45%



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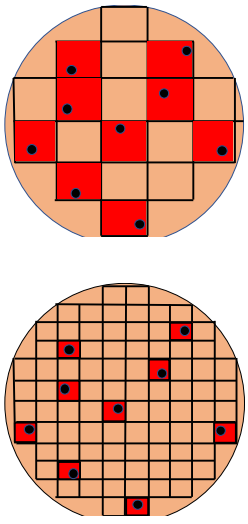
Effect of Die Size on Yield



Defect

Good die

Defective die

- Effect of 9 random defects
  - 18 dies and 9 good dies : Yield = 50%

$$Yield = \frac{Number\ of\ good\ dies}{Total\ number\ of\ dies}$$

$$Die\ Cost = \frac{Wafer\ Cost}{Dies\ per\ Wafer\ \times\ Yield}$$

- Dramatic increase in yield with smaller die
  - 92 dies and 83 good dies : Yield =90.2%

8

8

Chiplets Advantages

- Chiplets offer a compelling value proposition that includes:
  - Better yield due to smaller die size
  - Volume cost advantage when the same chiplet(s) are used
  - Lower manufacturing costs by purchasing known-good die (KGD)
  - Flexibility in picking the best process node for the part—RF, SerDes I/O and optical I/O do not need to be on the "core" process node
  - Shortened IC design cycle time and reduced integration complexity by using pre-existing chiplets: Accelerate time to market

9

9

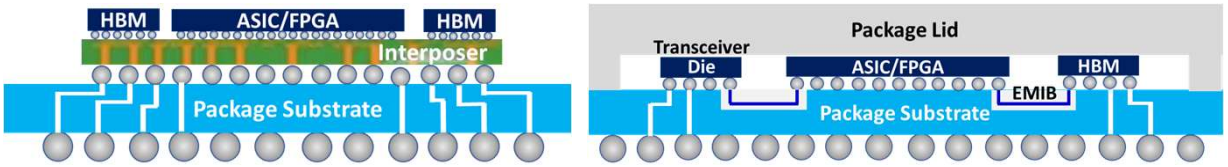
Chiplets Disadvantages

- Chiplets are not free
- Higher package costs
- Increase power consumption
- Additional design effort, complexity
- Current design methodology less suited for chiplets
- Additional area for interfaces
- Add latency as the cores are physically separated from each other
- Ability to move to the next node: some I/O components are hard to shrink.
- Not yet broader support, the economics do not favor this approach

10

10

Integration using Organic and Silicon Interposers



- A conceptual drawing of the cross-section of a heterogeneous system with *ASIC/FPGA* dies and *HBM* technology
  - Organic interposer
  - Silicon interposer : Chip-on-Wafer-on-Substrate *(CoWoS)*
  - Embedded Multi-Die Interconnect Bridge *(EMIB)*

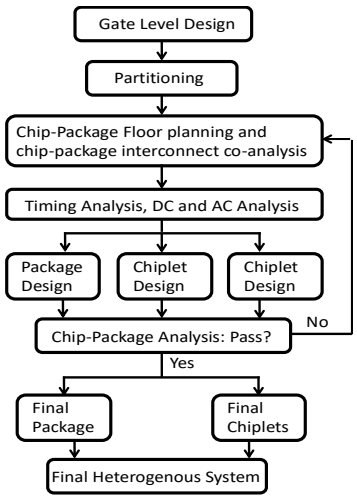
Chiu *et al., "Bridge interconnect with air gap in package assembly,"* U.S patent 2014/0070380 A1, Mar. 13, 2014.

11

11

Chiplet-Package Co-Design For High Performance

- Currently, each chiplet is designed independently without the knowledge of the package interconnect routing
  - The optimization of chiplets and package are conducted separately
  - Chiplets and the package never actually interact with each other until after they are fabricated and assembled
- To achieve the maximum performance with highest reliability, the chiplets and package need to be co-design
  - Implement co-design for 2.5D aware partitioning suitable for SoC design
  - The optimization steps of an individual chiplet also need to consider package routing as well as the other chiplets.
  - Perform chip-package floor planning and post design analysis



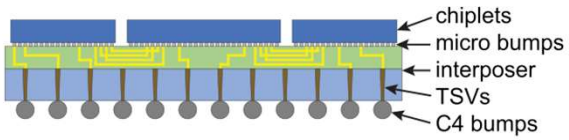
MD A. Kabir, Y. Peng, "Chiplet-Package Co-Design For 2.5D Systems Using Standard ASIC CAD Tools," 25th ASP-DAC, Jan. 13-16, 2020

12

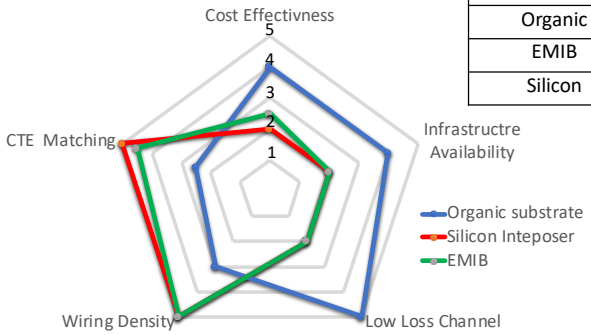
12

Advanced Packaging and Chiplets

- Silicon interposer
  - CoWoS and EMIB
  - Passive and active
- Organic substrate



Interposer Type	H (um)	T (um)	W (um)	S (um)	ε_r	tan (δ)
Organic	10	10	5-7	5-7	4.6	0.02
EMIB	2	1	<2	<2	3.9	0.001
Silicon	1	1	<1	<1	3.9	0.001



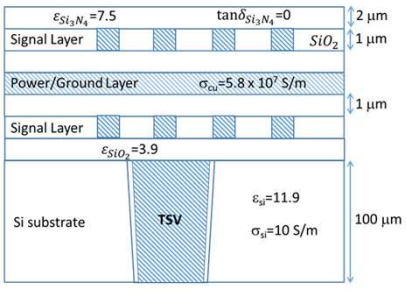
TSV diameter/depth	10 um / 100 um
Micro-bump pitch	< 55 um
C4 bump pitch	< 150 um
Die-to-die spacing	500 um – 4000 um
Metal layers	4

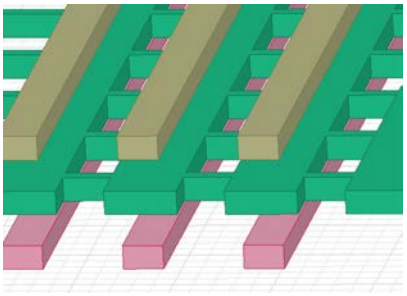
J. Kim et al., Proc. 56th DAC, Jun. 2019

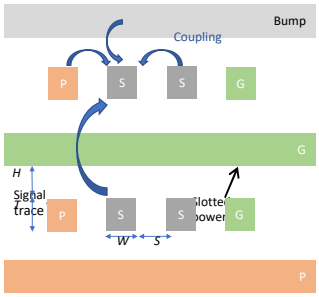
13

13

Typical Silicon Interposer Cross-Sections





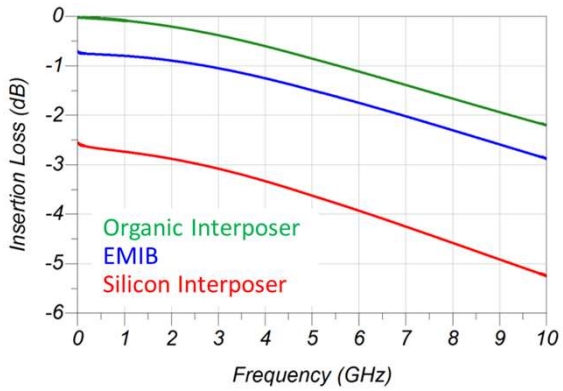


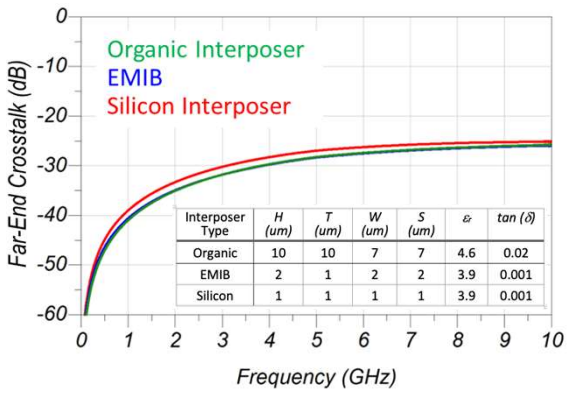
- Heterogeneous integrations on silicon substrates (TSV-interposers) are for multi- chips on silicon wafer or system-on-wafer (SoW)
- Heterogeneous integrations on organic substrates using finer metal line width and spacing (~ 5 µm) at high yield

14

14

Silicon and Organic Interposer Interconnects





Interposer Type	H (um)	T (um)	W (um)	S (um)	ε	tan (δ)
Organic	10	10	7	7	4.6	0.02
EMIB	2	1	2	2	3.9	0.001
Silicon	1	1	1	1	3.9	0.001

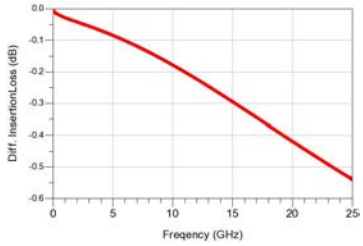
- The signal integrity of the three types of interconnects: organic and silicon interposers and *EMIB*, are analyzed using typical dimensions

15

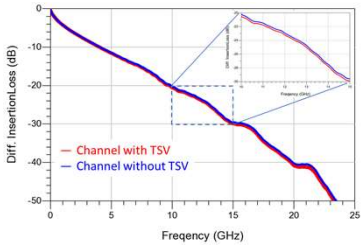
15

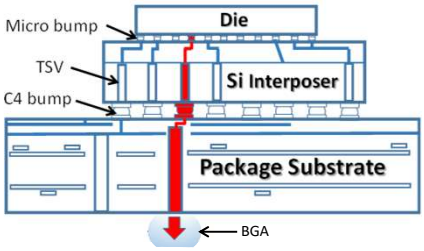
The Silicon Interposer : TSV Loss

Si Interposer TSV Loss



Long Channel Insertion Loss



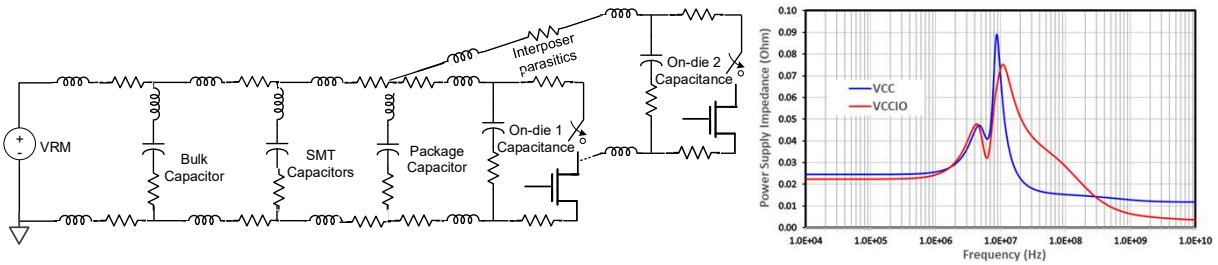


- The Interposer TSV's contribution to the loss of the long-reach channel is negligible
- Notice multiple interposer TSV's are often used for signal connection

16

16

PDN of the heterogenous integrated system

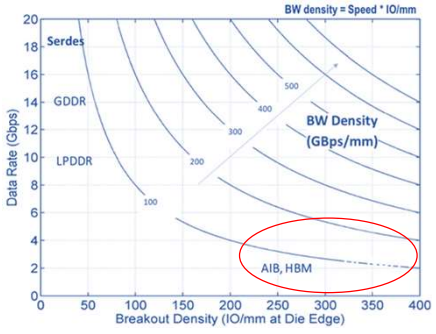


- The power distribution network connections between dies in interposer allows sharing of on-chip decoupling capacitors
  - Common in a multi-die system with *HBM*

17

17

I/O Characteristics



- Die-to-die interface (chiplet)
  - Very short reach and simple I/O
  - Lowest latency and lowest power
  - Parallel connections running at low data rates
- Memory interface
  - Medium length channel (4 in to 8 in)
  - Medium complexity I/O, low latency and medium power
  - Parallel connections at medium speeds
- High-speed serial interface (40 in)
  - Lowest connections running at highest speeds (at latency cost)
  - Very high channel insertion loss (closed eye without signal conditioning features)
  - Very complex, equalization, clock recovery, crosstalk cancellation, …

R. Mahajan, *et al.*, "*Embedded Multidie Interconnect Bridge—A Localized, High-Density Multichip Packaging Interconnect*," IEEE CPMT Oct. 2019 18

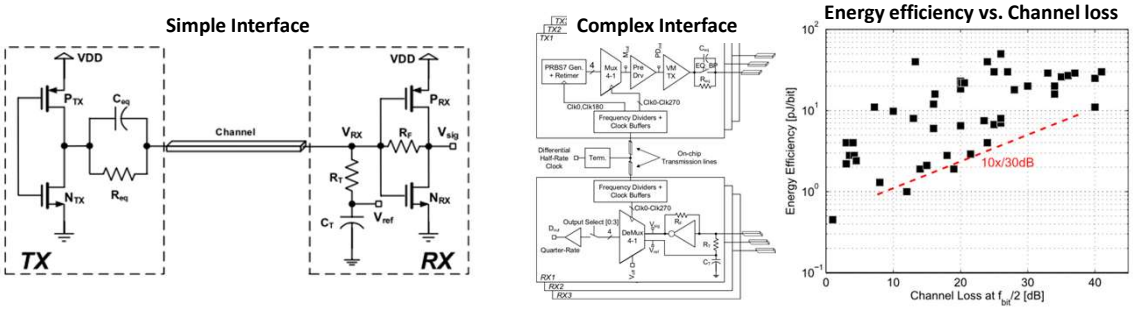
18

Current Chiplet Interfaces

- Chiplet interfaces in high-performance applications, such as memory and processor systems, run at 2 Gbps and higher
  - Closely integrating multiple chips using extremely wide bus
  - Improving performance by simplifying communication and clocking
  - Greatly improving bandwidth, power efficiency, latency due to proximity

Chiplet Interface	Intel AIB	Intel MDIO	TSMC LIPINCON	HBM2E	USR
Bandwidth per pin [Gb/s]	2	5.4	8	3.2	>32
Bandwidth density[GB/sec/mm^2]	150	198	320		
I/O Voltage swing [V]	0.9	0.5	0.3	1.2	1.2
PHY power efficiency [pJ/b]	0.85	0.5	0.56	0.8	1.6
Latency [ns]	3.56			low	>37

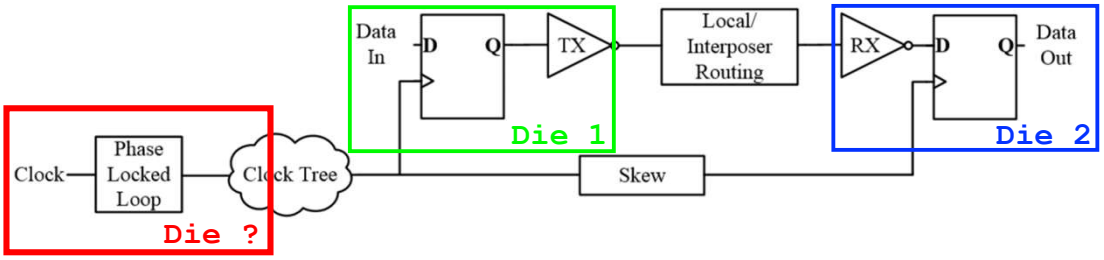
Die-to-Die Interfaces



- Die-to-die interfaces are very different from traditional memory interfaces or SerDes links in many respects
  - The massive die-to-die interconnects is not impedance controlled
  - Power is lower by order of magnitude when compared to high-speed links
- There are distinct challenges that requires unique approaches

B. Dehlaghi, and A. Carusone, IEEE JSSC, VOL. 51, NO. 11, NOV. 2016

Clock and Data in Chiplet Interfaces



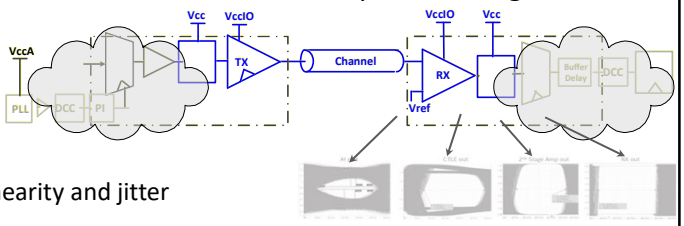
- Source-synchronous parallel interface are commonly used
- Clock for READ and WRITE operations is generated in Die 1, Die 2 or Die 3
- Signal and clock paths can involve multiple dies and interposer routing
- Delays of clock and data paths can be long and significantly different

21

21

Noise and Jitter Analysis of Chiplet Interfaces

- Voltage and timing jitter due to channel and front-end circuits captured using transistor-level circuit simulation
  - Channel inter-symbol interference
  - Simultaneous switching output noise
  - Driver strength variation,
  - Transmitter and receiver front-end nonlinearity and jitter

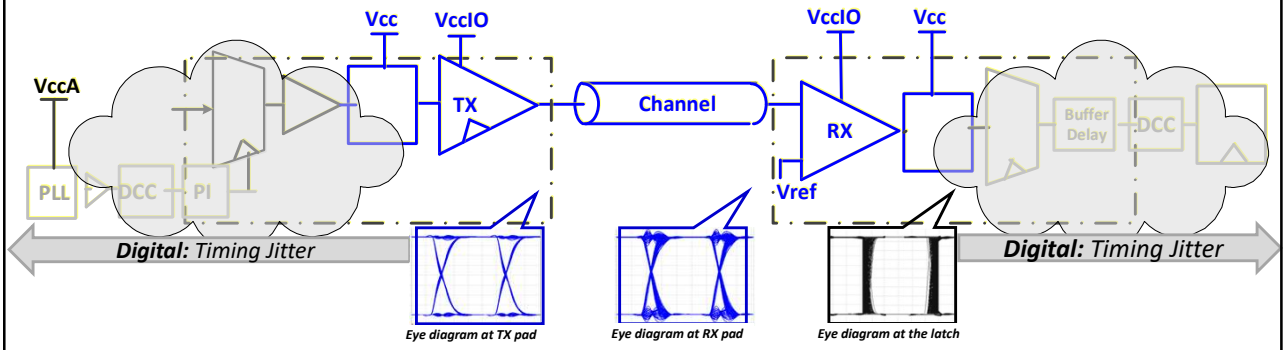


- Timing jitter impact of internal path (clock and data) is more critical to capture
  - Power Supply Noise Induced Jitter (PSIJ) for internal data/clock paths
  - PLL jitter, DCD, calibration error, VT variation, EOL (aging*), HBM budget
  - Receiver setup and hold time
  - High Volume Manufacturing Variation

22

22

Die-to-Die Interfaces Analysis Methodology



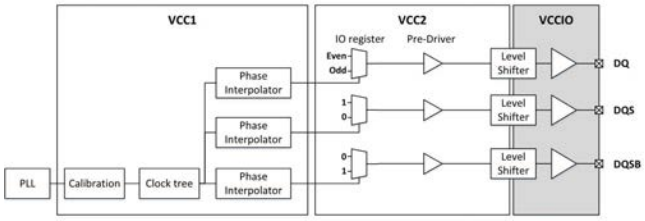
- *'Analog'* and *'Digital'* sections where two different approaches are used to capture the voltage and timing jitter
- Power supply noise and jitter are key factors that limit the performance of interface in die-to-die interfaces

Channel Jitter/Noise Sources	Contribution
ISI Jitter [UI]	0.07 – 0.10
ISI+ Crosstalk Jitter [UI]	0.10 – 0.13
ISI + Crosstalk + SSN jitter[UI]	0.13 – 0.17
Power Supply Noise [mV]	30 – 45

Jitter Budget (An Example)

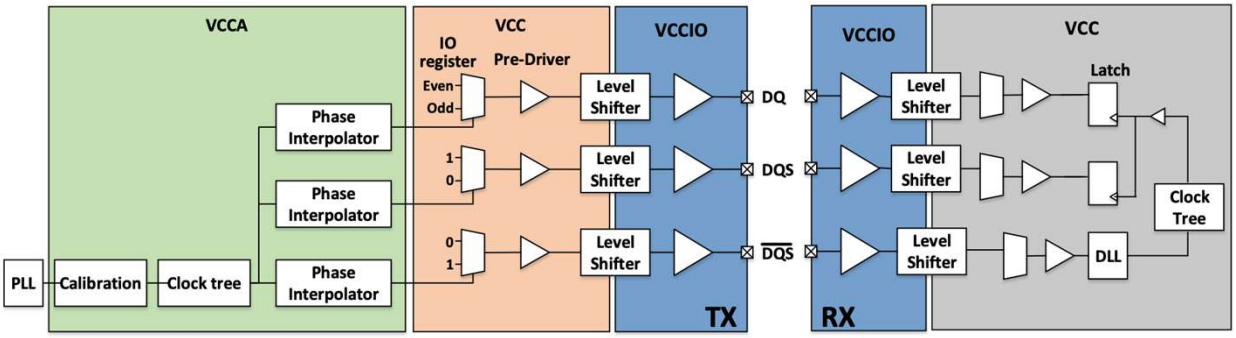
Items	Jitter [%UI]
PLL Jitter	4%
Calibration error	5%
Clock tree	9%
Phase interpolator	5%
I/O register	6%
Pre-driver	5%
Level Shifter	3%
TX & RX	27%
Channel	17%
VT variation	5%
HVM	7%
Margin	7%

- Supply noise, noise sensitivity, timing jitter of each subcircuit in the data and clock paths need to be calculate
  - Can take significant time and memory to obtain via transistor-level circuit simulation



UI : Unit Interval

Power Supply Partition in a Typical I/O Subsystem



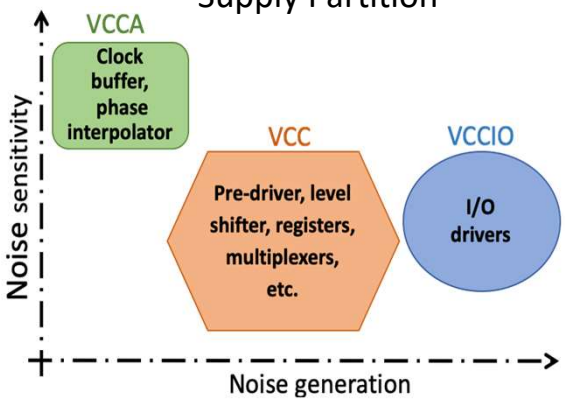
- In the *I/O* circuit block, there can be several power rails for performance improvement, lower-power consumption and meet fixed voltage level defined in the *I/O* interface specifications.

25

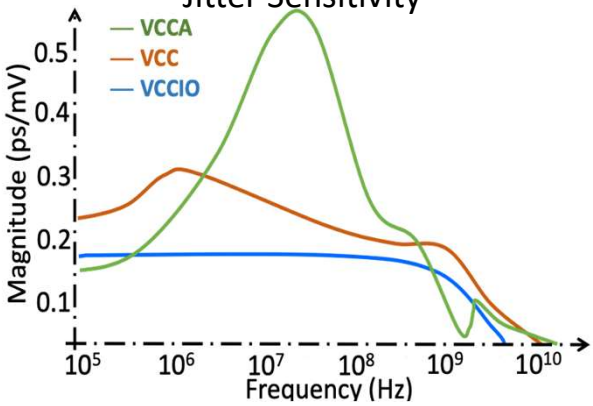
25

Supply Noise Partition for Performance

Supply Partition



Jitter Sensitivity

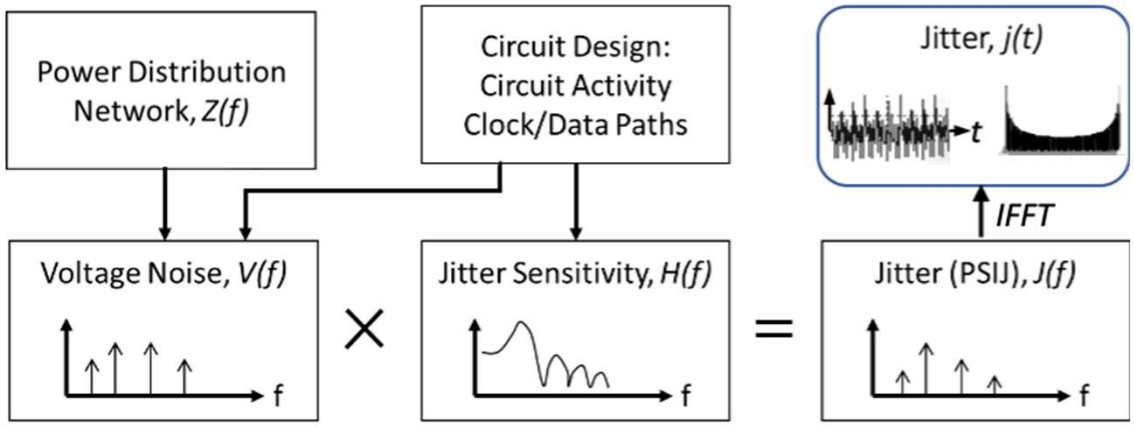


- Partition often based on noise generation and noise sensitivity
- Jitter sensitivity functions for VCCA, VCC, and VCCIO

26

26

Power Supply Noise Induced Jitter (PSIJ)

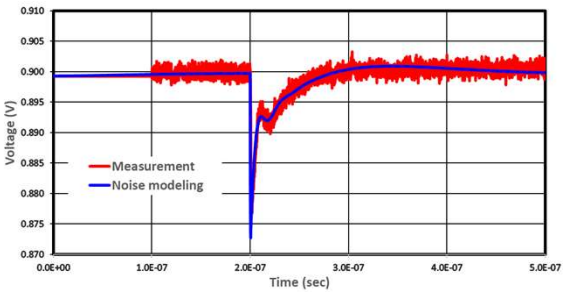


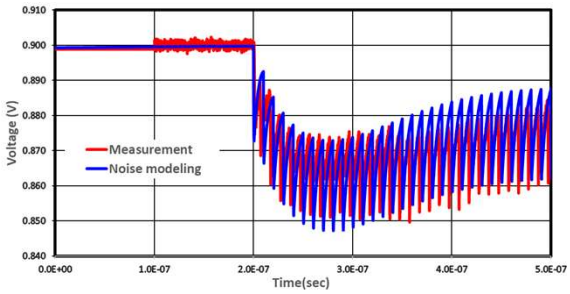
R. Schmitt et al., "Design and Characterization of the Power Supply System for a High Speed 1600 Mbps DDR3 Interface in Wirebond," DesignCon 2012, Santa Clara, CA, 2012.

27

27

Power Supply Noise : VCC



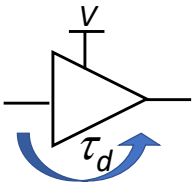


- Power supply noise and PSIJ are key factors that limit the performance of interface in die-to-die interfaces : ***Jitter = V_{noise}(f) X S(f)***
- In multi-die systems, one or more dies can turn on and off creating a large current surge in a very short period (of time)

28

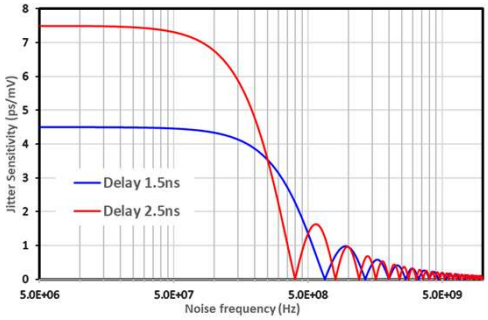
28

Empirical Jitter Transfer Functions



$$H_0 = \frac{\tau_{d\,@Vmin} - \tau_{d\,@Vmax}}{Vmax - Vmin}$$

$$|H(f)| = H_0 \left|\frac{\sin(\pi f \tau_d)}{\pi f \tau_d}\right| = H_0 |\mathrm{sinc}(\pi f \tau_d)|$$

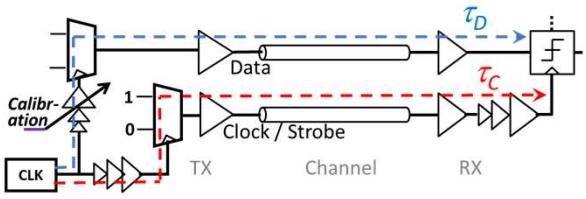


- The *DC* delay sensitivity is directly proportional to the delay of the circuit and the magnitude of the frequency-dependent jitter sensitivity
- When the path delay is large, the *DC* sensitivity (H_0) is high, the path is more sensitive to the low-frequency noise.

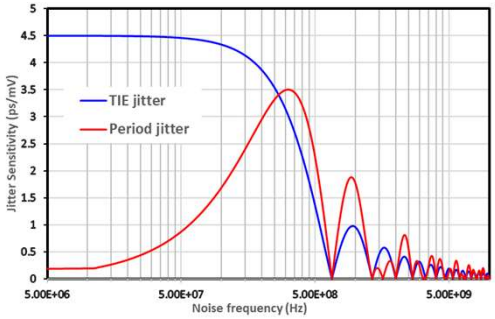
29

29

Jitter Transfer of Multi-Die Source Synchronous



$$|H_{period}(f)| = 2H_0 |\mathrm{sinc}(\pi f \tau_d)| \cdot |\sin(\pi f T_{clk})|$$

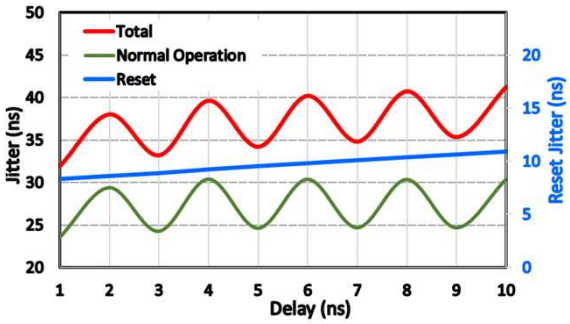


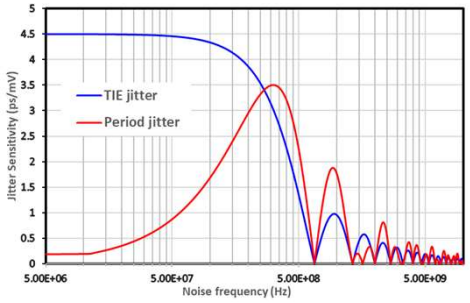
- Due to the jitter tracking effect, the jitter sensitivity has low value in lower frequency region, thus the low-frequency noise impact to period jitter becomes smaller

30

30

Jitter from Normal and Reset Operations



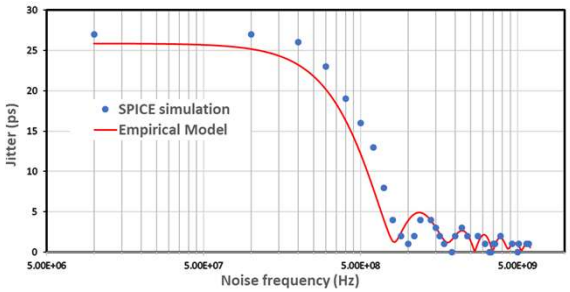


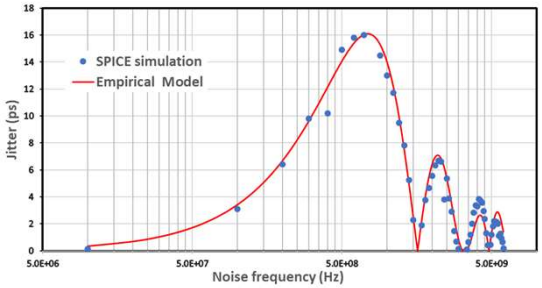
- Total jitter from normal and reset operation as a function of path delay
- The clock quality can significantly be degraded by the duty cycle distortion (DCD) and the power supply induced jitter (PSIJ)

31

31

Comparisons of Empirical and SPICE Simulation





- With the same *SPICE* simulations, data signal jitter induced by *VCCA* or *VCC* noise is measured and compared with empirical *PSIJ* analysis
- *Data jitter (without strobe signal triggering) as a function of VCCA noise*
- In source synchronous clocking systems, the data and clock jitter can be tracked out when the noise frequency

W. Beyene *et al.*, "*Noise and jitter characterization of high-speed interfaces in heterogeneous integrated systems*," *IEEE Trans. CPMT, Vol. 11, No. 1, Jan. 2021.* 32

32

Conclusions

- A heterogeneous integration solution can move us into the next semiconductor era
- Three types of interconnect designs using organic and silicon interposers (with and without TSV*)* are analyzed for heterogenous integration
  - Entirely new architectures using chiplets are possible
- Low-power and low-latency chiplet interface is essential
- The die-to-die interconnects are very short, and the signal integrity does not pose a challenge at current data rates
- The huge increase in the transient current in multiple dies and the unique clocking architectures of such systems make the supply noise and power supply induced timing jitter the limiting factors

33

33

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34

34