Bonding Technologies for the Next Generation Integration Schemes

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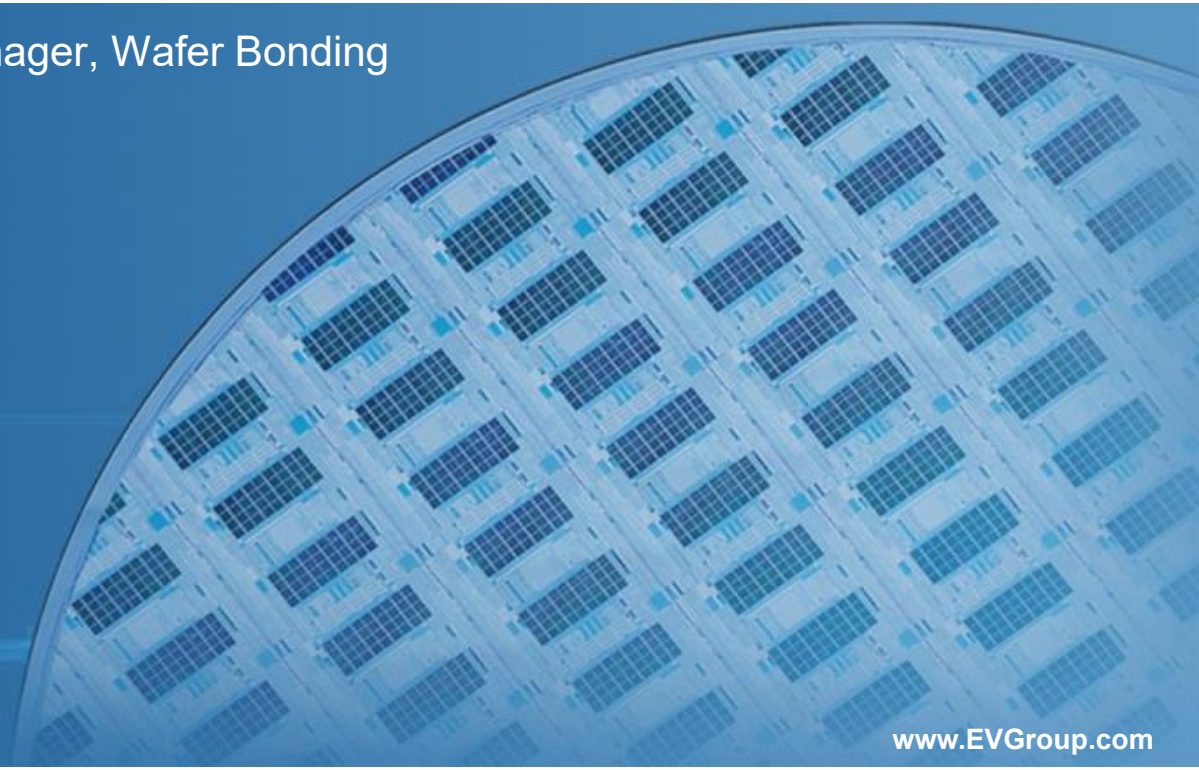


Outline

- Introduction
  - EVG at a Glance
  - Recent Developments
  - Product Portfolio & Competence
- Bonding Technology for the Next Generation Integration Schemes
  - Introduction
  - Bonding Requirements to meet trends
    - Fusion & Hybrid Bonding
    - ComBond®
- Wafer level vs. Die to Wafer integration
  - Overview
  - Process Results
- Summary & Outlook

EV Group | At A Glance

Leading supplier of wafer processing equipment for the MEMS, nanotechnology and semiconductor markets

Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1000 employees worldwide

Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China and Taiwan

EV Group Headquarters

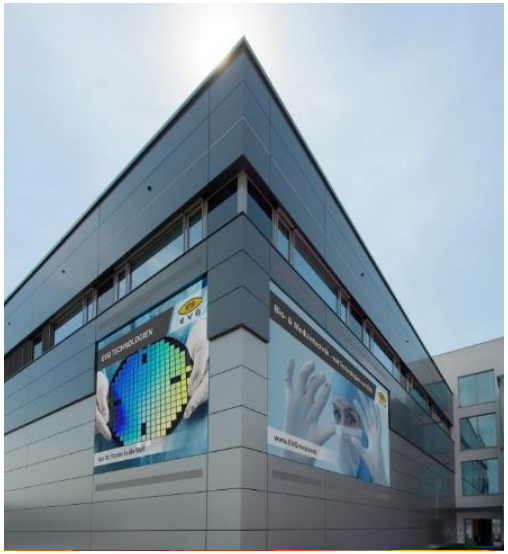
St. Florian am Inn, Austria

Newly Cleanroom V nearly doubles cleanroom capacity and strengthens capabilities of EVG's NILPhotonics® and Heterogeneous Integration Competence Centers

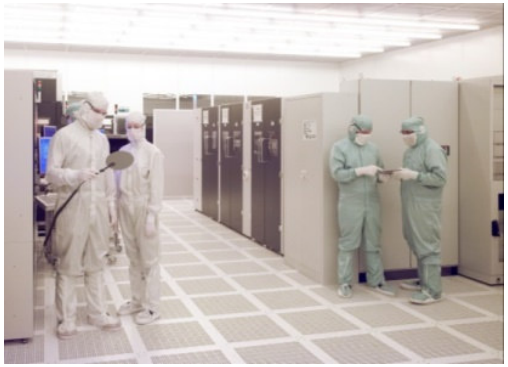
EV Group | At A Glance
Heterogeneous Integration Competence Center | Launch 2020

ST. FLORIAN, Austria, March 2, 2020

“Heterogeneous integration fuels new packaging architectures and demands new manufacturing technologies to support greater system and design flexibility, as well as increased performance and lower system design costs,” stated Markus Wimplinger, corporate technology development & IP director of EV Group.
“EVG’s new HI Competence Center provides an open access innovation incubator for our customers and partners across the microelectronics supply chain to collaborate while pooling our solutions and process technology resources to shorten development cycles and time to market for innovative devices and applications enabled by heterogeneous integration.”



Facility-Infrastructure	IT-Infrastructure	Risk Reduction
Process Development	Process Transfer	

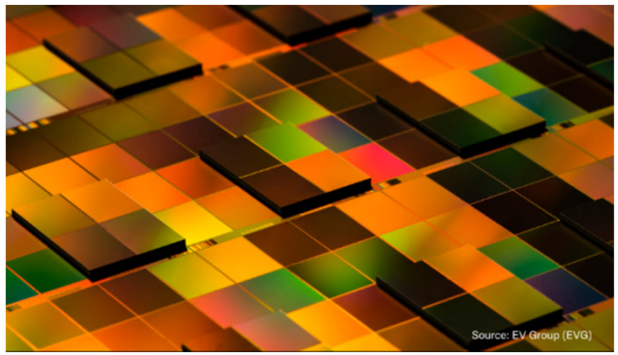


Invite our customers to take advantage from our collaboration frame work

EV Group | At A Glance
EVG Heterogeneous Integration Competence Center™

- **Features**
- EVG Heterogeneous Integration Competence Center™ Open Access Innovation Incubator
  - Fusion and Hybrid Bonding for W2W and D2W Bonds
  - Aligned Metal Bonding
  - Temporary Bonding and Debonding Open Platform
  - Advanced Resist Processing
  - Optical Lithography
  - Maskless Exposure Technology

- EVG's HI Competence Center is designed to help enable new products and applications driven by advances in system integration and packaging. Shown here: chiplet integration by collective die-to-wafer hybrid bonding.
- The Heterogeneous Integration Competence Center™ combines EV Group's world-class wafer bonding, thin-wafer handling, and lithography products and expertise, as well as pilot-line production facilities and services at its state-of-the-art cleanroom facilities.



EV Group | Product Portfolio

INDUSTRY LEADING WAFER PROCESSING EQUIPMENT

LITHOGRAPHY

- Mask Alignment Systems
- Resist Processing Systems
- Integrated Lithography Track Systems

NANOIMPRINT LITHOGRAPHY

- UV Nanoimprint Lithography / SmartNIL® Systems
- Hot Embossing Systems

BONDING

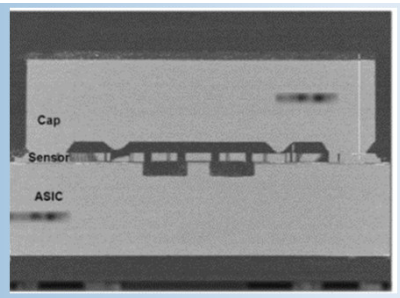
- Permanent Bonding Systems
- Temporary Bonding and Debonding Systems
- Bond Alignment Systems
- Fusion and Hybrid Bonding Systems

METROLOGY

- Inspection Systems
- Inline Metrology Systems

EVG I Product Portfolio & Competence

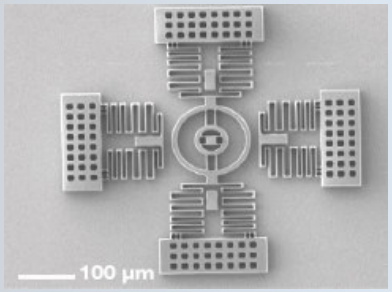
Wafer Bonding



Source: EVG

→ Direct Bonding
→ Metal Bonding
→ Adhesive Bonding
→ Temporary Bonding & Debonding
→ Metrology

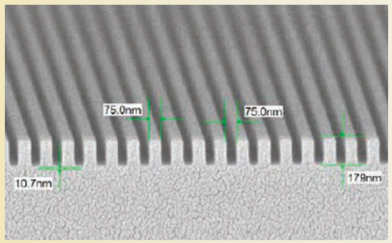
Coating & Lithography



Source: EVG

→ Lithography for Etching and Metallization
→ Bond Frames
→ Cavity Exposure
→ Bumping
→ Advanced Resist Processing

Nanoimprint Lithography



Source: EVG

→ UV-Nanoimprint Lithography
→ SmartNIL®
→ Lens Molding
→ Hot Embossing

Integration Schemes are Driven by Global Megatrends

Mobiles, AR/ VR, Sensing

Wireless Infrastructure

Big Data, IoT

Autonomous Driving

HPC, AI, Quantum

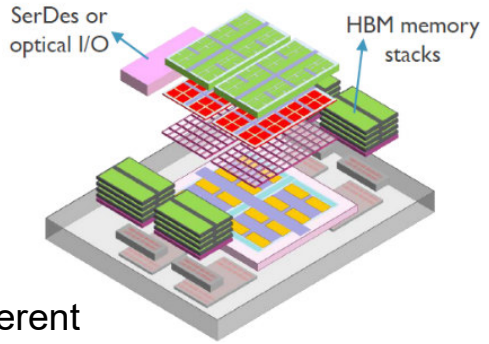
Consumer — Mission Critical Applications

Heterogeneous Integration

Bonding Technologies

Wafer to Wafer
Chip to Wafer
Integration

Combining different functionalities onto a single device e.g: Logic , Memory, Analog, RF and more



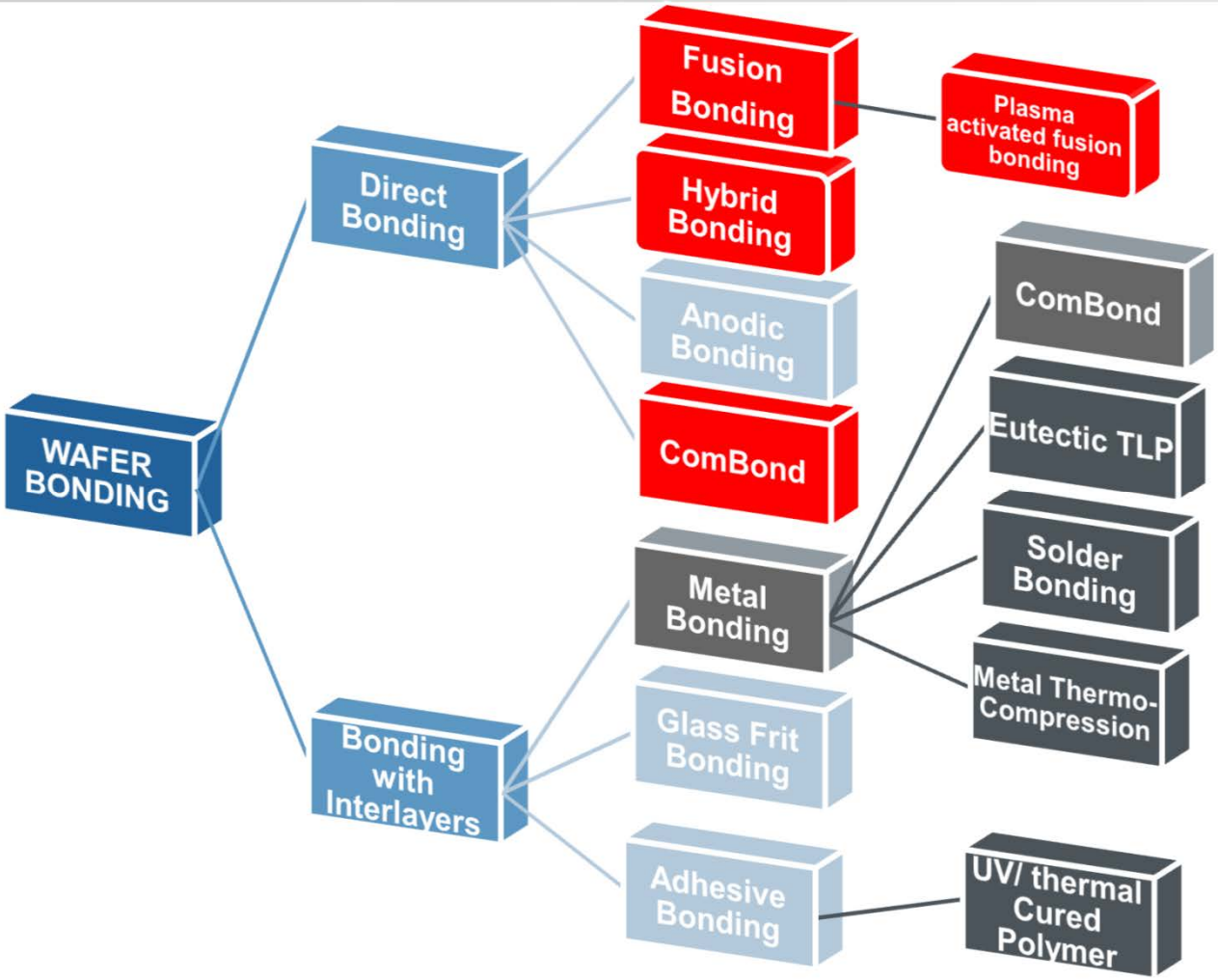
Source: IMEC

Combining different substrate materials and manufacturing nodes

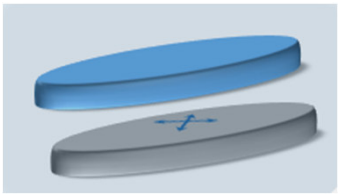
Requirements

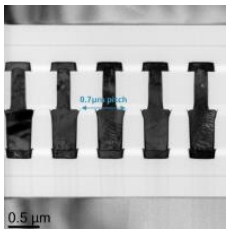
High bandwidth data transfer
Low power consumption
Smallest form factor

Bonding Processes to support Heterogeneous Integration

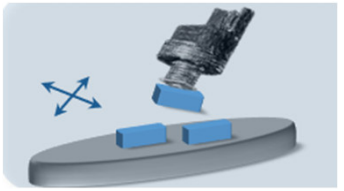


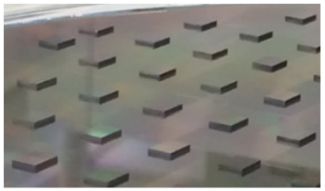
Wafer to Wafer





Chip to Wafer





Wafer Bonding Process
Fusion / Hybrid Bonding

Definitions, Principle

❑ Fusion bonding:

Wafer bonding process based on the adhesion of two flat and smooth surfaces placed in contact occurred due to chemical bonds established between molecules from the two surfaces.

Process consists of two steps:
Room temperature contacting of the wafers (pre-bonding)
Thermal annealing for strengthening the bond

❑ Plasma Activated Fusion Bonding:

Fusion bonding process using a plasma treatment of the substrate surfaces prior bonding.

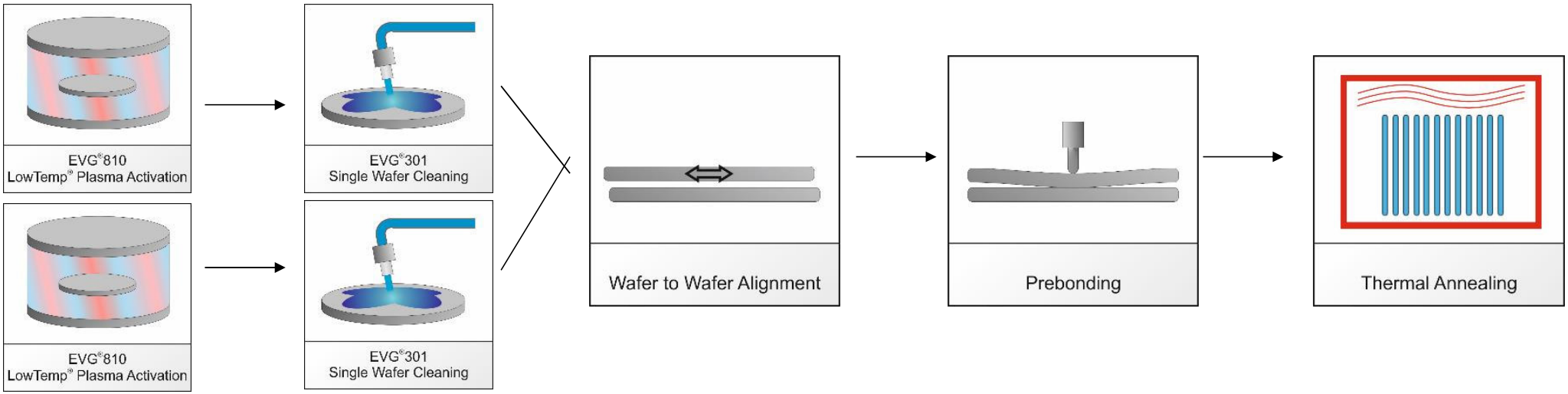
The plasma treatment produces changes to the surfaces resulting in higher energy bonds and requiring lower temperature/lower time for the final thermal annealing

❑ Hybrid Bonding

Hybrid Bonding is a Fusion bonding process using plasma treatment of the substrates prior to bonding whereas the wafer surface consists out of dielectric and metal interconnects on the same surface plane.

Room temperature contacting of the wafers (pre-bonding)
Thermal annealing for strengthening the bond and form the electrical contact of the interconnects

Process Flow I Fusion Bonding

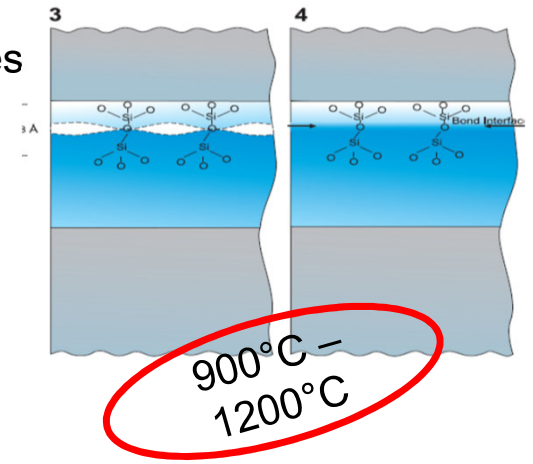


- Single wafer cleaning is an optional step for particle removal and it is not required for bond strength enhancement.
- Wafers' pre-bonding have to be performed immediately after wafers preparation (plasma activation and single wafer cleaning) in order to avoid potential contamination of the surfaces.

Fusion Bonding I Mechanism

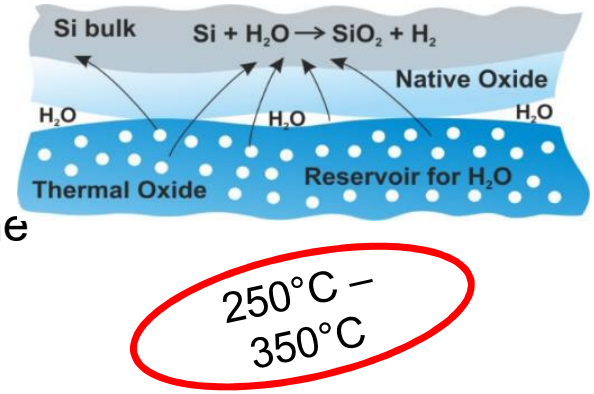
- **Fusion bonding:**
  Wafer bonding process based on the adhesion of two flat and smooth surfaces placed in contact occurred due to chemical bonds established between molecules from the two surfaces.
  Process consists of two steps:
  - Room temperature contacting of the wafers (pre-bonding)
  - Thermal annealing for strengthening the bond

  Gap closing due to viscous flow of oxide during high temperature annealing

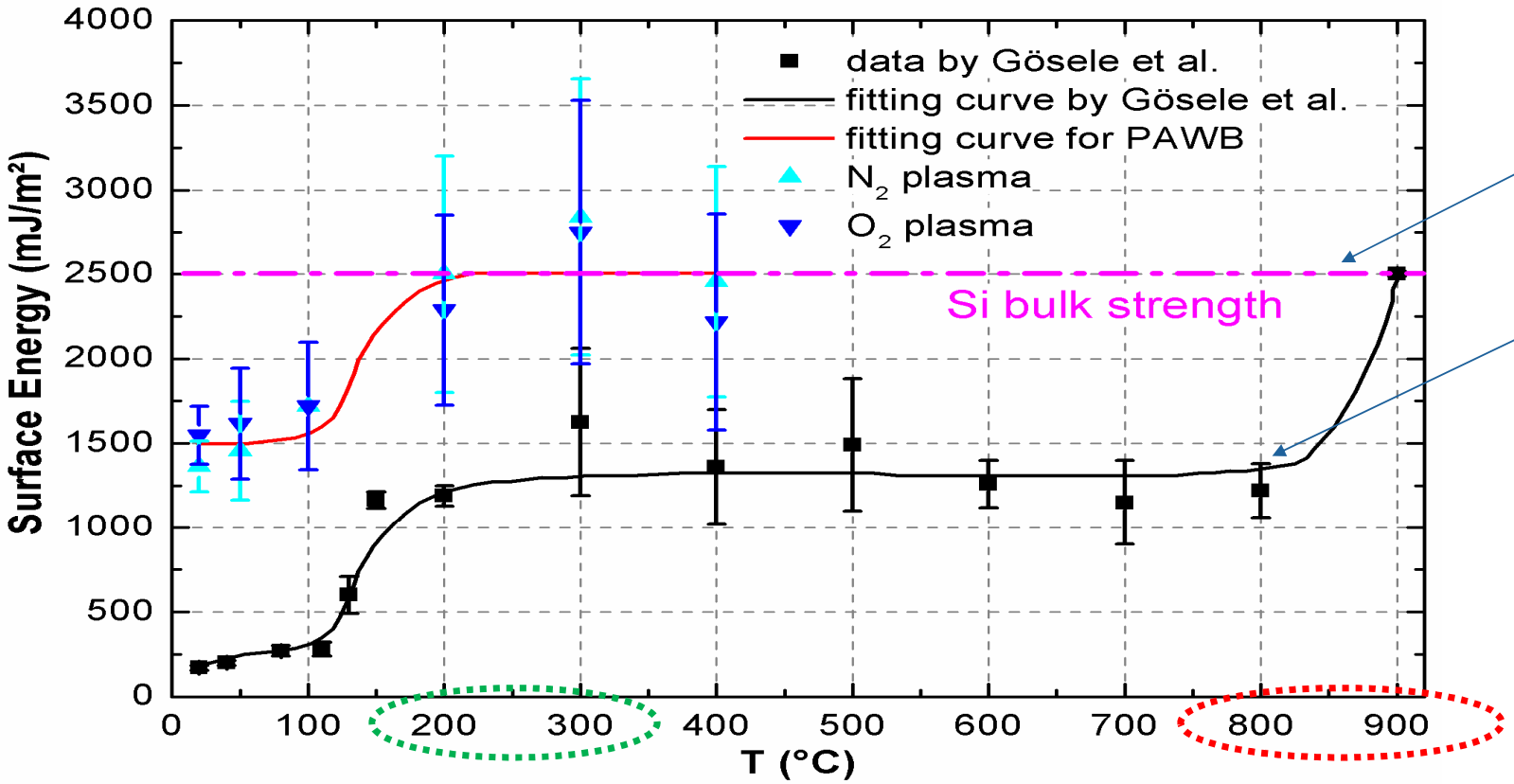


- **Plasma Activated Fusion Bonding:**
  Fusion bonding process using a plasma treatment of the substrates surfaces prior bonding.
  The plasma treatment produces changes to the surfaces resulting in higher energy bonds and requiring lower temperature/lower time for the final thermal annealing.

  Closing of the gap due to oxidation at low temperatures



Fusion Bonding vs. Plasma activated Fusion Bonding



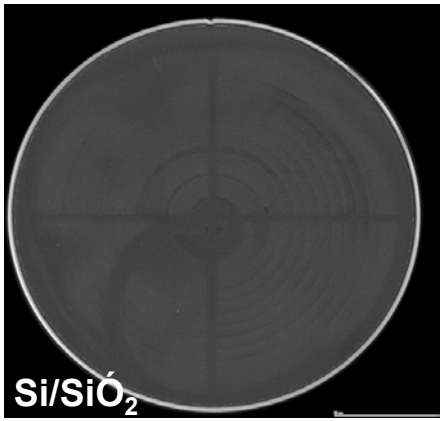
Plasma activated fusion bonding

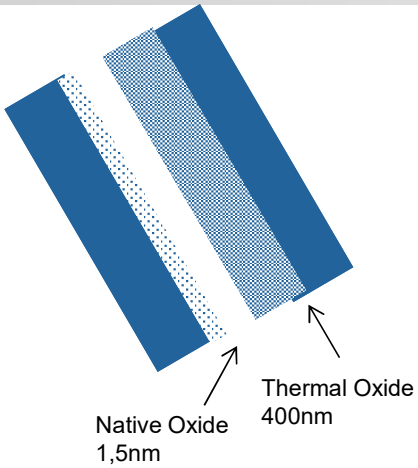
Fusion bonding
(no Plasma)

Plasma activation increases the bonding Energy at room temperature and for low temperature annealing

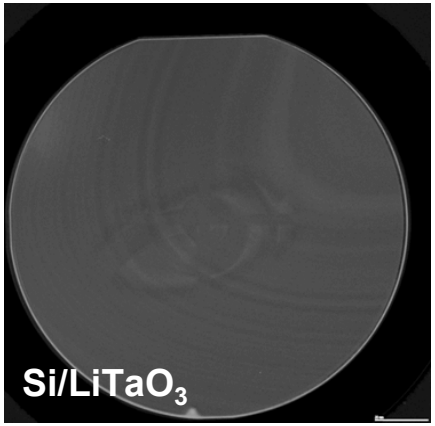
Q.-Y. Tong and U. Gösele, *Semiconductor Wafer Bonding: Science and Technology* (Wiley, 1998).

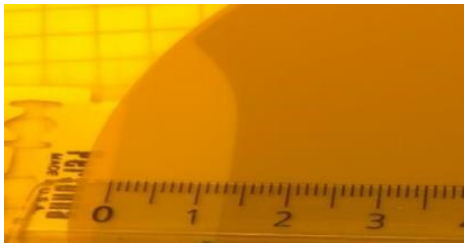
Process Results examples - Plasma activated direct bonding
Si/SiO_2 & $SiO_2/LiTaO_3$



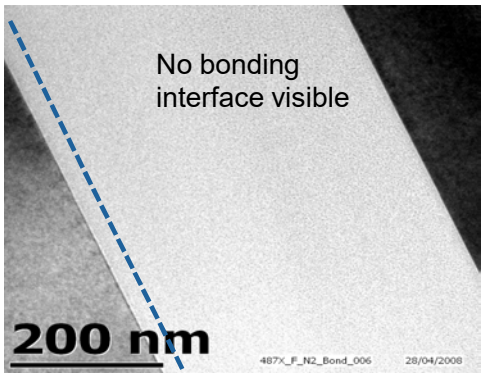


Bond Energy > 2 J/m²

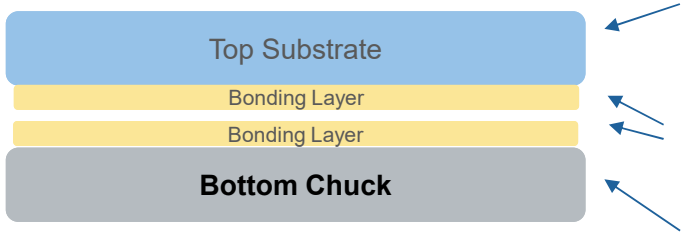




Bond Energy > 1,5 J/m²



Bonding setup



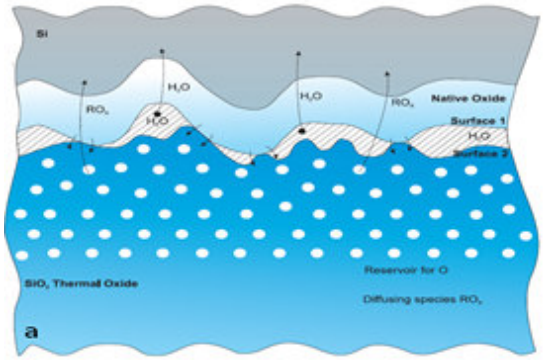
Substrates:
Silicon, GaAs, InP, GaN, SiC, Sapphire, Glass , Piezo, Ceramics, Diamond, etc…

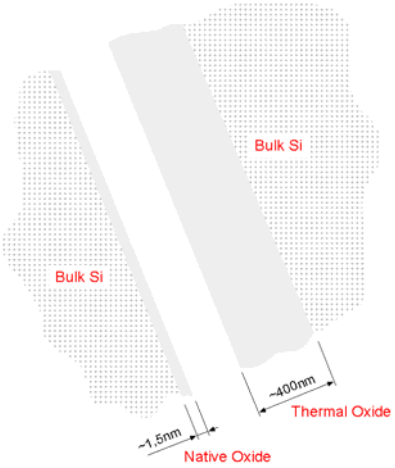
Bonding Layers:
SiN, SiO_2 , TEOS, SiCN, thermal Oxide etc…..

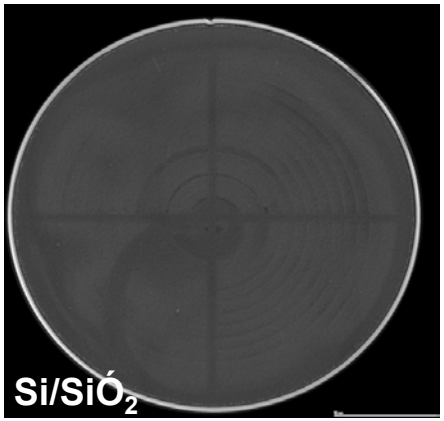
Substrates:
Silicon, GaAs, InP, GaN, SiC, Sapphire, Glass , Piezo, Ceramics, Diamond, etc…

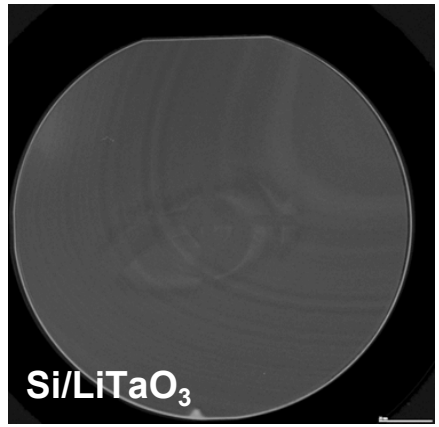
Direct bonding I Specification

Parameter	Value
Surface Micro roughness	< 0,5 nm Ideal < 0,3 nm
Incoming Wafer Bow / Wrap	≤ 30 µm *400 µm
Wafer TTV	< 3µm
Dielectric Material	SiO_2 , SiC_xN_y , SiO_xN_y ,SiN
Dielectric Material thickness	> 100nm
Metal Ion	Fe, Cu, Ni < 5e10 at/cm² Al, Na, K < 5e10 at/cm² Cr, Zn, Mn < 5e10 at/cm² Ti, K, Ca < 5e10 at/cm²
Surface cleaning	SC1 & SC2 cleaning
Particle	< 50 particles @ 90nm size
Organic Residues	No
Post annealing Temperature	200°C – 400°C
Substrate Material	Silicon, GaAs, InP, GaN, SiC, Sapphire, Glass , Piezo, Ceramics, Diamond, etc…



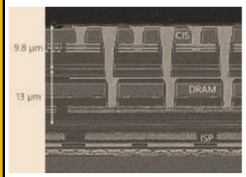
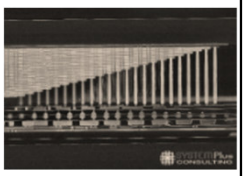
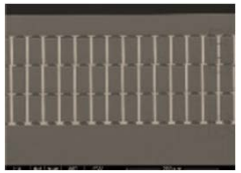
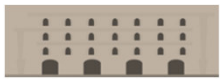
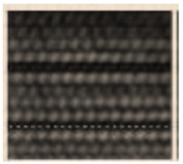
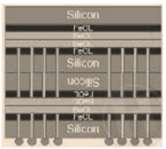
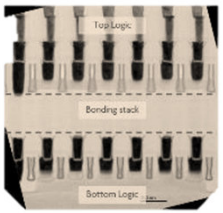






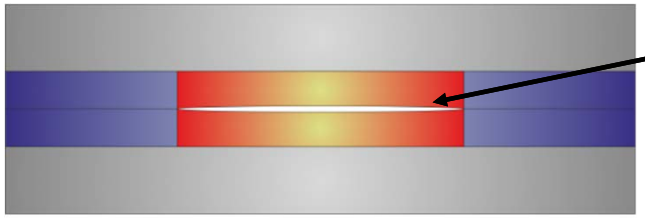
Hybrid Bonding

Hybrid Bonding I Market Segmentation

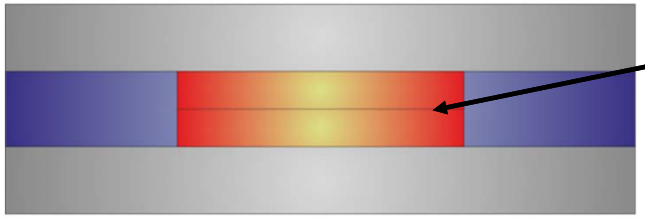
	Backside Illuminated Image Sensor	Memory				Logic		
		3D NAND Flash	HBM Stacks	DDR6+	Next Gen. Memory	SoC Partitioning		Scaling
Device Stack	Photo Diode + DRAM + Logic	NAND Block + Periphery	12+ layer stacking	Peri under DRAM	Peri on MRAM, FeRAM, PCM	SoIC	SRAM + Logic	Backside PDN (5nm node)
Bonding Process	W2W	W2W	W2W and/or D2W	W2W	W2W	W2W an/or D2W	W2W	W2W
	hybrid	hybrid	hybrid	fusion	fusion & hybrid	hybrid	hybrid	fusion
Pitch	2µm → 1µm	2µm → 1µm	5µm → 3µm	2µm → <1µm	2µm → <1µm	9µm → 2µm	2µm	By scanner
Maturity	HVM	HVM	R&D	R&D	R&D	Ramp Up	Ramp Up	Ramp Up
Example	 *Sony (System+)*	 *YMTC (System+)*	 *Xperi (ECTC2020)*	 *IMEC (PTW21)*	 *IMEC (PTW21)*	 *TSMC WoW SoIC*	 *IMEC Collaboration*	 *IMEC Collaboration*

Hybrid Bonding I Physical Mechanisms Basics

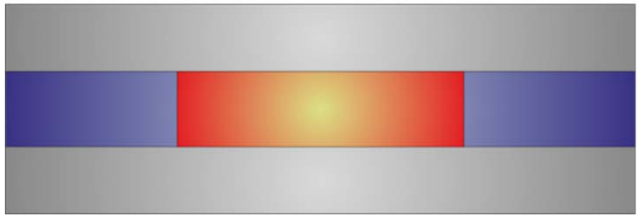
The gap (few nm) results/can be adjusted due to different removal rates during chemical mechanical polishing (CMP) of Cu and SiO_2.



1. After Si-direct bonding



2. After isolator annealing (intermediate step)



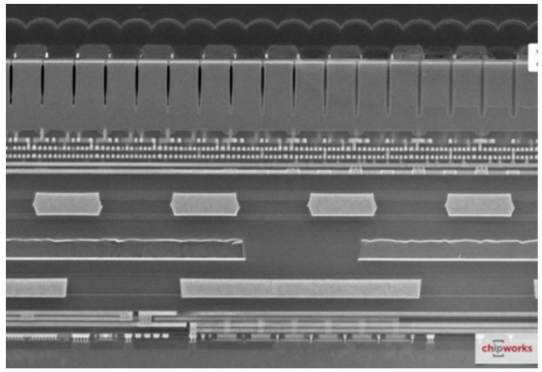
3. After annealing (final)

Cu dishing

- Depth and shape of the Cu influence the electrical conductivity and potentially the bonding strength
- Typically dishing is in the range of a few nm

Cu height & annealing temperature

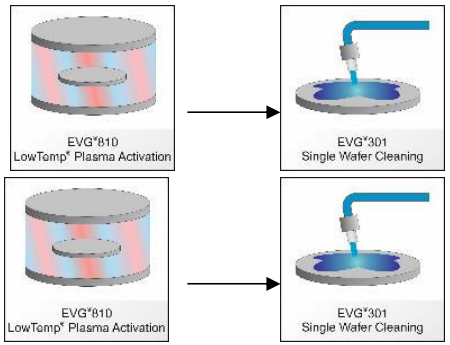
- During annealing the CTE-mismatch between Cu and SiO_2 causes the Cu to expand more than the surrounding dielectric
- Cu gets in direct contact (no dishing void)
- The (relative) Cu expansion directly depends on the Cu height, CTE-mismatch and annealing temperature
- Indirectly, the Cu deposition (purity grade, grain size,…) might also impact the expansion and „closing mechanism“

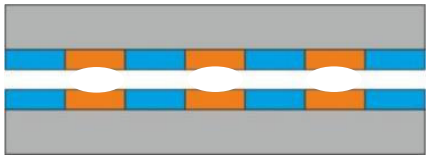


Reverse Engineering Image
Sony IMX260

Hybrid Bonding I Physical Mechanisms & Process Flow

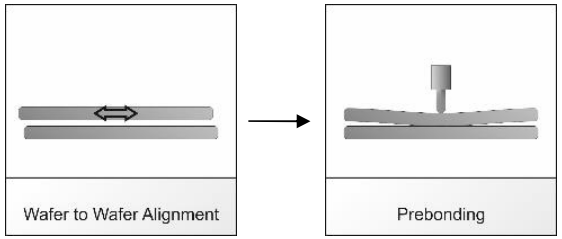
Wafer preparation Plasma activation and cleaning

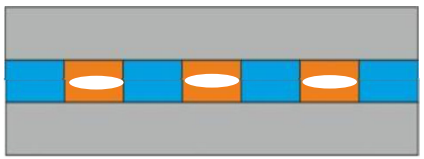




Wet cleaning and plasma activation are employed for surface preparation. Wet cleaning may include the use of chemicals for metal oxide removal

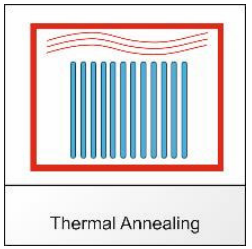
Wafer to Wafer alignment & Pre bonding

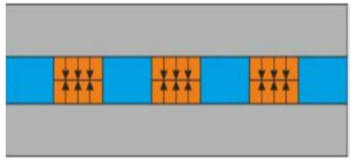


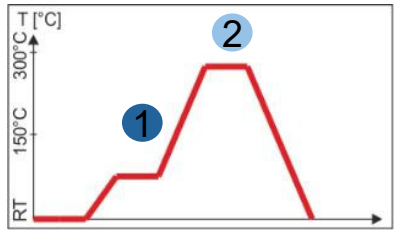


Wafers will be aligned using F2F optical alignment. Once aligned, wafers will be put in contact at room temperature and in regular cleanroom atmosphere.

Bond Pair annealing

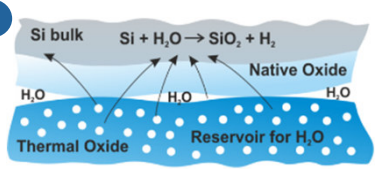






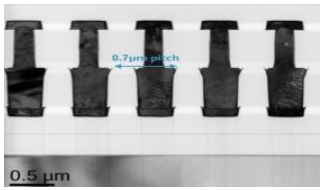
Annealing Process

1



Dielectric layer Annealing

2

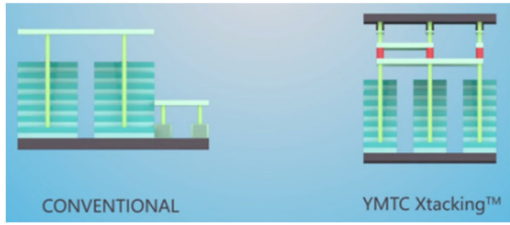


Interconnect gap closure due to different CTE of Dielectric bonding material and interconnect material

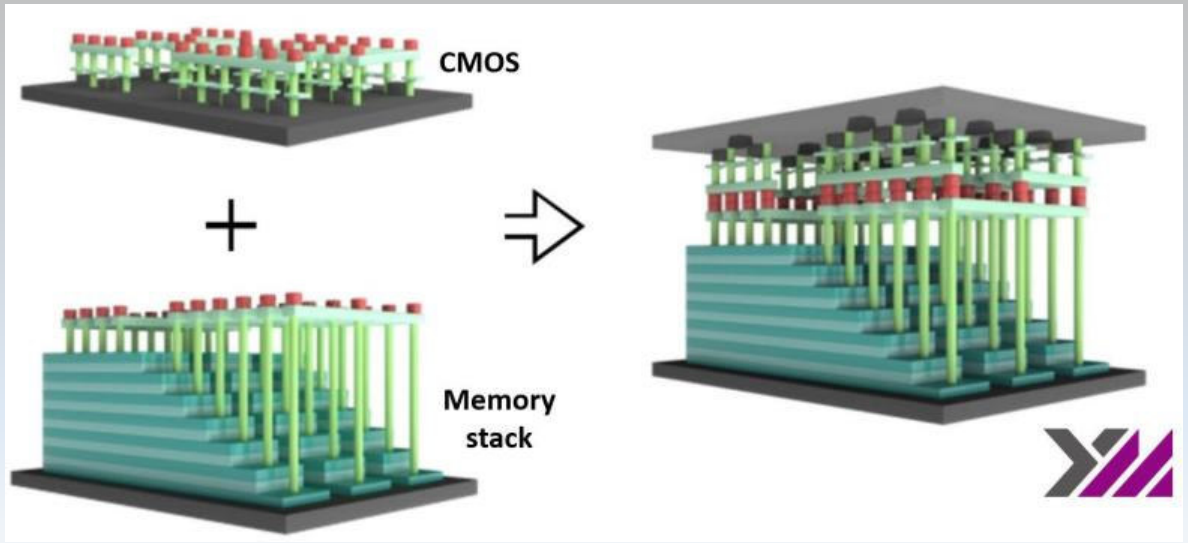
3D NAND Flash | Hybrid Bonding of Logic Circuitry to Memory Cell

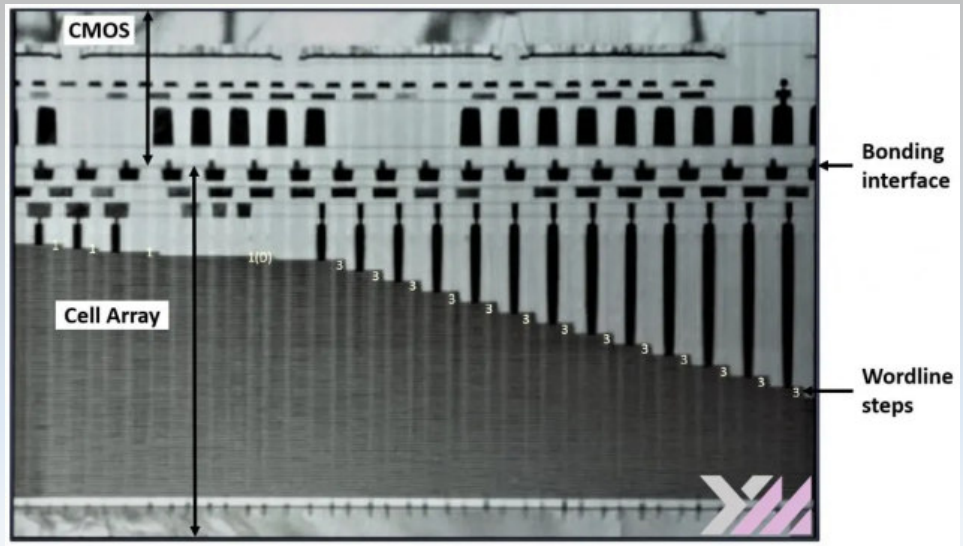
- NAND cell array benefiting from wafer bonded peripheral I/O circuits on top

- **Advantages:**
  - Peripheral circuits are processed on separate wafer using logic node FEOL processing allowing higher speed & bit density
  - Improved array efficiency thanks to the optimized area usage



Source: YMTC

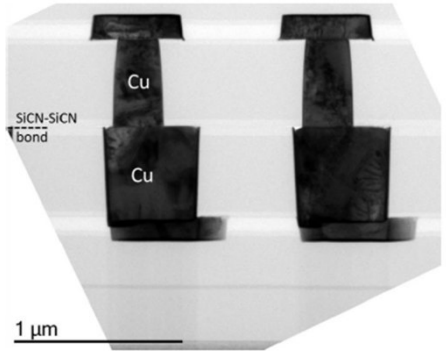




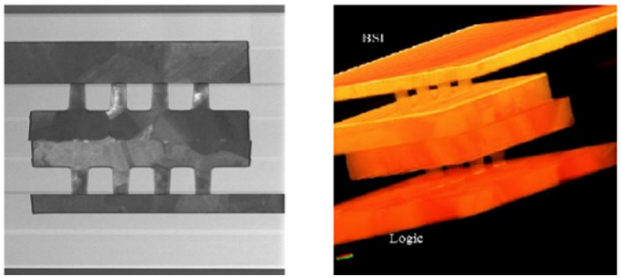
Source: TechInsights memory technology update from IEDM18, Apr 2019

Hybrid bonding I Specification

Parameter	Value
Surface Micro roughness	< 0,5 nm Ideal < 0,3 nm
Incoming Wafer Bow	≤ 30 µm *400 µm
Wafer TTV	< 3µm
Dielectric Material	SiO_2 , SiC_xN_y , SiO_xN_y
Pad shape	Square
Top / Bottom Pad size ratio	1:1 or 1:2*
Pad size	> 500 nm x 500 nm
Cu dishing	2 - 4 nm
Cu Pad shape	a, Dishing Top/Bottom Wafer b, Protrusion Top Wafer & dishing bottom Wafer
Pitch	1 µm / >1 µm
Cu Pad density	< 25%
Particle	< 50 particles @ 90nm size
Organic Residues	No
Post annealing Temperature	200°C – 400°C



TEM hybrid Cu/SiCN to Cu/SiCN bonding, Top Cu pads are 270nm and bottom ones are 540nm with 1.08 µm pitch.
Courtesy of IMEC; Peng et.al.; IITC 2018

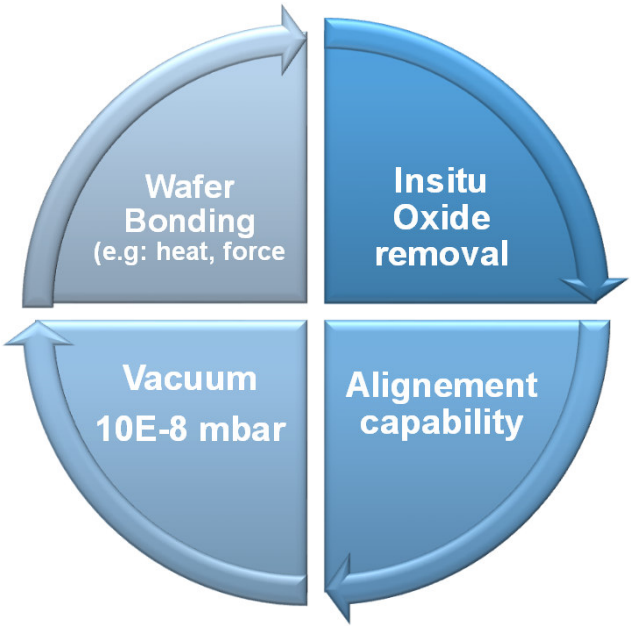


Courtesy of ST / CEA LETI (Polis Project); Lhostis et.al.; Proc. IEEE ECTC, 2016

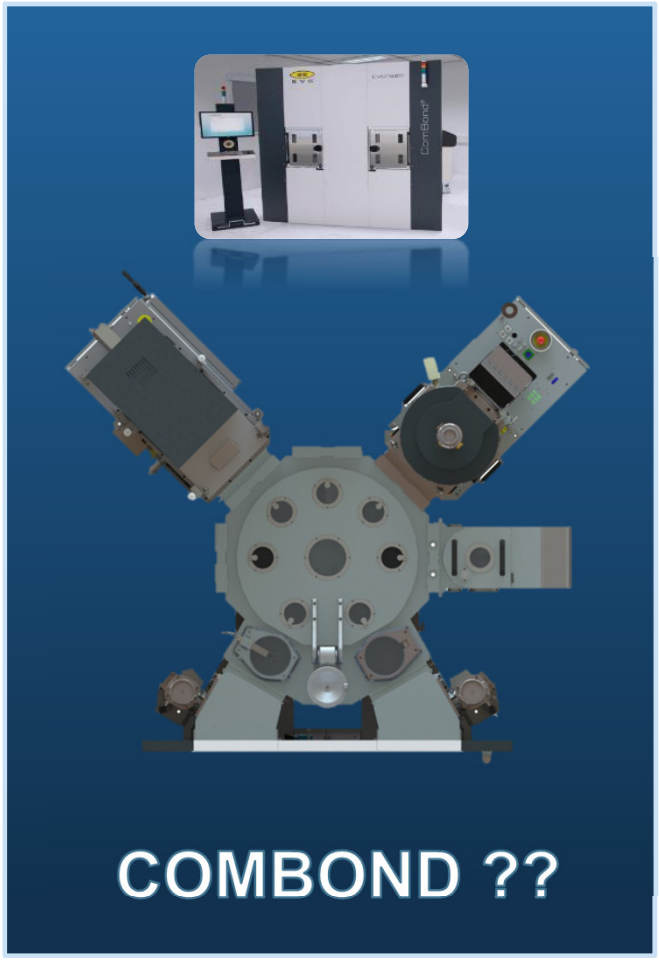
ComBond
Oxide free / Conductive bonding interface

Motivation I ComBond Technology

Process Capabilities



Conductive bonding interface : thermal, electrical, optical.

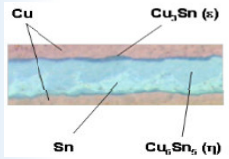


Supported Processes

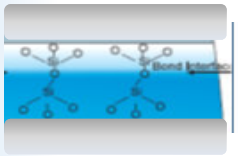
Thermo Compression Bonding

Eutectic Bonding

TLP Bonding

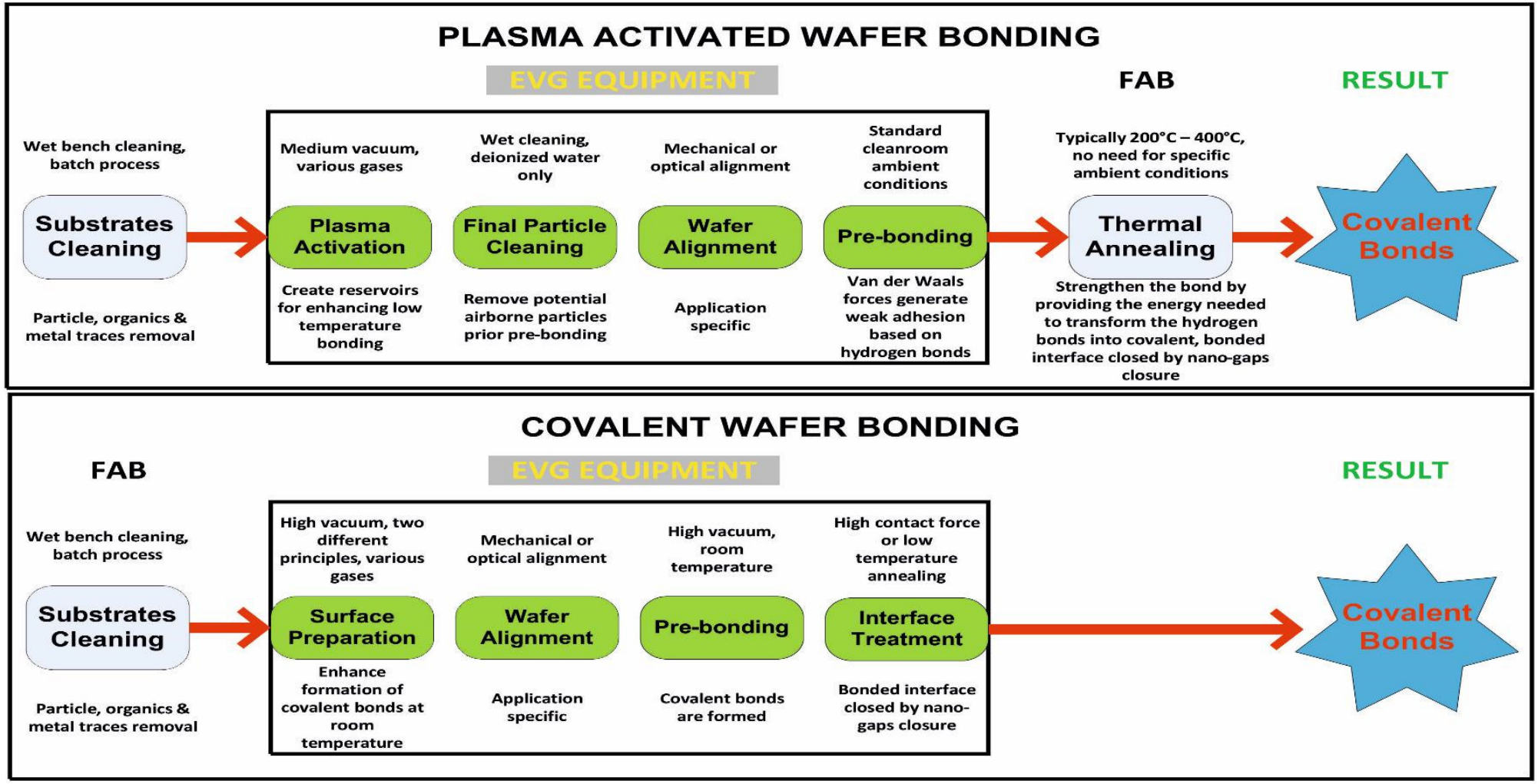


Direct (Covalent) Bonding

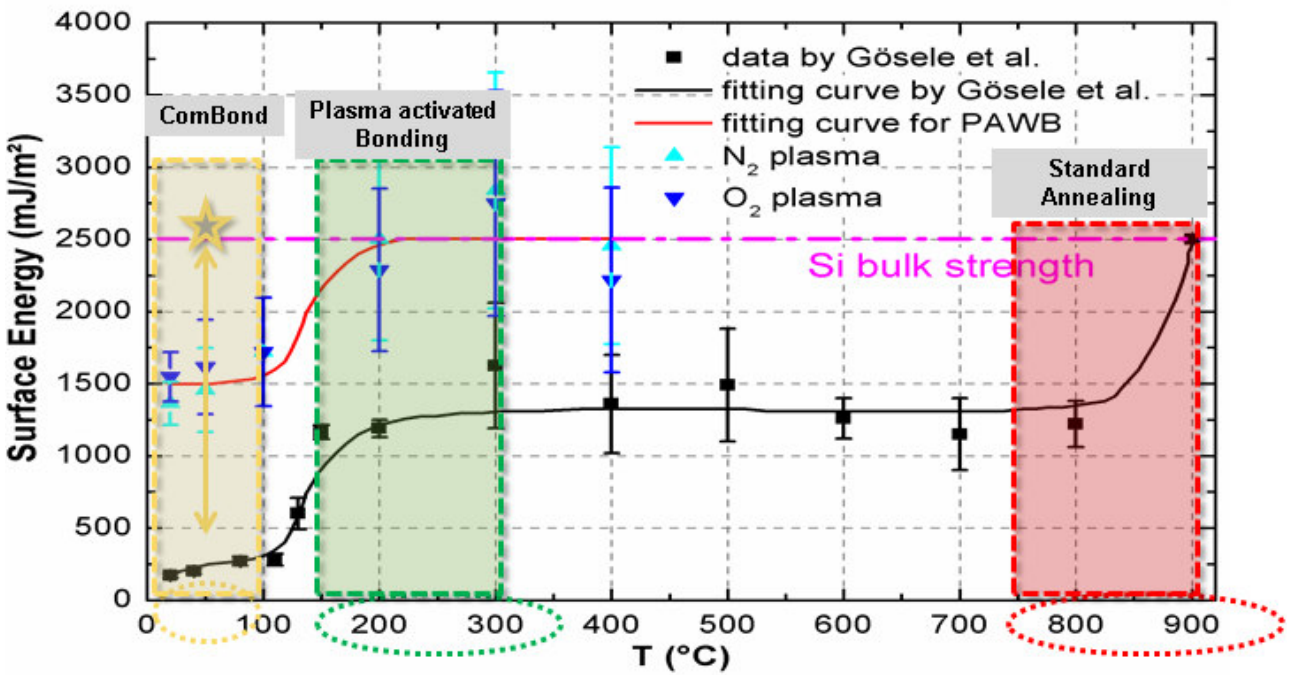


Method Comparison I

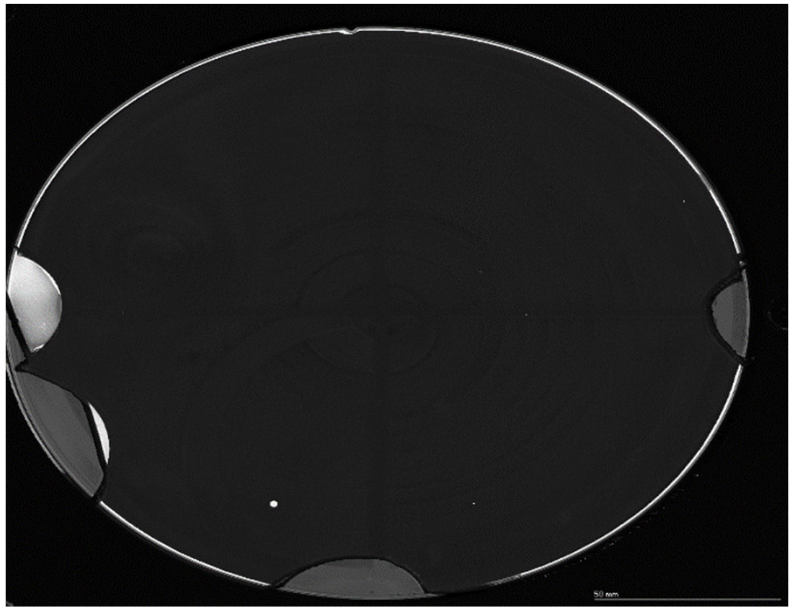
Plasma activated direct bonding vs. ComBOND



Bonding Energy I ComBond® vs. Plasma activated Fusion Bonding vs. Fusion Bonding



C-SAM scan

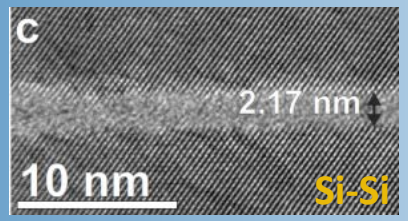


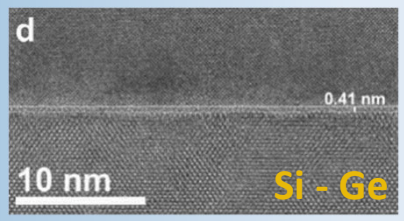
Bond strength > 2.5 J/m² (all measurement positions broken)

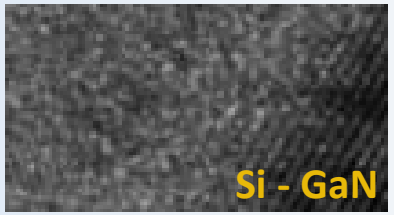
ComBond | Substrate Combination Overview

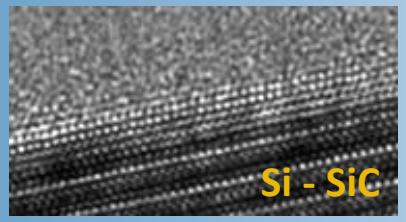
Bonding Materials	
Si (100)	Si (100)
	Sapphire
	GaN
	Ge
	$LiNbO_3$
	$LiTaO_3$
	Mo
	Si_xN_y
Si (111)	Si (100)
	Si (111)
$Si(SiO_2)$	Si
	$Si(SiO_2)$
SiC (4H)	Si
	SiC (4H)
	Poly-SiC
Poly-SiC	Poly-SiC
GaAs	InP
	Si
	SiC
Au	Au
Cu	Cu
Al	Al

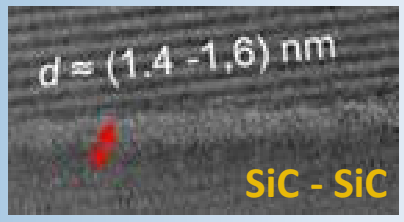
Examples of materials combinations successfully tested

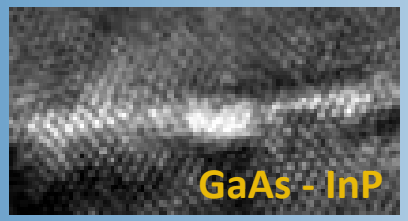


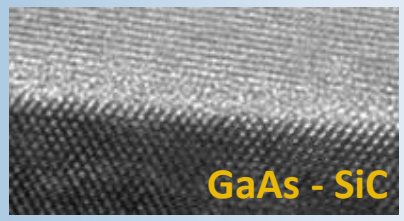


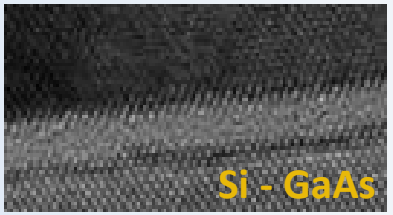


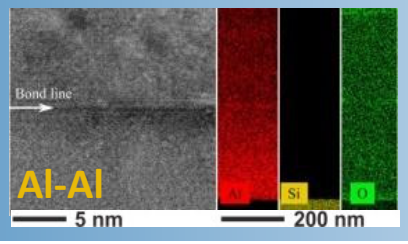


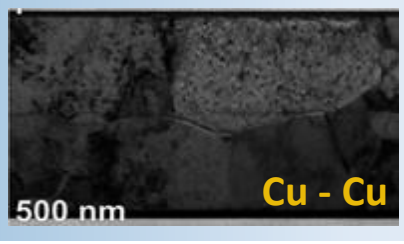




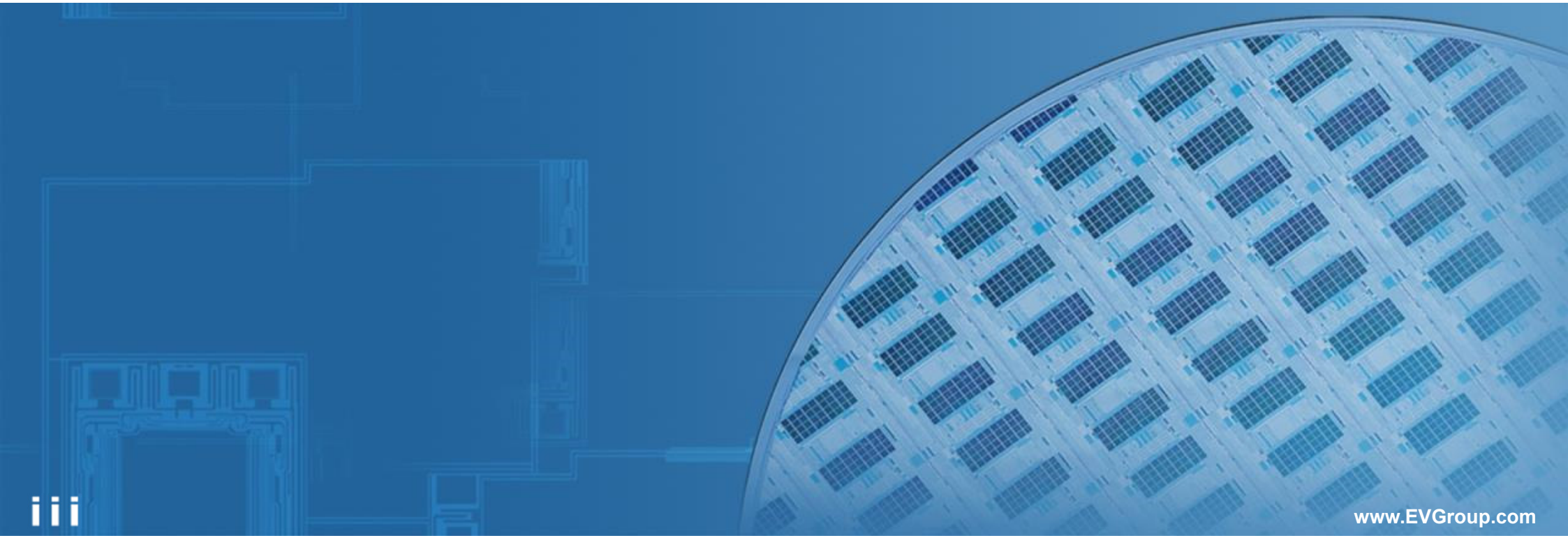






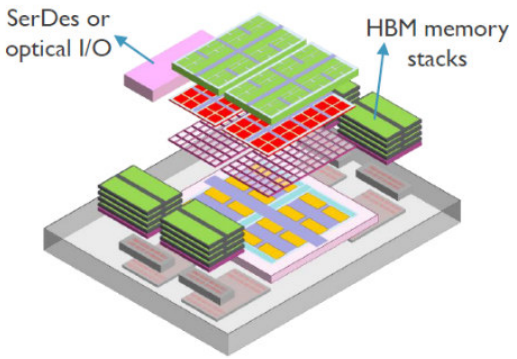


Wafer to Wafer vs. C2W vs. collective Die placement



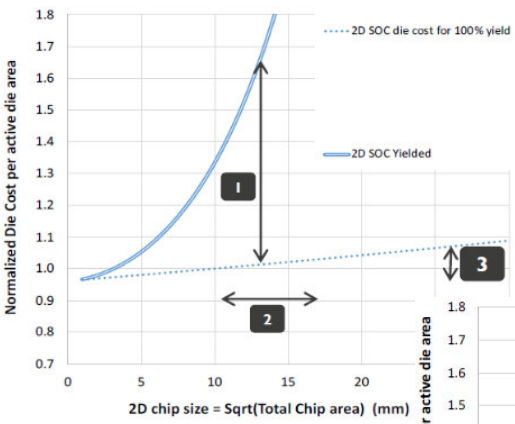
Die to Wafer vs. Wafer to Wafer integration

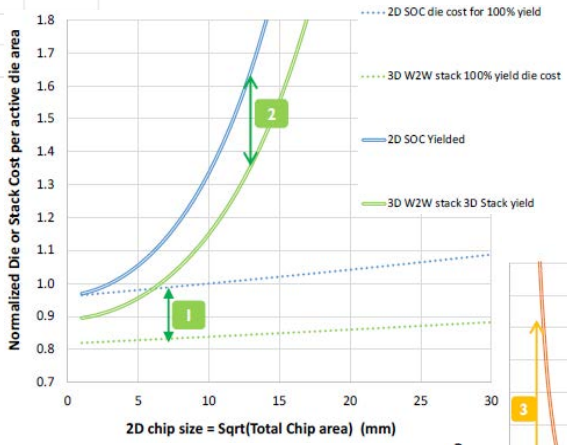
High Performance Device

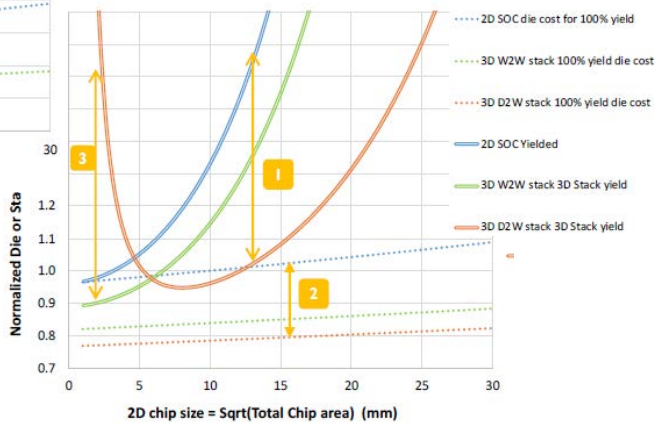


High performance systems require large die size
Lower yield for higher advanced nods

→ *High system integration costs*







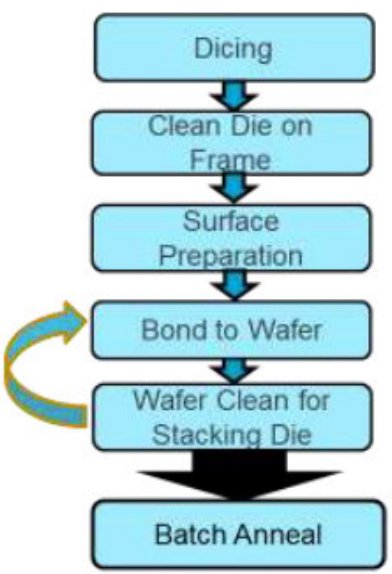
The bigger the die size the more favorable and cost effective it is to use D2W stacking (KGD)

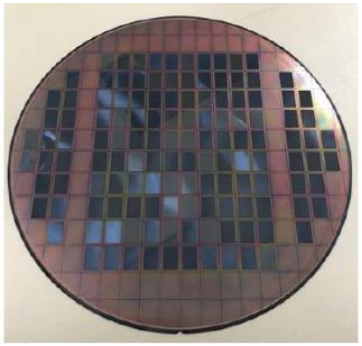
KGD strategy strongly improves compound yield
Cost reduction by cost differentiation technologies
C2W not effective for small die: W2W lower cost

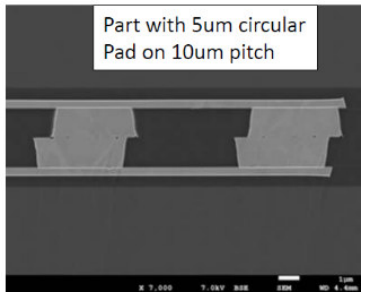
Source: IMEC – 2019 3D & systems summit

Die to Wafer Hybrid bonding | Status

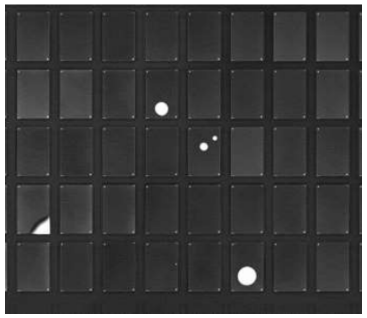
Current capabilities



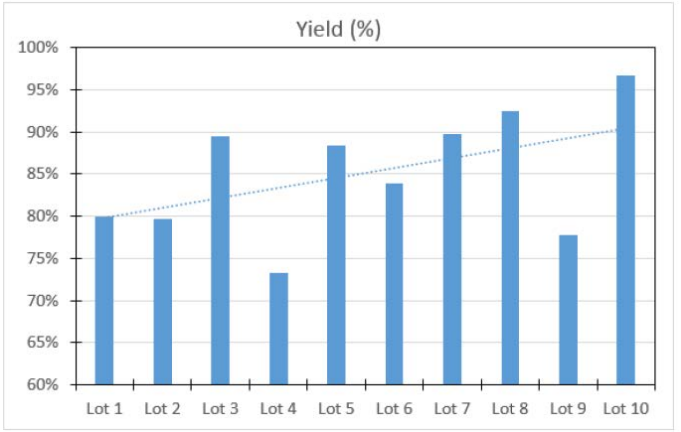




Challenge – Yield



Scanning Acoustic Microscope image



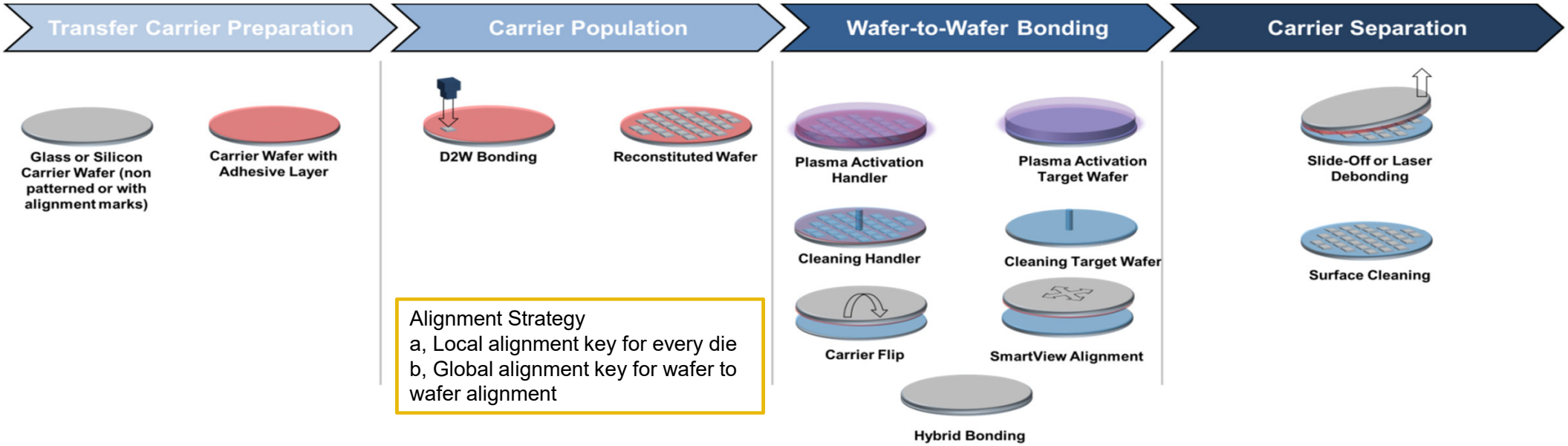
Yield issue

Surface contamination (organic, particle)

Process feasibility proven → yield challenge → collective Die carrier

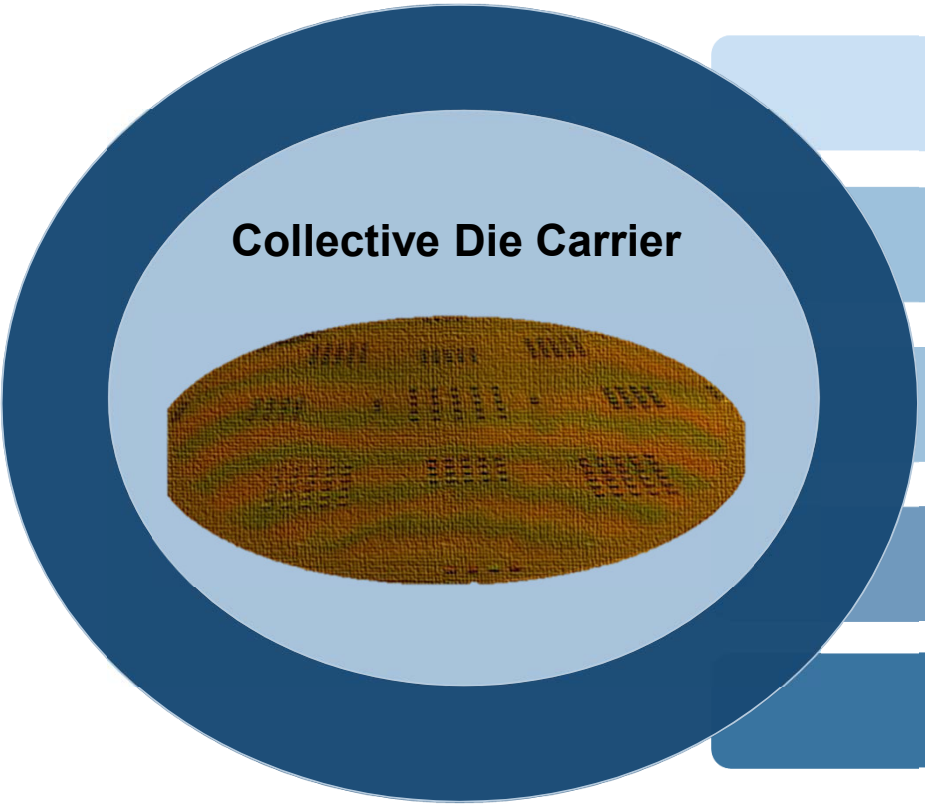
Source: Xperi - 2018 IEEE 68th Electronic Components and Technology

Collective Die Carrier | Process Flow

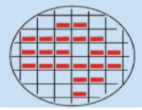


Transfer Method	Pro's	Con's	Maturity Level
Collective Die Transfer by Reconstituted Carrier	• Proven technology • Die activation and cleaning equivalent to W2W hybrid bonding • Oxide management • Reuse of carrier feasible	• Error propagation of D2W + W2W alignment • Cost of carrier prep, utilization and clean • Die thickness needs to be in narrow range	High Volume production proven for several years

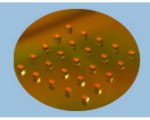
Die to Wafer Hybrid bonding
Collective Die Carrier | Overcome Yield challenge



Enables Wafer level processing
minimized risk of contamination



Enhanced oxide management
no Q-time impact, improved oxide management



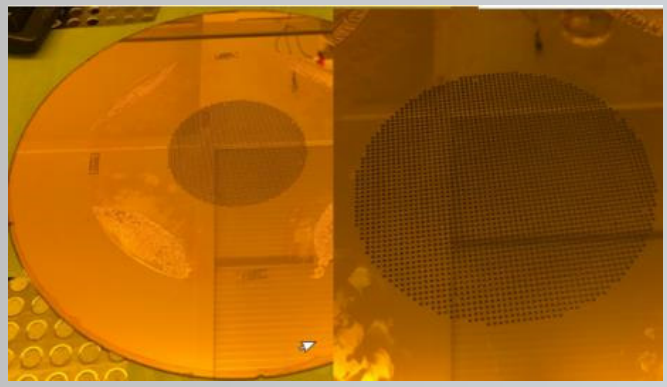
Compatible with standard wafer processing Equipment
post processing is performed at Wafer level

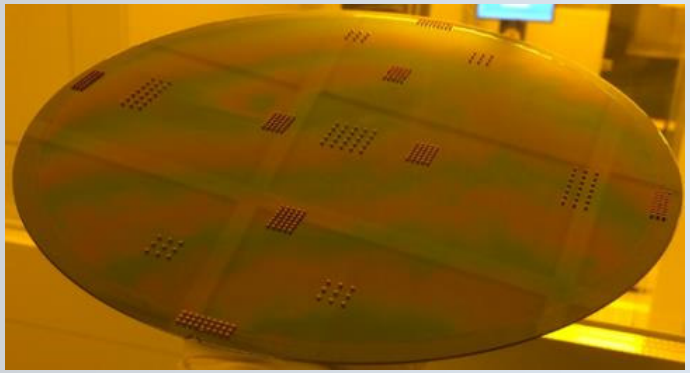
Die placement accuracy
mainly limited by die placement accuracy of the die bonder

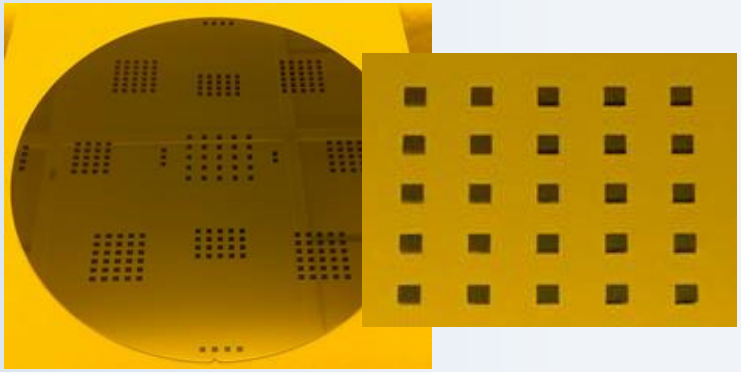
Compatible with multiple bonding technologies
Hybrid Bonding, Thermo compression, eutectic bonding, adhesive bonding

Collective Die Transfer - Bonding Results

Collective Die Transfer | Bonding Results

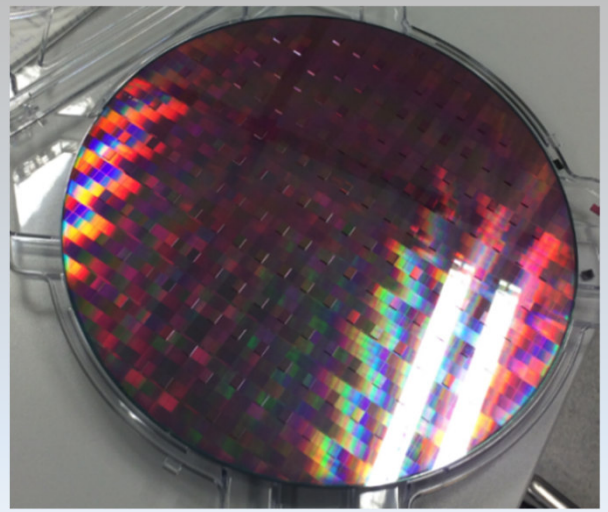




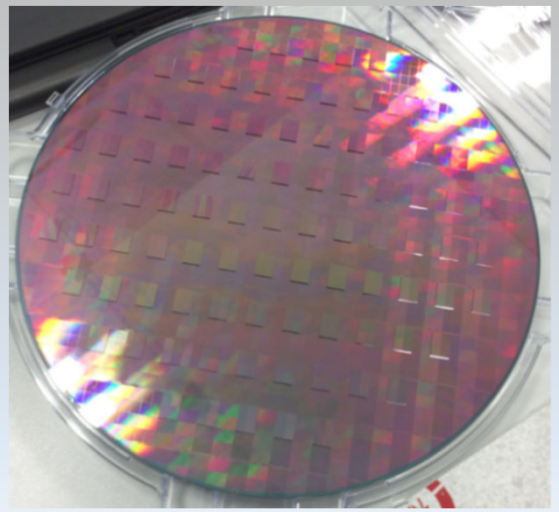


- **GaAs & GaN die transfer using Cu-Cu bonding process**
  - Die size: 800µm x 800µm
  - Transfer-rate: 100%
  - Total: 1500 Dies
- **Si die transfer using adhesive (BCB) bonding process**
  - Die size: 800µm x 800µm
  - Transfer-rate: 100%
  - Total: 420 Dies
- **SiO_2 die transfer using direct bonding**
  - Die size: 1000µm x 1000µm
  - Transfer-rate: >98%
  - Total: 185 Dies

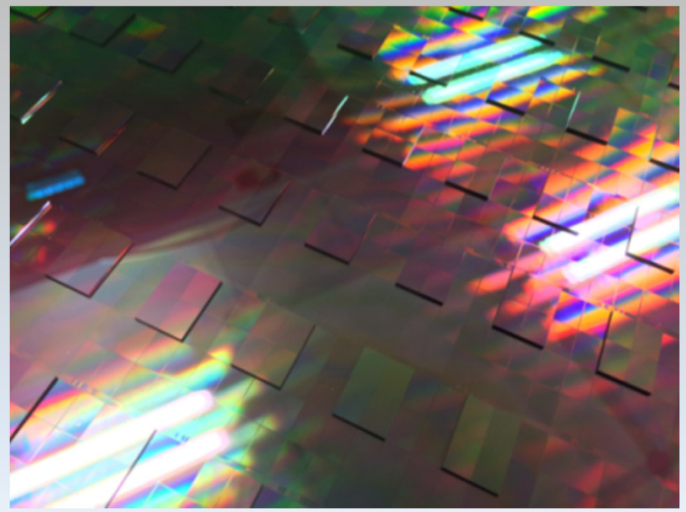
Collective Die Transfer | Hybrid Bonding

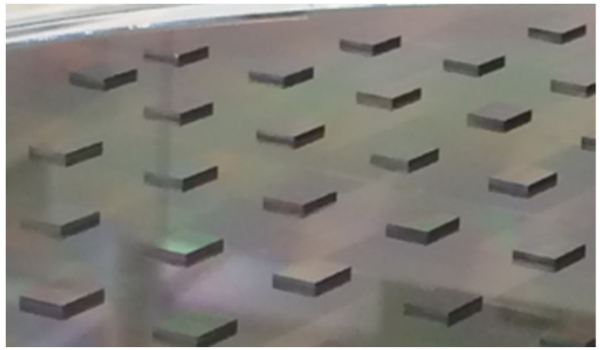


Demonstrator A - 300mm
Hybrid Bonding, 5 mm x 7 mm



Demonstrator B - 300mm
Hybrid Bonding,10 mm x 14 mm



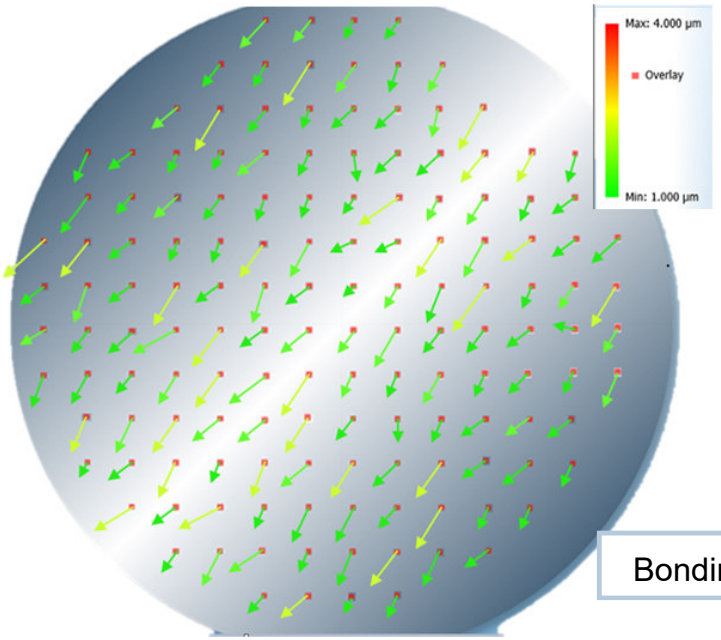


→ Pad Size 4 µm – 1 µm

→ Pitch 8,8 µm – 2 µm

Collective Die Transfer | Hybrid Bonding - Placement Accuracy

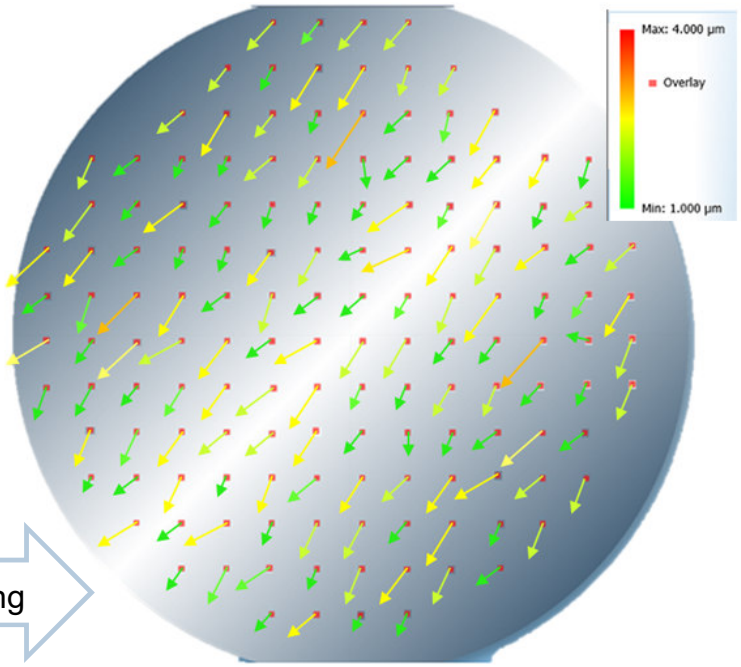
Die placement accuracy prior to bonding



EVG40NT Die placement accuracy map prior to bonding

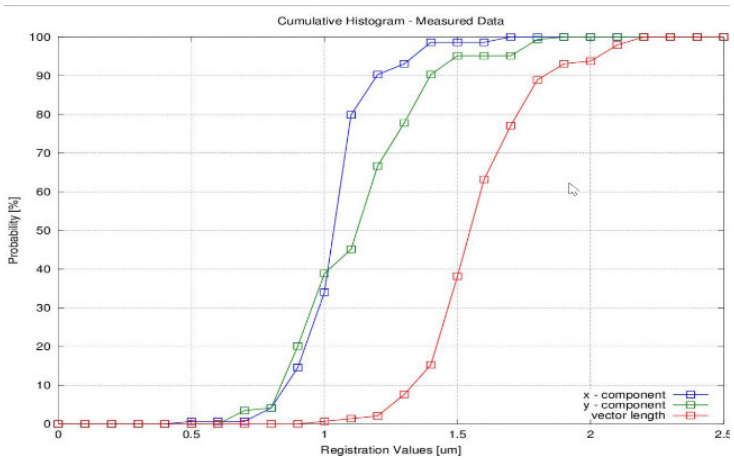
Bonding

Die placement accuracy post bonding



EVG40NT Die placement accuracy map post bonding

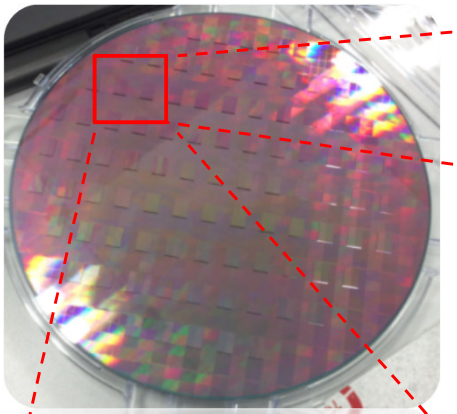
Post Bond Alignment accuracy Cumulative Plot



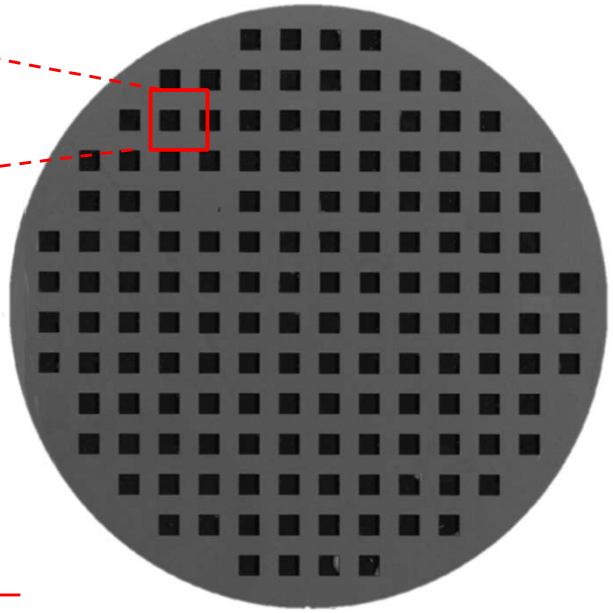
Post bond die transfer placement accuracy of ≤ 2 µm for 95% of the dies could be demonstrated using collective die carrier process.

SAM/TEM analyses of transferred Die – Hybrid Bonding

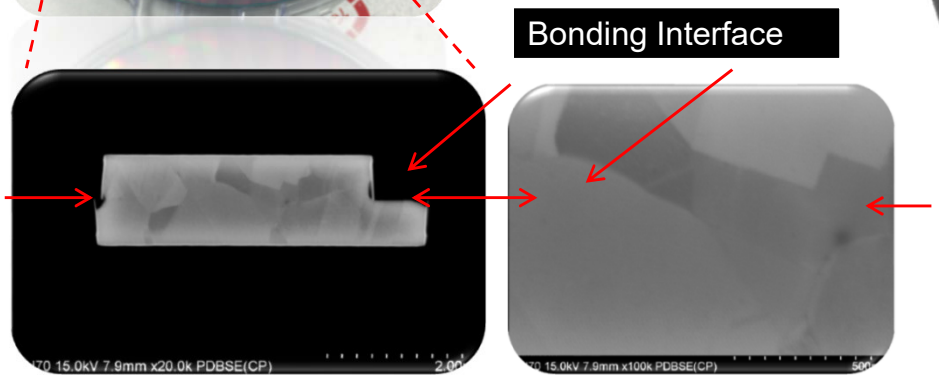
Bonding Process	Die Substrate Material	Die Dimension	Target Substrate Material	Bonding Interface	Bonding Parameter
Hybrid Bonding	Silicon	15 mm x 7 mm	Silicon	CuCu & SiO2/SiO2	RT



Scanning Acoustic Microscope Image post transfer - close up



Scanning Acoustic Microscope Image post



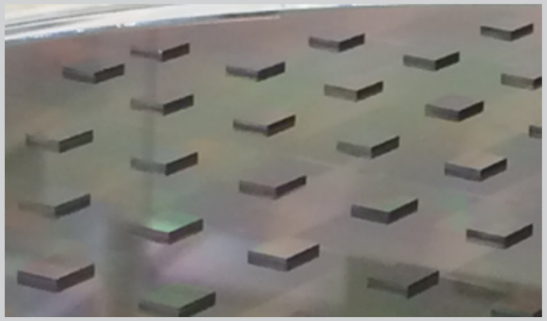
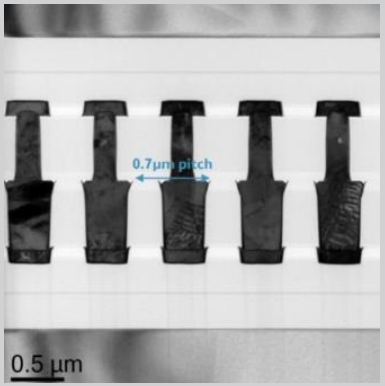
TEM Cross section Image – post Die Transfer

High transfer yield including high bonding quality based on Scanning Acoustic microscope images and TEM analyses could be demonstrated after final annealing.

TEM analyses showed Cu grain recrystallization over the bonding interface.

Protection layer removal and die preparation prior to bonding have been identified as most critical process steps for high transfer yield.

Summary | D2W vs. W2W Technolgoy

	D2W Hybrid Bonding	W2W Hybrid Bonding
Status	• Technology building blocks are proven • Proven technology • Die Activation and cleaning equivalent from W2W hybrid bonding • Oxide management • Rework on carrier feasible 	• Proven High Volume Technology • Wafer activation, wafer cleaning and oxide management are proven to work 24/7 in high volume with highest interconnect yield • Wafer to wafer overlay of <100nm proven 

EVG's Vision & Mission in Markets Driven by Global Megatrends

Mobiles, AR/ VR, Sensing

Wireless Infrastructure

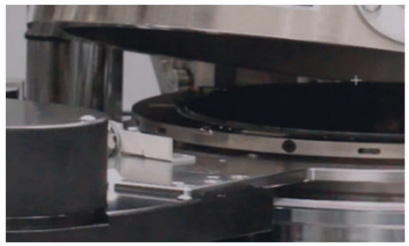
Big Data, IoT

HPC, AI, Quantum

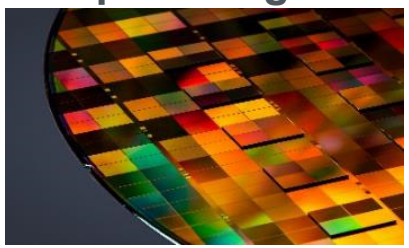
Consumer — Mission Critical Applications

EVG Contributions

Bonding Technology

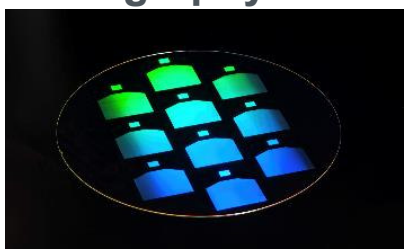


Heterogeneous & Chiplet Integration

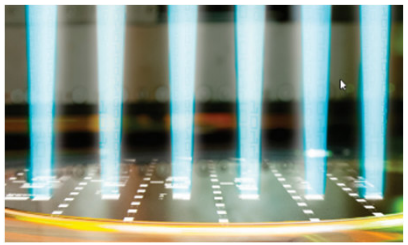


Temporary Bond/ De-Bonding

Nano – Imprint Lithography



Digital Maskless Lithography



Field Proven High Volume Manufacturing Technologies

Thank You for Your Attention!

Contact person:
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