Package Technology, Design, and Methodology Challenges and Solutions for High Bandwidth Electronics Systems

Kemal Aygün
Intel Corporation
August 19, 2021
Outline

• Introduction
• ‘Advanced’ Packaging Technologies
• Challenges for Electrical Analysis & Design
• Summary
Outline

• Introduction
• Advanced Packaging Technologies
• Challenges for Electrical Analysis & Design
• Summary
The Age of Data (...before the ‘Real’ Age of Data)

Global Data Creation is About to Explode
Actual and forecast amount of data created worldwide 2010-2035 (in zettabytes)

Source: Statista Digital Economy Compass 2019

New data revealed that users flocked to streaming platforms in massive numbers last year as the COVID-19 pandemic took hold — with the entertainment giant one of the biggest beneficiaries. According to a new report from mobile analytics and market data company App Annie, time spent on video streaming apps on Android phones hit 935 billion hours in 2020 — a 40% increase from 2019 levels.

New Opportunities ‘and’ Challenges with 5G, IoT, & AI

Source: intel.com

Source: habana.ai
Network connectivity roadmaps are showing 200 Gb/s as the next target for per-lane SERDES speed.

→ Significant challenge for package and system design!
Memory Bandwidth Scaling

- Memory bandwidth has been scaling both in terms of signaling rates and number of connections.

→ Significant challenge for package and system design!
Heterogeneous Integration

**PCB Integration**
- Limited Interconnect Density → Limited BW
- Long Interconnects → Increased Power
- Large Form Factor

**On-Package Integration**
- Lower Power
- Higher Bandwidth
- Heterogeneous Integration of Multiple Nodes, Multiple IP, & Multiple Functions

→ Significant challenge for package technologies and package design!
Outline

• Introduction
• Advanced Packaging Technologies
• Challenges for Electrical Analysis & Design
• Summary
What is a (Electronic) Package?

• Package provides the connectivity and the space transformation between the die and the motherboard. It is also responsible for:
  → Maintaining fidelity of high speed signals (signal integrity), supplying adequate power (power delivery), and minimizing electromagnetic interference (EMI/EMC)
  → Helping with heat dissipation from the die and providing mechanical stability
Examples of Advanced Packaging

- **Embedded Multi-die Interconnect (EMIB)**
  - bump pitch: 50-40 microns
  - leads industry
  - first 2.5D embedded bridge solution
  - products shipping since 2017

- **Foveros Technology**
  - bump pitch: 50-36 microns
  - wafer-level packaging capabilities
  - first-of-its-kind 3D stacking solution

- **Foveros Omni**
  - bump pitch: ~25 microns
  - next gen Foveros technology
  - unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

- **Foveros Direct**
  - bump pitch: < 10 microns
  - direct copper-to-copper bonding for low resistance interconnects
  - blurs the boundary between where the wafer ends and the package begins

Source: intel.com

**Terms you can hear:**

FCBGA, FCLGA, FCCSP, WLCSP, FOWLP, PLP, eWLP, MCP, MCM, FO-MCM, SiP, EMIB, Co-EMIB, Foveros, Fovers OMNI, Foveros Direct, ...
Motivation

- To enable high bandwidth density connection between dies on a package with simple I/O circuits and low power consumption → Works for ‘short’ lengths!
- We also need advanced packaging features such as very low loss materials, smooth copper, appropriate design rules, etc., for longer reach applications

Si Interposer Example

(Reproduced with permission of W. Beyene)
Si Bridge Example

‘More’ Advanced Packaging Example: Co-EMIB

- Architecture to enable reticle sized base die & high-density bridge links to companion dies, increased partitioning opportunities
- Results in more challenges in design and analysis
Additional Reading

Heterogeneous Integration Roadmap 2020 Edition

Interested in hearing the latest updates and news on the Heterogeneous Integration Roadmap? Please sign up.

Chapter 2: High Performance Computing
Chapter 3: Internet of Things (IoT)
Chapter 4: Medical, Health and Wearables
Chapter 5: Automotive
Chapter 6: Aerospace and Defense
Chapter 11: MEMS and Sensor Integration
Chapter 12: Co-design for Heterogeneous Integration
Chapter 14: Modeling and Simulation

Outline

• Introduction
• Advanced Packaging Technologies
• Challenges for Electrical Analysis & Design
• Summary
Package Modeling and Characterization Challenges

• As data rates increase and margins decrease, new phenomena that were insignificant in the past designs become significant
  – Frequency dependence of resistance losses and inductance for conductors
  – Non-ideal effects of the copper surface
  – Frequency dependence of dielectric permittivity and loss tangent
  – *New geometrical scales with new materials and processes*

• We need *validated models* that accurately predict these effects
Package Modeling-to-Measurement Correlation

- Comprehensive flow for an improved package modeling and correlation methodology is essential for efficient electrical design

With good dielectric, conductor, surface roughness models and a robust modeling methodology and tool, we can create accurate electrical models.
Impact of Environmental Conditions

Capturing impact of environmental conditions requires a temperature and humidity dependent modeling and characterization flow.

Impact of Environmental Conditions


- Temperature dependent material properties and surface roughness models help further improve measurement to modeling correlation quality

\[ K_{H}^{\text{new}}(T, \delta, sr, a) = 1 + \frac{3}{2} sr \left( 1 + \frac{\delta}{a} + \frac{\delta^2}{2a^2} \right)^{-1} + c_1(T-T_0)e^{-c_2\delta} \]
Impact of Measurement Uncertainties

• Generating high-fidelity package electrical models requires precise modeling & measurement methods, environmental control, and understanding of uncertainties for each measurement.

Accurate Signal Net Modeling for 2.xD Packages

• Novel Fine features in 2.xD packages require new interconnect modeling methodologies

2.xD Packaging Electrical Analysis Methodology

- Accurate signal channel modeling
- Unique power delivery network modeling
- Unified framework for SIPI co-simulation

Electrical analysis challenges of 2.xD packaging technologies range from extraction of very fines features to SIPI co-simulation which requires advanced modeling methodologies.
Modeling for Product Design: Full-Package Example

• A typical product package can have:
  – 30x30 to > 50x50 mm form factor
  – 4-20+ layers
  – Hundreds or more IO nets/traces
  – 10s of distinct power delivery planes/shapes
  – >10k die bumps (FLI connections)
  – Few hundred to few thousand package balls/pads/pins
  – Dimensions range from few microns to ~1 mm

• May also need to include connectors and sockets

• Analysis of a realistic full-package is expected to result in 10s of millions of unknowns with varying length scales and material properties, AND hundreds of ports
• For practical purposes, this is an unsolved problem that has resulted in sub-optimal final designs, driven by long simulation times and/or limited simulation domains
Full-Wave Analysis of a Full-Package – An Example

Reduced-domain layered-medium integral-equation* model for a full-package

Full-wave Analysis of a Full-Package – An Example

- Full-wave analysis of a package enables new package design optimization opportunities

Reproduced with permission of Prof. A. Yilmaz from UT Austin

28 GHz
Application of Machine Learning – An Example


- Emerging machine-learning algorithms for package modeling and design optimization
IEEE EPS TC-EDMS Packaging Benchmarking Suite

https://packaging-benchmarks.org/

• Benchmark problems can help research community with new methods and tools
IEEE EPS Conferences

- Multiple IEEE EPS conferences focused on electrical analysis of packaging and systems

http://www.epeps.org/
https://www.linkedin.com/groups/86343/

https://spi2021.uni-siegen.de/

http://www.edaps.org/
Summary

• Semiconductor packaging is experiencing an accelerated pace of innovation fueled by emerging electronic system connectivity and heterogeneous integration demands

• Novel advanced packaging architectures provide new opportunities to improve package electrical design for short reach interconnects

• These new technologies need to include features to enable also long reach interconnects

• Validated modeling methodologies & collaterals are key for both existing and emerging package and system designs

• Emerging modeling tools have to address modeling fidelity including new dimensions and materials, algorithm capability, and scalability simultaneously to solve connectivity problems of future