Package Technology, Design, and Methodology Challenges and Solutions for High Bandwidth Electronics Systems

Kemal Aygün

Intel Corporation

August 19, 2021

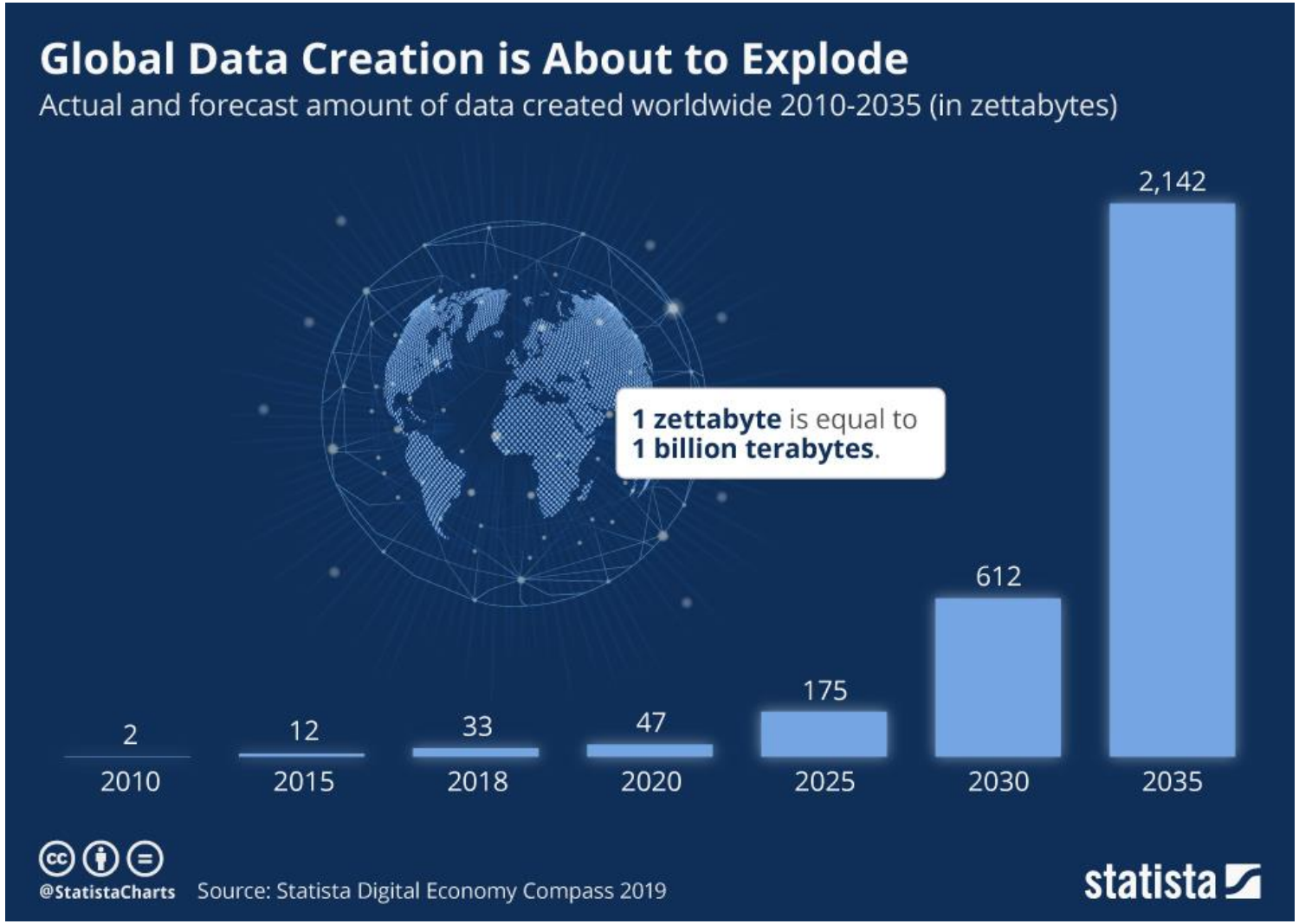
Outline

- Introduction
- ‘Advanced’ Packaging Technologies
- Challenges for Electrical Analysis & Design
- Summary

Outline

- Introduction
- Advanced Packaging Technologies
- Challenges for Electrical Analysis & Design
- Summary

The Age of Data (…before the 'Real' Age of Data)

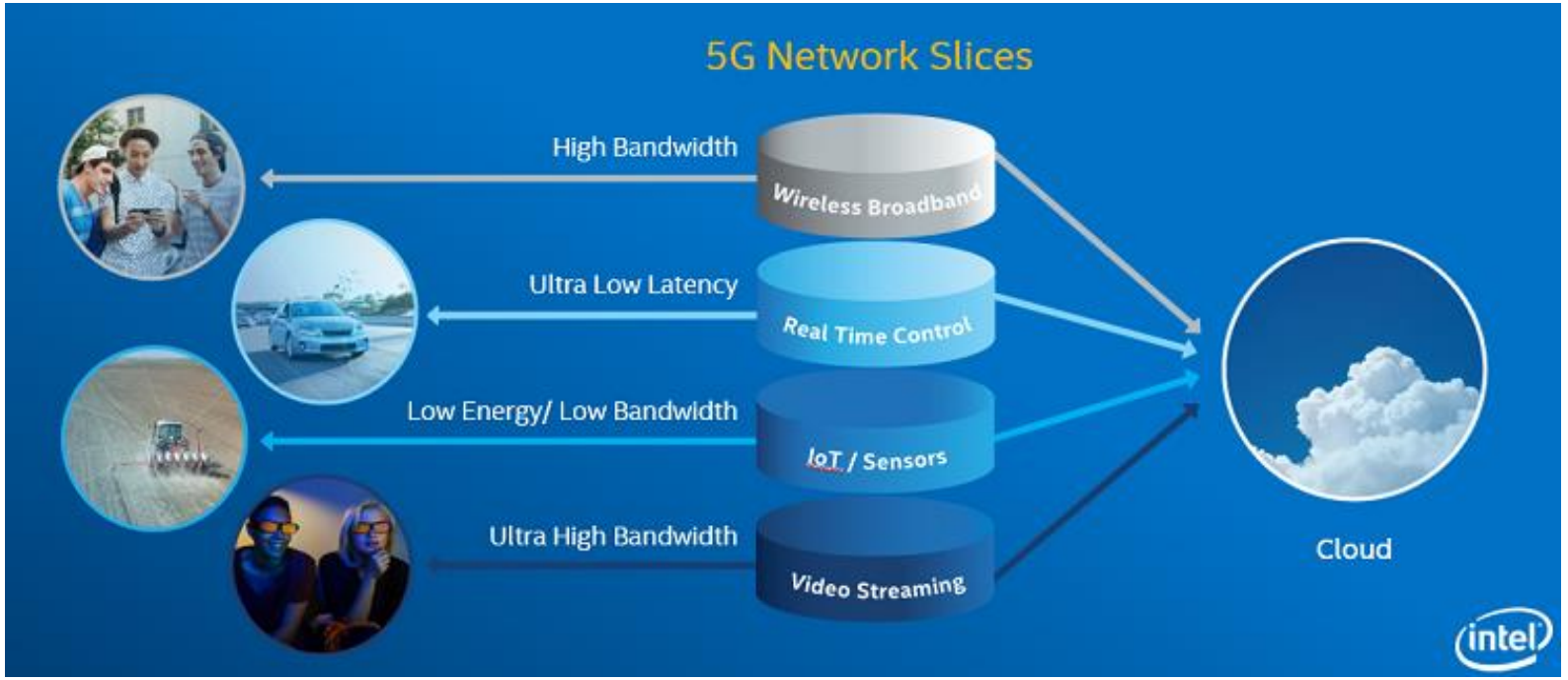


https://www.statista.com/chart/17727/global-data-creation-forecasts/

yahoo!finance

New data revealed that users flocked to streaming platforms in massive numbers last year as the COVID-19 pandemic took hold — with the entertainment giant one of the biggest beneficiaries. According to a new report from mobile analytics and market data company App Annie, time spent on video streaming apps on Android phones hit 935 billion hours in 2020 — a 40% increase from 2019 levels.

New Opportunities ‘and’ Challenges with 5G, IoT, & AI



Source: habana.ai

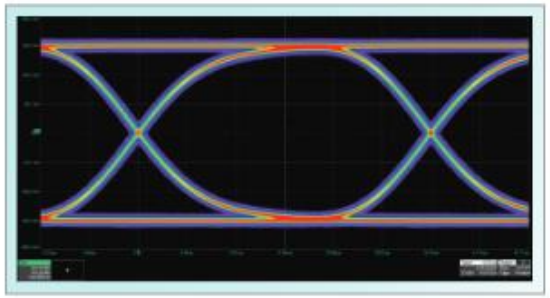
Source: intel.com

System/Network Connectivity Scaling

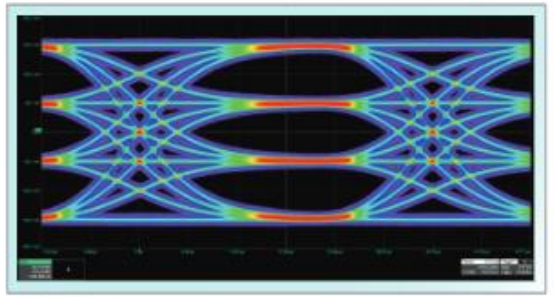
Reproduced with permission from Ethernet Alliance

ethernet alliance

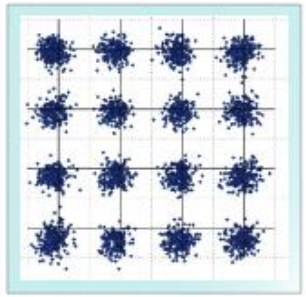
Emerging signaling methods



NRZ



PAM-4

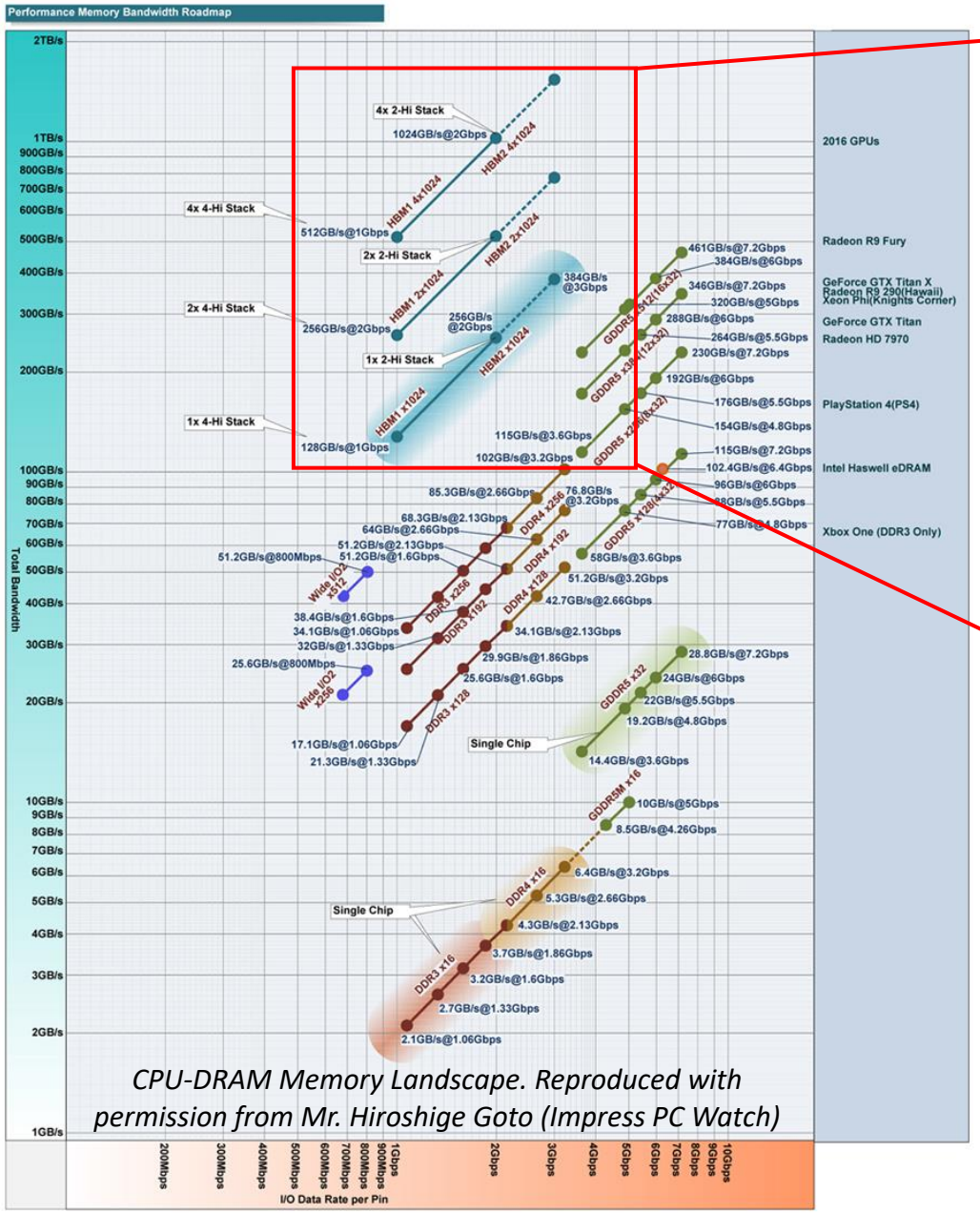


Coherent

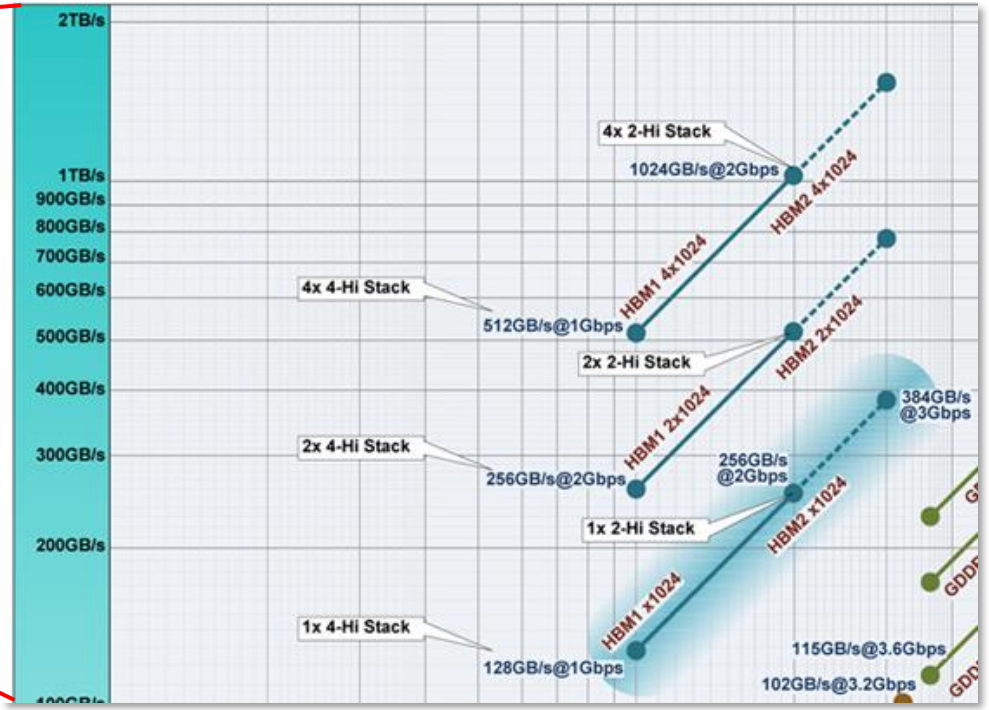
- Network connectivity roadmaps are showing 200 Gb/s as the next target for per-lane SERDES speed

  → Significant challenge for package and system design!

Memory Bandwidth Scaling



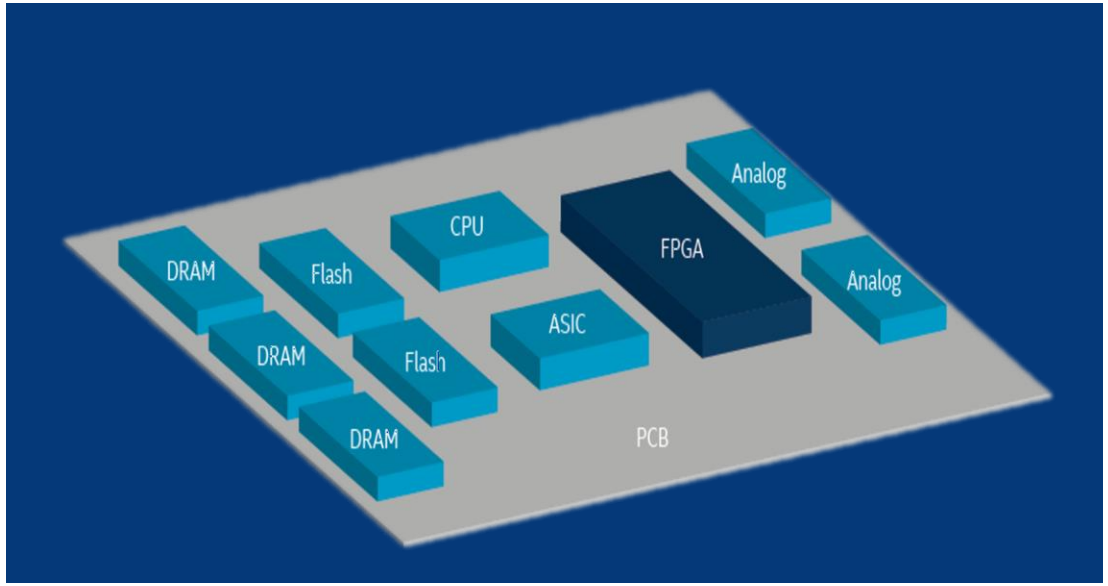
CPU-DRAM Memory Landscape. Reproduced with permission from Mr. Hiroshige Goto (Impress PC Watch)

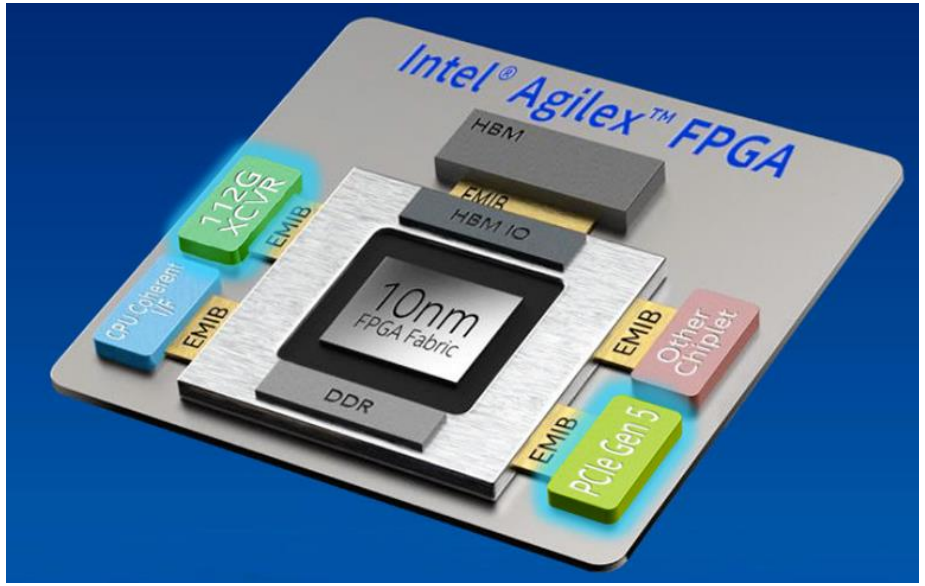


- Memory bandwidth has been scaling both in terms of signaling rates and number of connections

  → Significant challenge for package and system design!

Heterogeneous Integration





PCB Integration

- Limited Interconnect Density → Limited BW
- Long Interconnects → Increased Power
- Large Form Factor

On-Package Integration

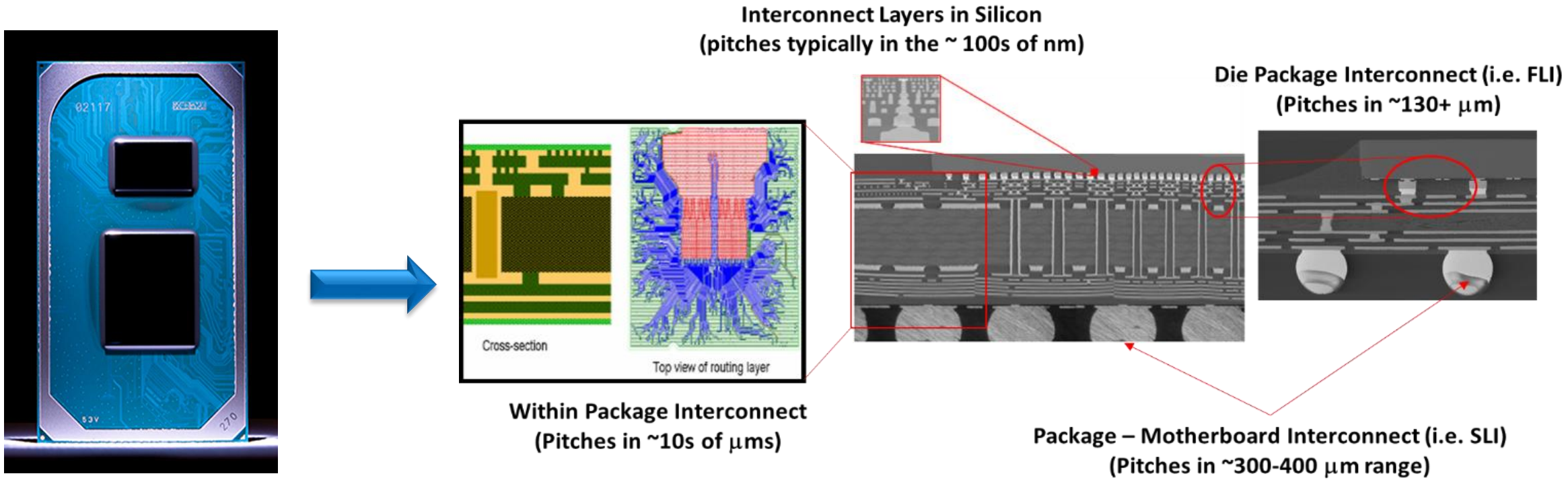
- Lower Power
- Higher Bandwidth
- Heterogeneous Integration of Multiple Nodes, Multiple IP, & Multiple Functions

→ Significant challenge for package technologies and package design!

Outline

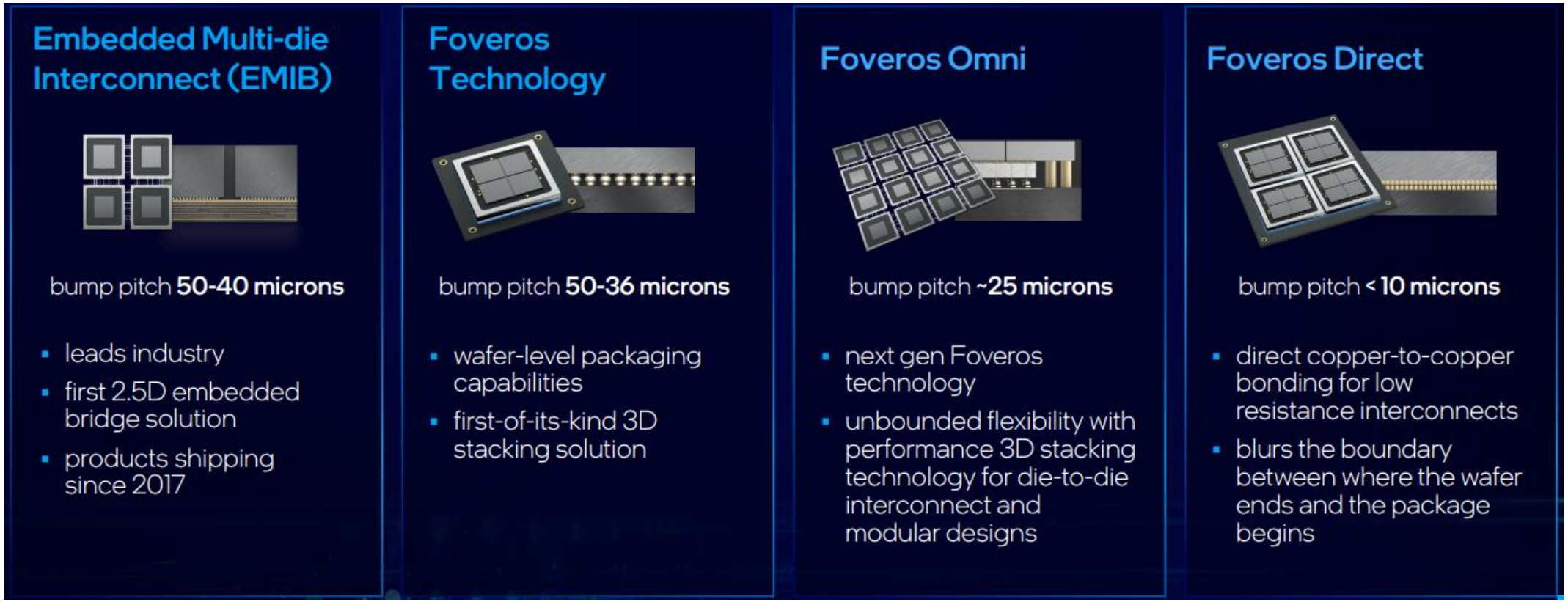
- Introduction
- Advanced Packaging Technologies
- Challenges for Electrical Analysis & Design
- Summary

What is a (Electronic) Package?



- Package provides the connectivity and the space transformation between the die and the motherboard. It is also responsible for:
  - → Maintaining fidelity of high speed signals (signal integrity), supplying adequate power (power delivery), and minimizing electromagnetic interference (EMI/EMC)
  - → Helping with heat dissipation from the die and providing mechanical stability

Examples of Advanced Packaging



Source: intel.com

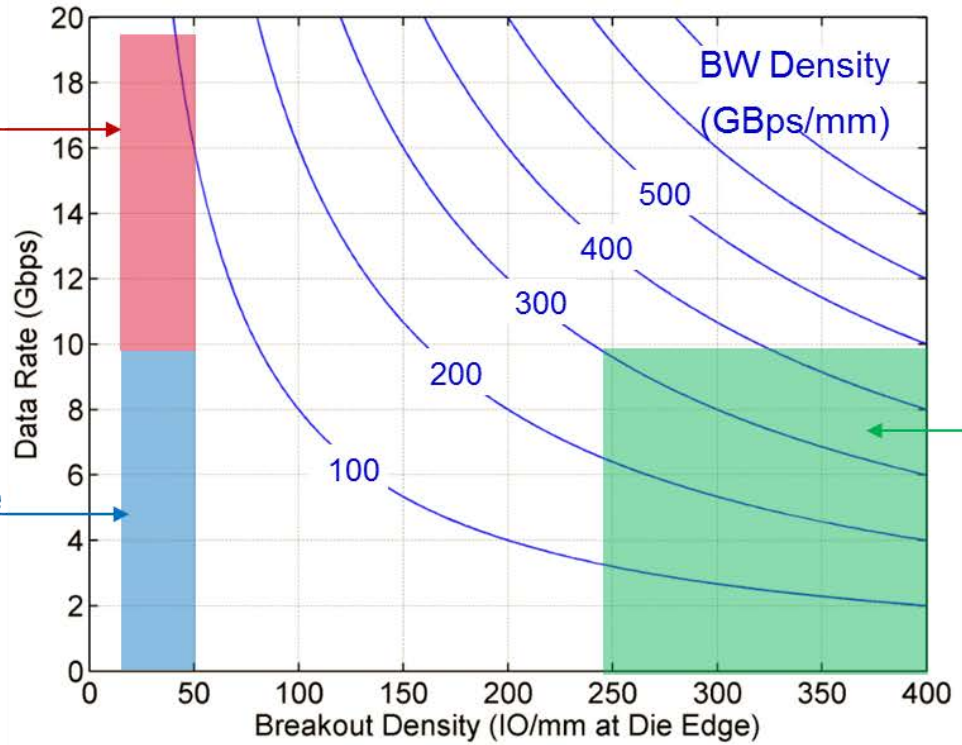
Terms you can hear:

FCBGA, FCLGA, FCCSP, WLCSP, FOWLP, PLP, eWLP, MCP, MCM, FO-MCM, SiP, EMIB, Co-EMIB, Foveros, Fovers OMNI, Foveros Direct, …

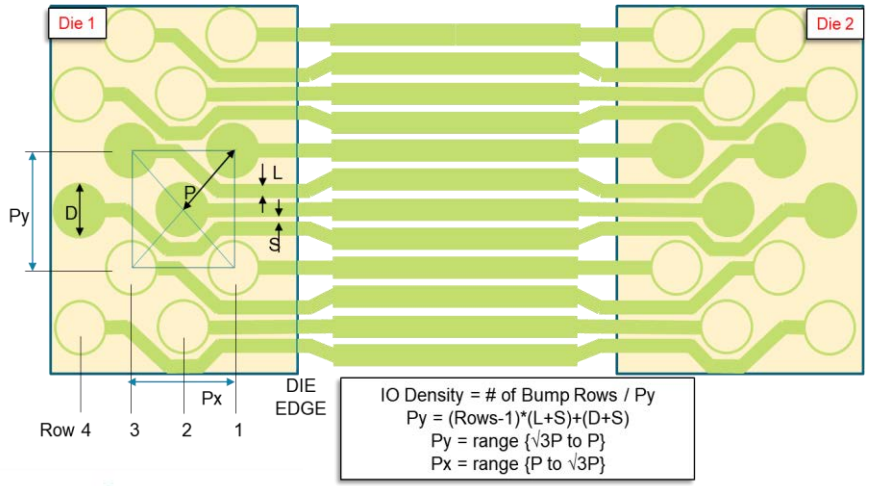
Motivation

More and more complicated I/O circuits

Organic substrate with very low bandwidth density



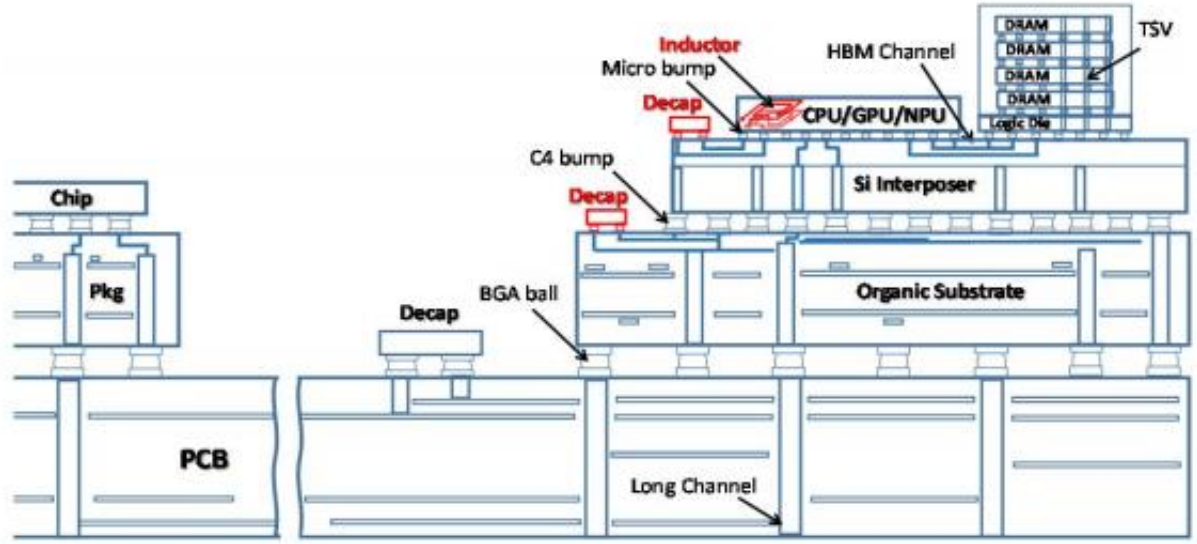
2.5D package with simple I/O circuits

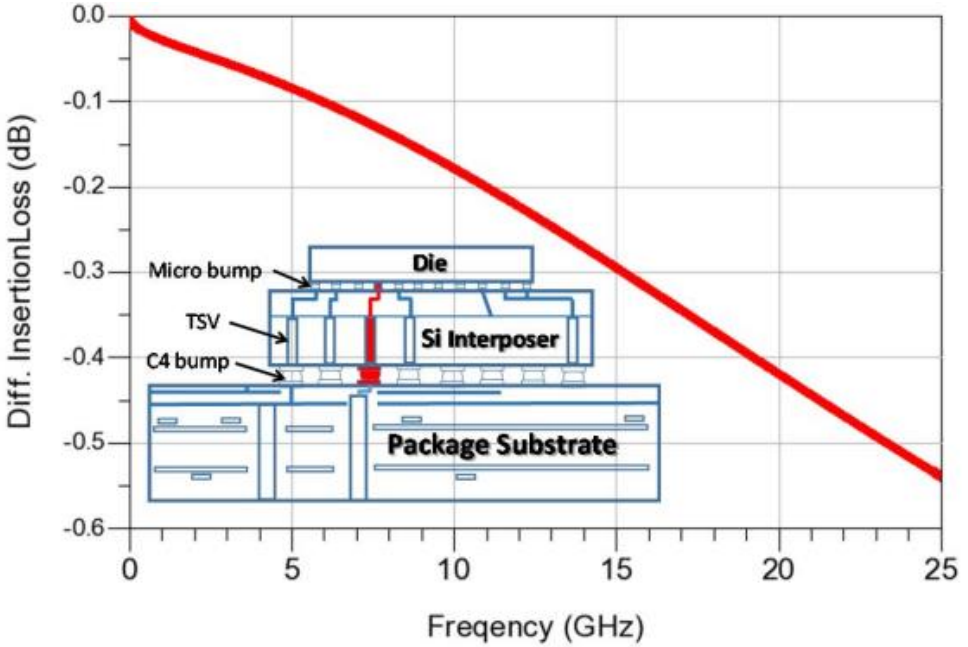


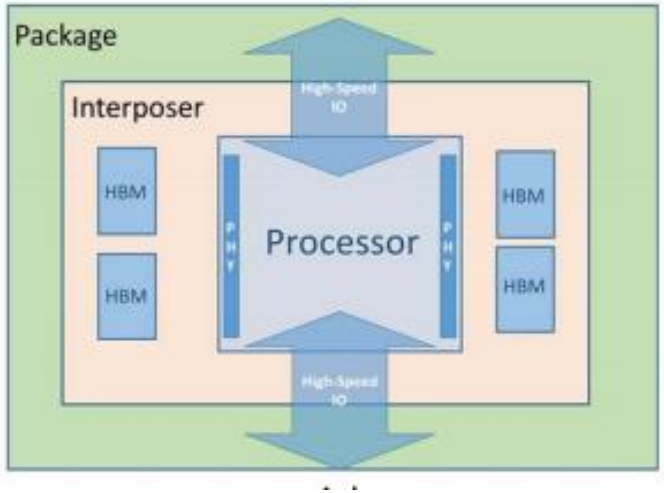
R. Mahajan et al., "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 557-565

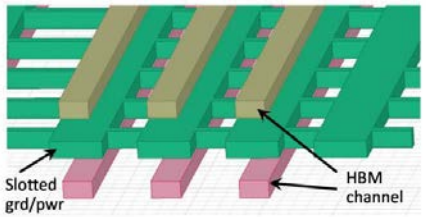
- To enable high bandwidth density connection between dies on a package with simple I/O circuits and low power consumption → Works for 'short' lengths!
- We also need advanced packaging features such as very low loss materials, smooth copper, appropriate design rules, etc., for longer reach applications

Si Interposer Example









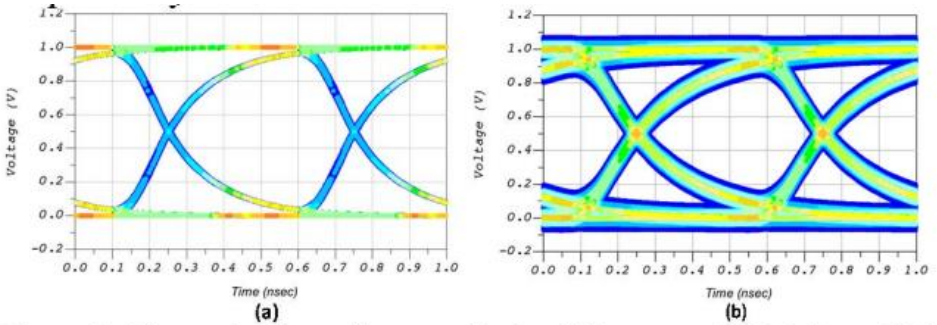
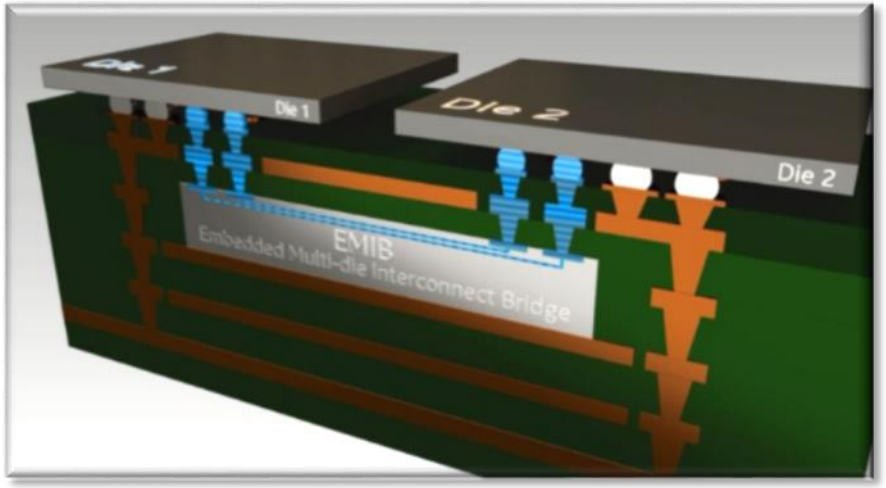
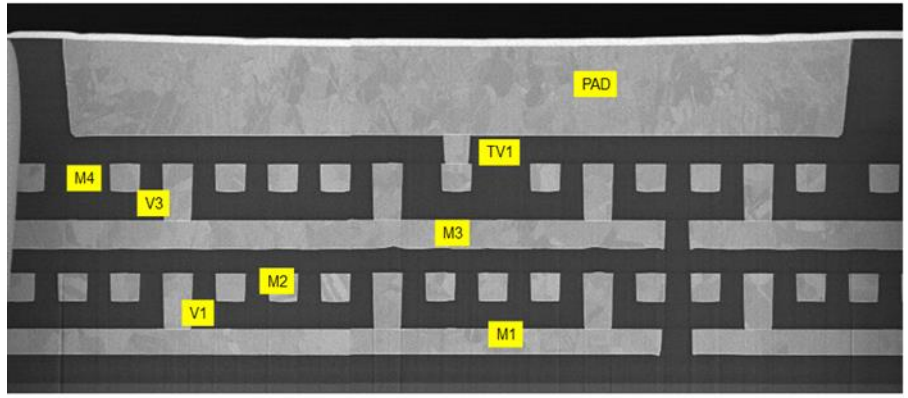


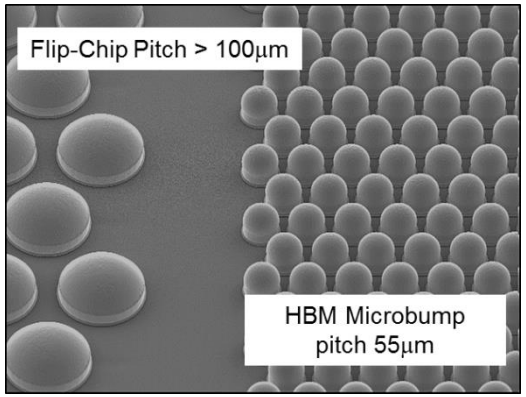
Figure 8: The received eye diagrams for the Si interposer HBM channel (a) without crosstalk and (b) with crosstalk.

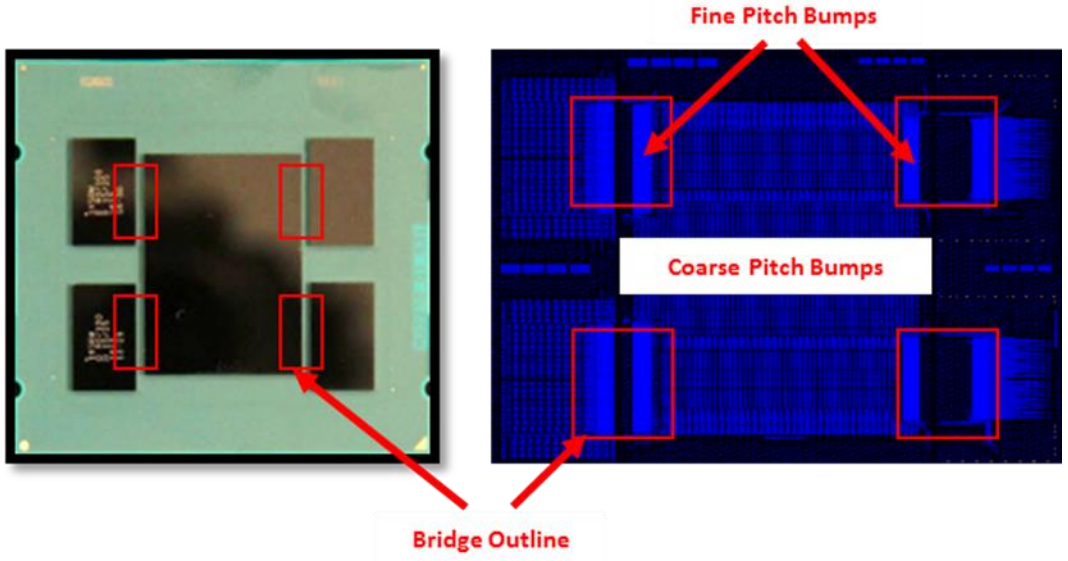
W. Beyene, N. Juneja, Y. Hahm, R. Kollipara and J. Kim, "Signal and Power Integrity Analysis of High-Speed Links with Silicon Interposer," 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), Orlando, FL, 2017, pp. 1708-1715
(Reproduced with permission of W. Beyene)

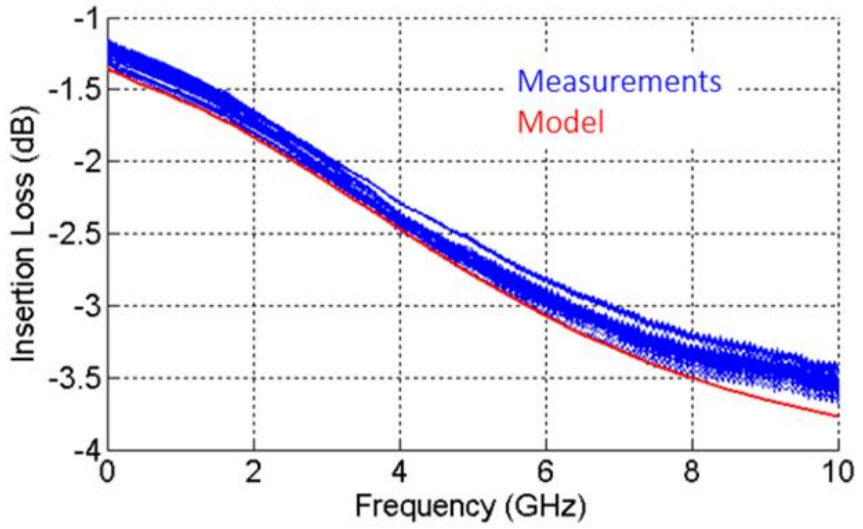
Si Bridge Example





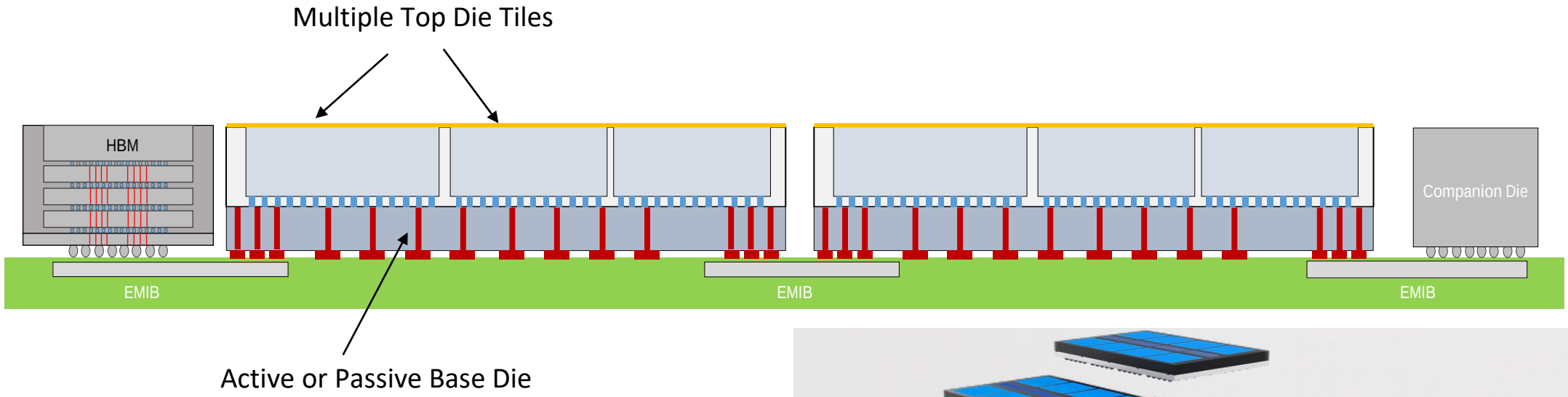


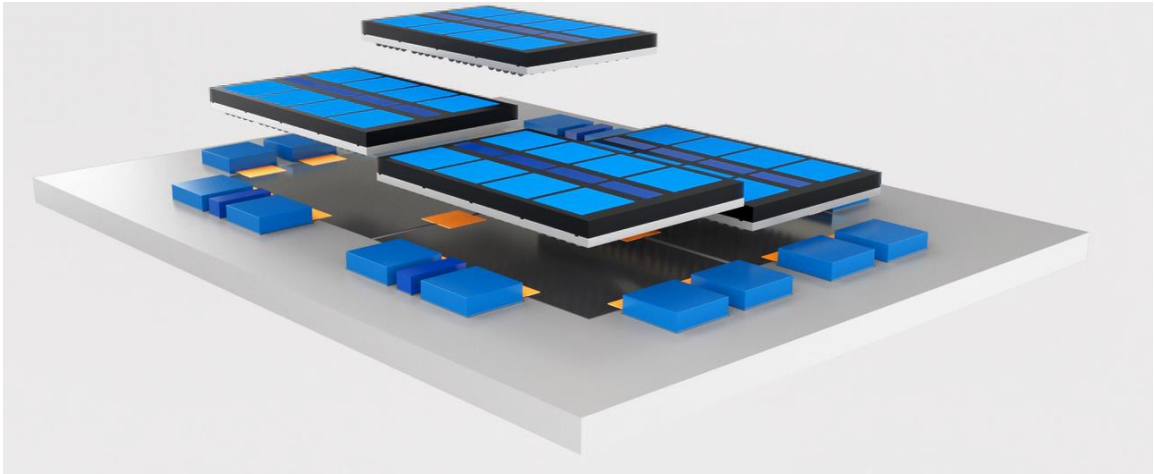




R. Mahajan et al., "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 557-565

‘More’ Advanced Packaging Example: Co-EMIB





- Architecture to enable reticle sized base die & high-density bridge links to companion dies, increased partitioning opportunities
- Results in more challenges in design and analysis

Additional Reading

...

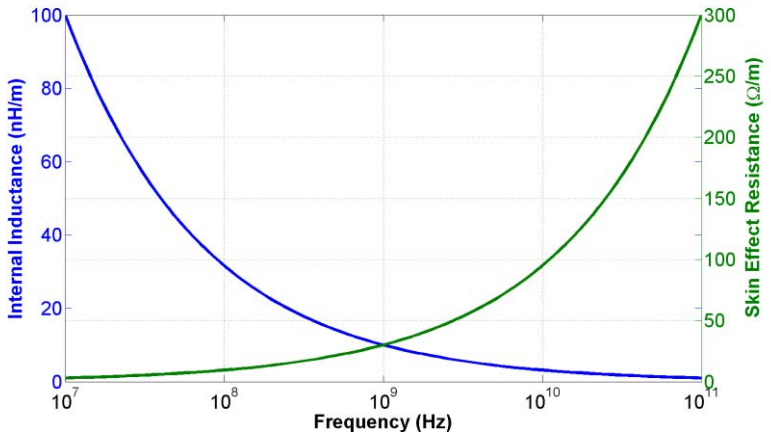
https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2020-edition.html

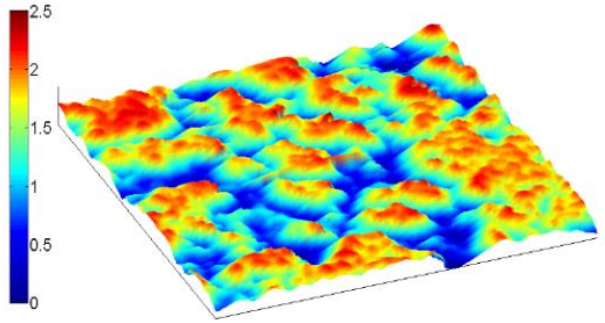
Outline

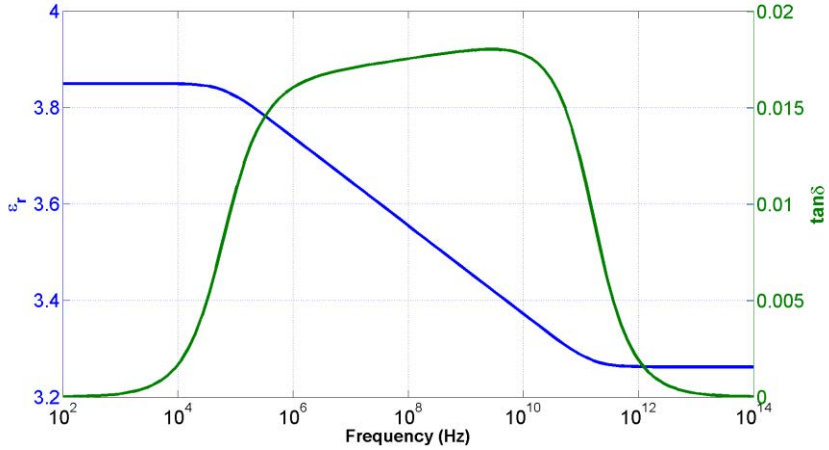
- Introduction
- Advanced Packaging Technologies
- Challenges for Electrical Analysis & Design
- Summary

Package Modeling and Characterization Challenges

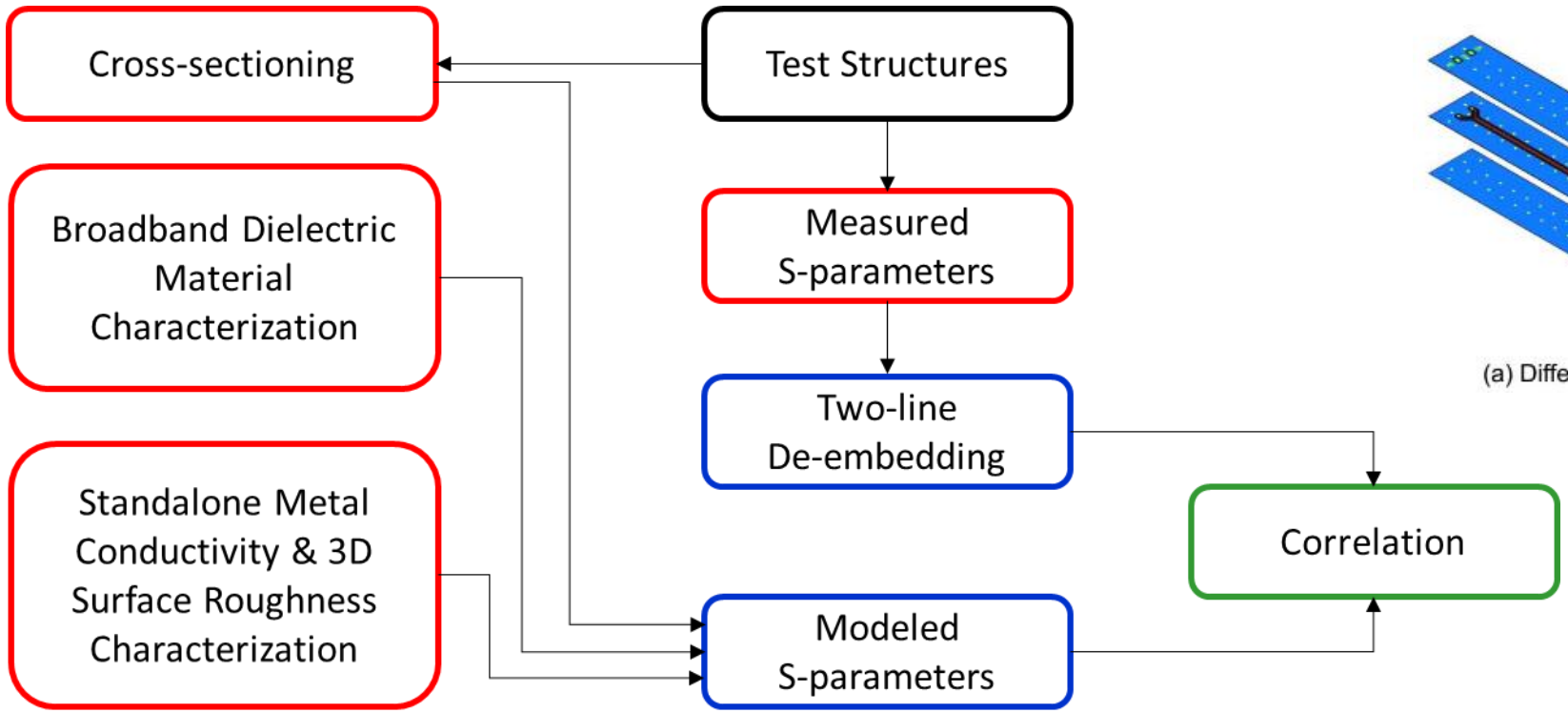
- As data rates increase and margins decrease, new phenomena that were insignificant in the past designs become significant
  - Frequency dependence of resistance losses and inductance for conductors
  - Non-ideal effects of the copper surface
  - Frequency dependence of dielectric permittivity and loss tangent
  - *New geometrical scales with new materials and processes*
- We need *validated models* that accurately predict these effects

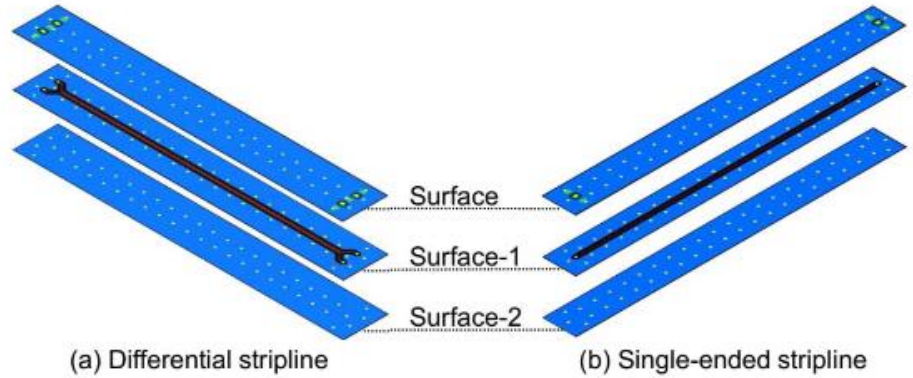






Package Modeling-to-Measurement Correlation



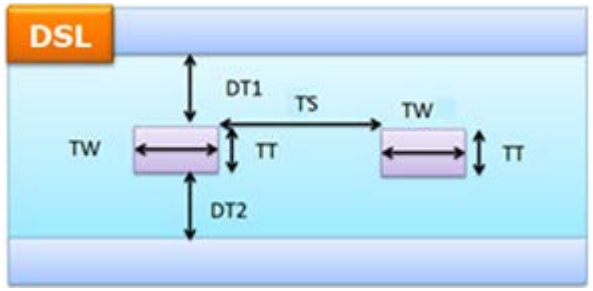


Example package interconnect problem

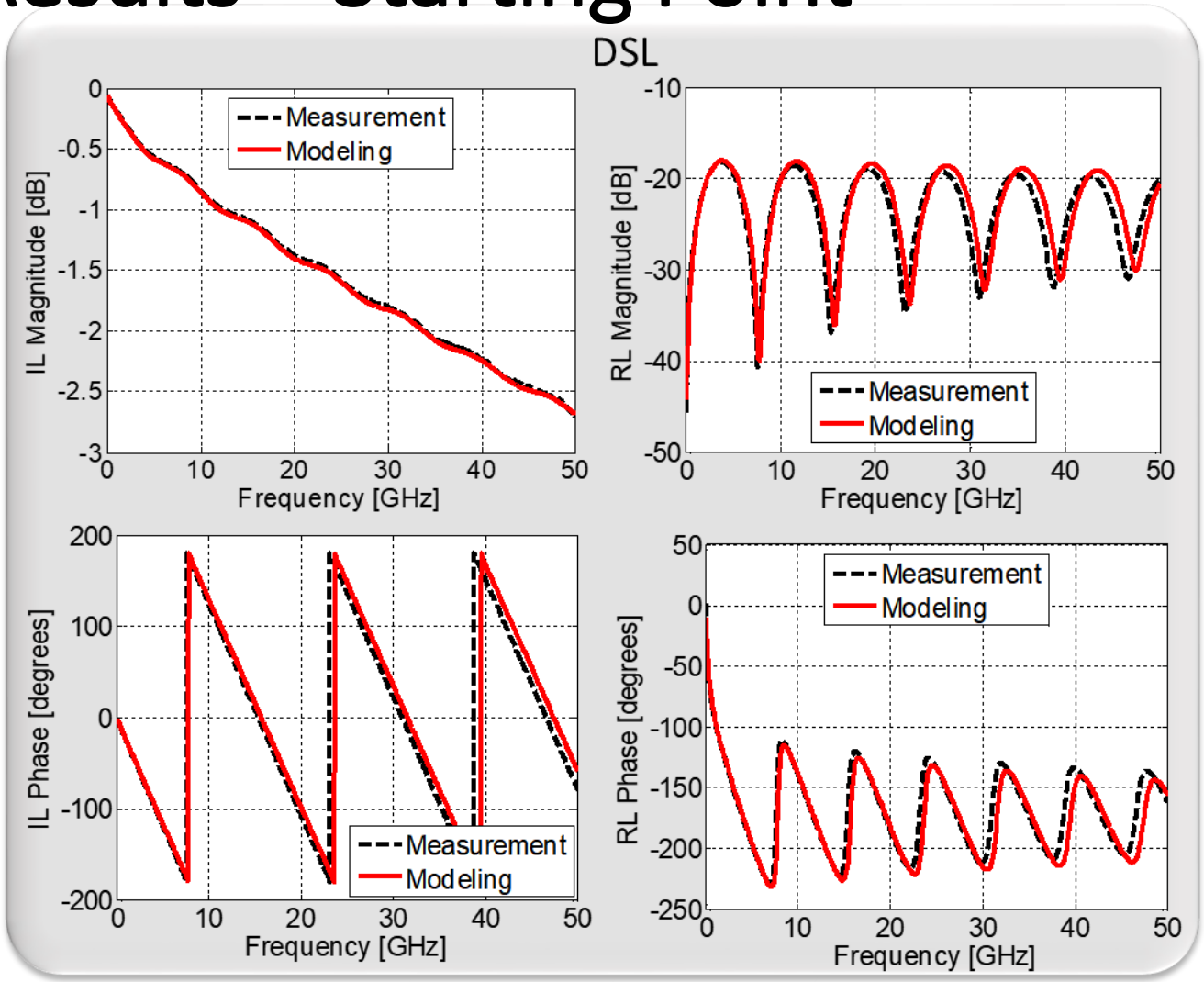
C. S. Geyik et al., "Improved Package Modeling and Correlation Methodology for High Speed IO Design," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 985-991

- Comprehensive flow for an improved package modeling and correlation methodology is essential for efficient electrical design

Example Validation Results – Starting Point

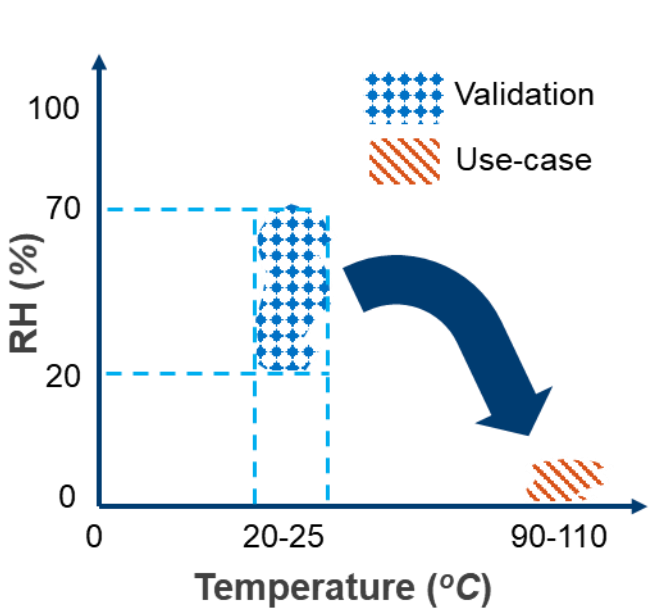


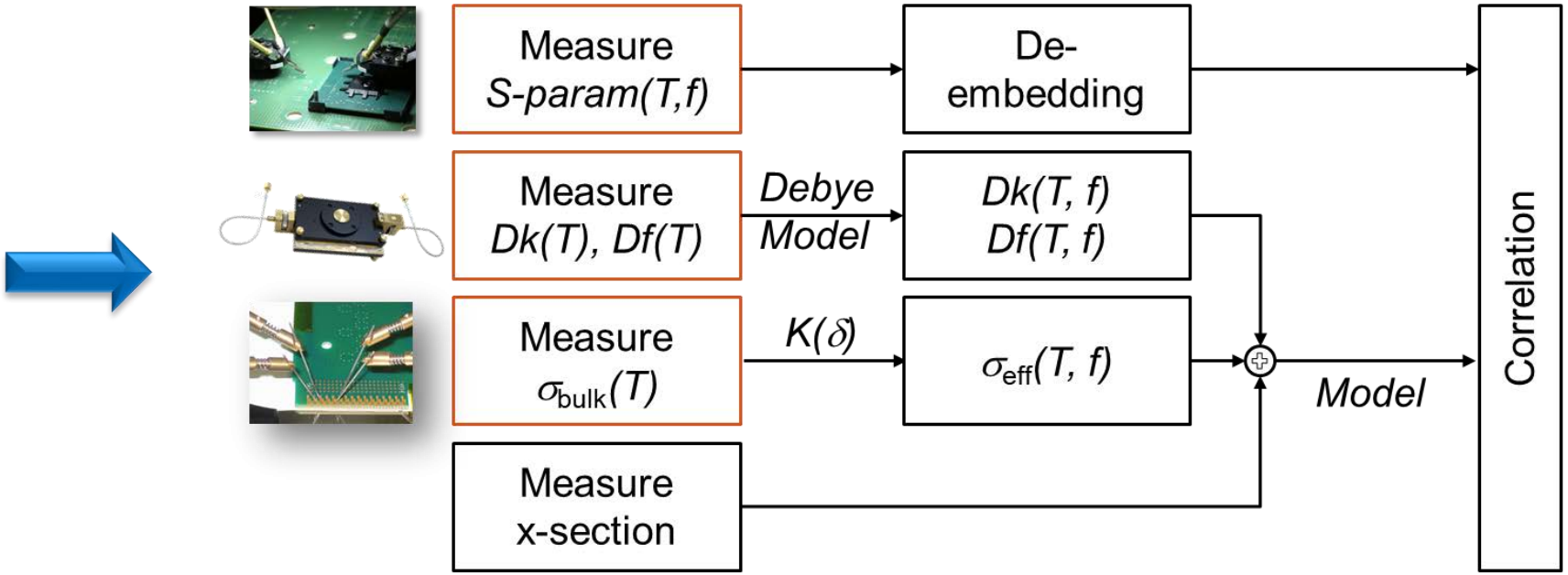
Parameters	DSL
TW	20 um
TT+DT1+DT2	65 um
TS	60 um
Length	(20, 30) mm



- With good dielectric, conductor, surface roughness models and a robust modeling methodology and tool, we can create accurate electrical models

Impact of Environmental Conditions

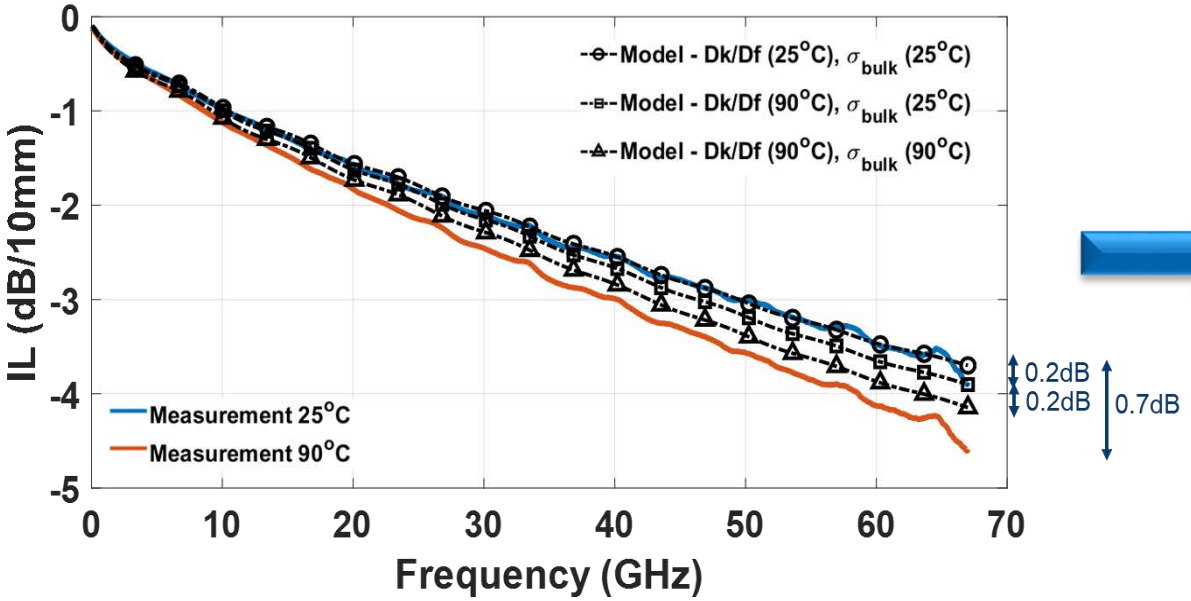


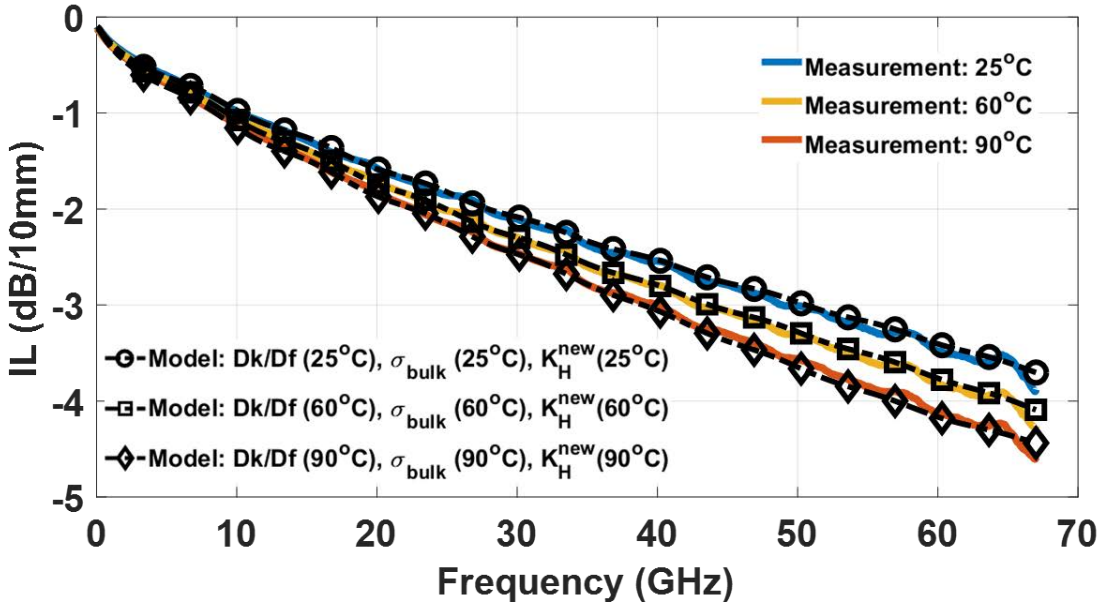


C. S. Geyik, Y. S. Mekonnen, Z. Zhang and K. Aygün, "Impact of Use Conditions on Dielectric and Conductor Material Models for High-Speed Package Interconnects," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 10, pp. 1942-1951, Oct. 2019

- Capturing impact of environmental conditions requires a temperature and humidity dependent modeling and characterization flow

Impact of Environmental Conditions



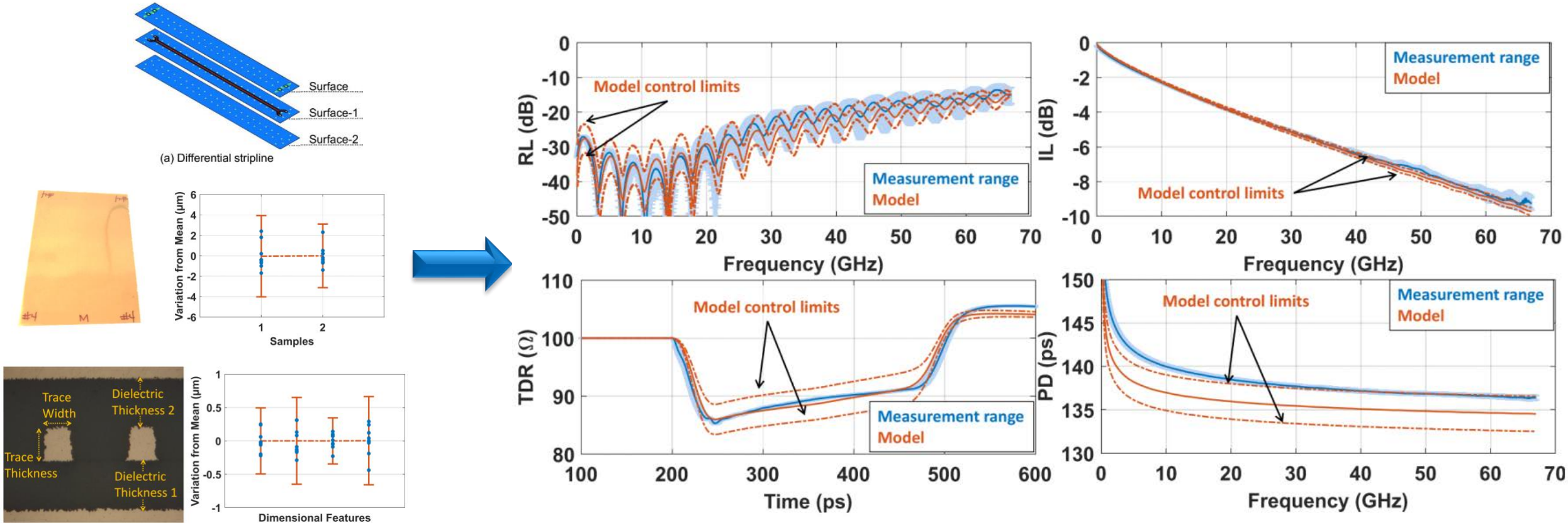


C. S. Geyik, Y. S. Mekonnen, Z. Zhang and K. Aygün, "Impact of Use Conditions on Dielectric and Conductor Material Models for High-Speed Package Interconnects," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 10, pp. 1942-1951, Oct. 2019

$$K_H^{\text{new}}(T,\delta,sr,a) = 1+\frac{3}{2}sr\left(1+\frac{\delta}{a}+\frac{\delta^2}{2a^2}\right)^{-1}+c_1(T-T_0)e^{-c_2\delta}$$

- Temperature dependent material properties and surface roughness models help further improve measurement to modeling correlation quality

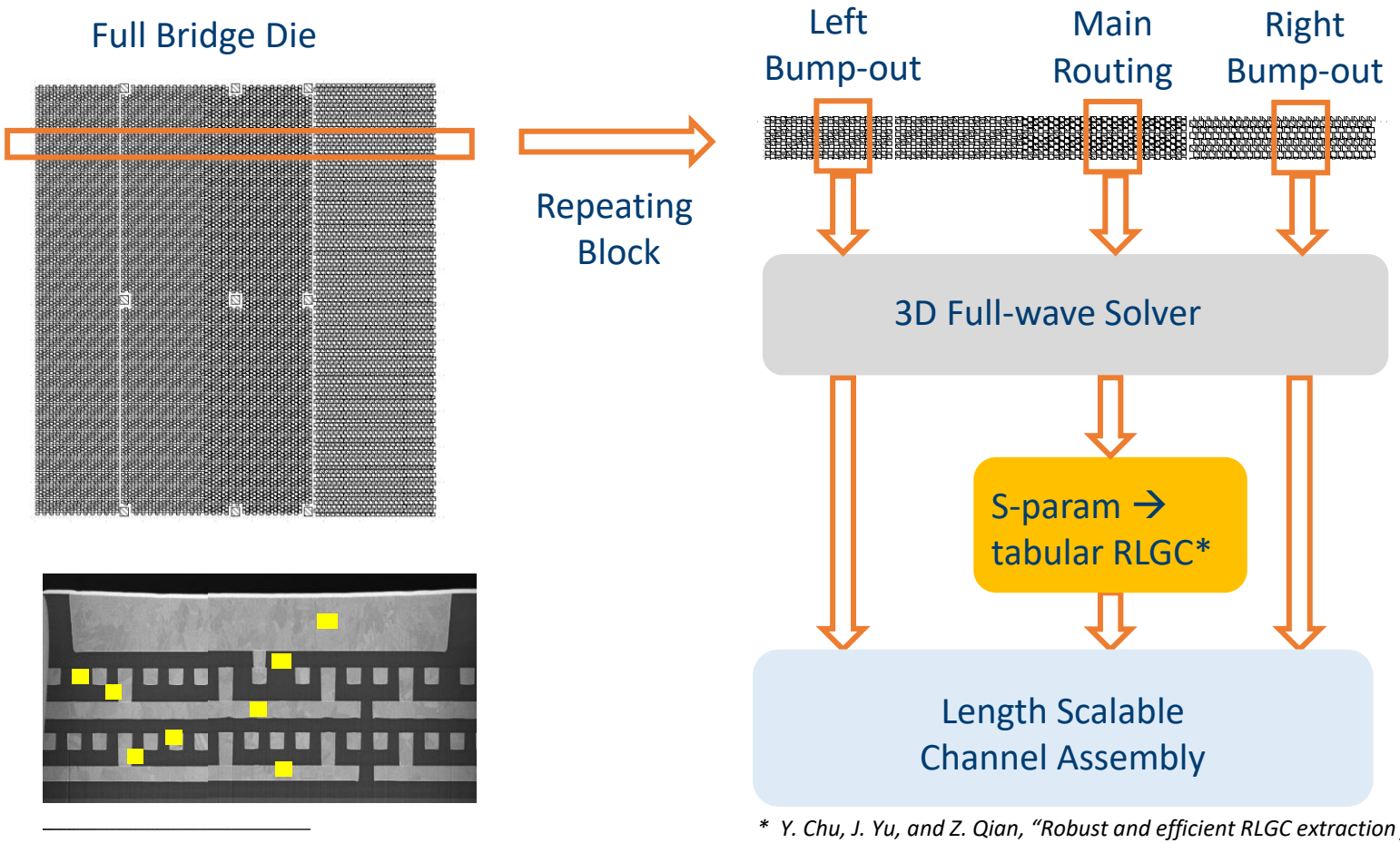
Impact of Measurement Uncertainties



C. S. Geyik, M. J. Hill, Z. Zhang, K. Aygün and J. T. Aberle, "Measurement Uncertainty Propagation in the Validation of High-Speed Interconnects," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2020, pp. 1-3

- Generating high-fidelity package electrical models requires precise modeling & measurement methods, environmental control, and understanding of uncertainties for each measurement

Accurate Signal Net Modeling for 2.xD Packages



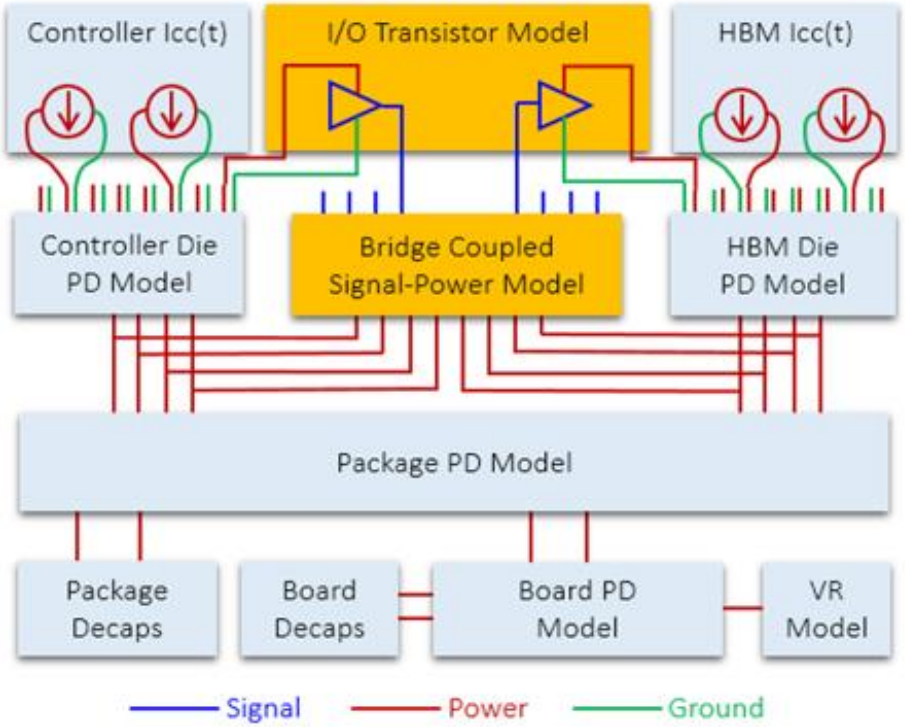
* *Y. Chu, J. Yu, and Z. Qian, "Robust and efficient RLGC extraction for transmission line structures with periodic three-dimensional geometries," IEEE EMC&SI 2015*

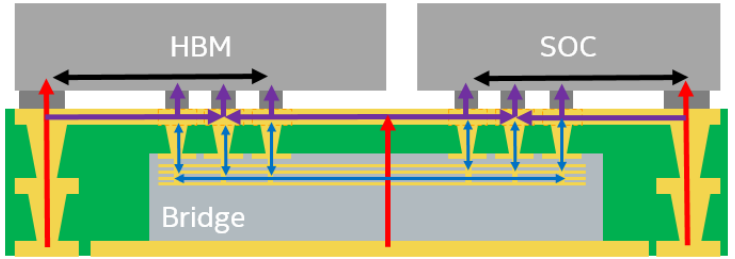
Z. Qian, J. Xie and K. Aygün, "Electrical Analysis of EMIB Packages," 2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2018

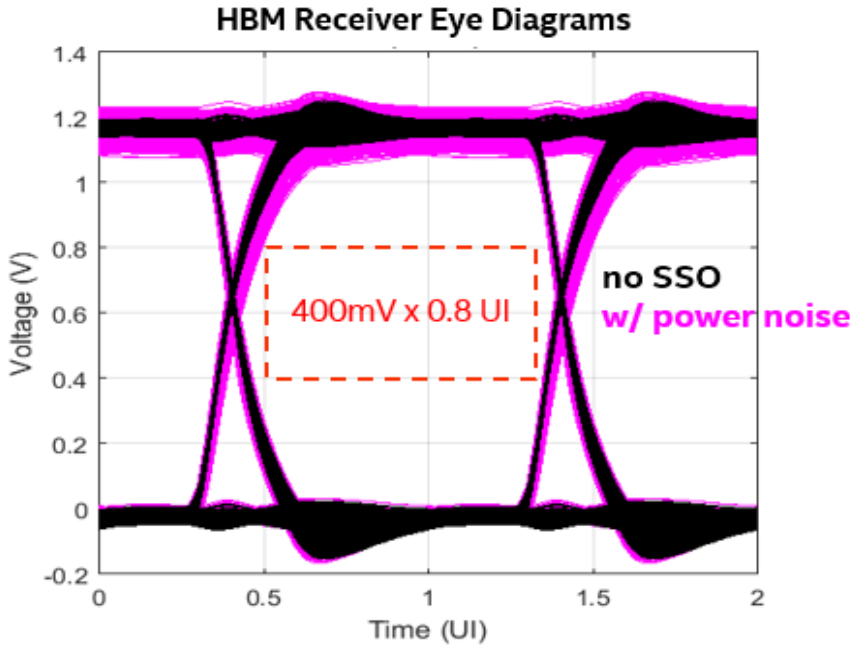
- Novel Fine features in 2.xD packages require new interconnect modeling methodologies

2.xD Packaging Electrical Analysis Methodology

- Accurate signal channel modeling
- Unique power delivery network modeling
- Unified framework for SIPI co-simulation







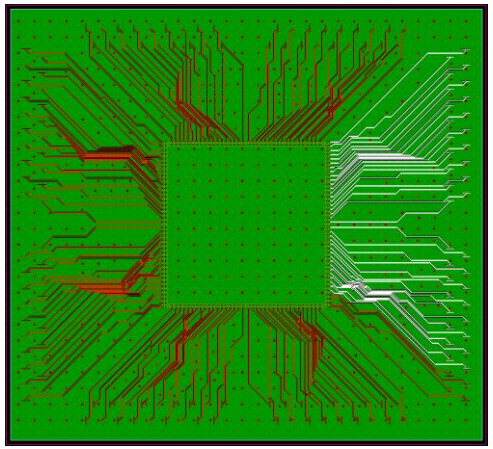
- Electrical analysis challenges of 2.xD packaging technologies range from extraction of very fines features to SIPI co-simulation which requires advanced modeling methodologies

Modeling for Product Design: Full-Package Example

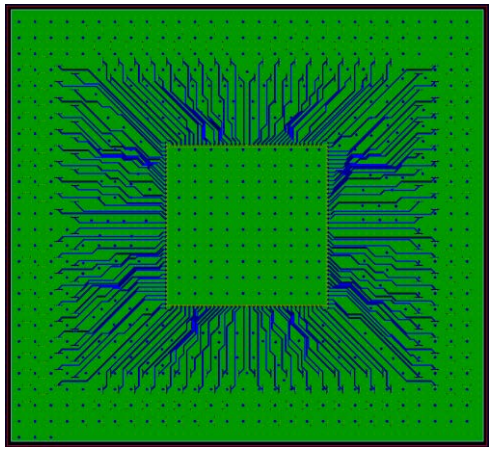
- A typical product package can have:
  - 30x30 to > 50x50 mm form factor
  - 4-20+ layers
  - Hundreds or more IO nets/traces
  - 10s of distinct power delivery planes/shapes
  - >10k die bumps (FLI connections)
  - Few hundred to few thousand package balls/pads/pins
  - Dimensions range from few microns to ~1 mm
- May also need to include connectors and sockets

- Analysis of a realistic full-package is expected to result in 10s of millions of unknowns with varying length scales and material properties, AND hundreds of ports
- For practical purposes, this is an unsolved problem that has resulted in sub-optimal final designs, driven by long simulation times and/or limited simulation domains

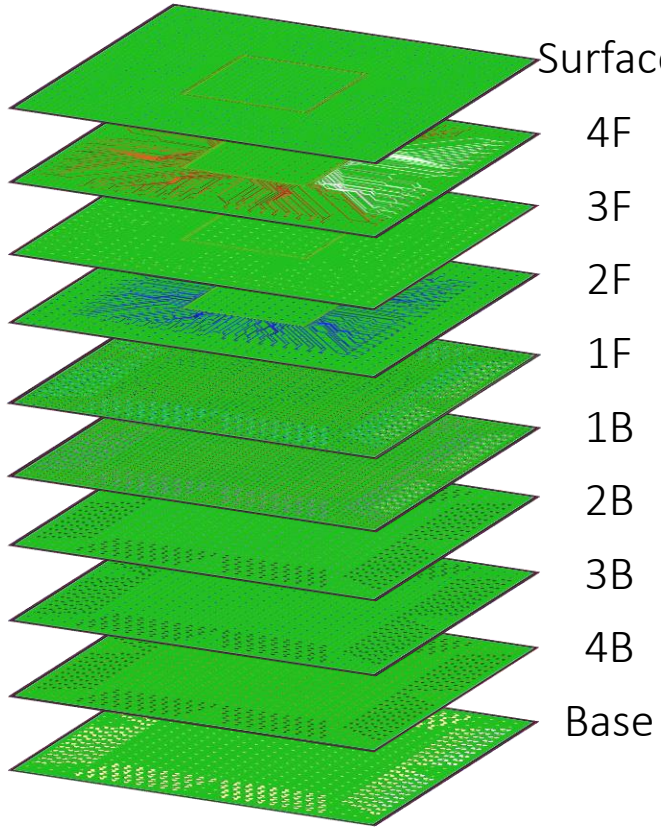
Full-Wave Analysis of a Full-Package – An Example



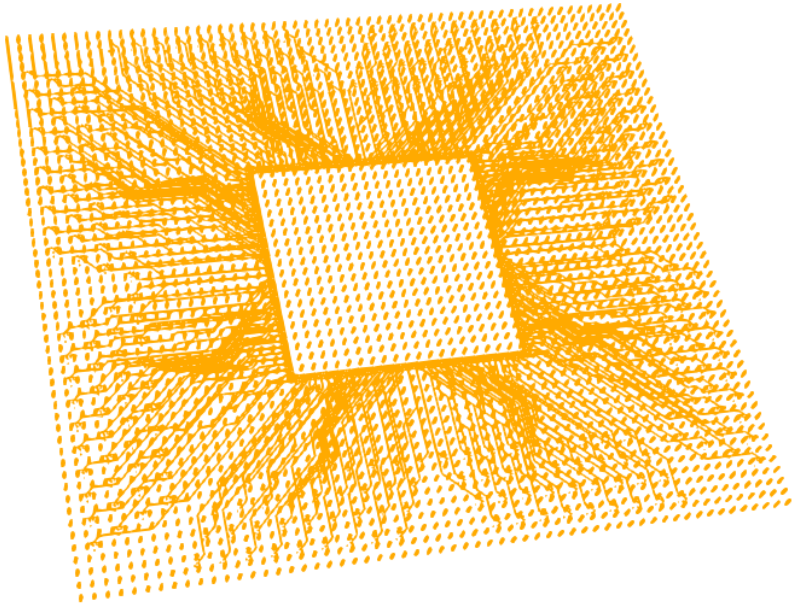
4F Layer



2F Layer

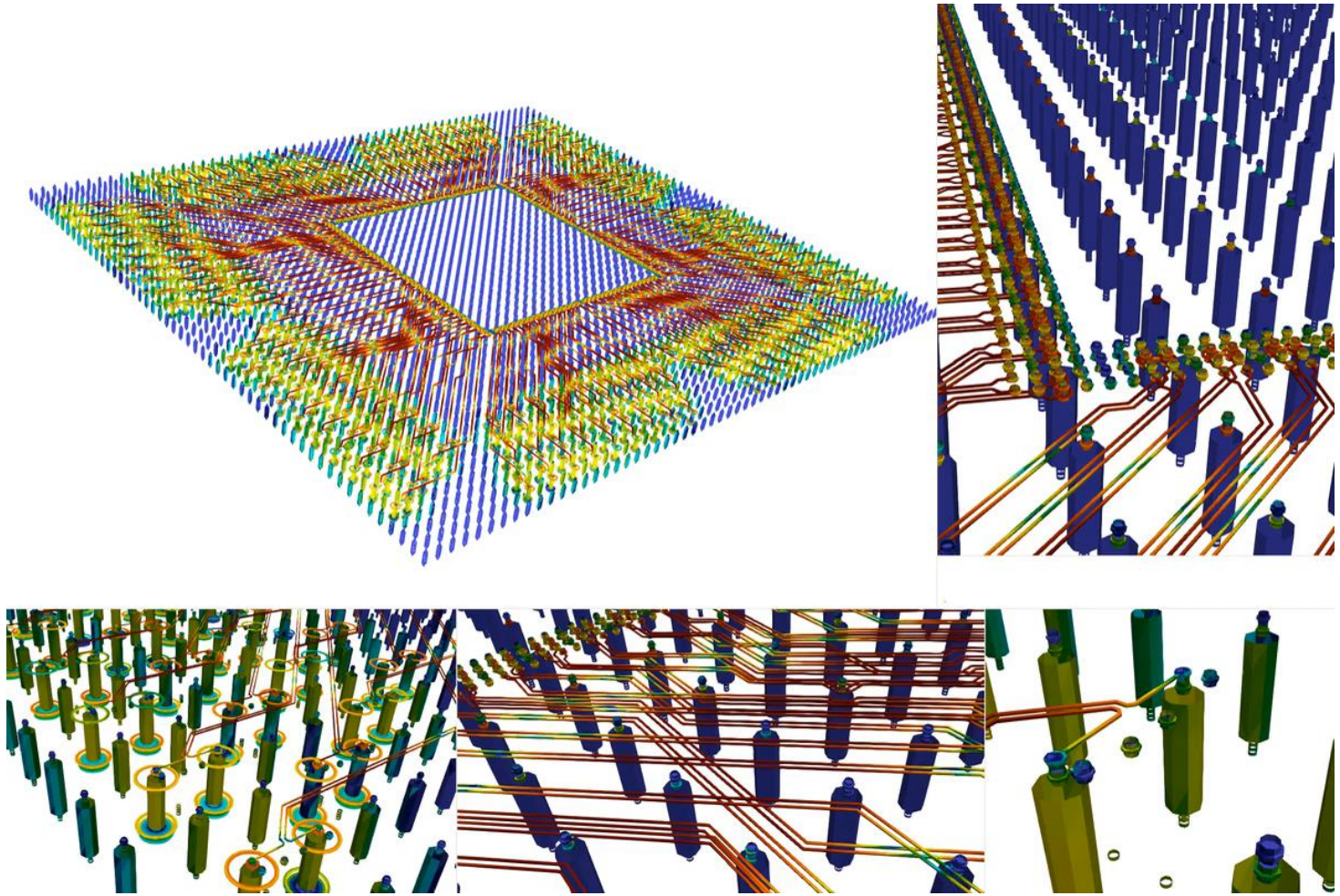


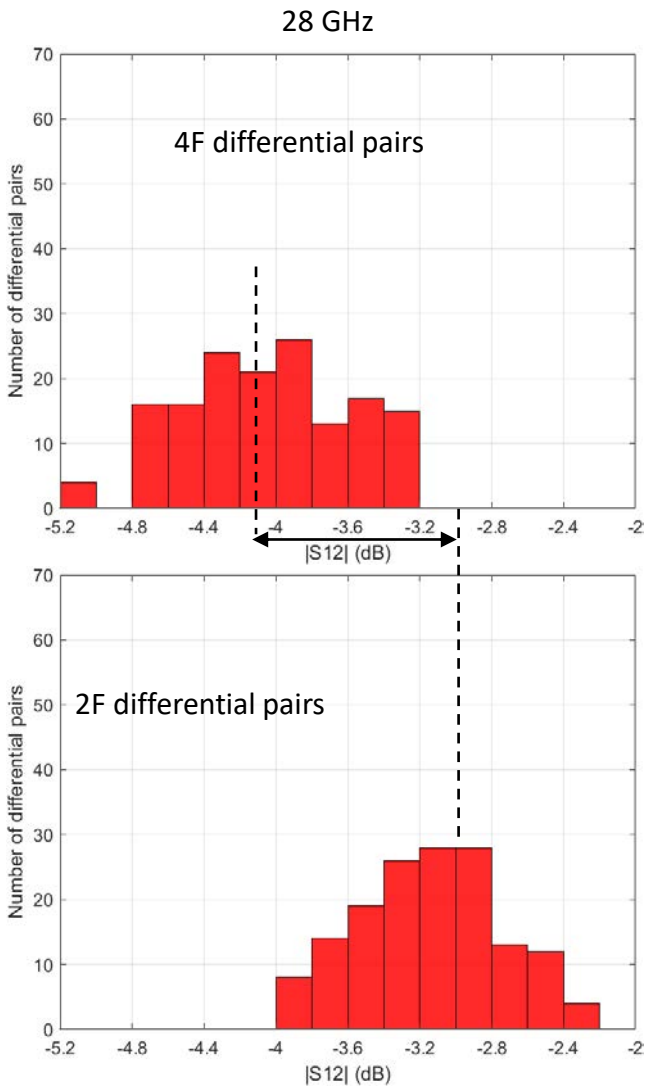
Reduced-domain layered-medium integral-equation* model for a full-package



** C. Liu and A. E. Yılmaz, "A reduced-domain layered-medium integral-equation method for electronic packages," in Proc. IEEE EPEPS, Oct. 2019*

Full-wave Analysis of a Full-Package – An Example

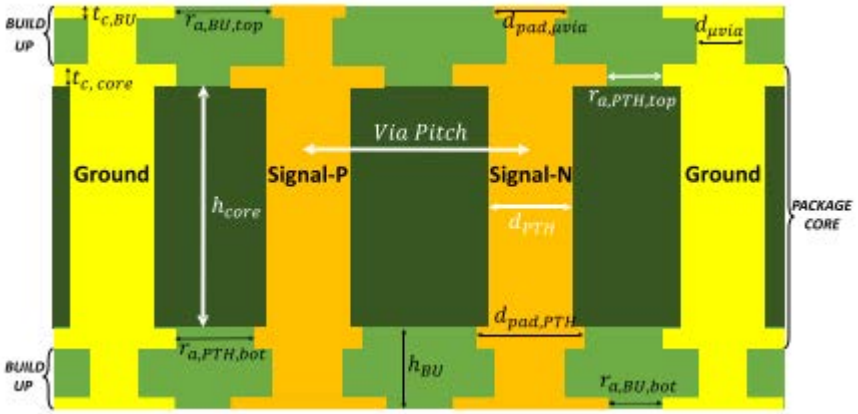


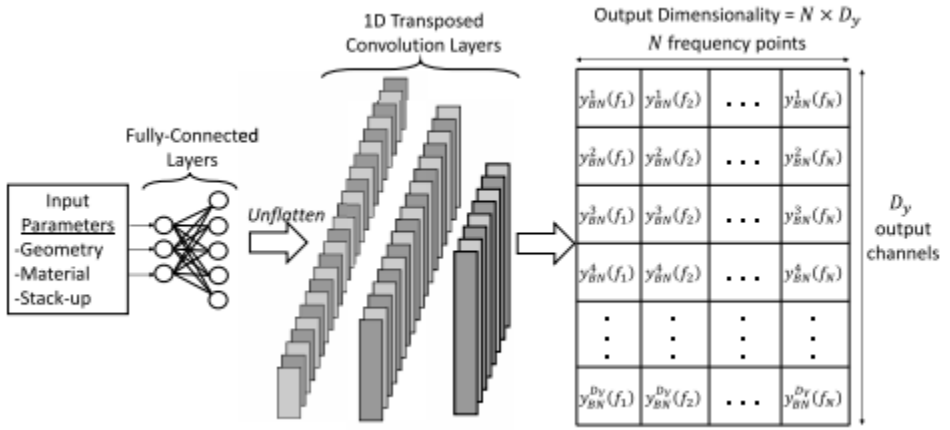


Reproduced with permission of Prof. A. Yilmaz from UT Austin

- Full-wave analysis of a package enables new package design optimization opportunities

Application of Machine Learning – An Example





Parameter		Unit	Min	Max
μ-via Diameter	$d_{\mu\text{-via}}$	μm	30	70
μ-via Pad Diameter	$d_{\text{pad, }\mu\text{-via}}$	μm	31	140
BU Layer Thickness	h_{BU}	μm	20	35
μ-via Top Antipad Radius	$r_{a,\text{ BU, TOP}}$	μm	100	500
μ-via Bot. Antipad Radius	$r_{a,\text{ BU, BOT}}$	μm	100	500
PTH Pitch	v_p	μm	300	1200
Core Thickness	h_{Core}	μm	100	1200
BU Copper Thickness	$t_{c,\text{ BU}}$	μm	10	20
Core Copper Thickness	$t_{c,\text{ CORE}}$	μm	11	40
PTH Diameter	d_{PTH}	μm	100	250
PTH Pad Diameter	$d_{\text{pad, PTH}}$	μm	110	500
PTH Top Antipad Radius	$r_{a,\text{ PTH, TOP}}$	μm	50	500
PTH Bot. Antipad Radius	$r_{a,\text{ PTH, BOT}}$	μm	50	500

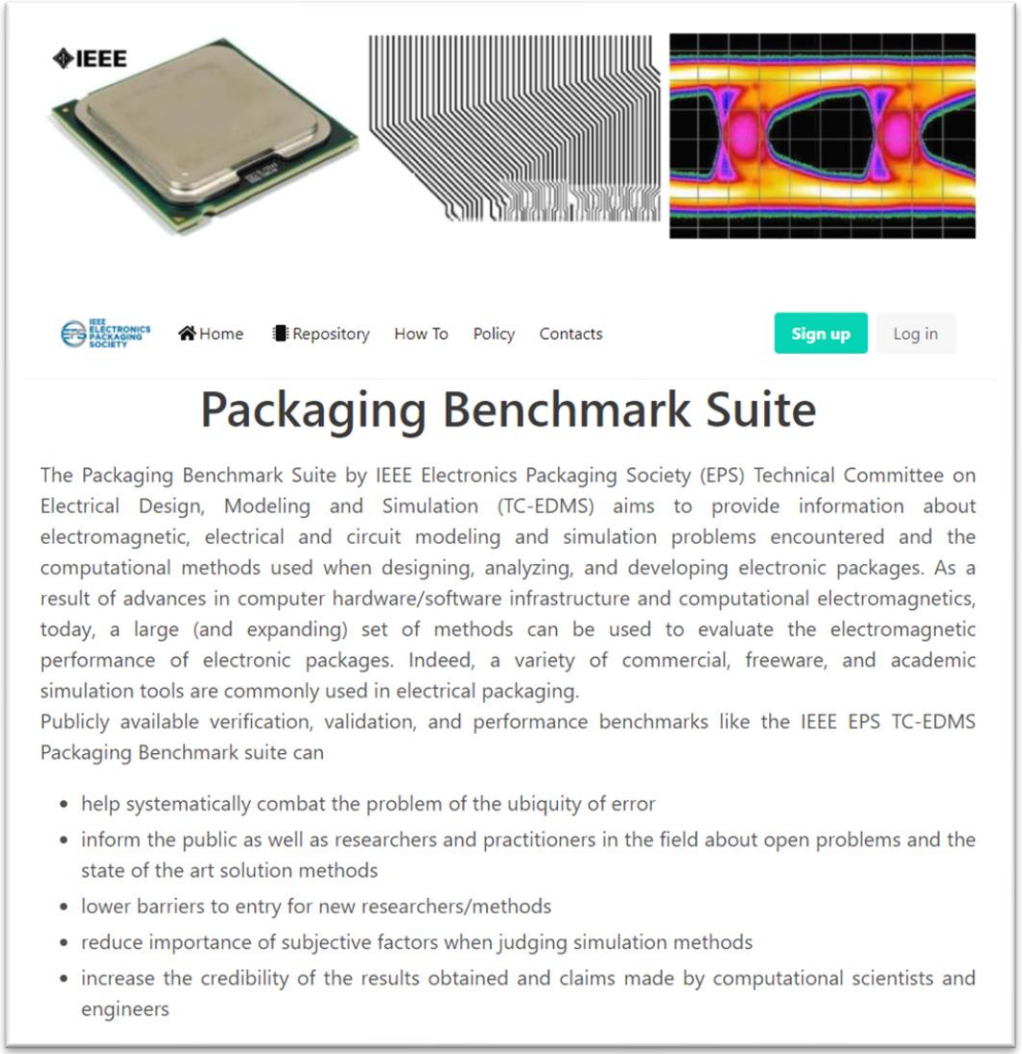
COMPARISON OF MODELS ON TEST DATA FOR PTH MODEL

	DNN	S-TCNN	S-TCNN + CEL + PEL
NMSE	9.42% ± 0.33%	5.08% ± 0.31%	5.34% ± 0.09%
Av. Causality Metric	7.49%	11.17%	100.0%
Range of σ_1	[0.615, 1.285]	[0.653, 1.131]	[0.607, 0.999]
Inference Time (for 1K broadband S-Params.)	0.26 s	0.13 s	0.91 s

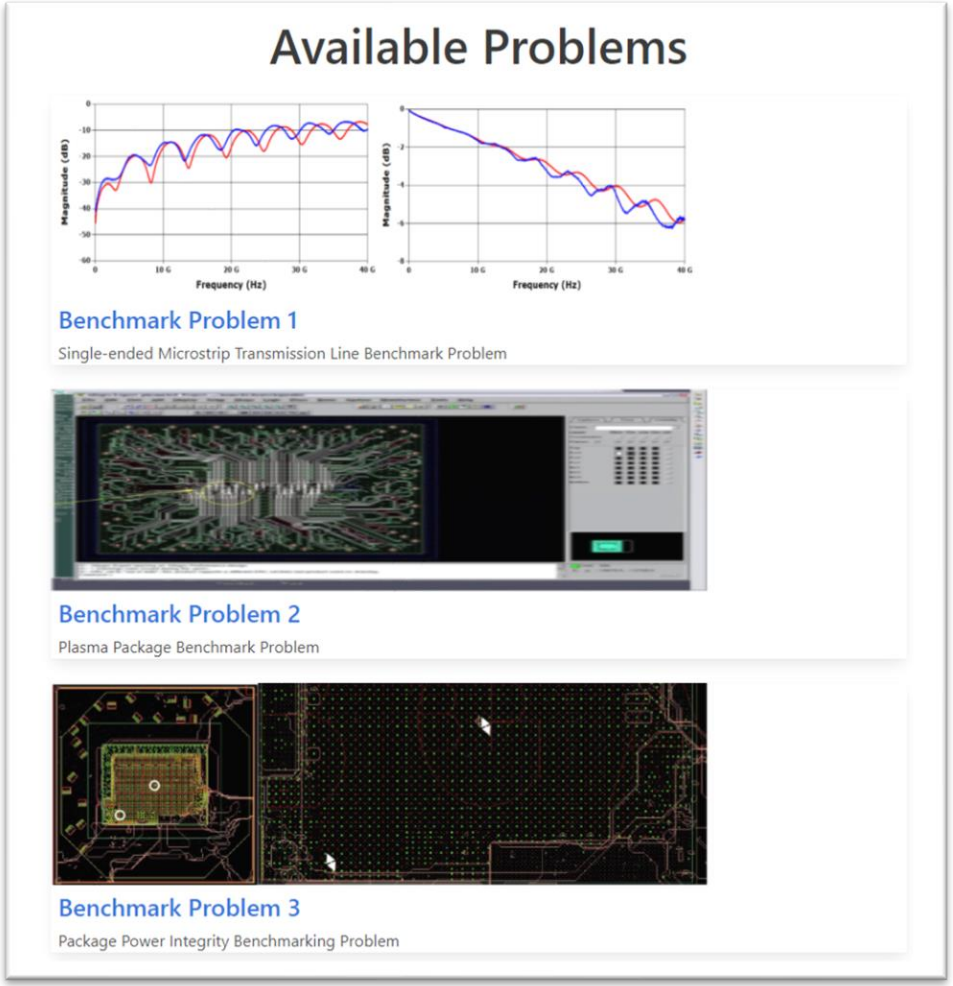
H. M. Torun, A. C. Durgun, K. Aygün and M. Swaminathan, "Causal and Passive Parameterization of S-Parameters Using Neural Networks," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 10, pp. 4290-4304, Oct. 2020

- Emerging machine-learning algorithms for package modeling and design optimization

IEEE EPS TC-EDMS Packaging Benchmarking Suite



https://packaging-benchmarks.org/



- Benchmark problems can help research community with new methods and tools

IEEE EPS Conferences

http://www.epeps.org/

https://www.linkedin.com/groups/86343/

https://spi2021.uni-siegen.de/

http://www.edaps.org/

- Multiple IEEE EPS conferences focused on electrical analysis of packaging and systems

Summary

- Semiconductor packaging is experiencing an accelerated pace of innovation fueled by emerging electronic system connectivity and heterogeneous integration demands
- Novel *advanced* packaging architectures provide new opportunities to improve package electrical design for short reach interconnects
- These new technologies need to include features to enable also long reach interconnects
- Validated modeling methodologies & collaterals are key for both existing and emerging package and system designs
- Emerging modeling tools have to address modeling fidelity including new dimensions and materials, algorithm capability, and scalability simultaneously to solve connectivity problems of future