Santa Clara Valley Electronics Packaging Society Chapter
September 30, 2021 *Visit* ***www.ieee.org/scveps***

Ultrafast Time Domain Cryogenic CMOS Device Characterization Platform for Quantum Computing Applications

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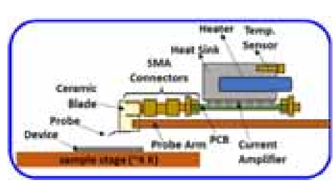
Acknowledgements : Jason Campbell, NIST

NIST
National Institute of Standards and Technology
U.S. Department of Commerce

Outline

- Introduction
  - Quantum computing
    - Challenges of scaling up
      - Why cryo CMOS electronics?
  - Applications of Cryo CMOS
- Motivation : Device characterization
  - Device operation at low temperatures
  - Fast time-dependent low temperature characterization
    - Understanding device physics
      - Analog circuit design
      - Device reliability
- Experimental Setup
- Future work



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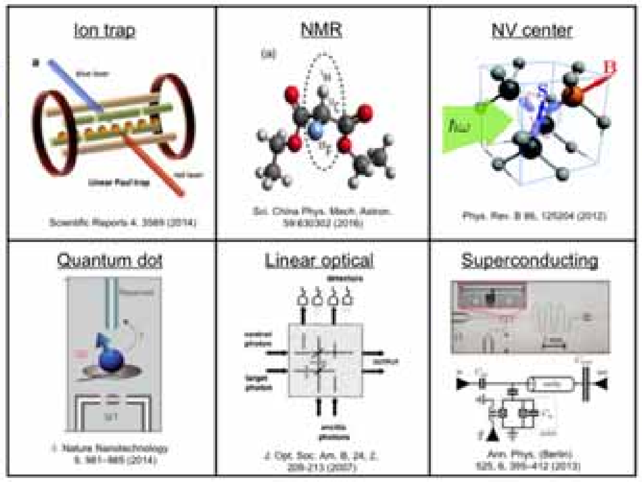
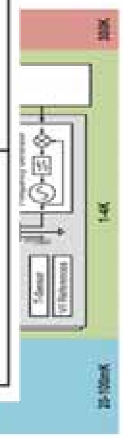
Quantum Computing





https://phys.org/news/2020-08-google-largest-chemical-simulation-quantum.html ; https://www.cnet.com/news/google-quantum-supremacy-only-first-taste-of-computing-revolution/;
Arute, F. et al, Science 2020, Patra, B. et al, IEEE J Solid-St Circ 2018, Amundson, J.; Sexton-Kennedy, E., Quantum Computing. EPJ Web Conf. 2019, 214, 09010.

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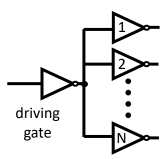
Challenges beyond Read/Control Electronics

- Fan-out not possible
  - ↑ I/O lines
    - ↑ heat load
    - ↑ Latency



- High frequency and small amplitude signals
  - Highly sensitive to environment
    - Noise, crosstalk/interference
    - Material system
      - Losses and noise at low temperature and low signals
- Need of platform
  - Compatible with read/control electronics along with qubits
  - Resilient to cool down cycles
  - Low loss and latency
  - Efficient power dissipation

Reilly, D. J., IEDM 2019, Rosenberg, D. et. al IEEE Microw Mag 2020.

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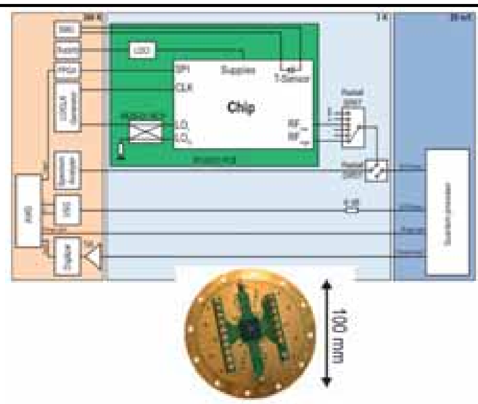
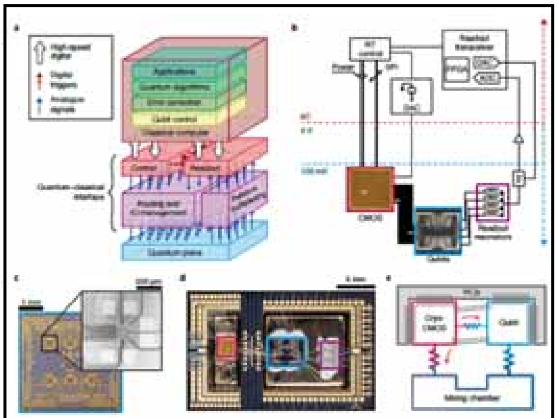
Electronics for quantum computing



Horse Ridge
Intel, QuTech..



Gooseberry
Microsoft, Univ. of Sydney….

Patra, B. et al 2020 IEEE ISSCC; Pauka, S. J. et al, Nature Electronics 2021.

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Cryogenic Electronics : Applications

✓ Quantum Computing

Quantum computer: < 20 mK

✓ High Performance Computing

Supercomputer : 77 K

✓ LT Source/Sensor Electronics

e.g., opto-electronics

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High Performance Computing

- ✓Speed
  - ✓High mobility, higher saturation velocity
- ✓Lower noise
- ✓Uniform electrical parameters due to the tighter thermal environment
- ✓Better reliability
  - ✓lower thermally assisted degradations
- ✓Increased integration density due to higher thermal conductivity of materials used in circuits
- ✓Less power consumption due to lower supply voltage

Gutierrez-D et all Low temperature electronics : physics, devices, circuits, and applications, 2001; Balestra, F. Et al, Device and circuit cryogenic operation for low temperature electronics, 2001.

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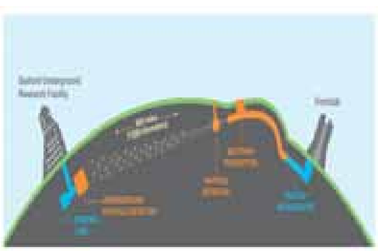
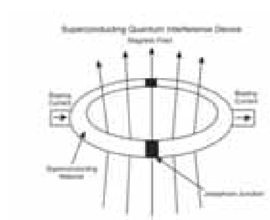
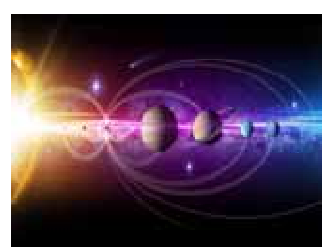
Low Temperature Sensor Electronics

- Satellite
- Space mission
- Dark matter physics
- Magnetometry
  - Measuring tiny magnetic fields
- Gravitational wave research

Sensors operated at low temperatures
- To improve sensitivity
- Low temperature required for it to work
- Due to environment







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Gutierrez-D et all Low temperature electronics : physics, devices, circuits, and applications, 2001

Space exploration

Location	Surface Temp (K)
Europa	93
Enceladus	80
Mars	131
Lunar shadowed region	43

- Radiation
- Constraints
  - Mass
  - Power
  - cost
- Thermal control
  - “Warm box” (-50 ^oC)

Castillo, L. D. et al 2018 IEEE Aerospace Conference.
https://solarsystem.nasa.gov/

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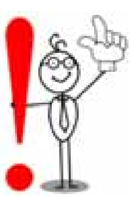
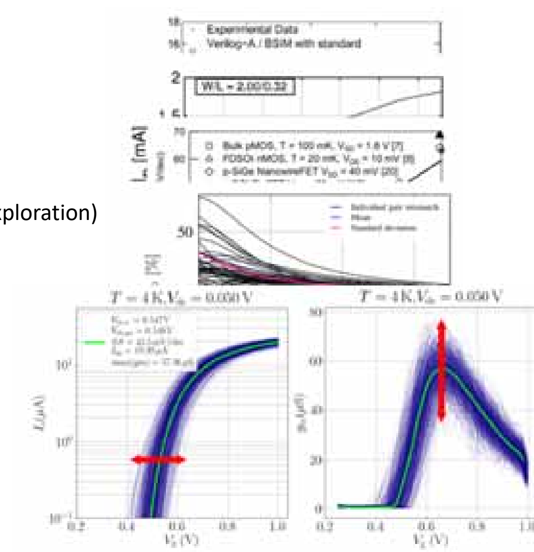
Motivation : Device Characterization



- Cryo-CMOS models
  - Build device model
    - Necessary for circuit design
    - Commercial device model
      - Up to 230 K (- 40 ^oC) (-50 ^oC for space exploration)
    - Does not account for
      - Kink effect
      - SS saturation
      - Transistor mismatch and variability
- Understanding device physics
  - Extrapolating parameters
  - Down selecting relevant technologies
  - Account for reliability issues



Akturk, A. et al, TED 2010; Beckers, A. et al JEDS 2018; Hart, P. A. T. et al, JEDS 2020, Grill, A. et al, 2020 (IRPS)

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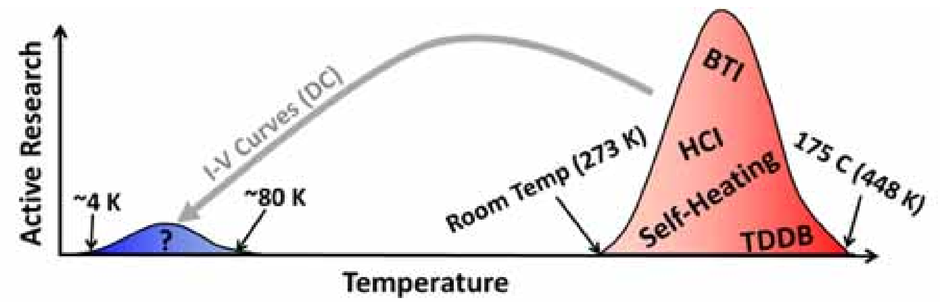
Why Worry?



RT	~4K	
Device Models	Device Model	☹
Reliability	Reliability	☹ ☹
Device Physics	Device Physics	😑

?

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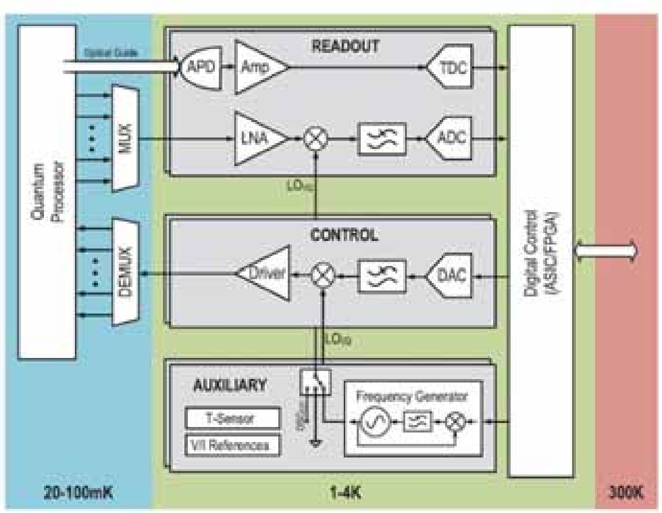
Loss of Time and $



- Digital
  - Speed and power
- Analog Circuits
  - Speed
  - Power
  - Gain
  - Precision
  - Supply voltage

Patra, B. et al, IEEE J Solid-St Circ 2018.

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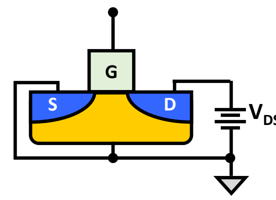
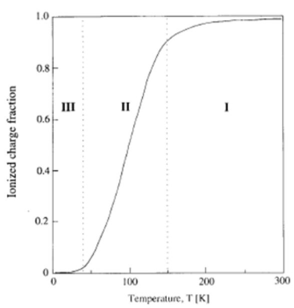
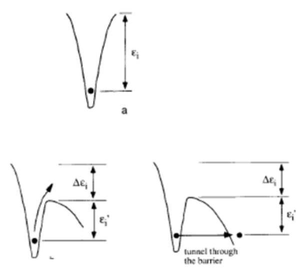
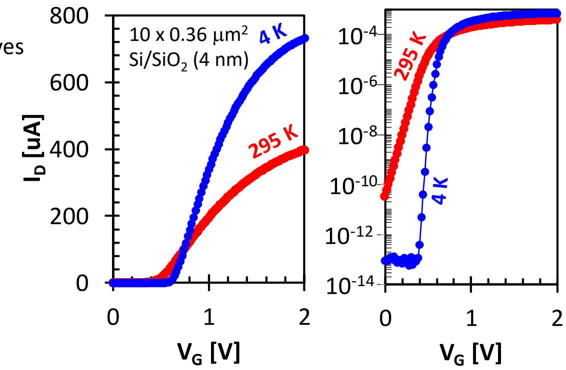
Device at Low Temperature

- Devices
  - BJT : minority carrier device, diffusion limited esp. at low temperatures
  - MOSFET : majority carrier device, gate controlled
- Devices function at cryogenic temps (4 K)
- In general: $|V_{th}|$ increases, I_{ON} increases (mobility), and SS improves









Gutierrez-D et all Low temperature electronics : physics, devices, circuits, and applications, 2001

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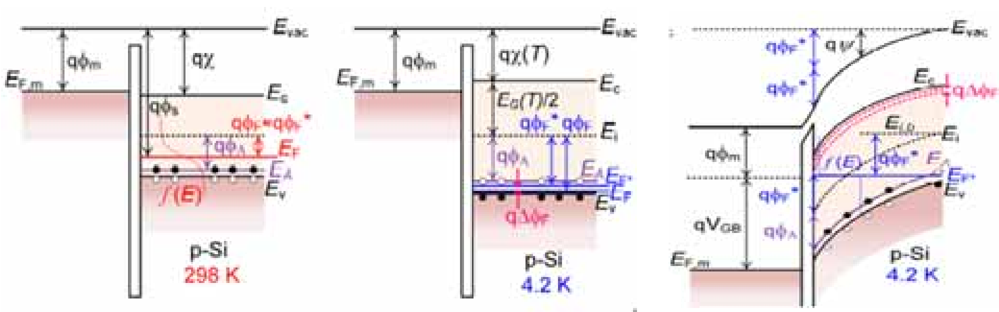
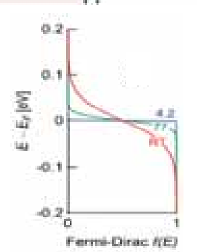
Temp. Dependence of V_{th}



- ↑ Bandgap and scaling of Fermi-Dirac function
- Scaling of intrinsic carrier density
- ↑ fermi potential
- Incomplete ionization
  - Thermal
  - Field



Beckers, A. et al, ESSDERC 2019; Beckers, A. et al, TED 2018.

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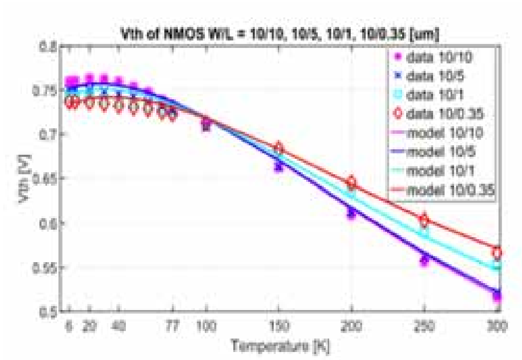
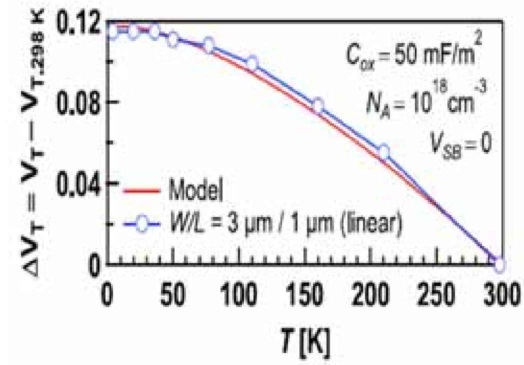
Threshold voltage





- ↓ Temp : ↑ V_{th}

Beckers, A. et al,, ESSDERC 2019; Dao, N. C. et al, Microelectron Reliab 2017.

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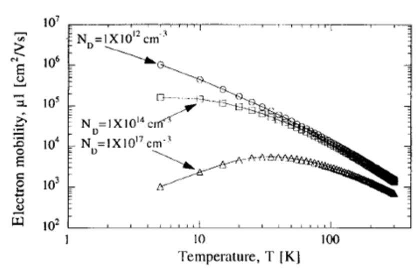
Mobility

- Lattice vibration↓
  - Effective mass↓
  - Relaxation time↑
- Coulomb scattering
  - Doping atoms, charges at interface
- Surface scattering
  - Roughness, crystal defects, open bonds etc.
- Velocity saturation
  - Higher electric field

Temperature ↓



Gutierrez-D et all Low temperature electronics : physics, devices, circuits, and applications, 2001; Balestra, F. Et al, Device and circuit cryogenic operation for low temperature electronics, 2001; Emrani, A. et al, IEEE TED 1993.

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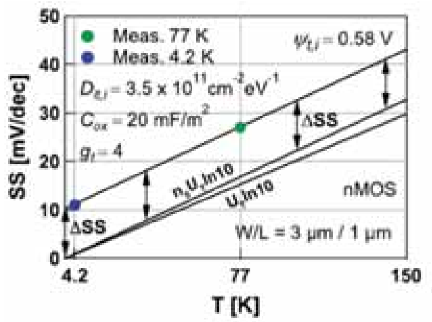
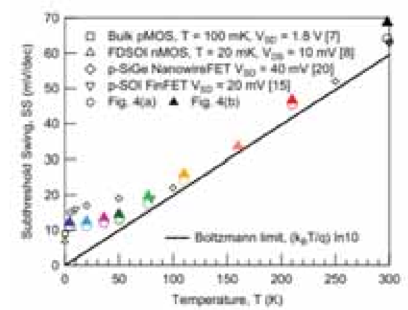
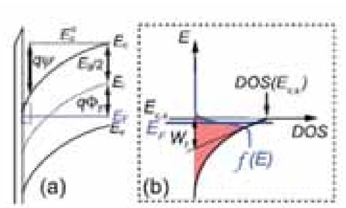
Sub-threshold Slope





$$SS = n_0 U_T \ln(10) + \Delta SS$$

- Slope factor
- Interface trap density
- Temperature independence
  - Thermal energy < band tail width



Beckers, A. et al, JEDS 2018; Beckers, A. et al, EDL 2020.

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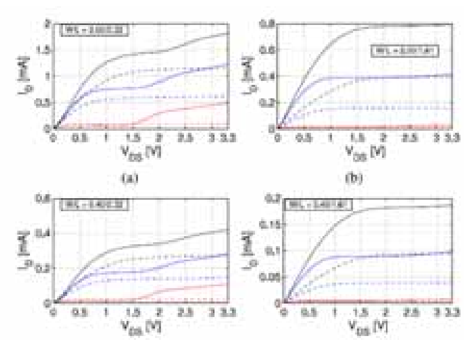
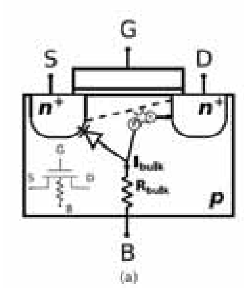
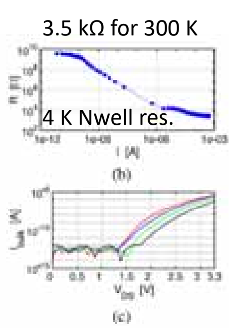
Kink effect







- Impact ionization
  - Raised bulk potential
  - Current saturates due to source-bulk forward bias
- Not present in long channel due to limited energy for impact ionization
- Not a problem in later technology due to reduced vertical field
- Very sensitive to probing

Incandela, R. M. Et al, JEDS 2018.

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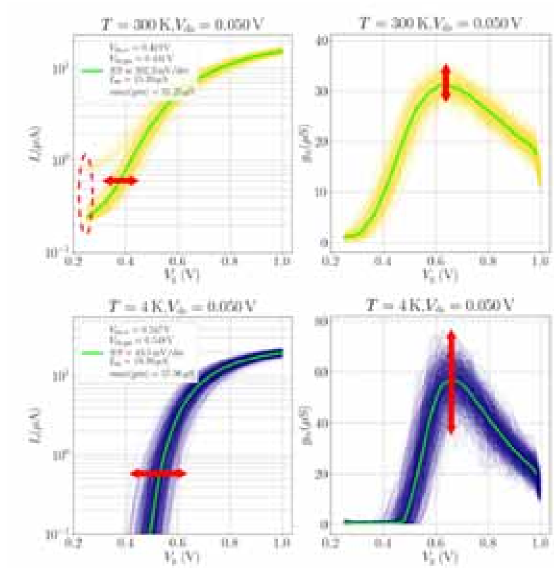
Low Temp. Variability

- 28 nm technology
  - W/L : 100 nm/28 nm
  - Linear region
  - 2000+ devices
- 4.2 K Temp : Variability ↑
  - Device to device
  - Partial doping freeze out
  - Coulomb blockage



Grill, A. et al, 2020 IEEE International Reliability Physics Symposium (IRPS)

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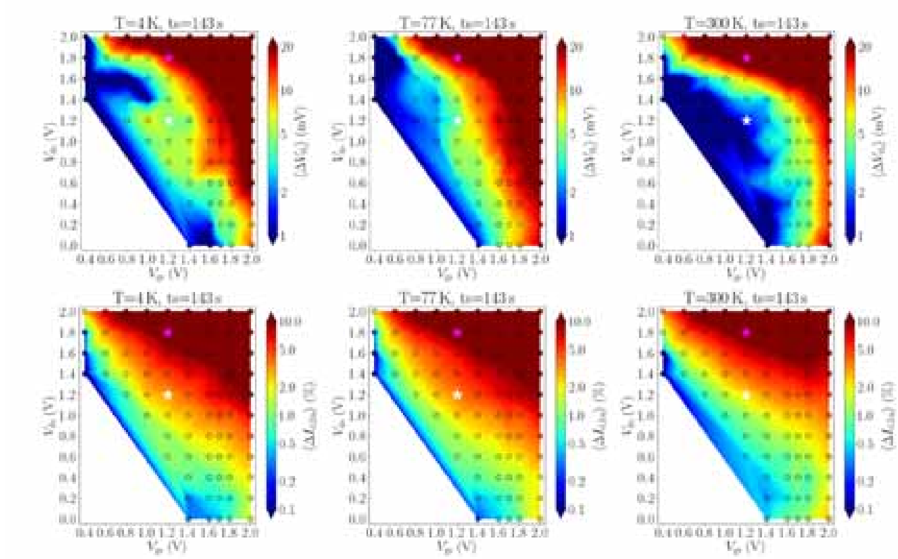
Reliability

- Significant degradation
  - Positive Bias Temperature Instability (PBTI)
  - Hot Carrier (HC)



Grill, A. et al, 2020 IEEE International Reliability Physics Symposium (IRPS)

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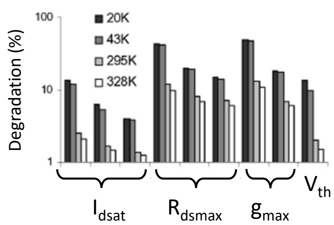
Reliability

- Parameters shown to degrade more for lower temperatures (Hot Carrier Stress)
  - Same stressing more degradation
- Same degradation stronger effect
- Not much information on low temp. reliability < 20 K



Westergard, L. et a, IRPS, 2007; Chakraborty, W. et al, 2020 IEEE IRPS.

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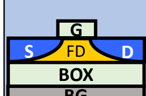
What has been tested and why?

Technology node		References	Comments
Bulk	180 nm	Huang, Gnani et al. 2020, Akturk, Holloway et al. 2010	• Easy access • Extensively investigated at various temperatures • Reliability - Larger devices → kink effect
	130 nm	Hoff, Deptuch et al. 2015	
	40 nm	Hart, Babaie et al. 2020	
	28 nm	Beckers, Jazaeri et al. 2018, Grill, Bury et al. 2020	
FDSOI 	28 nm	Nyssens et al. 2020, Pauka et al. 2021, Beckers, Jazaeri et al. 2019, gooseberry (microsoft)	• Ability to coexist with the quantum processor • Low leakage • Ability to tune for process and temperature variations • Back gate
	22 nm	Bonen, Alakusu et al. 2019	
FinFET	35 nm	Fan, Bi et al. 2020	• Latest technology • Lack information at low temperatures < 10 K
	22 nm	Horseridge, Intel	

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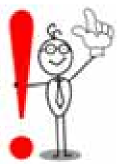
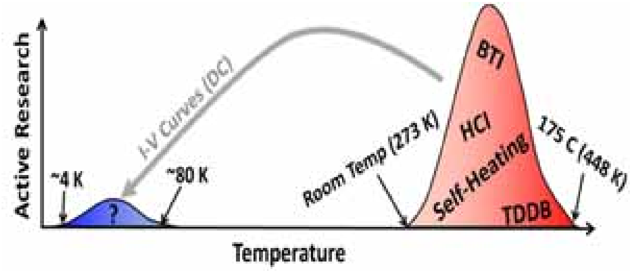
Motivation : Device Characterization

- Build device model
  - Necessary for circuit design
  - Commercial device model
    - Up to 230 K (- 40 °C)
- Understanding device physics
  - Extrapolating parameters
  - Down selecting relevant technologies
  - Account for reliability issues





RT	~4K	
Device Models	Device Model	☹
Reliability	Reliability	☹ ☹
Device Physics	Device Physics	😐

Akturk, A. et al, TED 2010; Beckers, A. et al JEDS 2018; Hart, P. A. T. et al, JEDS 2020, Grill, A. et al, 2020 (IRPS)

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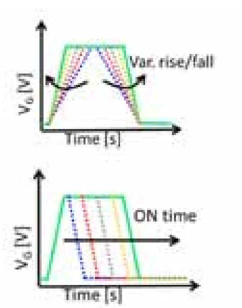
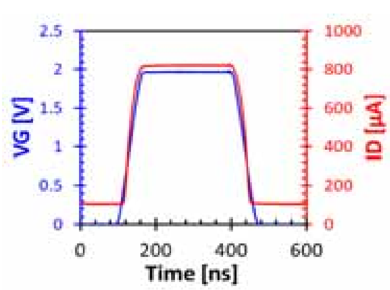
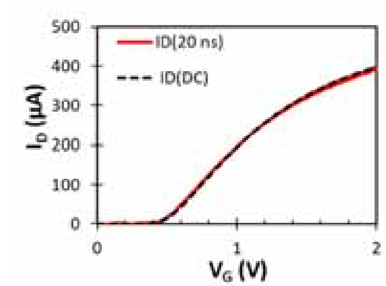
Time

- Measure dynamic response of a device
  - Fast IV : Pulsed ID-VG
- Understanding charge trapping mechanism
- Several different Fast-IV methodologies*







Device
180 nm, Si/SiO_2, 10x.18 µm

*A. Kerber, et al., IRPS (2003), C.D. Young, et al., IRPS (2005), Y. Qu, IEDM (2017), X. Yu, JEDS (2020)

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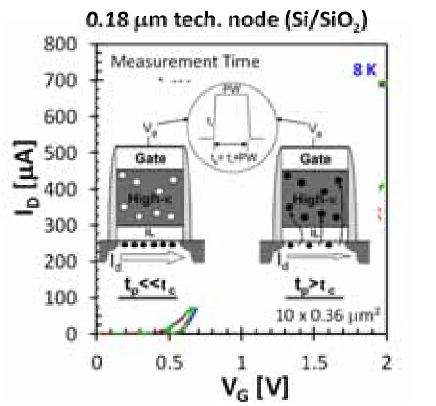
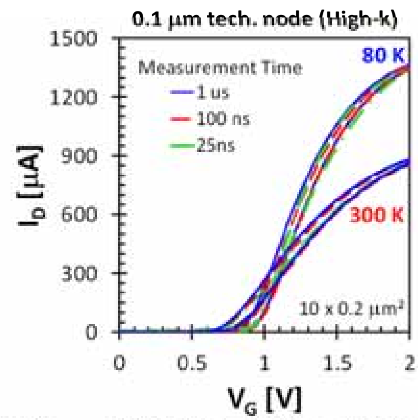
Information : Hysteresis





- Si/SiO_2 technology: limited (no) hysteresis
- High-k technology: hysteresis

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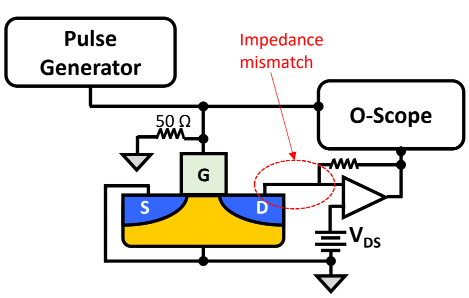
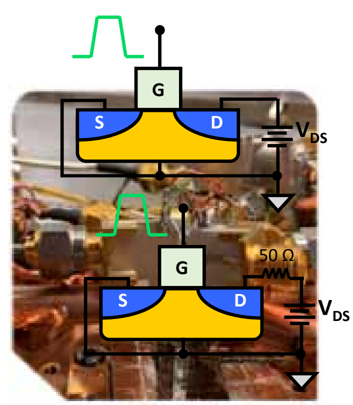
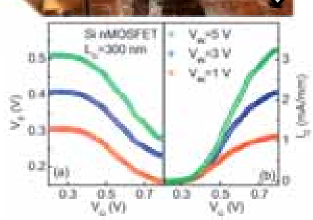
Experimental setup







- Not ground signal ground setup
- 50 Ω terminated gate
- Most of the fast measurements
  - 50 Ω at the input or directly to 50 Ω Osc.
- Amplifier acts as buffer to make sure the VD is fixed
- If amplifier not 50 Ω then must be close to the device

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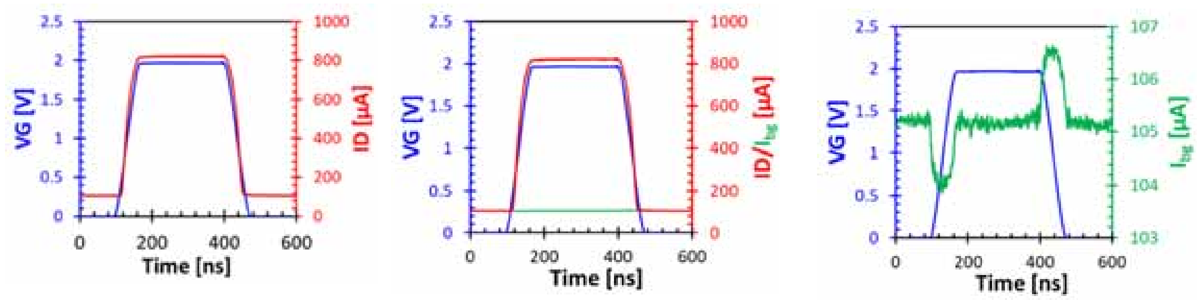
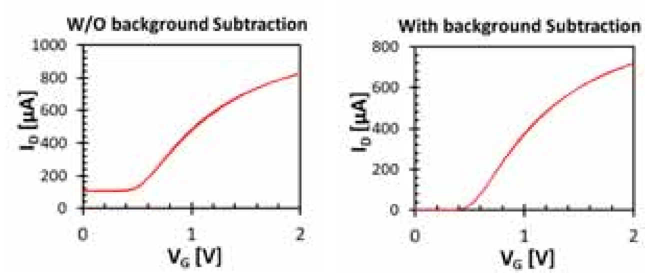
Qu, Y. et al, Microelectron Reliab 2018; Young, C. D et al, TED 2009.

Calibration



- Background subtraction
  - Amplifier offset current
  - $I_c = C\frac{dv}{dt}$
  - Any coupling of gate voltage to the output
- 180 nm, 10x.18 µm, Si/SiO_2



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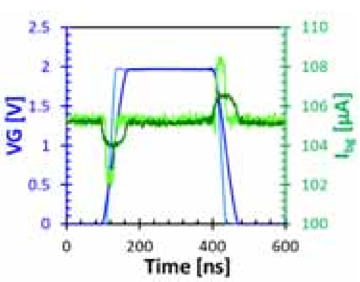
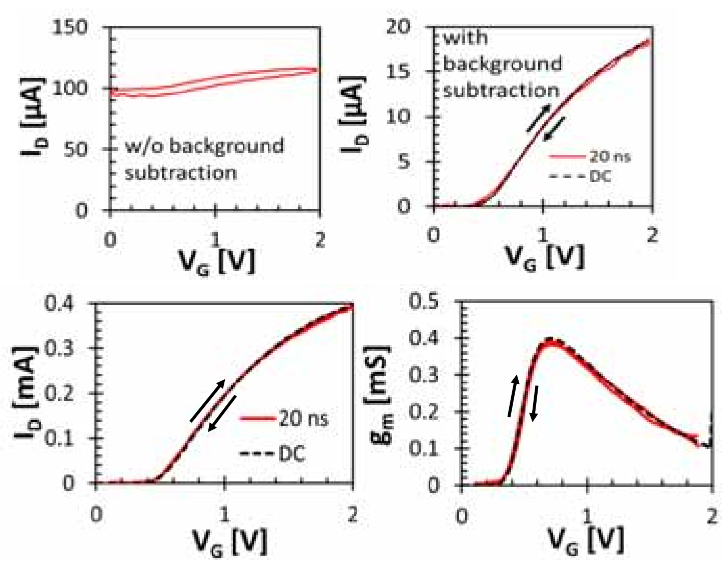
Affects of rise/fall time



Device
180 nm, Si/SiO_2, 10x.18 µm



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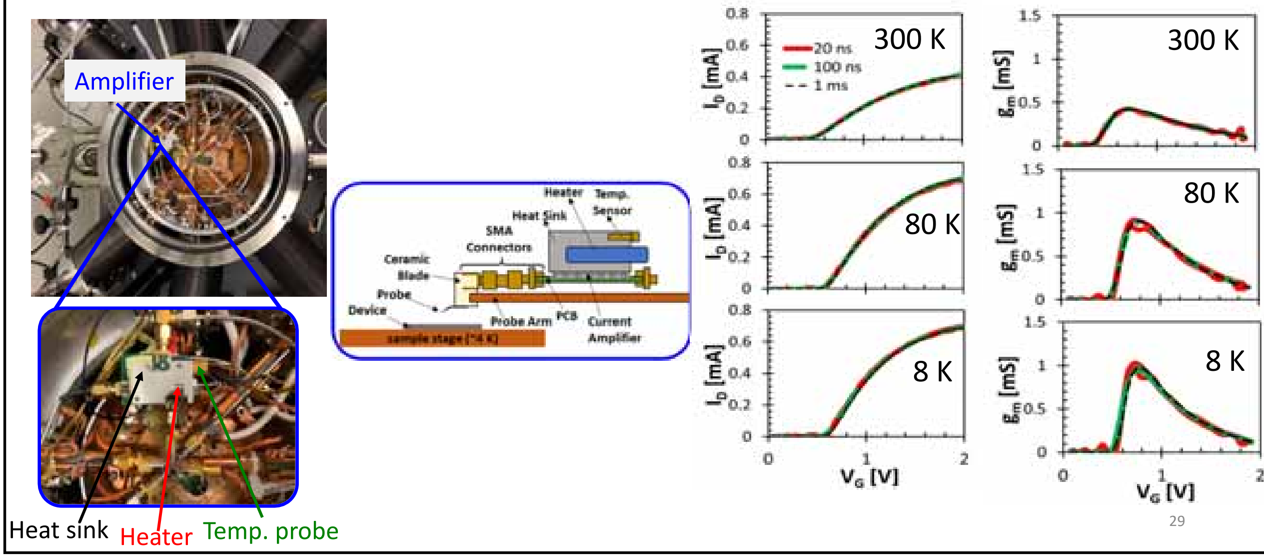
Cryogenic Fast IV Setup



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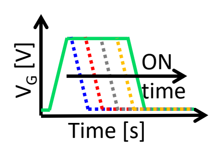
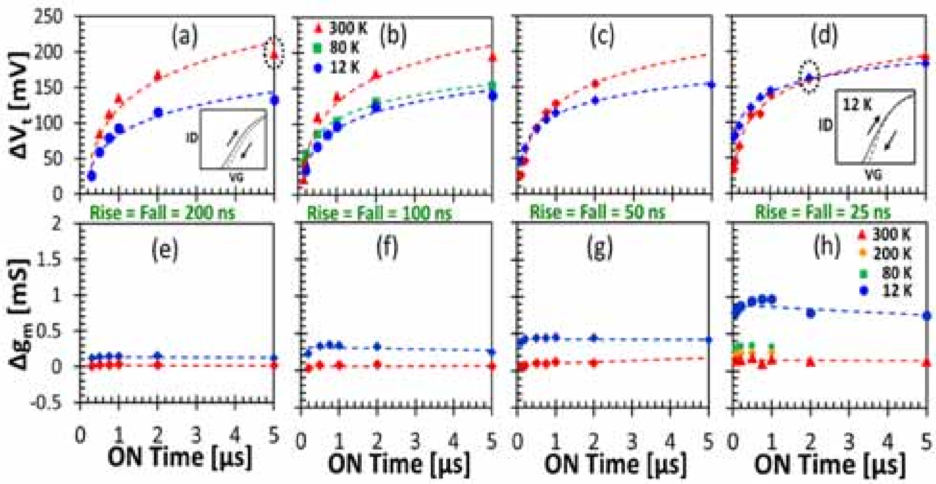
Probing non-equilibrium states



Period = 10 ms



- Electron trapping
- Slow traps
  - Oxide bulk
  - Shift in v_t
- Fast traps
  - Interface/ near interface
  - Shift in g_m

P. R. Shrestha et. al (submitted TED)

10 x 0.2 μm^2 Si/HfO_2 (3nm)

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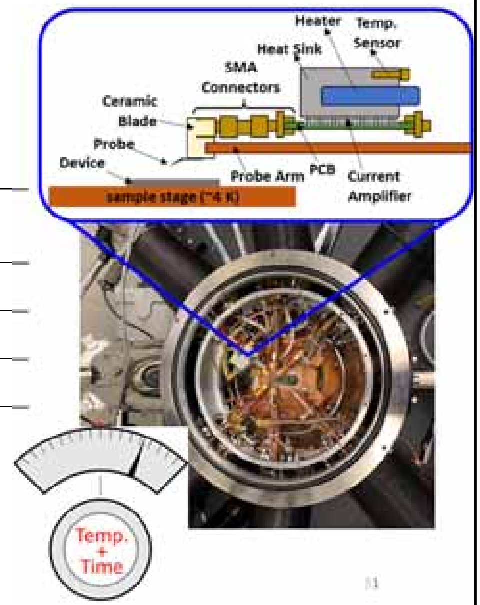
Summary

RT	~4K	
Device Models	Device Model	☹
Reliability	Reliability	☹ ☹
Device Physics	Device Physics	😑



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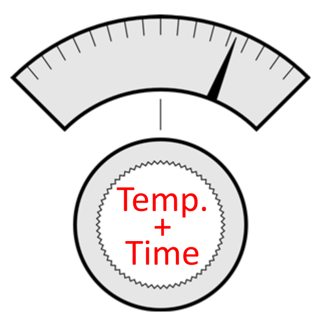
Future Work

- Device Characterization
  - Quantum computing and high-performance computing
  - Development of future technologies
- Measure “exotic” parameters
  - Sub-threshold swing
  - Series resistance



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