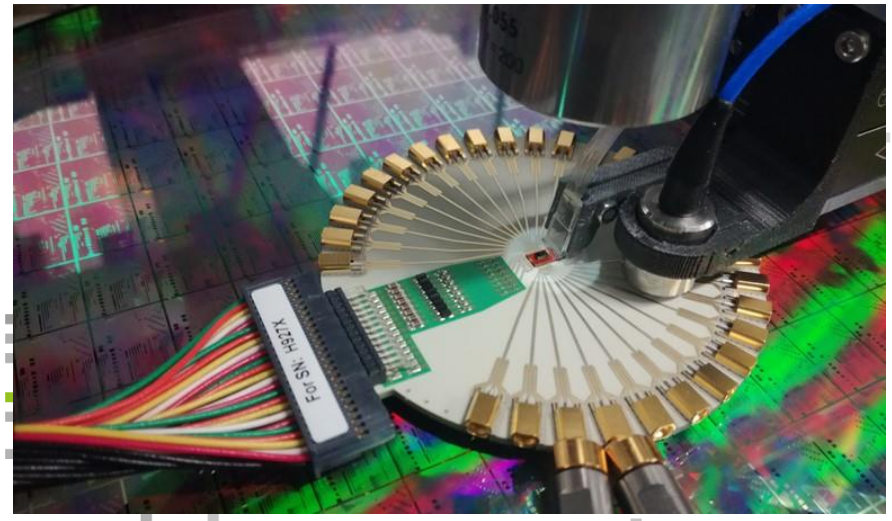
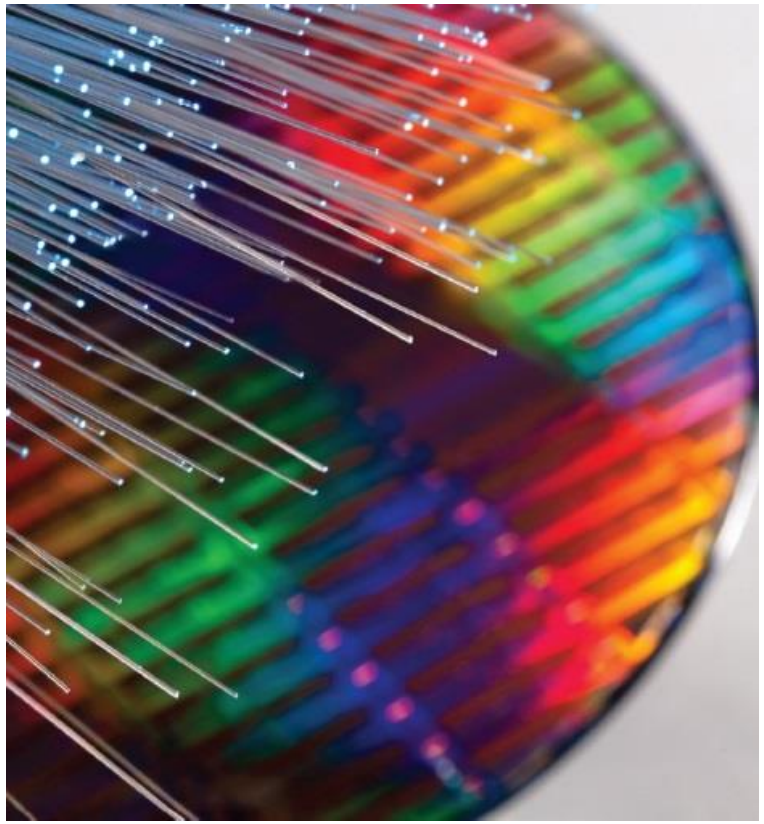


ADVANCED PACKAGING FOR SILICON PHOTONICS BASED MODULES AND APPLICATIONS

EPS Webinar| Stéphane Bernabé | 25.06.19

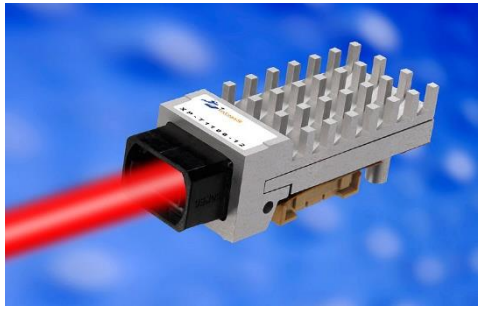
OUTLINE

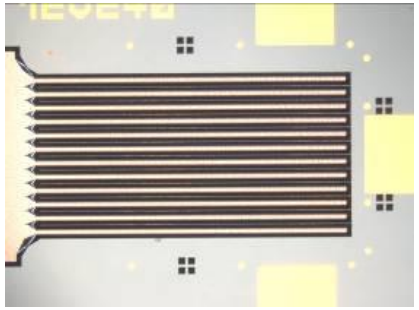
- **Silicon Photonics**
  - Promises
  - Challenges
  - What can advanced packaging bring to PIC modules ?
    - Some work in progress

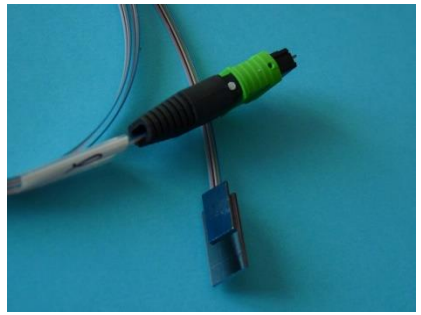


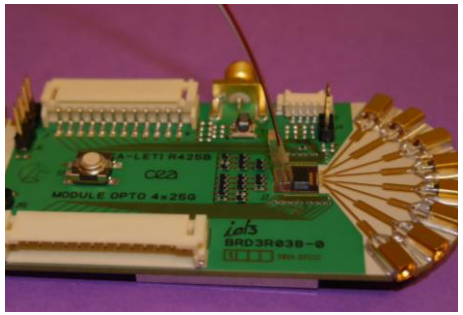
BIO

Bio: Stéphane Bernabé is the head of the Photonic Packaging Lab at CEA-LETI, Grenoble, France. His field of expertise is in Photonic Integrated Circuit packaging, Module integration (VCSEL and PIC), and Electronic/Photonic convergence for advanced applications of PICs. He previously led several R&D projects dealing with these topics and is currently involved in the EU-funded projects MASSTART, PIXAPP, and TINKER. He has also overseen module and packaging developments in companies Radiall and Intexys Photonics. He's a member of the Electronics Packaging Society (IEEE-EPS) and acts as committee member in the ESTC and ECTC conferences. He has co-authored 50 papers, 3 book chapters and holds 15 patents in the field of photonics packaging.









CEA-LETI AT A GLANCE

© JM. Francillon/CEA

Founded in 1967, based in France (Grenoble) with offices in USA and **Japan**

"3rd Innovative Public Research Organization Worldwide" 2012 -2020

Derwent™
A Clarivate Analytics company

Since **1967**

2,000 people

Patents:
- > 3,000 in portfolio
- 40% under license agreement

Startups:
- 68 created for 20 years (75% in activity)
- 3500 jobs created

Cleanrooms:
- 500 state-of-the-art equipment in 200 & 300 m²
- 10 000 square meters cleanroom

Budget:
- 315 M€
- 85% from R&D contracts

OPTICS & PHOTONICS DIVISION

- 12600 m² incl. offices, labs and clean rooms
- Dedicated clean rooms for III-V and II-VI materials (growth, epitaxy, process and packaging) on versatile substrate geometries up to 150 mm
- Electro-optical test and characterization facilities
- Design and simulation capabilities for process, growth, optics

400 people

Patents:
- 80 per year
- > 700 in portfolio
- 40 **%** under license agreement

Budget:
- 70 M€
- 90% from R&D contracts

CEA-LETI 8,500 m² CLEAN ROOMS for 200mm & 300mm wafers

LETI PHOTONICS DIVISION

Our mission : innovate by miniaturizing and integrating optical components for our industrial partners

Display

High brightness and 3D display components and systems

High-end Infrared Imaging

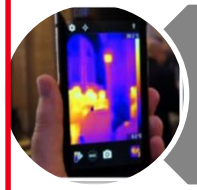
High performance IR image sensors for military, space and industrial applications

X and γ imaging systems

Security, non destructive test, healthcare

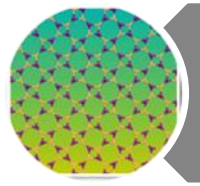
Integrated optics on Si

Integrated transceiver, receivers and sensors on silicon, VCSELs



Thermal and THz imaging

Toward low cost microbolometer matrices for consumer applications

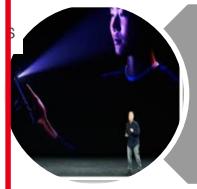


Materials

Crystal growth, epitaxy, substrate preparation

Optical sensors

MIR integrated gas sensors and analyzers. Particle detection



CMOS image sensors

Advanced image sensors and systems for 3D imaging

Semiconductor process

Miniaturization and integration technologies from 100 to 300 mm

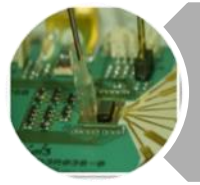
Solid-state lighting

LED matrices for industrial and automotive applications

3D imaging systems

Compact, smart, low cost lidars

3D image modules

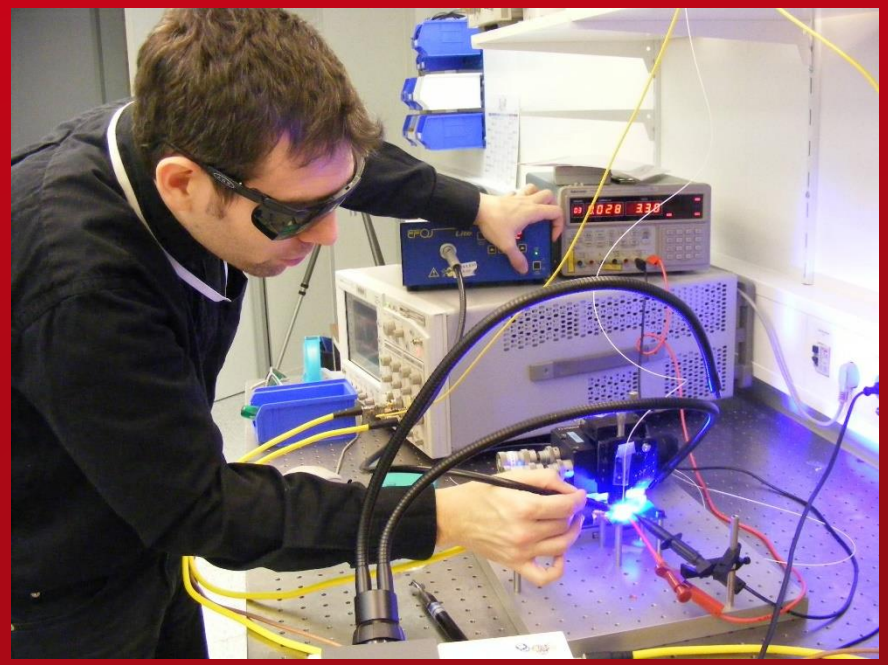


Packaging and assembly

Optics-electronics assembly, optical interfaces, component curvature

A SHORT HISTORY OF INTEGRATED OPTICS PACKAGING

BASED ON MY OWN EXPERIENCE ON ALIGNING, GLUING AND TESTING FIBERS TO PICS



EARLY STUDIES ON INTEGRATED OPTICS PACKAGING (70'S)

End fire coupling between optical fibers and diffused channel waveguides

W. K. Burns and G. B. Hocker

W. K. Burns is with U.S. Naval Research Laboratory, Washington, D. C. 20375; G. B. Hocker is with Honeywell Corporate Research Center, Bloomington, Minnesota 55420.

Received 24 February 1977.

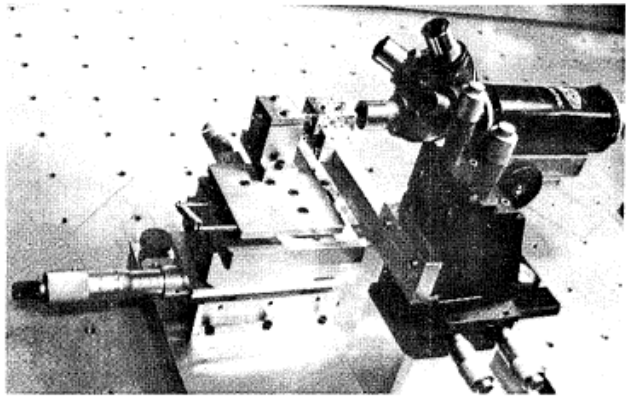


Fig. 1. Connecting equipment.

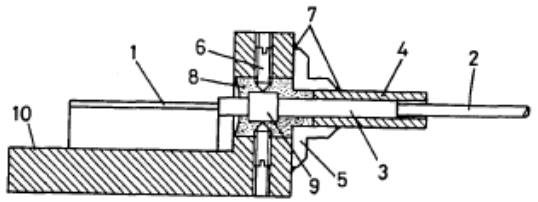


Fig. 2. Structure of the connection jig. This view shows the state after fixing the fiber to the waveguide—1: strip waveguide; 2: fiber; 3: stainless steel pipe; 4: sleeve; 5: flange; 6: set screws; 7: adhesive paste; 8: molder; 9: square block; 10: case.

Single-mode optical-waveguide fiber coupler

Juichi Noda, Osamu Mikami, Makoto Minakata, and Masaharu Fukuma

A single-mode fiber coupler to the Ti diffused $LiNbO_3$ strip waveguide has been devised. The influences of three axial displacements and two angular misalignments on the coupling efficiency have been investigated at 6328-Å wavelength. The coupler has a special feature wherein coupling degradation caused by fiber displacement after connection can be recovered to the initial state. The total optical insertion loss is 3 dB after fixing the fiber to the $LiNbO_3$ strip waveguide, which is 4 μm wide and 8 mm long.

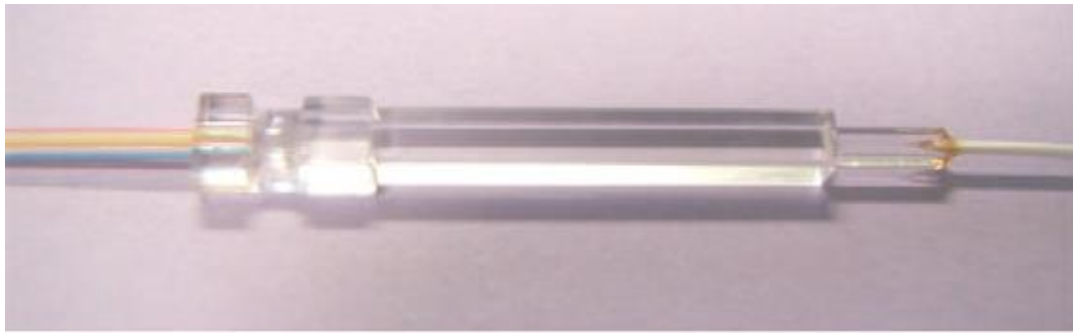
A waveguide to single-mode fiber coupler has been devised, and its coupling characteristics have been investigated experimentally. This method can provide highly accurate optical alignment between a fiber and a waveguide and is applicable for connecting a laser source or a detector to a fiber. The coupler has a special feature wherein degradation in coupling, yielded by fiber displacement after the connection, can be reset to the initial state. Present coupling loss is large because of insufficient optical field overlap between the fiber and the waveguide. Therefore, further technical improvement to fabricate the waveguide with the optical field close to that of the fiber is necessary for coupling loss reduction. Especially, Li_2O out-diffusion is one of the difficult problems which must be overcome in fabricating a narrow strip waveguide. More detailed investigation on coupling efficiency degradation due to aging effect or temperature variation will be made.

2K YEARS : PIGTAILING IS BECOMING MATURE

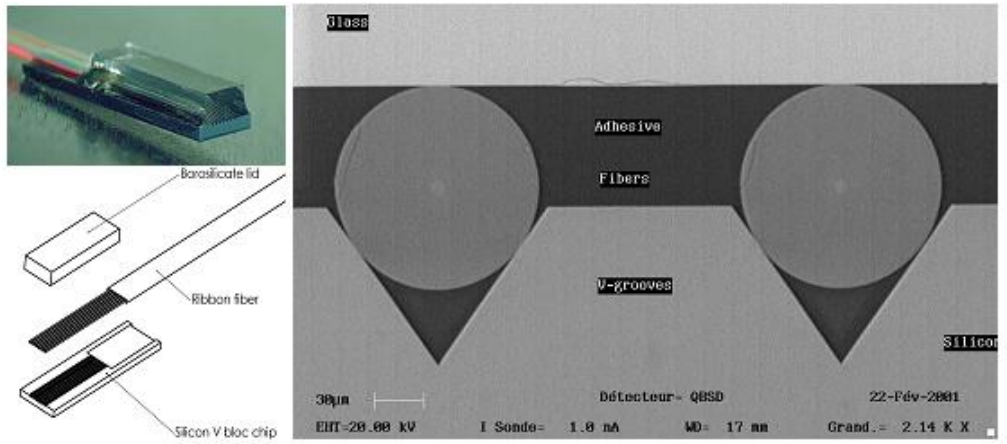
Boom of optical devices

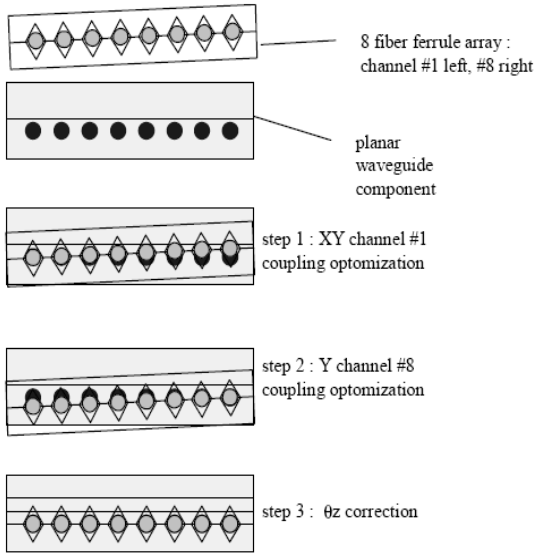
Several PIC technologies :

- Glass
- Silica On Silicon
- Lithium Niobate (for modulators)
- ASOC from Bookham (thick SOI)



Glass optical 1x8 splitter, from Teem Photonics





WHAT A PACKAGING ENGINEER SHOULD KNOW ABOUT (SINGLEMODE) PHOTONICS

PIC mode

$$\psi_b = \sqrt{\frac{2}{\pi w_x w_y}} \exp\left(-\frac{x^2}{{w_x}^2}\right) \exp\left(-\frac{y^2}{{w_y}^2}\right)$$

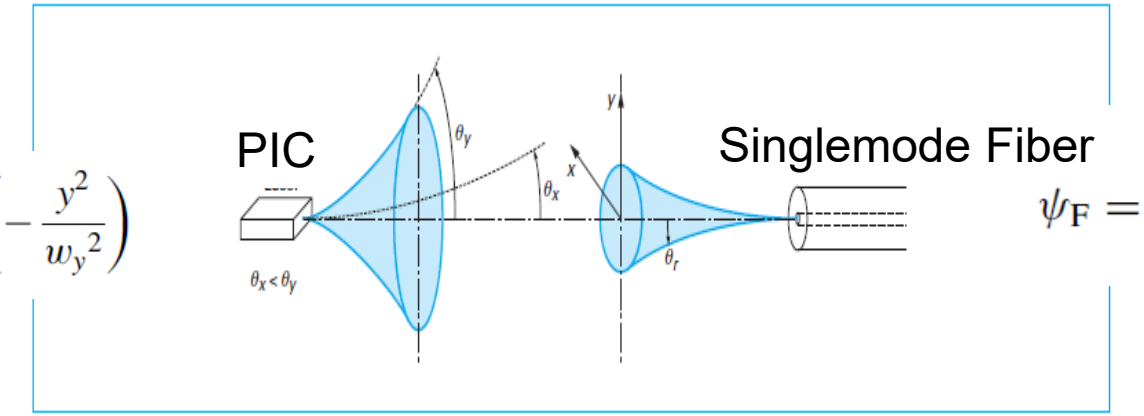


Figure 11 – Schéma de couplage entre une diode laser et une fibre optique

Fiber

$$\psi_F = \sqrt{\frac{2}{\pi}} \frac{1}{w_F} \exp\left(-\frac{r^2}{{w_F}^2}\right)$$

Coupling Efficiency

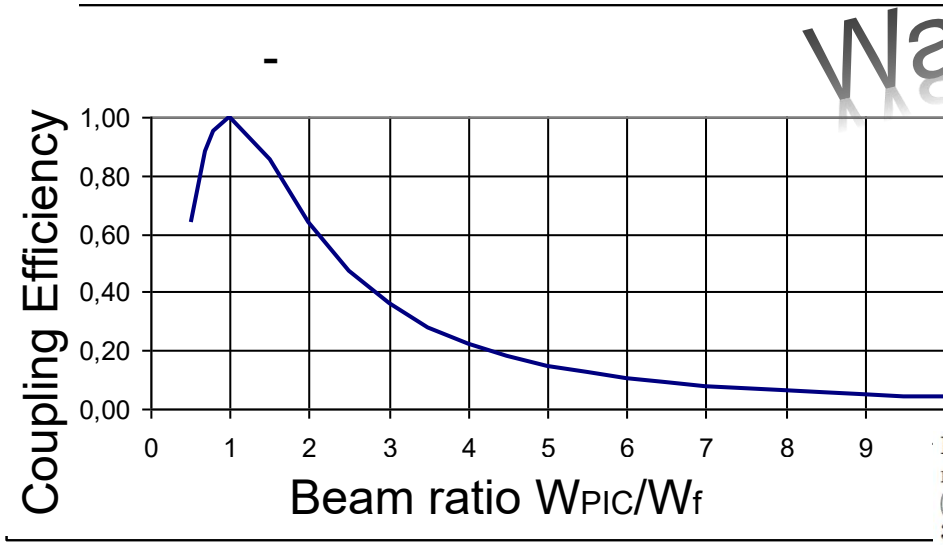
$$\eta = \frac{4}{\left(\frac{\omega_{0x}}{\omega_f} + \frac{\omega_f}{\omega_{0x}}\right) \cdot \left(\frac{\omega_{0y}}{\omega_f} + \frac{\omega_f}{\omega_{0y}}\right)}$$

$$\eta_{opt} = \frac{4\varepsilon}{(\varepsilon+1)^2}$$

ε : Ellipticity of PIC beam

Available in the following configuration :

- Butt coupling (z=0, no gap)
- No tilt
- No offset along x nor y



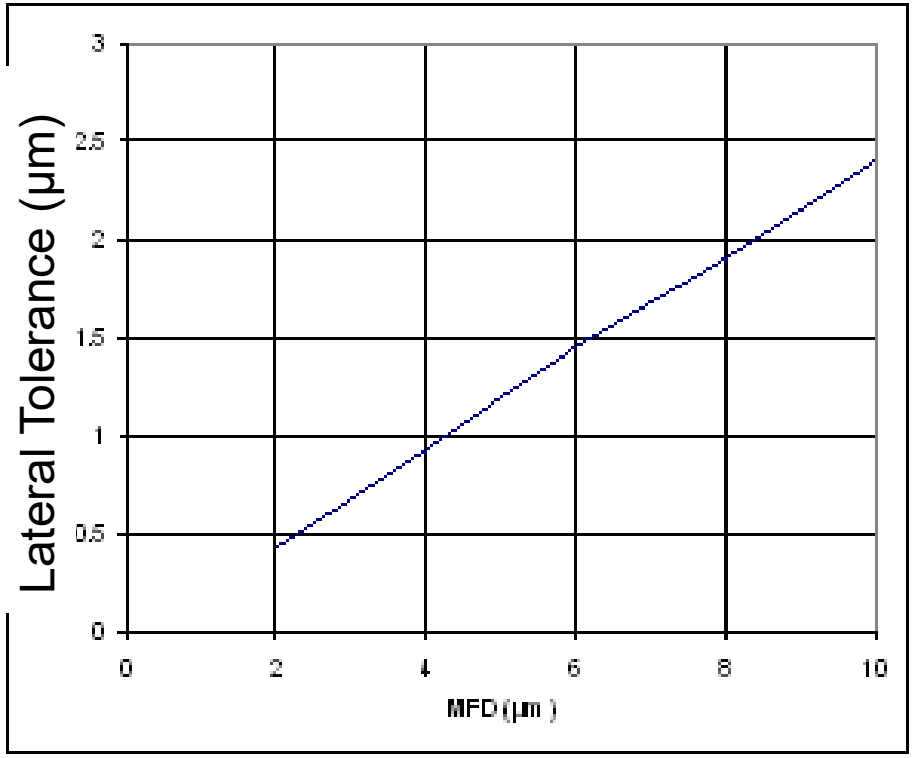
Waist is the key !

H. Kogelnik, "Coupling and conversion coefficients for optical modes," in *Microwave Research Institute Symposia Series* 14 (Polytechnic Institute of Brooklyn, New York, 1964), pp. 333–347.

W. B. Joyce, "Alignment of Gaussian beams," Appl. Opt. **23,** 4187–4196 (1984).

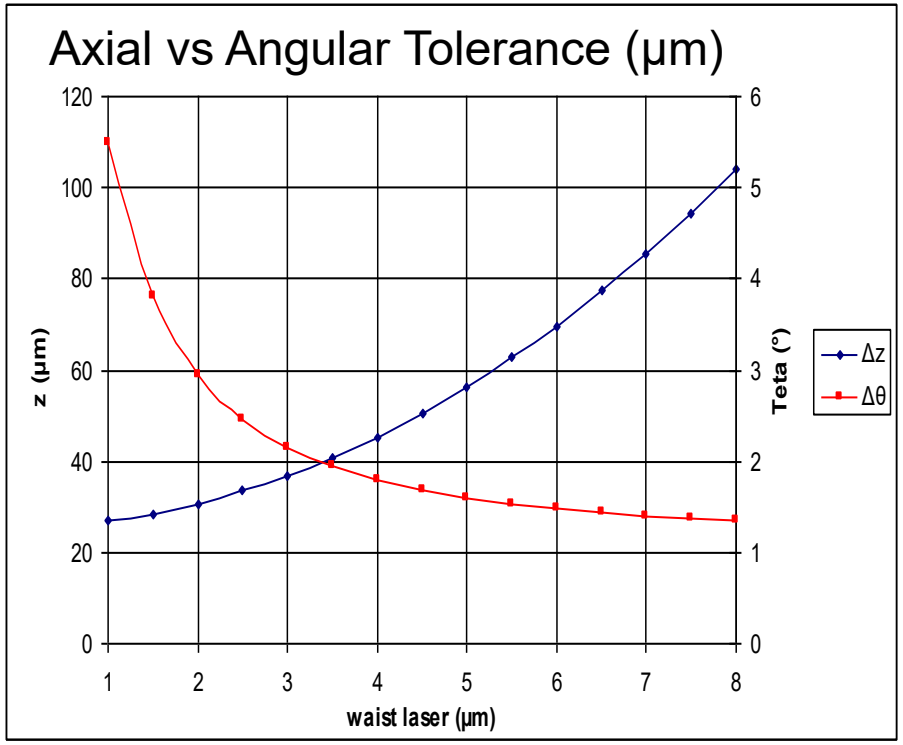
WHAT A PACKAGING ENGINEER SHOULD KNOW ABOUT (SINGLEMODE) PHOTONICS (2)

PIC packager Golden rule

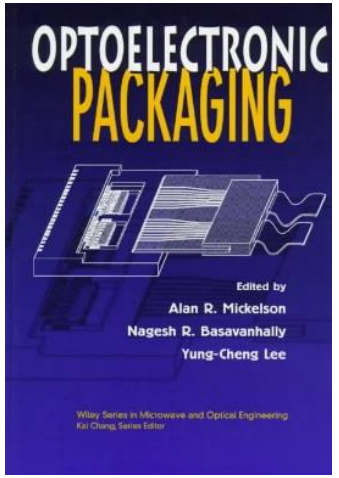


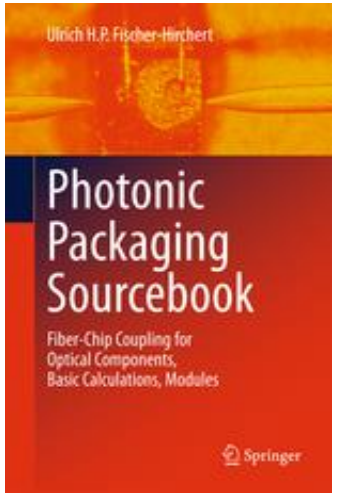
$$\Delta x = 0.33\sqrt{\left(\omega^2 + \omega_f{}^2\right)}$$

The offset/tilt trade-off

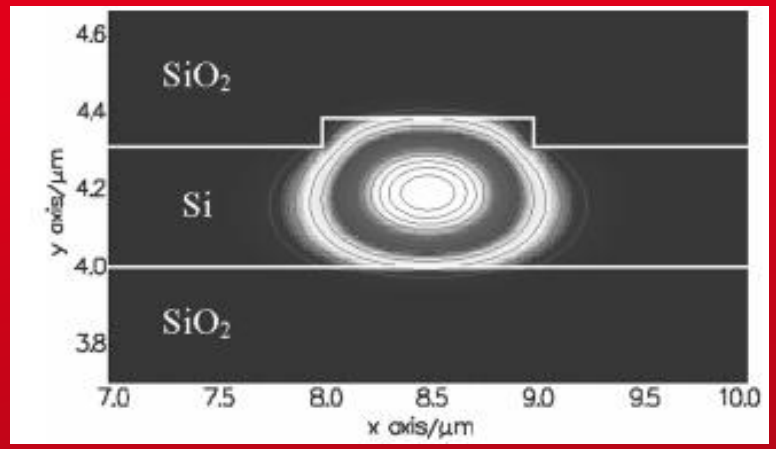


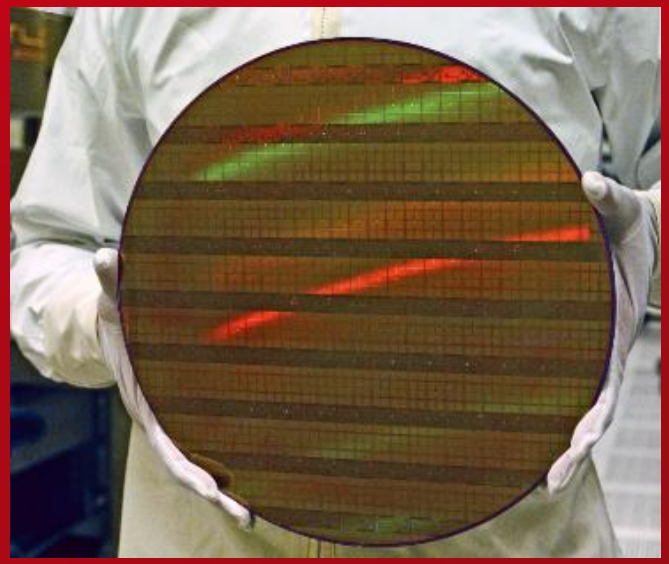
$$\Delta\theta = 60\frac{\lambda}{\pi^2}\sqrt{\frac{1}{\omega^2} + \frac{1}{\omega_f{}^2}}$$





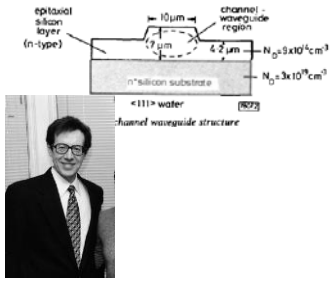
SILICON PHOTONICS : PLATFORM & ROADMAP





HISTORY

***1985 Soref's** paper on Si optical properties for modulation*



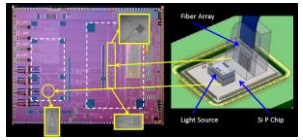
***1988-2003 Bookham** ASOC devices*

Bookham TECHNOLOGY

Thinking optical solutions

2001 Luxtera creation

LUXTERA



2016 : Intel, Acacia, MACom… launch SiPho products

Intel launches silicon photonics

The product, 16 years in the making, provides a solution as the cost of fiber optics in the datacenter grows.

By Stephanie Condon for Between the Lines | August 17, 2016 -- 17:15 GMT (08:15 BST) | Topic: Data Centers

2019 Cisco completes acquisition of Luxtera

2019 400G SiPho transceiver (Intel, Inphi, …)

TOWERJAZZ The Global Specialty Foundry Leader — Inphi Think fast

THE BELL SYSTEM
TECHNICAL JOURNAL

DEVOTED TO THE SCIENTIFIC AND ENGINEERING ASPECTS OF ELECTRICAL COMMUNICATION

Volume 48 — September 1969 — Number 7

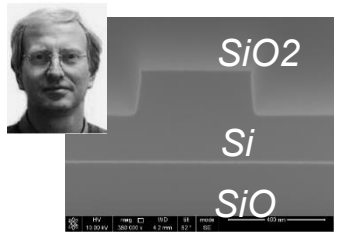
Integrated Optics: An Introduction

By STEWART E. MILLER

This paper outlines a proposal for a miniature form of laser beam circuitry. Index of refraction changes of the order of 10^{-2} or 10^{-3} in a substrate such as glass allow guided laser beams of width near 10 microns. Photolithographic techniques may permit simultaneous construction of complex circuit patterns. This paper also indicates possible miniature forms for a laser, modulator, and hybrids. If realized, this new art would facilitate isolating the laser circuit assembly from thermal, mechanical, and acoustic ambient changes through small overall size; economy should ultimately result.

from I.P. Kaminow, J. LT, 26,9,2008

***2002 J.M. Fedeli** Pioneered SiPho at Leti*

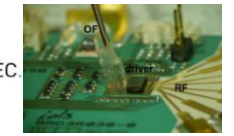


***2008-2012** HELIOS project*

heliOs

2012-… III-V Lab IRT Nanoelec

NANOELEC



III-V lab

DFB@1310nm + 32G EAM + SOA

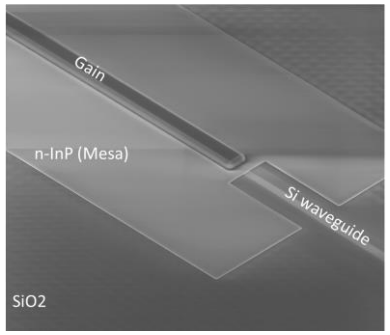
2017 O-Band MPW offer

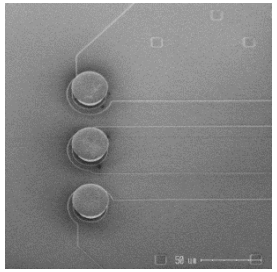
cmp

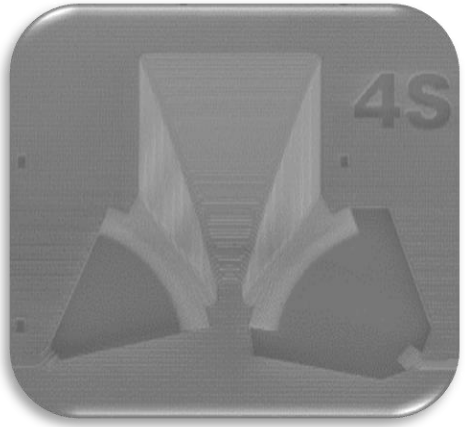
SCINTIL PHOTONICS

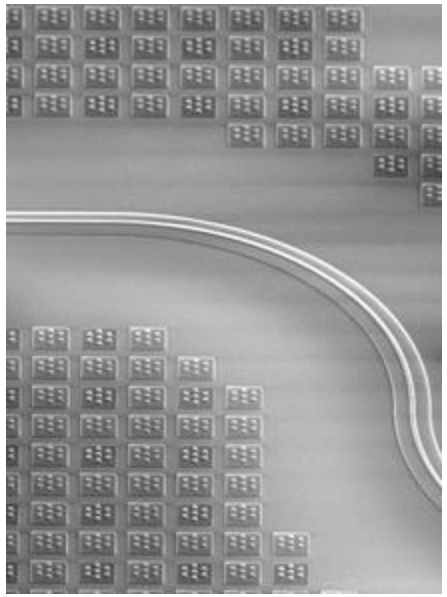
2021 Scintil Spin-off

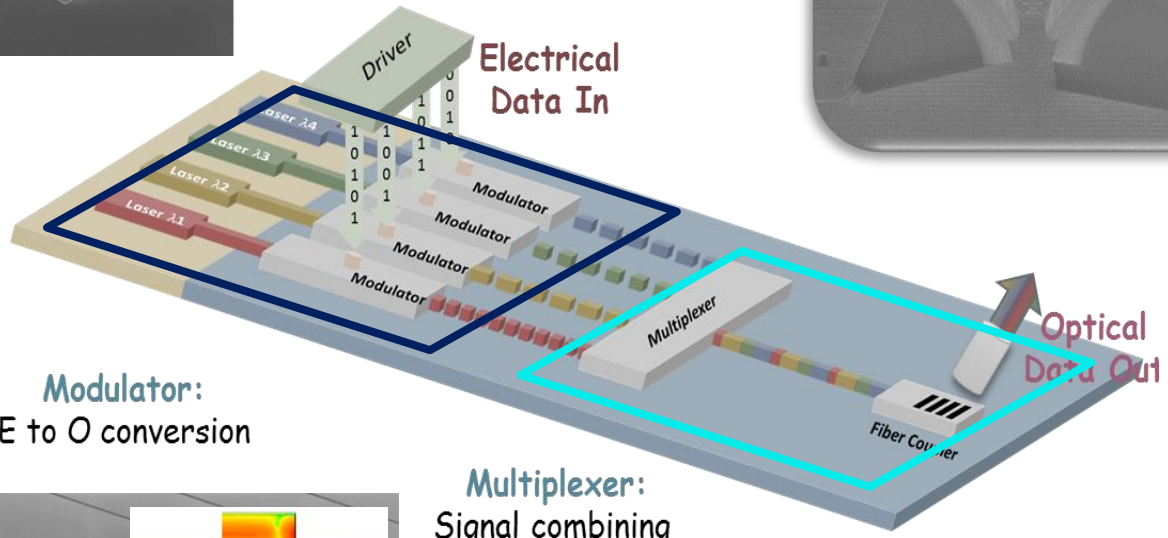
SILICON PHOTONICS PLATFORM

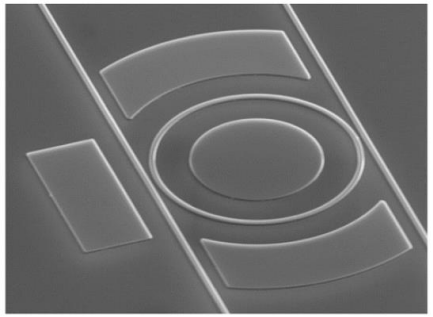






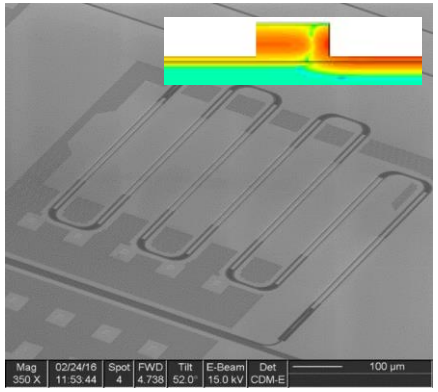


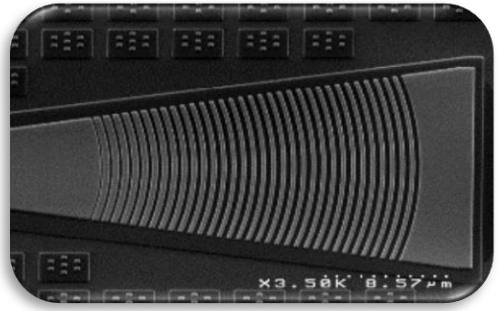




Modulator:
E to O conversion

Multiplexer:
Signal combining





SILICON PHOTONICS : TECHNOLOGY OVERVIEW

Silicon Implantation
- Modulator junction formation & activation

Silicon Patterning
- Define all the photonic devices
- Several silicon thicknesses and waveguide architectures

Germanium Epitaxy
- Photodetector patterning
- Germanium selective epitaxy

Germanium Implantation
- Photodetector contact formation

CMOS-based process with photonic dedicated optimizations

Silicon Photonic Process Flow

Silicidation
- Si Modulator contact silicidation

CMOS standard process

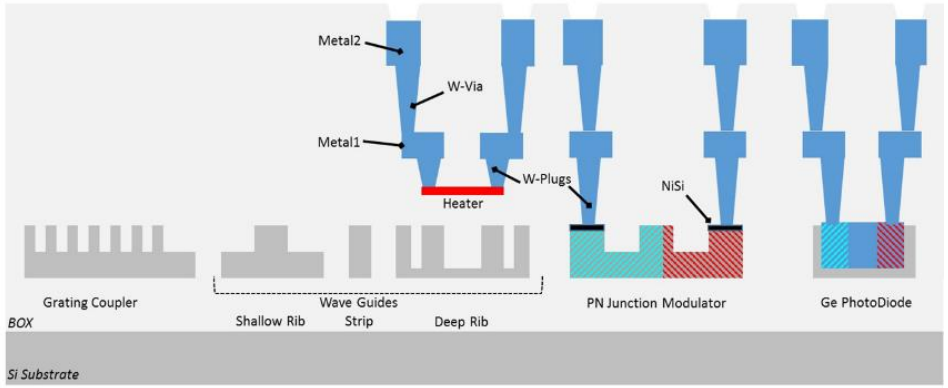
BEOL
- Metal interconnection
- Metal heater definition for wave length tuning

Far BEOL
- Cupi
- TSV
- RDL

OSAT standard process

Silicon On Insulator (SOI) substrate : ∅8" or ∅ 12"

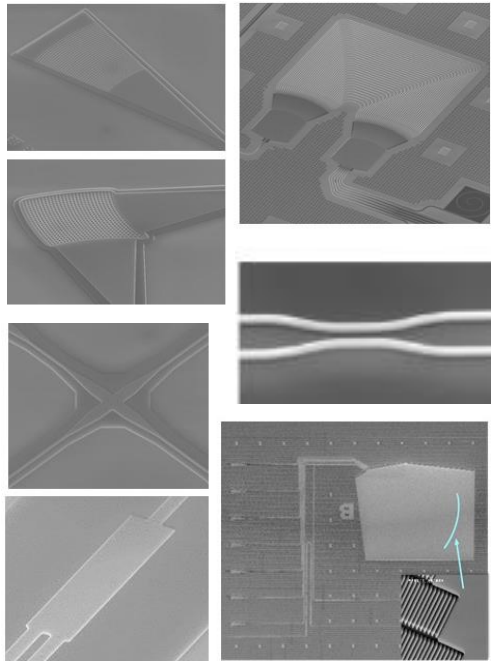
Schematic cross section of a silicon photonic circuit (Leti)

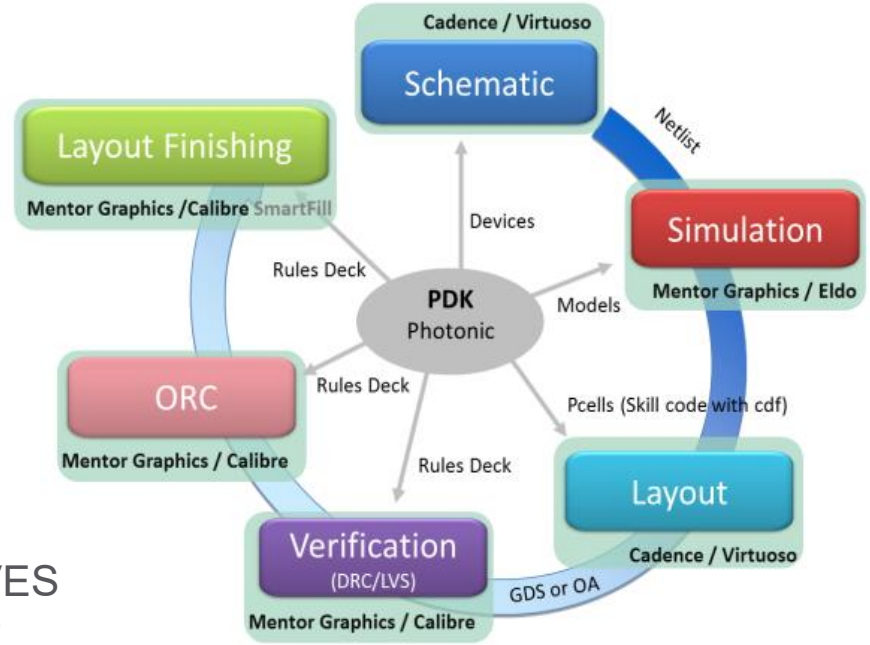


DEVICE LIBRARY AND PROCESS DESIGN KIT AVAILABLE

PASSIVES

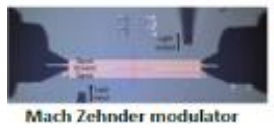
O-BAND & C-BAND
Rib, deep rib, strip, rib MM, bend strip, bend rib, bend deep rib, fiber grating coupler 1/2D, directional coupler, transitions, ring filter, MMI…

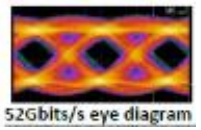


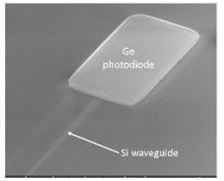


ACTIVES

O-BAND
Mach-Zehnder Modulator, ring racetrack modulator, Ge photodiode PIN longitudinal







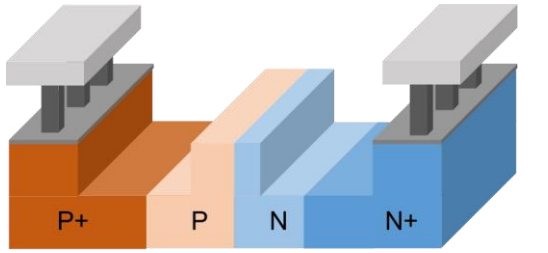
PhoeniX Software
Solutions for Micro and Nano Technologies

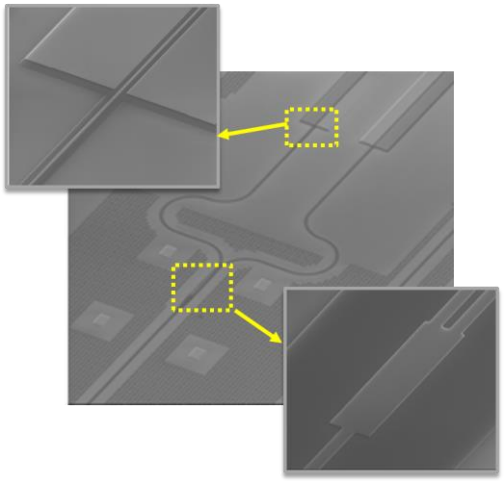
cadence

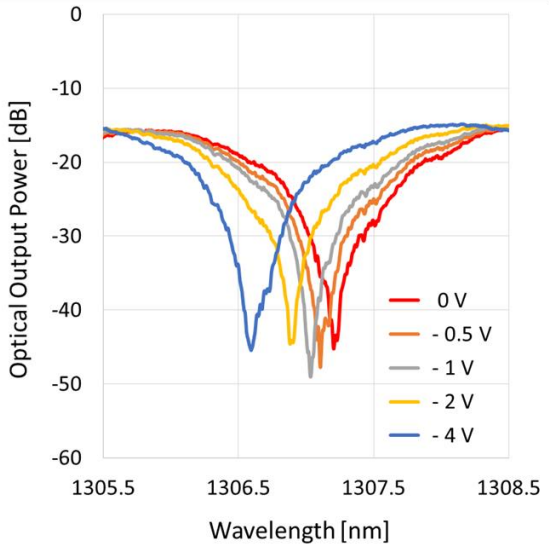
Mentor
A Siemens Business

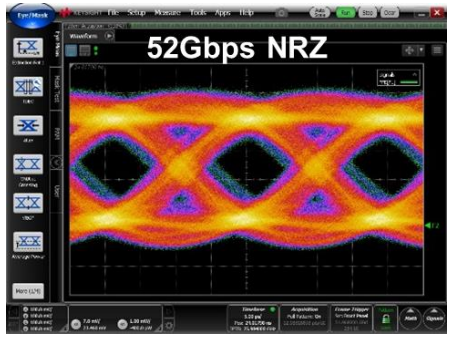
SILICON PHOTONICS PLATFORM

Carrier depletion in PN/PiN diode (reverse bias) for High Speed Modulation Section









Szelag B, et al. Optimization of 64Gbps O-band thin-rib PN junction. Mach- Zehnder Modulator fabricated on a 200mm silicon photonics platform. SSDM 2018.

Ge epitaxy in cavity for High Speed Ge PIN Photodiodes

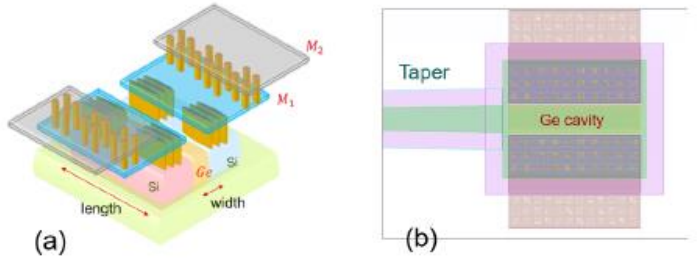


Figure 3. (a): Si/Ge/Si photodiode stack-up layers view. (b) Photo-diode planar view

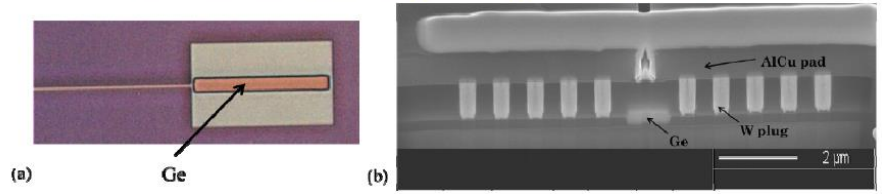
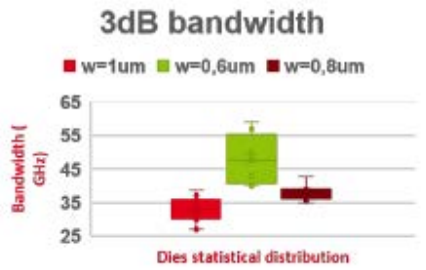
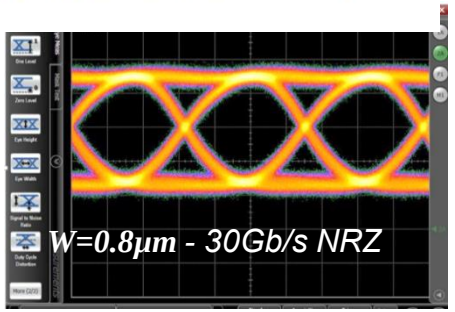


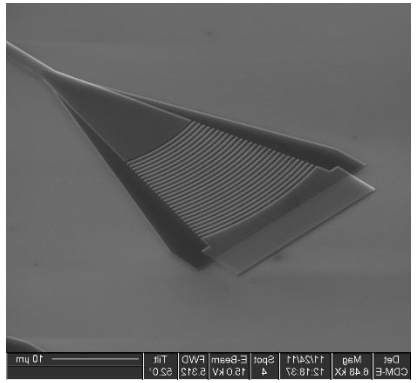
Fig. 3. (a) Top-view of a fabricated 1 µm wide Ge cavity after CMP. (b) Cross-sectional SEM image of a 1 µm wide Ge cavity photodiode.

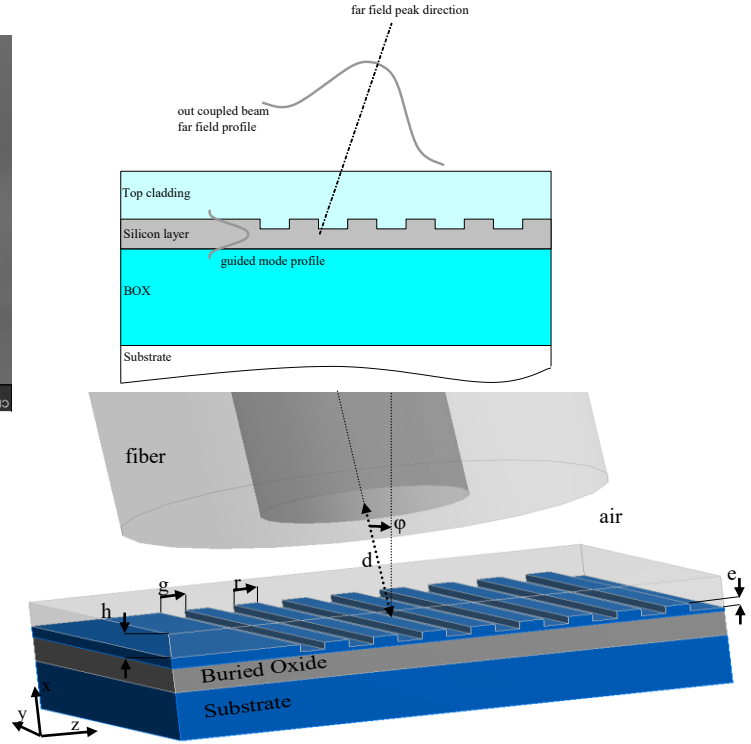


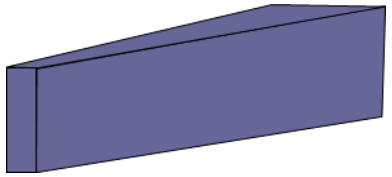


H. Zegmout *et al.*, « High speed integrated waveguide lateral Si/Ge/Si photodiodes with optimized transit time », 2020, vol. 11285.

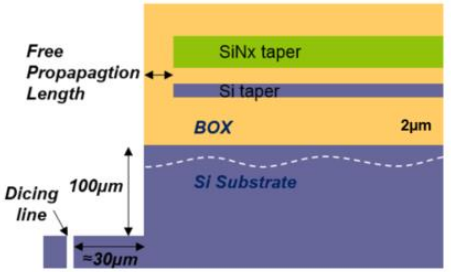
COUPLING STRUCTURES

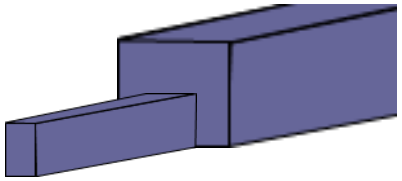




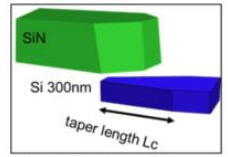


Si 300nm taper

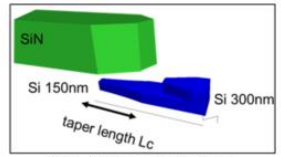




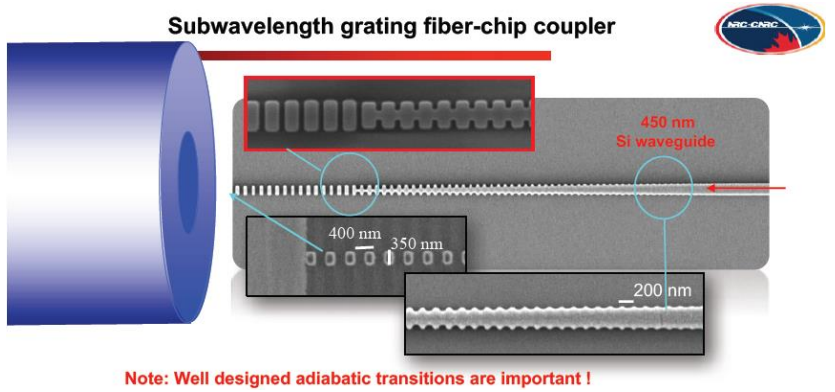
Si 150nm/300nm taper



SiN$_x$ 600nm-Si 300nm



SiN$_x$ 600nm-Si 150nm



Vertical Grating coupler

- 50% to 80% efficiency for 1 polarization
- Ideal for waferscale testing
- Limited bandwidth
- Alignment tolerance: +/- 2 µm (well fitting mode size)

Adiabatic taper coupler for Edge Coupling

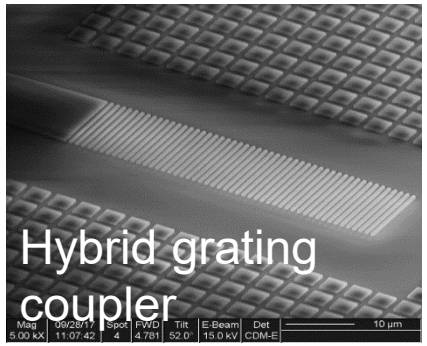
- Broadband
- Small mode size (3µm diameter)

ADVANCED COUPLING STRUCTURES

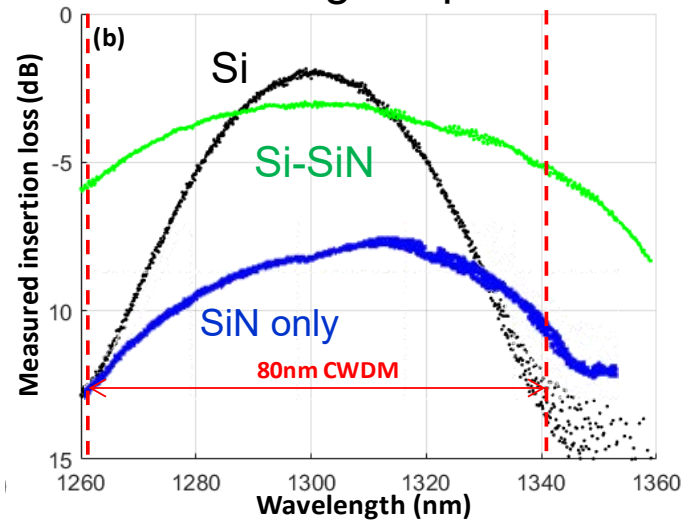
SiN-Si hybrid grating coupler

- 2-layers grating SiN-Si
- 2.8 dB insertion loss
- -1dB BW ~ 50nm

→ CWDM components wafer level testing (broadband)



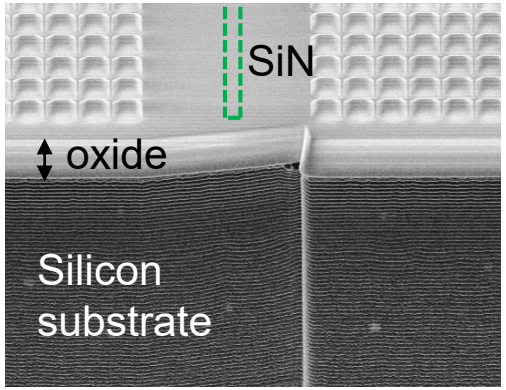
Grating couplers

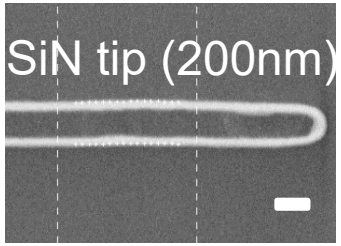


Q. Wilmart et al., Appl. Sci. (2019)

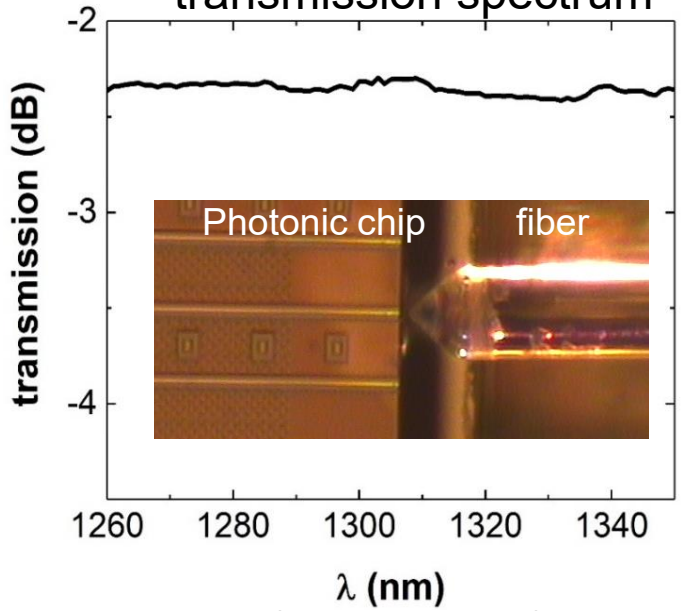
Edge coupler with SiN taper

- Lensed fiber : MFD = 2.5µm
- SiN inverse taper
- Deep trench by dry etching
- Coupler insertion loss : **< 2.4dB** (O-band)
- For CWDM modules

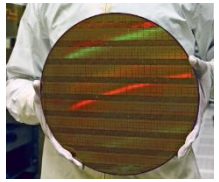


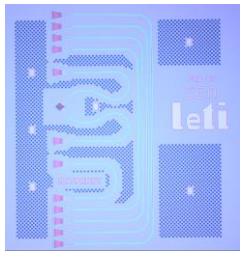


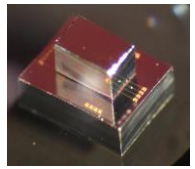
Edge coupler transmission spectrum

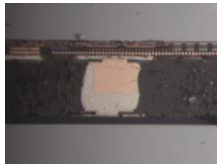


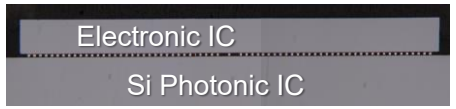
SILICON PHOTONICS MODULE ASSEMBLY FLOW







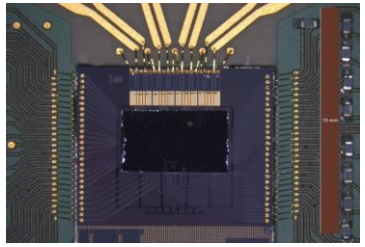


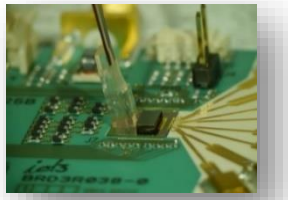


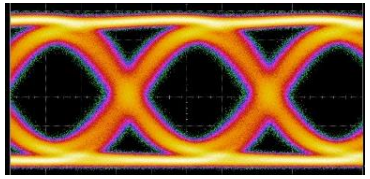
PIC fabrication → Wafer level test → Chip dicing → PIC/EIC assembly (optional)

↓

Die attach (Chip/board or package) → Electrical interconnect (wire bonding) → Optical interconnnect (pigtailing) → Module packaging & test

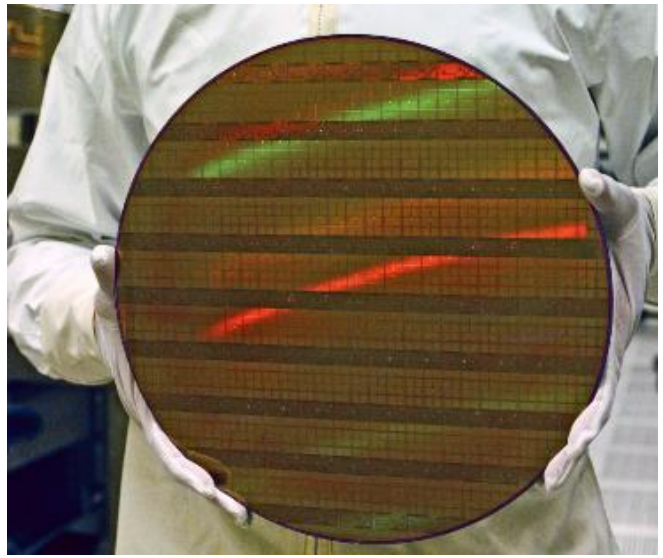


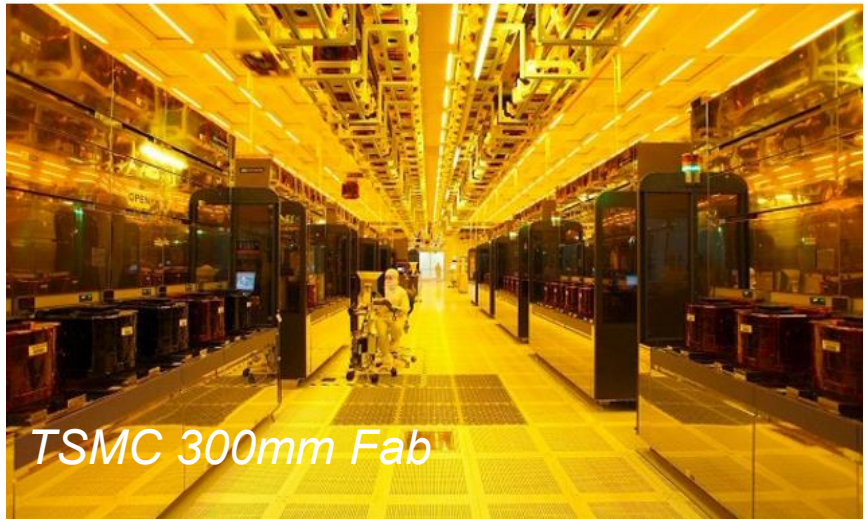




SILICON PHOTONICS : ADVANTAGES

- Small devices thanks to high index contrast between Silicon and oxide
- Integrated photonic device onto silicon, manufactured in a CMOS fab, enables low cost mass production
- Scalability to increase bit rate per channel : wavelength multiplexing, advanced modulation format
- Low-latency : architecture with unified switched photonic network
- High speed end-to-end network paths
- Wafer scale testing
- Solving electrical interconnect limits in Data centers, Supercomputers and ICs with higher capacity, lower cost optical interconnects



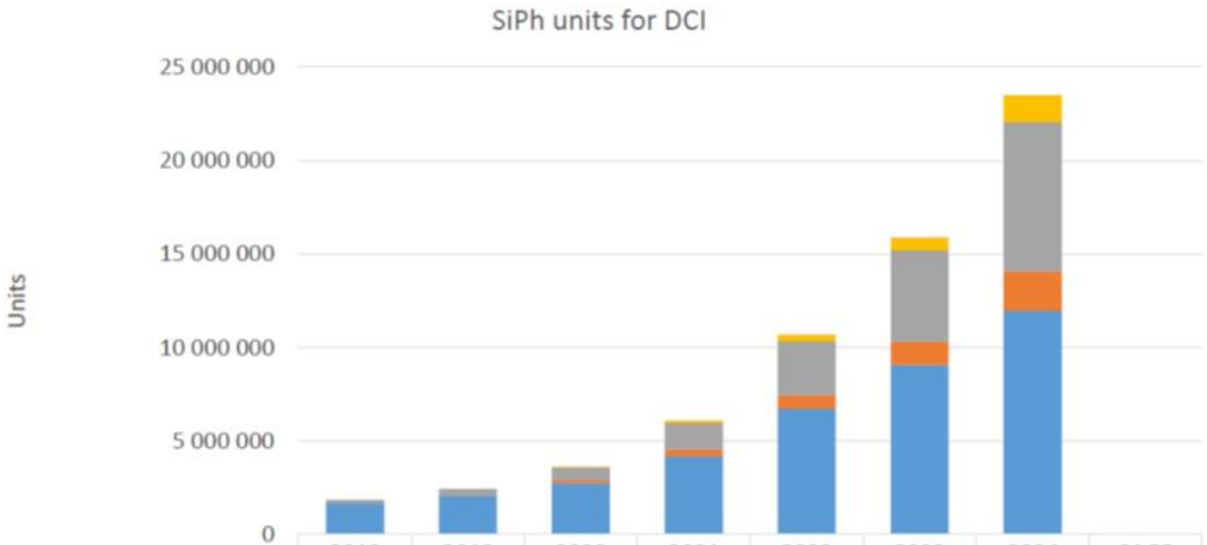


TSMC 300mm Fab

Google Data center

Intel Transceiver

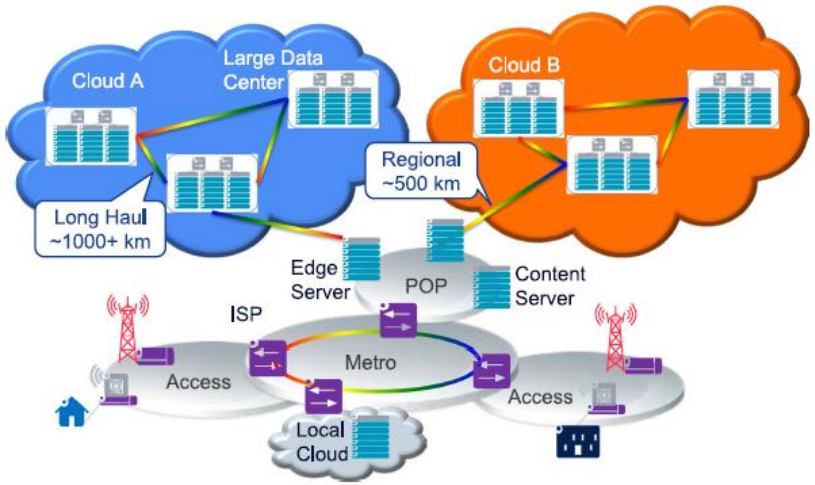
ROADMAP / MARKET TRENDS



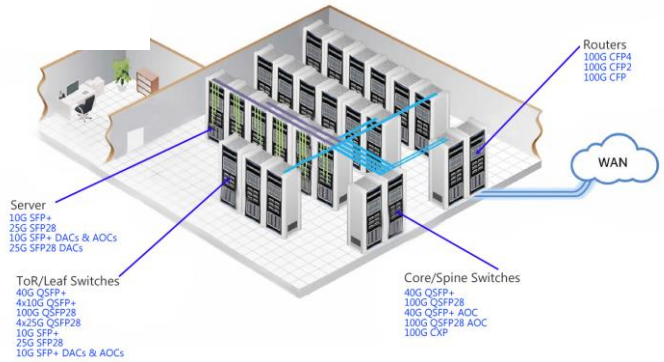
	2018	2019	2020	2021	2022	2023	2024	CAGR
200/400G units CWDM4	0	0	36 241	121 524	320 234	667 040	1 409 587	149,7%
100G units CWDM4	185 000	362 876	688 575	1 397 521	2 882 109	4 891 627	7 987 660	87,3%
200/400G units PSM4	0	0	144 963	364 571	747 213	1 238 789	2 114 380	95,4%
100G units PSM4	1 665 000	2 056 299	2 754 301	4 192 563	6 724 921	9 084 450	11 981 48	38,9%

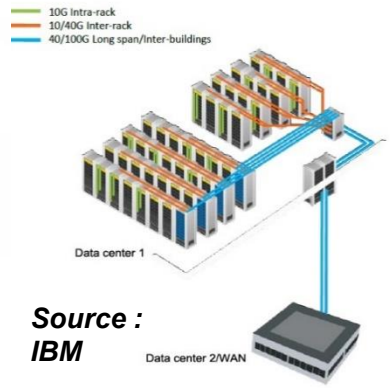
Source: Yole

- 400G is widepreading
- Increasing size of DCs
- <1$ / Gbps required
- Ethernet transceiver market Is expecting to reach 43Munits by 2025



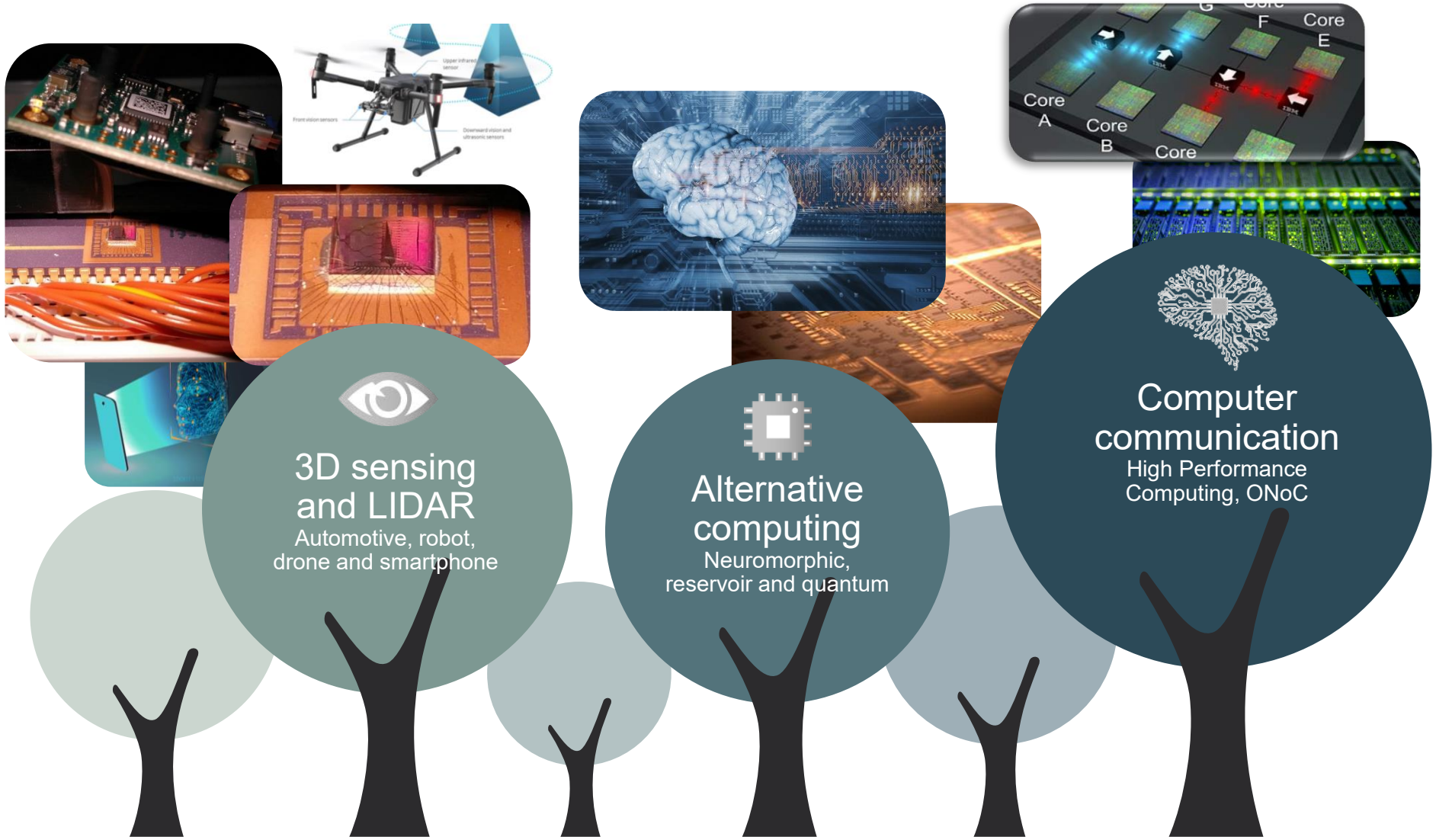
Source : ADVA



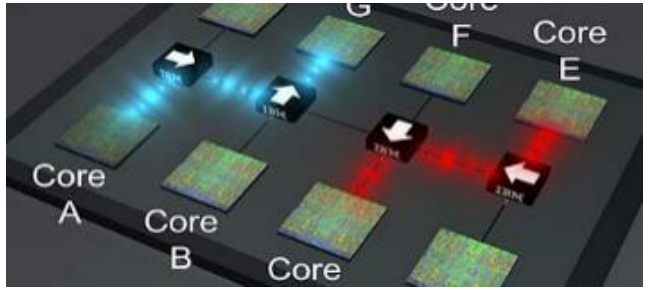


Source : IBM

APPLICATIONS BEYOND TELECOM & DATACOM



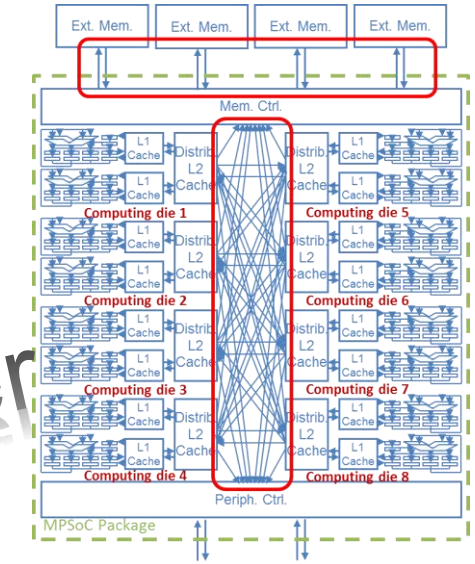
OPTICAL NETWORK ON CHIP

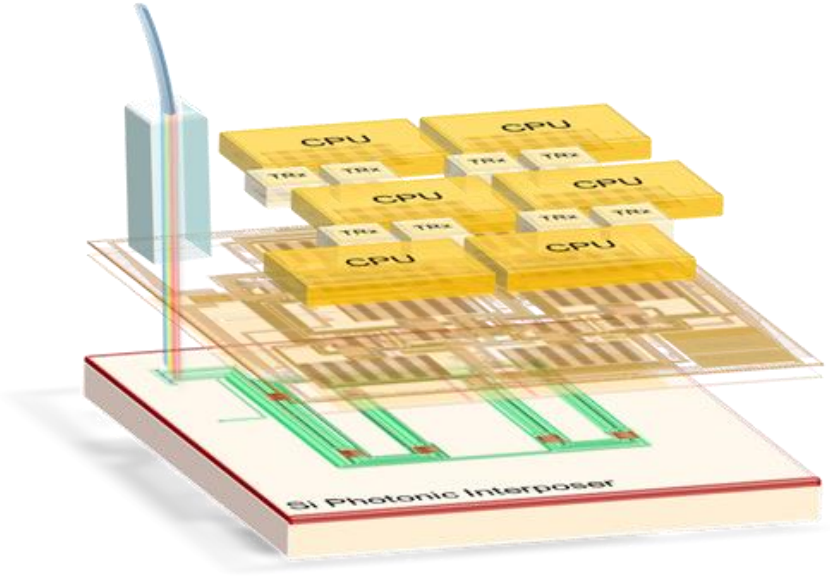


Photonic assisted processor

- **Multi-cores bottlenecks**

- **Chiplet approach**
- **Manycore architectures**
- **Known Good Die sorting**



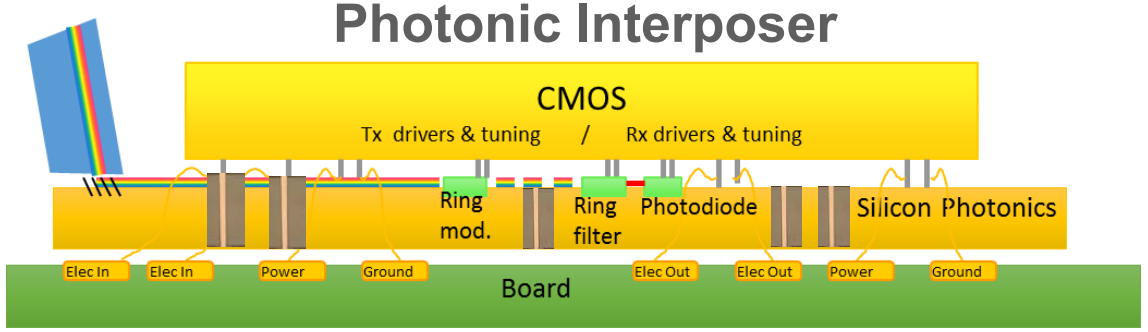


Photonic Interposer

with increasing maturity of silicon photonic platforms and compatibility with face-to-face die hybridization, it is now possible to consider the implementation **of optical network-on-chip (ONoC) topologies** on silicon photonic interposers to go beyond the scalability limitations of active CMOS interposers.

Y. Thonnart, ISSCC 2018

Photonic Interposer



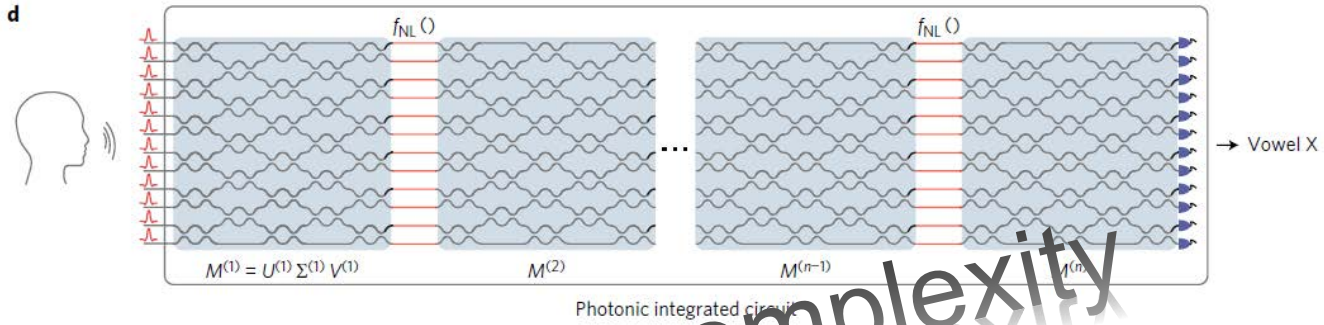
NEUROMORPHIC COMPUTING

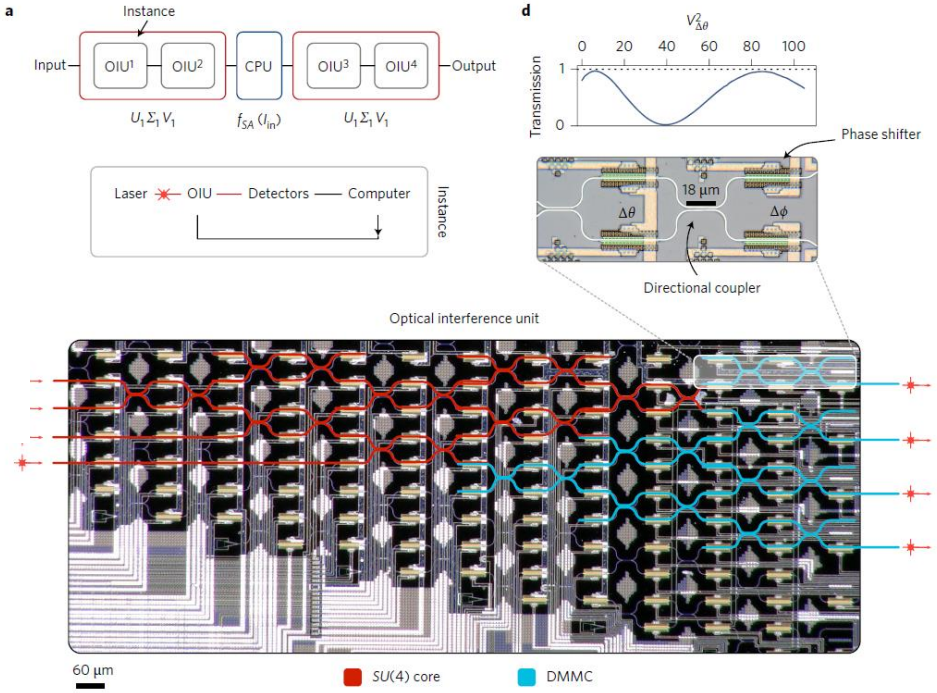
nature photonics
ARTICLES
PUBLISHED ONLINE: 12 JUNE 2017 | DOI: 10.1038/NPHOTON.2017.93

Massachusetts Institute of Technology

Deep learning with coherent nanophotonic circuits

Yichen Shen[1*†], Nicholas C. Harris[1*†], Scott Skirlo[1], Mihika Prabhu[1], Tom Baehr-Jones[2], Michael Hochberg[2], Xin Sun[3], Shijie Zhao[4], Hugo Larochelle[5], Dirk Englund[1] and Marin Soljačić[1]



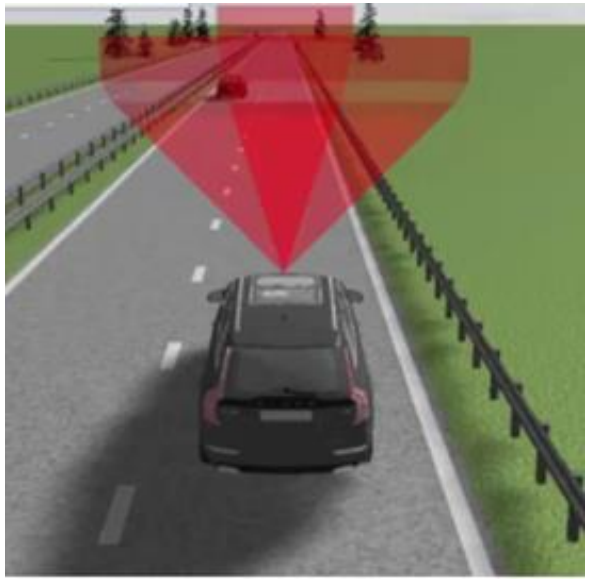


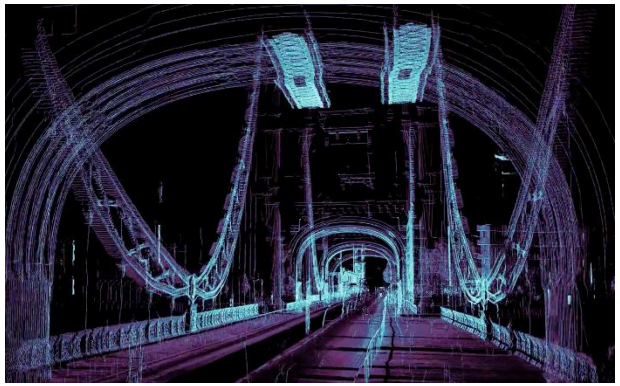
Optical interference unit

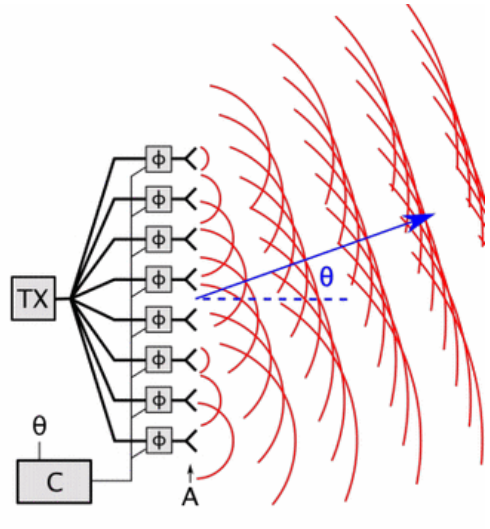
Increased complexity
=> Packaging challenges

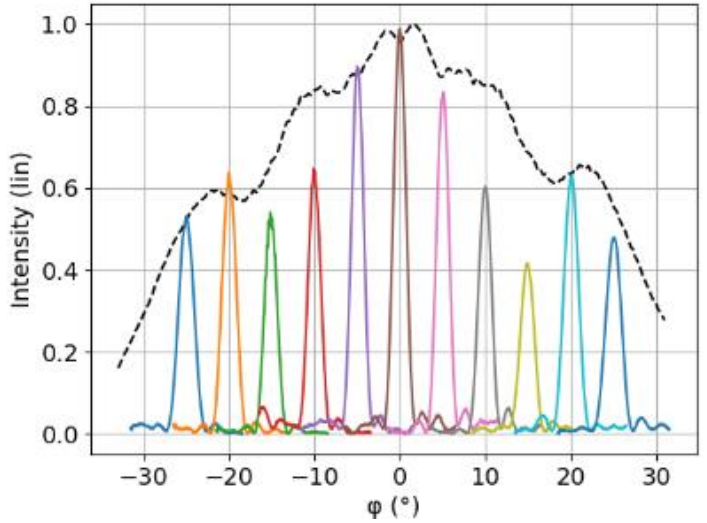
OPTICAL PHASED ARRAY LIDARS

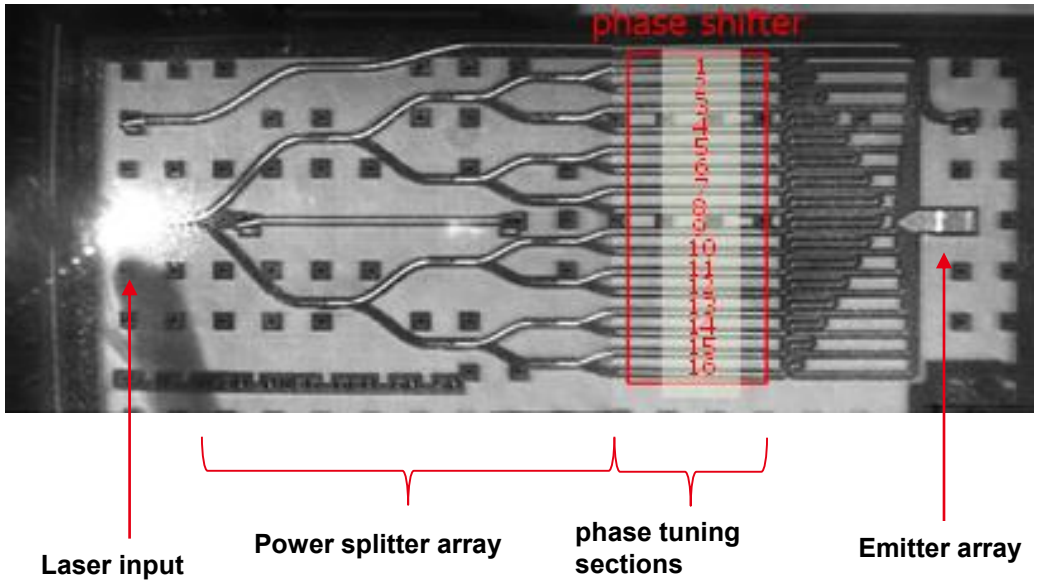
- Optical Beam steering for automotives









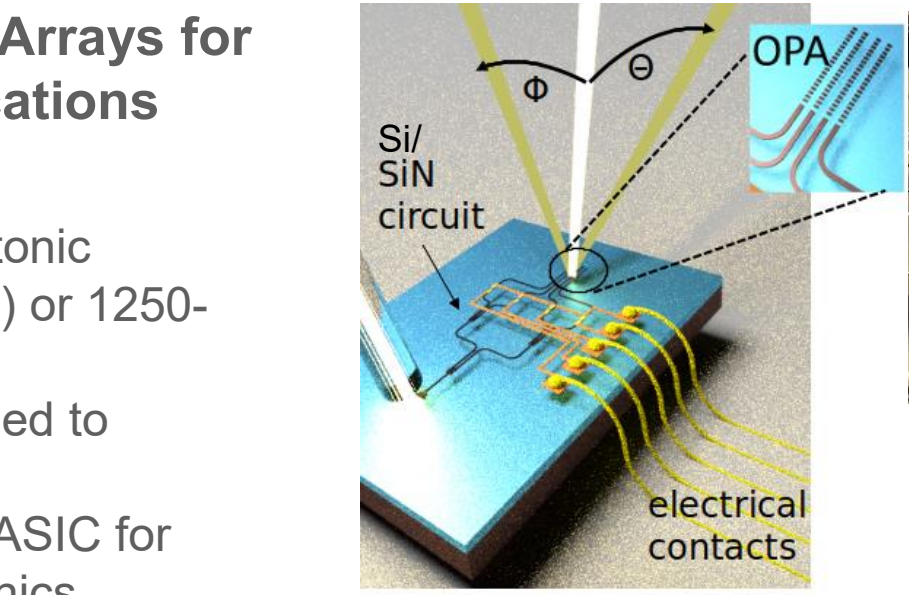


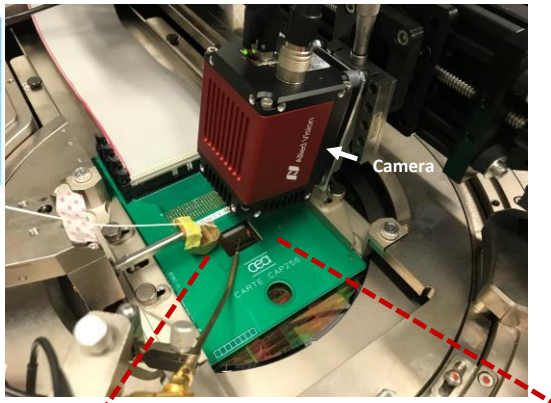
OPTICAL PHASED ARRAY LIDARS

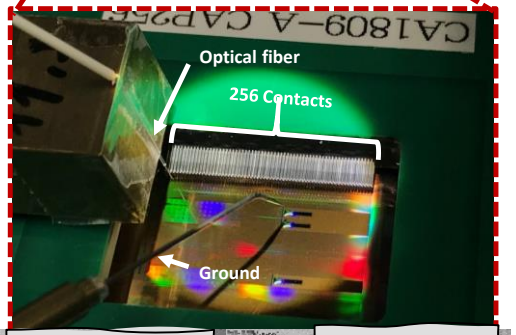
- **Development of Optical Phased Arrays for LIDAR systems and other applications**

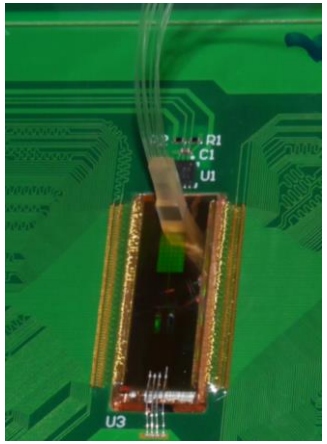
  - Application specific design of photonic components for 500-1000nm (SiN) or 1250-1600nm (Si or SiN).
  - Relies on thermo optic effect applied to waveguides
  - Co-design of photonic circuit and ASIC for hybrid integration of driver electronics.
  - Packaging of demonstrators

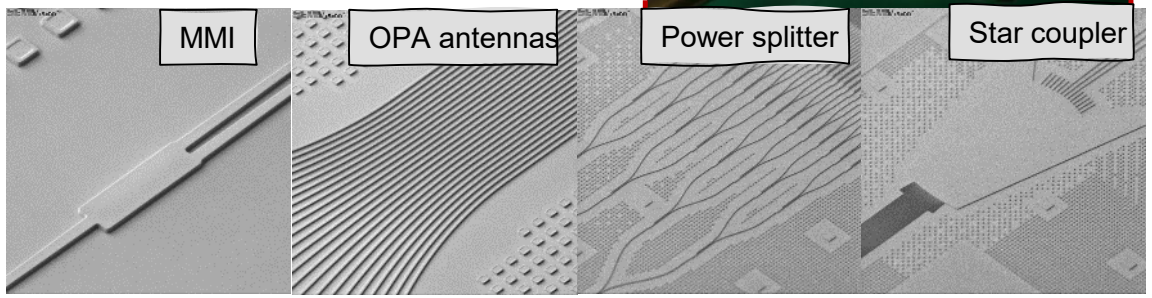
Packaging challenges





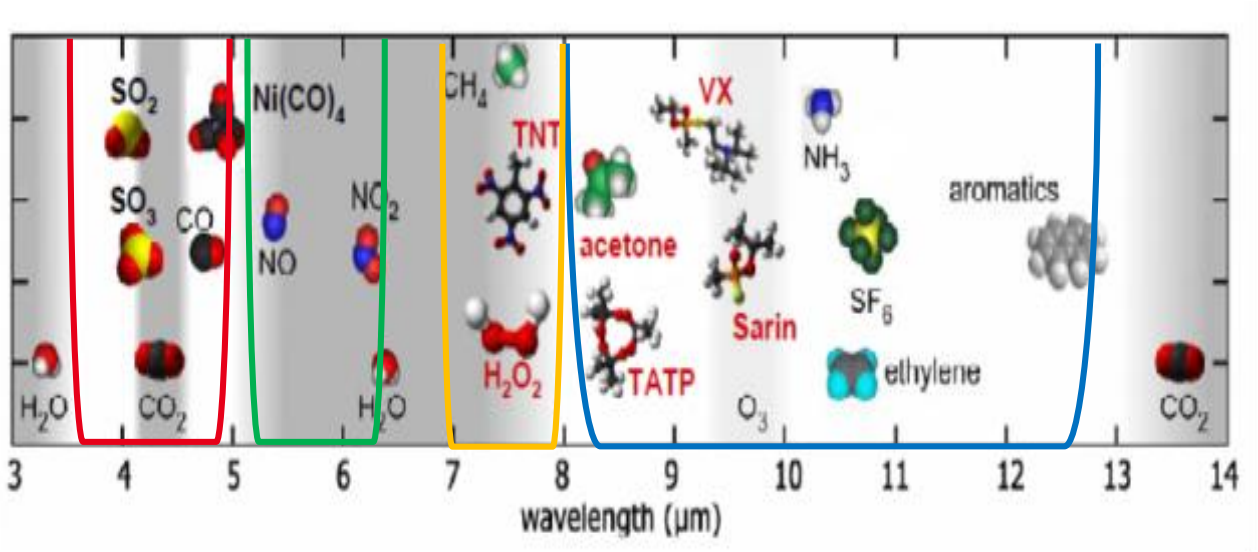


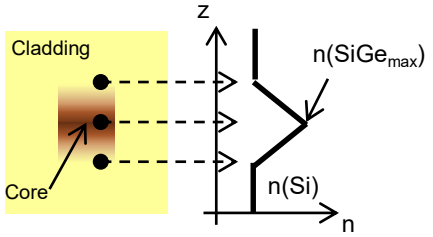


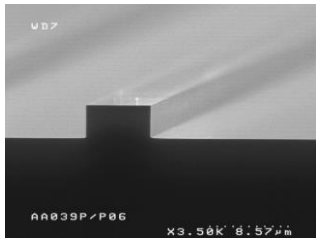


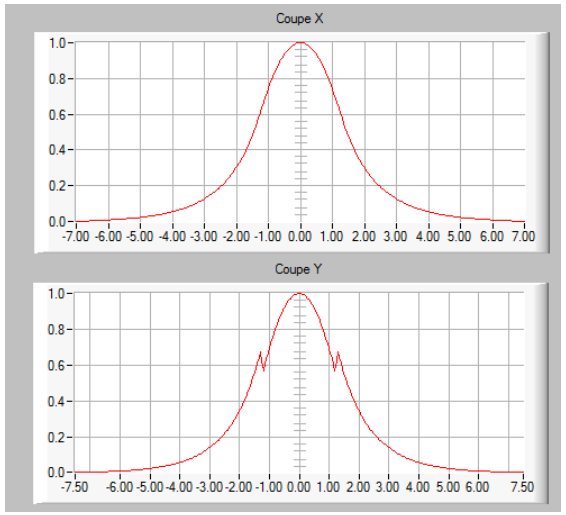
N. A. Tyler *et al.*, "SiN integrated optical phased arrays for two-dimensional beam steering at a single near-infrared wavelength," *Optics Express*, 2019
S. Guerber *et al.*, "Development, calibration and characterization of silicon photonics based optical phased arrays," *Smart Photonic and Optoelectronic Integrated Circuits XXIII* 2021.

GAS SENSORS

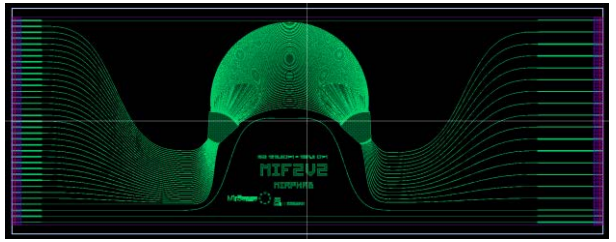


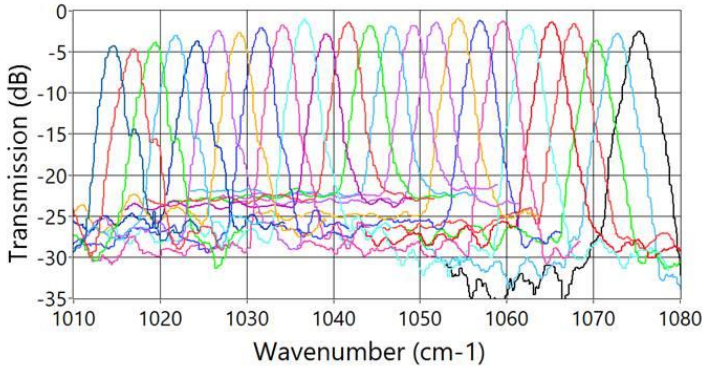






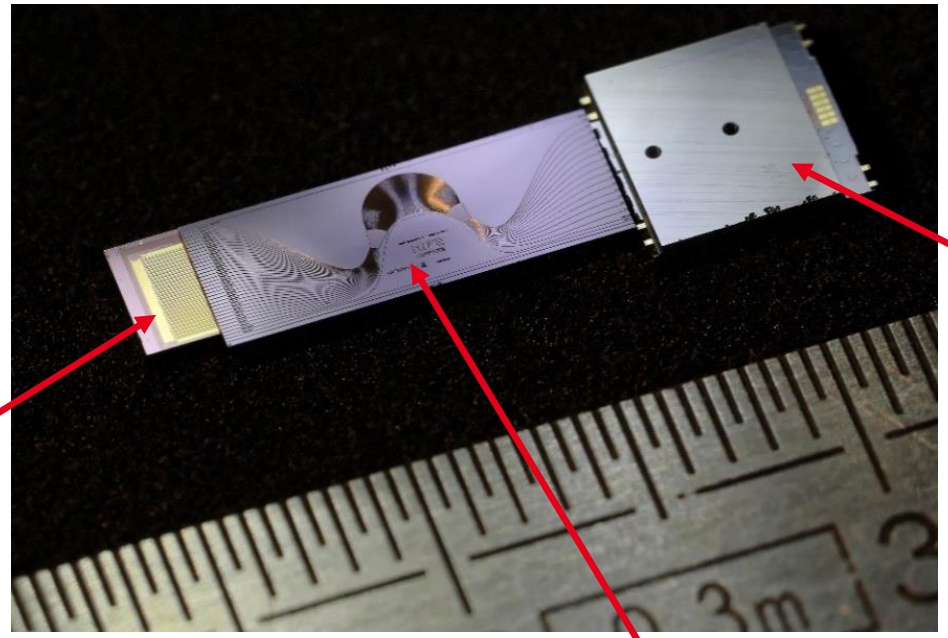
- **Single Mode waveguide:**
  - Core: Ge (section: 2.5 x 2.5 µm^2)
  - Cladding: SiGe
- **Characteristics FEM simulations:**
  - TM mode @ 8.7 µm
  - Mode size at (1% of max intensity) = 5.4 µm horizontal, 5.6 µm vertical
  - Minimum cladding of 6 µm SiGe around the Ge core





GAS SENSORS

Challenge: Combine source optics and detection on the same chip



Array Quantum Cascade Lasers on Si

Multigas detection enabler

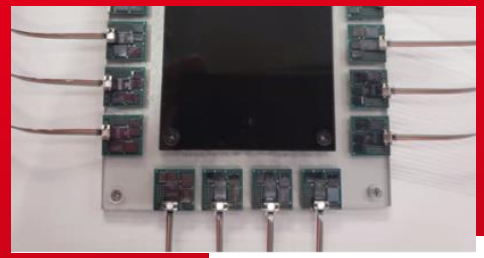
Photonics Integrated Circuit Beam Combiner

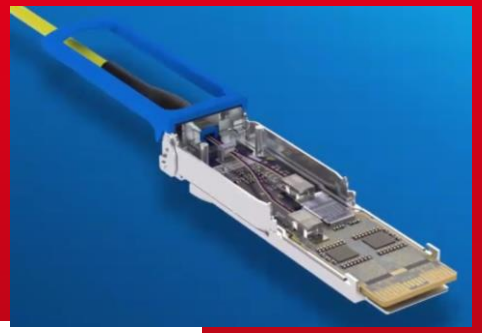
Replace costly and fragile discrete optics

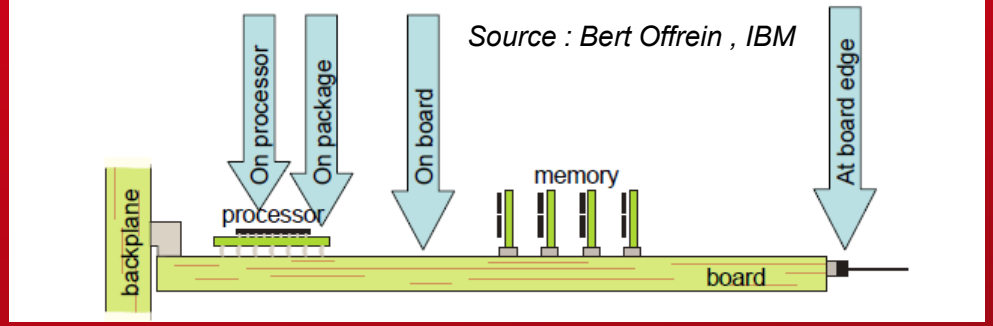
µ-PA: gas sensing cell with MEMS µPhone

Replace bulky multipass cells

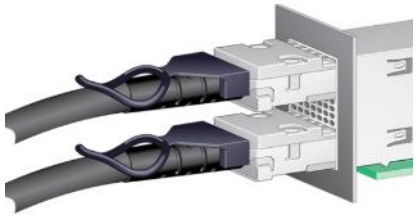
INTEGRATION CHALLENGES

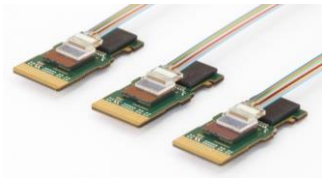


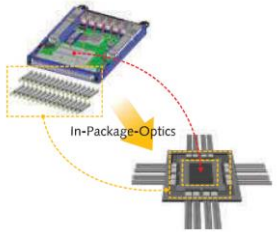


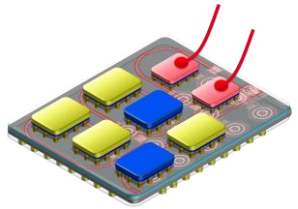


ROADMAP : FROM RACK INTERCONNECTS TO NETWORK ON CHIPS

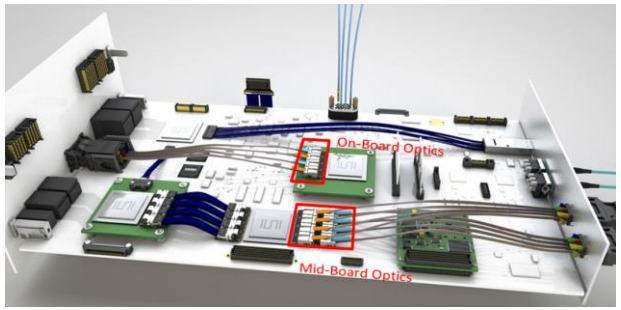


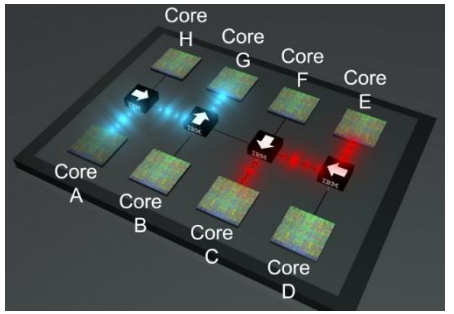






Intra and Inter Datacenter	Datacenter / HPC	Datacenter / HPC	HPC
Front Panel modules (100 to 400Gbps)	On-Board Modules	Host chip with dense optical I/Os (FPGAs, Switches)	Photonic Interposer



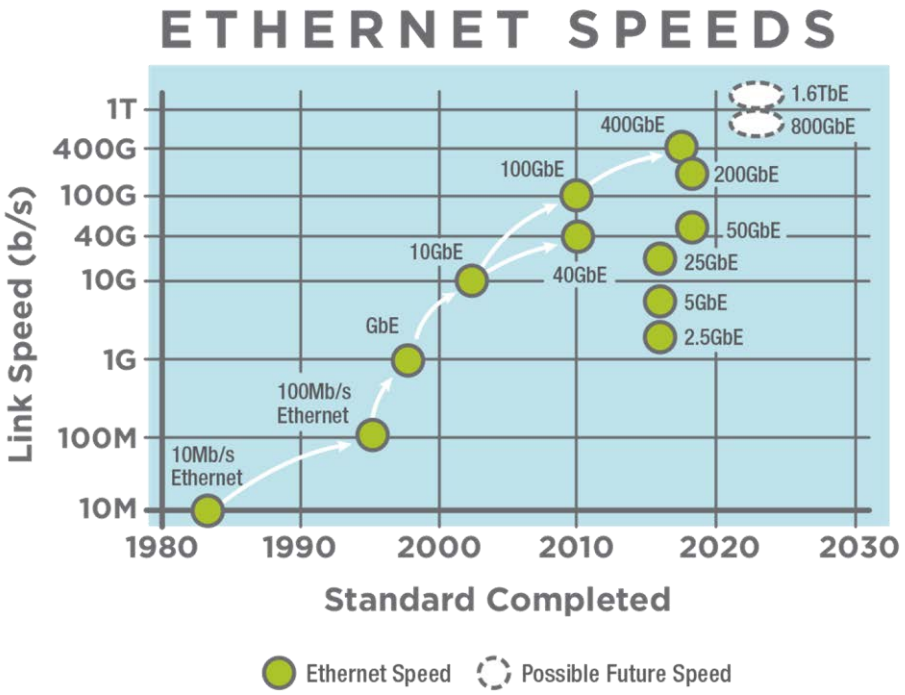


Review

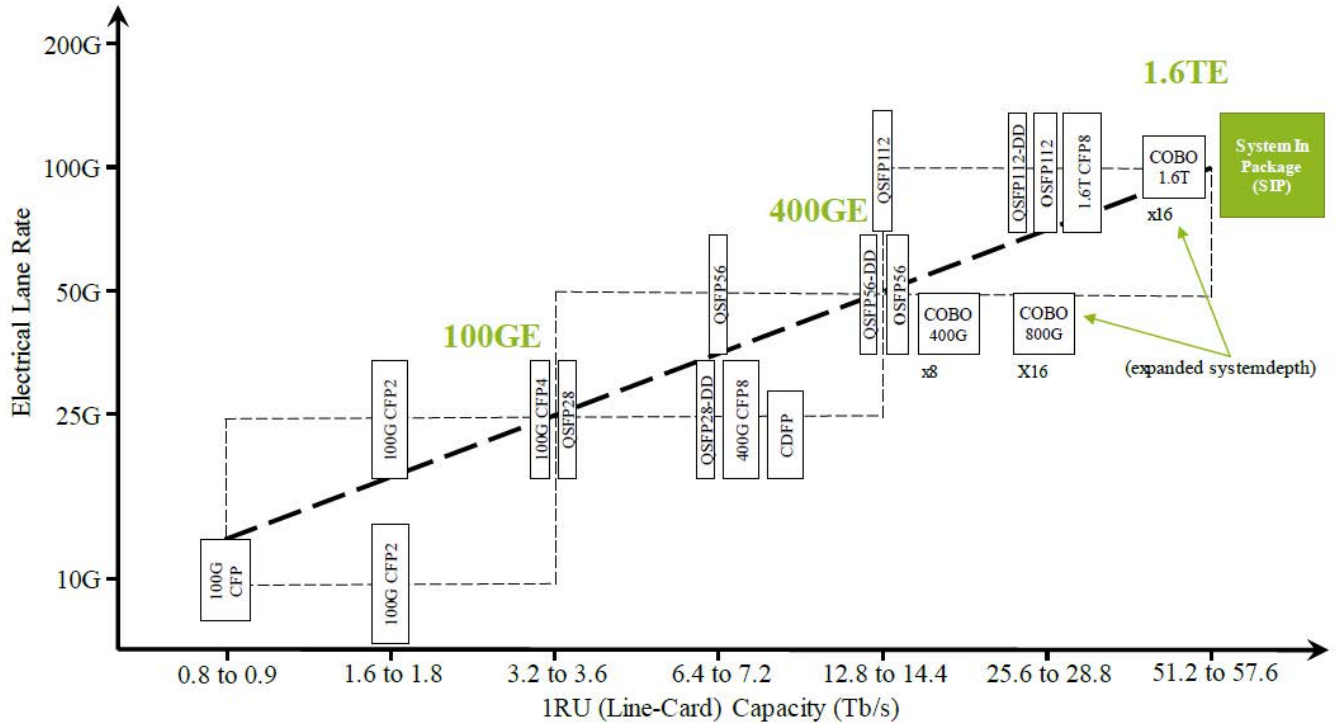
Silicon photonics for terabit/s communication in data centers and exascale computers

S. Bernabé [a], Q. Wilmart [a], K. Hasharoni [b], K. Hassan [a,e], Y. Thonnart [a], P. Tissier [d], Y. Désières [a], S. Olivier [a], T. Tekin [c], B. Szelag [a]

[a] Univ. Grenoble Alpes, CEA LETI, Minatec Campus, F38054 Grenoble, France
[b] DustPhotonics, 11 Tzela Hahar, Modiin, Israel
[c] Fraunhofer IZM, Gustav-Meyer-Allee 25, 13355 Berlin, Germany
[d] ST Microelectronics, Crolles, France
[e] III-V Lab, Joint Lab of Nokia, Thales & CEA, 1 A. Fresnel, 91767 Palaiseau, France



- 100G proliferating
- 400G ramping up

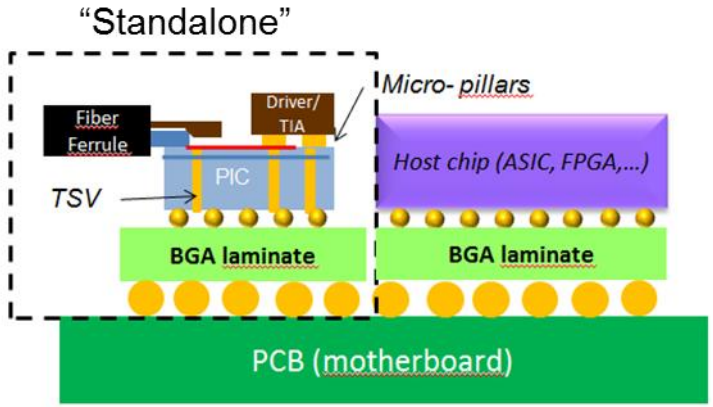


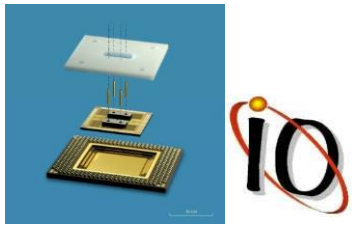
- Next stop, 800G and 1.6T
- Road >400G includes COBO and co-packaging

Courtesy of B. Sirbu, T. Tekin, Fraunhofer IZM

ON-BOARD

- Enable 2D use of the board
  (no more front panel limitation)
- >100Gpbs data rate
- Can be used for intra-rack or intra-board applications
- Optical modules integrated on PCB or on BGA package, near the host chip (processors or FPGA)
- RF lines are shorter and the whole motherboard surface can be used to provide host chips with E/O transceivers
- Already available with VCSEL embedded (e.g. Avago, TE…)
- **COBO** Initiative defining the RF interface





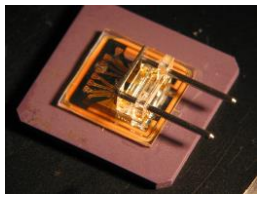
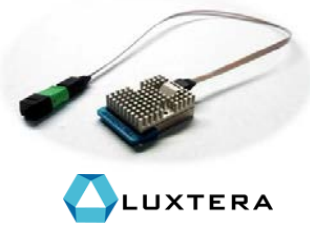
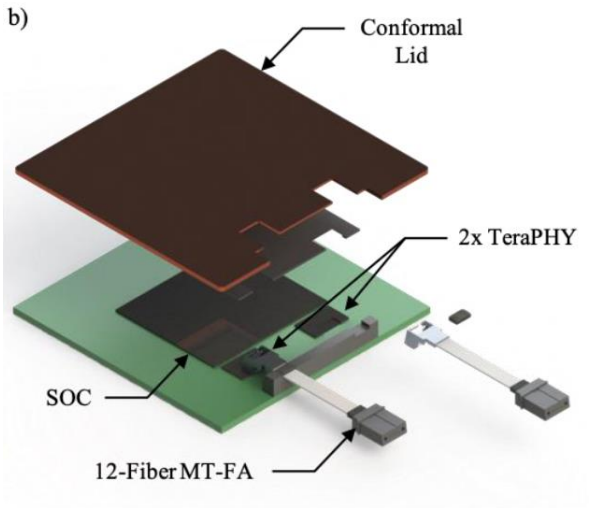



Figure 4. Mid-board optics modules shown here provide the key to a high-density interface.

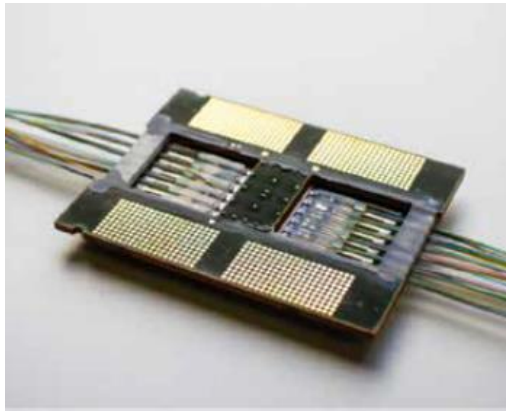
Tyco, 2012



NEXT STEP : SYSTEM IN PACKAGE REQUIREMENTS



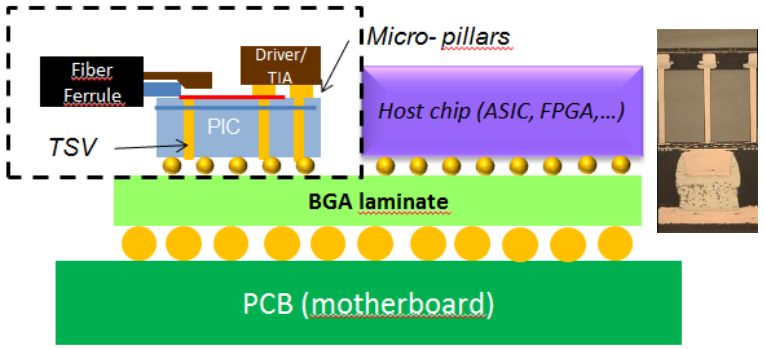
Ayar Labs' TeraPHY



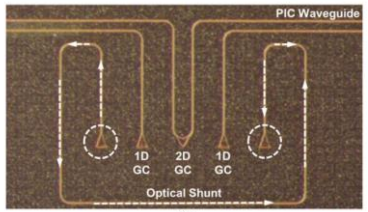
Rockley Photonics' OptoASIC

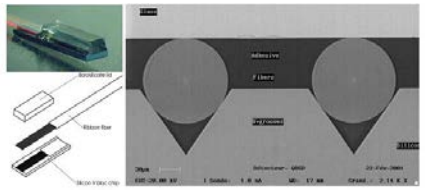
- To provide 25 Tbps switches (and 50 Tbps) with Photonic Transceiver
- Low footprint, high density modulators needed
- TSV may improve integration
- Reflow compatible connectors needed
- Laser integration management
- Many new module architectures from Start ups & RTOs

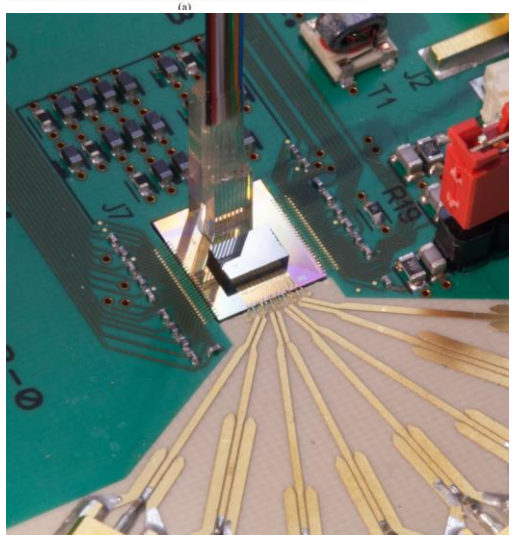
"System-in-package"

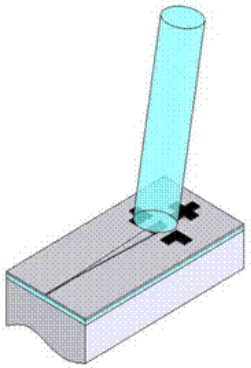


FIBER COUPLING









- Active alignment
- Not pluggable
- Not broadband

O. Castany, ESTC 2016 ;
Jun Su Lee, IEEE JSTQE 22,6, 2016

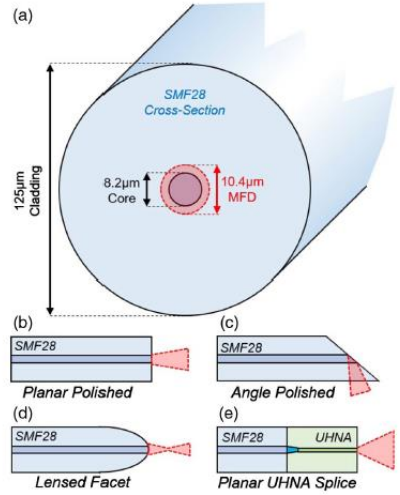


Fig. 2. (a) Cross-section schematic of an SMF28 fiber, showing the 8.2 μm fiber core centered in the cladding layer, wave-guiding the 10.4 μm MFD 1.55 μm mode. Side view schematics of (b) planar polished, (c) angle polished, and (d) lensed SMF28. (e) Schematic of UHNA-to-SMF28 splicing, showing the thermally expanded adiabatic taper. The (b), (d), and (e) geometries are commonly used for edge coupling, while the (c) geometry is preferred for grating coupling.

Passive alignment
Easy to package
Broadband
Small Form Factor

WANTED !

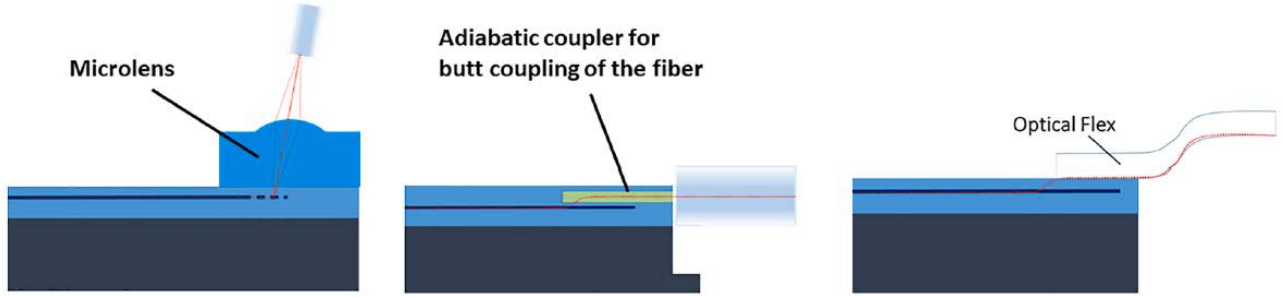
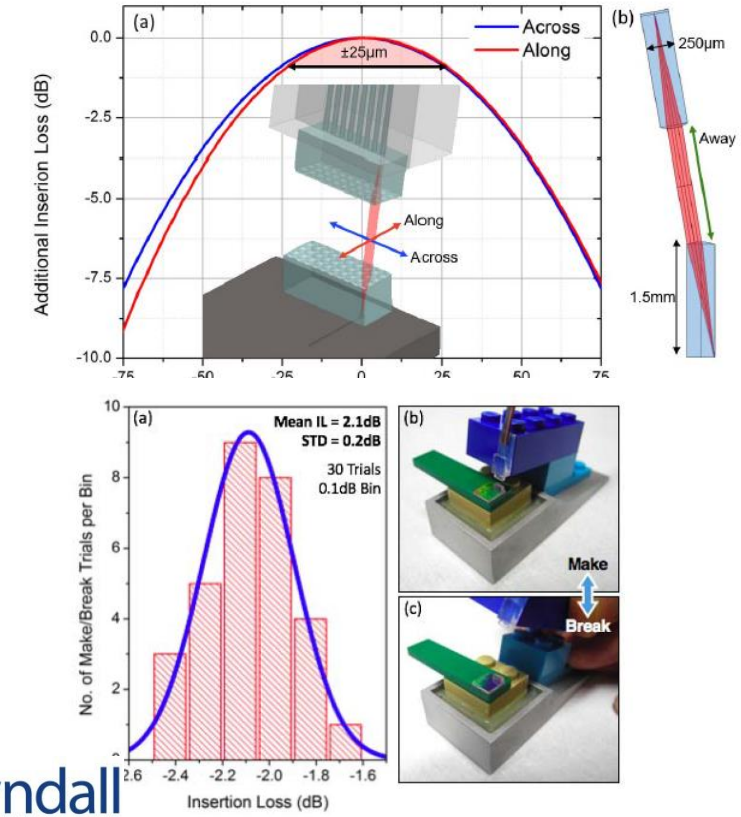


Fig. 22. Alternative techniques for fiber attach to PIC.

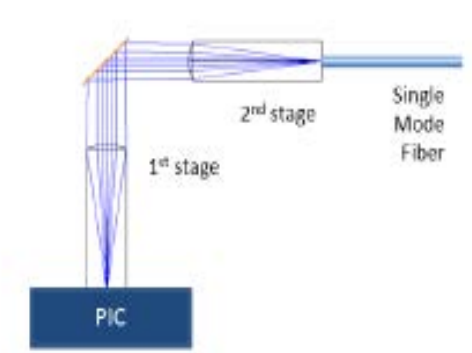
FIBER CONNECTION

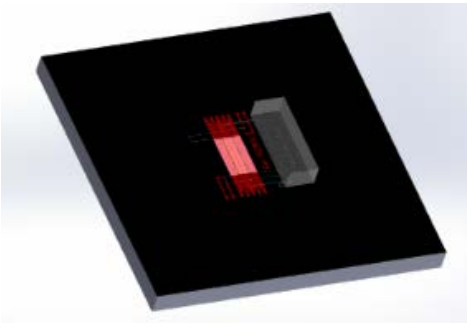
Microlens coupling

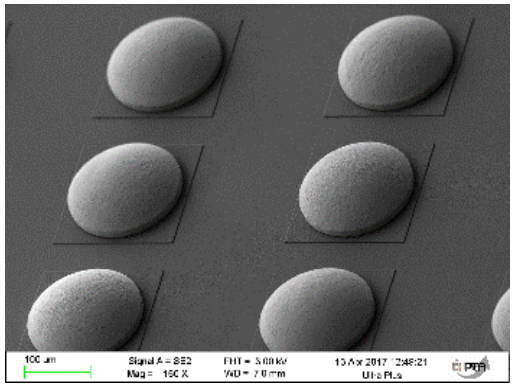
- Relaxed lateral tolerance
- Two stage optical train
- Enable pigtail free module

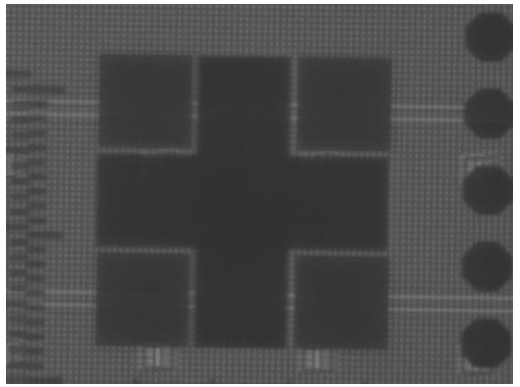


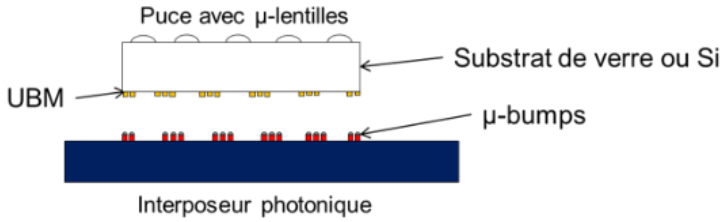
Scarcella et al., IEEE PTL 29, 22 , 2017











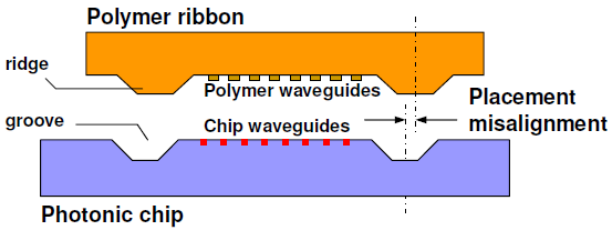
0,5 µm misalignment demonstrated

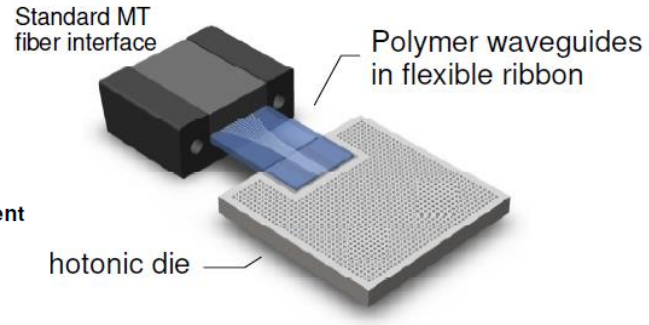
D. Zonou et al. , ECTC 2017

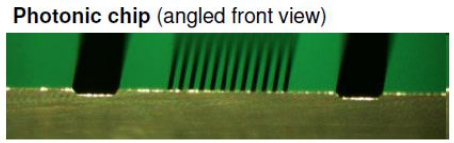
FIBER CONNECTION

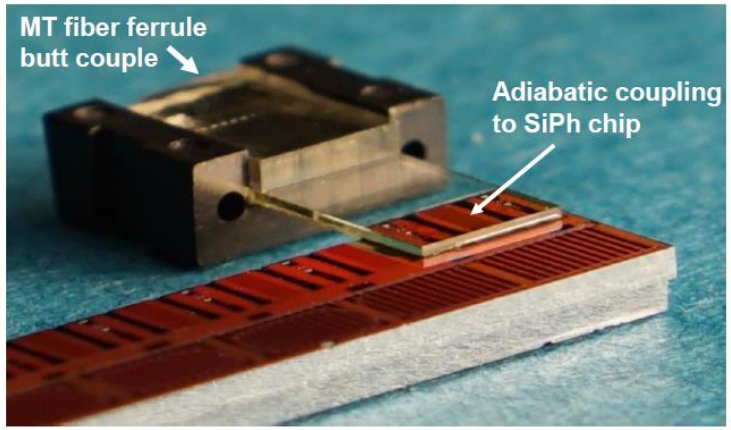
Evanescent coupling approach (IBM)

- Evanescent coupling between PIC and polymer waveguide
- Passive alignment









P. Fortier et al., C2Mi workshop, 2015

Evanescent coupling to SiN-on-Si waveguide layer (ST / Teem Photonics):

- **Broadband and single-mode** in O-band and C-band
- **Low loss** (< 1.5 dB from fiber to SiN)
- **Low PDL** (< 0.2 dB)
- **Alignment tolerant**

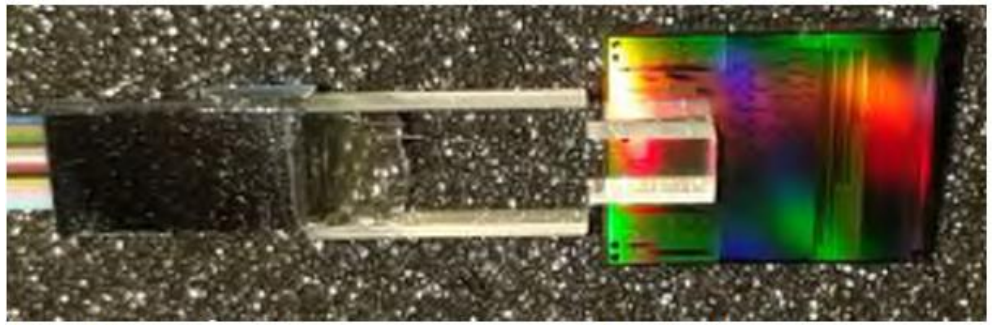
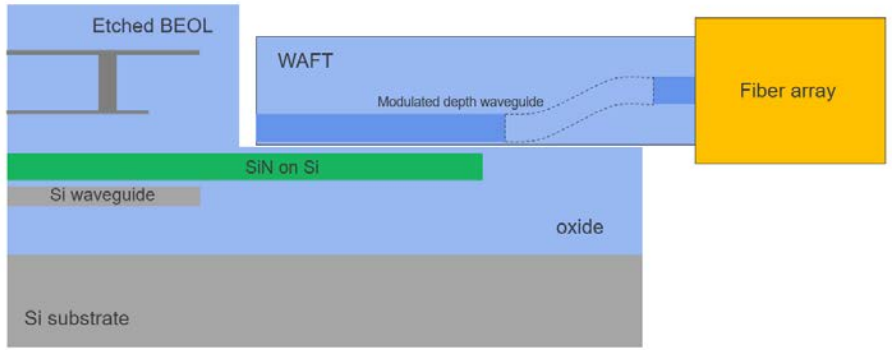
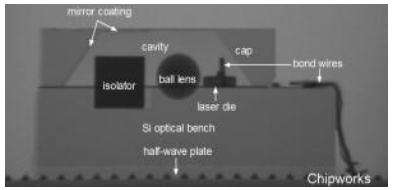


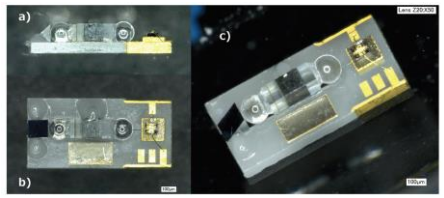
Fig 15 Glass interposer assembled Silicon Photonics Device with Cavity Etched BEOL



From Binda et al, EMPC 2019

LASER INTEGRATION STRATEGIES





De Dobbelaere, OFC 2014

Micropackaging

Luxtera, Tyndall

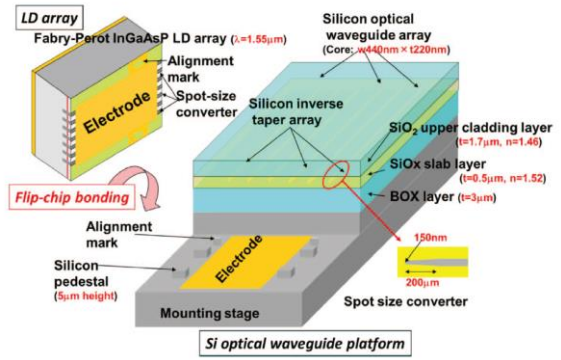
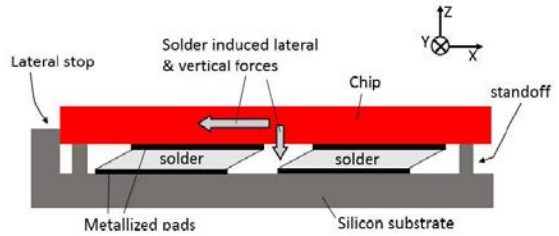


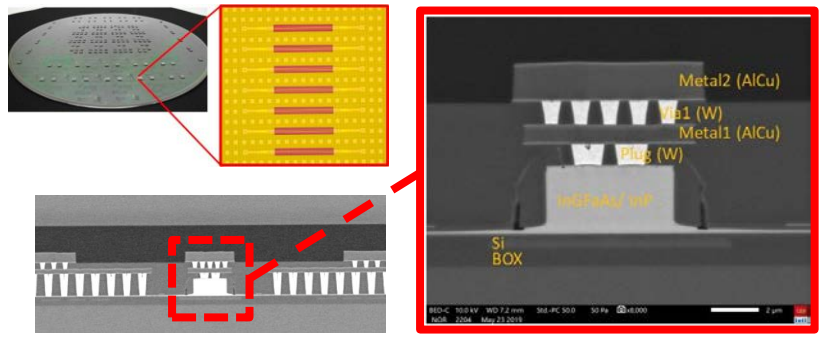
Fig. 1 Schematic of hybrid integrated light source with LD array on silicon platform made using SSC with SiO_x slab layer.

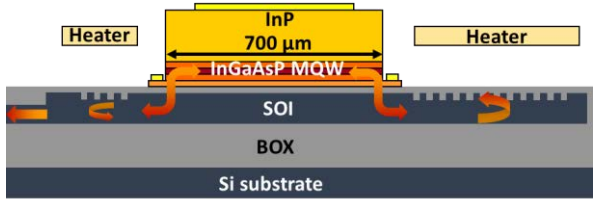
Shimizu et al., Trans. Jap. Inst. Of Elec. Pkg., 2014

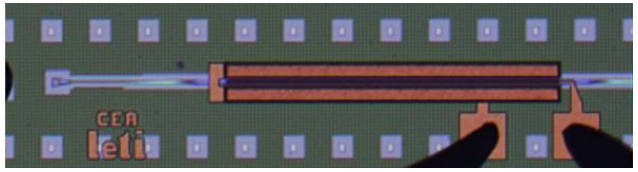


Self aligned flip-chip (Hybrid)

Petra, IBM, IZM







B. Szelag, IEDM 2017

Direct bonding

Intel, UCSB, LETI

THERMAL CONSTRAINS

- Photonic devices are temperature sensitive
- In co-packaging approach, proximity to the host chip could be a problem

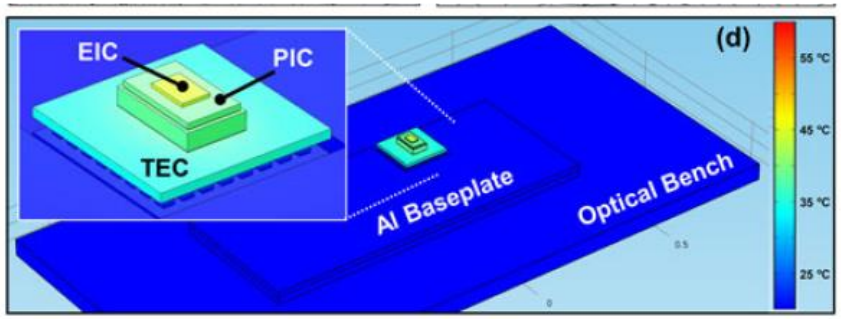
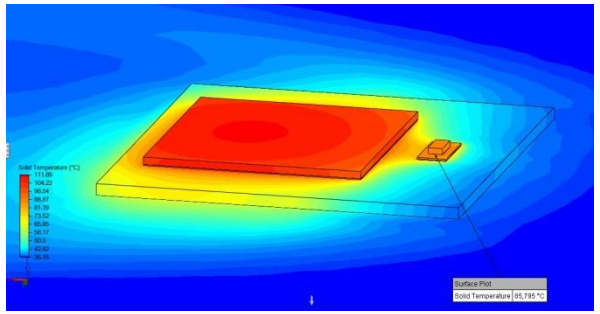
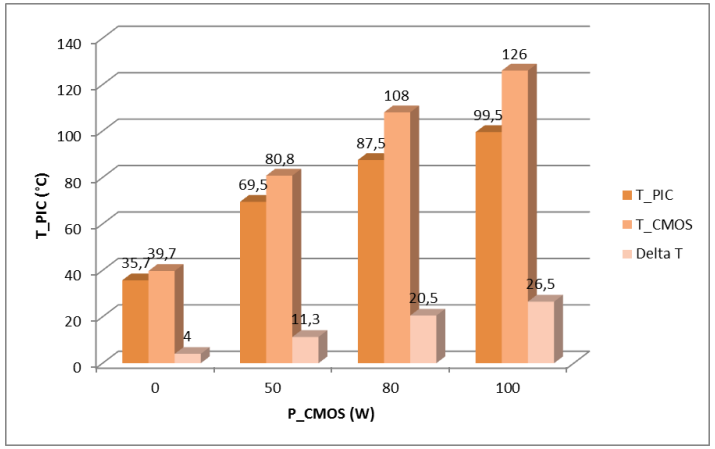
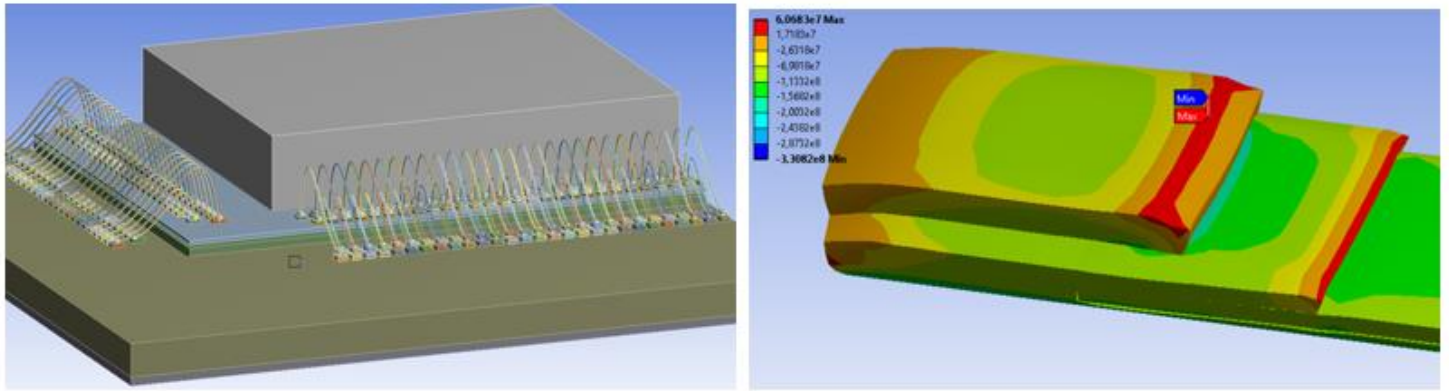


Fig. 8. (a)–(c) COMSOL model of the ONU, spanning the macroscopic dimensions of the TEC and Al baseplate to the microscopic dimensions of the CPB interconnects between the electronic-IC and PIC. (d) An example of the temperature map of the thermal stack and Al base-plate used to extract the temperature profiles in Fig. 9(a).

J. S. Lee et al., « Meeting the Electrical, Optical, and Thermal Design Challenges of Photonic-Packaging », *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 22 nº 6, p. 409-417, nov. 2016



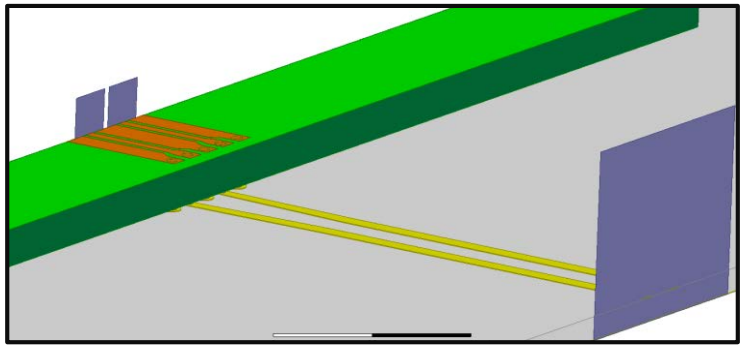


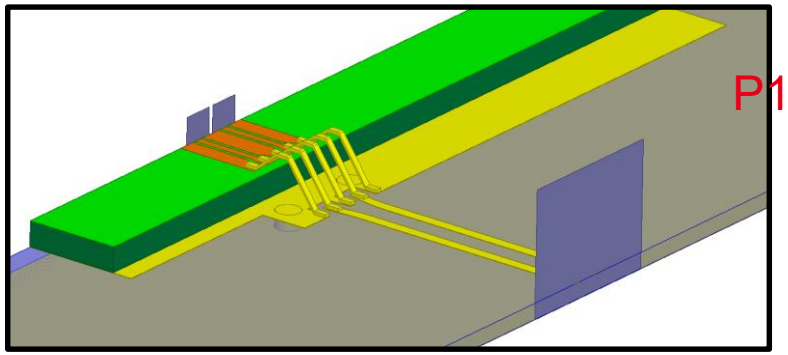


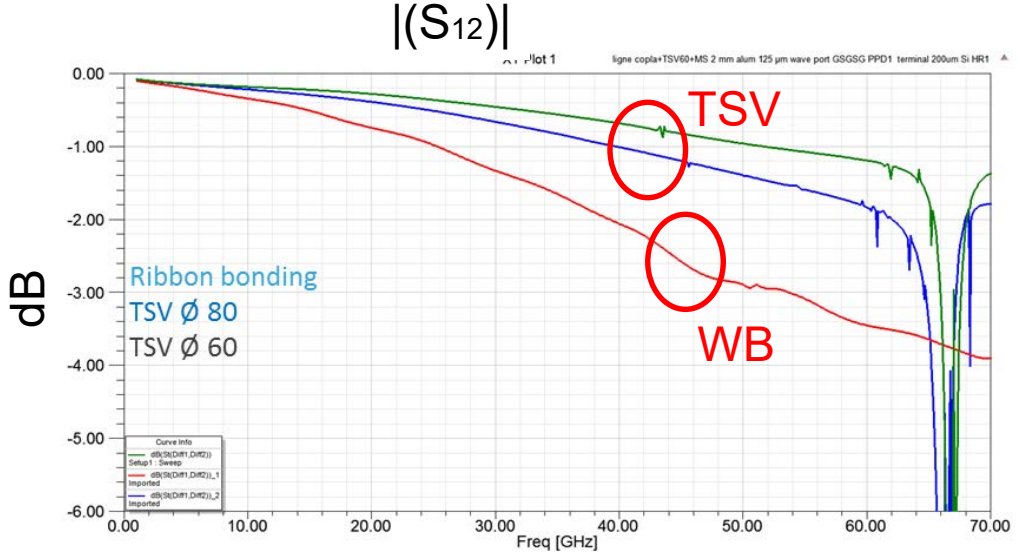
FEM thermo-mechanical simulation model of a wire-bond based PIC package module with the typical material deformation maps due to mechanical stress and/or heat within the package. Source: B. Sirbu / Fraunhofer IZM

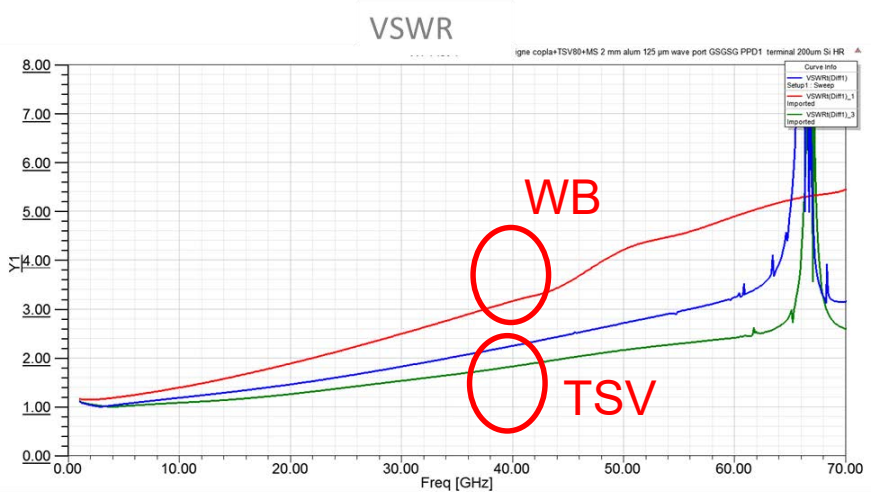
RATIONALE FOR TSV

- RF S-parameters









25 Gbits/s 50 Gbits/s 75 Gbits/s

L. Fourneaud, Internal report, CEA Leti

A STRATEGY FOR ELECTRONIC/PHOTONIC CONVERGENCE

THROUGH SOME EUROPEAN R&D INITIATIVES

PIXAPP
Photonic Packaging
Pilot Line

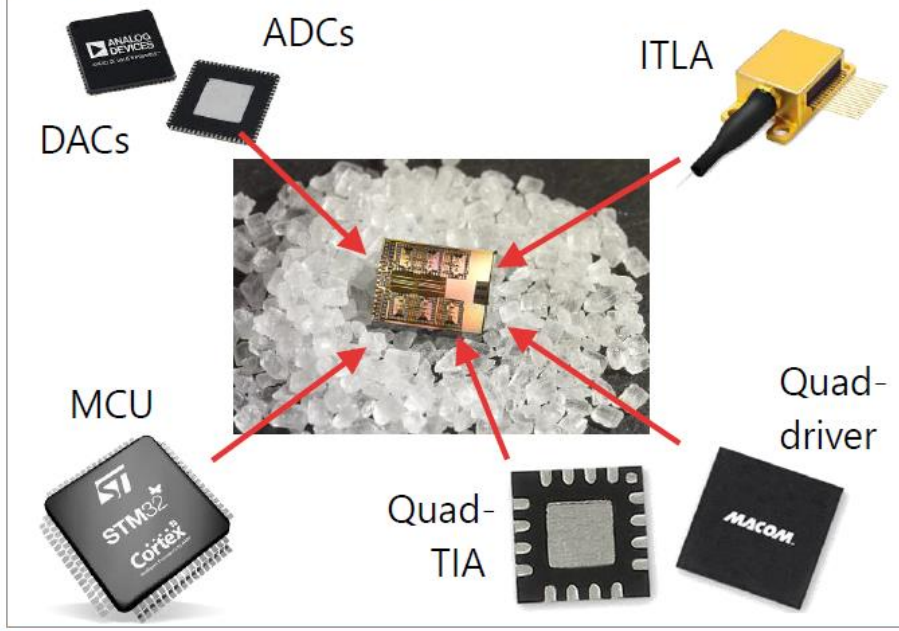
MASSTART

STEP1 : MASSIVE AUTOMATION

Cost

~80% of cost is in packaging

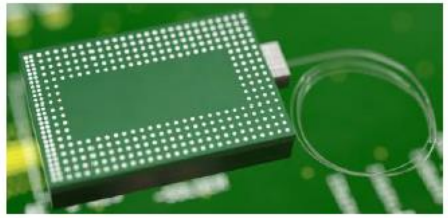
Higher level of integration



Automation & standards

- Single automated optical alignment step

- Leverage electronic IC infrastructure (e.g. flip-chip assembly)

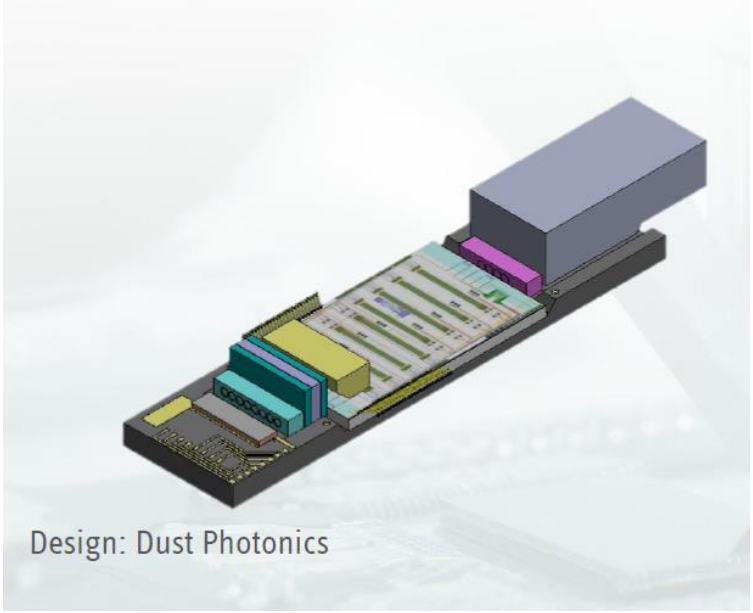


Integration, automation & volume

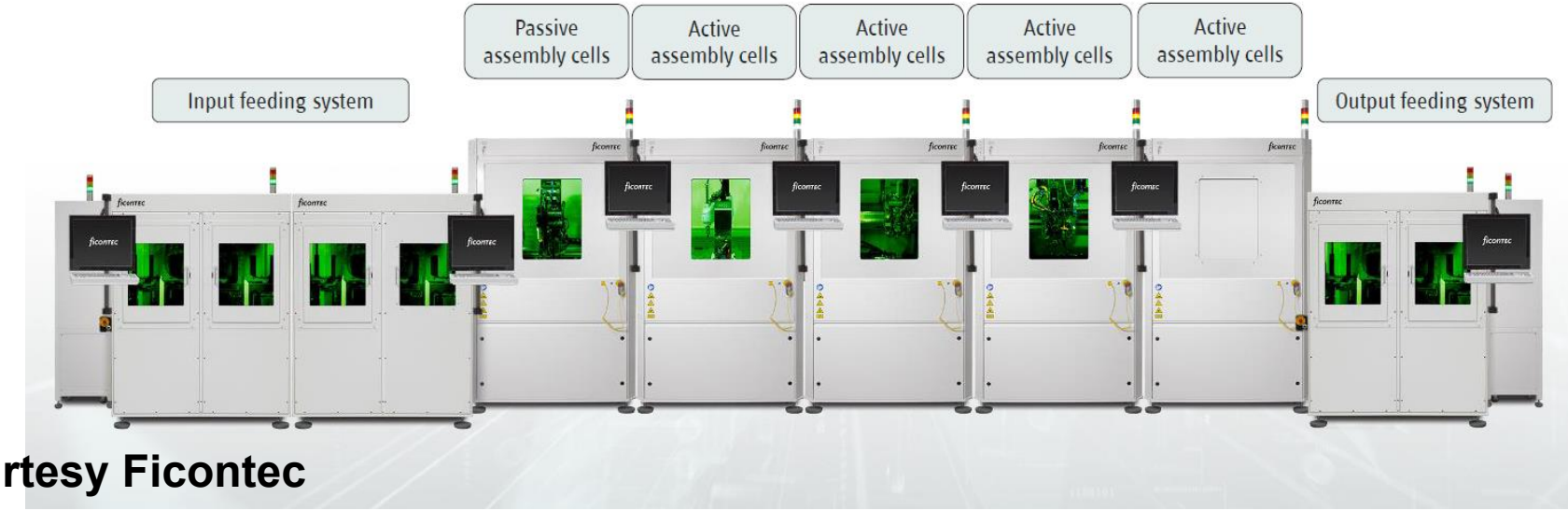
Courtesy of B. Wolfheil, ADVA

STEP1 : MASSIVE AUTOMATION

Active assembly machine Passive assembly machine

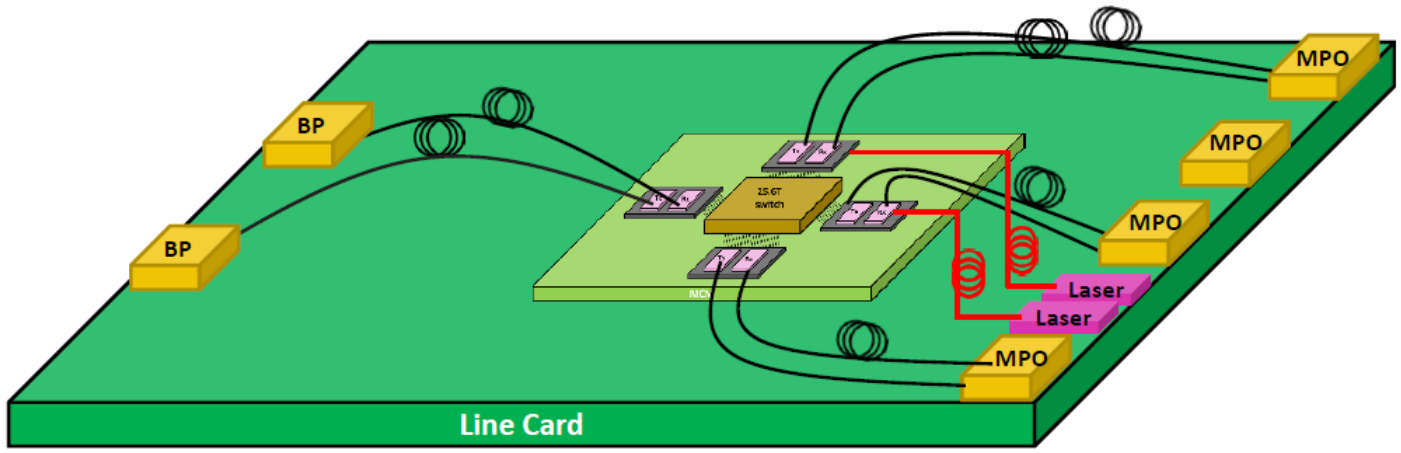


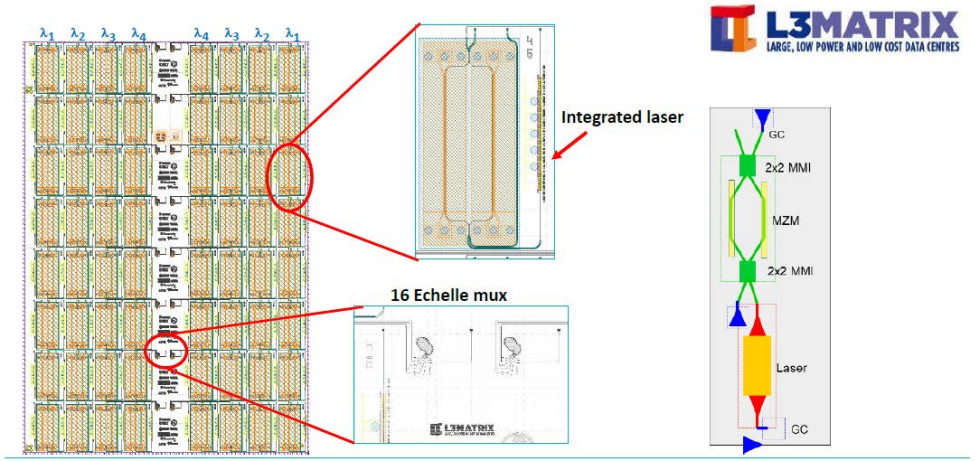
Design: Dust Photonics



Courtesy Ficontec

STEP2 : DENSE INTEGRATION / PASSIVE ASSEMBLY





- All fibers are routed to the passive front panel or backplane fiber connectors
- Module can be connected to the line card either using:
  - Socket – bad thermal connectivity, fibers may be glued in place during assembly
  - BGA – good thermal performance, fibers cannot go through reflow
- Air flow through the line card is improved due to the elimination of the pluggables on the front panel

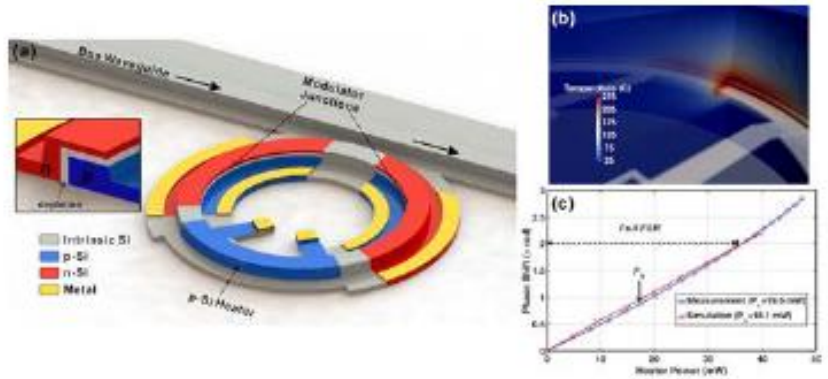


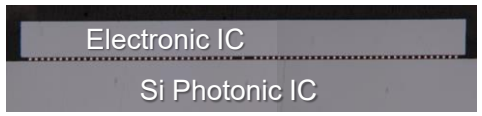
Figure 20: High speed microring with 45GHz BW, demonstrated by Intel [17].

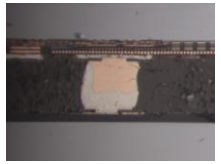
The Chiplet approach

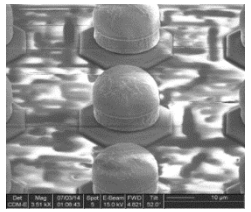
STEP2 : DENSE INTEGRATION / PASSIVE ASSEMBLY

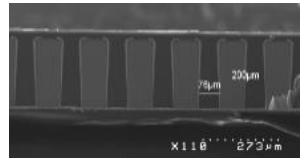
Wire bonding ***Flip Chip*** ***TSVs***

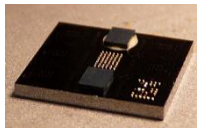
Integration/Co-integration level



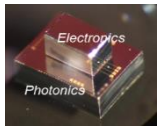








44 Bumps
(SBB)

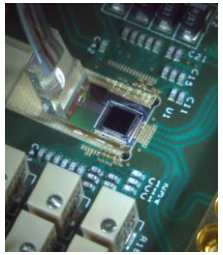


100 Bumps

144 bumps

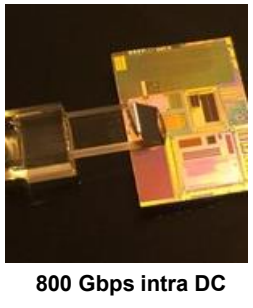
484 bumps

2091 bumps



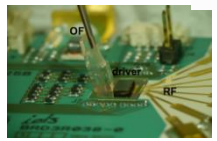
200 Gbps/ (50G NRZ, WDM-2)
4 fibers (2 Rx/2Tx)

Enabler for 400Gbps++

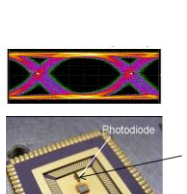


800 Gbps intra DC

200 Gbps Tx/Rx
MBOM



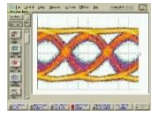
Module Rx 100 Gbps
Chip On Board



Module Rx 25Gbps
Wire bonding

Module Rx 25Gbps
Flip Chip

Module Rx 12,5Gbps
Wire bonding

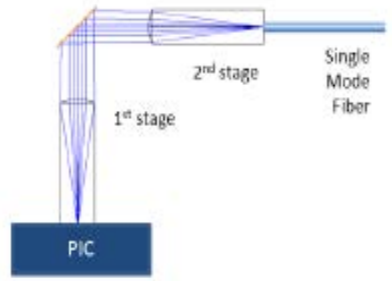


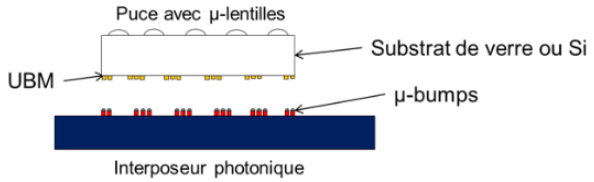
Module Rx 8Gbps
Wire bonding

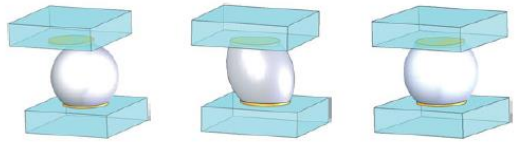
2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021

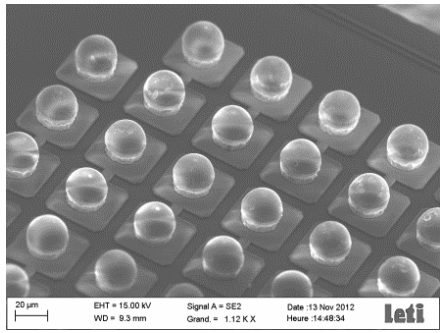
SELF ALIGNMENT OF MICROLENSES

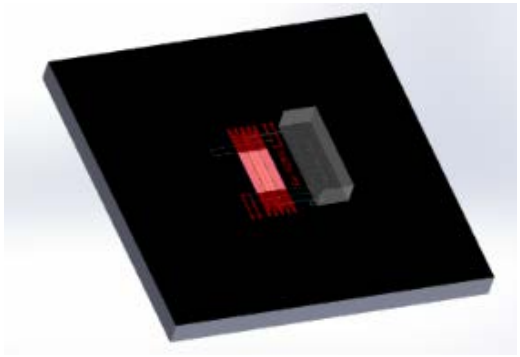
- Use of copper pillars to align first stage
- Through substrate IR observation of verniers
- <0,5 µm misalignment obtained
- Robust process (7µm offset is realigned)
- Compatible with High throughput bonding machine

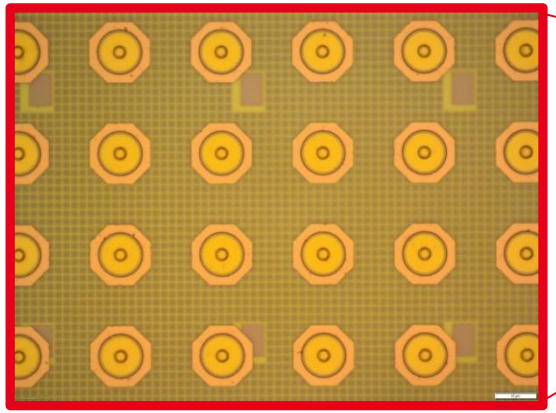


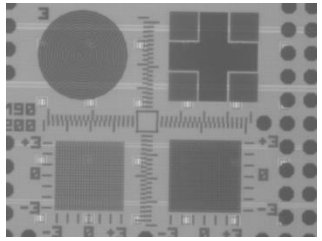


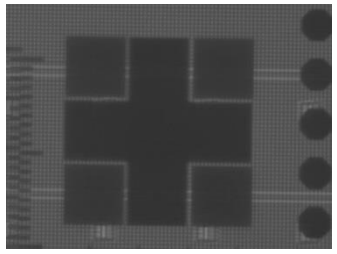










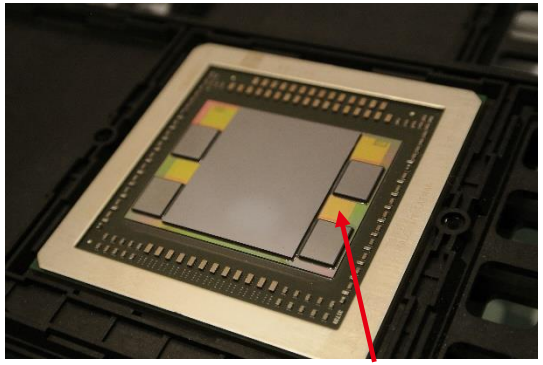


D. Zonou et al. , ECTC 2017

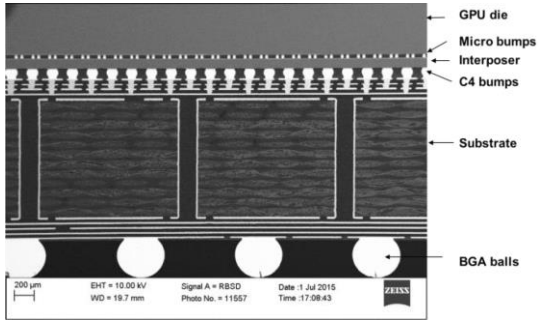
STEP 3 : THE ROAD TO PHOTONICS INTERPOSERS

Passive Interposer

Only electrical Routing



GPU AMD avec interposeur passif

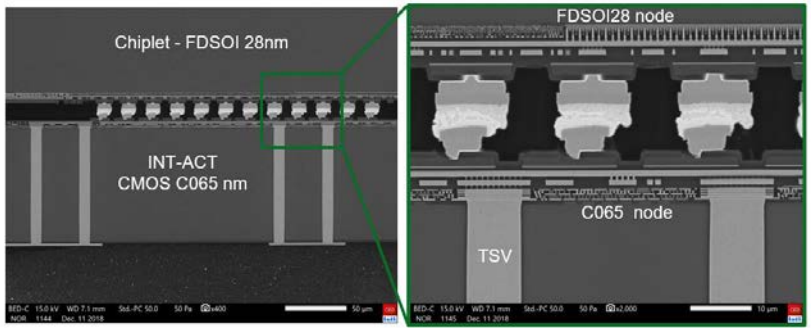


Interposeur passif AMD [1]

2016

Active Interposer

Electrical Routing
DC-DC conversion
Electrical Network On Chip

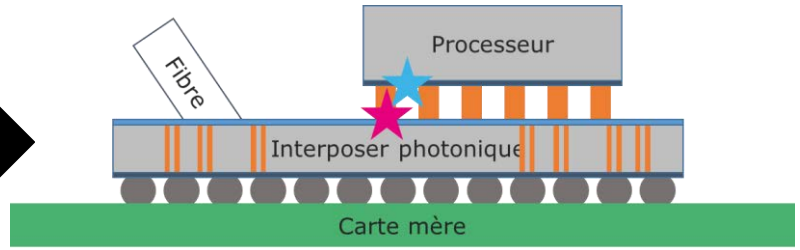


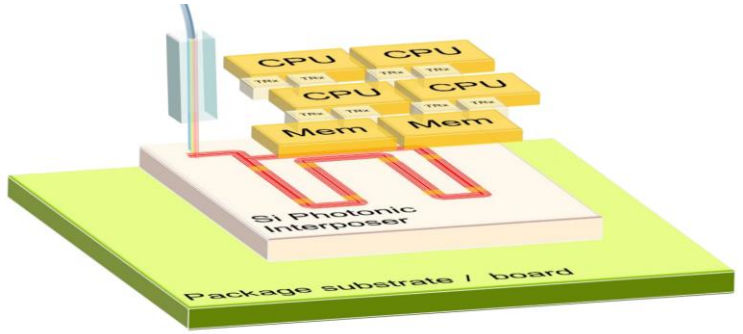
Interposeur actif INTACT [2]

2019

Photonic Interposer

Electrical Routing
Optical Network On Chip
OE conversion





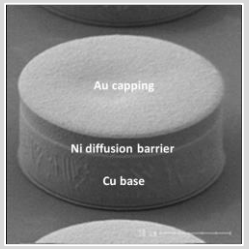
202x?

[1] C.-C. Lee et al., 2016 IEEE 66th Electronic Components and Technology Conference (ECTC)
[2] P. Coudrain et al., 2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

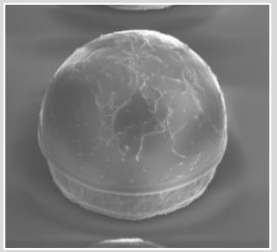
Courtesy of P. Tissier

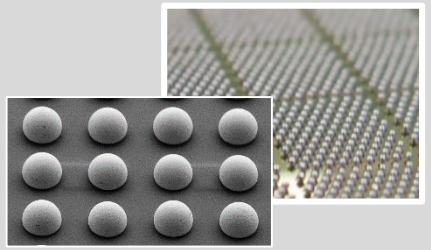
3D TECHNOLOGIES - LAB STATE OF THE ART

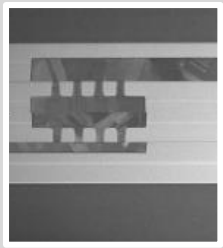
Connecting



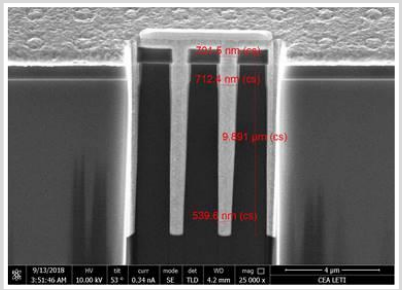
Copper pillars (Ø10µm)

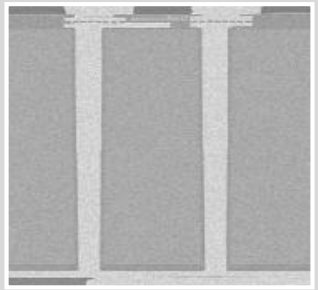

Copper- bumps (Ø10µm)

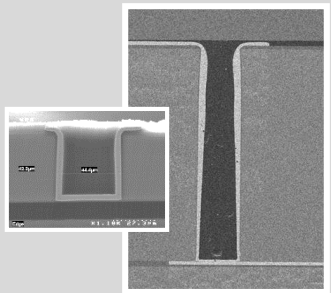

Bumping (Ø70µm)– Balling (Ø300µm)

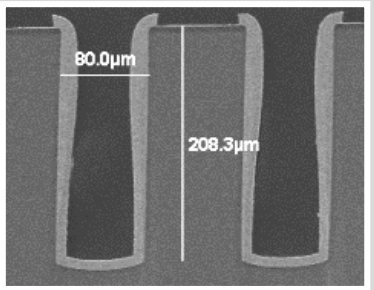

Hybrid bonding (LIFT)

TSV


TSV High Density AR10 Ø1µm

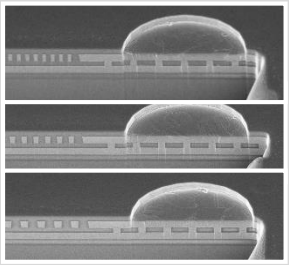

TSV mid AR10


TSV last AR 0,5 → 5

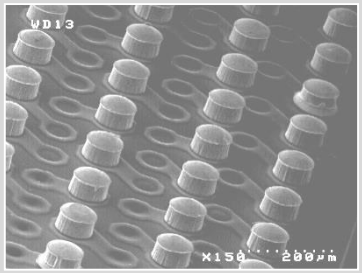


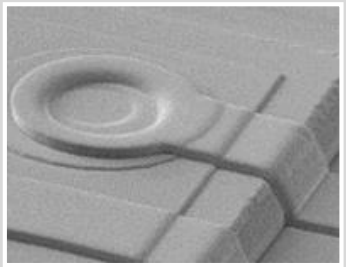
TSV last power (thick Cu-liner)

Rerouting


Front-side damascene (Pitch 400nm)

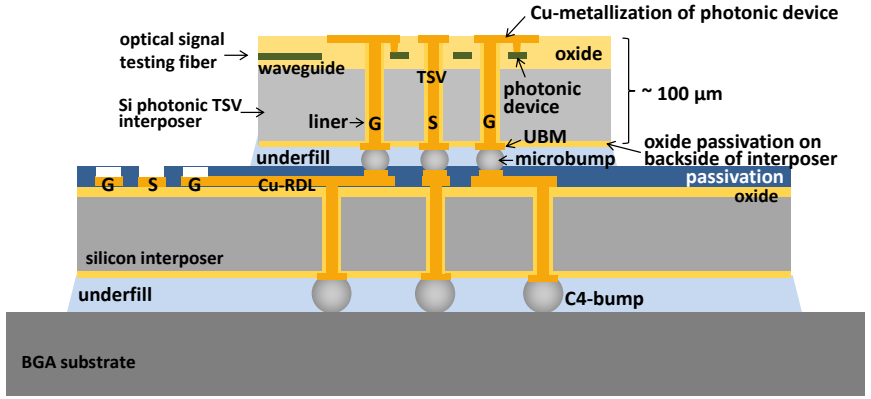

Back-side RDL co-integration (Pitch 20µm)

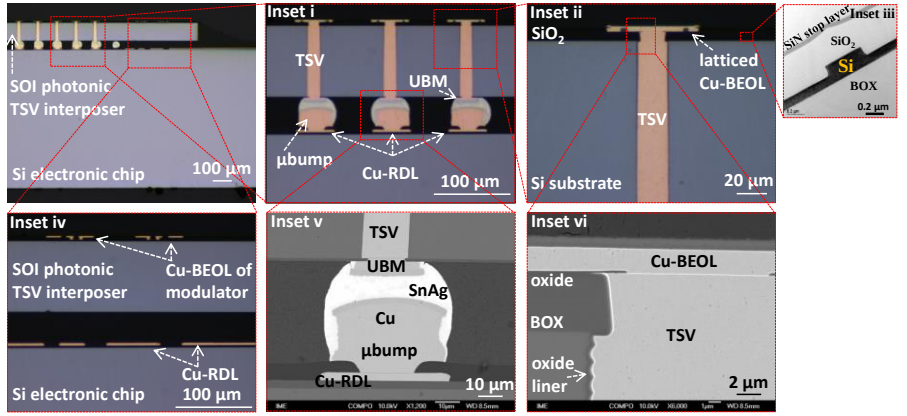


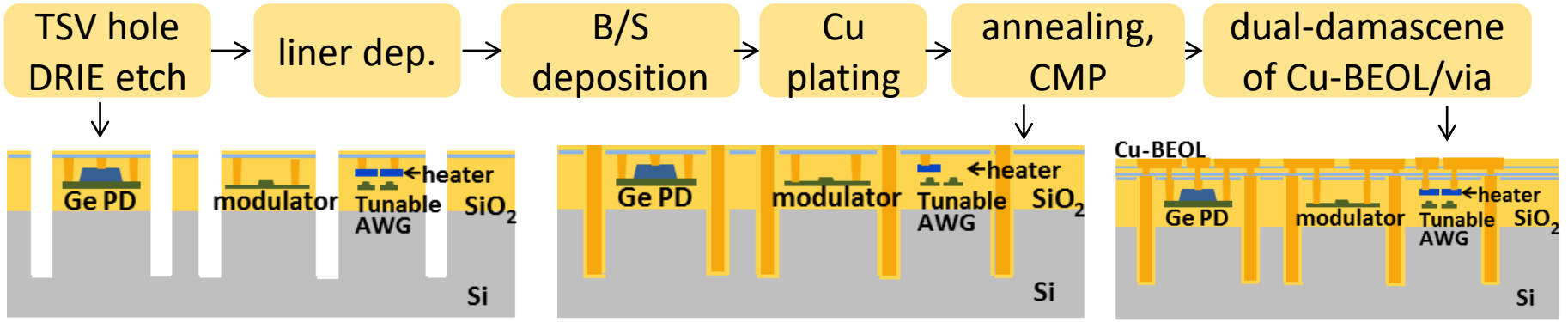

Cu conformal routing

Courtesy of J. Charbonnier

FIRST PHOTONIC INTERPOSER (IME/ASTAR, 2016)



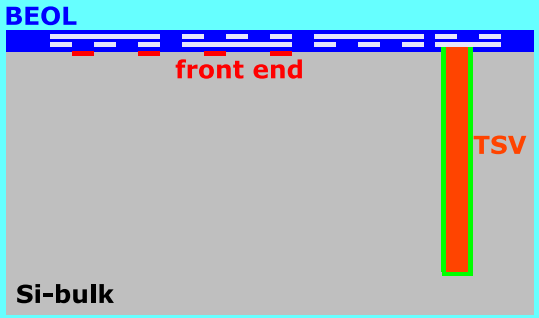




Yang, ECTC 2016

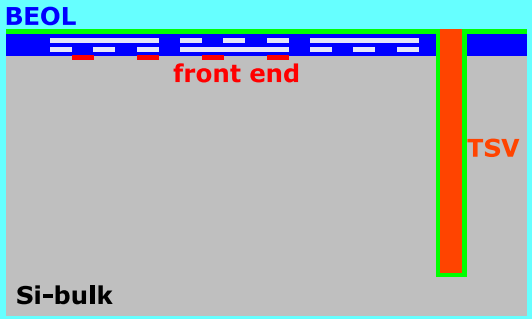
TSV DEVELOPMENT

Via first or middle;

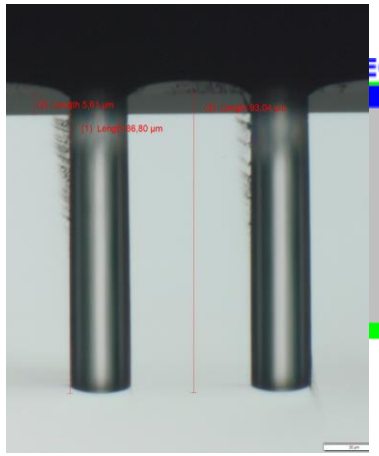


- TSV integration before FEOL or after FEOL / before BEOL
- Processes established at IDMs

Via last;



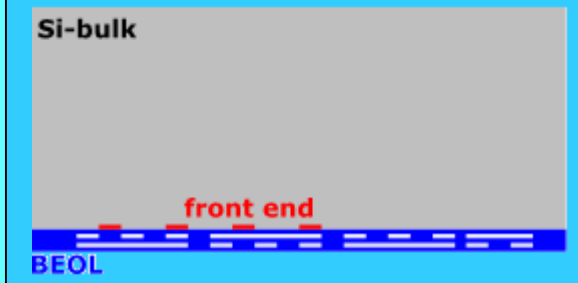
- TSV integration after complete wafer processing
- TSV through thick BEOL oxide
- Requires keep out zones in FEOL and BEOL for TSV integration



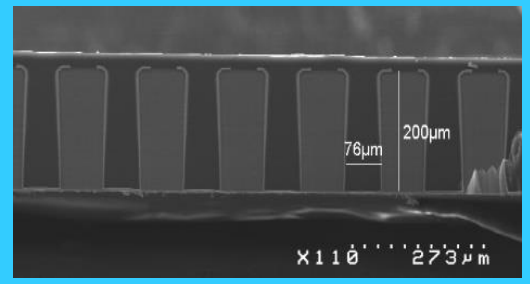
- Support wafer bonding
- Wafer backside thinning
- TSV reveal
- Backside RDL and bump formation
- Support wafer de-bonding

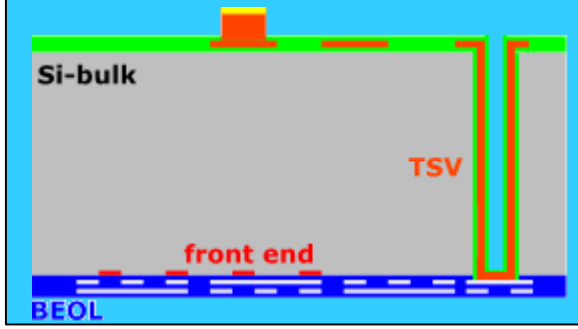
Courtesy of B. Sirbu, Fraunhofer IZM.

Back Side Via last



- TSV integration after complete wafer processing
- Requires landing pads in BEOL for prepared TSV connection



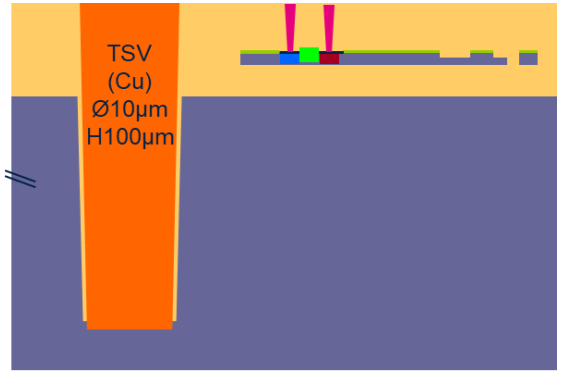


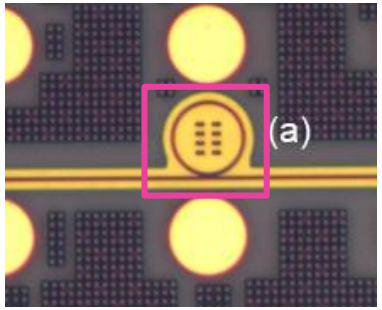
- Support wafer bonding
- Wafer backside thinning
- TSV formation with acess to landing pads
- Metall liner and back side RDL formation
- Support wafer de-bonding (if required)

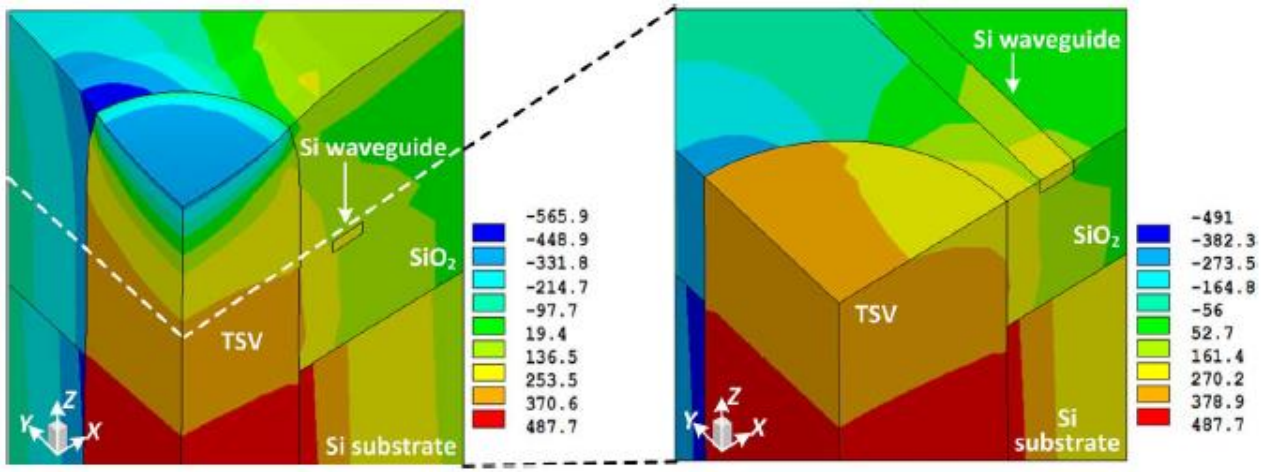
PHOTONIC INTERPOSER AT CEA LETi

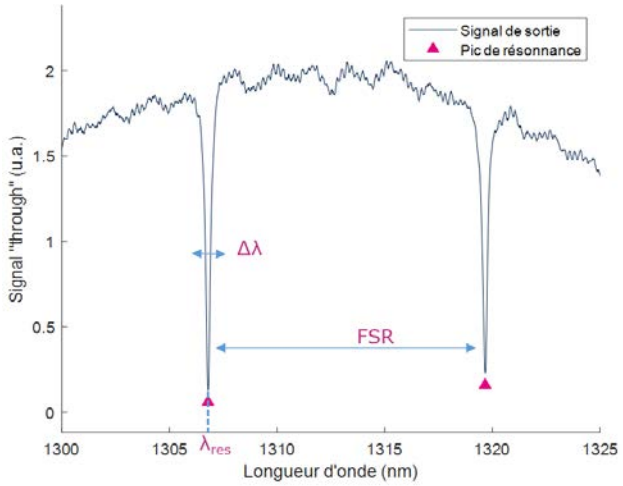
Dia. 10~12 µm, height 100 µm
TSV mid process

Does TSV interfere with photonics structures?
- CTE differential
- Thick BOX (can lead to warpage then stress)
- Optomechanical effect
- Keep Out Zone for Designers ?









P. Tissier, PhD Thesis defence

PHOTONIC INTERPOSER AT CEA LETi

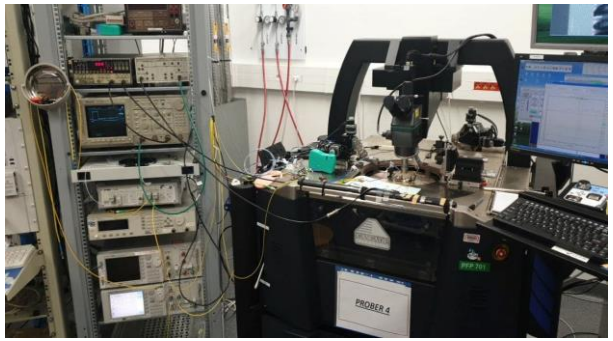
- Fabrication of Ring filters with TSV –last, on ST + LETi 300mm platform
- Measurement of X-Ray diffraction (Synchrotron)

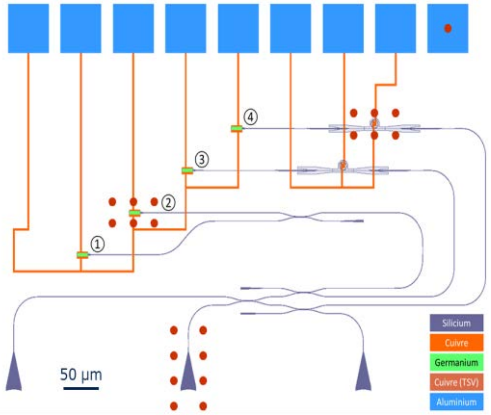
No evidence of high stress due to the TSV above 5µm distance

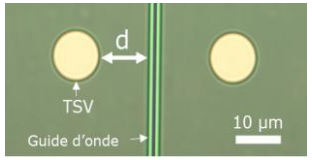
Confirmed by mixing simulated field of stress with FDTD optical simulations (Lumerical)

$$\Delta n_{eff} = 5{,}8 \cdot 10^{-4}$$

Experimental O/E measurements of Ring Filters







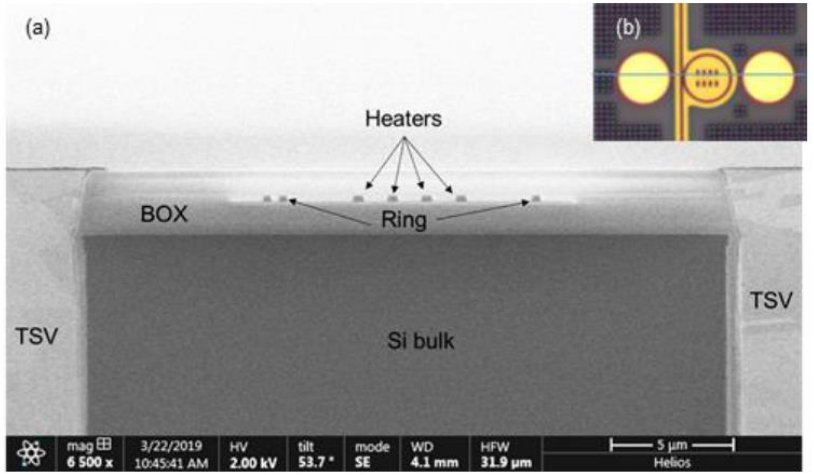
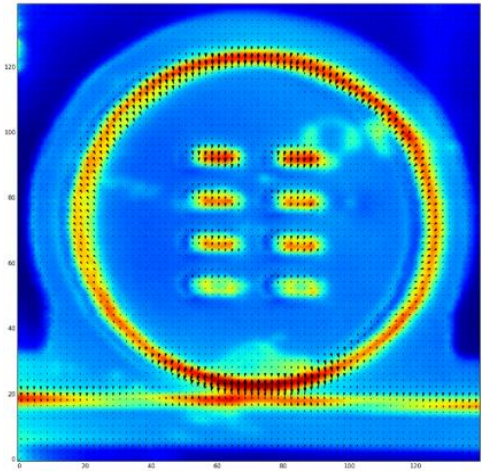
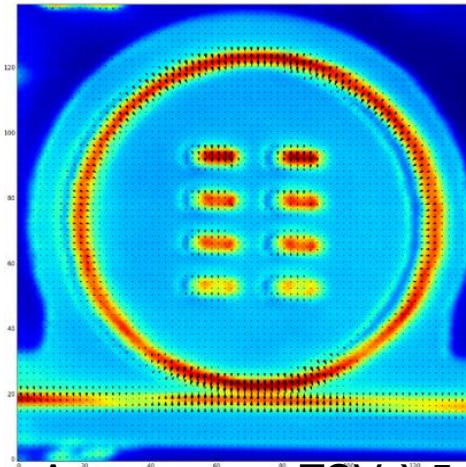


Fig. 4. a) SEM cross section of the TSV-surrounded ring before BEOL, b) optical top view of the ring and its TSVs and corresponding cross section plane



Anneau de référence

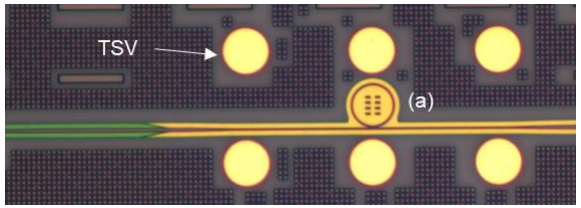


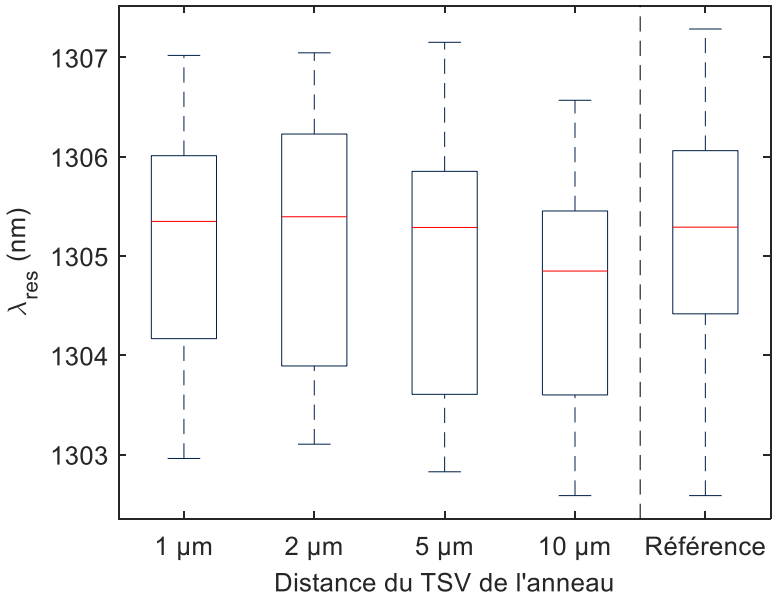
Anneau avec TSV à 5 µm

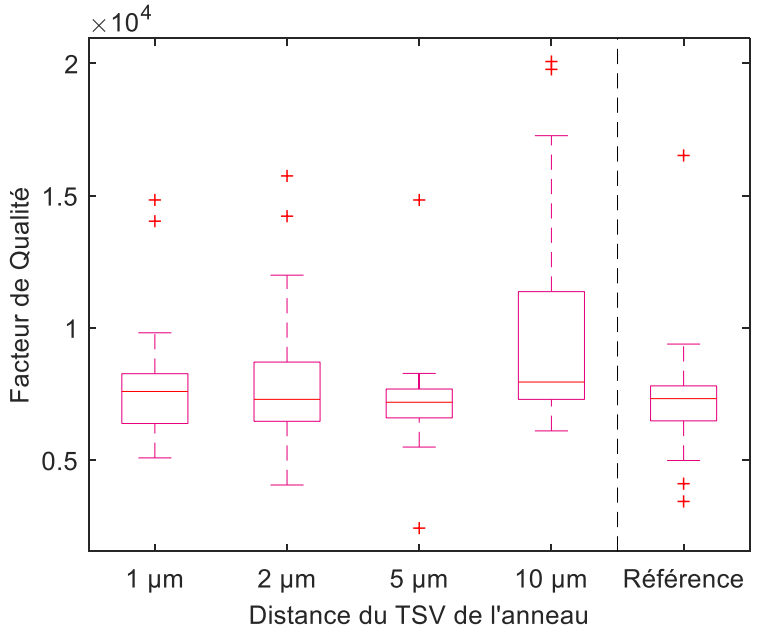
P. Tissier, PhD Thesis defence

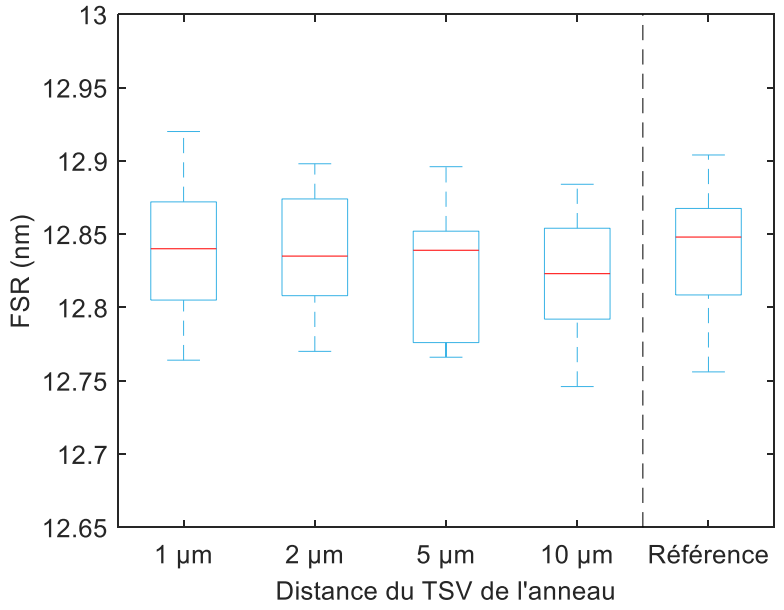
PHOTONIC INTERPOSER AT CEA LETi

- Ring features as a function of TSV-Ring distance





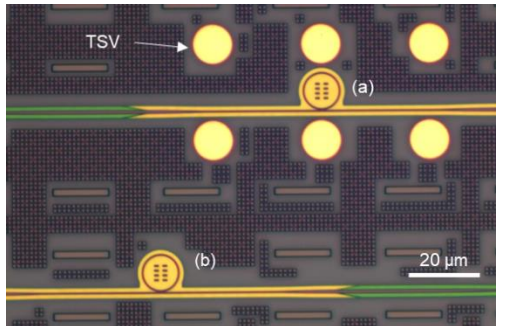


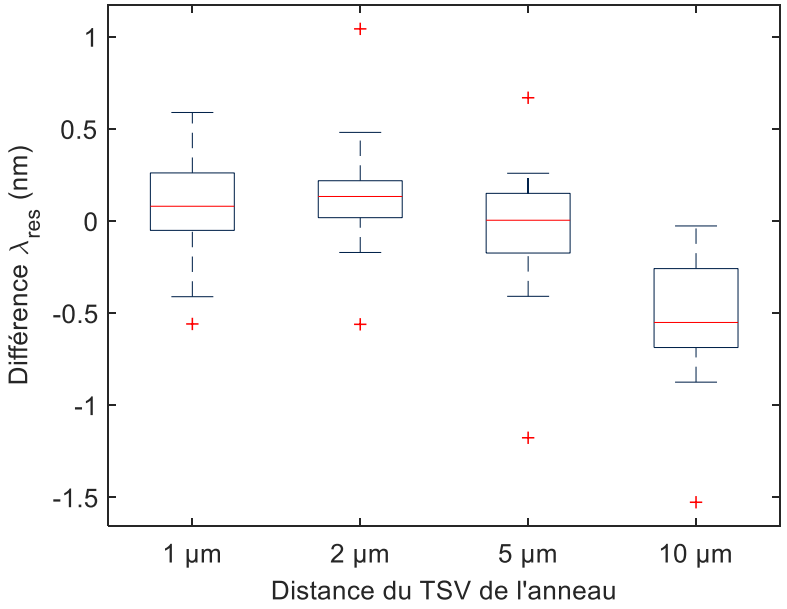


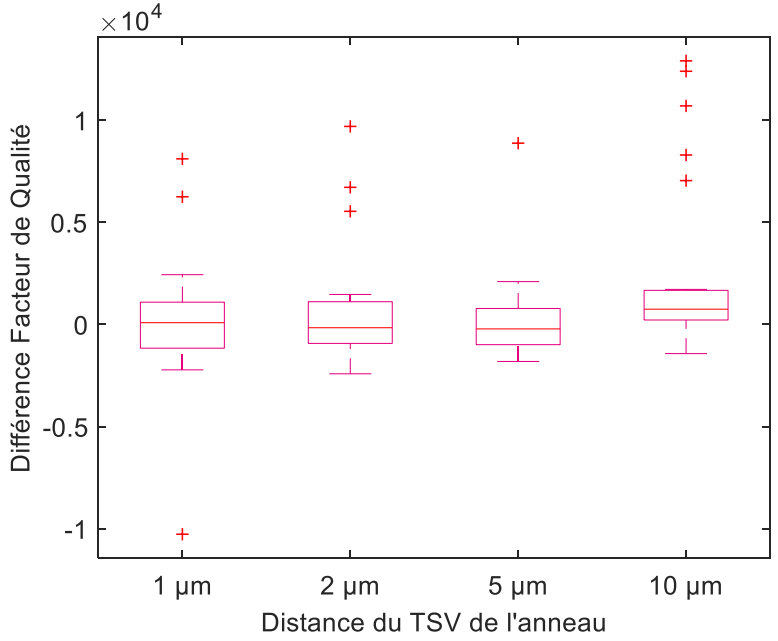
TSV effect is below process dispersion

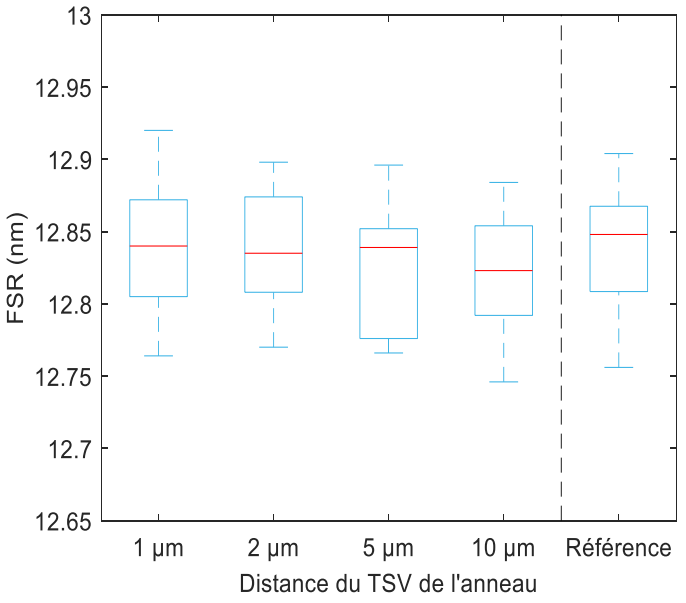
PHOTONIC INTERPOSER AT CEA LETi

Comparision with reference ring









No measured impact of TSV, KOZ > 1µm is safe

CONCLUSION

Silicon Photonics has widespread at every stage of the Internet Network, now targeting emerging applications

This lead to a new paradigm in terms of packaging & assembly

- Mass manufacturing is needed
- Advanced packaging technologies will be applied
- The main driver will always be the **Cost !**

SiPho packagers have to face some challenges:

- Laser integration
- Thermal constrains
- Fiber connector
- 3D integration

CEA LETI with ST microelectronics achieve a Photonics Interposer using Via Mid TSV

=> Keep Out Zone >1µm is OK for designers

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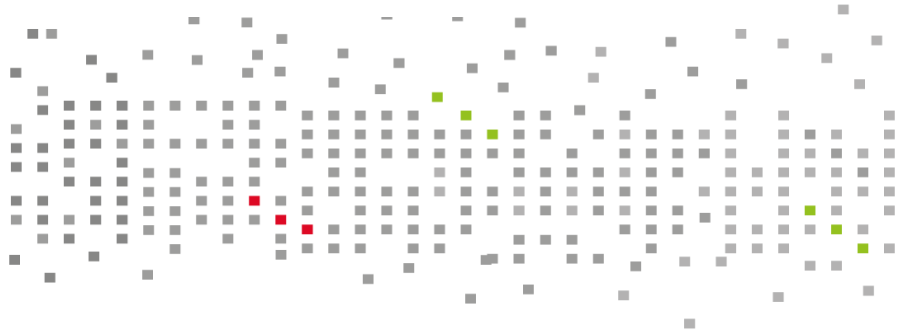
Paraskevas Bakopoulos (nVIDIA)

Leti Photonics team
Leti Packaging team
MASSTART project partners



IEEE ELECTRONICS PACKAGING SOCIETY

Q & A

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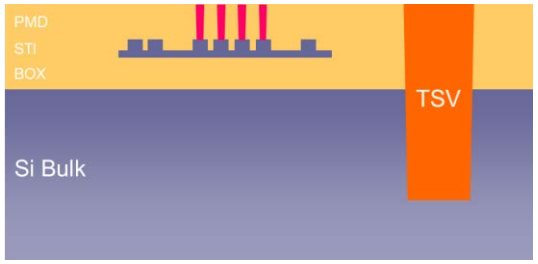
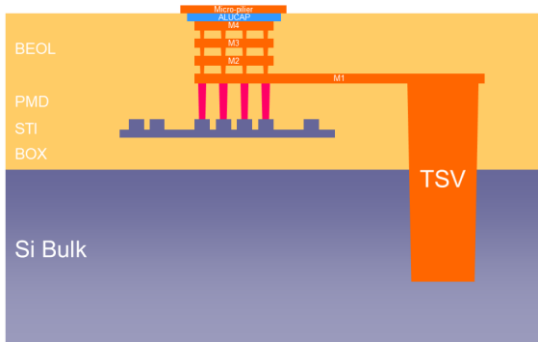
INSTITUT CARNOT Leti

Procédés de fabrication de l'interposeur photonique

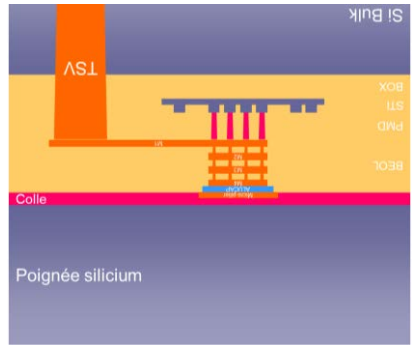
Eléments photoniques



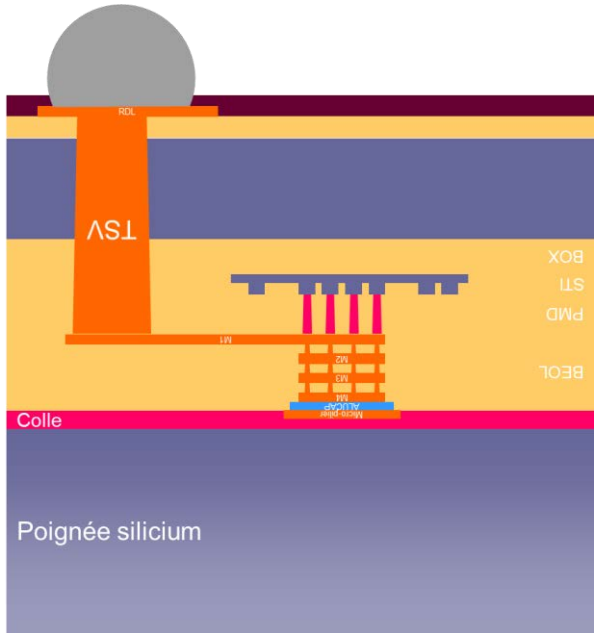
TSV mid-process



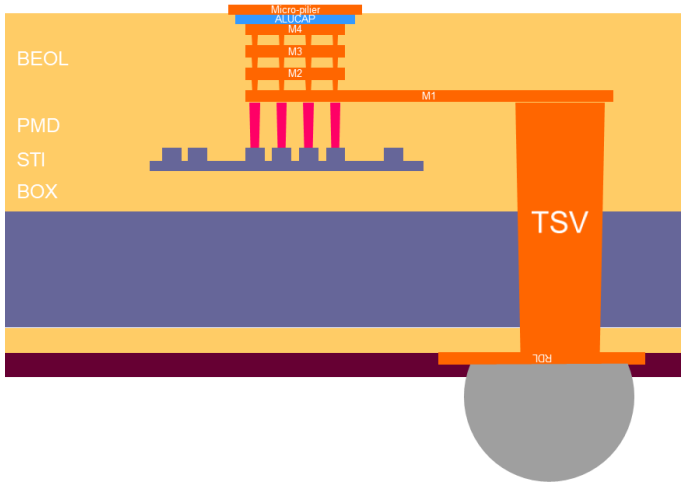
BEOL



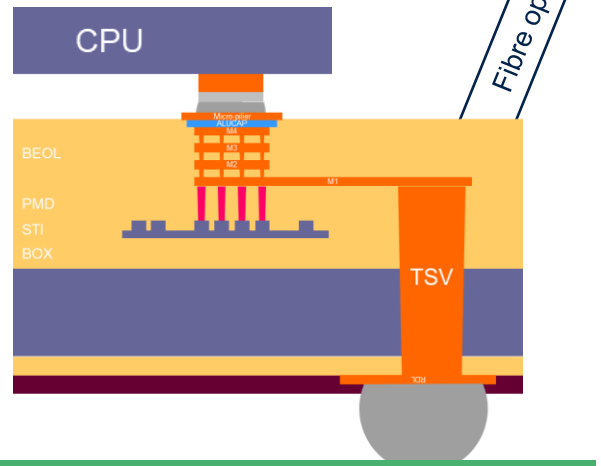
Collage et amincissement



RDL et billage



Interposeur final



Substrat organique

Interposeur assemblé