New routes and paradigms in Device Engineering for Nanoelectronics and Nanosystems

Distinguished Lecture IEEE SCV/SF Jt. Section Chapter, ED15 Joint Chapter
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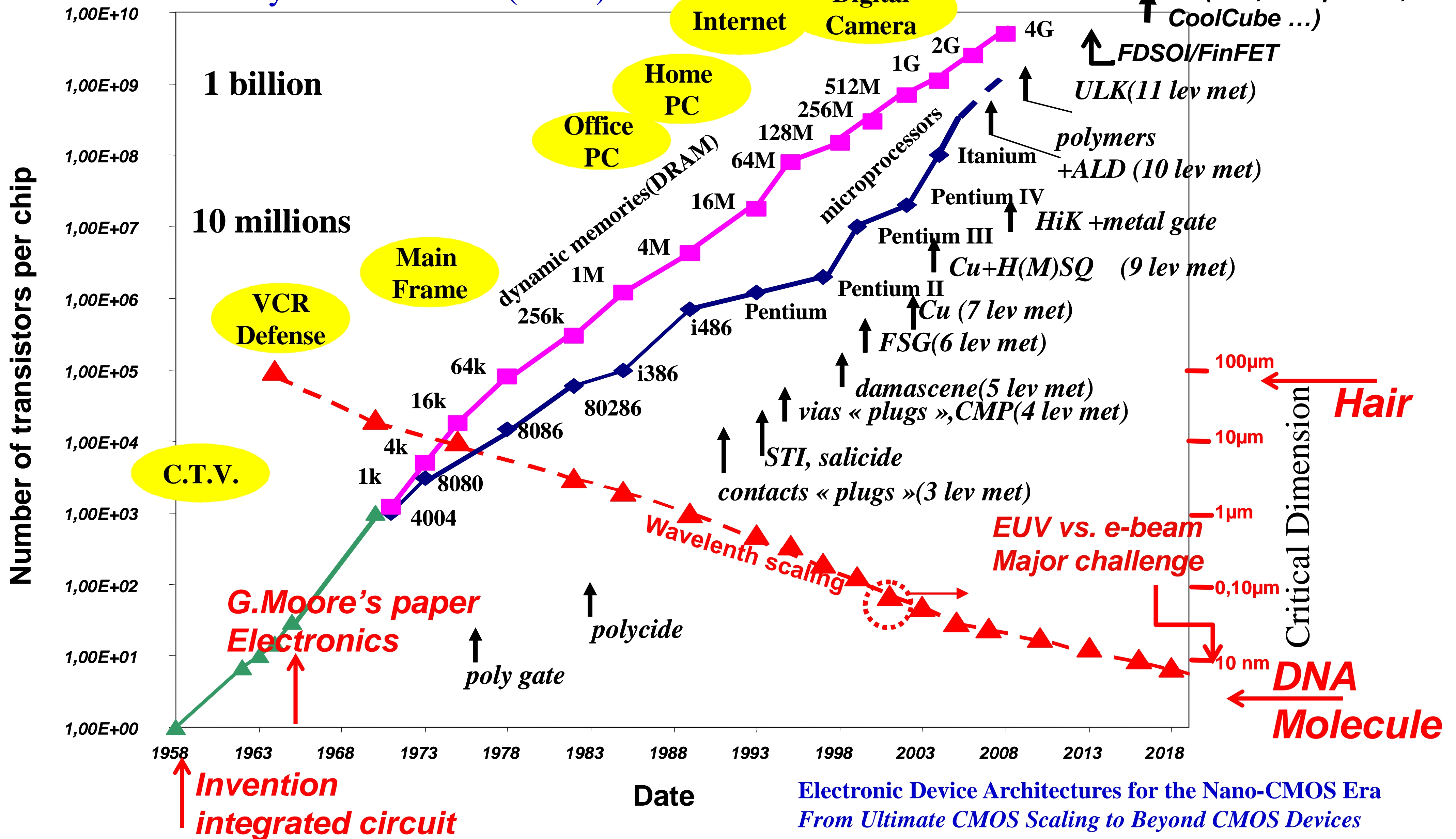
Simon Deleonibus,

Fellow IEEE, Fellow Electrochemical Society, CEA Research Director

Past Chief Scientist Université Grenoble Alpes, CEA, Leti
Grenoble, France

email address: simon.deleonibus.1992@ieee.org

Scaling: a success story…thanks to innovation
A succession of Things impossible to Make!!
Progress law for microelectronics



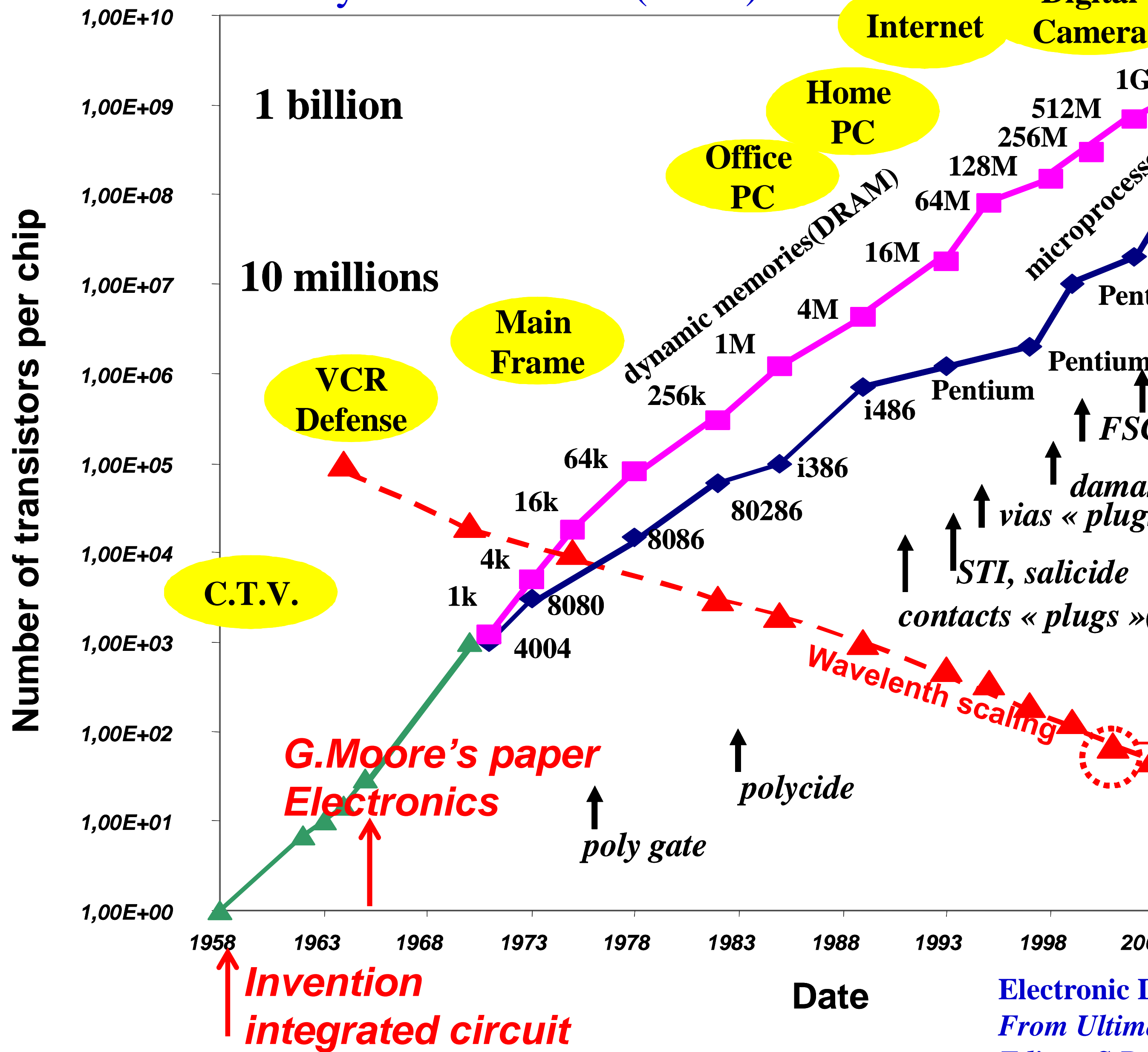
Electronic Device Architectures for the Nano-CMOS Era
From Ultimate CMOS Scaling to Beyond CMOS Devices
Editor: S.Deleonibus, Pan Stanford Publishing, Oct 2008

Scaling: a success story…thanks to innovation
A succession of Things impossible to Make!!
Progress law for microelectronics

Moore's law: 2Xdevices/year
10-15 years incubation(ITRS)

Smart Phone

Internet of Things & «Everything»

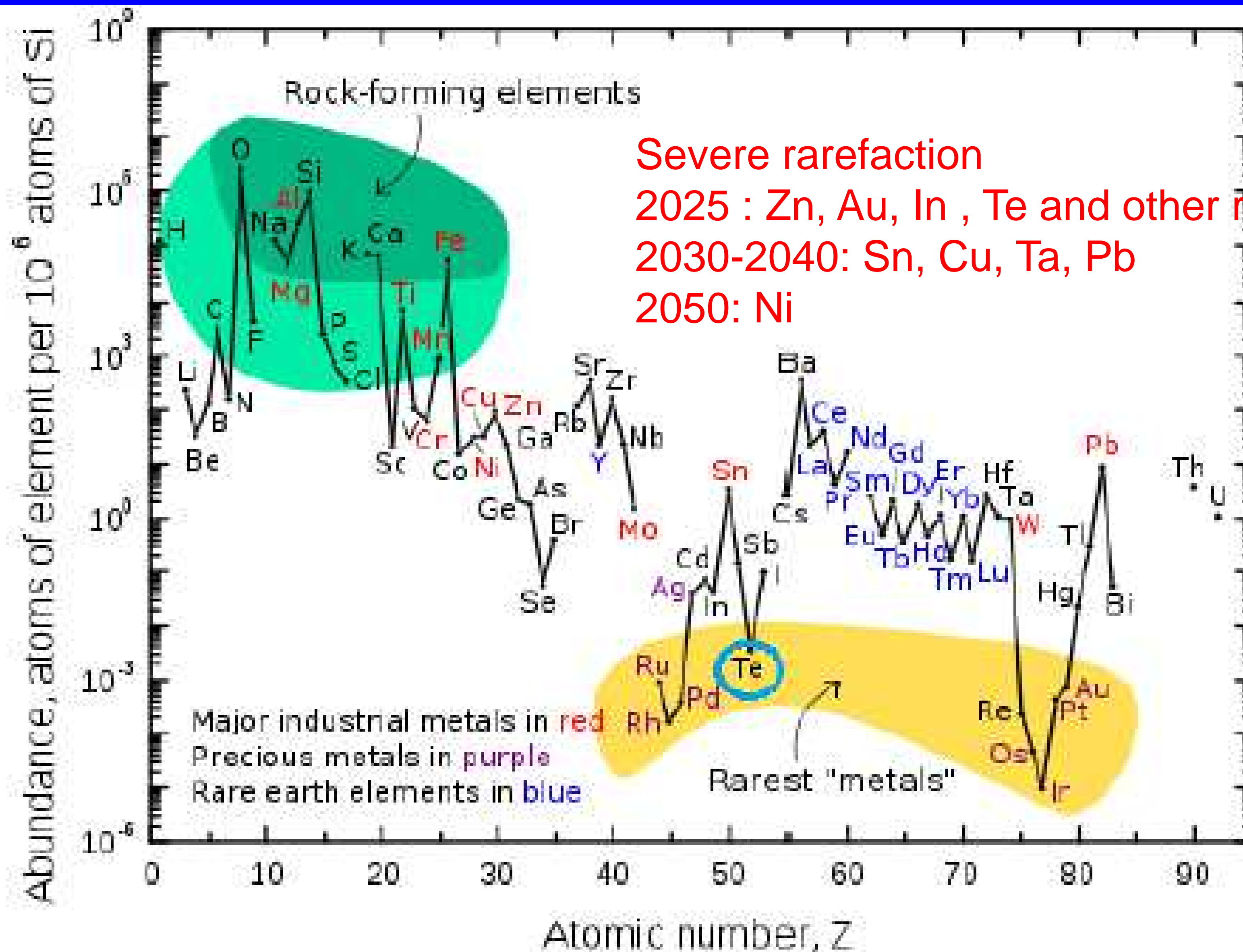


Energy and Variability Efficiencies are main concerns for ICT!!:
-Computing
-Data storage
-Communication
-Diversification

More than Moore:
Analog/RF, Passives, Sensing/ actuating, HV-Power, Bio&Healthcare)

2025: 25% WGDP will depend on ICT (pervasiveness):
****10^{21} exchanges of information/year(2017)***
**** Ecological footprint** (4% world electricity, CO2 emission)*
****Scarcity of spice metals***
****Market drivers(Autonomous /Nomadic /Heterogeneous):***
U-Low Power, Hi Perf
Drastic variability reduction

Availability of elements world reserve



Severe rarefaction
2025 : Zn, Au, In , Te and other rare earths
2030-2040: Sn, Cu, Ta, Pb
2050: Ni

Green Chemistry
i.e. catalysis is bio inspired
Circular economy

do make sense

Strengthened in research

http://infoterre.brgm.fr/rapports/RP-60206-FR.pdf

http://ec.europa.eu/environment/archives/greenweek2014/index.html

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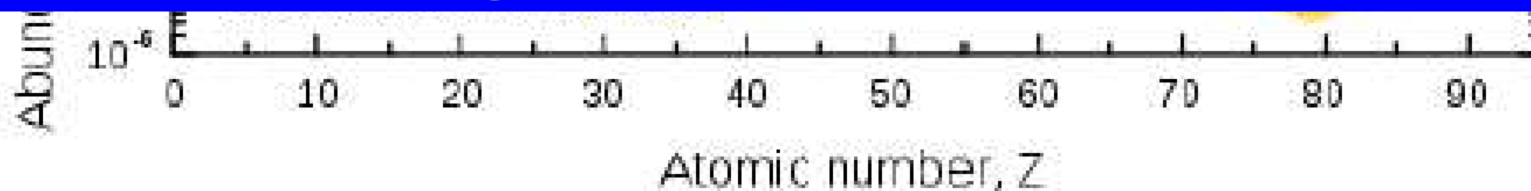

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More Integrated Sustainable Functions (MISF)

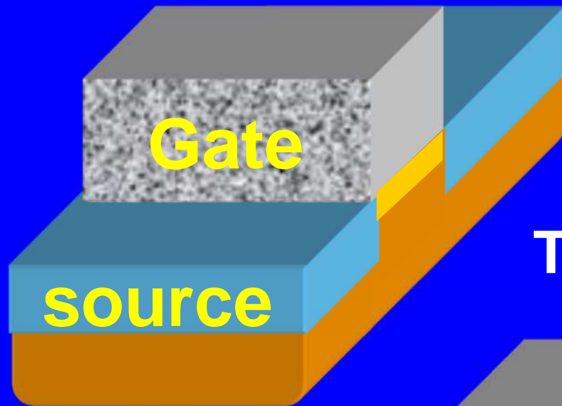
http://infoterre.brgm.fr/rapports/RP-60206-FR.pdf

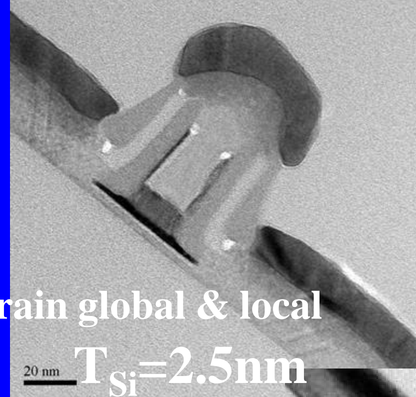
http://ec.europa.eu/environment/archives/greenweek2014/index.html

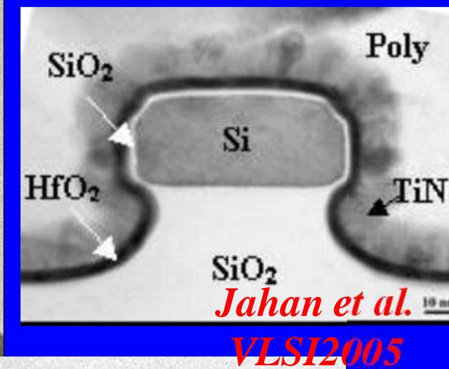
Outline

- Introduction
- Scaling of Silicon and thin films devices(More Moore):
  towards Low Power/High Performance
  and Zero Intrinsic Variability
- From 2D to 3D co-integration of More Moore
  and More than Moore devices for Diversification.
- Conclusion

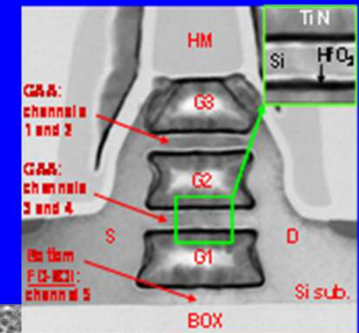
Bulk or thick SOI







VLSI2005

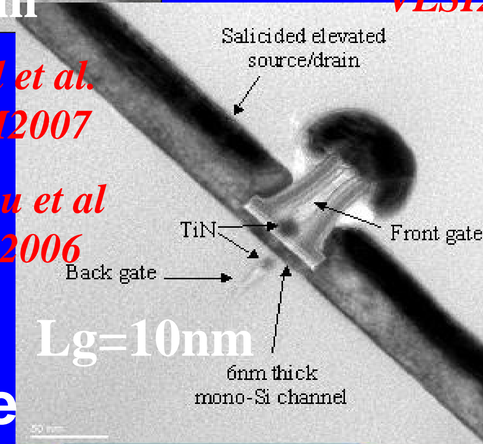


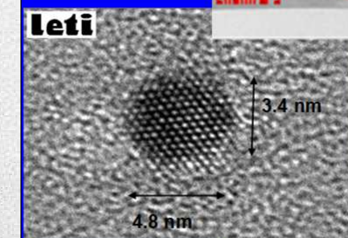
ThinSOI

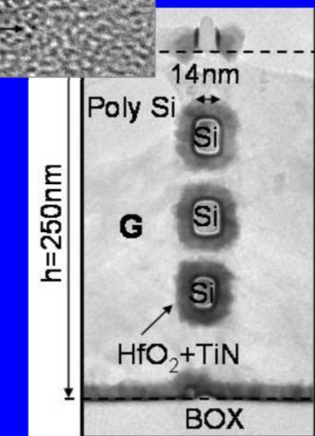
Planar

Barral et al. IEDM2007

Andrieu et al VLSI2006



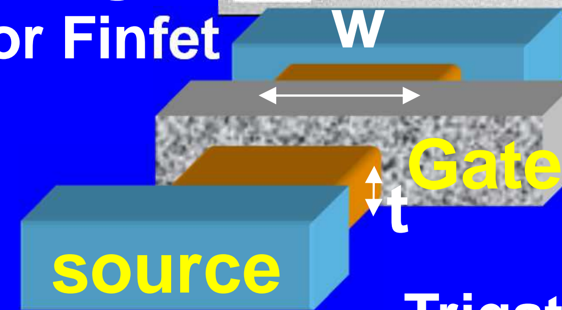




Double-gate
Planar or Finfet

Vinet et al. EDL 2005

T_{Si}= ¼ Lg



Bernard et al. VLSI 2008

Thin Films MOSFET Devices Scaling

-Electrostatic Integrity (clamping leakage current)

-Relaxing optimization scaling rule by architecture

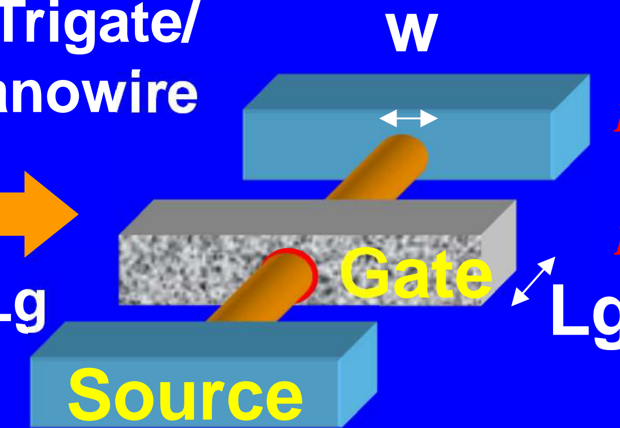
T_{Si}= ½ Lg

Trigate/ nanowire

Dupré et al. IEDM 2008

Ernst et al. IEDM 2008

T_{Si}= 1 to 2 Lg

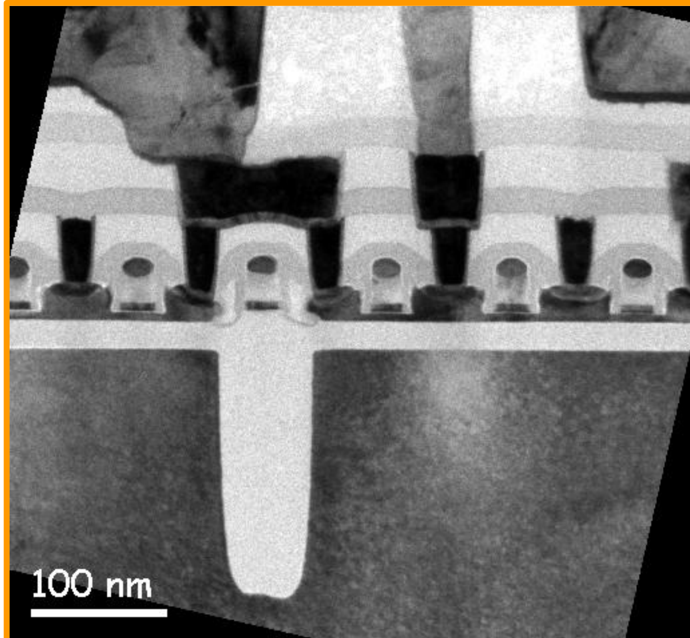


Energy efficient FDSOI

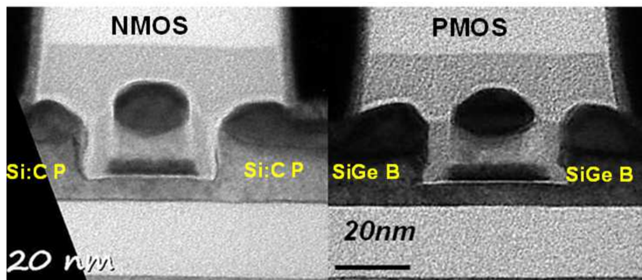
Thin Films Undoped channels

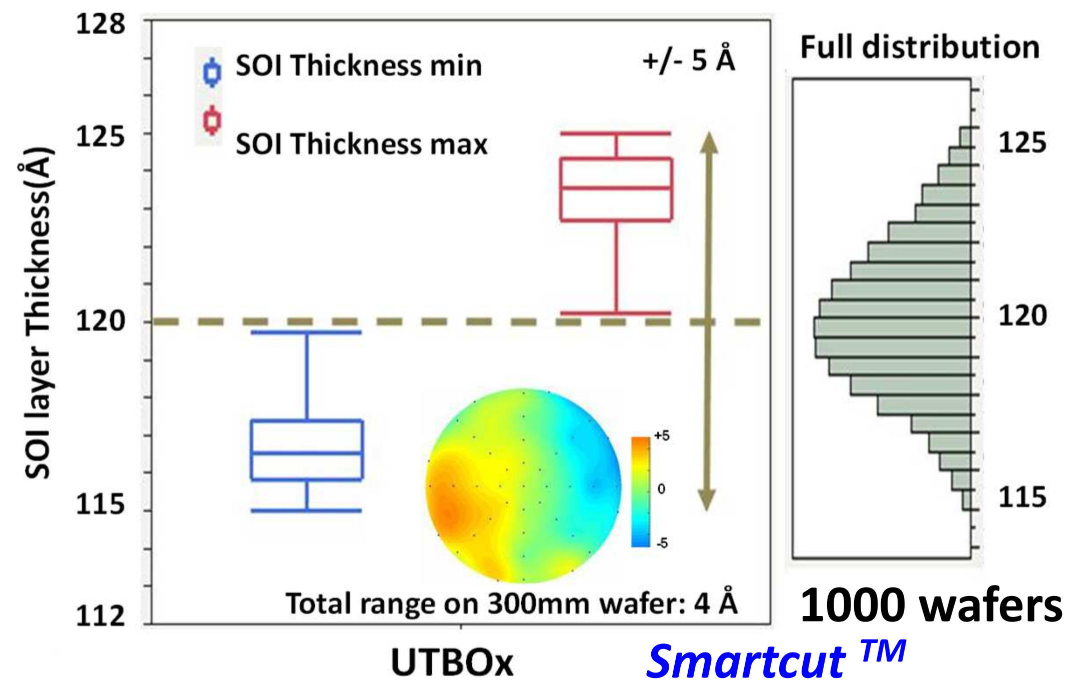
Ideal Electrostatic control

14 nm node 300mm wafers



T_{Si}=6nm
T_{Box}=20nm





*Record-high V_T matching performance (AVT=1mV.µm)
*Low Power and High performance -strain engineering (Tsi=6nm)(bi-ax, CESL, ESD)
=> outperfroms bulk(leakage, delay,Pwxdelay)
*Design platforms increased energy efficiency
*Scalability from 28 to 8 nm proven

LETI, ST Micro, SOITEC : O.Weber et al., VLSI Symp 2014 , IEDM 2008; S.Barraud et al, VLSI Symp 2013 ; C.Fenouillet-Béranger et al., IEDM 2007, VLSI Symp 2010 ; V.Barral et al., IEDM2007 ; S. Morvan et al, VLSI Symp 2011; R. Coquand et al. VLSI, Symp 2011; R. Wilson et al, ISSCC 2014; E. Beigne, DATE 2013

leti Soitec ST IBM

FDSOI outperforms state of the art bulk counterpart

Increased energy efficiency (including body red. capacitance and biasing techniques)

Novathor® platform : 35% performance increase;

(28 nm node) 25% lower power consumption; simpler design

Frequency (MHz)

2,7 GHz @ 1,3V

$P_{dyn}=CV_{dd}^2f$

$P_{stat}=V_{dd}I_{off}$

$P_{tot}=P_{stat}+P_{dyn}$

2500

Ultra Wide Voltage Range

Ultra Low Power

Low Power

High performance

460 MHz @ 0,397 V

INTEL (1.1V,1.8GHz,22nm)

TI(1.2V,1.2GHz,40nm)

INTEL (11mW/MHz)

1000

TI(1.1V,1GHz,40nm)

CEVA(1.1V,1GHz,40nm)

100

TI(200µW/MHz)

CSEM(100µW/MHz)

10

INTEL, 280mV 22 nm

NXP,IMEC (0.45V, 3MHz)

JSSCC'10(TI,MIT) (0.6V, 40MHz)

ISSCC'10(TI, MIT) (0.34V, 3MHz, ext mem)

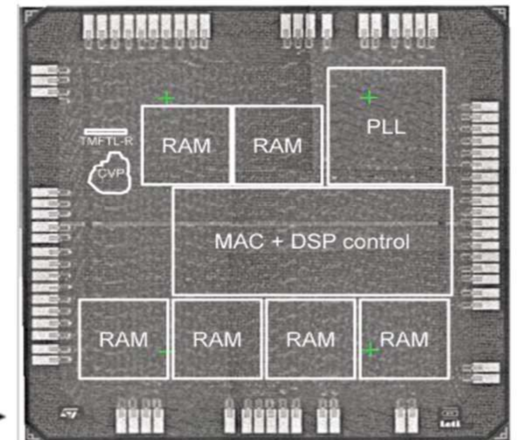
1

0.35V

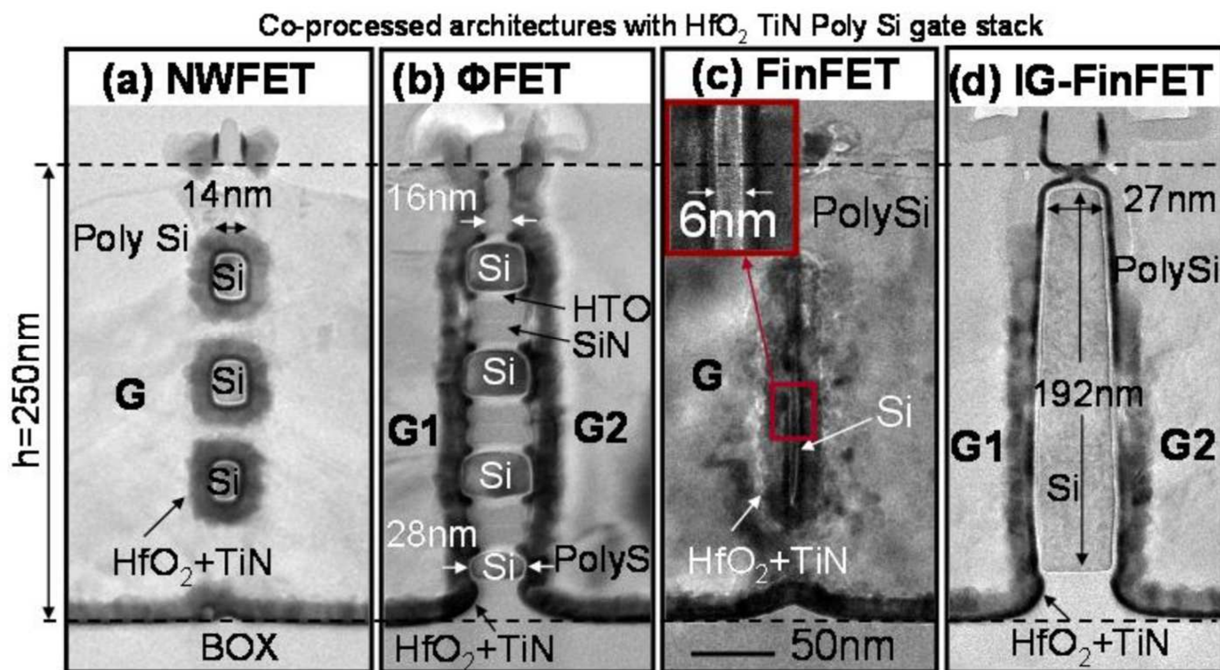
1.0V

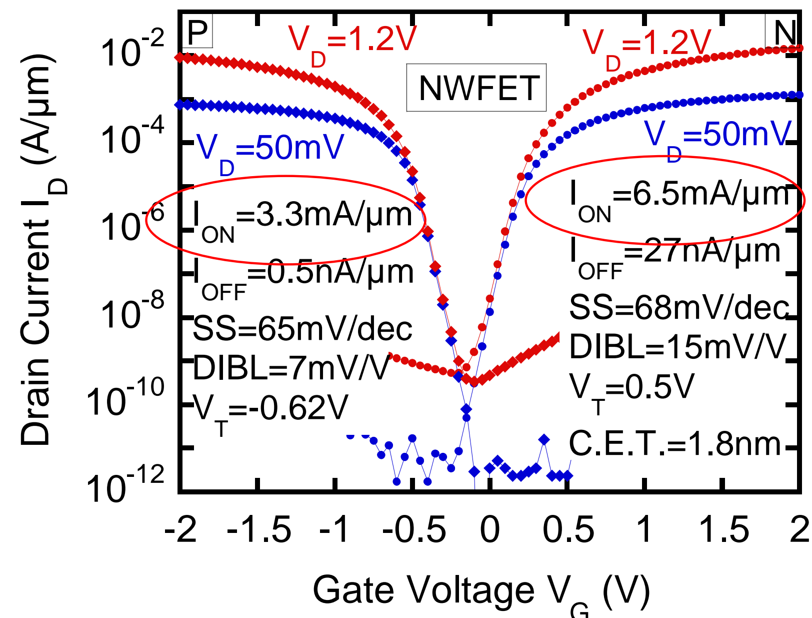
1.3V

Vdd (V)

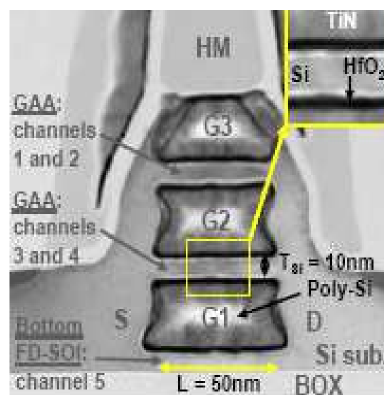


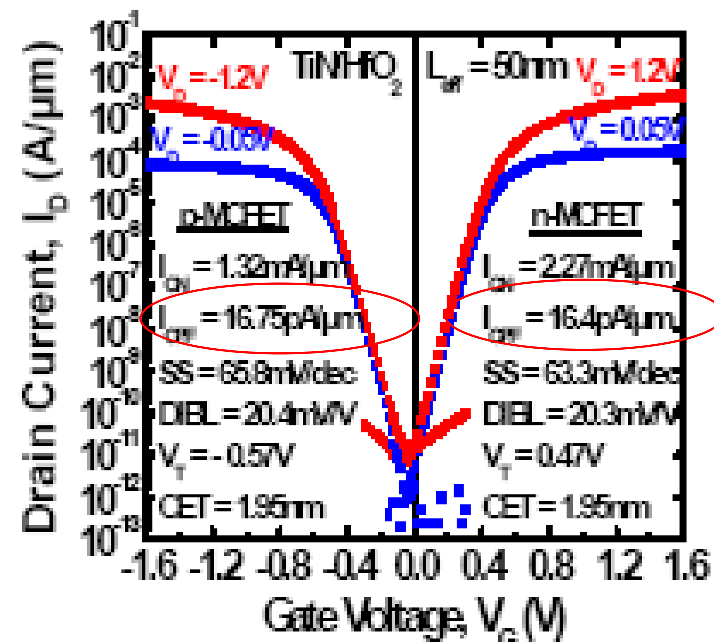
Stacked Multichannels and MultiNanowires « Top-Down » approach





LETI top down approach for Low Power and High performance



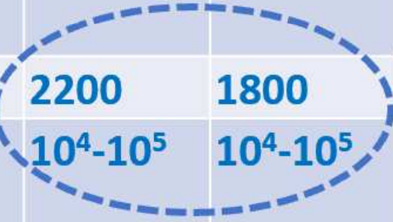


LETI: Dupré et al. IEDM 2008, San Francisco(CA)
Ernst et al., Invited talk IEDM 2008, San Francisco(CA)
Bernard et al, VLSI Symposium 2008 Honolulu
A.Hubert et al, ECS Spring Meeting, 2008,

Undoped channels

Opportunities for other materials on Silicon

Material	μn ($cm^2V^{-1}s^{-1}$)	μp ($cm^2V^{-1}s^{-1}$)	σth (W/m/K)	Rel. k	Eg (eV)	v_{sat} (10^7 cm/s)	n_i (cm^{-3}) (1)	Dielectric strength (10^6V/cm)
Si *Well established high quality material (>50yrs experience) Oxidizable !*	1400	500	141	11.9	1.12	0.86	$2X10^{10}$	0.25
Ge *Silicon compatible. Available in all fabs GaAs lattice constant matching*	3900	1900	59.9	16	0.66	0.60	$2X10^{13}$	0.10
GaAs *Opto/Power RF applications Ge compatible*	8500	400	55	12.9	1.42	0.72	$2.1X10^6$	0.40
$InGa_{0.47}As_{0.53}$ *HP N channel*	12000	300	5	13.9	0.74	0.60	$6X10^{11}$	0.20
InSb *Highest μ_n but Worst μ_n/μ_p!! Poorest short channel effect immunity*	77000	850	1.8	16.9	0.17	5.0 @77K	$2X10^{16}$	0.001
C-diamond (sp3) *Most compact logic, Interconnect*	2200	1800	2000 *Highest σ_{th}*	5.7	5.47	2.7	10^{-27}	2000
Graphene/CNT (sp2)	10^4-10^5	10^4-10^5	1000	5.7 *High immunity to short channel effect*	Semi metal & Low BG	4.00	$1X10^{12}cm^{-2}$ /$1X10^{15}$	
Si:C(3C/4H)	800/900	40-320 /115	320 /370	9.72 /9.66	2.36/ 3.23	2.5 /2.00	$1.5X10^{-1}$ /$5X10^{-9}$	2.12/2.2
GaN(Wurtz/Zinc Blende)	1000	200 /350	130	8.9 /9.7	3.44 /3.23	2 /1.75	$5x10^{-11}$ /$2x10^{-10}$	5



(1) $(m^*_e m^*_h)T^{3/2}exp(-Eg/2kT)$

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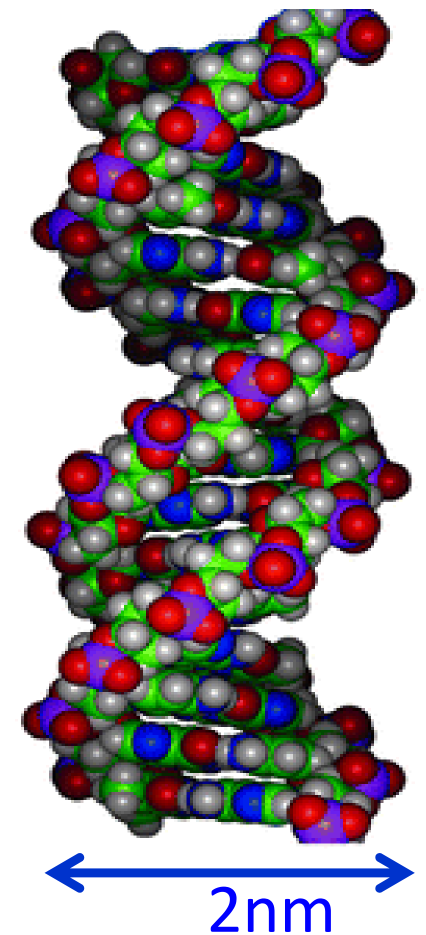
Approaching Zero Intrinsic Variability at sub-5 nm devices level on Si and challenging materials

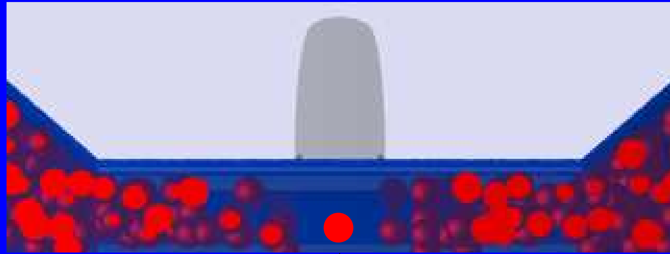


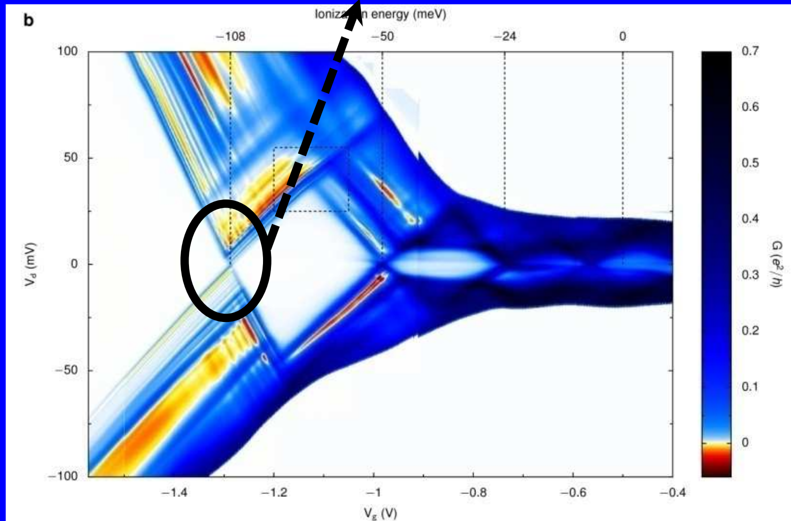
Main topics to be addressed :

- Dopant control at the single atomic level:
  deterministic doping by single ion implantation, chemical grafting, STM aided CVD ***(Tohoku Univ., CEA-LETI/CPE, UNSW)***
- Monodisperse patterning:
  self assembly block co-polymers, self limiting chemical dry etching,… ***(CEA-LETI/Arkema, CNRS-LTM, Stanford Univ)***
- Interconnect with monodisperse features and objects :
  CNT,MIM contact heterostructures, DNA templates,… ***(CEA-LETI, Tsukuba U., Tokyo, UCSB,…)***
- Few to Single electronics (memories, logic): opportunities for Q-computing by spin manipulation using Pauli blockade
  (CEA-LETI, Tokyo Institute of Technology, Hokkaido Univ.,…)
- Are Atomically thin active 2D Semiconductors Challenging Si ?
  Zero Intrinsic Variability: materials physical properties atomically thin sheet
  Opportunities to Si add-ons and Diversifications ***(EPFL, Notre Dame U., Penn State U.)***

S. Deleonibus et al., Invited talk, IEDM 2014

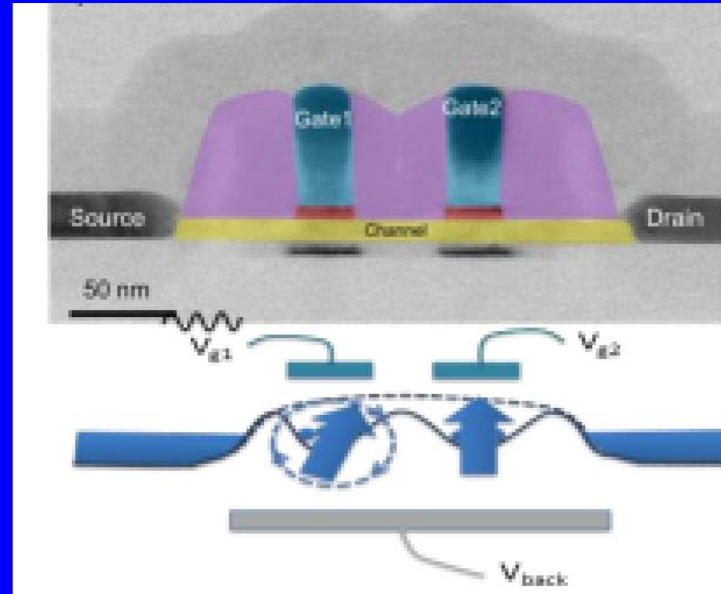
SINGLE ELECTRON, SINGLE ATOM, SINGLE SPIN EFFECTS

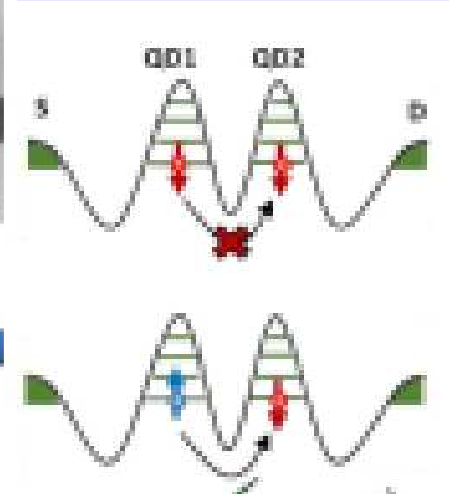


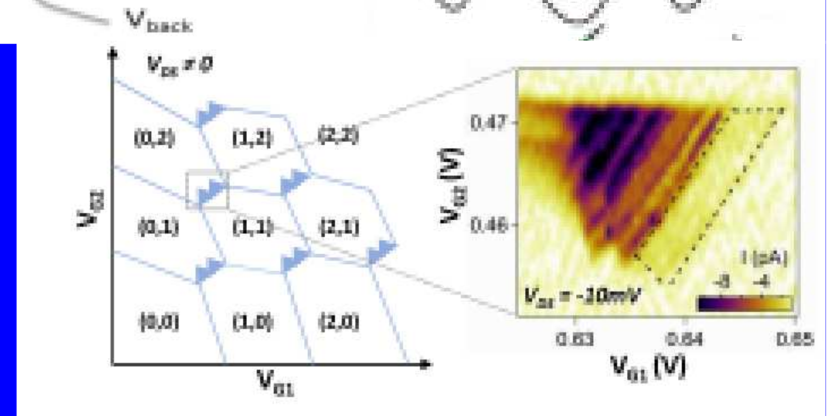


T<90K

Coulomb Blockade- Discrete nature of dopants *distributed randomly* affects MOSFET device behaviour at small sizes





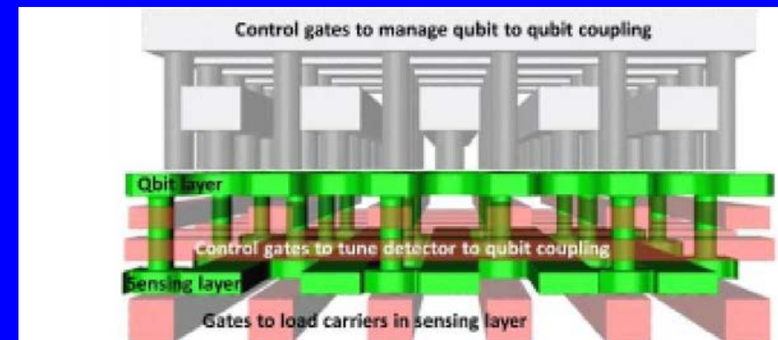


Pauli Blockade Spin manipulation T<1K

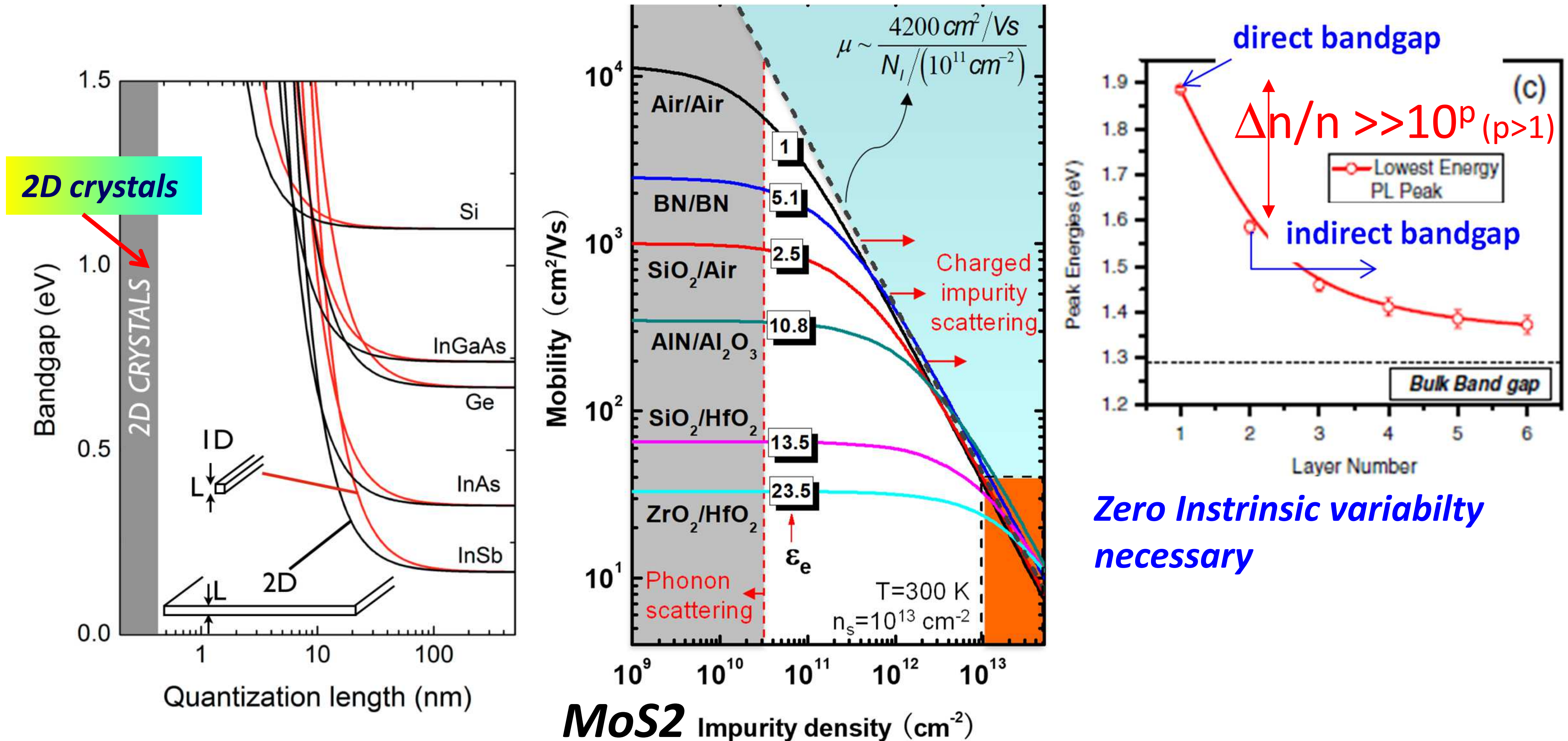
Electron pump, Multivalued Logic, Quantum Computing

CEA-LETI&CEA-INAC:
M.Vinet et al, IEDM 2018
M. Urdampitella et al. , VLSI Tech 2017
R.Maurand et al., , Nature Comm., 2016
L.Hutin et al., VLSI Tech 2016
S. de Franceschi et al. IEDM 2016
M. Pierre *et al.*, Nature Nano. 5, 133, 2010
Roche B. et al., Nature Comm., 4, n° 1581
R. Wacquez *et al.*, VLSI symposium 2010
TIT: T.Kodera , S.Oda , JJAP, 2010

Sequential 3D matrix approach
(sensing, reading , actuating,…)



2D Crystals offer new spaces and add-ons to Si



Atom-thick, hexagonally arranged 2D sheets : graphene, hBN, silicene, germanene , layered oxides and chalcogenides (MoS_2 , WSe_2 , Bi_2Se_3 , Bi_2Te_3)

Flexible

Transparent

Highly conductive

Jena et al, 2014 SNW

Ma & Jena, PHYS. REV. X 4, 011043 (2014)

K. F. Mak et al, Phys. Rev. Lett. 105, 136805 (2010).

2D Crystals offer new spaces and add-ons to Si

2D crystals

Bandgap (eV)

1.5
1.0
0.5

2D CRYSTALS

Si
InGaAs
Ge
InAs

ID
L

Mobility (cm²/Vs)

10^4
10^3
10^2

$\mu \sim \frac{4200\, cm^2/Vs}{N_I/(10^{11} cm^{-2})}$

Air/Air
BN/BN
SiO_2/Air
AlN/Al_2O_3
SiO_2/HfO_2
ZrO_2/HfO_2

1
5.1
2.5
10.8
13.5
23.5

Charged impurity scattering

direct bandgap

(c)

$\Delta n/n >> 10^p$ (p>1)

Lowest Energy PL Peak

indirect bandgap

Peak Energies (eV)

1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2

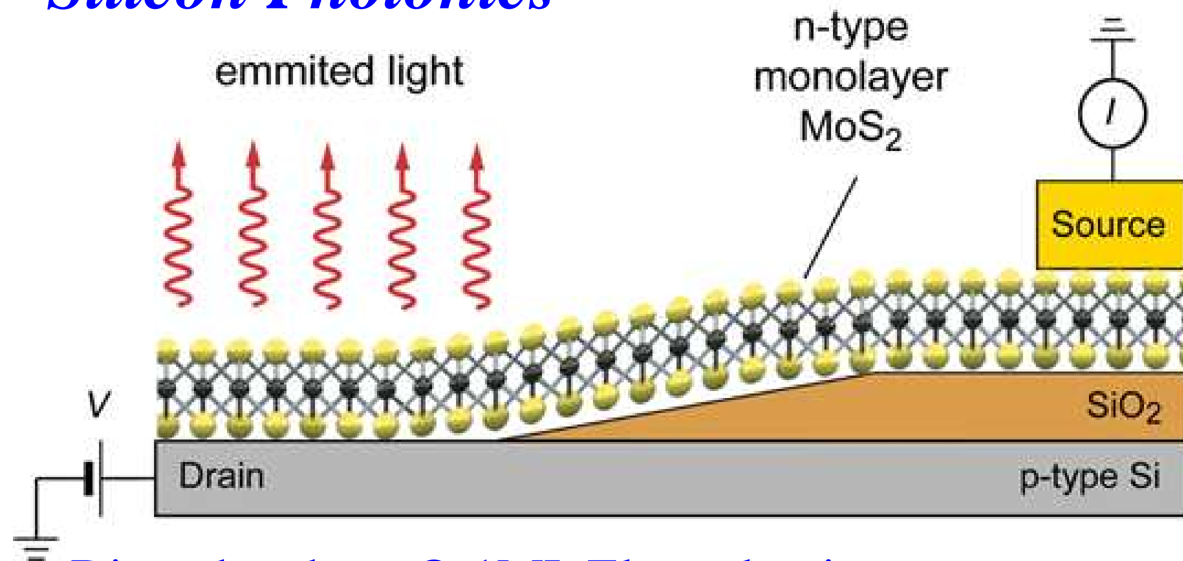
Bulk Band gap

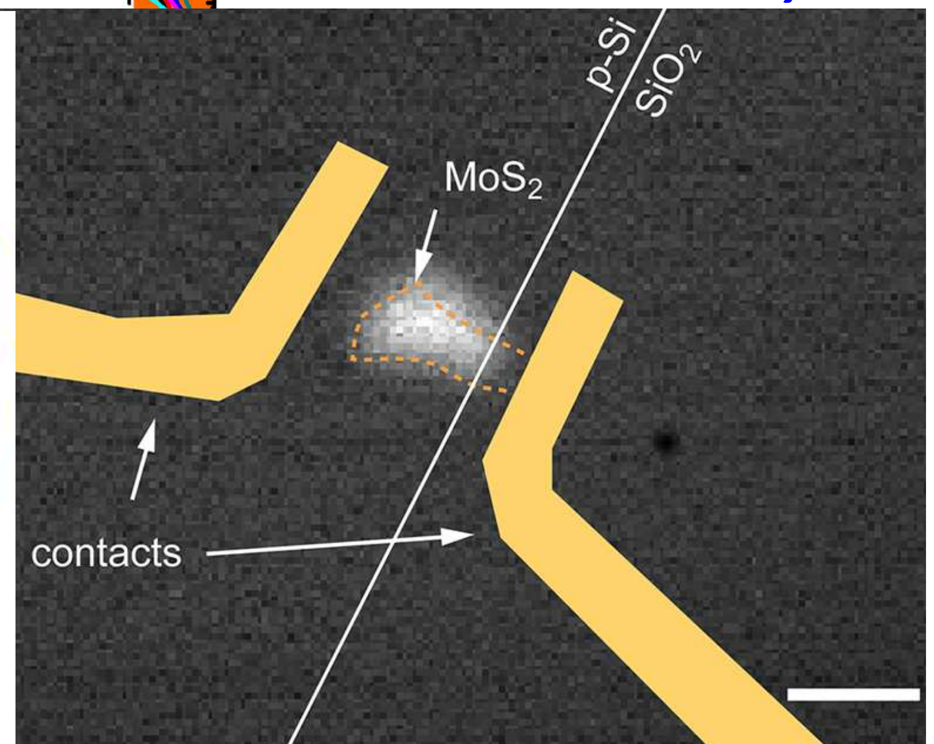
1
2
3
4
5
6

Layer Number

Zero Instrinsic variabilty

Silicon Photonics





Direct bandgap @ 1ML Electroluminescent
and PV heterostructure *O.Lopez-Sanchez, ACS Nano, 2014*

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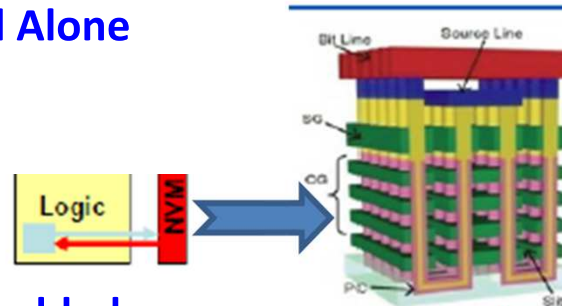
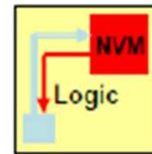
Opportunities for innovations with Resistives memories

Typical implementations

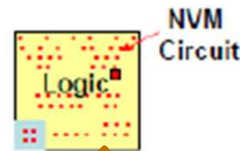
Revise Memory Hierarchy and Exploit granularity

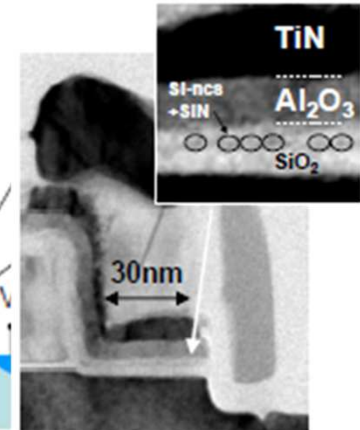
Stand Alone 3D





Embedded

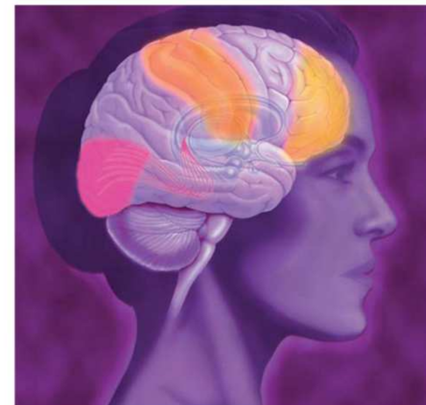


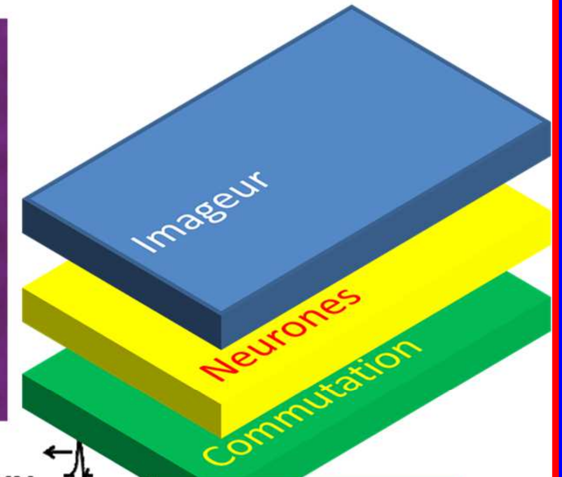


Distributed

NVM Circuit

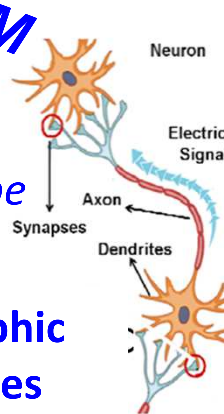
Logic

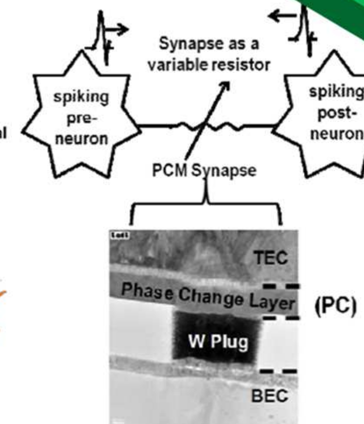


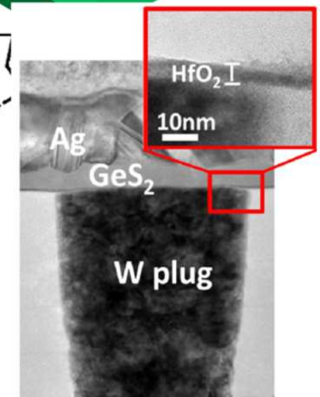


Logic + NVM

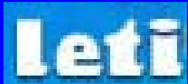
Vision & Audition type
Pattern recognition



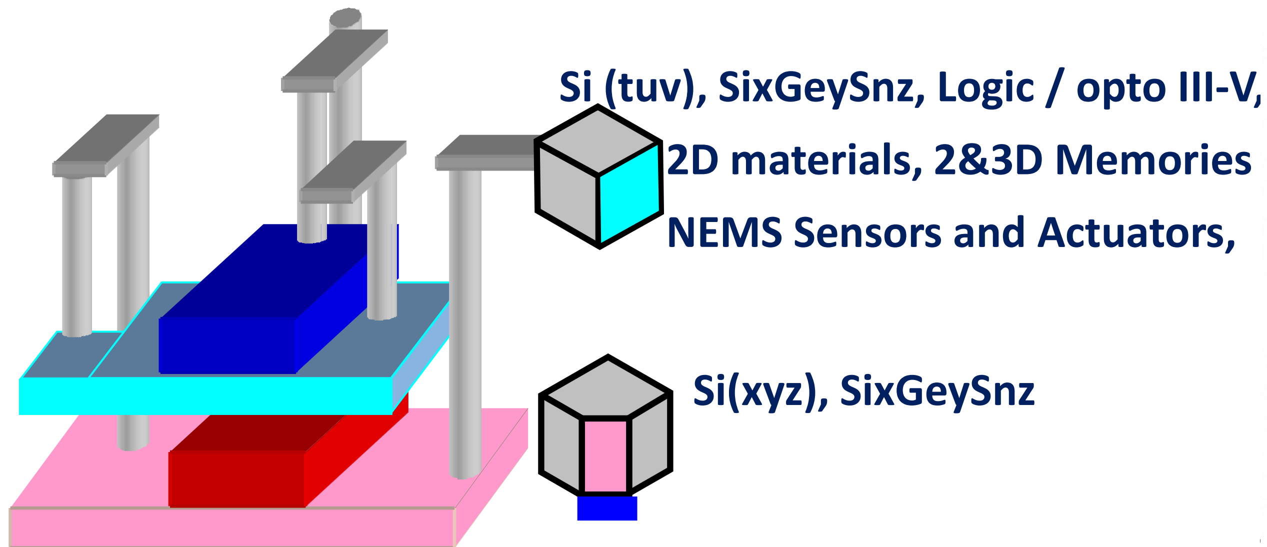


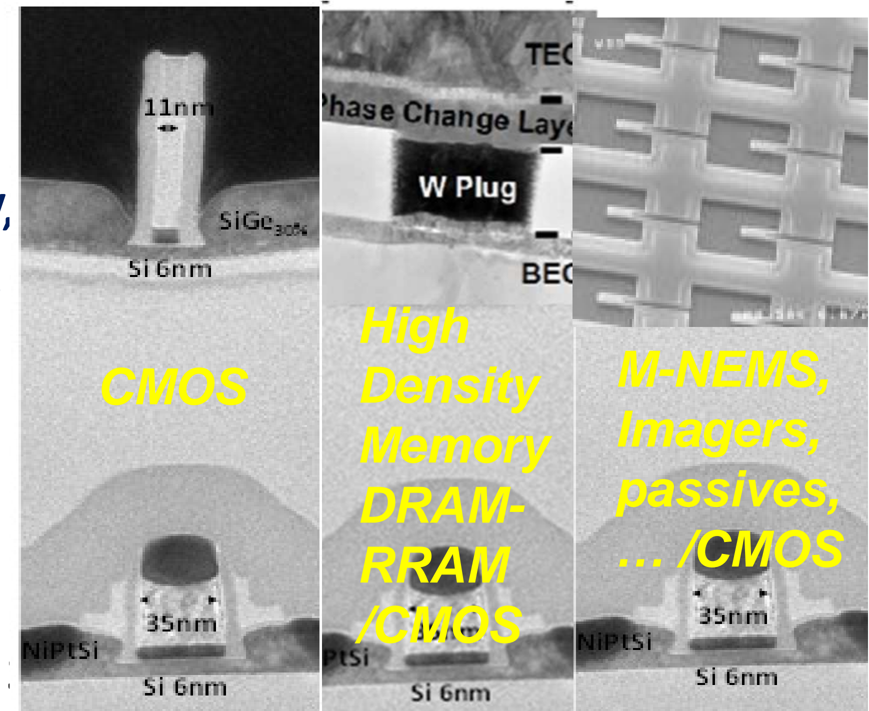


Neuromorphic Architectures



3D sequential process: Highly Performing Heterogeneous Co-Integration





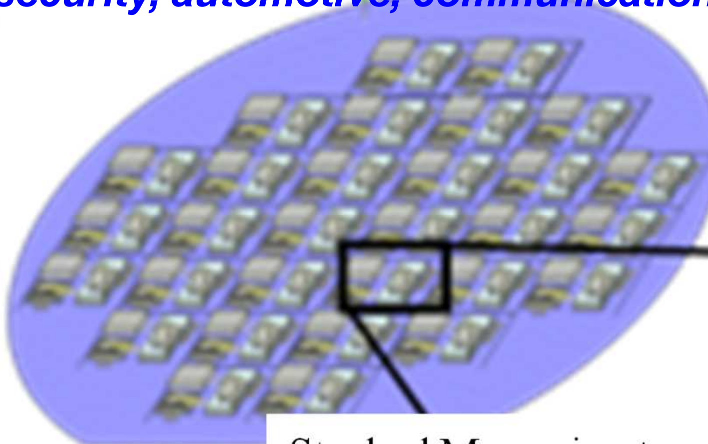
-Cold end process(bonding) & Low Thermal Budget (SPER, Laser anneal): 2nd tier 525°C
-Opportunities for other SC(Ge and alloys, III-V, C 1D,2D, 3D, ...)
-Layout Improvement by partitioning: 1 node/stacked layer, X100 via density/packaging
- High density Embedded intelligence(sensors, actuators,…): mixing CMOS, High Density Memories, Nano-objects(wires and NEMS) and Nanomaterials
- Alternative Computing paradigms from «in-memory-immersed» to massively parallel Quantum Computing, Neuromorphic Computing,…

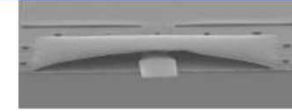
=> increasing bandwith and energy efficiency - up to x1000

P.Batude et al., IEDM 2009, IEDM 2011 Invited ; VLSI Tech Symp 2011, 2014 , VLSI-TSA 2013;
VLSI Tech Symp 2015 Invited ; IEDM 2017 Invited ;
C.Fenouillet-Beranger et al. IEDM 2014; I. Ouerghi et al., MEMS 2016 IEDM 2015;
S. Deleonibus et al., IEDM 2014 Invited ; Shulaker et al., IEDM 2014 ; Aly et al., Rebooting computing, 2015 ;
Veldhorst et al. , arXiv:1609.09700v, 2016 ;

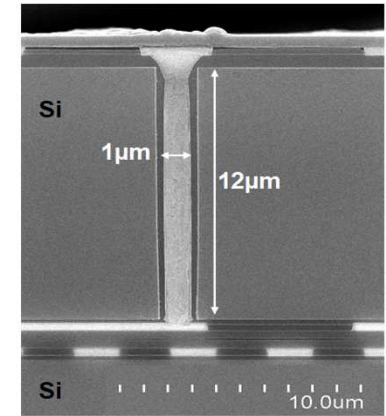
System On Wafer: Heterogeneous co-Integrated Systems
Parallel 3D : towards Zero Power from grid Systems

Extendable/multiple sectors: ***healthcare, security, automotive, communication, energy,…***

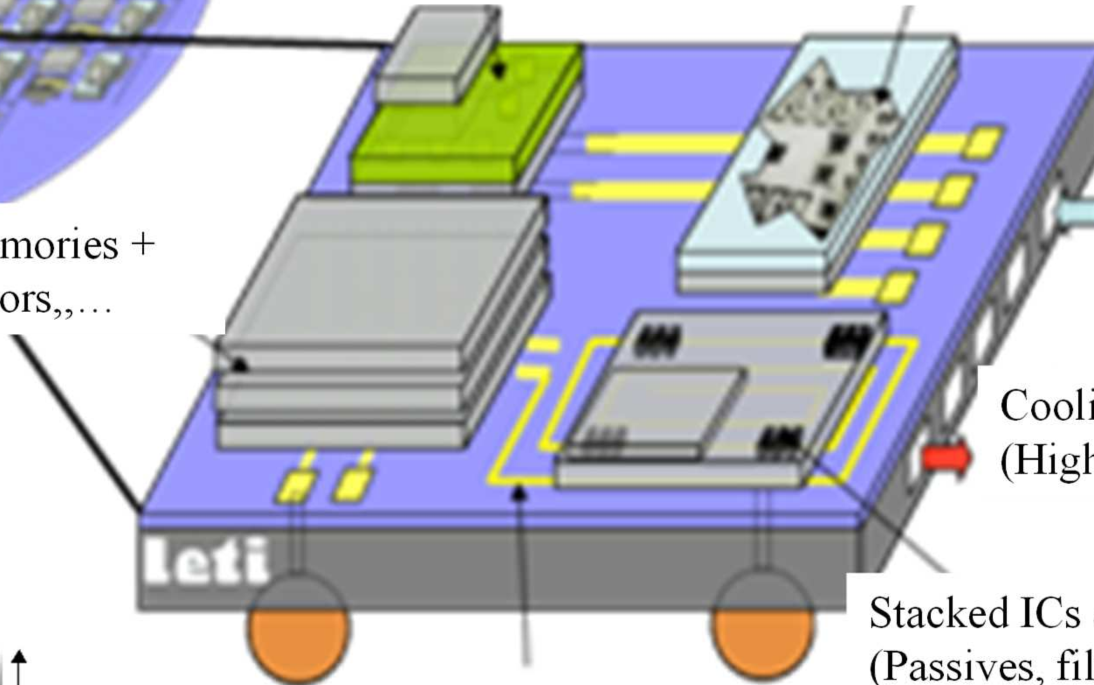


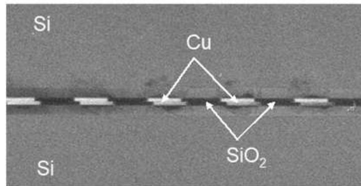


Wafer level packaged MEMS

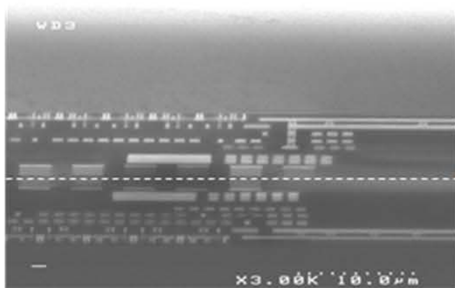


High AR TSV stacked ICs



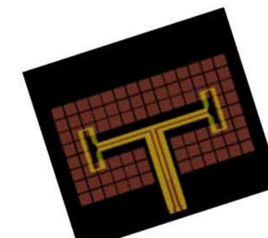


Copper/Copper bonding



Oxide/Oxide bonding

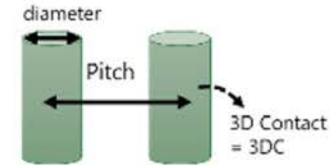
Packaging(thin films) : 3D wafer level



Interposer: Si, polymer,…

S. Deleonibus et al., Invited talk, IEDM 2014

3D Fine Pitch connections landscape

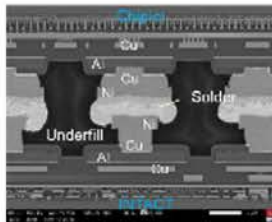


3D Contact density

TSV Mid + Micro bumps [1]:
Pitch 10-200µm

10^3 3DC/mm^2
➔ Entire Core

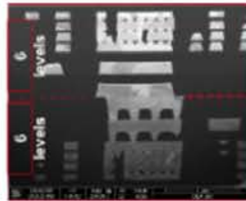
Active interposer



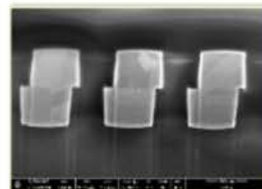
Pitch 20µm

TSV HD + Cu/Cu [2]:
Pitch 1-10µm

10^5 3DC/mm^2
➔ Logic blocs
➔ Logic gates



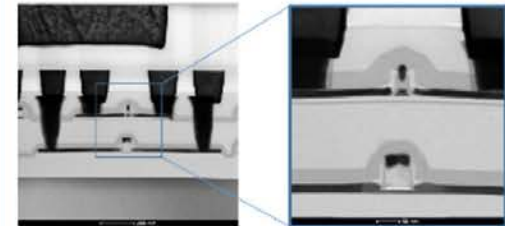
Pitch 6µm



Pitch 1µm

M3D (CoolCube™) [3]:
Pitch 0,05-0,1µm

10^8 3DC/mm^2
➔ Transistor level



[1] P.Coudrain et al., "Active interposer technology for chiplet-based advanced 3D system architectures", ECTC 2019.
[2] A. Jouve et al., « 1µm Pitch Direct hybrid bonding with <300nm Wafer-to-Wafer overlay accuracy", Proceeding of S3S conference, Oct. 2017, San Francisco
[3] P.Batude et al. « 3DVLSI with CoolCube process: An alternative path to scaling », VLSI technology symposium, 2015

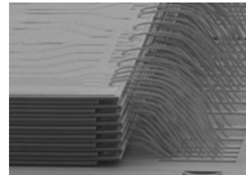
Tomorrow driving embedded sensing applications ? Autonomous & Heterogeneous co-integration:

Moore

3D "play ground"

Towards «Zero Power» from the grid systems

90nm



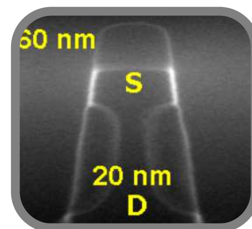
3D die stacking

65nm
Strained

45nm
High-k

3D circuit

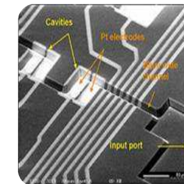
32nm



22nm
3D Tr

3D transistor

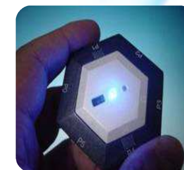
Adapted from Kwon et al, 2007 DAC



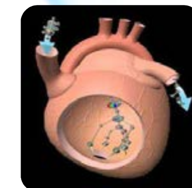
Lab on chip

RF Chip
Image Sensor
DNA Chip
MEMS
Processor
Memory
Battery

Capsule endoscope



Integrated / wearable Sensors



Medicine nano-robot

Implantable/BioCompatible, wearable,…

Extendable/multiple sectors:
health, security, automotive, communication, energy,…

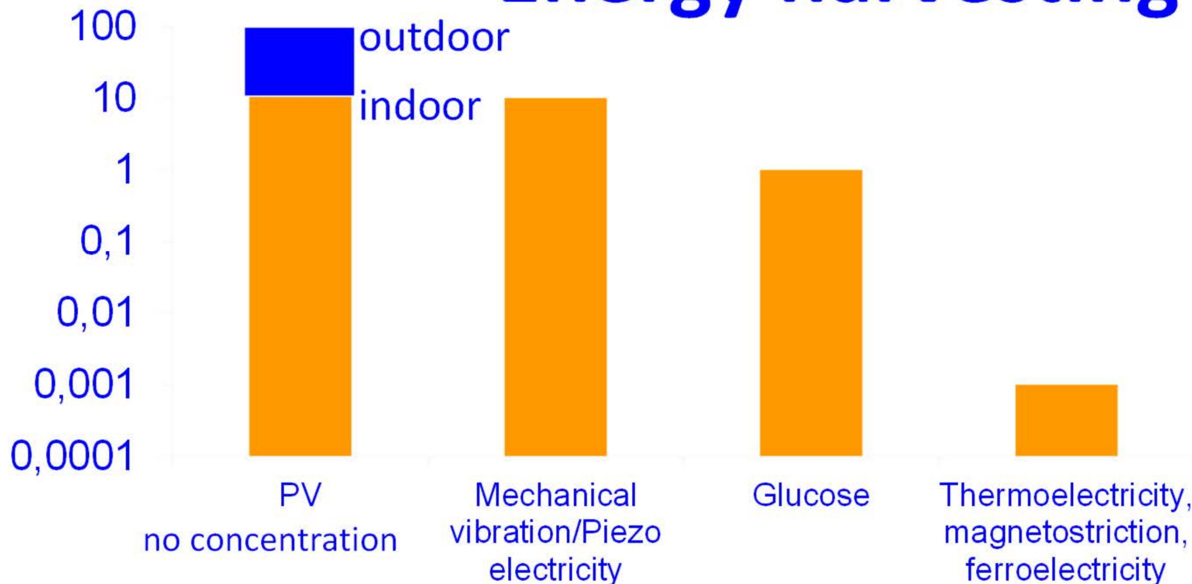
S. Deleonibus et al., Invited talk, IEDM 2014

Energy to cleverly harvest and save

Global energy balance efficiency!!

Low power sensors and actuators, data processing, communication, …
Energy Harvesting … from unwasted energy!
Energy Storage for nomadic/autonomous systems.

Micro Batteries
-co-integrated on chip
-flexible, foldable, stretchable,…
(bio compatible ceramics, polymers,…)



S. Deleonibus et al., Invited talk, IEDM 2014

implantable wearable

Conclusion : from Nanoelectronics Devices to Systems

- **Si CMOS: Nanoelectronics Base platform beyond ITRS hosting novel process modules and add-ons towards Diversification:**

3D at the device(GAA), steep slopes (TFET) and functional level to lower power consumption (towards sub 0.5V VDD) and to increase integration

Opportunitiers for different materials(Ge, SiGe, C-based , III-V, 2D) on Si

(bonding, deposition, epi): cold end processing/above IC & sequential 3D integration

Major interest for sub 5 nm and add-on materials: Zero Intrinsic Variability

Device and System Architecture revisions: Memory /Logic hierarchy and intermixing (latency & power management, Neuromorphic architectures,…), Quantum Computing, Adiabatic Computing,…

- **Heterogeneous 3D co-Integration on Si.**
  Towards Zero Power from a grid Nomadic/Autonomous Systems:

Add Functionalities for diversification. NonCMOS & CMOS

Bio compatibility (gases, liquids)

3D partitioning : sub system or System On Wafer

Energy Harvesting, Storage and Management.

«Multiphysics», New Progress Laws & New Models,

Training & Education

- **Cramming More Integrated Sustainable Functions (MISF) on Chip:**
  Low Power solutions for healthcare, environment, quality of life, IST,…

Merci de votre attention

Thank you for your attention

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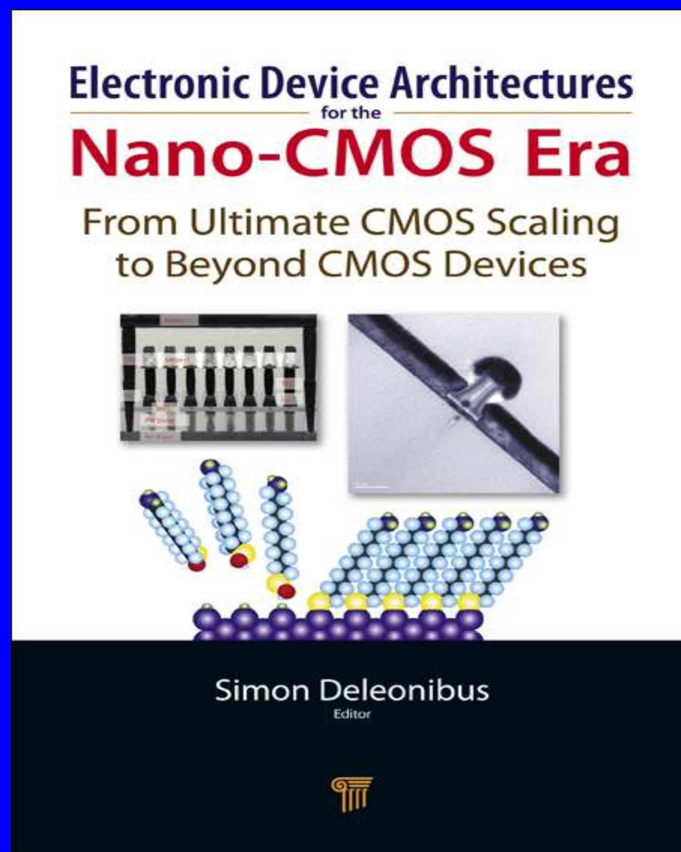
IEEE EDS MQ/DL Program, IEEE SCV/SF Jt. Section Chapter, ED15 Joint Chapter

Luu Nguyen (PsiQuantum)



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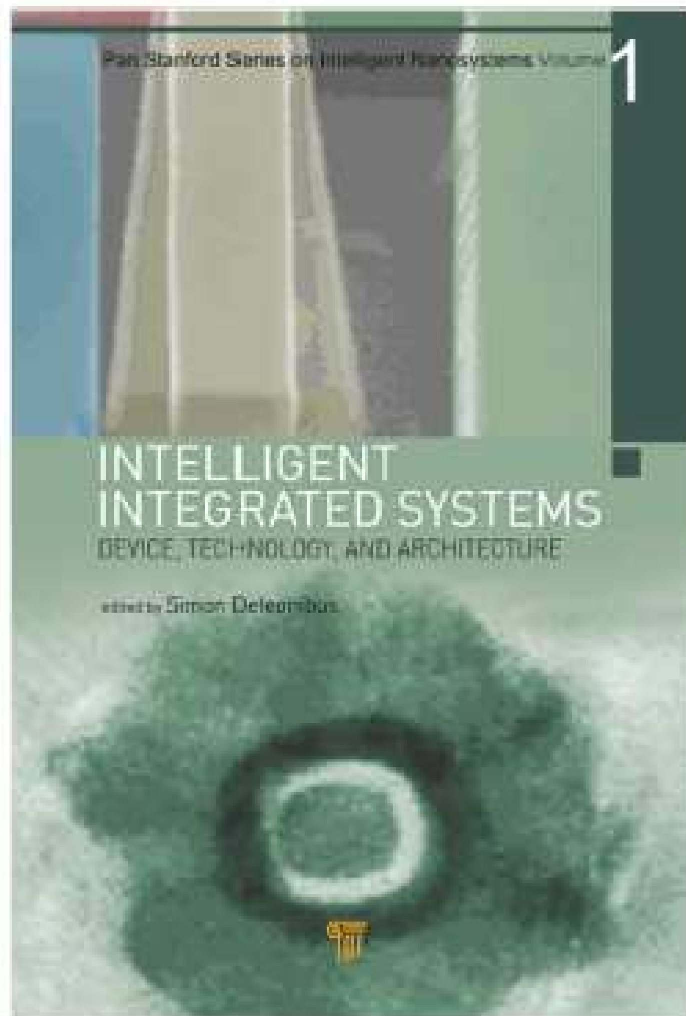

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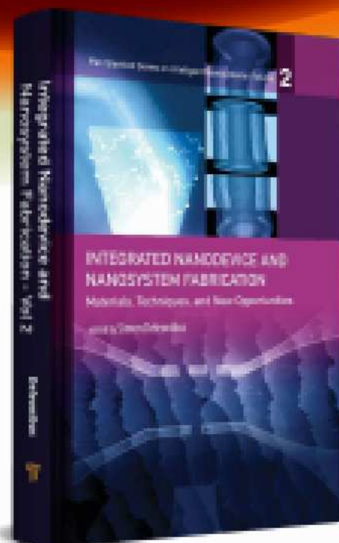
Materials, Techniques, and New Opportunities



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Since its invention, the integrated circuit has necessitated new process modules and numerous architectural changes to improve application performances, power consumption, and cost reduction. Silicon CMOS is now well established to offer the integration of several tens of billions of devices on a chip or in a system. At present, there are important challenges in the introduction of heterogeneous co-integration of materials and devices with the silicon CMOS 2D- and 3D-based platforms. New fabrication techniques allowing strong energy and variability efficiency come in as possible players to improve the various figures of merit of fabrication technology.

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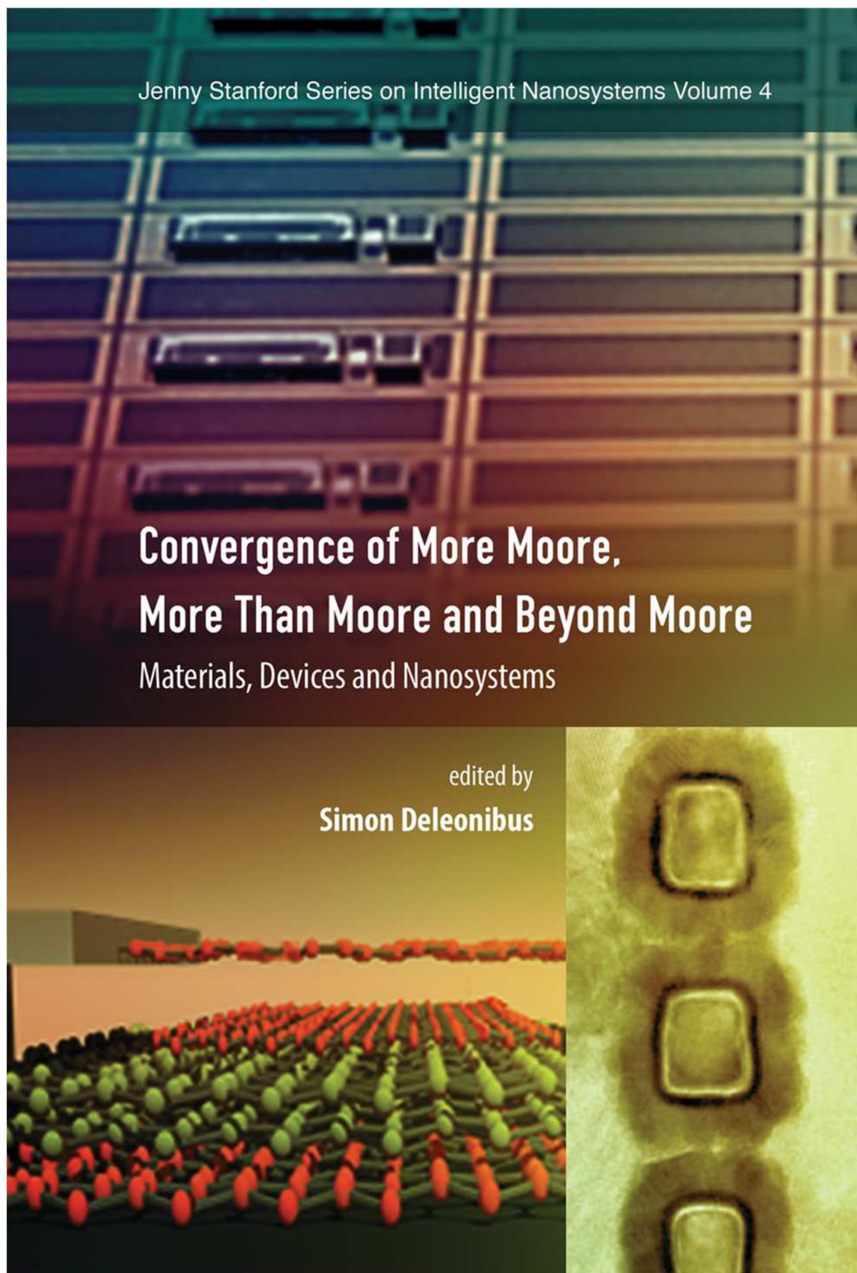

"This book rightly acknowledges that More Moore, More than Moore and Beyond Moore are temporary if not artificial partitions. The three cannot displace nor substitute one another. Denser integration, new devices and additional materials complement each other and emerge..."

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"...new heterogeneous integration technologies based on all aspects of materials, devices, and nanosystems are indispensable in the era of sustainable and energy efficient nanoelectronics and nanosystems. This book provides many useful information and insights to prospect the future technological revolution."
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The Energy and Variability Efficient Era (E.V.E.) is Ahead of Us

SIMON DELEONIBUS (Fellow, IEEE)

Université Grenoble Alpes, Commissariat à l'Energie Atomique et aux Energies Alternatives, Laboratoire d'Electronique et des Technologies de l'Information, Grenoble 38054, France

CORRESPONDING AUTHOR: S. DELEONIBUS (e-mail: simon.deleonibus.1992@ieee.org)

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ABSTRACT Major power consumption reduction will drive future design of technologies and architectures that will request less greedy devices and interconnect systems. The electronic market will be able to face an exponential growth thanks to the availability and feasibility of autonomous and mobile systems necessary