
# On-Shoring the Next Generation of Advanced Packaging

*February 17, 2022*

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# Agenda

- SkyWater History & Background
- Chiplets - 3D Heterogeneous Integration
- SkyWater AP Offerings
  - Si-Interposers
  - Hybrid Bonding Interconnect
  - Wafer Level and Fan-Out Packaging
  - Solder bumping & Assembly
- Roadmap
- Summary

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# We streamline the **concept to market journey** for micro- and nanotechnologists.

**Technology as a Service (TaaS)**

**Innovation as a Service** + **Manufacturing as a Service**


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# We are the only **U.S.-owned** pure-play foundry.

## Extending a legacy of manufacturing excellence to meet the industry's needs in a **post-Moore's Law reality**


Cypress

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**2005** — 65 nm qualified

**2008** — Technology foundry opens to non-Cypress customers

**2017** — SkyWater received DMEA Cat 1A Trusted Accreditation

**2018** — SkyWater and MIT selected for DARPA 3DSoC program

**2019** — $170 M rad-hard technology and building expansion announced

**2020** — 3-year anniversary of SkyWater completion of Cypress ToP contract

**2021** — Florida Advanced Packaging Facility integrated into operation

**2021** — $112M IPO closed April 2021

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# SkyWater **Minnesota**

Bloomington, MN


# SkyWater **Florida**

Kissimmee, FL

## OPERATION

200 mm equipment
91,000 $ft^2$ Cleanroom
Class 10 + SMIF
10,000 30 ML CMOS wafers or 50,000 MOSFET wafers per month
90 nm+ feature geometries

## CERTIFIED

ISO9001 / IATF16949 Automotive Certified
ISO13485 Medical Certified
ISO14001 Environmental Certified
DMEA Cat 1A Trusted
ITAR and Secure Processing Supported

## OPERATION

200 mm equipment
Size: 109,000 $ft^2$ total
- 26,000 $ft^2$ of class 1000
- 9,400 $ft^2$ of class 10,000

## NOTES

Site added to operation Feb 2021
*DMEA Cat 1A Trusted* – pending, planned late 2021
Facility will enable custom advanced packaging solutions

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# SkyWater is Defining a New Category

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**Technology Foundry**

**Advanced Technology Services + Wafer Services**

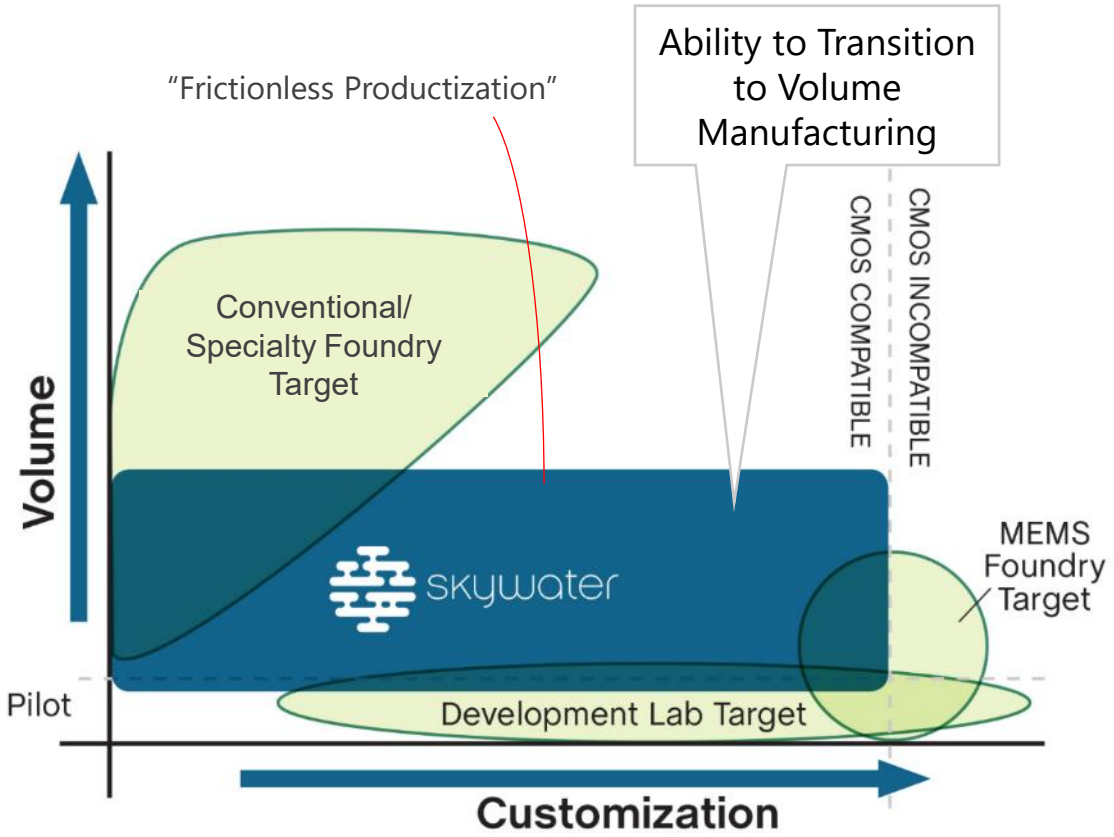
- ✓ High customization
- ✓ Next-generation technologies
- ✓ Variable volumes
- ✓ 200 mm substrates

**Specialty Foundry**

- Moderate customization
- Specialty technologies
- Medium volumes
- 200 mm and 300 mm substrates

**Conventional Foundry**

- Minimal customization
- Digital processors, CPUs, GPUs
- High volumes
- 300 mm substrates

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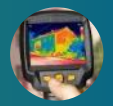
# Partnership Pathways: Prototype to Production

| | Research | | Commercialization | |
|---|---|---|---|---|
| | **Advanced Technology Services (ATS)** | | **Qualification** | **Wafer Services** |
| **Primary Activity** | **R&d**:<br>Proof of Concept<br>Tech Demonstration<br>Process Development | | **r&D**:<br>Maturing & Qualifying Capabilities, Process Flows, and Products for Scale | ~~r&d~~:<br>Mfg. Volume Production |
| **Technology Readiness & Manufacturing Readiness** | TRL / MRL: 3~6 | | TRL / MRL: 6~8 | TRL / MRL: 8~9 |
| **Operating & Business Model** | • NRE<br>• Tooling | | • MPW<br>• NRE<br>• Tooling<br>• Early Access Program<br>• Flow Transfer | • 1x Setup<br>• Per Wafer |
| **Example Start Points** |  3DSoC |  90nm Rad-Hard |  MEMS |  Photonics |  Mixed-Signal |  Power Discrete |

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# How Does an ATS Project Work?

## Why A Technology Foundry?

| | |
|---|---|
| Efficient Development | **Agility** for unique processing flows |
| | **Fast** progress at speed of production |
| | **DEM** from the start |
| Rapid Scale-Up | **No additional IP sharing** |
| | **No New Relationships** |
| | **No Transfer Time** |
| Production | Automotive **Quality** |
| | Heritage of **Operational Excellence** |
| | **Right-Size Fab Services** |

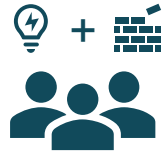
### It Starts with YOUR Idea

### Initial Consultation

- Understand the device performance objective
- Review device architecture concepts
- Jointly brainstorm possibilities
- Identify end goal

### Detailed Project Scoping & Setup

- Align on project objectives
- Align team resources with timeline requirements
- Establish interface requirements
- Establish business terms
- Choose fixed-price or consumption model
- Identify tool hosting needs



### Co-Create Your Ideas

- Customer and SkyWater team execute development work
- Continuous learning and idea generation
- Data exchange per customer requirements
- Quarterly reviews
- Customer defined milestones

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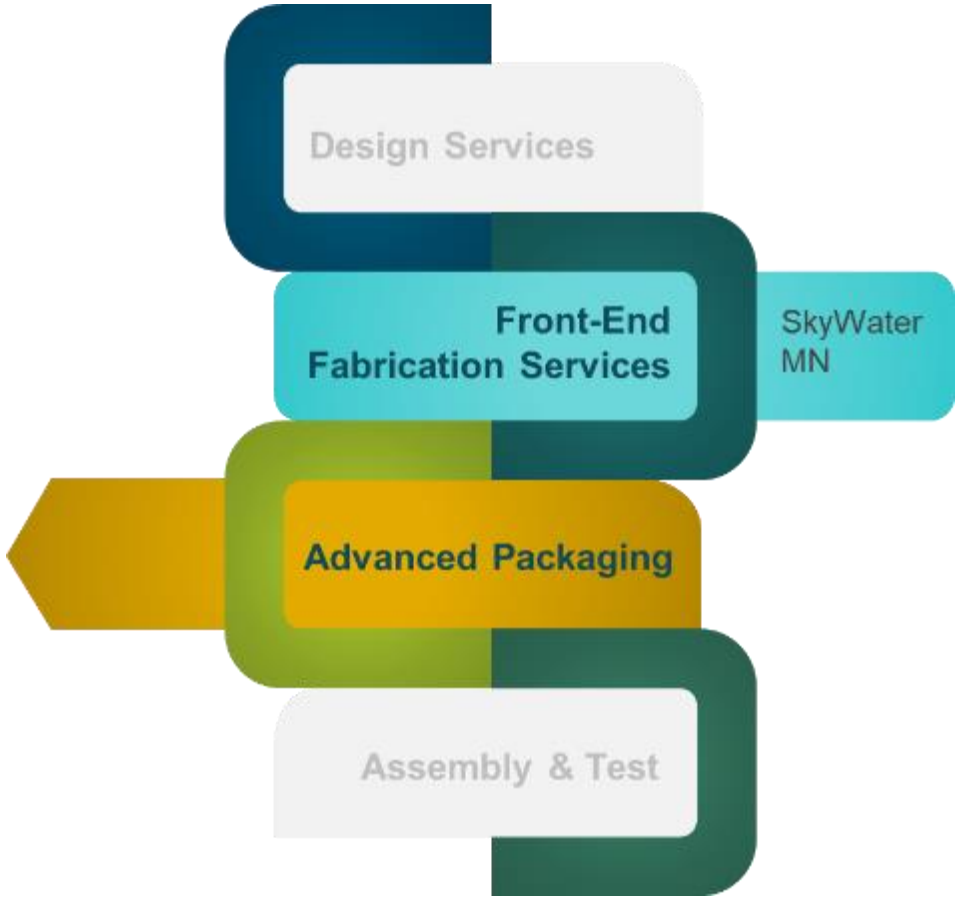
# Capabilities for Advanced Integrations

**Silicon Interposers w/TSV**

**Hybrid Bonding**

**Wafer Level and Fan-Out Packaging**

**Solder Bumping & Assembly**

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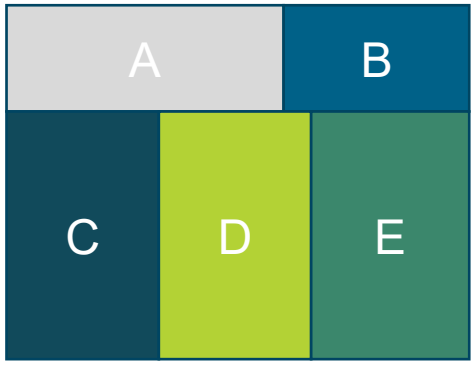
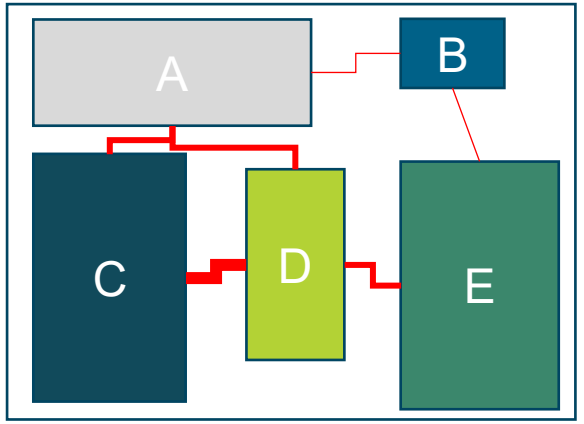
# Drivers for Chiplet Integration

SOC




End of Cost Advantage of Moore's Law

Shared Package




- Difficult
- Very Costly
- Low Initial Die Yield

**Pros**

- **SWAP**
- Flexibility
- Optimized Performance
- Lower Power
- Shorten Time-to-Market
- Gordon Moore predicted that eventually one would go to packaging individual chips – Original paper.
- Thermal optimization
- Spin multiple products faster

**Cons**

- **Create System Integration Ecosystem (Supply Chain and Business).**
- KGD – Known Good Die
- Establish a pull by customers
- Standards
- Software Design Tools
- Yield Loss Ownership

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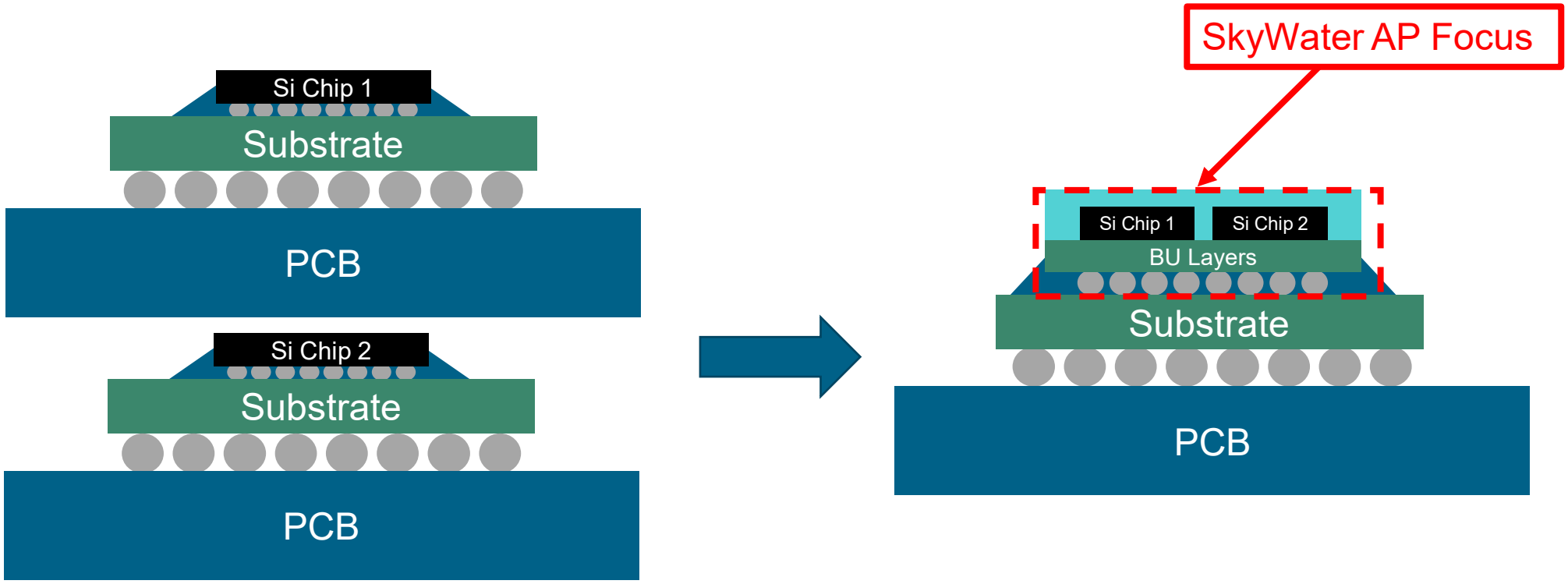
# Pathway to 3D Integration (Fan-Out)




Conventional
Flip Chip Attach

Fan-Out Chip on Substrate

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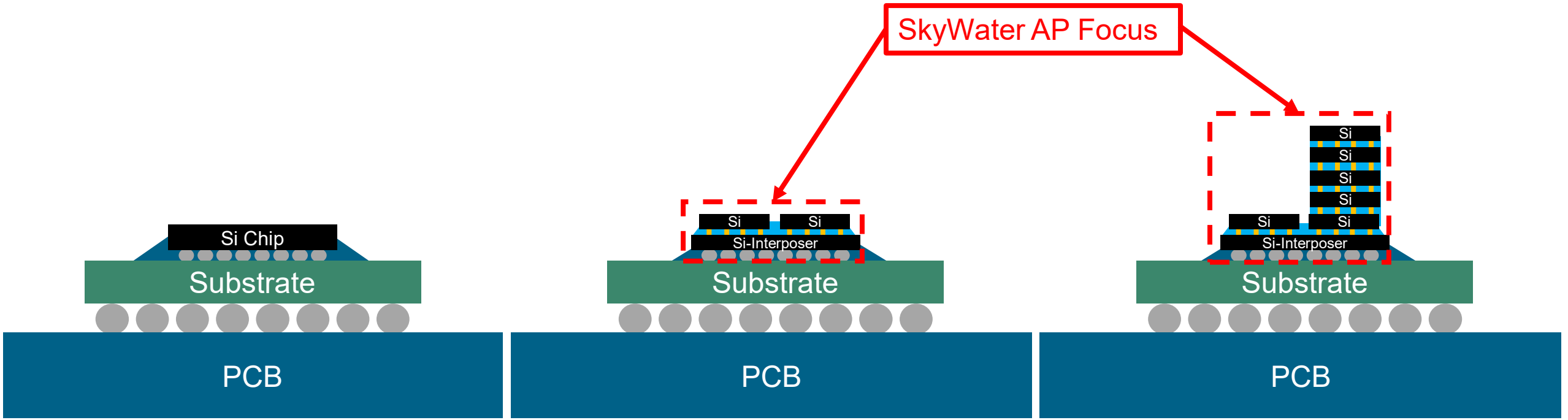
# Pathway to 3D Integration (Interposer)




Conventional
Flip Chip Attach

2D Interposer Integration

3D IC Integration

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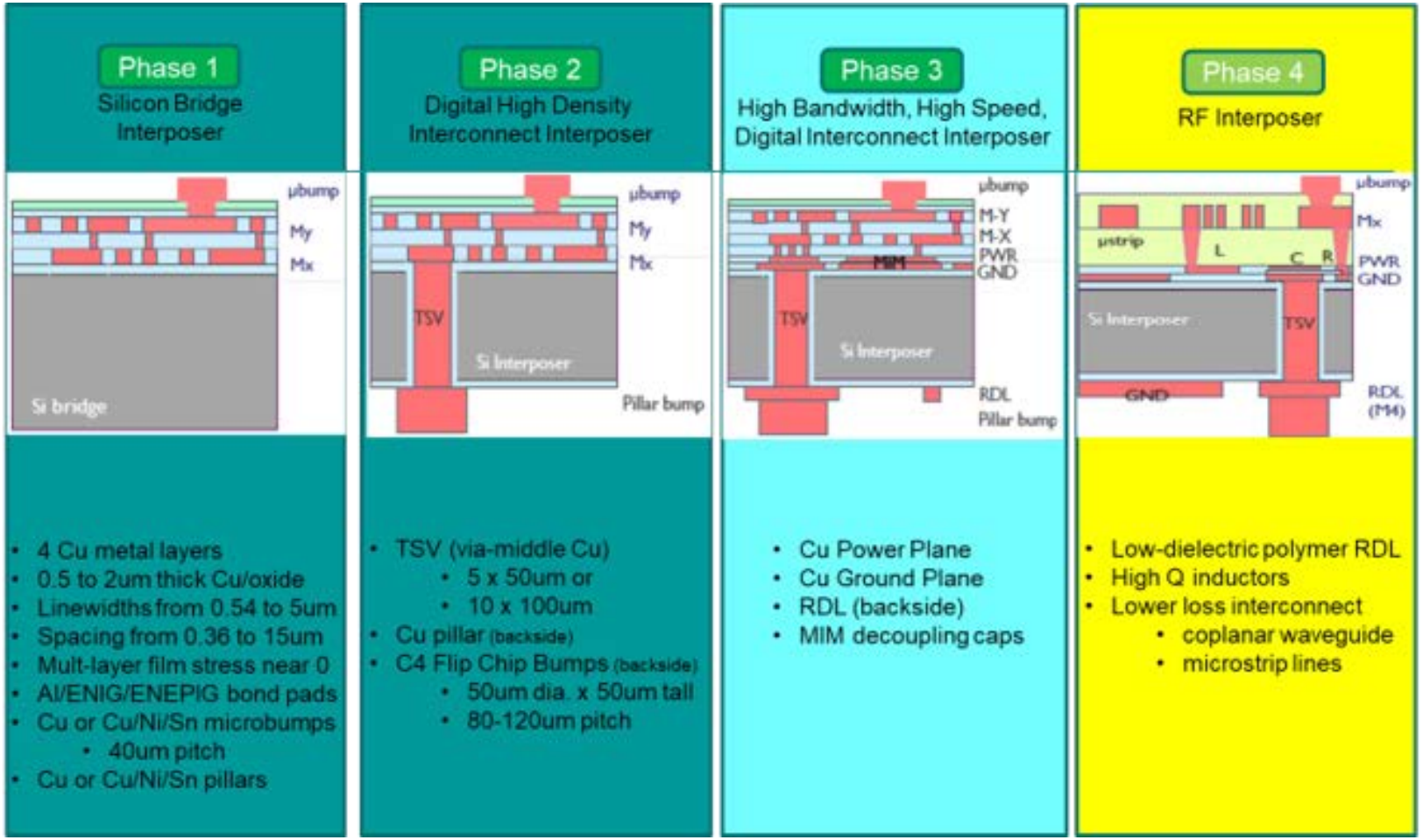
# Partnership with BRIDG to Develop Si-Interposers

## Heterogeneous Integration & Advanced Packaging

Establishes a domestic silicon interposer capability for the industrial base




*BRIDG Industrial Base Analysis and Sustainment (IBAS) Program

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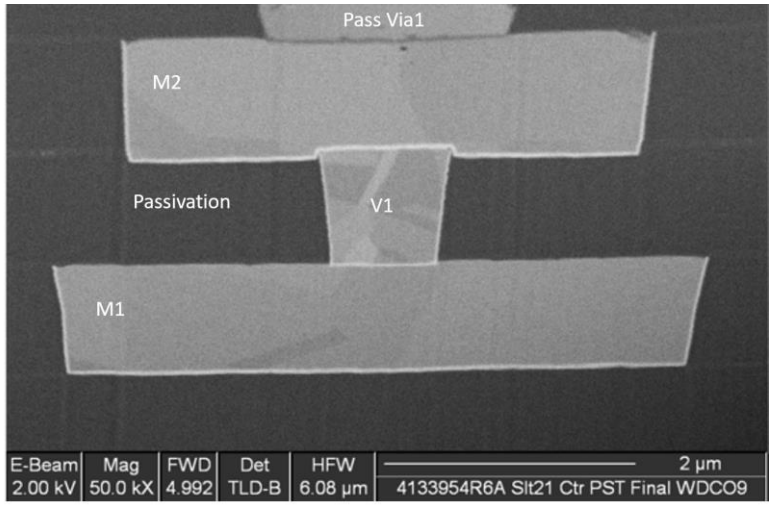
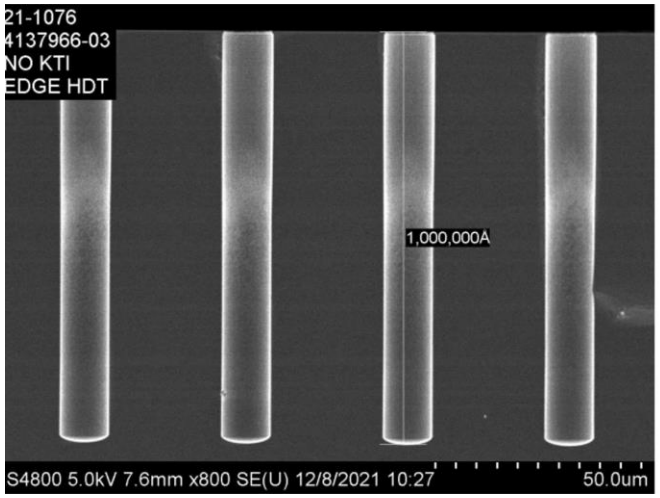
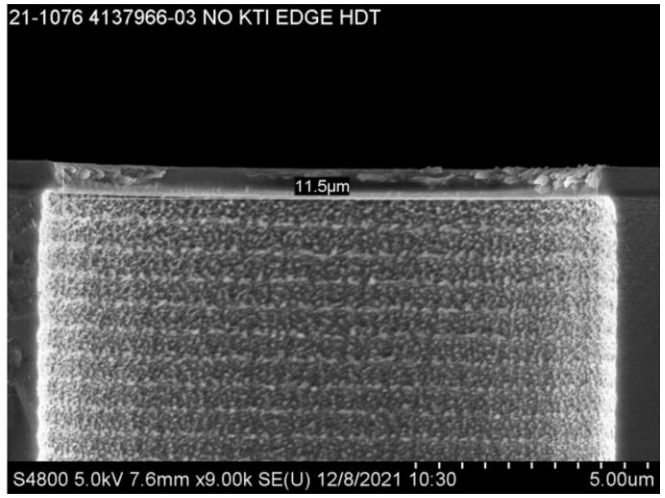
# SkyWater Si-Interposer



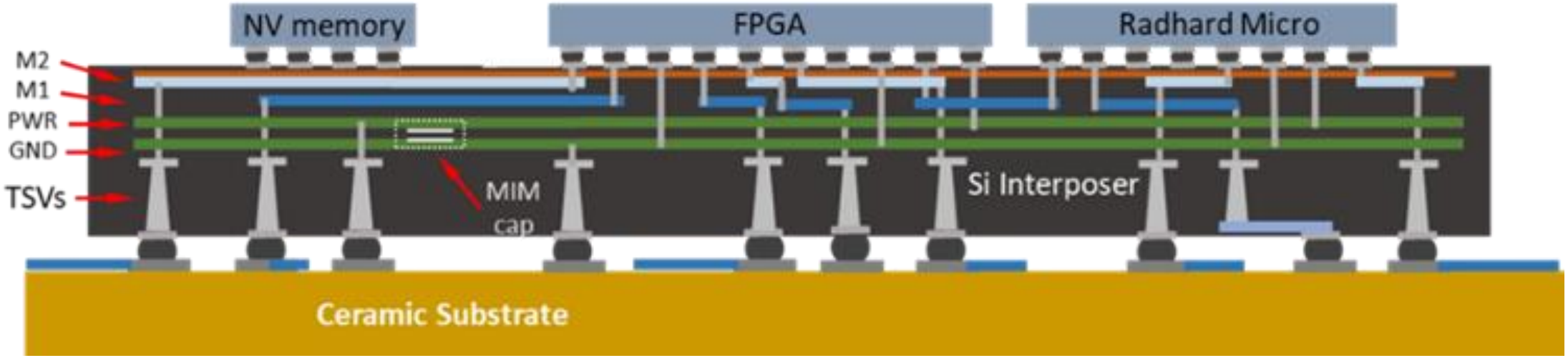

Phase I: Metallization buildup layers.




Phase 2: Via formation

# Si-Interposer Assembly – BRIDG & SWFL




Schematic Courtesy of BRIDG

- Build Si-Interposer at SWFL.
- BRIDG and SWFL work with domestic supplier on first phase of assembly development. Goal is to have capability at SWFL.
- Generate reliability test data with Navy Crane.

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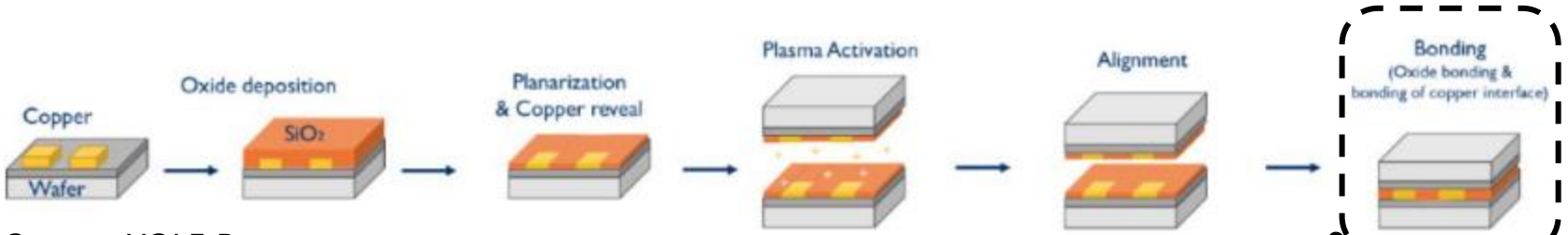
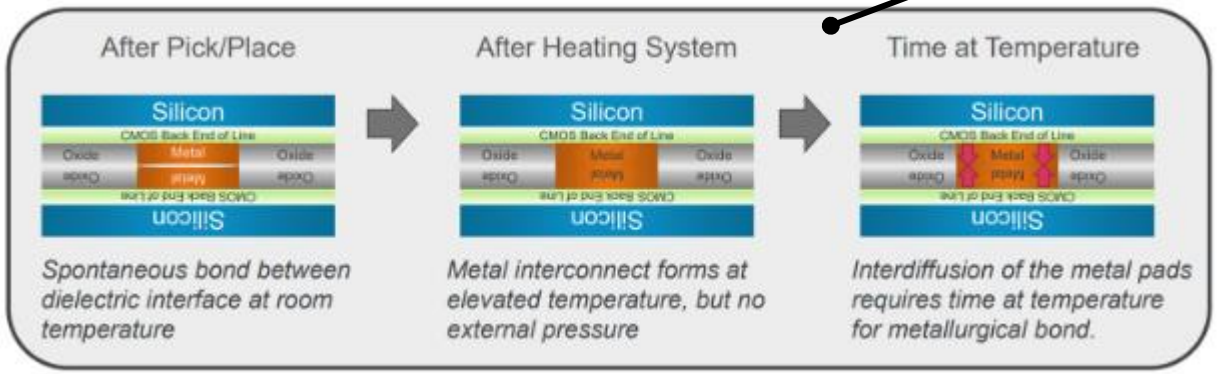
# Hybrid Bonding Interconnect Formation

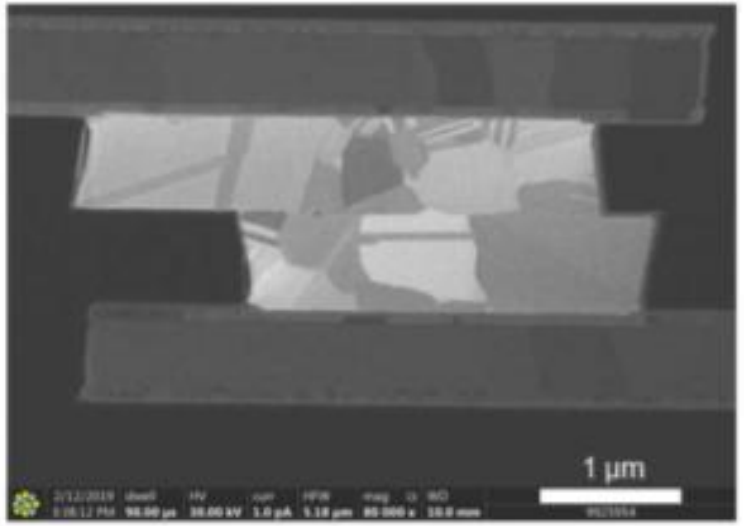
- Dielectric bonding at room temperature
- Metal interconnect formation at elevated temperature
- Thermal annealing of metal pads




Source: YOLE Report




Source: Xperi




Source: J Mudrick, et.al., MESA, Sandia National Laboratories

*FIB-SEM images of metal pads after thermal annealing*

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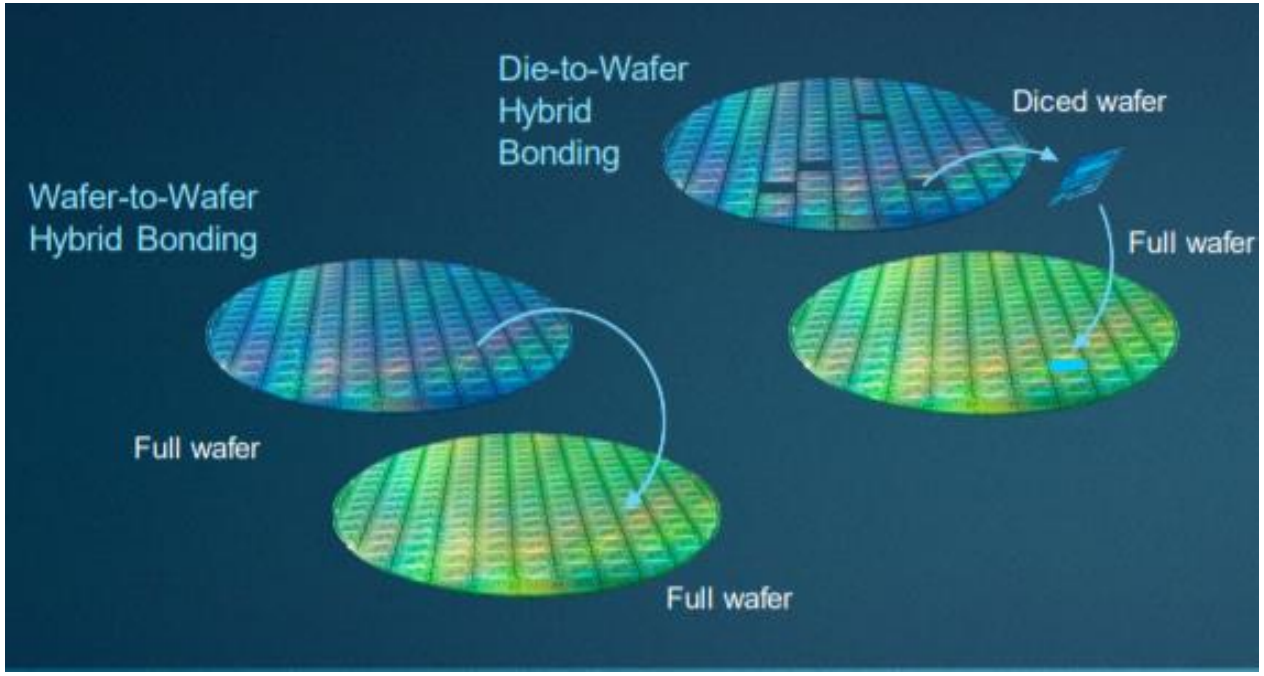
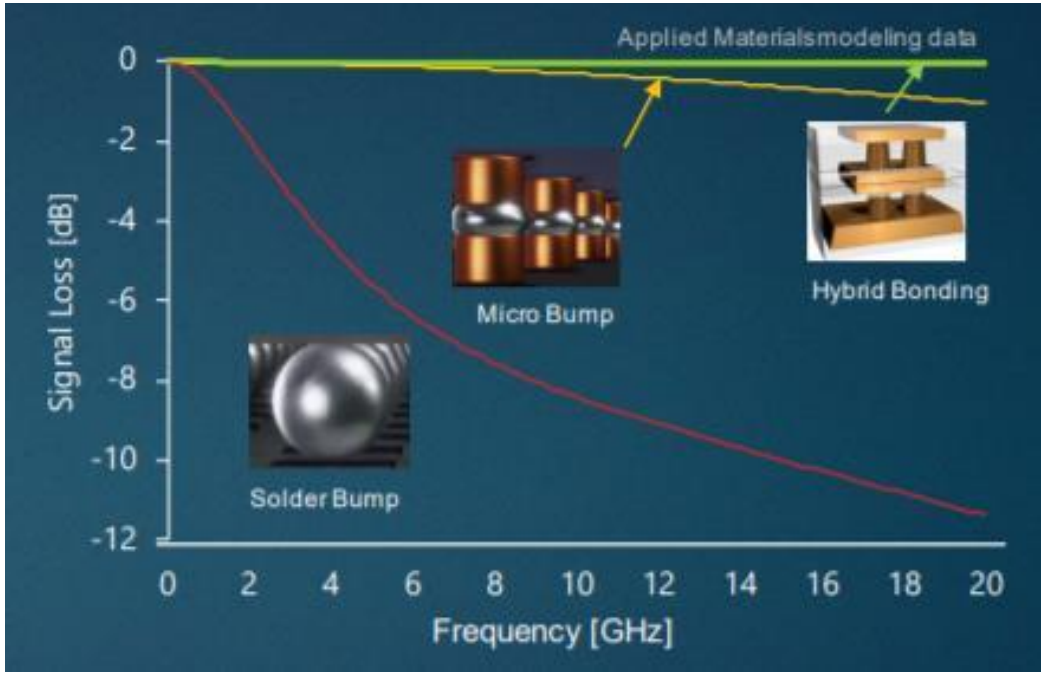
# Hybrid Bonding Interconnect

- Shortest connections with face-to-face chip bonding
- Outstanding performance compared to solder and micro-bumps




Source: Applied Materials, 2021 ICAPS and Packaging Master Class

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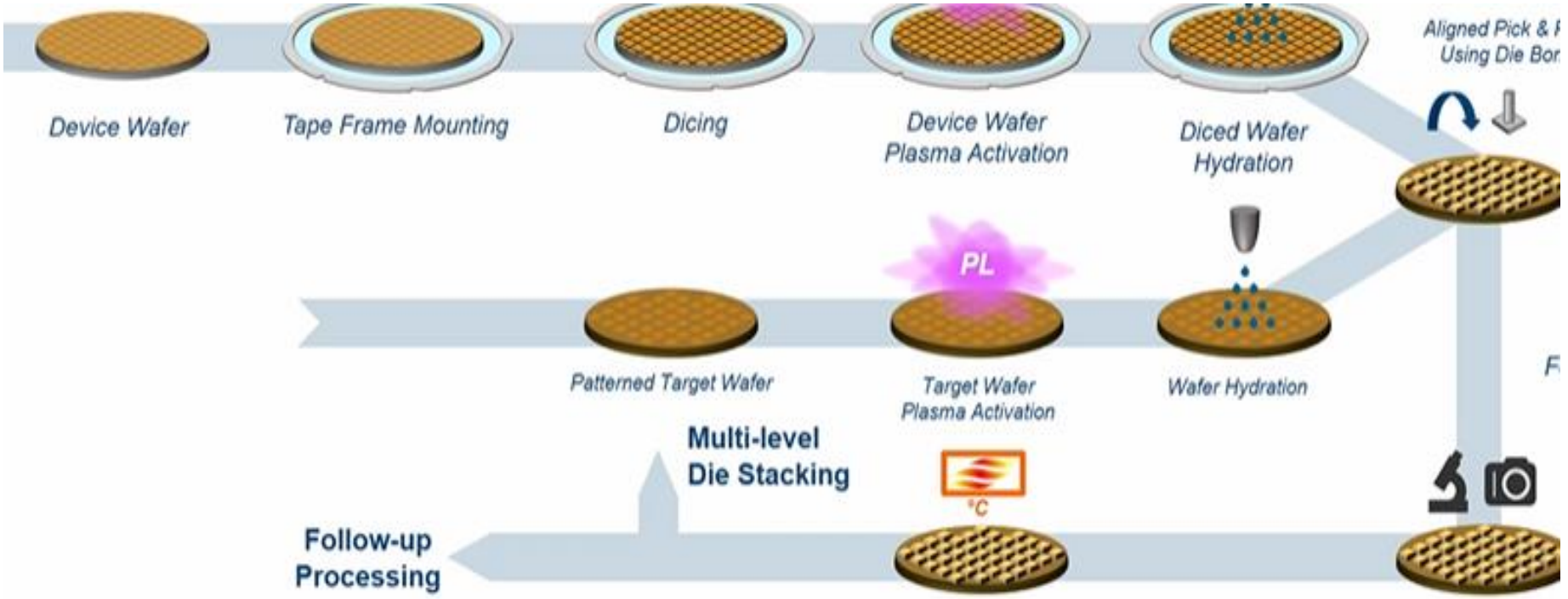
# Hybrid Bonding Die to Wafer (D2W) process flow and equipment

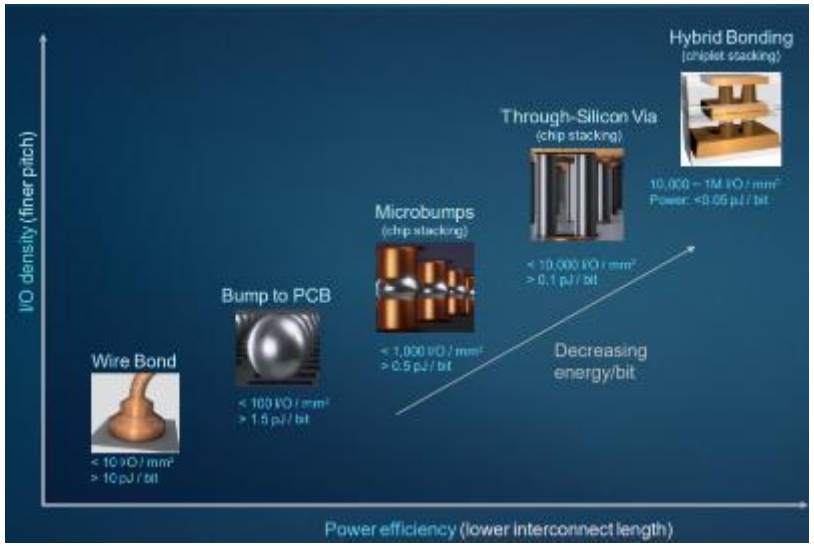



Source: SUSS

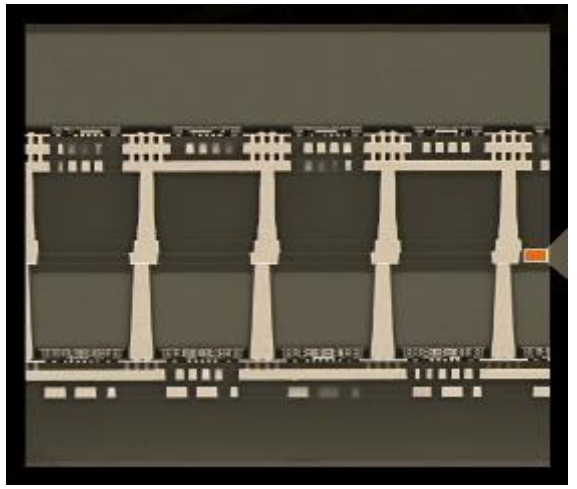
# Hybrid Bonding Die to Wafer (D2W)

- Advanced micro bumps and pillars are structures with a 40-um pitch (25 um pillar). Going forward, the industry can scale bump pitch to 20 um
- The industry needs a new interconnect solution beyond bumps and pillars
- Enabling Cu/Cu Hybrid bonding to stack memory on memory or memory on logic. This process is challenging and involves complex fab-level processes
- **Hybrid bonding enables 250K to 1M interconnects per square millimeter**
- **40 um pitch micro-bumps enables ~600 interconnects per square millimeter**

*Packaging System Interconnect Scaling Roadmap*




Source: Applied Materials, 2021 ICAPS and Packaging Master Class



Source: AMD, Hot CHIPS conference 2021

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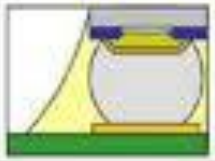
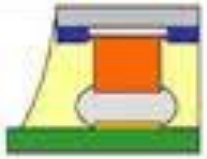
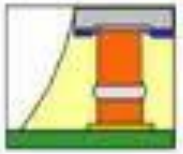
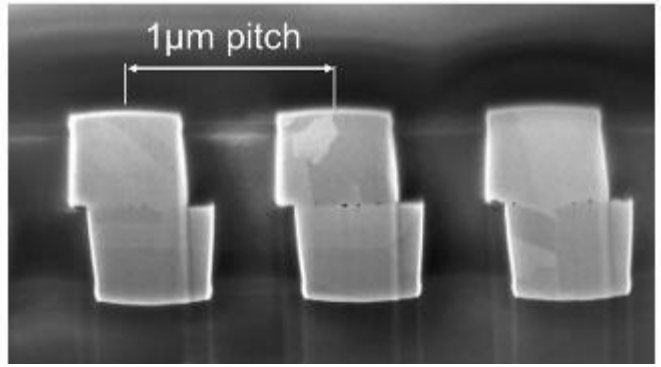
# Evolution of Bonding Methods

| Bonding Method | C4 FC (Contolled Collapse Chip Connect) | C2 FC (Chip Connect) | TC/LR (Local Reflow) FC | TC FC |
|---|---|---|---|---|
| Schematic Diagram |  |  |  |  |
| Major Bump Pitch Range at Application | > 130 um | 140 um ~ 60 um | 80 um ~ 20 um | < 30 um |


Source: AMD, Hot CHIPS conference 2021




Source: SUSS

*Hybrid Bonding Interconnect with 1 µm pitch*

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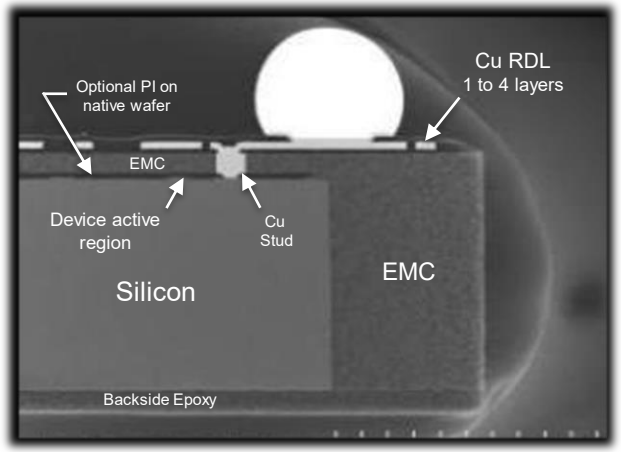
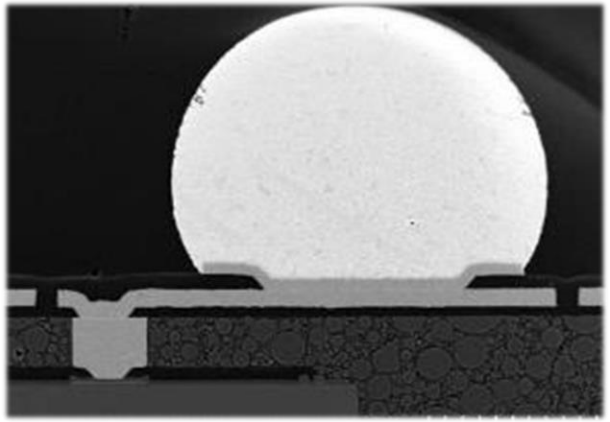
# Deca's M-Series™ Fan-Out Basics

- Chips-first, chips-up fan-out technology
- Fully encapsulated active device region (key differentiator)
- Production yields > 99.85%+ on over 3 million shipping per day
- Planar surface enables scaling to fine CDs
  - 5µm line & space in Gen 1.5
  - 2µm in Gen 2
- Adaptive Patterning® for high yield & high interface density
  - 45µm bond pad pitch in Gen 1
  - 20µm in Gen 2
  - Next closest competitors: TSMC InFO at 55µm & Intel EMIB at 45µm
- 300mm wafer format in high volume production for Gen 1
- 600mm square panel starting production in 2021 for Gen 1



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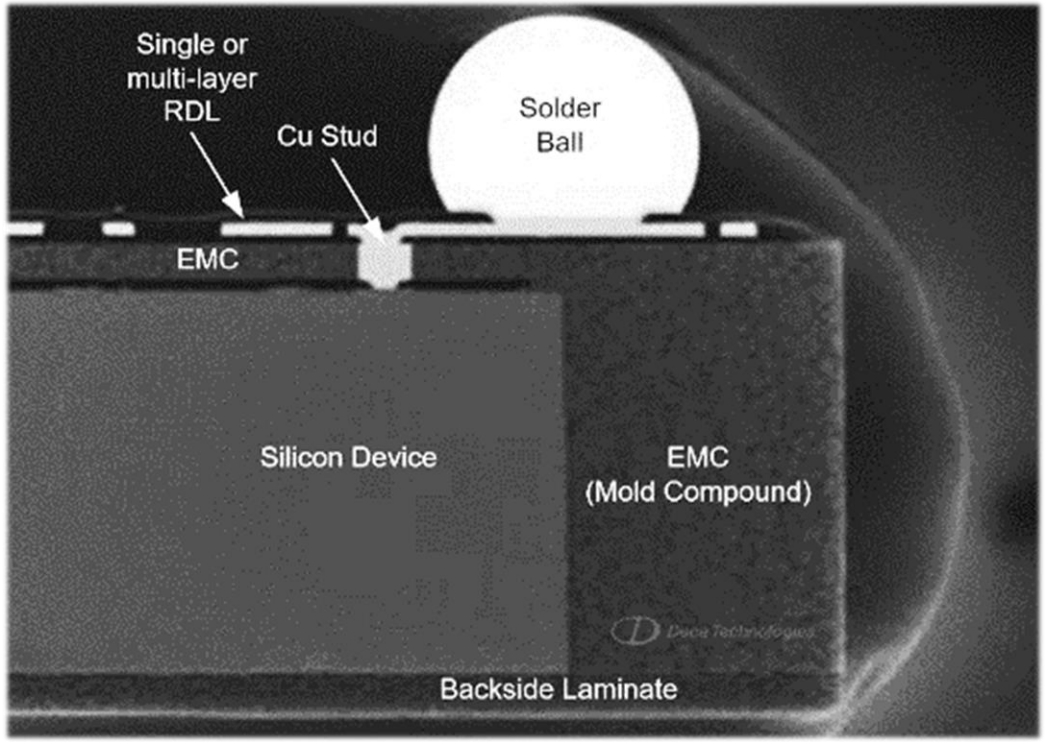
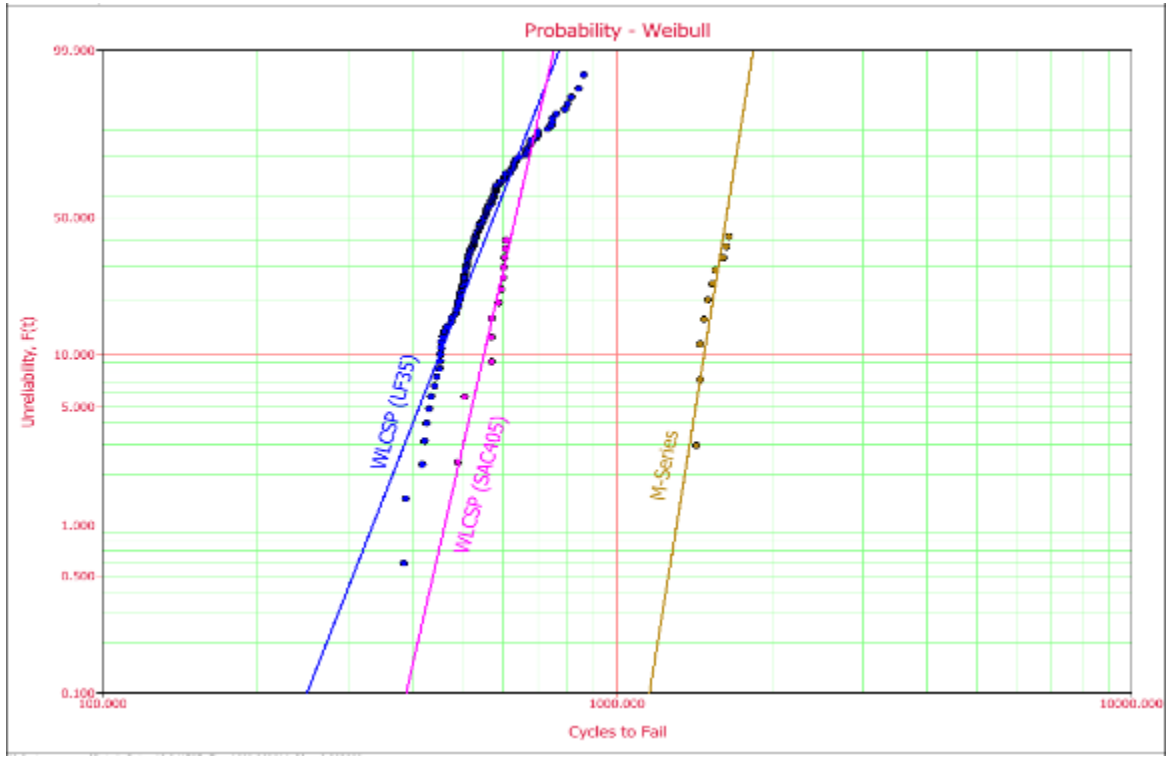
# M-Series Structure – Planarity key to 3DHI




Basic Package Construction of M-Series



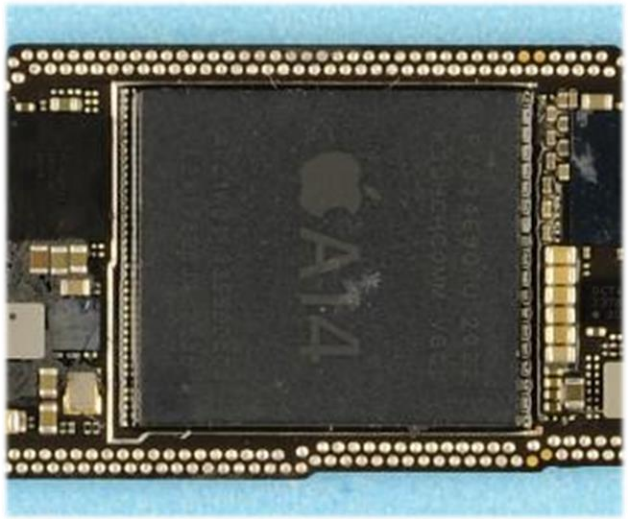

BLR Comparison of M-Series versus WLP

- Lowering of e-CBI (chip board interaction) stresses applied to device due to molded stress buffer layer between the device surface and the PCB
- Typical 200% BLR performance improvement over traditional fan-in wafer level packaging (WLP)

# Customer Adoption Examples of Fan-out

**Apple Applications Processor Device in InFO PoP**

iPhone 12 Pro Max 5G



Prismark, CUSTOM TEARDOWN ANALYSIS: APPLE A14
Report No. 6771 - January 2021

XILINX

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**New UltraScale+ Devices in InFO Packaging Enable Compact Industrial Cameras**

technologies, and while certain standards exist (e.g., interface standards like MIPI, GigE Vision, and PCI Express®), camera requirements can differ wildly.

## Zynq UltraScale+ MPSoC in InFO Packaging

Adaptive computing devices like MPSoCs offer the compute performance and flexibility often appreciated by developers of industrial cameras but have historically only been available in larger package sizes with hundreds of pins. For example, at their initial release, Zynq UltraScale+ ZU2CG/EG and ZU3CG/EG MPSoCs smallest package size was 19x19mm, a 484-pin, flip-chip, ball grid array (BGA) with 0.8mm pitch.

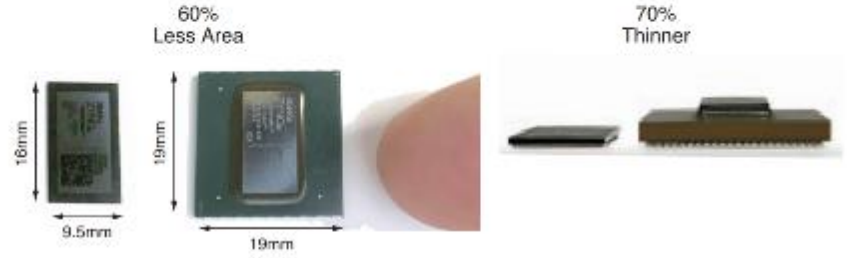


*Figure 6:* **Zynq UltraScale+ Devices in InFO Packaging**

https://www.xilinx.com/support/documentation/white_papers/wp527-info-cameras.pdf

*Significant electrical signal integrity benefits of fan-out vs. Si interposer or flip chip on substrate*

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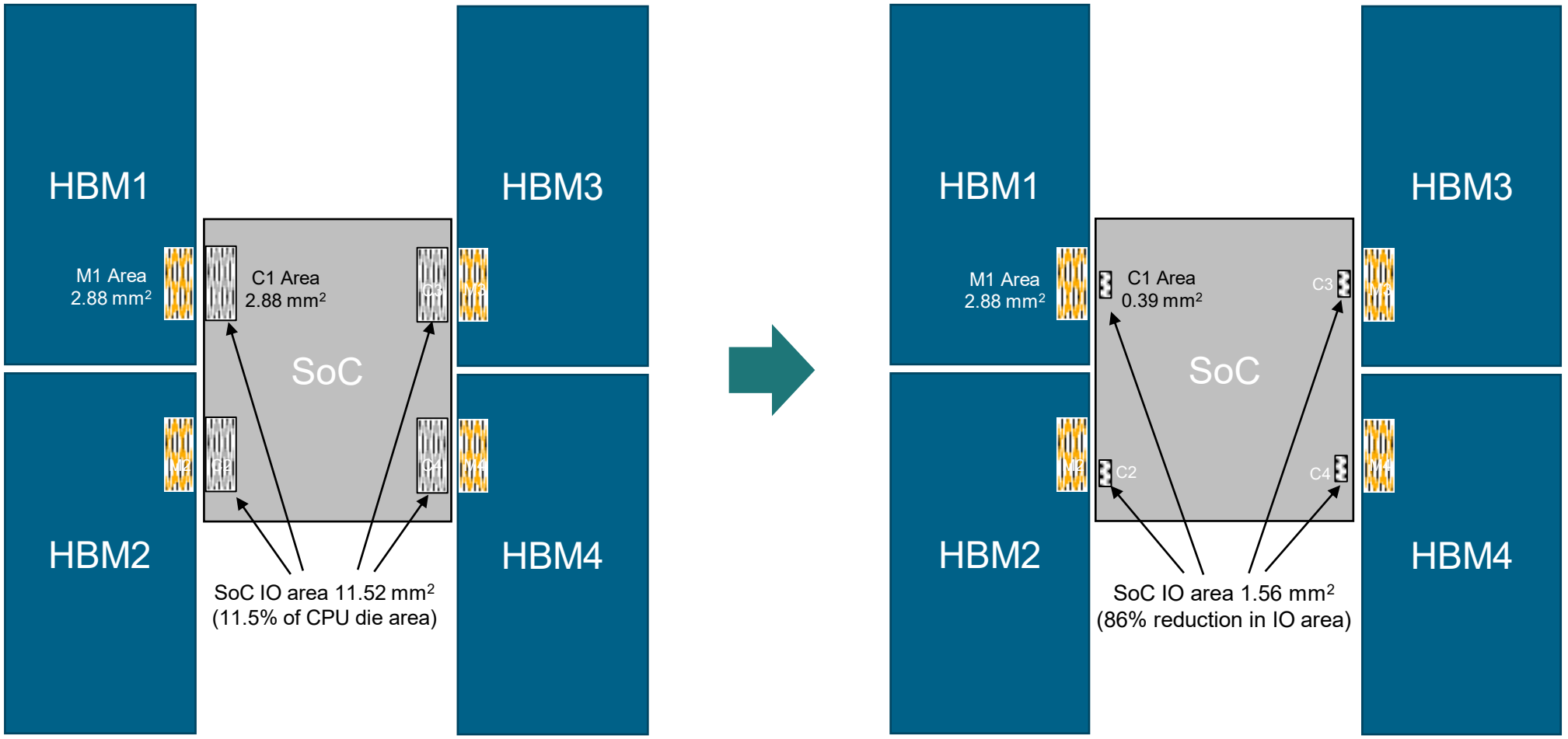
# FEOL Silicon Area Reduction From Pitch Reduction

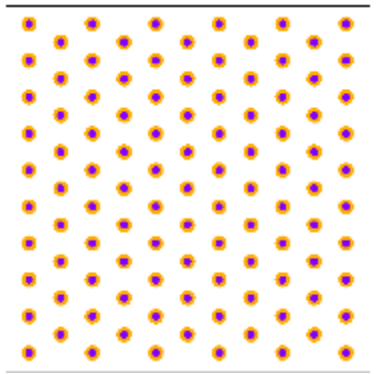
> 10% reduction in advanced silicon die size



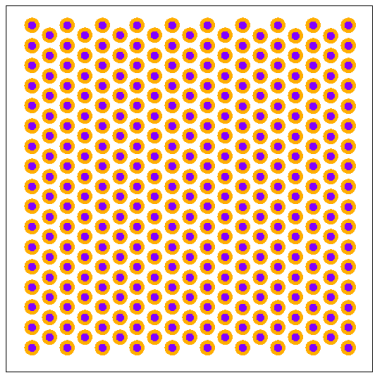
# Competitive Device Interface Pitch Density Comparison

| Cu Pillar Flip Chip | TSMC InFO | M-Series Gen 1 | EMIB | M-Series Gen 2 |
|---|---|---|---|---|
| (flip chip on substrate) | (Chips first fan-out) | (Chips first fan-out) | (Hybrid chips in substrate) | (Chips first fan-out) |

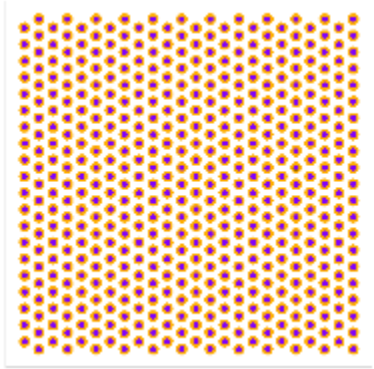
Higher density bond pad pitch



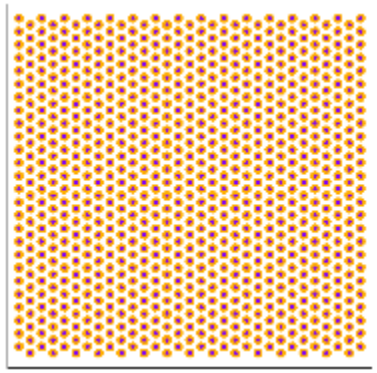
**Flip Chip Cu Pillar**
Die pad pitch: 100 µm
IO per mm$^2$: 105



**TSMC InFO**
**Die pad pitch: 55 µm**
**IO per mm2: 314**

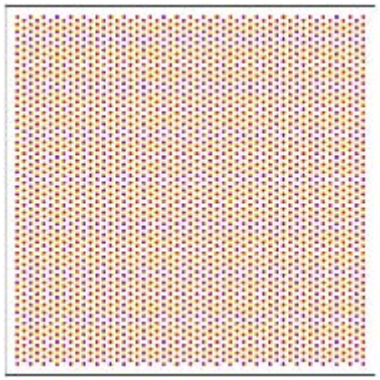


**Deca M-Series Gen 1**
**Die pad pitch: 45 µm**
**IO per mm2: 492**



**Intel EMIB**
**Die pad pitch: 45 µm (36 µm*)**
**IO per mm2: 492 (806)**

*https://www.anandtech.com/Show/Index/15980?cPage=2&all=False&sort=0&page=1&slug=intel-next-gen-10-micron-stacking-going-3d-beyond-foveros



**Deca M-Series Gen 2.1**
**Die pad pitch: 20 µm**
**IO per mm2: 2,518**

#1 in high density

*M-Series Gen 2 delivers order-of-magnitude density increase*

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DECA

# Deca's M-Series Technology Roadmap

## Gen 1
2018 →


Codec


RF


IoT Device

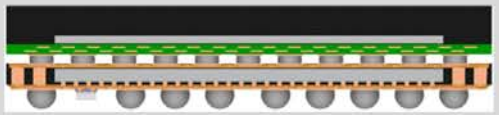

PMIC


Dual PMIC

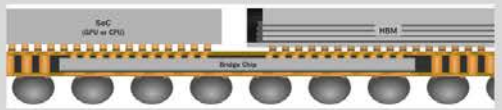
**Single-die**
- Protected fan-in
- Fan-out

**Multi-die**
- RF & IoT modules
- Integrated PMICs

## Gen 1.5
2021 →


**3D PoP** - Mobile Applications Processor


**Fan-out SoC** – Advanced node silicon


**Embedded Bridge Die Interposer** – HBM intg


**Passive & Active Interposers** – CPU, GPU, AI
- *Existing lithography & AOI equipment*
- *Optimized direct & indirect materials*
- *Enhanced process flows for 3D integration*
- *New design rules supporting 3D*

## Gen 2 (SkyWater FI.)
2022 →

20 µm bond pad pitch
2 µm lines & spaces
Up to 5 layers of RDL
Full frontside & backside routing
- 3D PoP
- Fan-out SoC
- Embedded Bridge Die Interposer
- Passive & Active Interposers

**Ultra-High Density (UHD) Integration**

- *New lithography & AOI equipment*
- *Further material optimization for 5 µm vias*
- *New design rules supporting 2 µm RDL*
- *Adaptive metal fill for up to 5 layers of RDL*

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# Agenda

- SkyWater History & Background
- Chiplets - 3D Heterogeneous Integration
- SkyWater AP Offerings
  - Si-Interposers
  - Hybrid Bonding Interconnect
  - Wafer Level and Fan-Out Packaging
  - Solder bumping & Assembly
- Roadmap
- Summary

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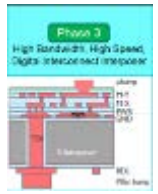
# Capabilities for Advanced Integrations

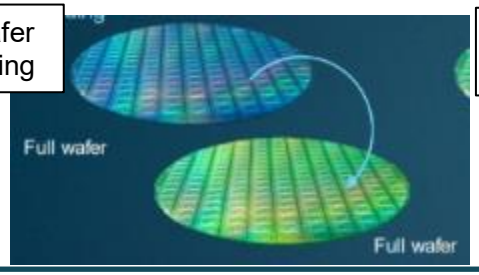
## Silicon Interposers w/TSV

200mm Glass Interposer

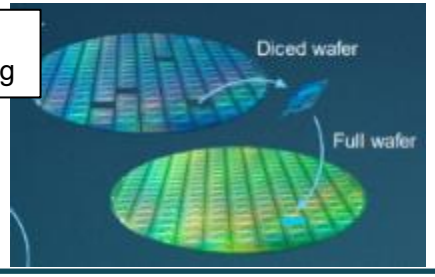


## Hybrid Bonding

Wafer to Wafer Hybrid Bonding




Die to Wafer Hybrid Bonding



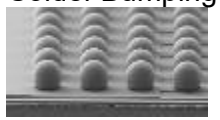

## Wafer Level and Fan-Out Deca's M-Series Gen 2

300 mm

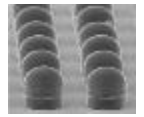
600 mm

## Solder Bumping & Assembly

Solder Bumping



Solder Capped Cu-Pillar



2021 | | 2024

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# Agenda

- SkyWater History & Background
- Chiplets - 3D Heterogeneous Integration
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# Summary

- SW AP Roadmap consists of the following core technologies:
  - Fan-Out  Packaging (Initially wafers, migrating to panels)
  - Si-Interposers
  - Glass Interposers
  - Hybrid Bonding Interconnect
- Maintain technical leadership for all AP areas to ensure our customers have access to a domestic state-of-the-art AP facility.
- Provide solder bumping services (Sn-Pb and Pb-free) and solder assembly services.
- SW is working with our partners to enable a domestic Eco-system for AP.


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**Are you working on an idea? Let's talk.**
**Get in touch today!**

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**swfoundry@skywatertechnology.com**

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