Greetings from Georgia Tech

Semiconductor Packaging
The Future is Now!

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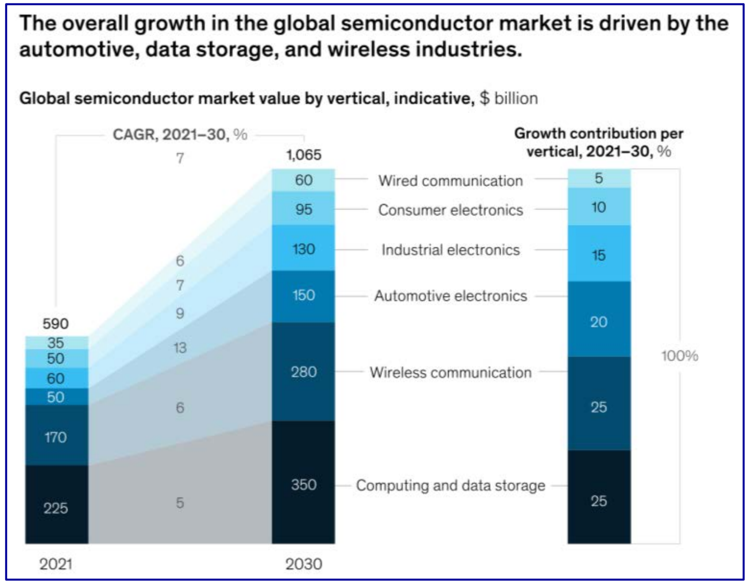
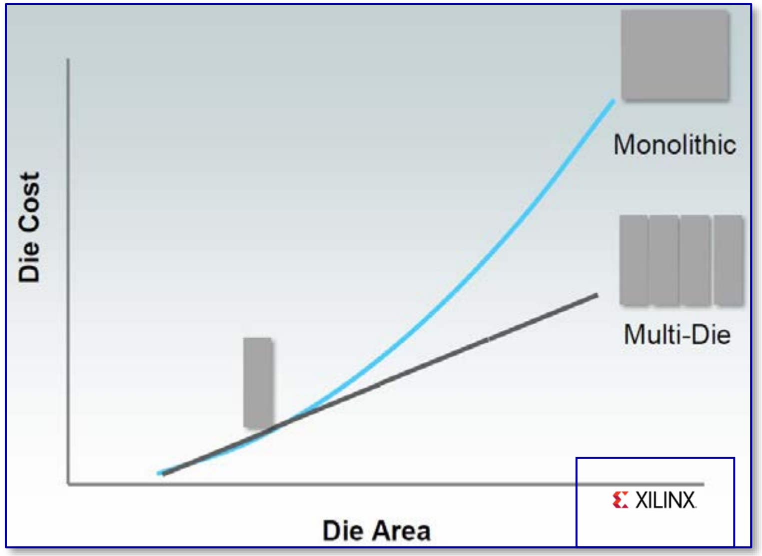
Georgia Tech
PACKAGING RESEARCH CENTER

Georgia Tech | Institute for Electronics and Nanotechnology

Recent Events/Announcements in Semiconductors….

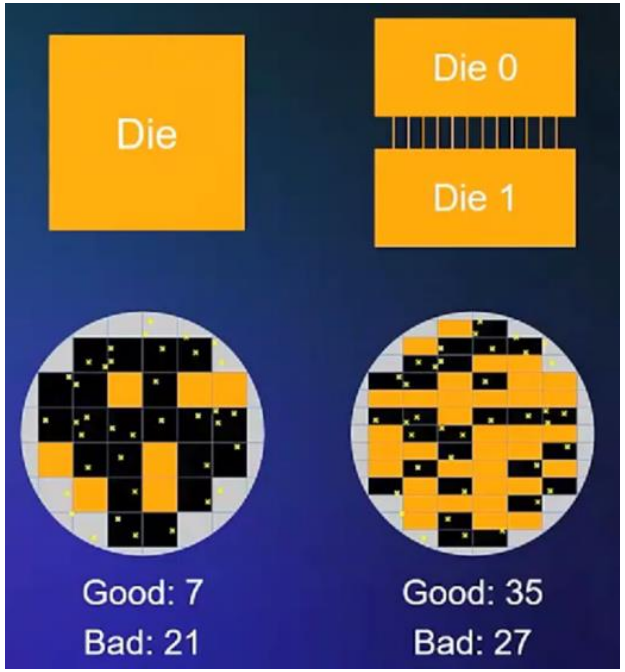
- Global semiconductor industry projected to become a trillion-dollar industry by 2030 (Source: McKinsey & Company)
  - Drivers: Automotive, Computing & Wireless
- 2021: CHIPS for America Act ($52B)
  - Reshoring and U.S. Leadership
  - 2021: U.S. Innovation and Competition Act (USICA) - Senate
  - 2022: America COMPETES Act – House
  - Mar. 1, 2022: State of the Union Address by the President, USA
  - Mar 9, 2022: President's Roundtable with CEOs and Bipartisan Governors Support of Bipartisan Innovation Act
- Continuation of Moore's law becoming challenging
  - DARPA ERI recognized this
  - 2017: CHIPS (Common Heterogeneous Integration and IP Reuse Strategies) Program
  - Relying on Advanced Packaging for continuing Moore's law



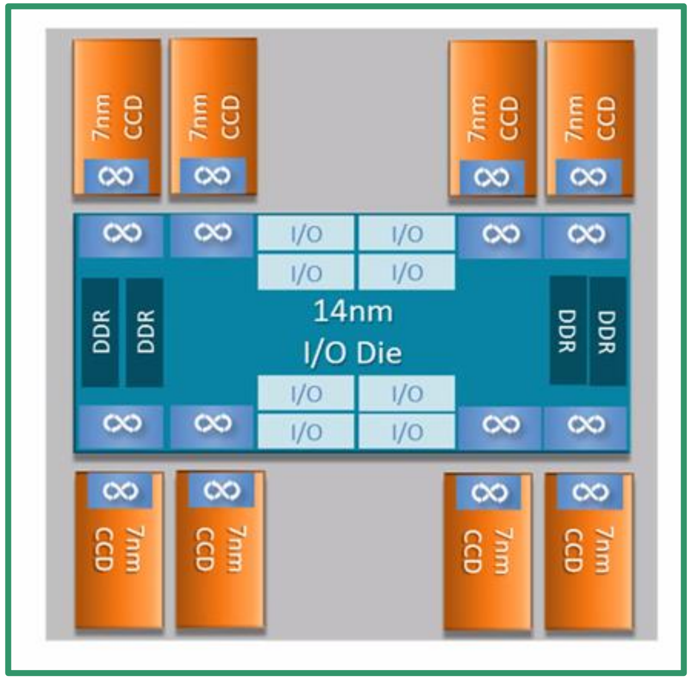


Advanced Packaging – its relevance for the Future of Semiconductor Systems

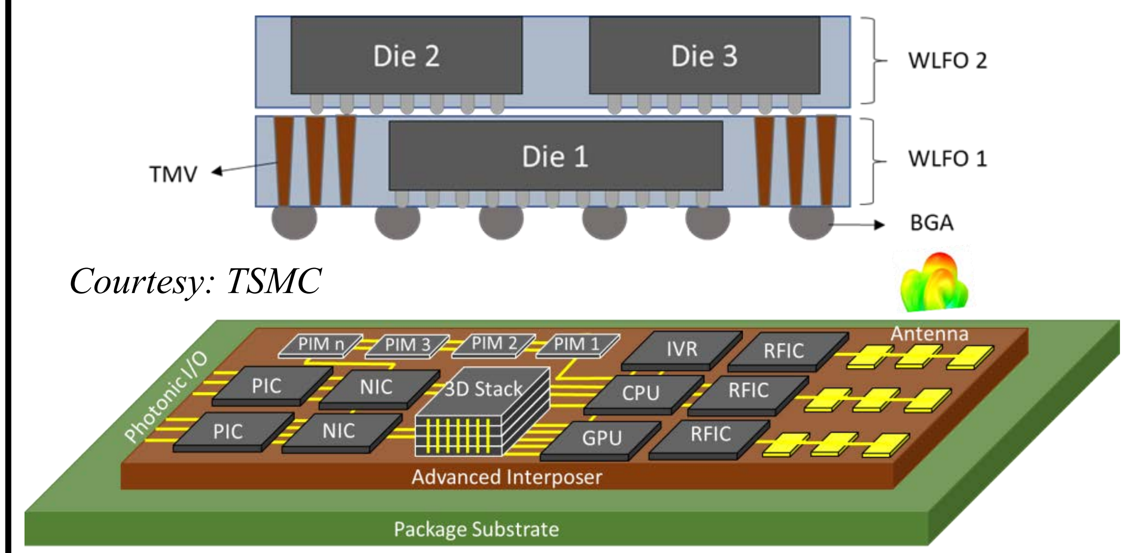
1. Higher yield using smaller dies in advanced nodes.
2. Shorter time to design with smaller dies from optimized legacy technology nodes with enhanced functionality.
3. Move towards **HETEROGENEOUS INTEGRATION**.



Courtesy: EDAPS Keynote, 2020



Courtesy: AMD

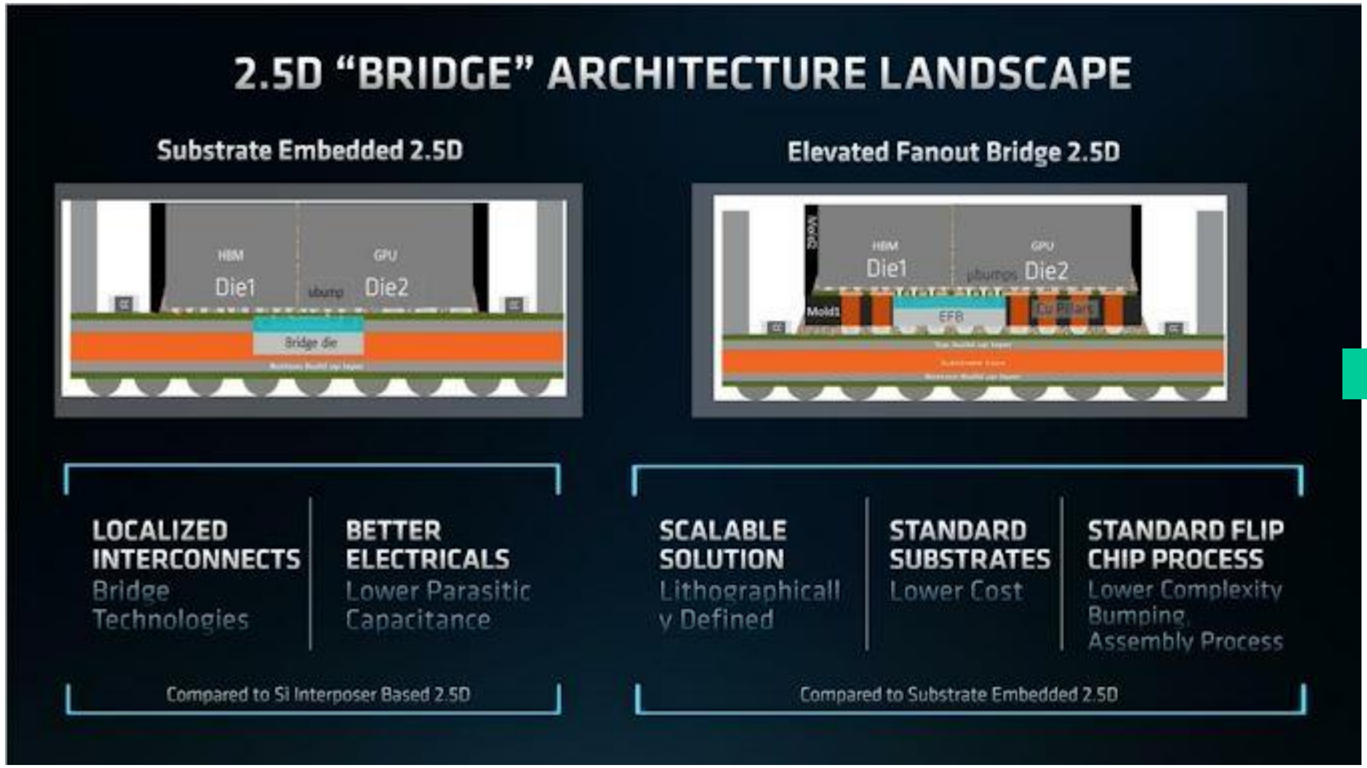


Courtesy: TSMC

Courtesy: GT-PRC, Chip Scale Review, 2022

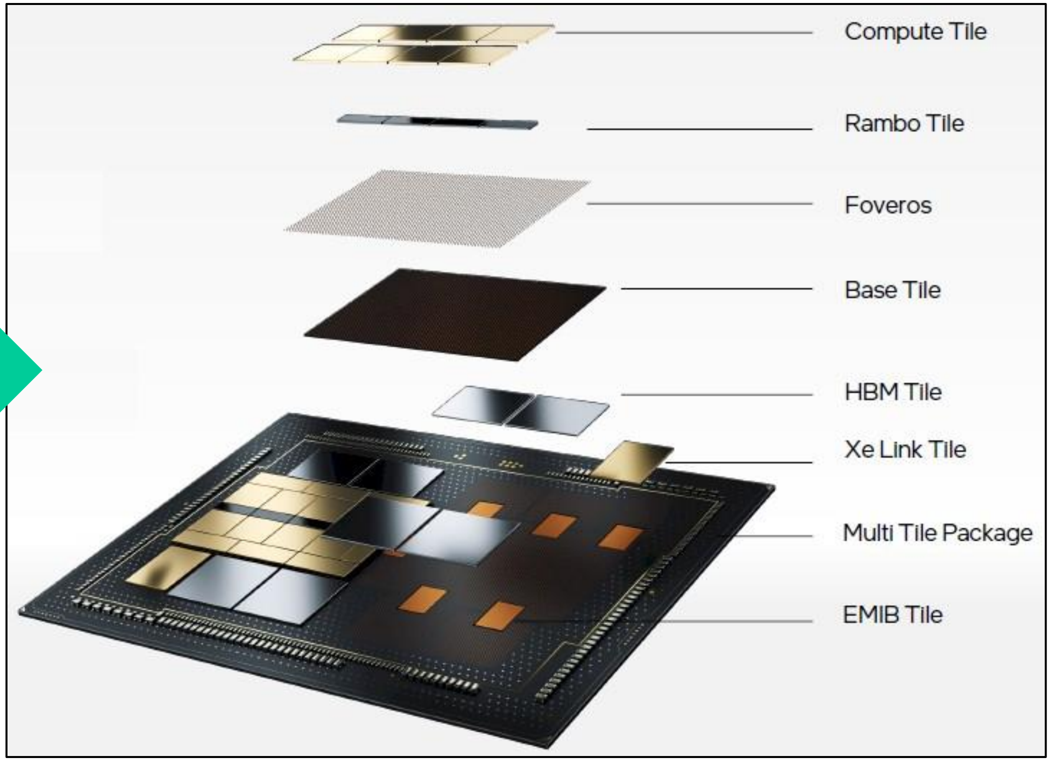
Heterogeneous Integration – Industry SOTA

2D Connectivity



https://www.anandtech.com/show/17054/amd-announces-instinct-mi200-accelerator-family-cdna2-exacale-servers/2

2D & 3D Connectivity



https://www.nextplatform.com/2021/08/24/intels-ponte-vecchio-gpu-better-not-be-a-bridge-too-far/

Ponte-Vecchio - 47 dielets with over 100 billion transistors

Role of Universities

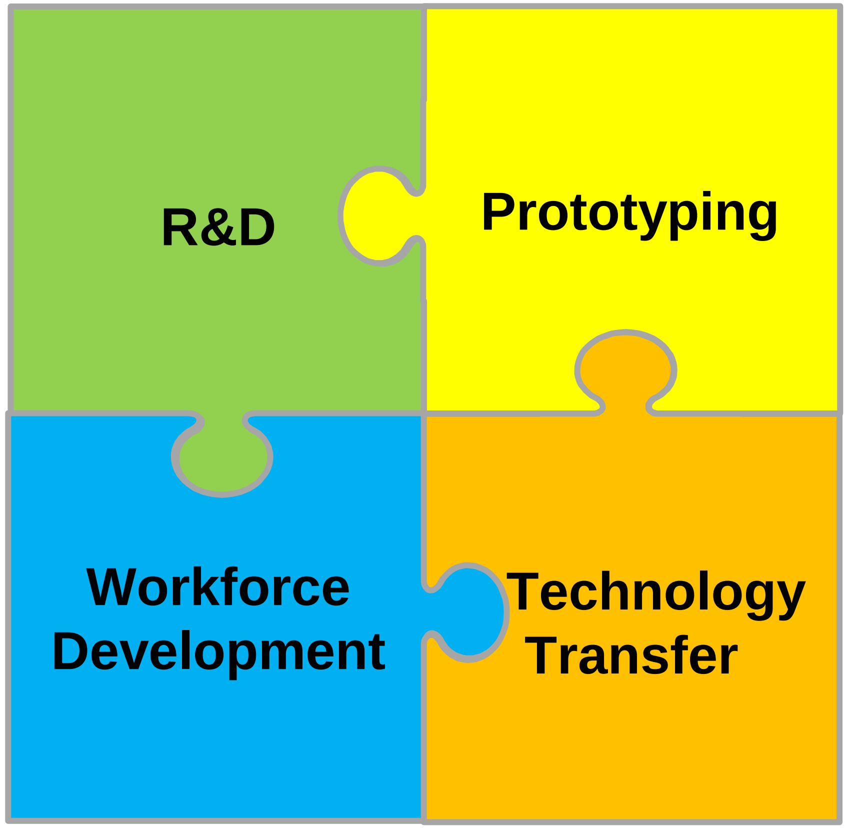
Universities have two important roles:

❑ Workforce development

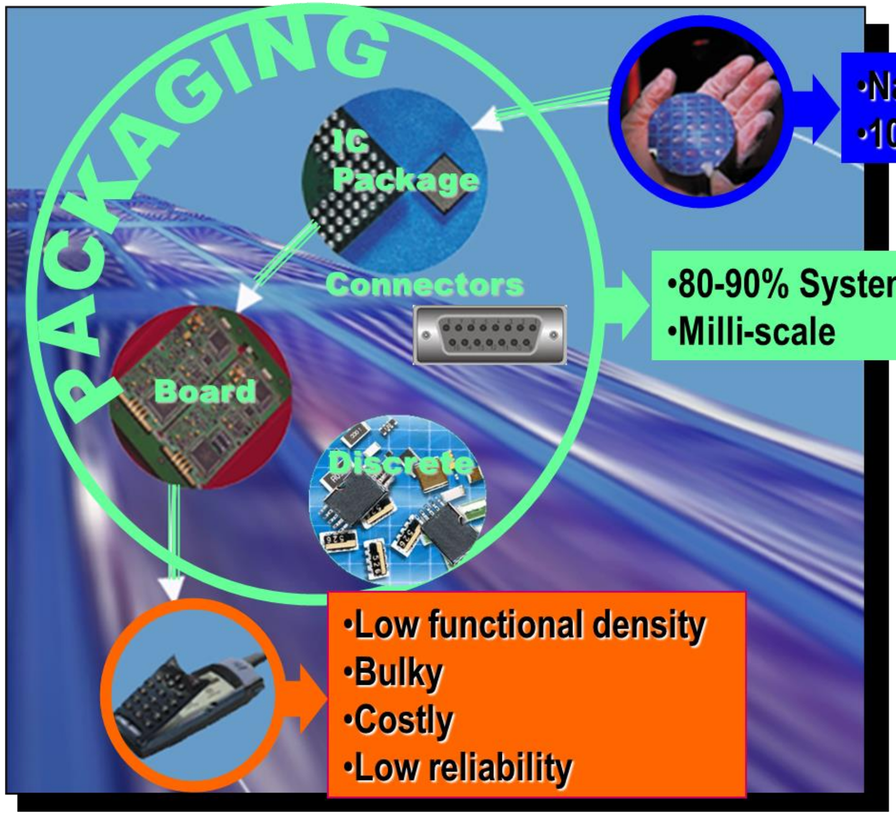
- K-12, 2 Year, 4 Year, Advanced Degrees
- Technical Training.

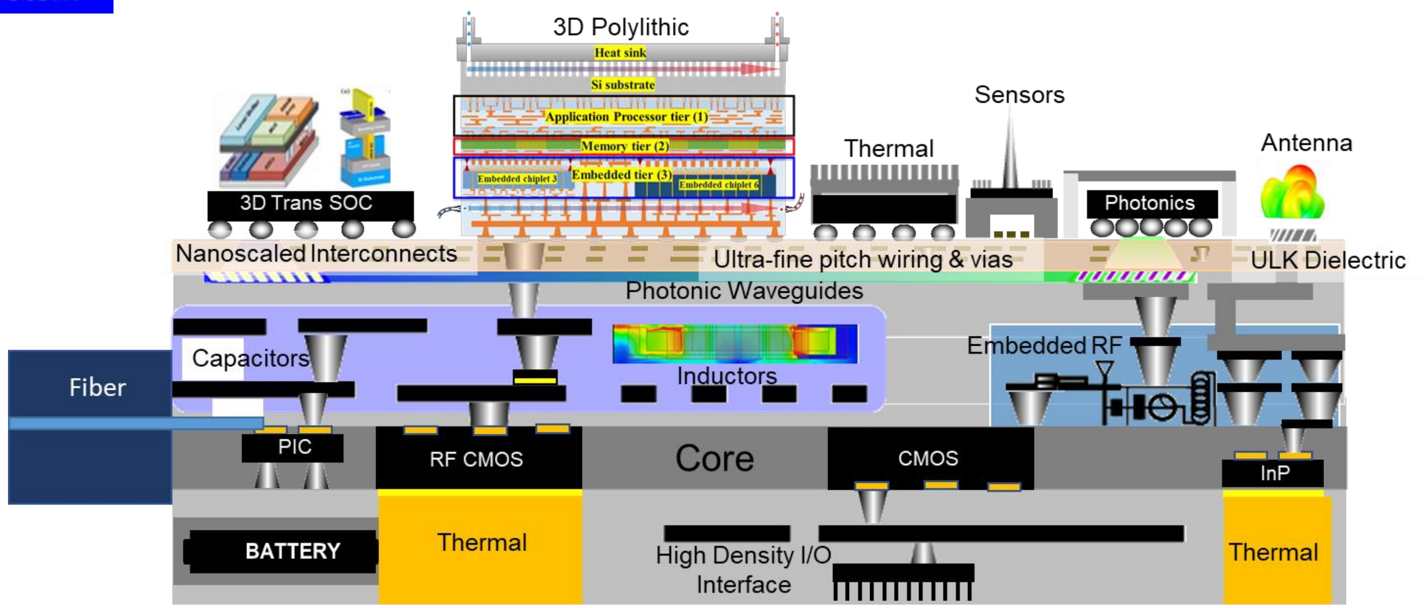
❑ <u>Academic research driving US leadership</u>

- Support fundamental, applied, and translational research, from concepts to prototypes, that will ensure the U.S. is a global leader in semiconductor based electronic systems manufacturing, while also securing the supply chain.



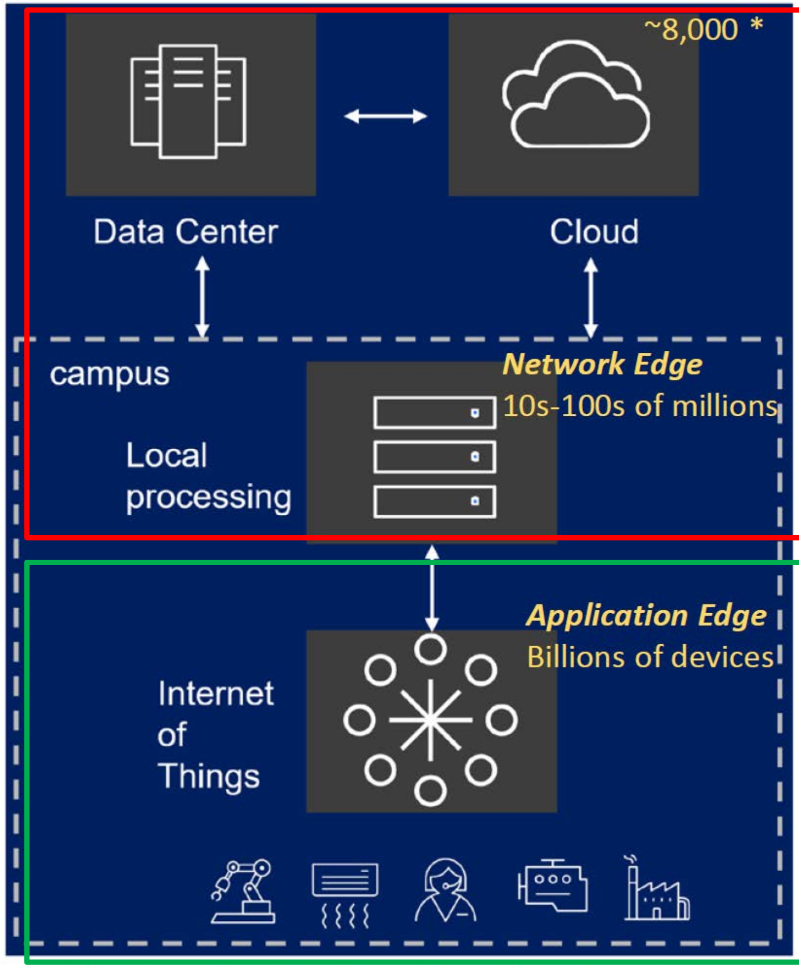
Our Vision – The Future of Packaging





- ❑ **Advanced Devices** (Transistor Scaling)
  - 3D Transistors, Monolithic 3D
- ❑ **Advanced Packaging** (Package Scaling)
  - High density interconnectivity between chips with integrated and embedded 2D & 3D
- ❑ Transistor Scaling + Package Scaling = **System Scaling**

Emerging Distributed Computing & Communication Requirements

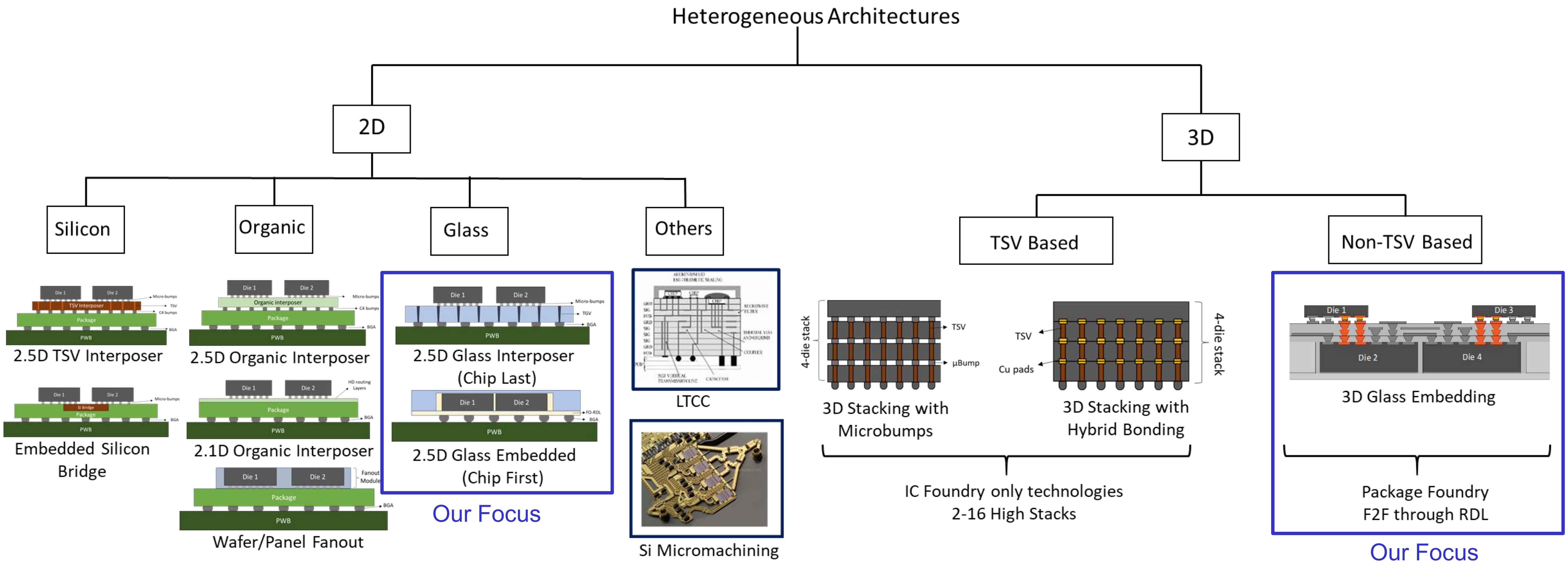


- Neuromorphic (& Quantum) Computing
- Bandwidth Density: 1000Tbps/mm^2 @ fJ/bit
- Thermal Design Power (TDP): >1kW/cm^2
- Power Delivery: 1kW to 50kW with >80% efficiency

- Unmanned mobility (Automotive)
- Pervasive Connectivity: 10^6 devices/km^2 (5G) to 10^7 devices/km^2 (6G)
- Capacity: 20Gbps (5G) to 1Tbps (6G)
- High Energy Efficiency

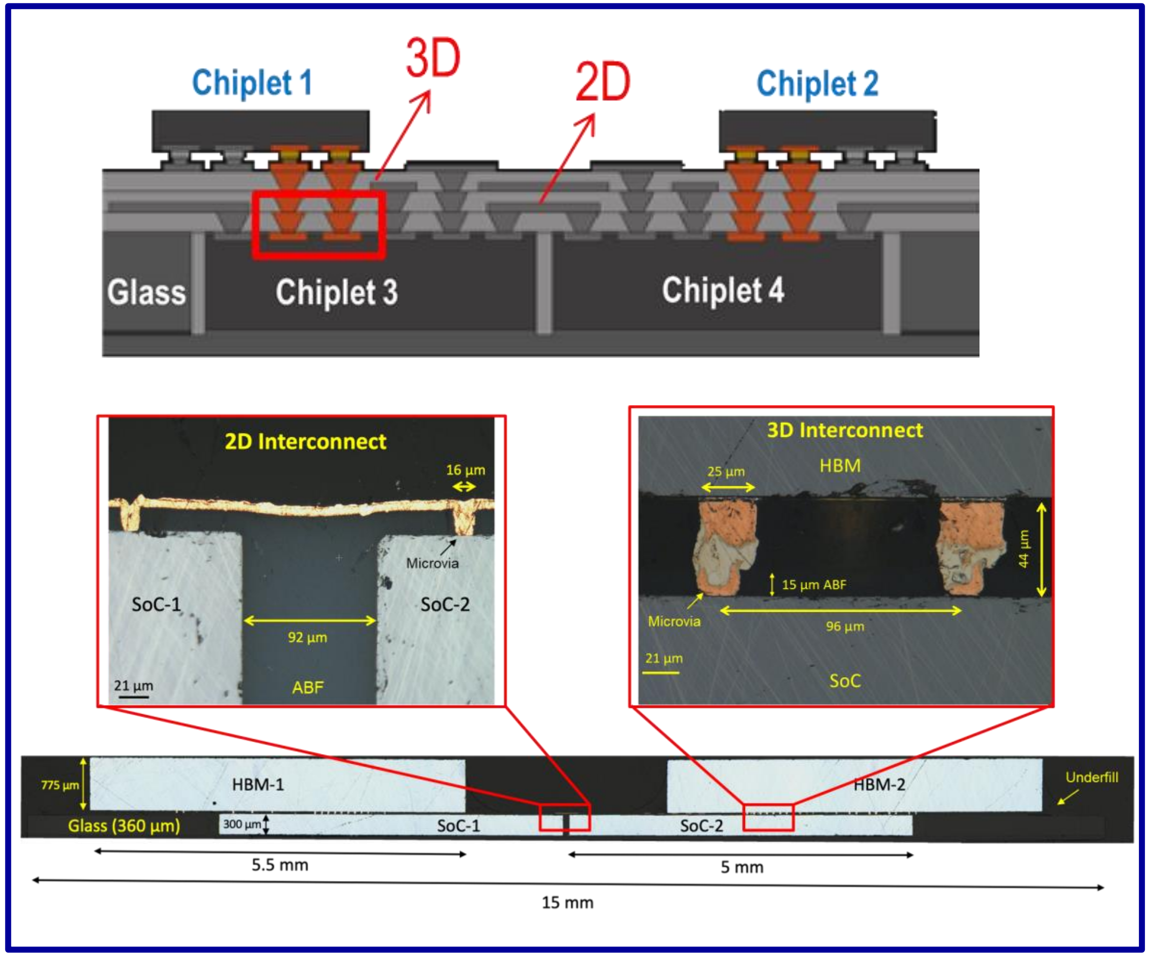
* *USITC Executive Briefings, May 2021* “**Data Centers Around the World: A Quick Look**“

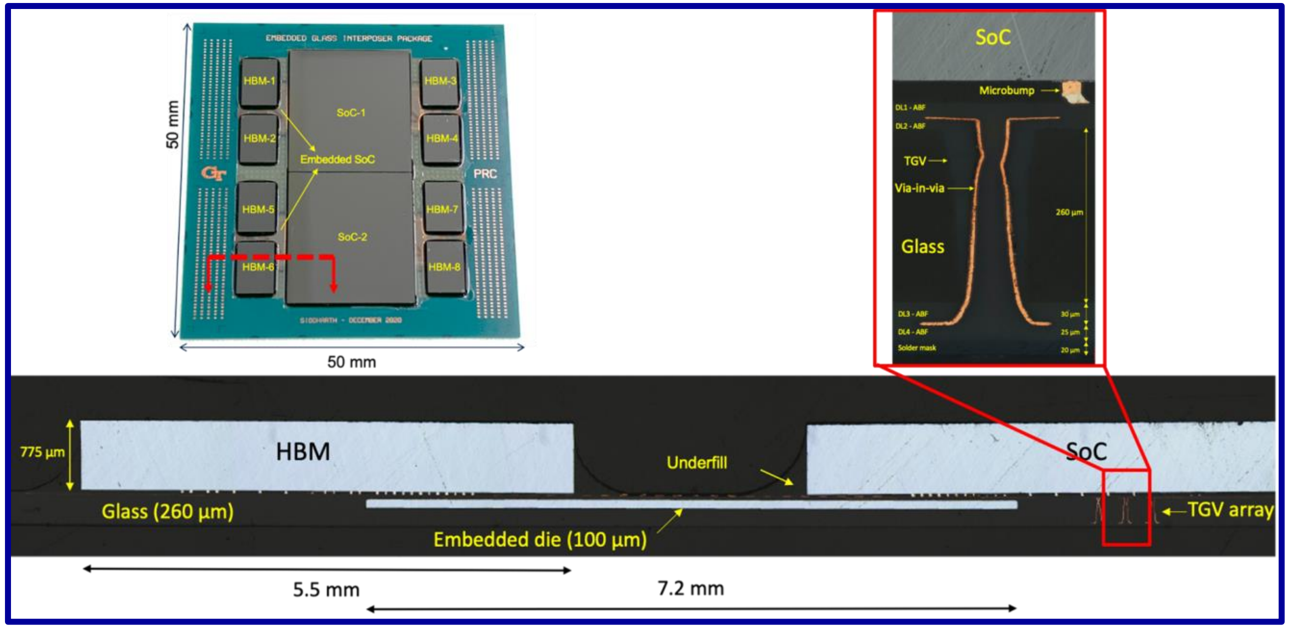
Advanced Packaging & Heterogeneous Integration State of the Art



S. Ravichandran & M. Swaminathan, Heterogeneous Integration for AI Applications: Status & Future Needs, Chip Scale Review, 2022

Glass Interposer w/ 2D & 3D Connectivity

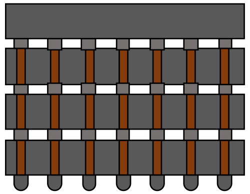
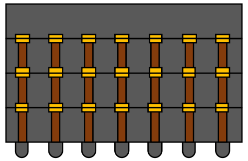
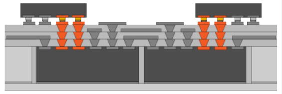




Features

- ❑ High density 2D & 3D Connectivity
- ❑ Eliminate assembly for embedded dies
- ❑ Panel (square) scalable to 500mm
- ❑ Tailorable CTE for maximizing 1st and 2nd level reliability
- ❑ Thermal insulation between dies
- ❑ High heat flux removal from top & bottom
- ❑ Large Panel Size to reduce cost

3D Heterogeneous Integration

	TSV-based		Non-TSV
	3D IC /w TSV *[Zhang, et al. '18]* 	**Hybrid Bonding** *[Chen, et al, '19]* 	**3D Glass Embedding** *[Ravichandran, et al, '19]* 
Status	Commercial	Commercial	Research
Dielectric Constant	3.9*	3.9*	2.5-3
IO pitch	40 μm	10 μm	20 μm
Interconnect length	75 μm*	50 μm*	35-50 μm
Interconnect density (IO/mm^2)	625	10000	2500
V_{swing}	0.7 V*	1 V*	1 V
$R_{on}/C_{Tx}/C_{Rx}$ (Ω/F/F)	n/a	n/a	50/50f/50f
Data rate/IO	1.69 Gbps	n/a	1.86 Gbps
Bandwidth density	1.76 $Tbps/mm^2$*	n/a	4.65 $Tbps/mm^2$
Energy-per-bit	76.2 fJ/bit	7 fJ/bit*	11.2 fJ/bit

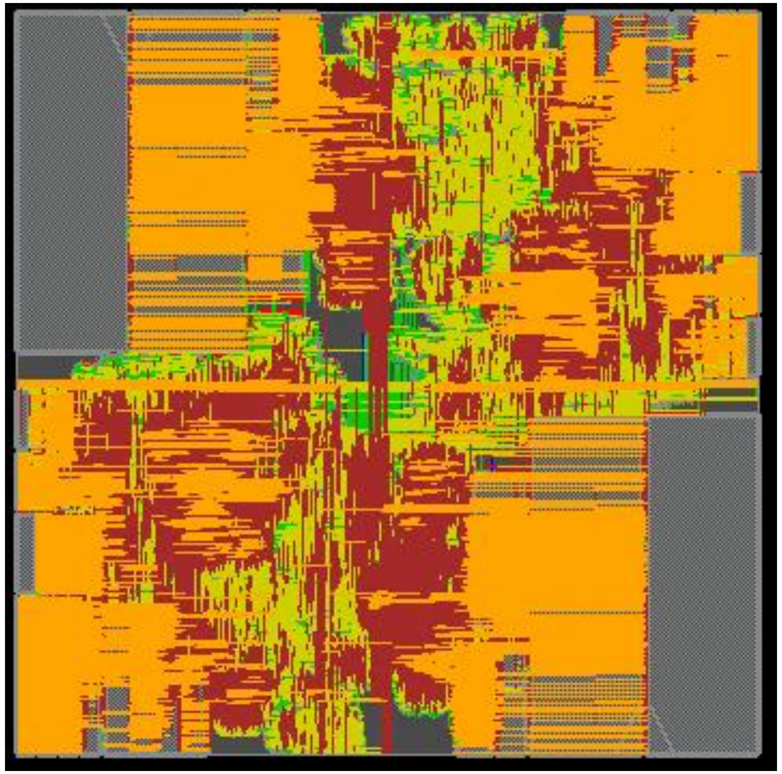
** Derived metric*

S. Ravichandran and M. Swaminathan, Chip Scale Review (2022)

What can this enable? Case for Chiplets/Dielets!

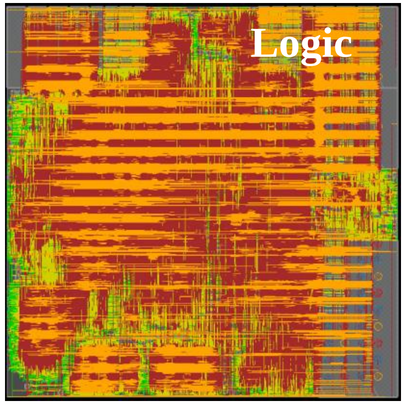
partitioned into 4 dielets

1.6 mm

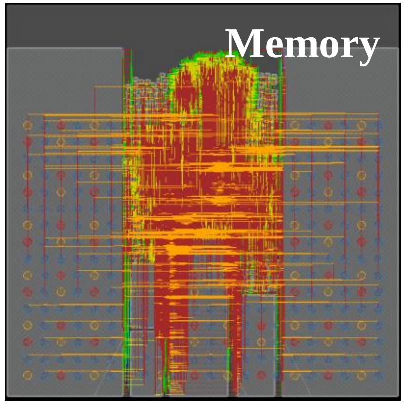


2D Monolithic (RISC-V)

0.82mm

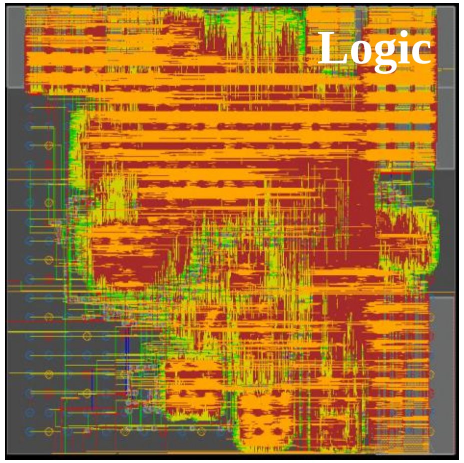


0.82mm

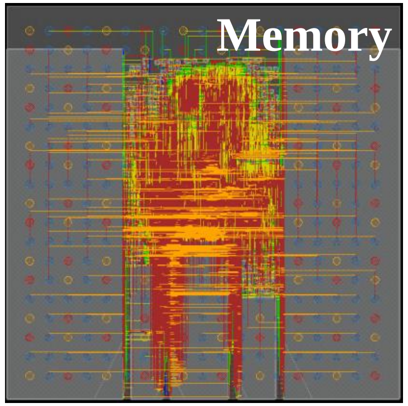


Glass Interposer

0.94mm



0.82mm



Silicon Interposer

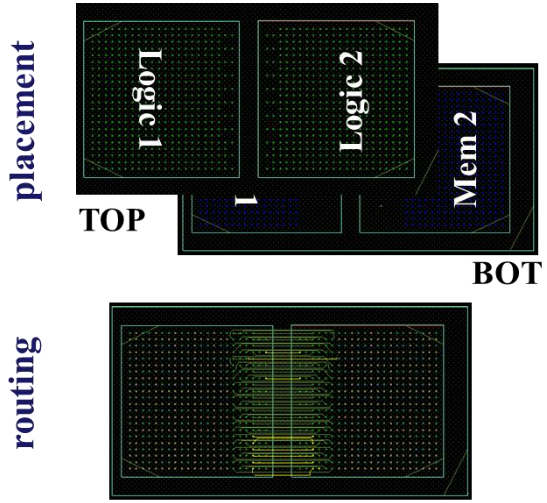
Collaboration with Pruek Vanna-iampikul (GT), Sungkyu Lim (GT) & Ravi Agarwal (Meta)

Interconnect Wiring Details

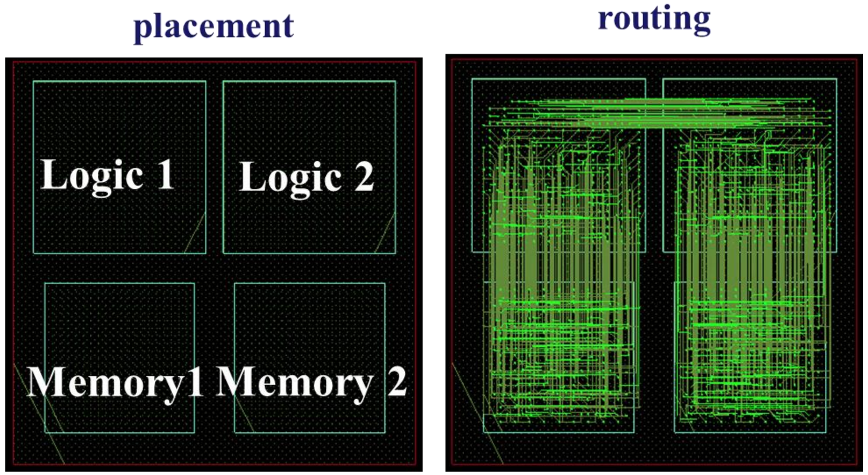
CoWoS (TSMC)
SOTA

	Glass Interposer	Silicon Interposer
# Metal Layer	3	4
Metal thickness	4um	1um
Dielectric thickness	15um	1um
Min. Wire width / spacing	2um / 2um	0.4um / 0.4um
Via size	12um	0.4um
Pad size	22um	0.7um
Die-to-Die spacing	100um	100um
Micro-bump pitch	35um	40um
PDN width/spacing	40um / 100um	

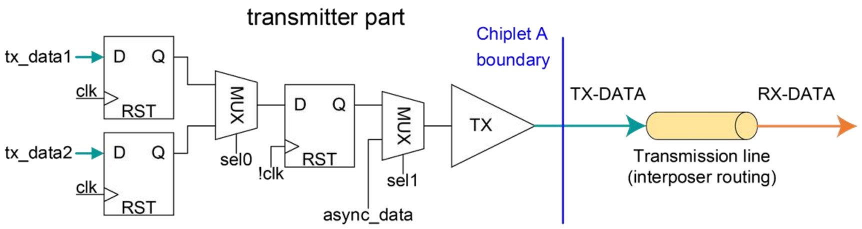
Dielet-to-Dielet Connectivity

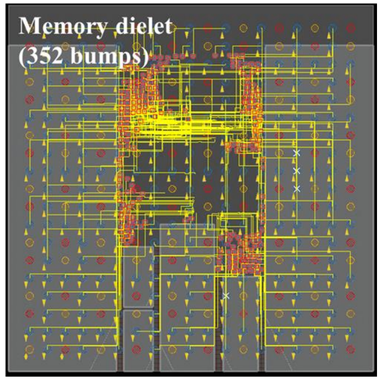


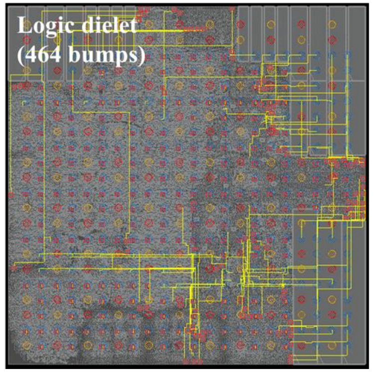
3D (glass Interposer)

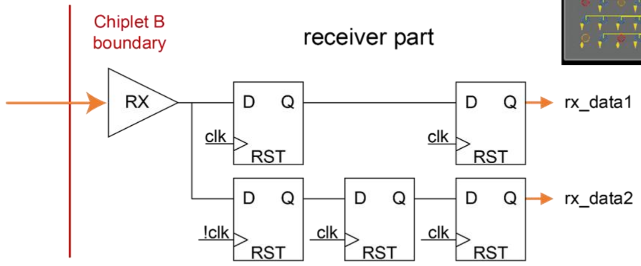


2D (silicon Interposer)









- ❑ Dielets communicate with each other through AIB signaling

Area & Wire Length Comparison

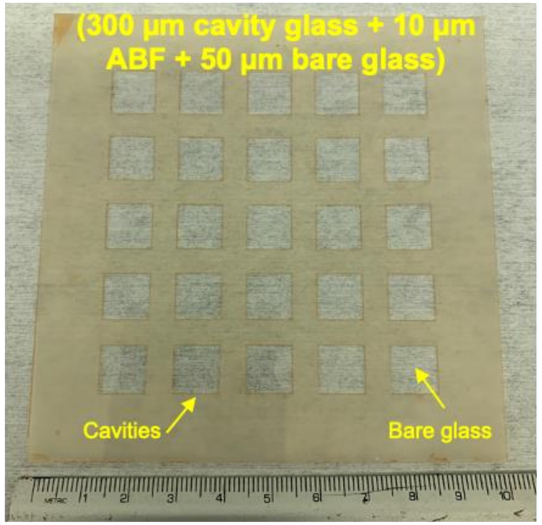
- ❑ Huge savings with 3D Glass due to 3D connectivity
- ❑ 3D Glass 1.36X smaller than 2D Monolithic

Parameter	2D	3D (glass)	2.5D (silicon)	3D vs. 2.5D
Metal layer used	-	2	4	2x
Total interposer WL (mm)	-	29.69	620.21	20.8x
Average interposer WL (mm)	-	0.43	0.50	-
Max interposer WL (mm)	-	0.67	3.01	5x
interposer via usage	-	21 + 924	1542	1.6x
Footprint (mm x mm)	1.6 x 1.6	1.84 x 1.02	2.2 x 2.2	-
Area (mm2)	2.56	1.87	4.84	2.6x

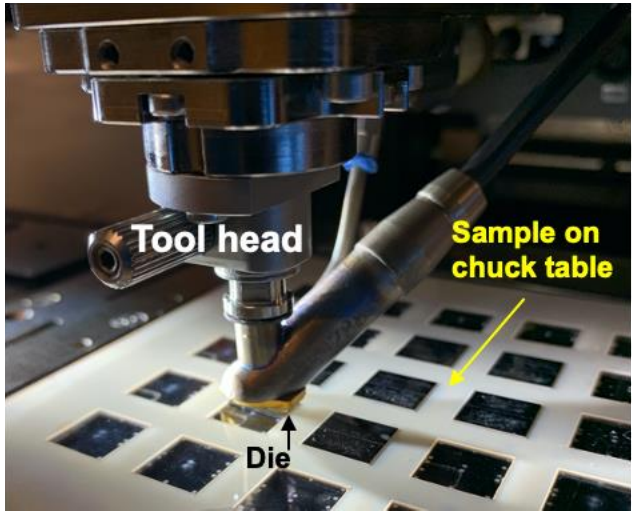
- ❑ 12% Power Overheard for 3D Glass over 2D Monolithic
- ❑ 5% increase in frequency with 3D Glass over 2D Monolithic

Glass Panel Embedding (GPE) Process

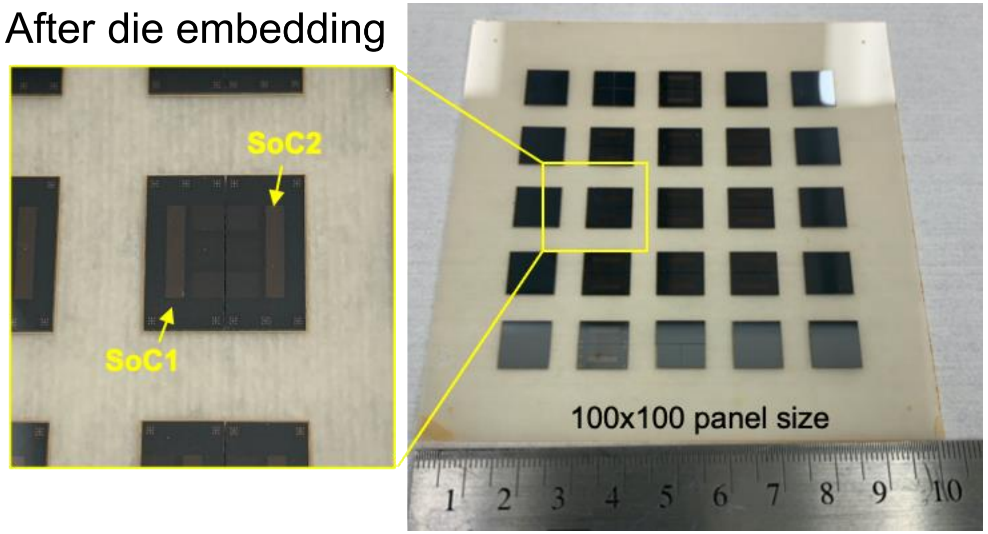
Laminated cavities



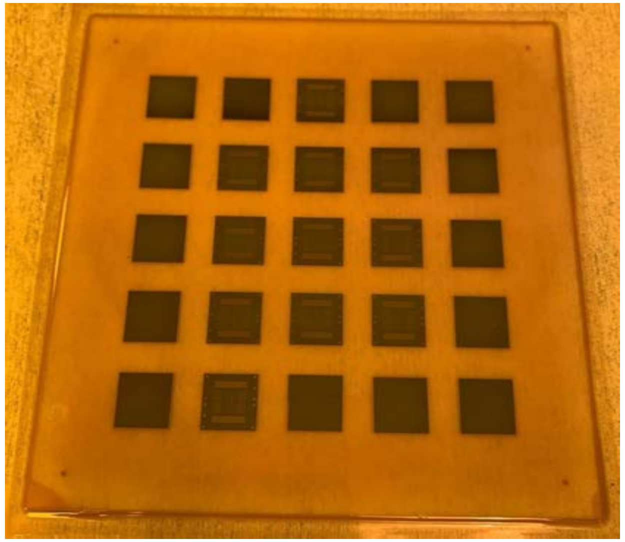
Die placement



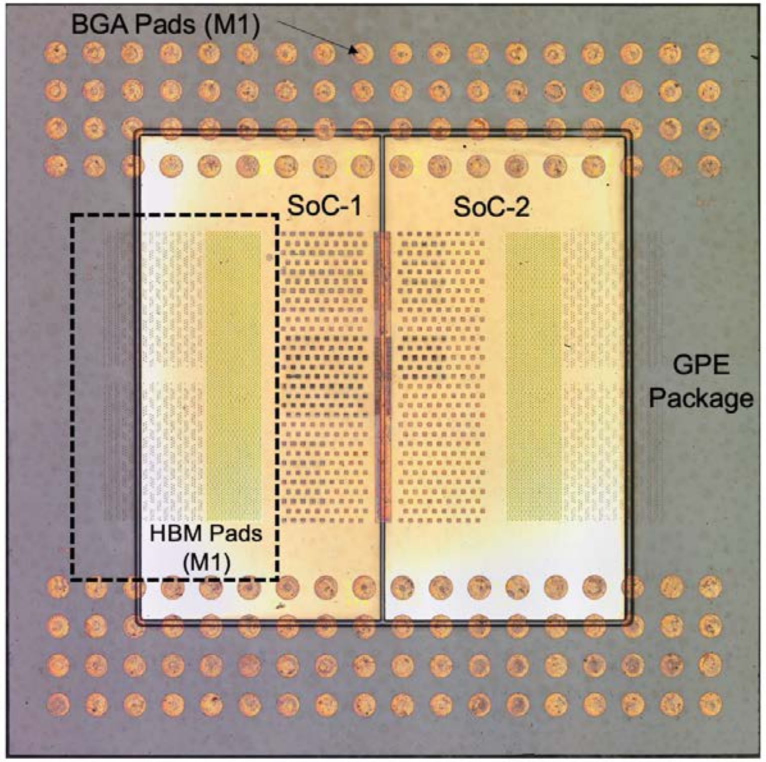
After die embedding



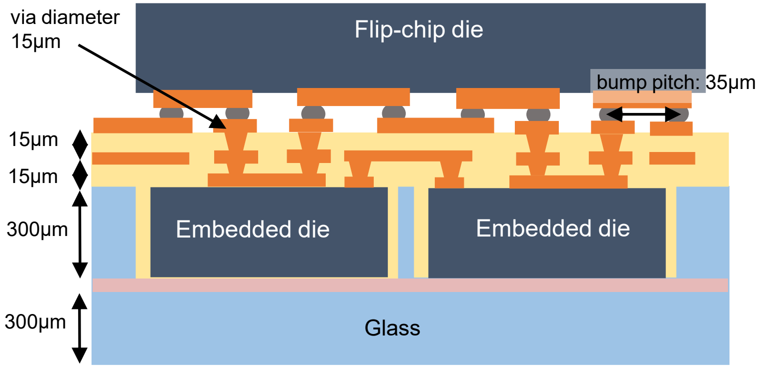
After dielectric lamination



Fully fabricated GPE substrate

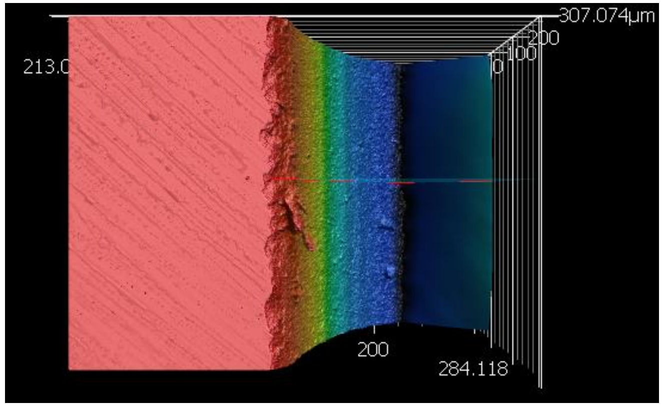


Bandwidth Density

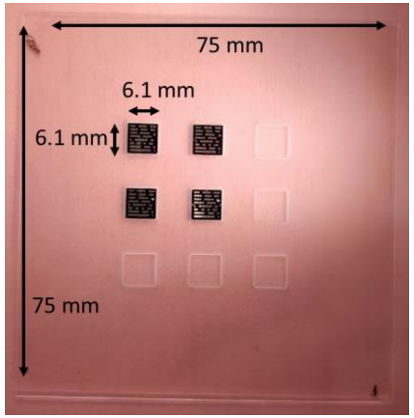


Cross section of the 3D embedded die with die-to-die interconnects

Cavity drilling process

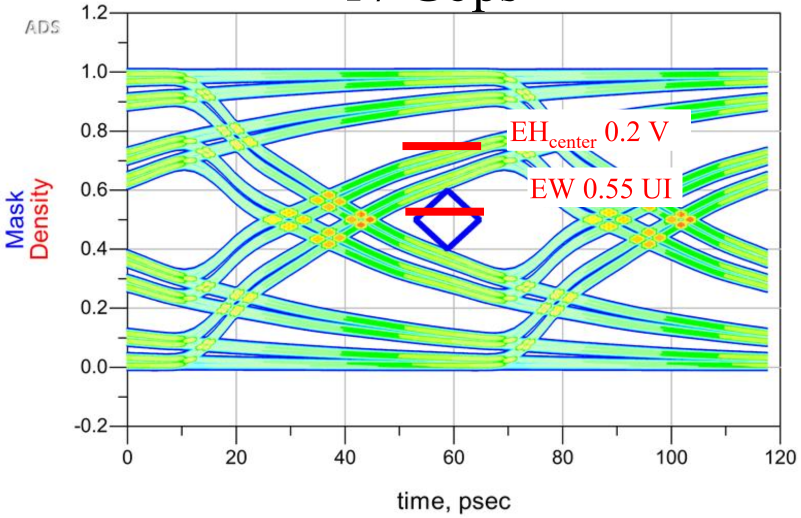


Cavity wall top profile



Panel with some embedded dies

17 Gbps

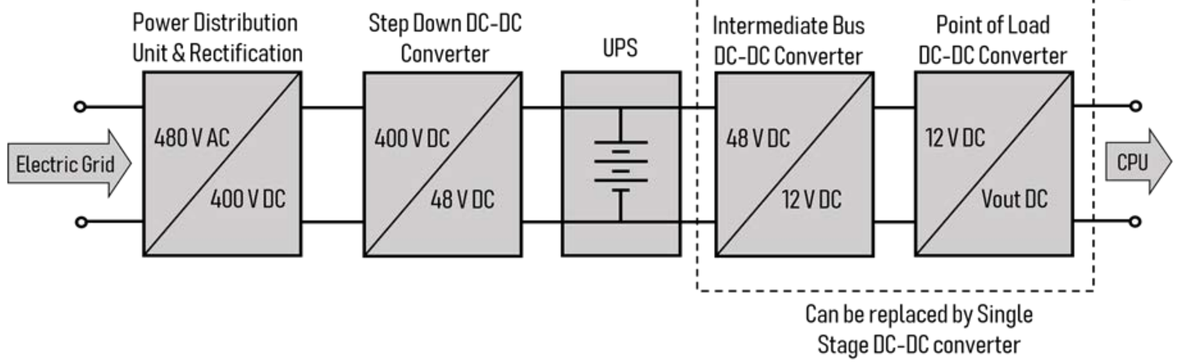


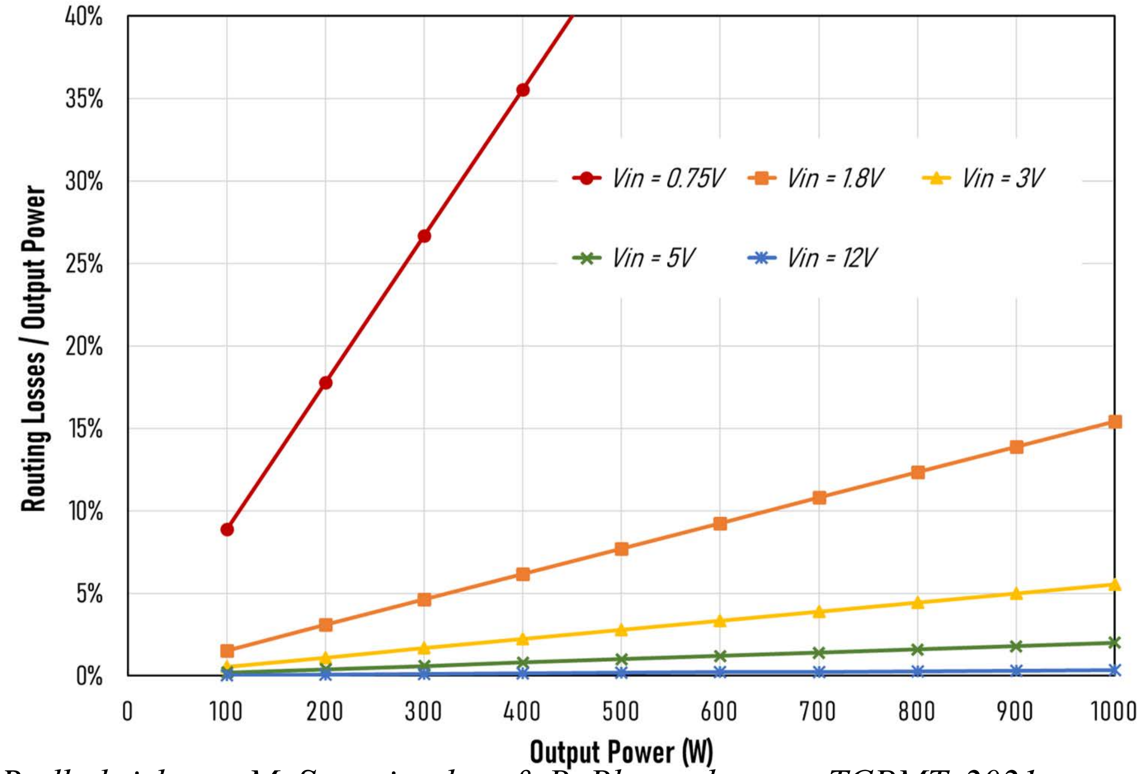
$C_{tx} = C_{rx} = 0.5$pF, $R_{on} = 50$ Ohm

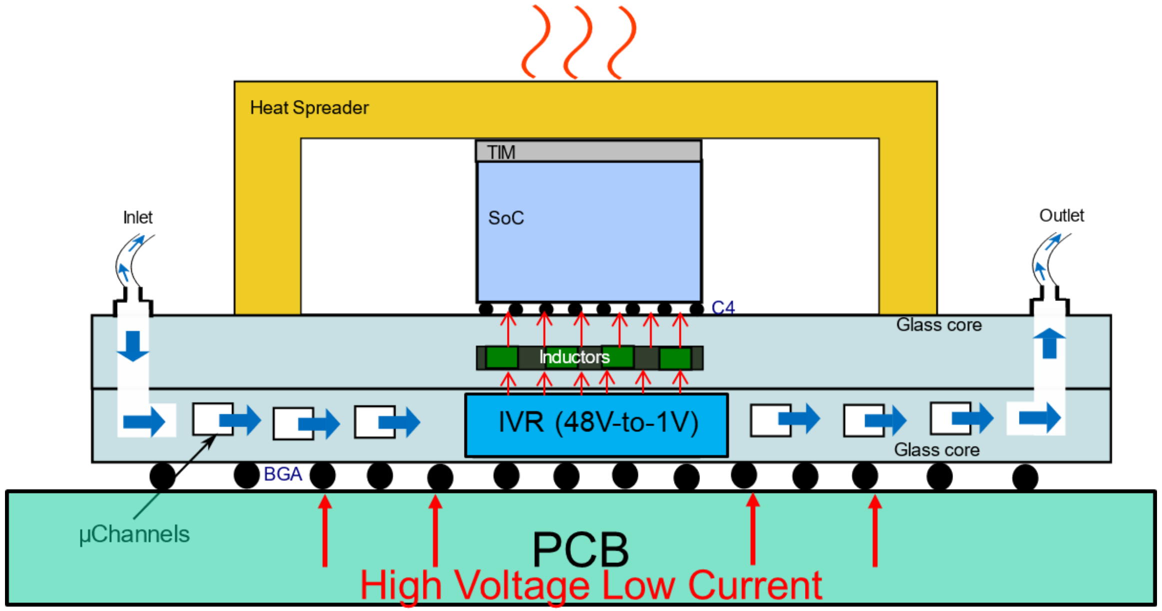
- Signal-to-GND ratio 2:1
- Based on 0.2 V EH - 0.2UI EW and BER=1e-12
  - Data rate / IO = 17 Gbps / IO
  - **BW density = 9.25 Tbps/mm²**

Courtesy: Serhat Erdogan, Ph.D. Student, GT

Power Delivery – Going Vertical





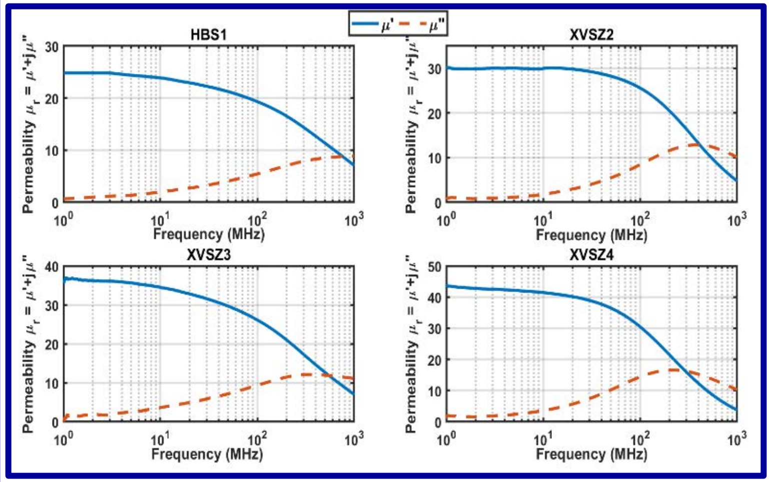


- 1000W; 2-5 A/mm²; >80% Efficiency
  - Integrated Voltage Regulator (IVR)
  - Integrated Inductors
  - Vertical Power Delivery
  - Minimum routing losses
  - Effective heat removal

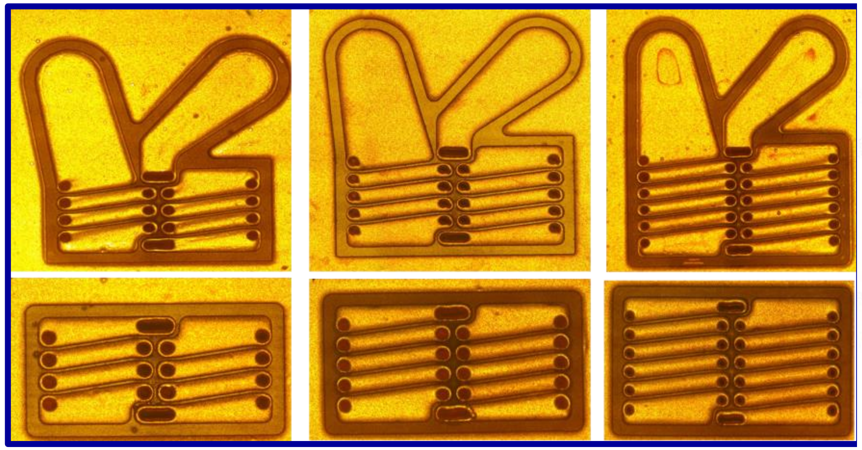
K. Radhakrishnan, M. Swaminathan & B. Bhattacharyya, TCPMT, 2021

Embedded Inductors for Power Delivery

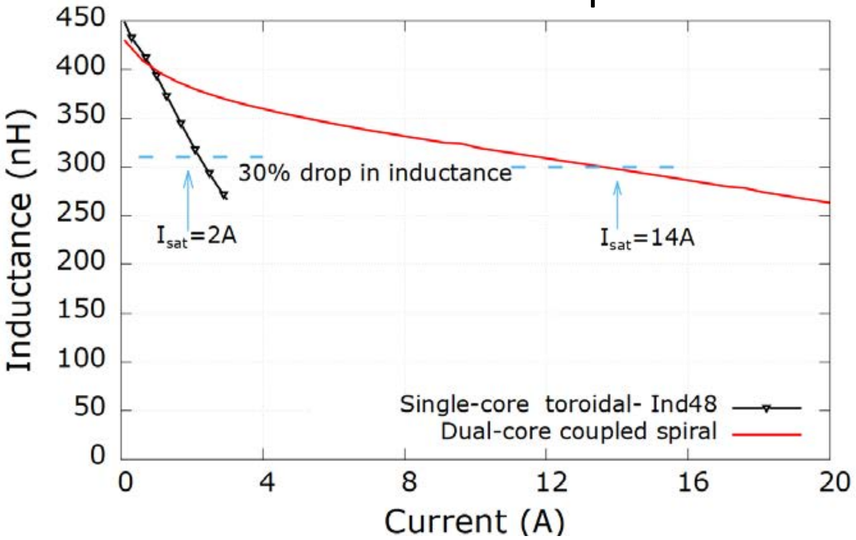
Magnetic Materials



Fabricated Inductors

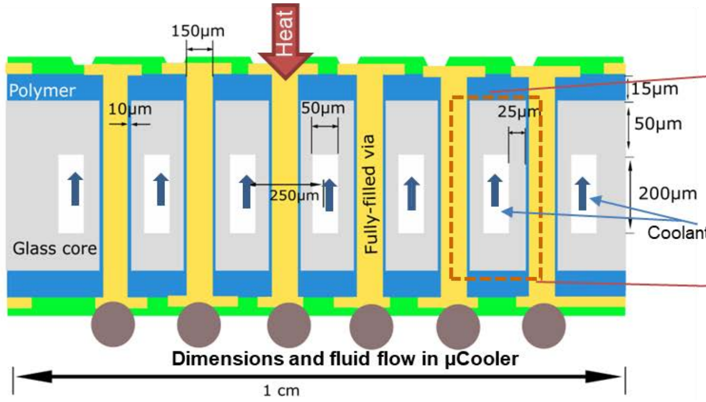


Inductor Response

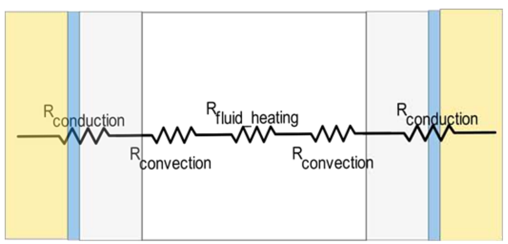


	Inductance (nH)	Conversion (D)	Switching frequency, f_{sw} (MHz)	Sat. current (A)	Energy Stored/per cycle (W)
Coax (Intel) [ECTC '21]	2.5	1.8V-to-1V	140	8	23
Air core (Intel) [APEC '14]	1.2	1.8V-to-1V	140	9.6	17
Array (Intel) [ECTC '20]	3	1.8V-to-1V	140	4	7
Toroid HPE1 (GT PRC) [ECTC '21]	450	48V-to-1V	5	0.02	3
Dual spiral (GT PRC)	400	48V-to-1V	5	4	32 (ongoing)

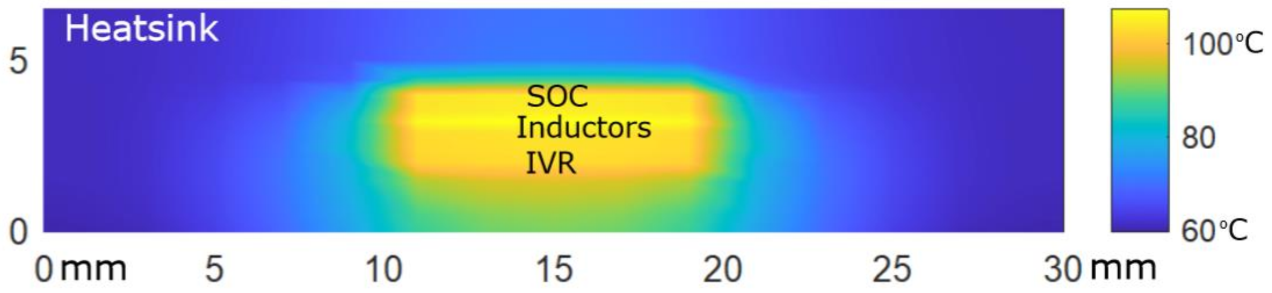
Micro-coolers for Power Delivery



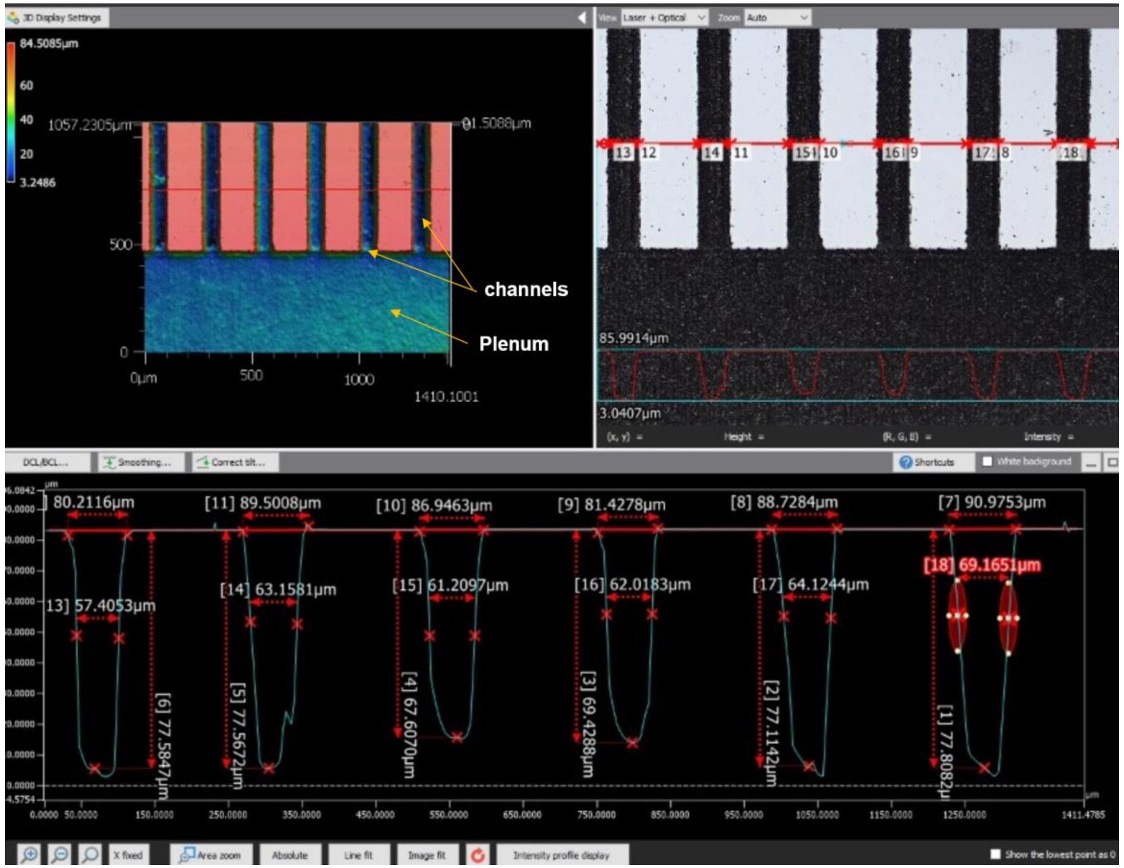
Dimensions and fluid flow in μCooler



Compact thermal model of a micro-channel

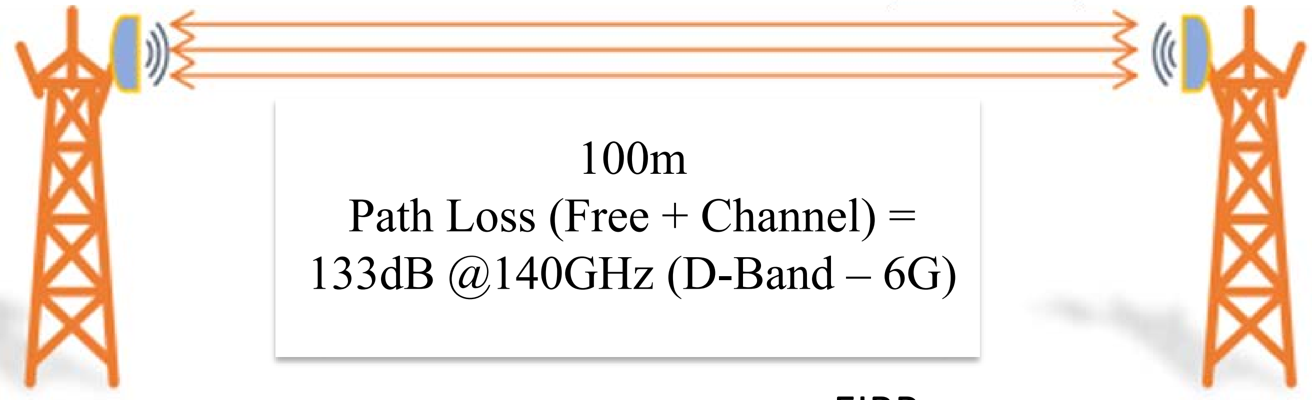


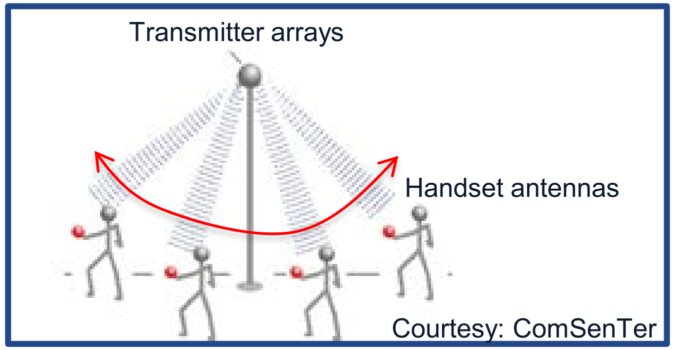
Heat map of the 3D IVR

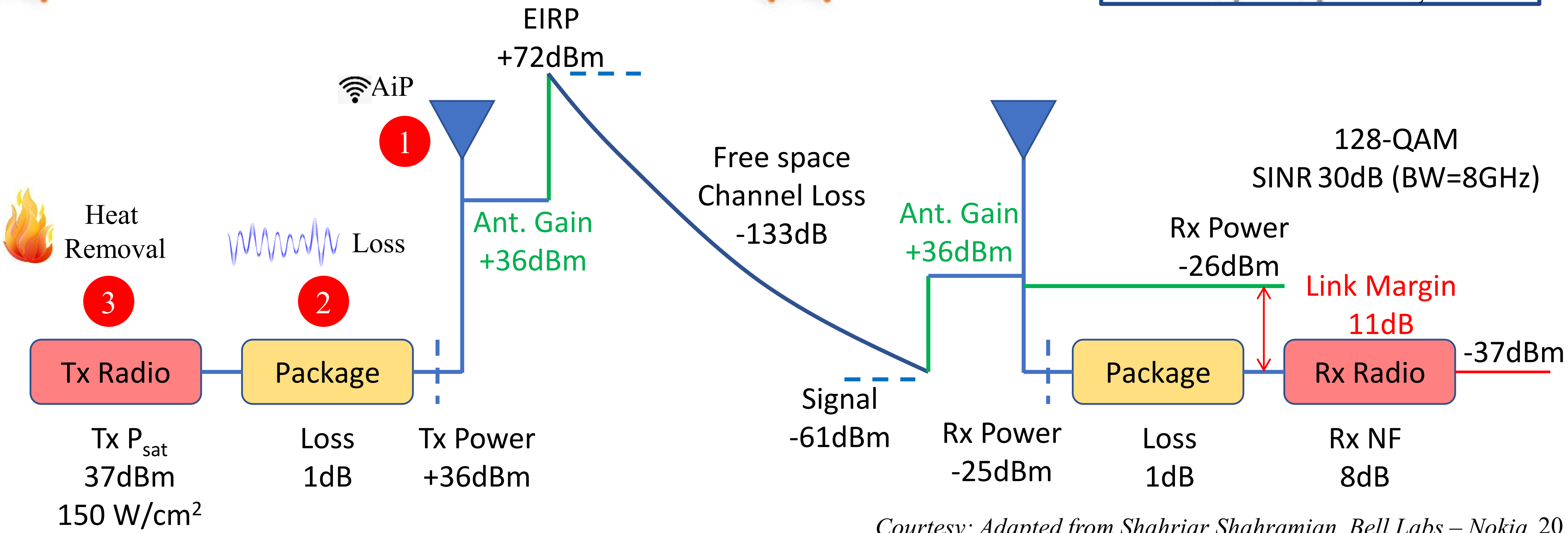


Collaboration with Vanessa Smet & Yogendra Joshi (GT) *Courtesy: Venkatesh Avula, Ph.D. Student, GT*

Wireless Communication Link – 6G





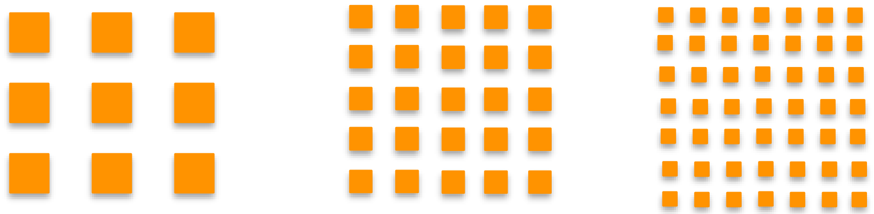


Courtesy: Adapted from Shahriar Shahramian, Bell Labs – Nokia 20

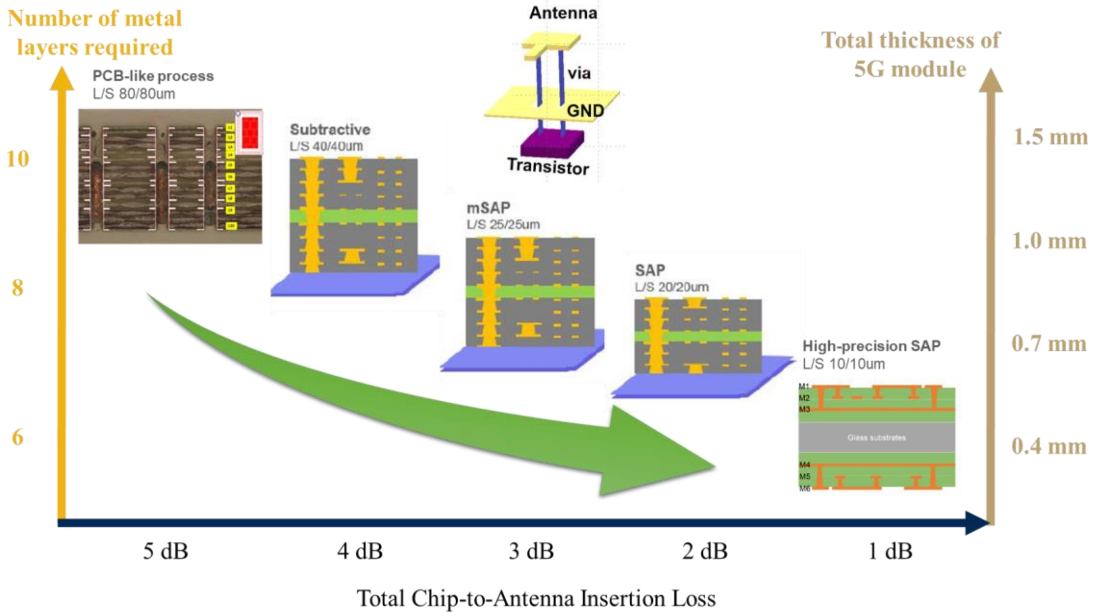
Enabling Connectivity @ sub-THz Frequencies

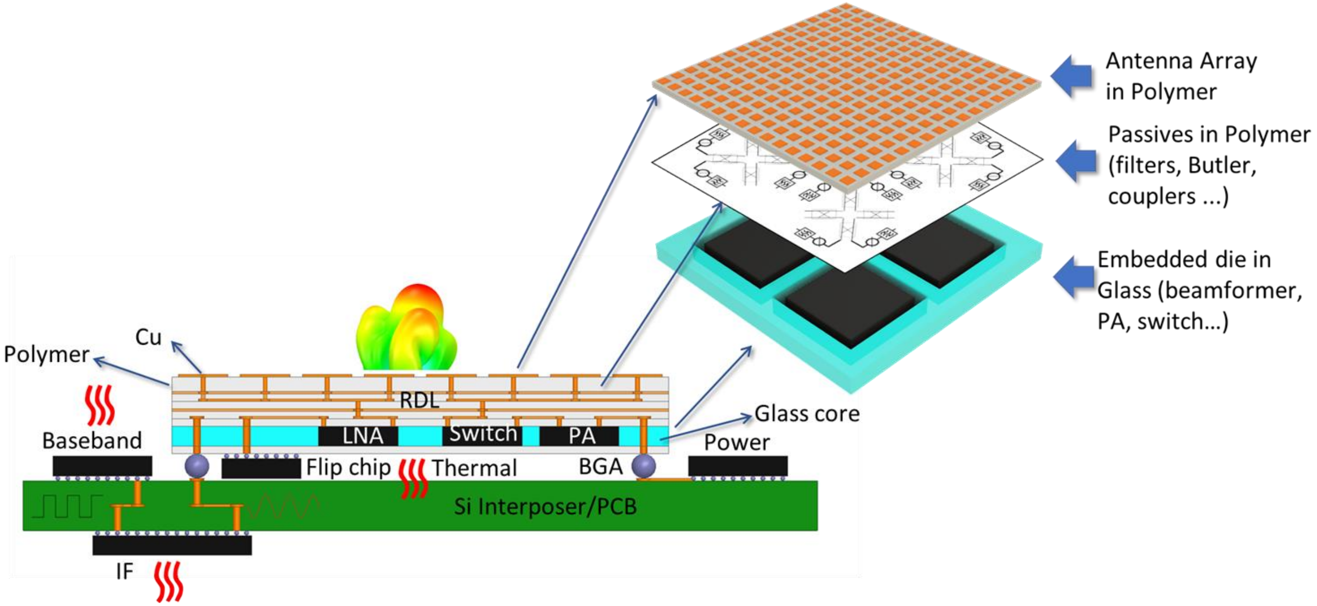
Scalable Antenna Array

140GHz | 205 GHz | 280 GHz



$\lambda/2$=1.1mm | $\lambda/2$=0.7mm | $\lambda/2$=0.54mm

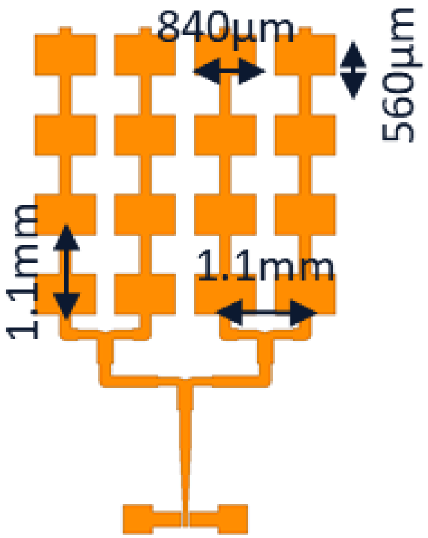


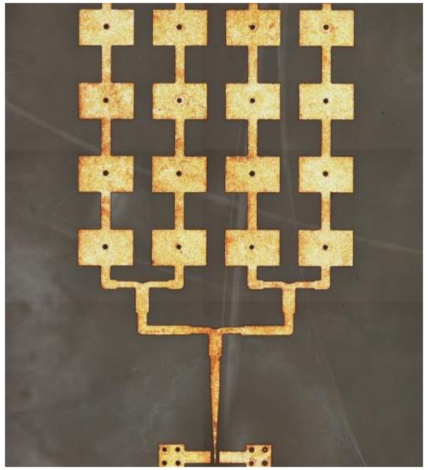


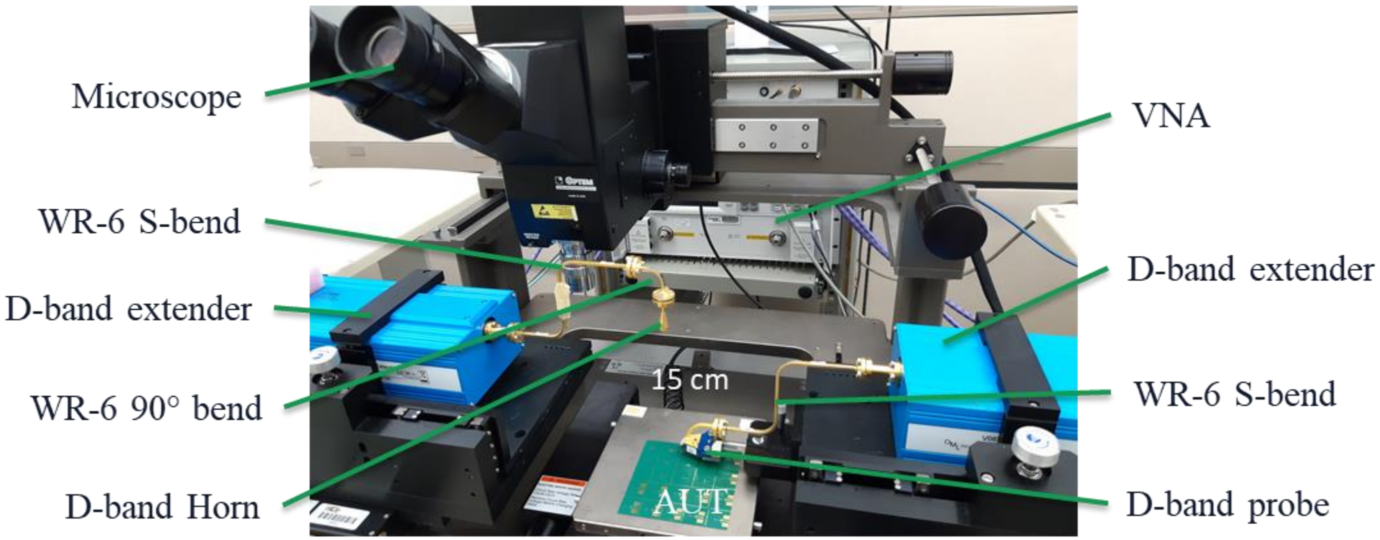
- ❑ $\lambda/2$ lattice for Antenna Array and interconnects (AiP)
- ❑ Enough elements to achieve appreciable gain
- ❑ 1dB or less loss between PA input and Antenna Array
- ❑ Efficient heat removal

Tx Antenna Array in Package (AiP): D-Band

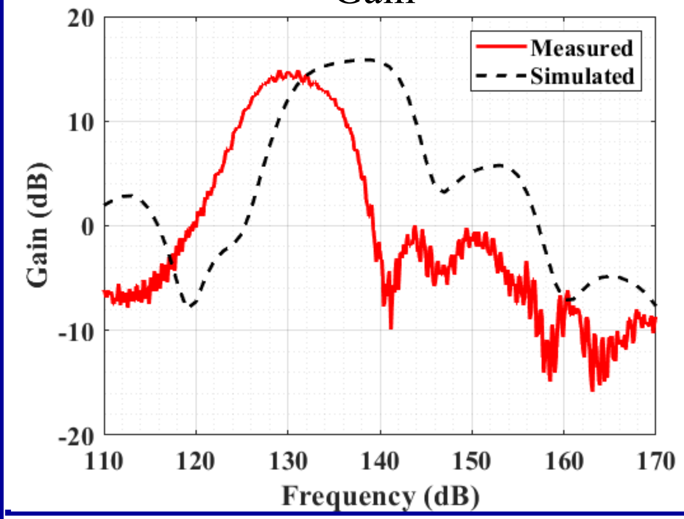
4x4 Array



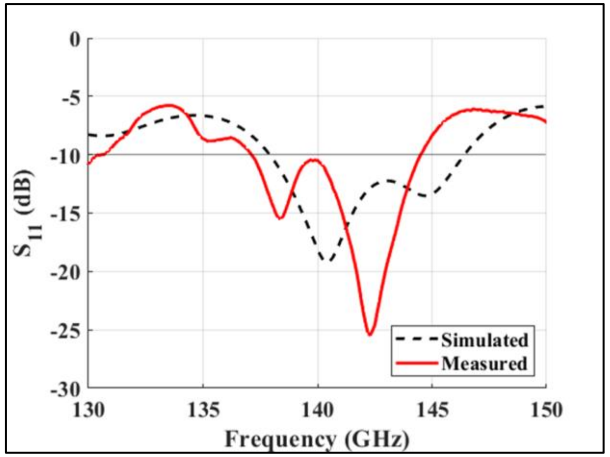




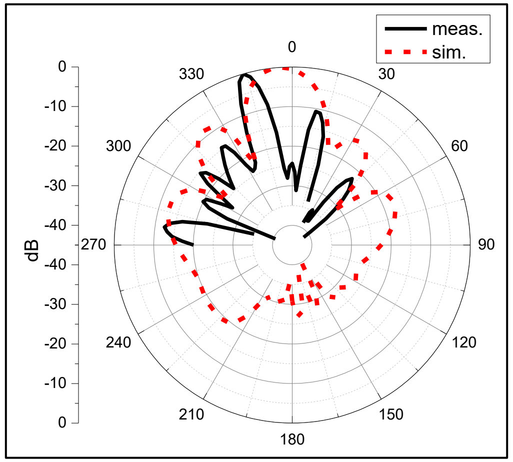
Gain



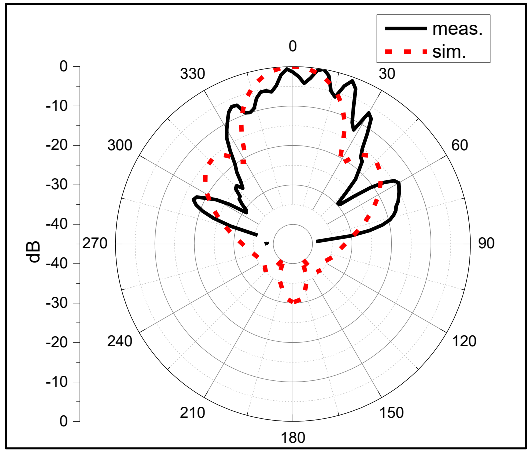
Return Loss



E-Plane

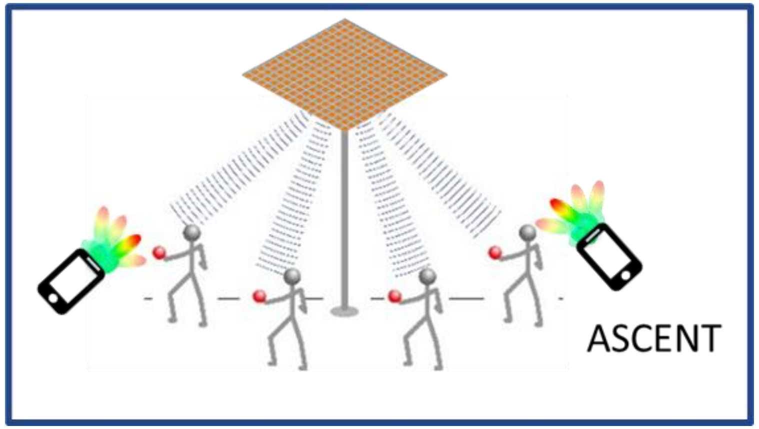


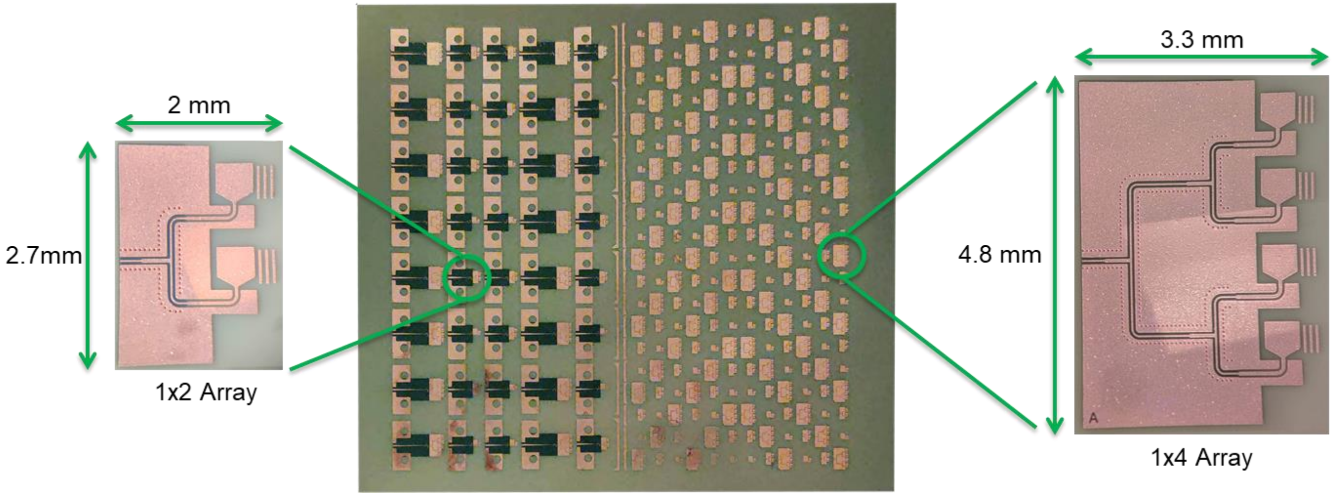
H-Plane

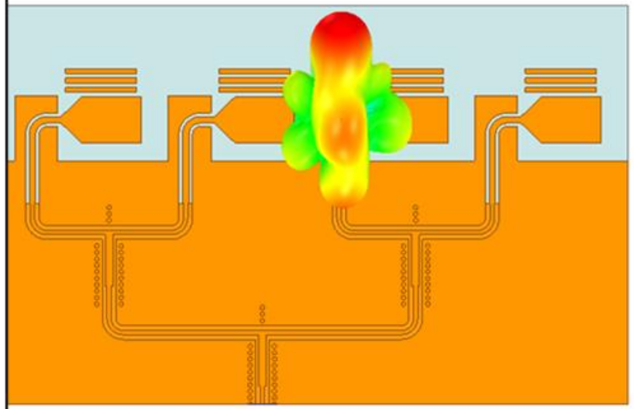


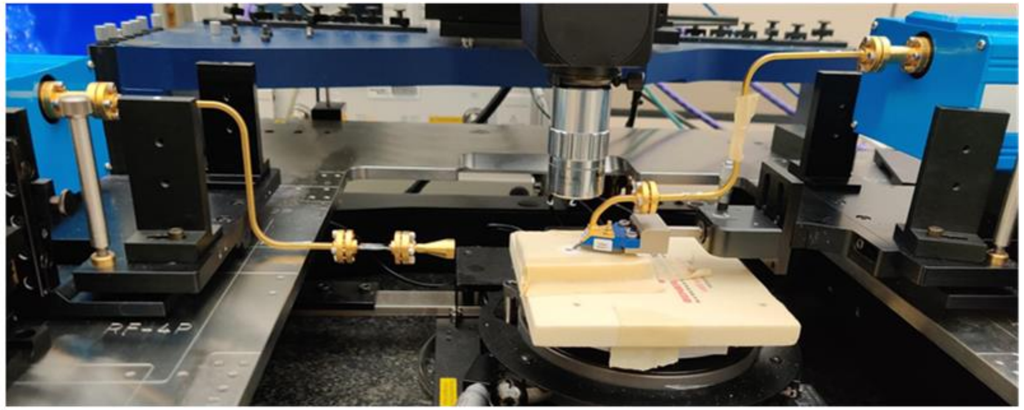
Kai-Qi Huang et al, ECTC 2021

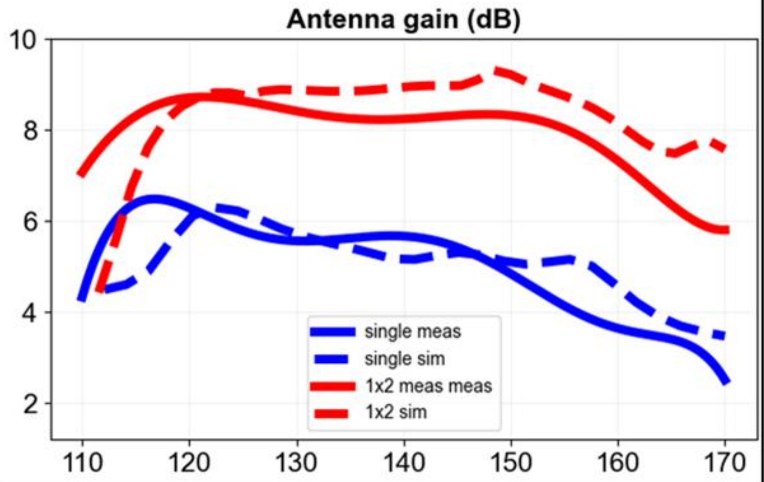
Rx Antenna Array in Package (AiP): D-Band





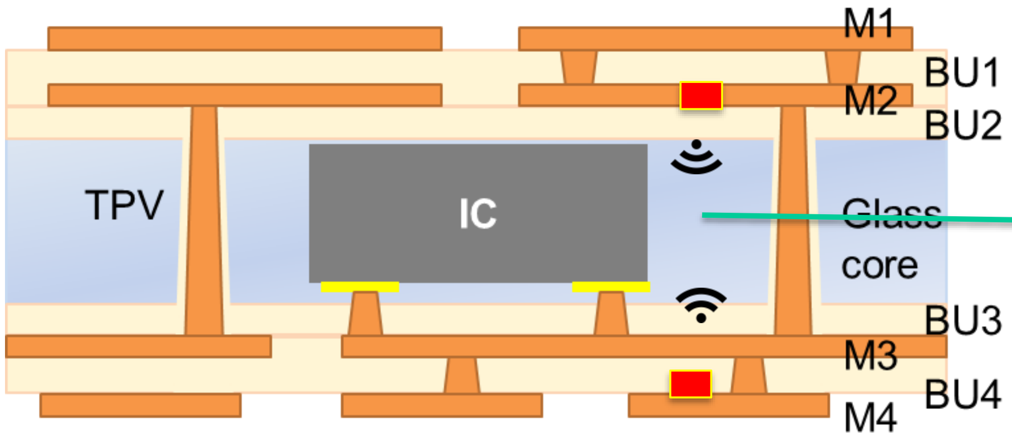






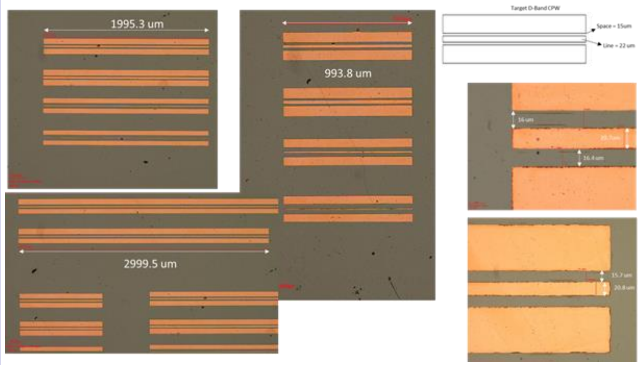
S. Erdogan et al, IMarC, 2021

D-Band (140GHz) Interconnects



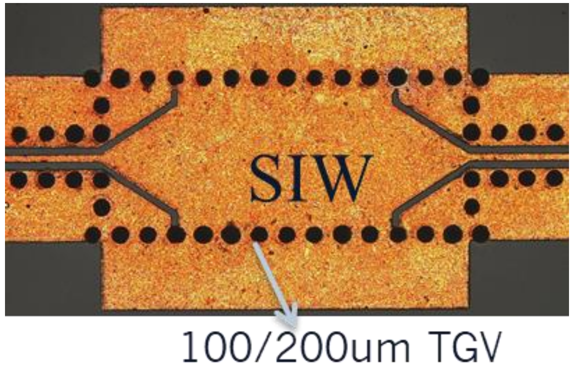
1. Co-planar Waveguide (CPW)
2. Microstrip (MS)
3. Substrate Integrated Waveguide (SIW)
4. Via-less Interconnect
5. Planar Goubau Lines (PGL)

CPW & MS



CPW Loss: 0.25dB/mm
MS Loss: 0.25dB/mm
0.43dB/mm *Mutee Rehman et al, CPMT 2021*

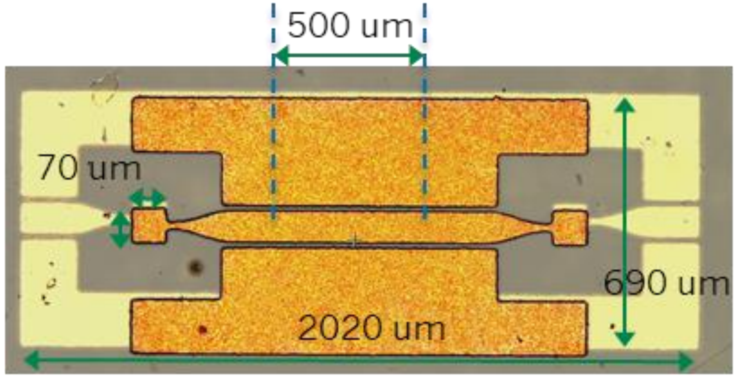
SIW



SIW Loss: 0.7dB/mm

Mutee Rehman et al, IMS 2021

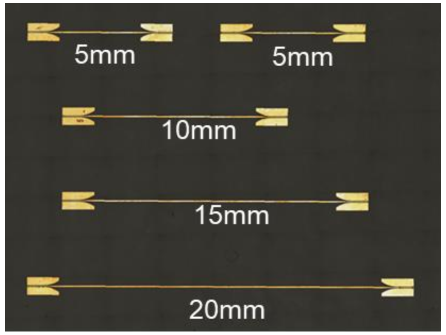
Via-less



Via-less Loss: 1.8dB

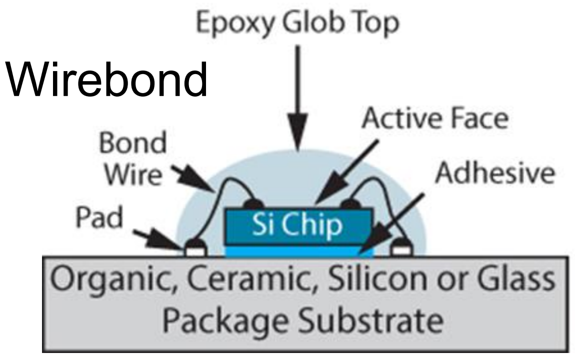
L. Vijaykumar et al, ECTC 2022

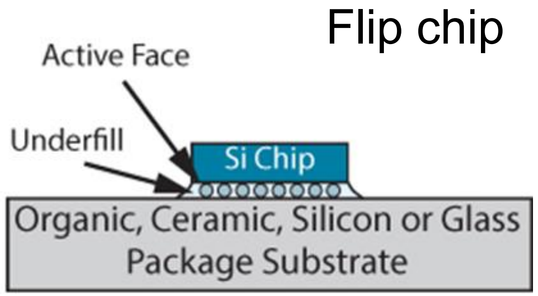
PGL



Goubau Loss:
0.34dB/mm
Xiaofan Jia et al, IMS 2022

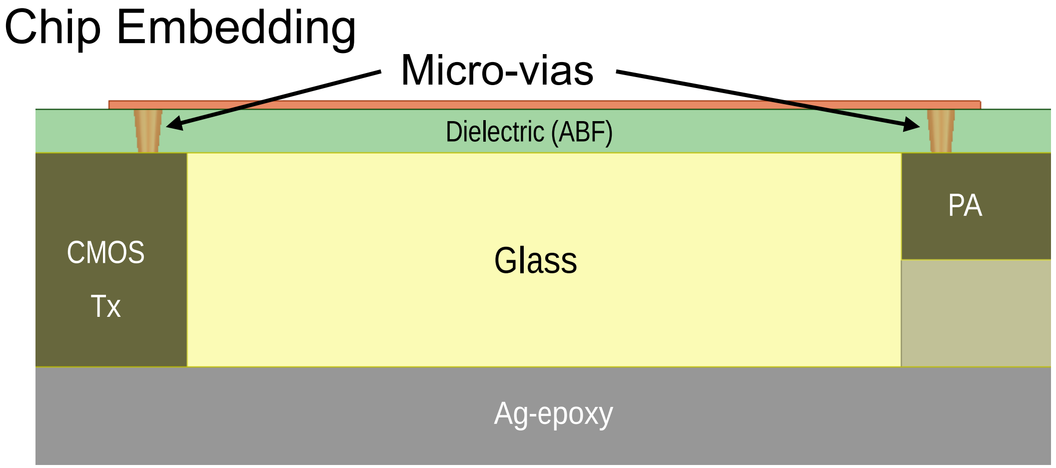
Reducing Loss by Eliminating Assembly



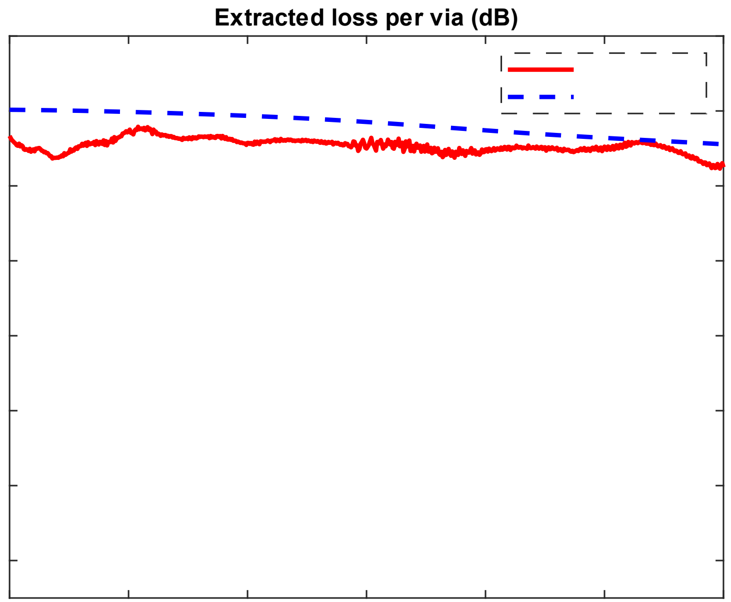


Rao Tummala, McGraw Hill, 2019

	Material	Interconnect type	Loss per interconnect
This work	ABF GL-102	Microvia	0.145 dB @ 140 GHz 0.177 dB @ 170 GHz
[15]	LTCC	Flip-chip	0.3 dB @ 165 GHz
[16]	Astra MT77	Flip-chip	0.3 dB
[10]	Astra MT77	Wirebonding	1.8 dB @ 140 GHz



No Assembly

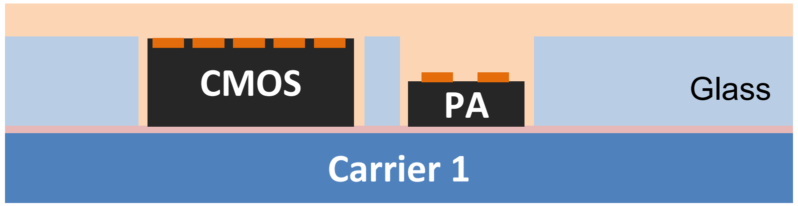


- ❑ RDL to Chip loss reduction!
- ❑ 0.15dB lower than Flip chip
- ❑ 1.65dB lower than Wirebond

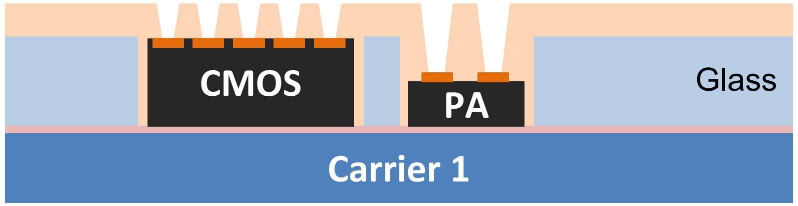
Serhat et al, ECTC, 2021

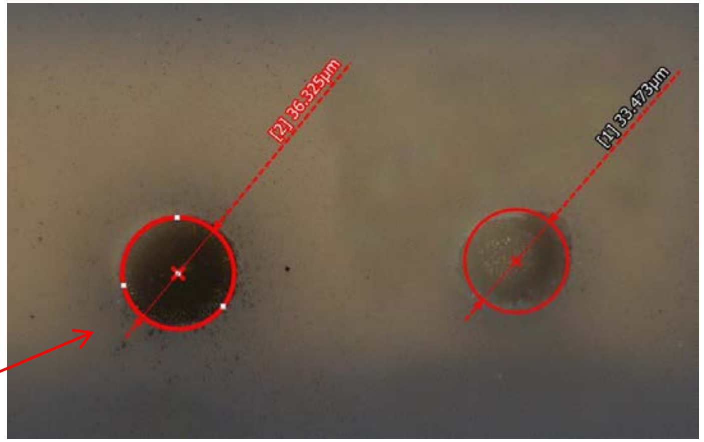
Embedded Heterogeneous Dies for mmWave

ABF Lamination



Via drilling

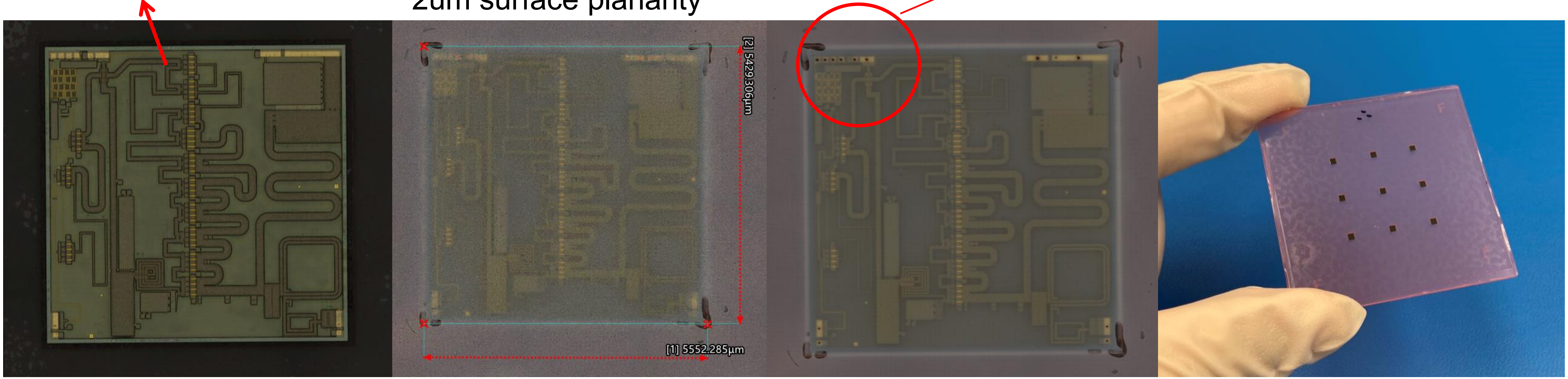




X. Jia et al, 2022 ECTC (under review)

Qorvo Die

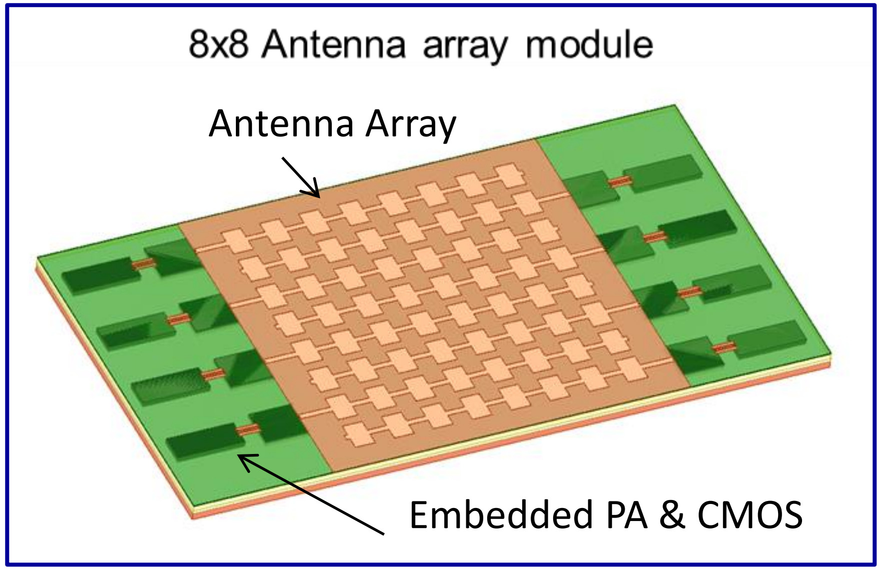
2um surface planarity

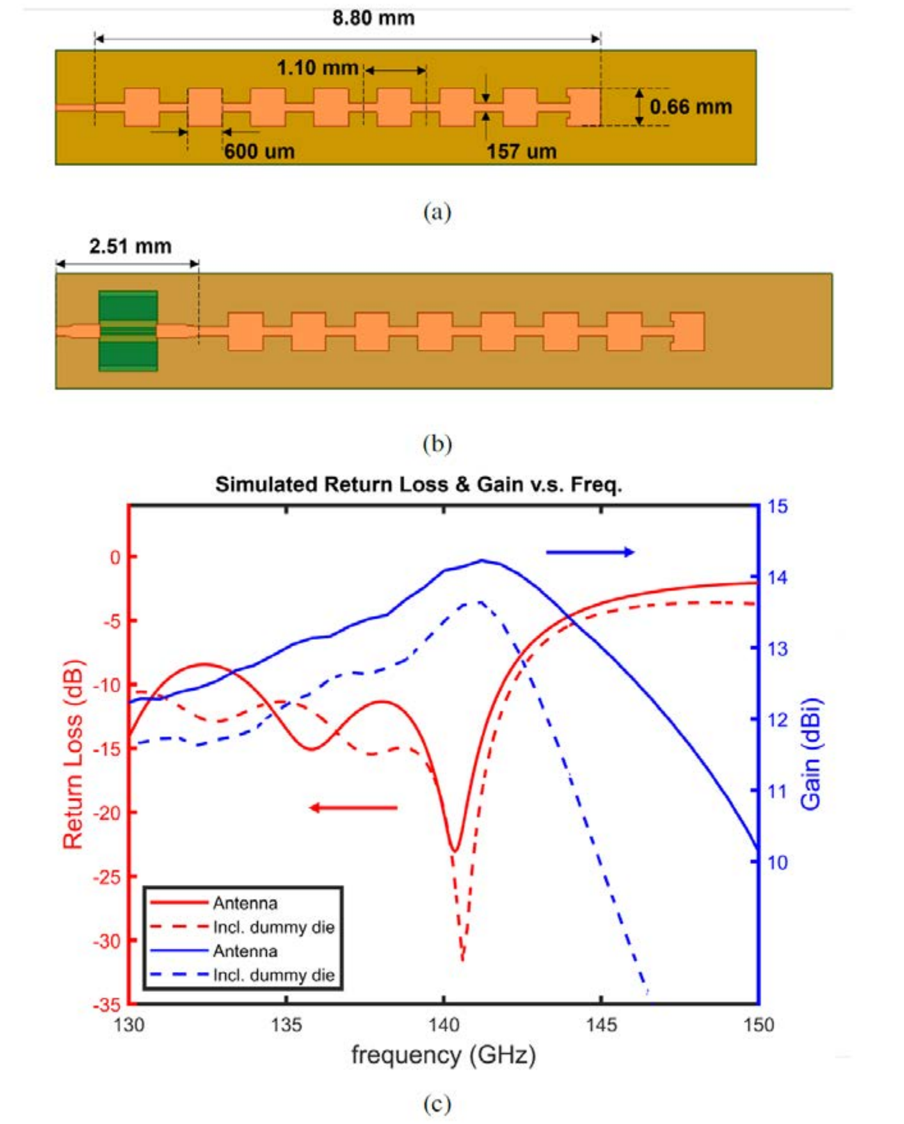


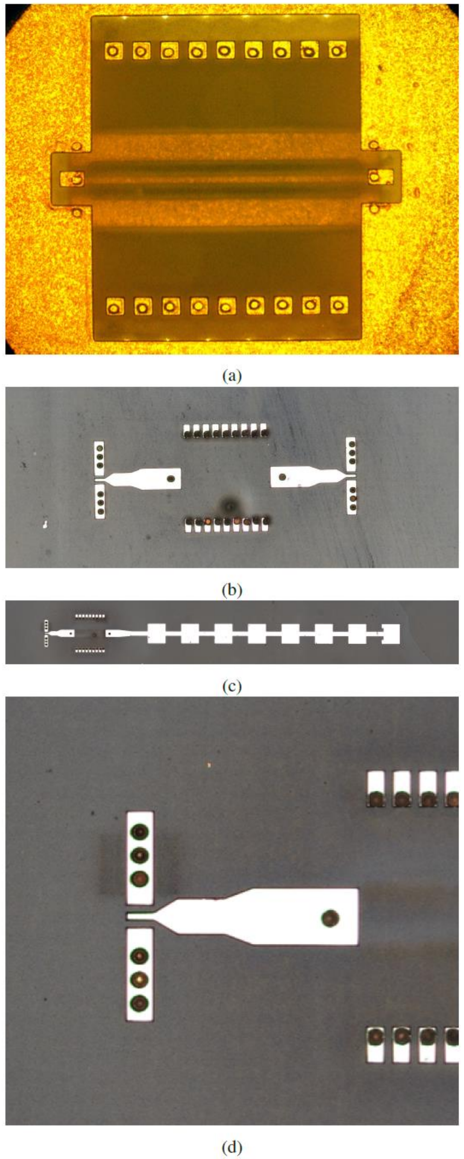
Before ABF lamination | 30um ABF GL102 laminated | Laser Via Drilling | Panel

Functional Antenna in Package Module (D-Band)

Mark Rodwell, UCSB

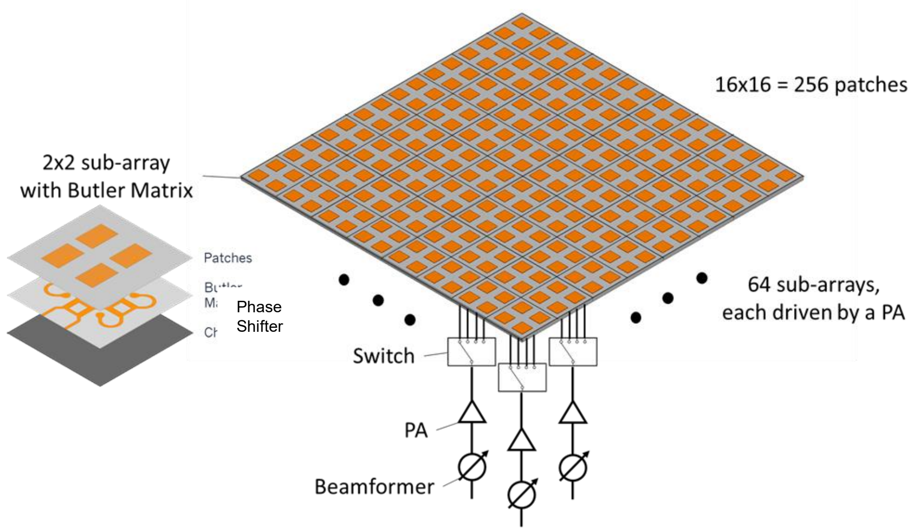




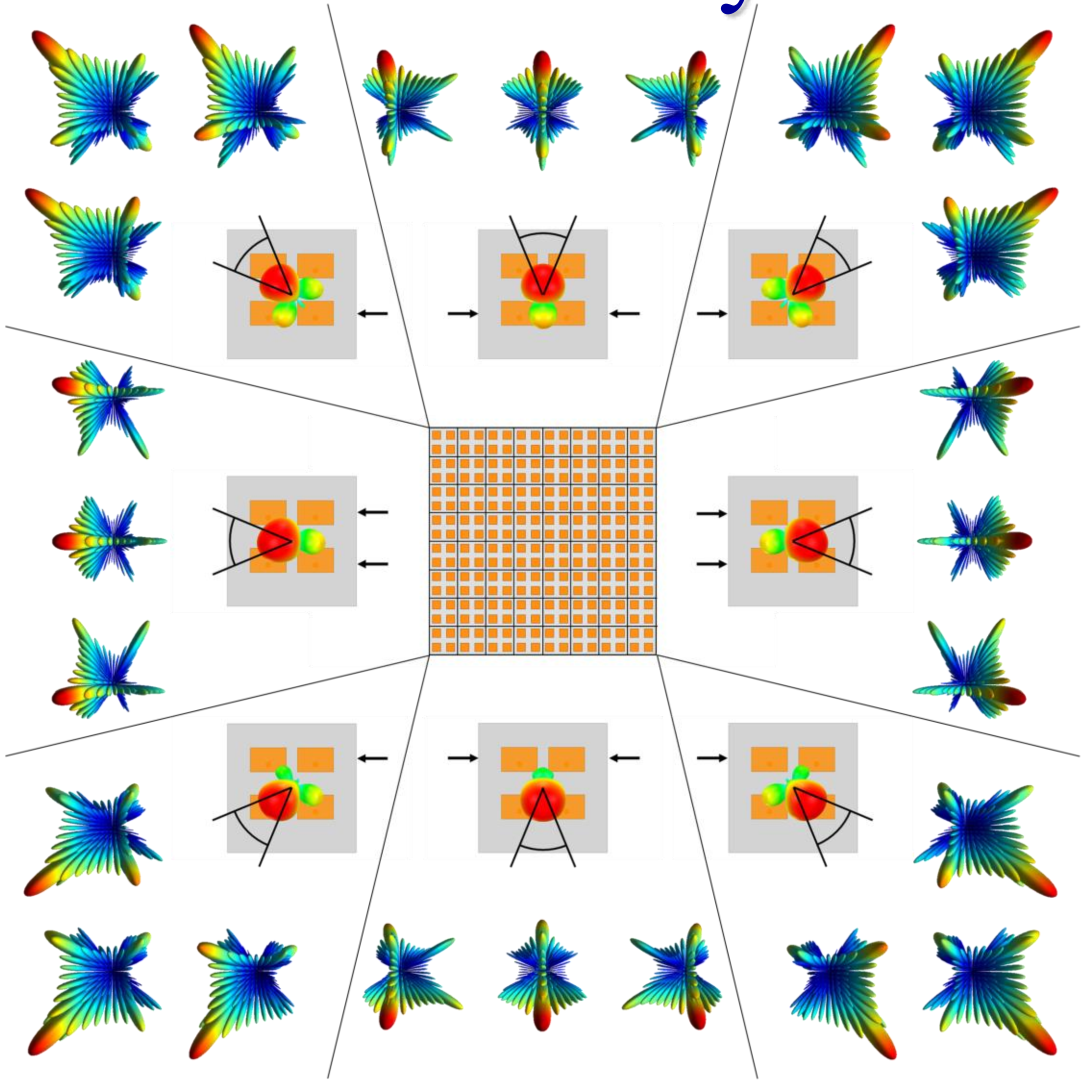


Xiaofan Jia et al, ECTC 2022

Hybrid Beamforming Tx Antenna Array

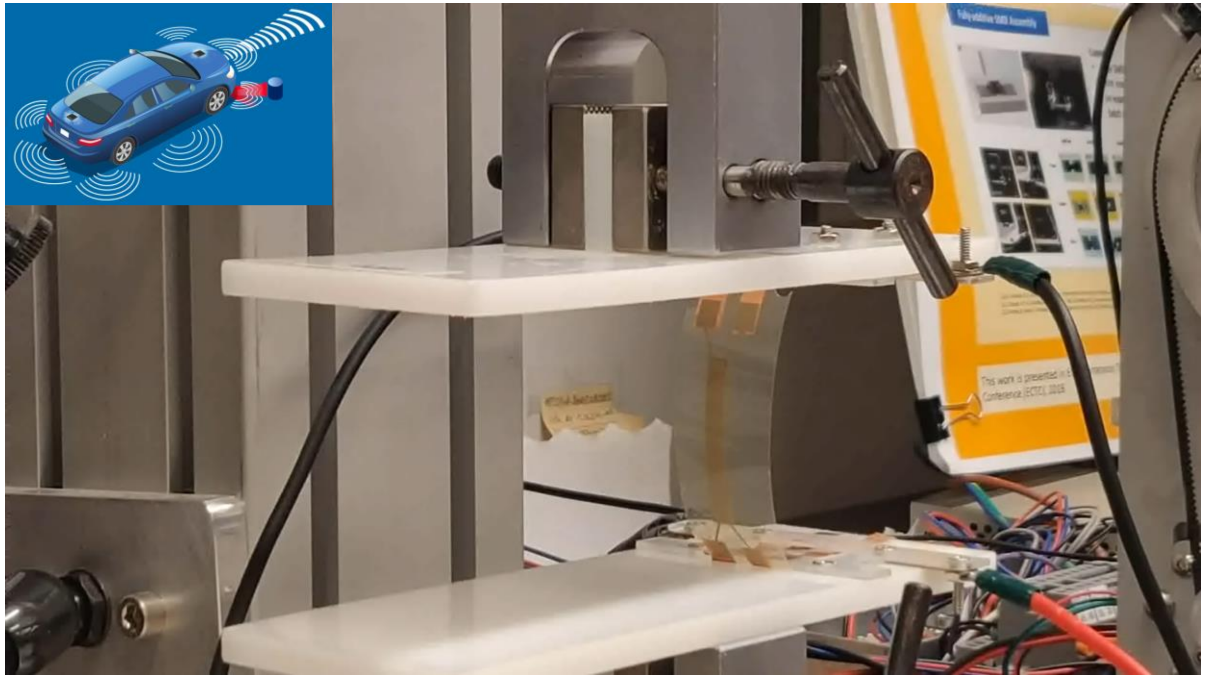


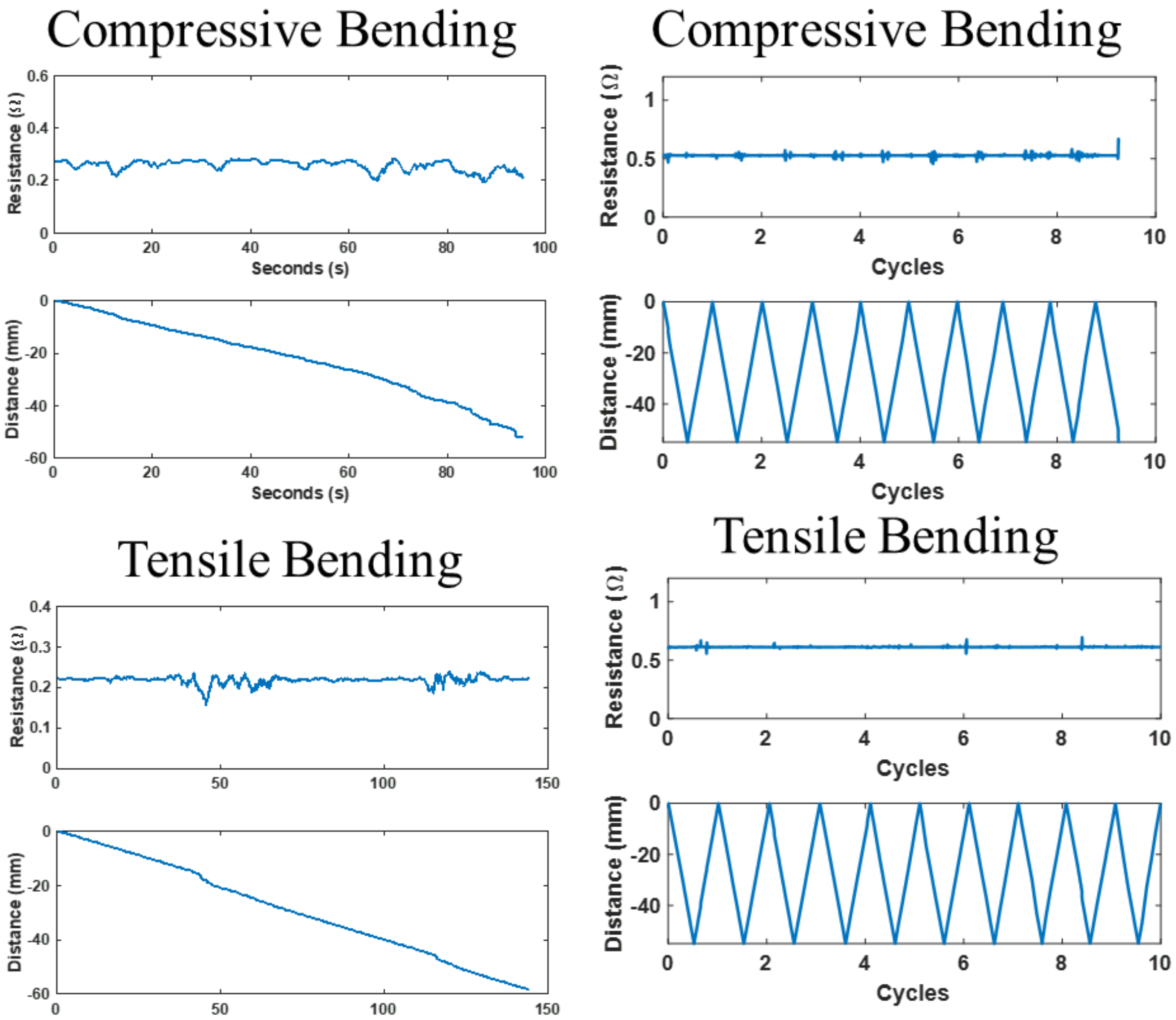
- Building Block: 2x2 sub-array
- Large Arrays using 2x2 sub-array
- Ex: 256 antenna elements using 64 (8x8) sub-arrays: Gain~25-28dBi (D-Band)
  - 8 basic beams
  - Active beamformers steer the beam in 2D within each 1/8 (azimuth) of the half space
- 64x32 elements (32x16 sub-array): Gain~36dBi



K. Huang & M. Swaminathan, APS, 2021

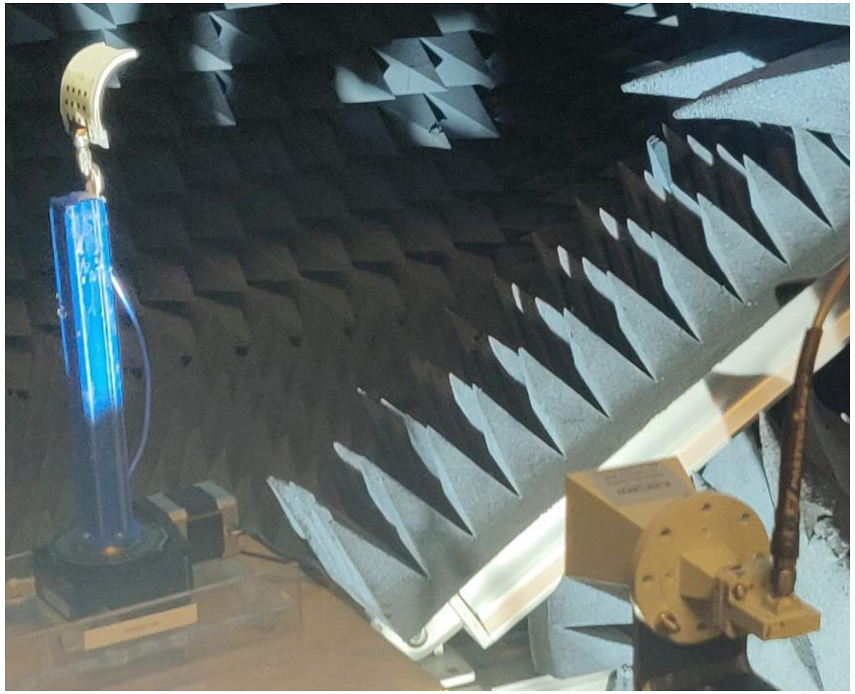
Electronics on Flexible Thin Glass

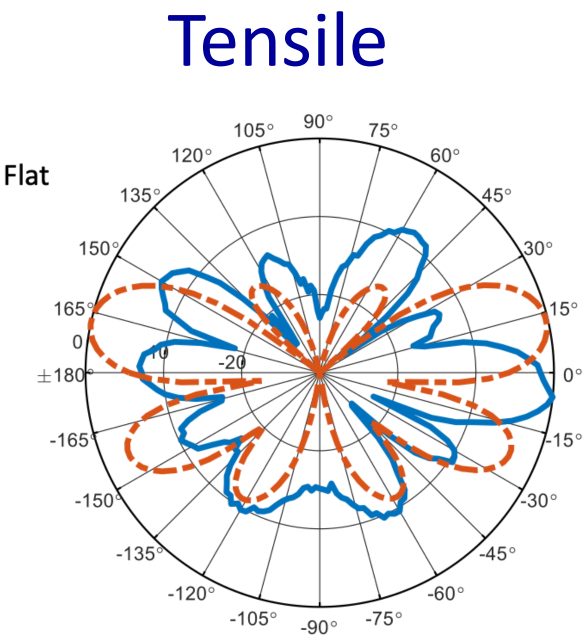


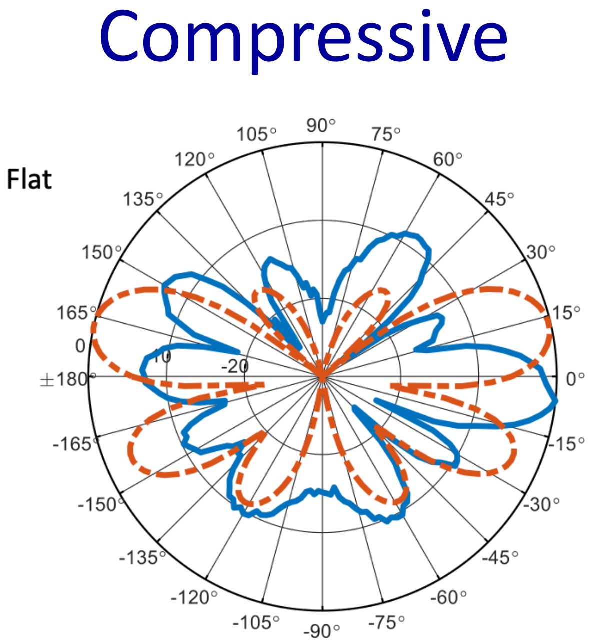


- ❑ Ultra-thin, flexible glass (30 µm Schott AF 32) on two different build up dielectrics (JSR GT-N01 and Taiyo PID)

Antenna on Thin Glass

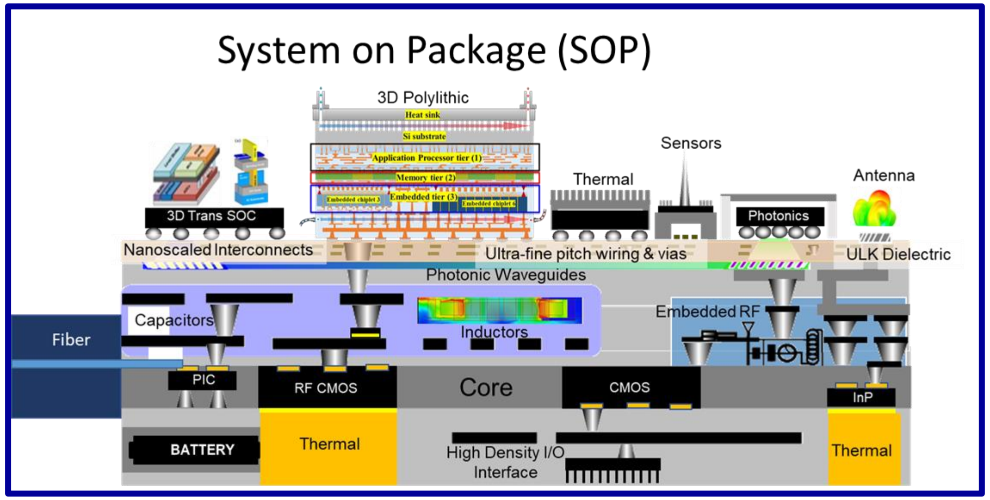


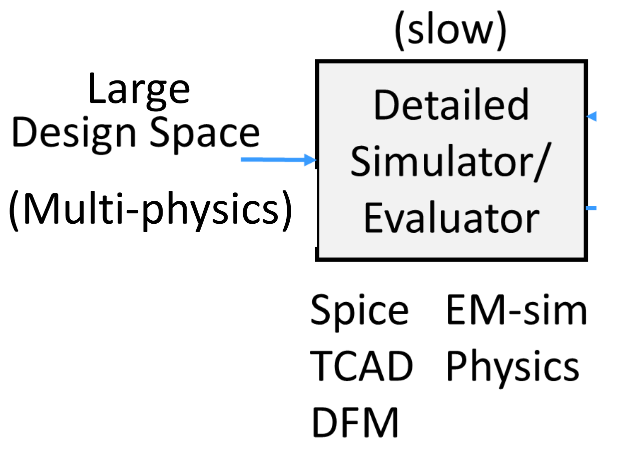




- ❑ 4x3 patch array; 3.05 mm (L) x 4.05 mm (W); 8.56 mm (S); 10dBi Gain
- ❑ 50 Ohm feed lines (135um width)
- ❑ Taiyo PID followed by SAP process
- ❑ Design frequency: 24GHz

Emerging Design Challenges

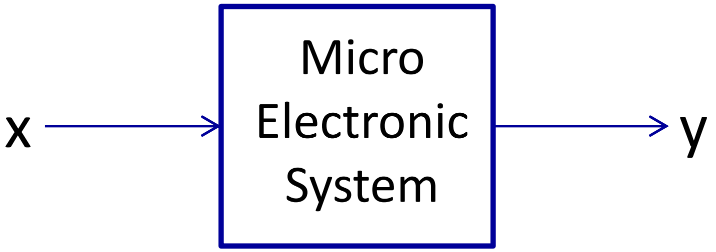




- <u>Fact</u>: Design Space can be large and exploring trade-offs can be painful.
- <u>Fact</u>: Simulators are slow and using them in design optimization has had only limited success.
- <u>Key Takeaway</u>: Why not re-think the Design process with a focus on Heterogeneous Integration & System Scaling?
- Can fast-to-evaluate "learned" model accurately replace detailed slow model in design and optimization?

M. Swaminathan, H. M. Torun, H. Yu, J. Hejase, and D. Becker, "Demystifying Machine Learning for Signal and Power Integrity Problems in Packaging", IEEE CPMT, 2020

Rethinking Design & Optimization



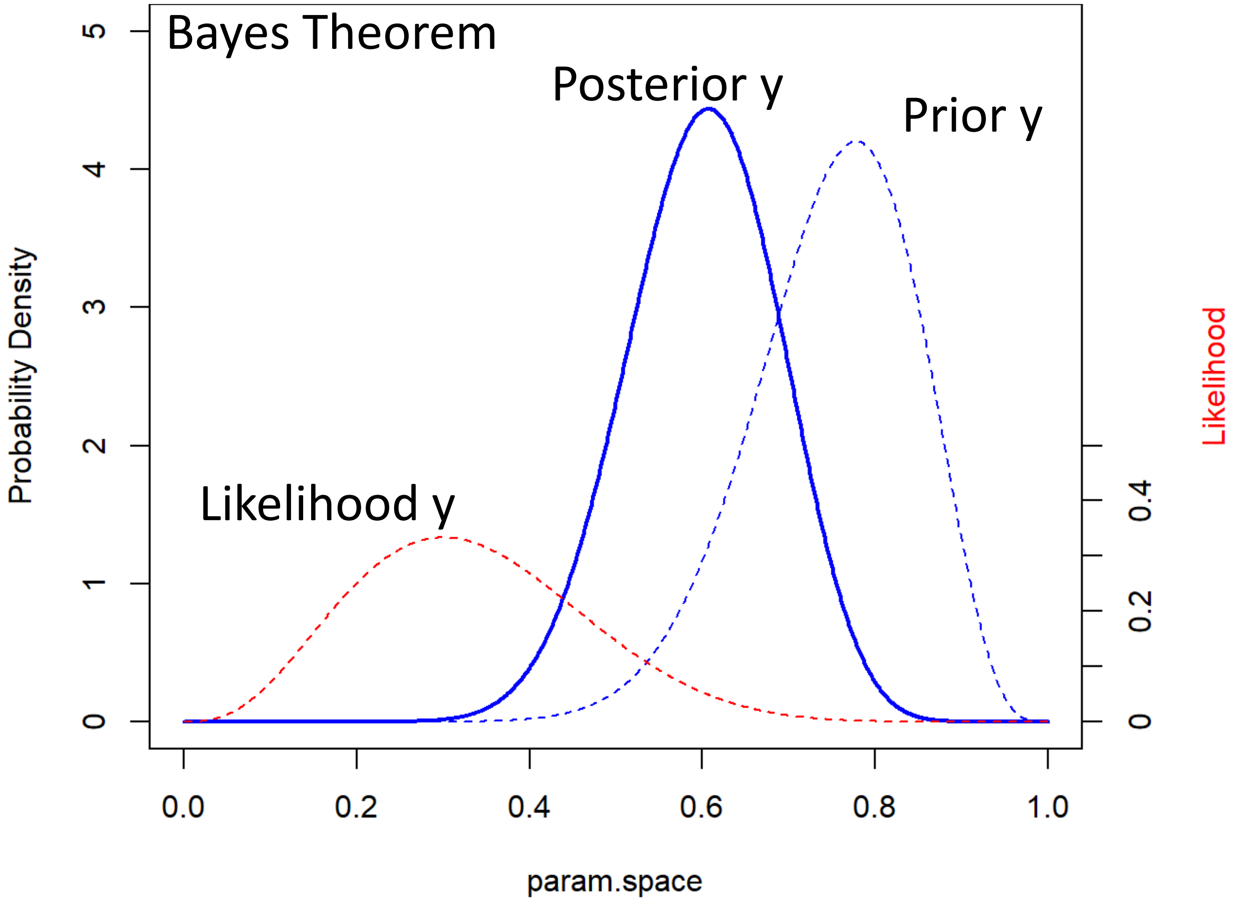
- Rather than using point simulations:

$$x \rightarrow y$$

- Why not repose the problem using probabilities:

$$x \rightarrow P(y|x)$$

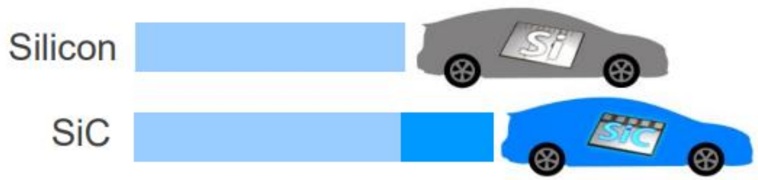
- Machine Learning provides enormous opportunities here for searching design spaces and design optimization.
- Establish confidence in the predictions and solutions by establishing confidence bounds.

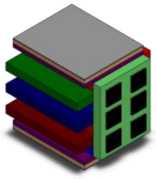


https://kevintshoemaker.github.io/NRES-746/LECTURE6.html

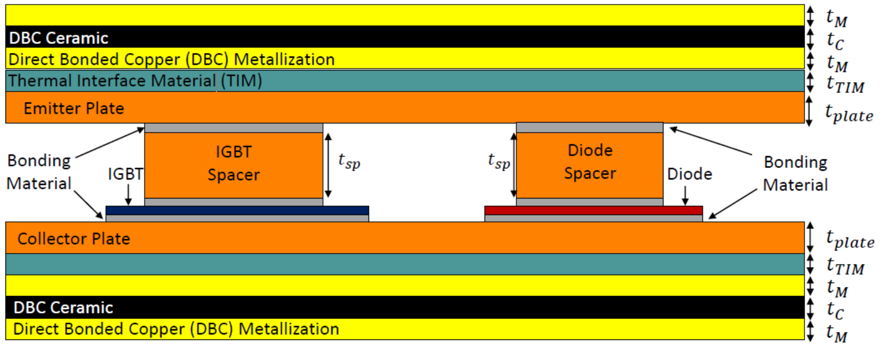
M. Swaminathan, H. M. Torun, H. Yu, J. Hejase, and D. Becker, "Demystifying Machine Learning for Signal and Power Integrity Problems in Packaging", IEEE CPMT, 2020

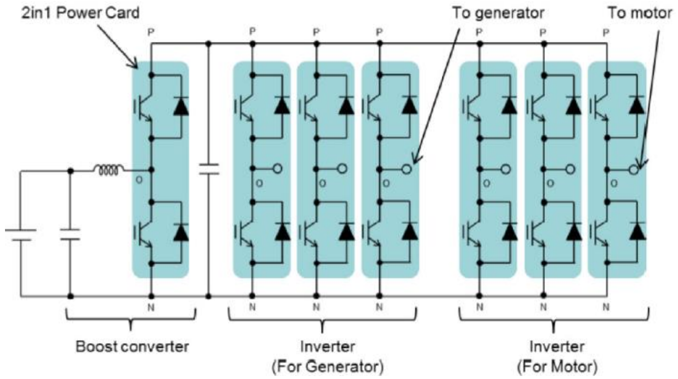
Inverters for Electric Vehicles





Denso Half-Bridge Module





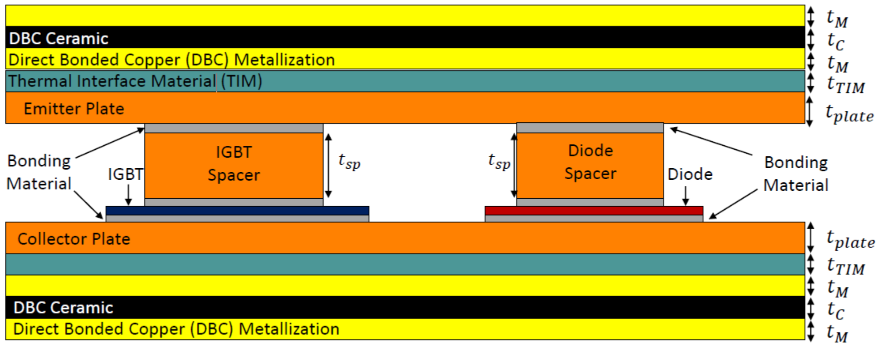
- ❑ **3D package architectures**
- ❑ **Integrated cooling**
- ❑ **Material Innovations**

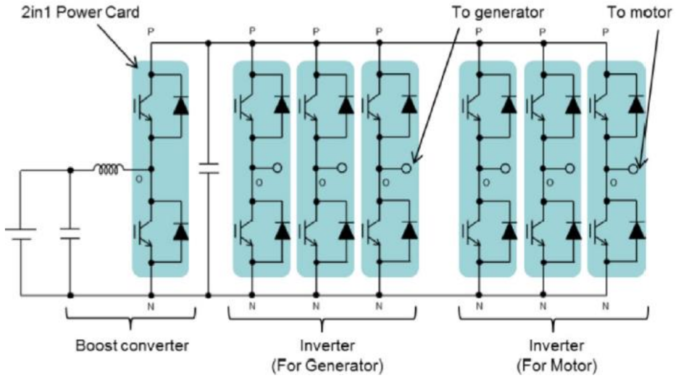
- ❑ What is the appropriate package architecture, geometries & materials for half-bridge inverter power modules for electric vehicles?
- ❑ Electrical-Mechanical-Thermal <u>multi-physics simulations</u> required for Co-Design!

Collaboration with Vanessa Smet, GT

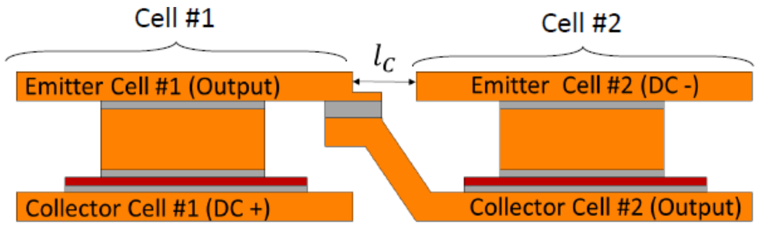
Inverter Module

Denso Half-Bridge Module

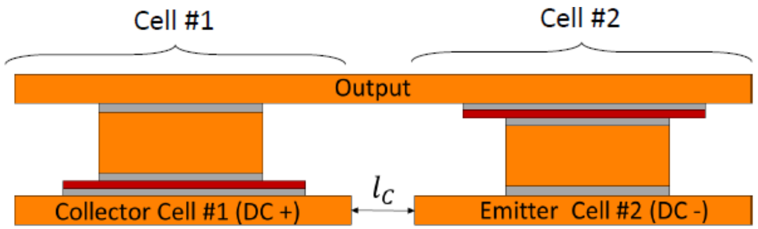




Package Architecture #1



Package Architecture #2



Mixed-Variable Parameter Space

Parameter	Type	Unit	Min	Max
Plate Thickness	Cont.	mm	0.2	3
TIM Thickness	Cont.	mm	0.1	1
Ceramic Thickness	Cont.	mm	0.25	2
Metallization	Cont.	mm	0.25	2
Spacer Thickness	Cont.	mm	0.2	3
Di/IGBT Spacing	Cont.	mm	2	8
Plate Clearance	Cont.	mm	0.2	3
Cell Separation	Cont.	mm	2	10
Package Architecture	Cat.		U-Structure, N-Structure	
Cooling h	Cat.	$\frac{W}{m^2K}$	[1000, 5000, 10000]	
Conductor	Cat.		Cu, Al	
Ceramic Material	Cat.		Al_2O_3, AlN, BeO, Si_3N_4	
Bond Material	Cat.		Solder, Sintered Silver, Epoxy Paste	

: Thickness Related
: Layout Related

Continuous Parameters

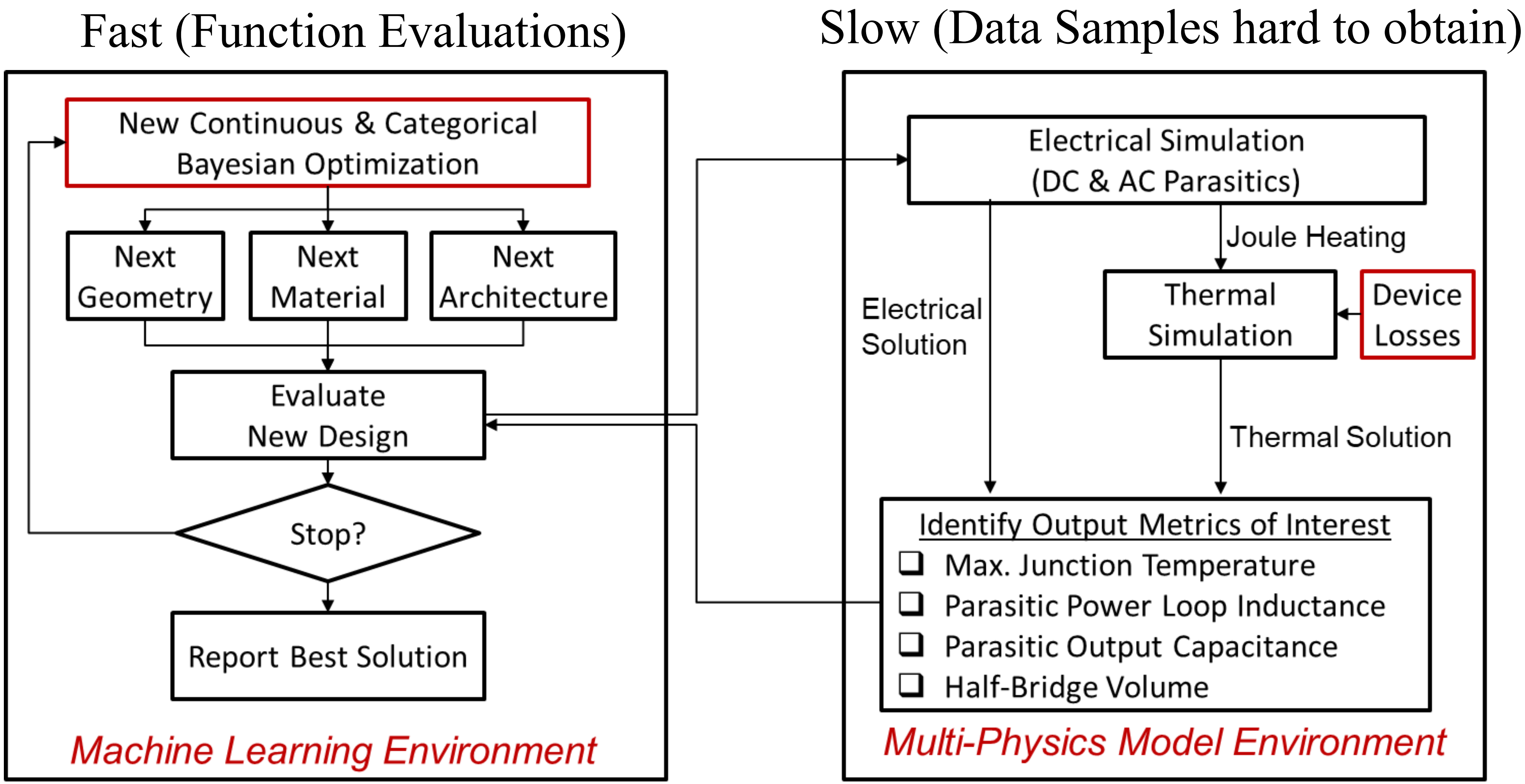
: Material
: Package Architecture

Categorical Parameters

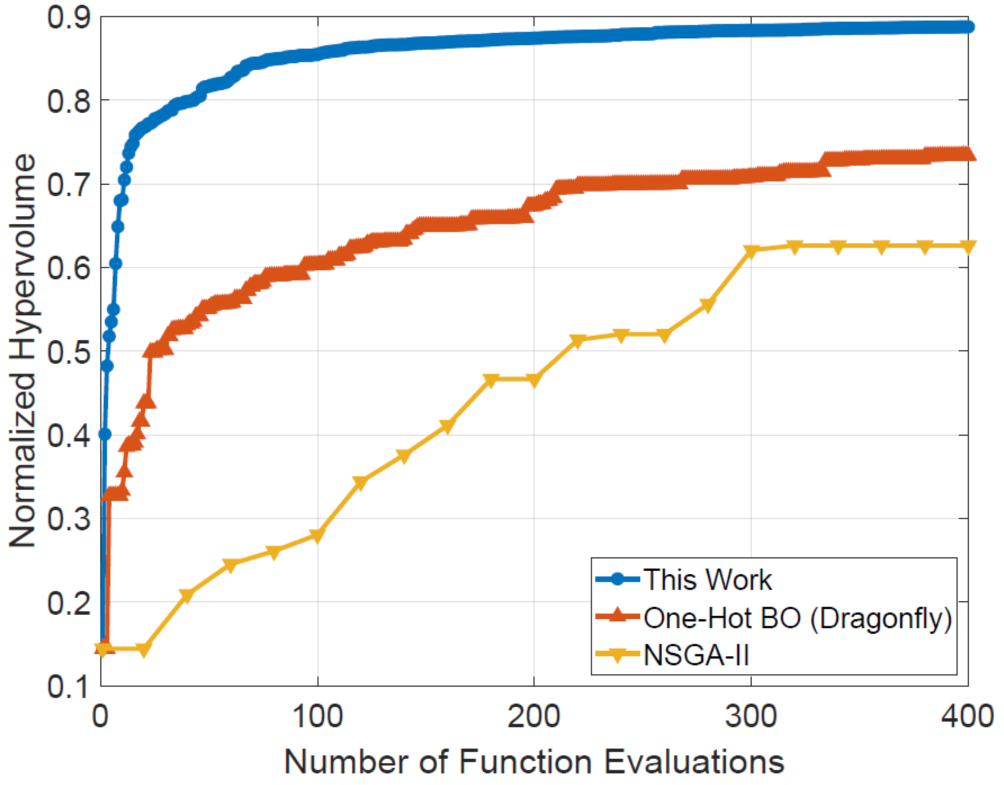
- 4 objectives to minimize (Pareto Front): Parasitic inductance, parasitic capacitance, package volume, temperature.
- 8 continuous, 5 categorical parameters (Total 144 combinations).
- Data generation through electrical-thermal multi-physics simulations.

Torun et al., IEEE Access, under review.

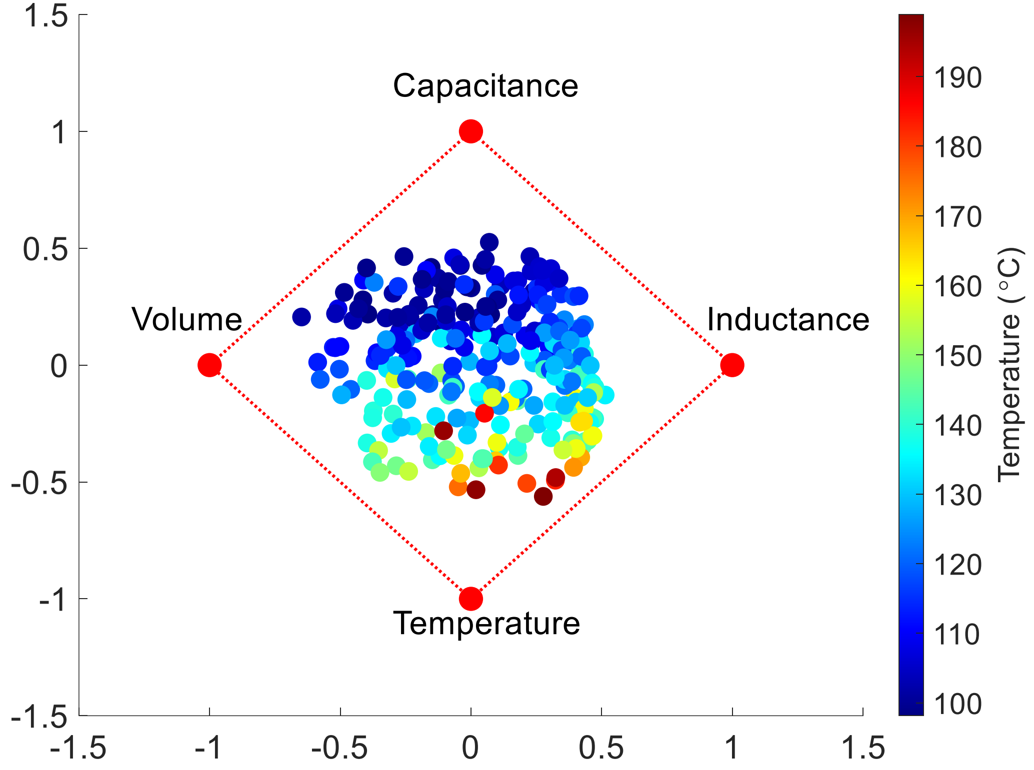
Optimization Environment



Inverter Module Results



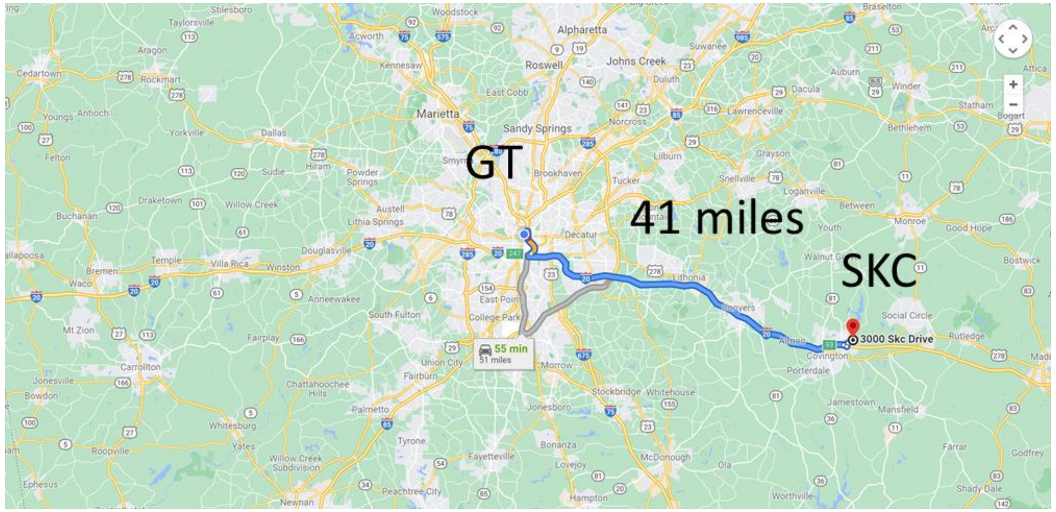
Radial Visualization of the 4-D Pareto Front



- ❑ Imagine ML predicting the best package architecture with the appropriate materials & geometries.
- ❑ Optimized design has up to (compared to hand-tuned design):
  - **68.7%** reduced package volume.
  - **29.4%** reduced parasitic capacitance.
  - **2.7%** reduced max. junction temperature.

H. Torun, Ph.D. thesis, 2021

Recent Translational Activities



- ❑ SK Group to Locate First of its Kind Glass-based Semiconductor-part Venture in Covington, GA (based on GT-PRC research)
- ❑ Announcement by Governor Brian P. Kemp (Atlanta, GA – October 28, 2021)
- ❑ Company will invest more than $473 million in this unprecedented venture and will create more than 400 new jobs in Newton County

https://www.georgia.org/press-release/sk-group-locate-first-its-kind-glass-based-semiconductor-part-venture-covington

Qorvo® Wins U.S. Government Project to Create Advanced, State-of-the-Art, RF Semiconductor Packaging Center

GREENSBORO, NC – November 5, 2020 – Qorvo® (Nasdaq:QRVO), a leading provider of innovative RF solutions that connect the world, has been selected by the U.S. government to create a State-of-the-Art (SOTA) Heterogeneous Integrated Packaging (SHIP) RF production and prototyping center. The SHIP program will ensure that microelectronics packaging expertise and leadership is available for both U.S. defense contractors and commercial clients that require design, validation, assembly, test and manufacturing of next-generation RF components.

The exclusive SHIP Other Transaction Agreement (OTA), worth up to $75 million, was awarded to Qorvo by the Naval Surface Warfare Center (NSWC), Crane Division. This program is funded by the Office of the Undersecretary of Defense for Research and Engineering's (OUSD R&E) Trusted and Assured Microelectronics Program (T&AM), and is administered by the Strategic & Spectrum Missions Advanced Resilient Trusted System (S²MARTS) Other Transaction Agreement (OTA), managed by National Security Technology Accelerator (NSTXL).

Under the SHIP program, Qorvo will design and deliver the highest levels of heterogeneous packaging integration. This is essential to meet the size, weight, power and cost (SWAP-C) requirements for next-generation phased array radar systems, unmanned vehicles, electronic warfare platforms and satellite communications.

James Klein, president of Qorvo Infrastructure and Defense Products, said, "We are honored to be selected to establish state-of-the-art RF packaging capability for the U.S. Department of Defense (DoD). This award reflects Qorvo's proven track record as a global leader in RF technology with over 35 years of experience. As part of this collaboration, Qorvo will expand its proven capabilities in Texas to create a SOTA facility that best serves the needs of the U.S. government and commercial customers."

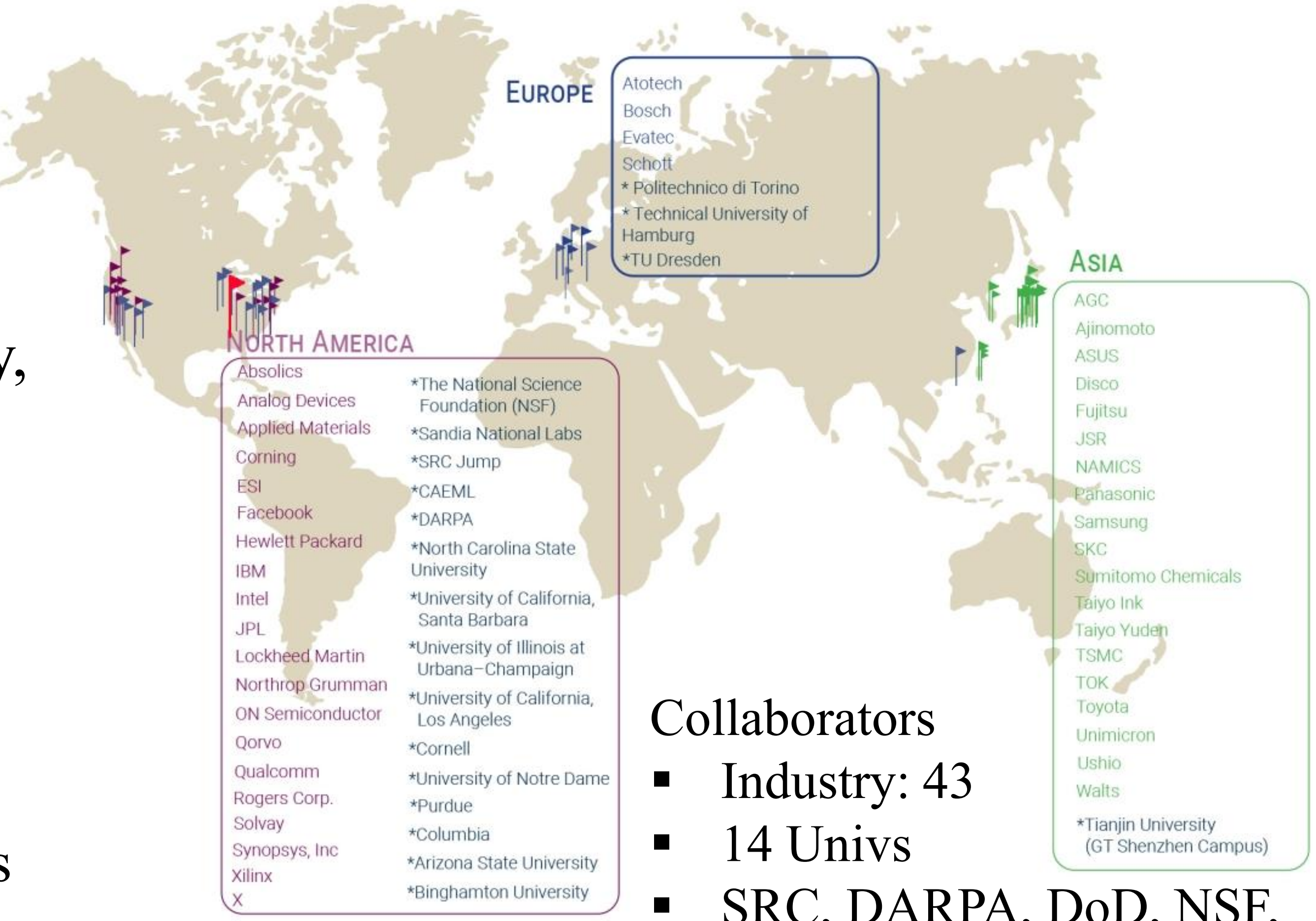
Qorvo's U.S.-based capabilities include advanced manufacturing, packaging and testing for both high- and low-power applications ranging from DC to

- ❑ Qorvo wins SHIP RF Center
  - ▪ $75M from US Government
  - ▪ GT-PRC will focus on Glass Based Advanced Packaging for RF (Start Date: Mar. 2022)

https://www.qorvo.com/newsroom/news/2020/qorvo-wins-us-gov-project-to-create-advanced-state-of-the-art-rf-semiconductor-packaging-center

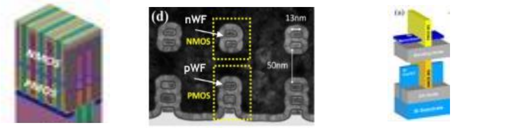
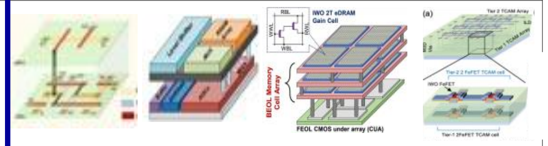
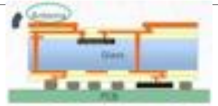
Packaging Research Center (PRC) – A Snapshot

- ❑ Graduated NSF Engineering Research Center (in its 28th year)
- ❑ Research, Education & Workforce development in heterogeneous integration, advanced packaging and system miniaturization.
- ❑ Design, Materials, Process, Assembly, Reliability, Thermal & System Integration.
- ❑ Center team:
  - 29 faculty from five schools (ECE, MSE, ME, ChBE, CS)
  - 11 research/administrative staff
  - 60+ graduate/undergraduate students
  - Visiting engineers.



Collaborators
- Industry: 43
- 14 Univs
- SRC, DARPA, DoD, NSF, iNEMI, Semi

The Future ….

Category	Granularity	Technology	Interconnect Density (mm^{-2})	Examples
3D Transistor (before M1)	**Transistor**	▪ **Epitaxial growth** ▪ **Stacked nanosheet** ▪ **Sequential Integration** ▪ ***in situ* dep and anneal** ▪ **layer transfer & bonding**	**10^9**	 C-FET; Stacked Nanosheet; Ge nanosheet PMOS on FinFET NMOS
Monolithic 3D (after M1)	**Gate, Block**	▪ **Sequential Integration** ▪ ***in situ* dep and anneal** ▪ **layer transfer & bonding**	**$>10^8$**	 3D Transpose SRAM; 3D RRAM; 3D eDRAM; 3D FeFET TCAM
Polylithic 3D (W2W bonding)	**Block, Chiplet**	▪ **Parallel Integration** ▪ **Hybrid bonding** ▪ **Metal ALD**	**10^6 -10^8**	 SiO2-reconstituted tier in the BEOL
Heterogeneous 2.5/3D Packaging	**Chiplets, Modules**	▪ **3D Packaging**	**10^4 – 10^5**	 Stacked and assembled chiplets on glass interposer

Transistors

Packaging

Adapted from Suman Datta, U. Notre Dame

- ❑ Addressing multiple length scales critical.
- ❑ THE FUTURE IS ABOUT **SCALING SEMICONDUCTOR SYSTEMS** THROUGH BOTH **PACKAGE** & **TRANSISTOR** SCALING. **LET'S START NOW**!

Thank You

Join us in our Journey!

www.prc.gatech.edu