Recent Advances and Trends in Advanced Packaging

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eps.ieee.org
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Transactions on CPMT
- 595 submissions (2020)
- 240 papers published
- Impact Factor: ~ 1.7 (2020)
- Xplore Usage: 40,000+

VP Publications – Dr. Ravi Mahajan, Intel
CPMT Transactions, Monthly eNewsletter, and Bi-Annual printed Newsletter
EPS Awards & Recognition

IEEE Electronics Packaging Award
(IEEE Technical Field Award)

Outstanding Sustained Technical Contribution Award

Electronics Manufacturing Technology

David Feldman Outstanding Contribution

Exceptional Technical Achievement

Outstanding Young Engineer

Transactions Best Papers

Regional Contributions

PhD Fellowship
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➢ Advanced Packaging
  ● 2D IC Integration
  ● 2.1D IC Integration
  ● 2.3D IC Integration
  ● 2.5D IC Integration
  ● 3D IC Integration

➢ Chiplet Design and Heterogeneous Integration (HI) Packaging
  ● Chip partition and integration
  ● Chip split and integration
  ● Multiple System and Integration
  ● HI on Organic Substrates (SiP)
  ● HI on Silicon Substrates (Passive/Active TSV-Interposers)
  ● Lateral Communication between Chiplets (e.g., Bridges)
  ● HI on Fan-Out (Chip-First) RDL-Substrates/Interposers
  ● HI on Fan-Out (Chip-Last) RDL-Substrates/Interposers
  ● HI on Ceramic Substrates

➢ Summary

➢ Q&A
The Biggest Difference between Chiplet and Heterogeneous Integration:

- Chiplet is a Chip Design Method
- Heterogeneous Integration is a Chip Packaging Method
Semiconductor Packaging Technologies

Semiconductors (Regular, SoC, Chiplets, etc.)

- Single chip
- Multichip
  - Thin-Film or Bridge
  - Inorganic or Organic TSV-less Interposer
  - Passive TSV-Interposer
  - Active TSV-Interposer

Conventional Packaging

- COB or DCA
- fcCSP
- PBGA

Package Substrate (Carrier)

- 2D
- 2.1D
- 2.3D
- 2.5D
- 3D

PCB
Conventional Packaging: Direct Chip Attach (DCA) and Flip Chip Ball Grid Array (fcBGA)
Groups of Advanced Packaging: 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration

Semiconductors (Regular, SoC, Chiplets, etc.)

- Single chip
- Multichip
  - Thin-Film or Bridge
  - Inorganic or Organic TSV-less Interposer
  - Passive TSV-Interposer
  - Active TSV-Interposer

Advanced Packaging

Package Substrate (Carrier)

- COB or DCA
- fcCSP
- PBGA
- 2D
- 2.1D
- 2.3D
- 2.5D
- 3D
- PCB
Advanced Packaging Ranking According to Their Density and Performance

Interconnect Density

Electrical Performance

- Bumpless Chiplets 3D IC Integration
- Bumpless 3D IC Integration
- μBump Chiplets 3D IC Integration
- μBump 3D IC Integration
- 2.5D (C2 or μBump) IC Integration
- 2.5D (C4 or solder bump) IC Integration
- 2.3D Fan-Out (Chip-Last) IC Integration
- 2.3D Flip Chip IC Integration
- 2.3D Fan-Out (Chip-First) IC Integration
- 2.1D Fan-Out IC Integration with Bridge
- 2.1D Flip Chip IC Integration with Bridge
- 2.1D Flip chip IC Integration
- 2D Fan-Out (Chip-Last) IC Integration
- PoP, SiP
- 2D Flip Chip IC Integration
- 2D Fan-Out (Chip-First) IC Integration
Advanced Packaging

➢ 2D IC Integration
➢ 2.1D IC Integration
➢ 2.3D IC Integration
➢ 2.5D IC Integration
➢ 3D IC Integration
2D IC Integration

➢ 2D (Flip Chip) IC Integration

➢ 2D (Fan-Out) IC Integration
  ● Chip-First die Face-Down
  ● Chip-First die Face-Up
  ● Chip-Last (RDL-First)
2D (Flip Chip / Wirebond) IC Integration

(a) Flip Chip Bump

Chip1

Chip2

Build-up Package Substrate

Solder Joint

PCB

(b) Encapsulation

Flip Chip Bonding

Wire Bonding

Build-up Package Substrate

Solder Ball

PCB
2D (Fan-Out) IC Integration: Chip-First (Die Face-Down)

There is no substrate which is replaced by RDLs (redistributed-layers).
Heterogeneous Integration of Mini-LEDs for RGB-display (Chip-First Die Face-Down)

Not-to-Scale

LED

Solder Joint

Solder Mask

Cu Pad

PCB

RDLs

EMC (ABF)

Driver

Solder Joint

LED

RDLs

PCB

EMC (ABF)

Solder Joint

IEEE Trans. on CPMT, 2021
Fan-Out Chip-First (Die Face-Up)

Reconstituted Wafer (325 packages)

Chip (10mm x 10mm)

Package

Solder balls on package

Chip corner

Pads on package for TMV

Contact-Pad

CHIP

RDL1

UBM-less Pad

V₁₂

RDL2

Vc₁

RDL3

V₂₃

Solder ball

RDL1 = 5µm
RDL2 = 10µm
RDL3 = 15µm

IEEE Trans., CPMT, JUN 2018
Chip-Last (RDL-First) Fan-Out Panel-Level Packaging

IEEE Trans. on CPMT, JUL 2020
Antenna-in-Packaging (AiP)

IBM (ECTC2014) RF Flip Chips on Organic Substrate with Patch Antenna Array

TSMC (ECTC2018) RF Flip Chips in Fan-Out EMC with Patch Antenna Array (InFO_AiP)

THE TRANSMISSION LOSS FOR RDL AND SUBSTRATE TRACE AT 28 AND 38GHZ

<table>
<thead>
<tr>
<th>Frequency</th>
<th>InFO RDLs</th>
<th>Substrate Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td>28GHz</td>
<td>0.175dB/mm</td>
<td>0.288dB/mm</td>
</tr>
<tr>
<td>38GHz</td>
<td>0.225dB/mm</td>
<td>0.377dB/mm</td>
</tr>
</tbody>
</table>
TSMC’s AiP Patent: US 10,312,112 (June 4, 2019)

Unimicron’s Heterogeneous Integration of Baseband and AiP Patent: TW 1,209,218 (November 1, 2020)
2.1D IC Integration

- Shinko’s integrated thin-film high-density organic package (i-THOP)
- JECT’s ultra format organic substrate (uFOS)
2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (Shinko)

Line width and spacing = 2µm

40µm pad-pitch

25µm-pad

40µm pad-pitch

Φ 25µm-pad

IMAPS 2013, ECTC2014
2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (JCET)

- uFOS (ultra format organic substrate)
- e-STF (embedded stiffness)

Carrier
Surface Treatment
PI Coating
Metal Formation
PI Coating
Laser via drill
Metal formation and laser via drill
Carrier removal
Backside Laser via
ENIG Finish
2.5D IC Integration

- Examples: TSMC, Xilinx, AMD, Nvidia, Samsung
- TSV-less 2.5D by Samsung
- 2.5D heterogeneous integration of PIC (photonic IC) and EIC (electronic IC)
2.5D IC Integration

SoC
CPU/GPU/FPGA/ASIC

μSolder Joints

Cu

μSolder Joints

TSV

Memory Cube

TSV

C4

μSolder Joints

Logic

RDLs

Build-up Package Substrate

BGA

PCB

IEEE2017

Semiconductors for HPC applications driven by AI and 5G
Xilinx/TSMC’s 2.5D IC Integration with FPGA

CoWoS (chip on wafer on substrate)

Homogeneous Integration on Si-substrate

- RDLs: 0.4μm-pitch line width and spacing
- Each FPGA has >50,000 μbumps on 45μm pitch
- Interposer is supporting >200,000 μbumps
AMD’s GPU (Fiji), Hynix’s HBM, and UMC’s Interposer
Nvidia’s P100 with TSMC’s CoWoS-2 and Samsung’s HBM2

HBM2 by Samsung

4 DRAMs

Base logic die

TSV Interposer (CoWoS-2)

C4 bump

μbump

Build-up Package Substrate

Solder Ball

PDC, ECTC2017
Samsung’s Interposer-Cube4 (I-Cube4) (2.5D IC Integration)

Top View

Cross-section View

Bottom View

May 21, 2021
When integrating six or more HBMs, the difficulty in manufacturing the large-area substrate increases rapidly, resulting in decreased efficiency. Samsung solved this problem by applying a hybrid substrate structure in which HDI substrates that are easy to implement in large-area are overlapped under a high-end fine-pitch substrate. By decreasing the pitch of solder ball, which electrically connects the chip and the substrate, by 35% compared to the conventional ball pitch, the size of fine-pitch substrate can be minimized, while adding HDI substrate (module PCB) under the fine-pitch substrate to secure connectivity with the system board.

November 2021
Novel 2.5D RDL Interposer Packaging: A Key Enabler for the New Era of Heterogeneous Chip Integration (R-Cube)

Min Jung Kim, Seok Hyun Lee, Kyoung Lim Suk, Jae Gwon Jang, Gwang-Jae Jeon, Ju-il Choi, Hyo Jin Yun, Jongpa Hong, Ju-Yeon Choi, Won Jae Lee, SukHyun Jung, Won Kyoung Choi and Dae-Woo Kim
Test & System Package (TSP), Samsung Electronics Co., Ltd, Cheonan-si, Chungcheongnam-do, South Korea, South Korea mj3076.kim@samsung.com

ECTC2021, IWLPC2022
2.5D Heterogeneous Integration of EIC and PIC Devices
2.3D IC Integration

- Chip-First (either face-up or face-down)
- Chip-Last (RDL-First)
2.1D, 2.3D, and 2.5D IC Integration

Thin-Film Layer

Fine Metal L/S RDL-Substrate

Microbump

Underfill

C4 Bump

Build-up Substrate

Chip

Solder Ball

PCB

2.1D

2.3D

2.5D

Fine Metal L/S RDL-Substrate = Thin-Film Layer
Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions

Seung Wook Yoon, Patrick Tang, Roger Emigh, Yaojian Lin, Pandi C. Marimuthu, and Raj Pendse
STATSChipPAC Ltd., 5 Yishun Street 23, Singapore 768442

➢ The µbump, underfill-1, and TSV-interposer are eliminated.
➢ The RDLs are made by fan-out technology.

Chip-First
Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

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IEEE Transactions on CPMT, August 2021
High-Density Hybrid Substrate for Heterogeneous Integration

Chia-Yu Peng, John H. Lau, Life Fellow, IEEE, Cheng-Ta Ko, Paul Lee, Eagle Lin, Kai-Ming Yang, Puru Bruce Lin, Tim Xia, Leo Chang, Ning Liu, Curry Lin, Tzu Nien Lee, Jason Wong, Mike Ma, Tzyy-Jang Tseng

Unimicron

IEEE Transactions on CPMT, March 2022
2.3D Heterogeneous Integration of EIC and PIC Devices

Chip-Last

EMC

Fine metal L/S
RDL-substrate

Underfill

μbump

Heat Sink

ASIC/Switch

Electrical

Fibers

Optical

Driver

ASIC/Switch

(Laser/PD)

PIC

EIC

(Driver/TiA)

Heat Sink

C4 bump

Package Substrate

Solder Ball

PCB

Fiber Block

Fiber

40
3D IC Integration

- 3D IC Packaging (without TSVs)
- 3d IC Integration (with TSVs)
3D IC Packaging (without TSVs)
3D (Wirebonding) IC Packaging

(a) Top Chip
(b) Bottom Chip
(c) Substrate

16 Samsung 48L V-NAND die (40µm-thick)
3D (Flip Chip and Wirebond) Packaging

(a) Wirebond
(b) Heat spreader/sink (optional)

- Wirebond
- Mold
- DRAM (75µm)
- Baseband AP (75µm)
- 3L ETS
- PCB
- Cu-Pillar with solder cap

- Solder ball 0.35mm
- Solder
- Molded Underfill
- 8mm x 9mm x 580µm
- 115µm

- Memory
- SoC/Logic
- Rigid or Flex Substrate
- Underfill
- Daughter die
- Mother die
Snapdragon 805 Processor:
- 10.9mm x 11mm x 95µm
- CuSnAg bumps @110µm pitch
- 30µm bump-height after TC-NCP

Shinko’s MCeP®
3D PoP: Apple/TSMC InFO (Integrated fan-Out) for the iPhone Application Processor (Chip-First Die Face-up)

SoC

PoPzzz

3-Layer Coreless Package Substrate

Molding

Wirebond

Solder Ball

EMC

TIV (Through InFO Via)

Solder Ball

Mobile DRAM

3L Coreless substrate

Underfill

DAF

AP A10

EMC

RDLs

TIV

Solder Ball

PCB

~1300 solder balls at 0.4mm pitch

~1300 solder balls at 0.4mm pitch

Shipped in 2016
3D (PoP with Fan-Out) Packaging (Apple/TSMC)

AP SoC
9.9mm x 8.4mm

PoP
13.4mm x 14.4mm

3-Layer Coreless Package Substrate
Memories cross-stacked with wirebonds

Solder balls at 0.35mm-pitch

Solder bumped flip chip IPD

RDLs

EMC

PCB

A12 AP

Underfill

Over Mold

Wirebond

Solder Ball

A12 AP (150µm)

RDLs

Solder balls

Semiconductor Advanced Packaging, 2021
3D (PoP with Fan-Out) IC Packaging (Samsung)

- Memory ePoP
  - 2DRAM, 2NAND, 1Controller

- 3L Package substrate (90µm)

- Underfill
- Solder Ball

- 4RDLs

- AP (5mmx3mm)

- PMIC

- PCB

- Solder Ball

- Package substrate

- ABF

- 3L Organic Substrate

- 3D (PoP with Fan-Out) IC Packaging (Samsung)
3D IC Integration (with TSVs)
3D IC Integration

(a) Logic Base Chip

(b) Memory

(c) Bumpless Chip

Underfill

μbump

TSV

DRAM4

DRAM3

DRAM2

DRAM1

Package Substrate

CPU/Logic

TSV

TSV

Bumpless Chip

Chip

Chip
3D IC Integration with Active Interposer (High Bandwidth Memory)

<table>
<thead>
<tr>
<th></th>
<th>HBM</th>
<th>HBM2 (Original)</th>
<th>HBM2/HBM2E (Current)</th>
<th>HBM3 (Upcoming)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Pin Transfer Rate</td>
<td>1Gbps</td>
<td>2Gbps</td>
<td>2.4Gbps</td>
<td>?</td>
</tr>
<tr>
<td>Max Capacity</td>
<td>4GB</td>
<td>8GB</td>
<td>24GB</td>
<td>64GB</td>
</tr>
<tr>
<td>Max Bandwidth</td>
<td>128GBps</td>
<td>256GBps</td>
<td>307GBps</td>
<td>512GBps</td>
</tr>
</tbody>
</table>
Intel 3D IC Integration – FOVEROS Technology

Lakefield

3D IC Integration
Chip-to-Active TSV-Interposer (Samsung X-Cube)

3D IC Integration

μ-bump (Under3μm pitch)

3D Heterogeneous Integration of EIC and PIC Devices
System-on-Chip (SoC)
Moore’s Law - Apple’s Application Processors (AP): SoC (System-on-Chip) - A10, A11, A12, A13, A14, and A15

A10 consists of:
- 6-core GPU (graphics processor unit)
- 2 dual-core CPU (central processing unit)
- 2 blocks of SRAMs (static random access memory), etc.
- 16nm process technology
- Transistors = 3 billion
- Chip area = 125mm²

A11 consists of:
- More functions, e.g., 2-core Neural Engine for Face ID
- Apple designed tri-core GPU
- 10nm process technology
- Transistors = 4.3 billion
- Chip area = 89mm²

A12 consists of:
- Eight-core Neural Engine with AI capabilities
- Four-core GPU (faster)
- Six-core CPU (better performance)
- 7nm process technology
- Transistors = 6.9 billion
- Chip area = 83mm²

A13 consists of:
- Eight-core Neural Engine with Machine Learning
- Four-core GPU (20% faster > A12)
- Six-core CPU (20% faster and 35% save energy > A12)
- 7nm process technology with EUV
- Transistors = 8.5 billion
- Chip area = 98.5mm²

A14 consists of:
- 16-core Neural Engine with Machine Learning (11 trillion/s, 10 times faster > A13)
- Four-core GPU (30% faster > A13)
- Six-core CPU (40% faster > A13)
- 5nm process technology with EUV
- Transistors = 11.8 billion
- Chip area = 88mm²

A15 consists of:
- 16-core Neural Engine to speed up AI tasks with Machine Learning (15.8 trillion/s)
- Four-core GPU, but 5-core for iPhone Pro and 13Pro Max
- Six-core CPU (faster > A14)
- 5nm process technology with EUV
- Transistors = 15 billion
- Image signal processor
It is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC.
Design Cost for Advanced Nodes in Semiconductors

It will take another $1 billion for 5nm process development.

Sources: International Business Strategies
Yield (Cost) per Wafer vs. Chip Size for SoC and Chiplets

Chiplet Design and Heterogeneous Integration Packaging

- Chip partition and integration
- Chip split and integration
- Multiple System and Integration
Chiplet Design and Heterogeneous Integration Packaging

Chip partition and integration (Driven by cost and technology optimization)

SoC

Logic

I/O

Partition

Chiplet Designs

Logic

I/O

μBump, Bumpless, CoW, WoW

Frontend Chiplets Integration (Optional), e.g., SoIC

Heterogeneous Integration Packaging

Backend Chiplets Packaging Integration on the same substrate

Semiconductor Advanced Packaging, Springer, 2021
Chiplet Design and Heterogeneous Integration Packaging

Chip split and integration (Driven by cost and yield)

SoC

Logic

Split

Logic1
Logic2
Logic3

Chiplet Designs

μBump, Bumpless, CoW, WoW

Frontend Chiplets Integration (Optional), e.g., SoIC

Backend Chiplets Packaging Integration on the same substrate

Heterogeneous Integration Packaging

Semiconductor Advanced Packaging, Springer, 2021
Chiplet Design and Heterogeneous Integration Packaging

Multiple System and Integration (1)
2.5D IC Integration

Multiple System and Integration (2)
2.3D IC Integration

Chiplet Design and Heterogeneous Integration Packaging with TSV-Interposer

Chiplet Design and Heterogeneous Integration Packaging with Fan-Out RDL-Substrate

Semiconductor Advanced Packaging, 2021
Chiplet Design and Heterogeneous Integration Packaging

- **Chip (CPU)**
  - FAB-1
  - 5nm
  - 12”-wafer

- **Chip (I/O)**
  - FAB-2
  - 90nm
  - 8”-wafer

- **Chip (GPU)**
  - FAB-3
  - 7nm
  - 12”-wafer

**Heterogeneous integration or SiP**

- Time-to-market
- Less IP issues
- Flexibility
- Low cost alternative than SoC
- Optimized signal integrity and power
- Better thermal performance

Heterogeneous integration uses packaging technology to integrate dissimilar chiplets, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.
The key advantages of chiplets heterogeneous integration are:

1. Yield improvement (lower cost) during manufacturing;
2. Faster time-to-market;
3. Cost reduction during design;
4. Better thermal performance;
5. Reusable of IP;

The key disadvantages are:

1. Additional area for interfaces;
2. Higher packaging costs;
3. More complexity and design effort;
4. Past methodologies are less suitable for chiplets.
Examples on Chiplet Design and Heterogeneous Integration Packaging

- Xilinx
- AMD
- Intel
- TSMC
- Nvidia
- Samsung
For better manufacturing yield (to save cost), a very large SoC has been split into 4 smaller chips.

The key function of the RDLs on the interposer is to perform lateral communications between the chips.

Shipped in 2013
The I/O and CCD (core complex die or CPU compute die) are partitioned.

The CCD is split into two chiplets (7nm process technology).

The I/O chip is with 14nm process technology.

Shipped in 2019
AMD’s Future Chiplet Design and Heterogeneous Integration Packaging

3D IC Integration

ENGINEERING THE 3D CHIPLET ARCHITECTURE

- Structural Silicon
- 64MB L3 Cache Die
- Direct Cu-Cu Bonding
- TSVs For Si-to-Si communication
- Up to 8-Core “Zen 3” CCD

➢ AMD’s RYZEN 9 5900X Prototype chip for gaming
➢ Same 7nm process technology as RYZEN, but using 3D chiplet copper-to-copper bumpless hybrid bonding
Intel’s Chiplet Design and Heterogeneous Integration Packaging

➢ The memory and graphics are partitioned
➢ The large CPU is split into 5 smaller CPUs (10nm process technology)
➢ All the tiles (or chiplets) are attached on an active interposer

3D IC Integration

(a) Lakefield

(b) Foveros Technology

3D face-face chip stacking for heterogeneous integration

Compute Chip

Memory, Modem, ...

FTF Micro-Bumps

Thru-Silicon Solder Bumps

Active Interposer

Package Substrate

Shipped in 2020
Intel’s Future Chiplet Design and Heterogeneous Integration Packaging:- FOVEROS Direct

**FOVEROS (Micro Bumps)**

- 50μm pitch μbump bonding
- 400 bumps/mm²

**FOVEROS Direct**

- 10μm pitch hybrid bonding
- 10,000 pads/mm²

**Top Die**

**Bottom Die**

IEEE Hot Chip Conference, August 2021
Intel’s Future Chiplet Design and Heterogeneous Integration Packaging: - Ponte Vecchio GPU

- 47 Chiplets (16 HPC)
- Max. size = 41mm²

[Diagram showing chiplet design and integration packaging]

- Compute Tile
- Rambo Tile (8)
- Roveros
- Base Tile (2)
- HBM Tile (8)
- Xe Link Tile (2)
- Multi Tile Package
- EMIB Tile (11)

77.5mm x 62.5mm

IEEE Hot Chip Conference, August 2021
TSMC’s Chiplets Bonding, Density, and Performance

(a) Typical 3DIC
- μbump formation
- Flip chip stacking
- Underfill
- C4 FC bumps
- FC assembly on substrate

(b) SoIC
- Bond formation
- SoIC stacking (Hybrid Bonding)
- Underfill
- RDL (optional)
- FC or Wafer-level system integration

(c) Bump Density (counts/mm²)
- SolC
- SolC+
- 2.5D/3DIC
- Flip Chip

- Insertion Loss (dB)
  - SolC Hybrid Bonding
  - Flip Chip Bonding

- Frequency (GHz)
  - >1000x
  - >10x

IEEE/ECTC2020 and 2021
TSMC’s Chiplet Design and Heterogeneous Integration Packaging

CoWoS with SoIC

InFO PoP with SoIC
Classification of Heterogeneous Integration Packaging

- Chip (CPU)
  - FAB-1
  - 5nm
  - 12”-wafer

- Chip (I/O)
  - FAB-2
  - 90nm
  - 8”-wafer

- Chip (GPU)
  - FAB-3
  - 7nm
  - 12”-wafer

Heterogeneous integration or SiP

- Time-to-market
- Less IP issues
- Flexibility
- Low cost alternative than SoC
- Optimized signal integrity and power
- Better thermal performance

Heterogeneous integration uses packaging technology to integrate dissimilar chiplets, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.
Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations on Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposers
- Heterogeneous Integrations on Fan-Out RDL Substrates
- Heterogeneous Integrations on Ceramic Substrates
Amkor Automotive SiP (System-in-Package)

- Large singulated body SiP
- Infotainment & ADAS
- Autonomous driving
- Computers in a car
- Increasing trend in designs

Heterogeneous Integration on organic-substrate
The Apple Watch is SiP and was Assembled by ASE (Universal Scientific Industrial – Shanghai)
Three Substrate-Like PCBs (SiPs) in iPhone

Rear PCB (A)
- 8L HDI, 4mSAP layers, 16cm²
- Single-Sided Assembly
- Baseband, RF, WiFi/BT
- All components face inward

Front PCB 1 (B)
- 10L HDI, 6 mSAP layers, 10cm²
- Double-Sided Assembly
- A12 CPU, Memory, Connectors
- A12 CPU faces inward

Front PCB 2 (C)
- 6L HDI, 2 mSAP layers, 2cm²
- Double-Sided Assembly
- RF FEM, Connectors
- RF FEM face inward

[1] Intel Baseband Chipset
[2] Intel PM IC
[3] Intel RF Transceiver
[4] Skyworks RF FEM
[6] USI WiFi/BT Module
[7] Broadcom Wireless Charger
[8] NXP NFC Controller

[1] Apple A12 Chipset
[2] Flash Memory
[3] Power Manager
[4] ST Power Manager
[5] Power Manager
[6] TI Battery Charger
[7] Audio Codec
[8] Audio Amplification
[9] Avago RF FEM
[10] Skyworks RF FEM
Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations on Silicon Substrates (Passive TSV-Interposers and Active TSV-Interposers)
- Heterogeneous Integrations on TSV-less Interposers
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates
Xilinx’s HPC Applications Driven by AI and 5G (Passive TSV-Interposer)
Intel 3D IC Integration – FOVEROS Technology (Active TSV-Interposer)

Lakefield

12 mm

3D IC Integration

μbump

10nm Compute Die (Chiplets)

22FFL Base Die

TSV

Active Interposer

Package Substrate

Solder Ball

C4 bump

Semiconductor Advanced Packaging, 2021
Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposer (e.g., Bridges – lateral communication between chiplets)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates
Lateral Communications (Bridges) between Chiplets

- Bridge Embedded in Build-up Package Substrate
- Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)
- Flexible Bridge
Bridge Embedded in Build-up Package Substrate
Intel’s EMIB Patent and Agilex Module

Intel’s Embedded Multi-die Interconnect Bridge (EMIB) in package substrate
Intel’s FPGA (Agilex) with EMIB

- **C4 Solder Joint**
- **PCB**
- **Solder Joint**
- **Package Substrate**
- **EMIB**
- **FPGA**
- **HBM**
- **RDL**
- **Micro Solder Joint**
- **C4 bumps**
- **Microbumps**

*Intel’s FPGA (Agilex) with EMIB*
Intel’s EMIB
(Embedded Multi-die Interconnect Bridge)

C4 (controlled collapse chip connection) bumps and C2 (Cu-pillar + solder cap) bump on chip

- The minimum metal L/S/H is 2μm.
- The dielectric layer thickness is 2μm.
- The bridge size is from 2mm x 2mm to 8mm x 8mm
- Usually, there are ≤ 4 RDLs.
IBM’s Direct Bonded Heterogeneous Integration (DBHi) Si Bridge

- Chiplet 1
- Chiplet 2
- Bridge
- Build-up Package Substrate
- C4 Bump
- NCP
- μBump
- UBM
- C4 Bump
- C2 Bump
- Solder
- Underfill
- Trench
- BRIDGE
- Laminate FC layers
- Underfill Anchor

ECTC2021
Differences between Intel’s EMIB and IBM’s DBHi

➢ For Intel’s EMIB, there are two different (C4 and C2) bumps on the chiplets (and there are no bumps on the bridge), while for IBM’s DBHi, there are C4 bumps on the chiplets and C2 bumps on the bridge.

➢ For Intel’s EMIB, the bridge is embedded in the cavity of a build-up substrate with a die-attach material and then laminated with another build-up layer on top. Therefore, the substrate fabrication is very complicated. For IBM’s DBHi, the substrate is just a regular build-up substrate with a cavity on top.
IBM’s DBHi Key Process Steps

ECTC2021
Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)
Applied Materials’ Fan-out Chip (Bridge) First Face-up Process

US patent 10,651,126 (filed on December 8, 2017)
TSMC’s LSI (Local Silicon Interconnect)
Fan-out Chip (Bridge) First Face-up Process

InFO_LSI

CoWoS_LSI

TSMC Annual Technology Symposium, August 25, 2020
Apple’s UltraFusion
(M1 Ultra = M1 Max + M1 Max + Si Bridge)

UltraFusion — Apple’s innovative packaging architecture that interconnects the die of two M1 Max chips to create a system on a chip (SoC) with unprecedented levels of performance and capabilities

March 8, 2022
Unimicron’s Fan-out Chip (Bridge)  
First Face-down Process

U.S. patent was filed on May 7, 2021
Advanced HDFO Packaging Solutions for Chiplets Integration in HPC Application

Lihong Cao Teck Lee1, Yungshun Chang1, SimonYL Huang1, JY On1, Emmal Lin1 and Owen Yang1

Advanced Semiconductor Engineering Inc. (US) Inc., Austin, TX 78704. USA

Corporate R&D Center, Advanced Semiconductor Engineering Inc., Kaohsiung, Taiwan (R.O.C)

sFOCoS (Stacked Si bridge Fan-Out Chip-on-Substrate)
S-Connect Fan-out Interposer For Next Gen Heterogeneous Integration

JiHun Lee, GamHan Yong, MinSu Jeong, JongHyun Jeon, DongHoon Han, MinKeon Lee, WonChul Do, EunSook Sohn, Mike Kelly, Dave Hiner JinYoung Khim
Research & Development Amkor Technology Korea Incheon, Korea JinYoung.Khim@amkor.co.k

(a) ASIC or processor
(b) HBM
(c) integrated passive device or active device
(d) bridge die for ASIC to memory interconnection
(e) Package substrate

IEEE/ECTC June 2021
Electrical Performances of Fan-Out Embedded Bridge (FO-EB)

JinWei You, Jay Li, David Ho, Jackson Li, Ming Han Zhuang, David Lai, C. Key Chung, Yu-Po Wang
Siliconware Precision Industries Co. Ltd Taichung, Taiwan jinweiyou@spil.com.tw

IEEE/ECTC June 2021
Heterogeneous Integration with Embedded Fine Interconnect (EFI)

Chai Tai Chong, Lim Teck Guan, David Ho, Han Yong, Chong Ser Choong, Sharon Lim Pei Siang, Surya Bhattacharya

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IEEE/ECTC June 2021
Flexible Bridge
Flexible Bridge

U.S. 2006/0095639 A1 was filed by SUN Microsystems
Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposer (Bridges)
- Heterogeneous Integrations on Chip-First and Chip-Last Fan-Out RDL-Substrates (interposer) – 2.3D IC Integration
- Heterogeneous Integrations on Ceramic Substrates
Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate (FOCoS)

Yuan-Ting Lin, Wei-Hong Lai, Chin-Li Kao, Jian-Wen Lou, Ping-Feng Yang, Chi-Yu Wang, and Chueh-An Hseih*

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Chip-First

CoWoS

ASE’s FOCoS

IEEE/ECTC2016
Heterogeneous Integration with Multilayer Fan-Out RDL Interposer


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Email: *spjeng@tsmc.com
Classification of Heterogeneous Integrations

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MCM (Multichip Module) on Ceramic Substrate

IBM 9121 TCM
(Thermal Conduction Module)

- TCM weighs 2.2Kg
- Contains up to 121 chips about 8-10mm square
- Each chip has a spring-loaded Cu piston to remove heat
- Up to 10W dissipation per chip
- Up to 600W dissipation per TCM

Ceramic substrate has:
- 63 layers
- Up to 400m of wirings
- Up to 2 million vias

- 5Kg air-cooled heatsink to remove heat from TCM
How to Select Substrate for Heterogeneous Integration Packaging?

➢ It depends on the applications.

➢ The most important indicator (selection criterion) is the metal line width and spacing of the RDLs for the substrates being used for the heterogeneous integrations.

➢ Also, low loss dielectric materials for high-speed and high-frequency are very important.
Heterogeneous Integrated Substrates (Next 5 Years)

- TSV-Interposer (L/S ≤ 1µm)
- Can be > 100,000
- FO-RDL Chip-Last, (L/S ≥ 2µm)
- Organic Substrates (12-12 and L/S ≥ 6µm; Thin-film layer L/S ≥ 2µm)
- Bridge (L/S ≥ 2µm)
Hybrid Substrates for HPC and Data Center Applications Driven by AI and 5G/6G

- Hybrid Substrate = Inorganic Substrate + Organic Substrate

- Inorganic Substrate made from PECVD, PVD, Stepper, ECD, CMP, etc.

- Organic Substrate made from PID, PVD, LDI, ECD, etc.

![Diagram of hybrid substrate with layers labeled Inorganic and Organic Substrate, showing C4 Bump or Solder Ball, RDL layers, and Microbump/Bumpless connections.]
Roadmap for Df (Dissipation Factor or Loss Tangent) and Dk (Dielectric Constant or Permittivity)
Bumpless Cu-Cu Hybrid Bonding
Key Process Steps (Fundamental) of Hybrid Bonding

Metal (Cu) recess = 3nm
Plasma surface Activation

Oxide to Oxide Initial Bond
at Room Temperature

Heating Closes Dishing Gap
(Metal CTE > Oxide CTE)
(Optional)

Annealing (300°C for 0.5h)
w/o External Pressure

The challenges (opportunities) of CoW hybrid bonding are:

- CMP for metal recess, clean, and flat surface.
- the edge effects;
- contaminants;
- particles due to singulation;
- the requirement of higher accuracy pick and place machines;
- slightly larger pads to compensate the pick and place tolerance.
Sony’s CMOS image sensor made by hybrid bonding
Other Hybrid Bonding

10μm pitch hybrid bonding 10,000 pads/mm²

Intel

Bumpless Cu pads for hybrid bonding

TSMC

RYZEN 9 5900X

AMD/TSMC
Summary and Trends

➢ Advanced packaging has been defined, and the kinds of advanced packaging have been ranked according to their interconnect density and electrical performance and grouped into 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration.

➢ The **2D** IC integration, such as **SiP**, is and still will be used the most.

➢ The challenge of **2.1D** IC integration (with thin film layers on build-up package substrate) is (warpage) manufacturing yield.

➢ The **2.3D** IC integration is creeping into production.

➢ For extreme high-performance and high-density applications, **2.5D** IC integration is the solution.

➢ The **3D** IC integration are already in volume production for mobile processors, and they will be used for more different kinds of products.

➢ Fan-outs, such as chip-first (face-down) and chip-first (face-up), have been in **HVM** for consuming products. Chip-first (face-down) is and will still be used the most. **Chip-last or RDL-first is not** in HVM yet but it will be soon.
Summary and Trends

➢ More than 75% of the flip-chip applications are with C4 bumps mass reflowed on organic package substrates and CUF (capillary underfill) (SiP).

➢ TCB (thermocompression bonding) of C2 bumps with small-force and CUF is getting traction because of the interest in using thin chips and thin organic substrates.

➢ No more than 25% of the flip-chip applications are for silicon-to-silicon, such as CoC, CoW, and WoW.

➢ Roadmaps of Df and Dk for low-loss dielectric materials of advanced packaging have been provided.

➢ The TSV-interposer integration platform for PIC and EIC of high-speed and high-bandwidth applications is getting lots of tractions. A couple of examples have been provided.

➢ A heterogeneous integration of AiP and baseband chipset with heat spreader/sink by chip-first with die face-down packaging for high performance and compact 5G millimeter wave system integration has been proposed.
SoCs with finer feature sizes are and will be here to stay. Chiplets design and heterogeneous integration packaging provide alternatives to SoCs, especially for advanced nodes.

The key advantages of chiplets heterogeneous integration are:
1. Yield improvement (lower cost) during manufacturing,
2. Time-to-market,
3. Cost reduction during design,
4. Better thermal performance,
5. Reusable of IP,

The key disadvantages are:
1. Additional area for interfaces,
2. Higher packaging costs,
3. More complexity and design effort,
4. Past methodologies are less suitable for chiplets.
Summary and Trends

➢ Bridge technology such as EMIB for chiplets’ horizontal communication in organic substrate has been in production. Recently, there are many publications on bridges embedded in EMC.

➢ More than 75% of heterogeneous integration are on organic substrate (SiP by SMT and flip chip on board) and no more than 25% are on other substrates.

➢ Hybrid bonding can be applied to extremely fine pitch (as low as 4μm) pads and used for very high-density and high-performance applications.

➢ Hybrid bonding is only suitable for silicon-to-silicon assembly such as CoC, CoW, and WoW.
  ➢ Because of the throughput issue, CoC bonding will not be popular.
  ➢ Because of the chip-size and yield issues, WoW bonding is limited even it will be used more than today.
  ➢ Because of the flexibility, CoW will be the mainstream.
Some Recent Advanced Packaging Publications by the Lecturer and his Colleagues


Thank You Very Much for Your Attention!