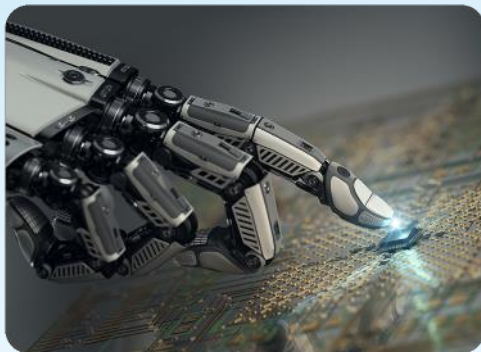# Recent Advances and Trends in Advanced Packaging

John H Lau
Unimicron Technology Corporation
john_lau@unimicron.com
IEEE EPS Binghamton Chapter, April 13, 2022

This Presentation is supported by the IEEE Electronics Packaging Society's Distinguished Lecturer Program

eps.ieee.org

◆IEEE

IEEE Electronics Packaging Society

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…Chapters, members, constituents spanning the world

38 Chapters located in US, Asia/Pacific, Europe

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4500 attendees at 25 Conferences/Workshops

Packaging Field + 6 EPS Awards + PhD Fellowship

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Bulgaria

Canada (4)

France

Germany

Hong Kong

Hungary/Romania

Israel

Korea

Japan

Malaysia

Nordic

(Sweden, Denmark, Finland, Norway, Estonia, Iceland)

Poland

Russia

Shanghai

Singapore

Switzerland

Taipei

Ukraine (2)

United Kingdom & Republic of Ireland

United States (12)

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Peer-Reviewed Technical Publication
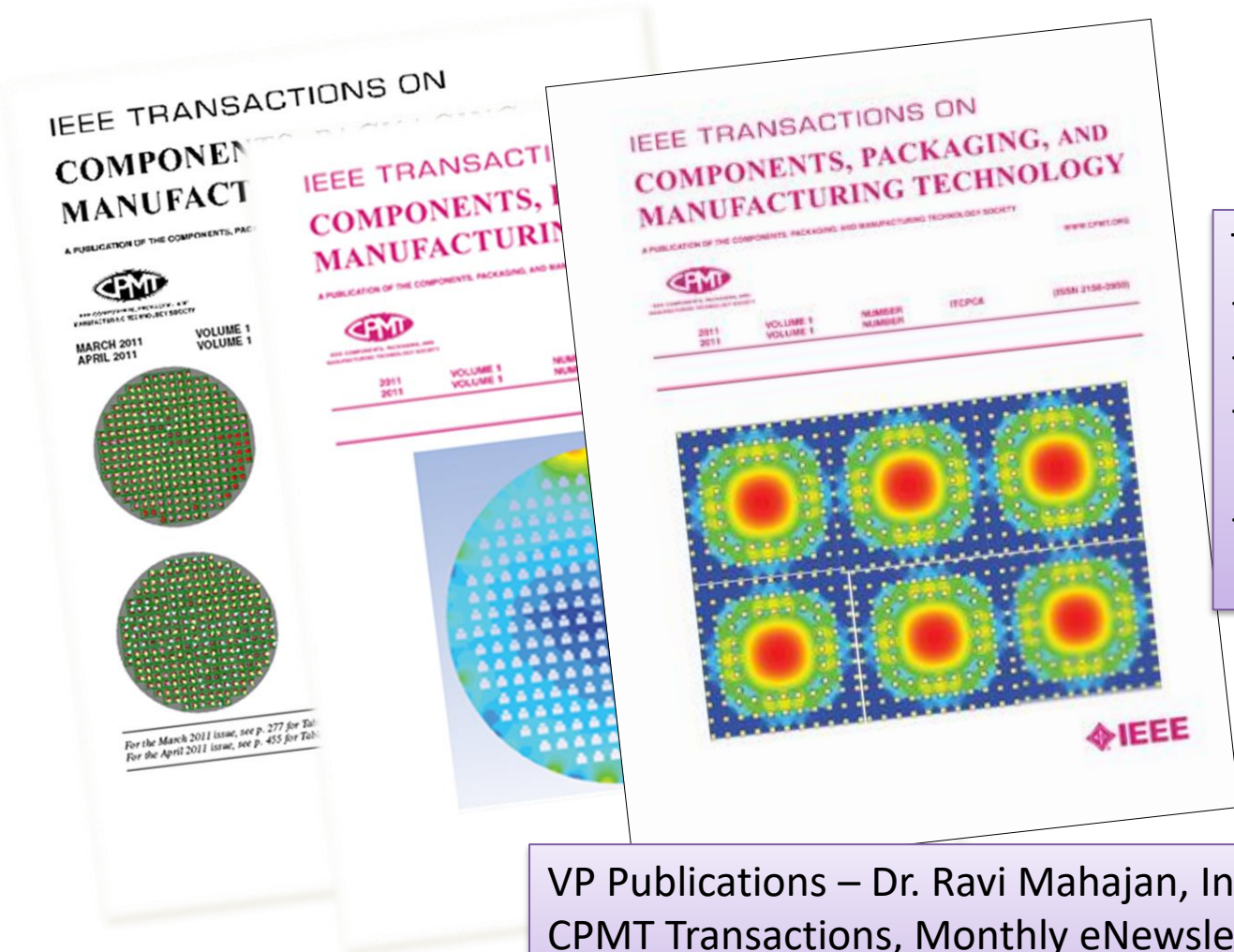
Transactions on CPMT
- 595 submissions (2020)
- 240 papers published
- Impact Factor: ~ 1.7 (2020)
- Xplore Usage: 40,000+

VP Publications – Dr. Ravi Mahajan, Intel
CPMT Transactions, Monthly eNewsletter, and
Bi-Annual printed Newsletter

EPS Awards & Recognition

IEEE Electronics Packaging Award
(IEEE Technical Field Award)

Outstanding Sustained Technical Contribution Award

Electronics Manufacturing Technology

David Feldman Outstanding Contribution

Exceptional Technical Achievement

Outstanding Young Engineer

Transactions Best Papers
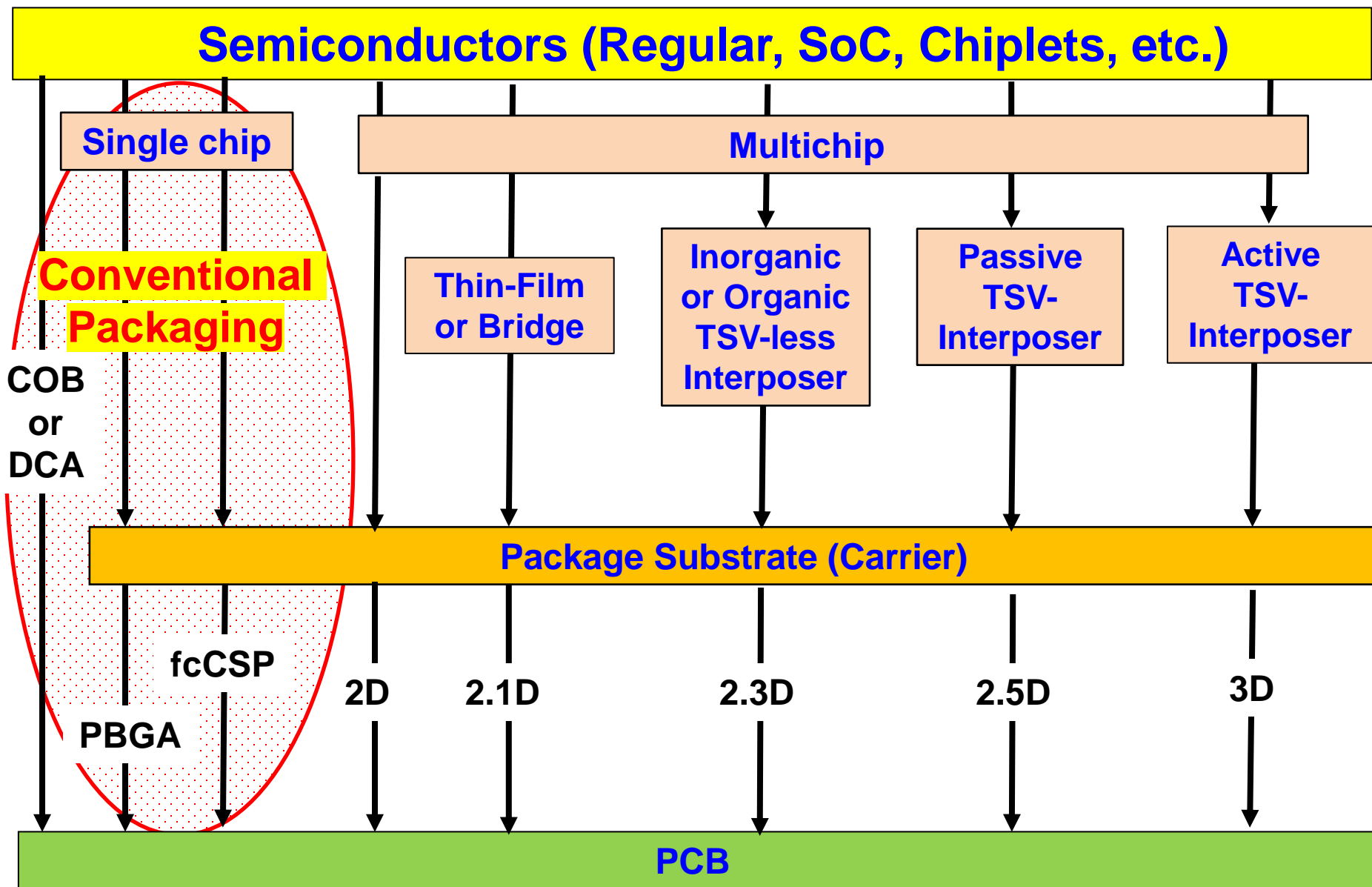
Regional Contributions

PhD Fellowship

CONTENTS
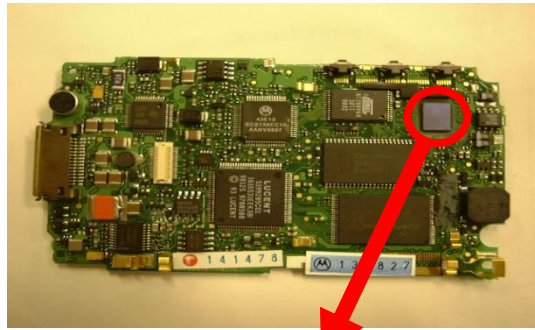
The Biggest Difference between Chiplet and Heterogeneous Integration:

➢ **Chiplet is a Chip Design Method**

➢ **Heterogeneous Integration is a Chip Packaging Method**

Semiconductor Packaging Technologies

Semiconductors (Regular, SoC, Chiplets, etc.)

Single chip

Multichip

Conventional Packaging

Thin-Film or Bridge

Inorganic or Organic TSV-less Interposer

Passive TSV-Interposer

Active TSV-Interposer

COB or DCA

Package Substrate (Carrier)

fcCSP
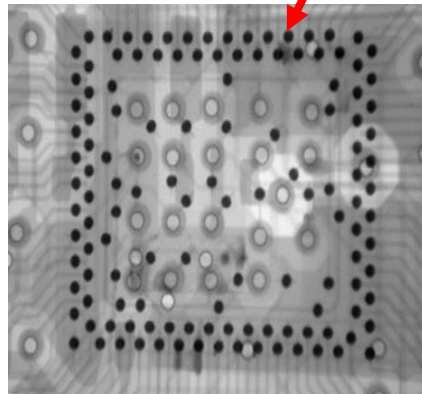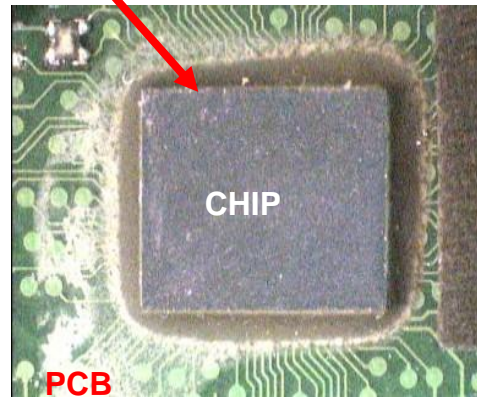
2D   2.1D   2.3D   2.5D   3D

PBGA

PCB

Conventional Packaging:
Direct Chip Attach (DCA) and
Flip Chip Ball Grid Array (fcBGA)

Underfill

Solder joint

CHIP

PCB

X-ray showing solder joints

Chip

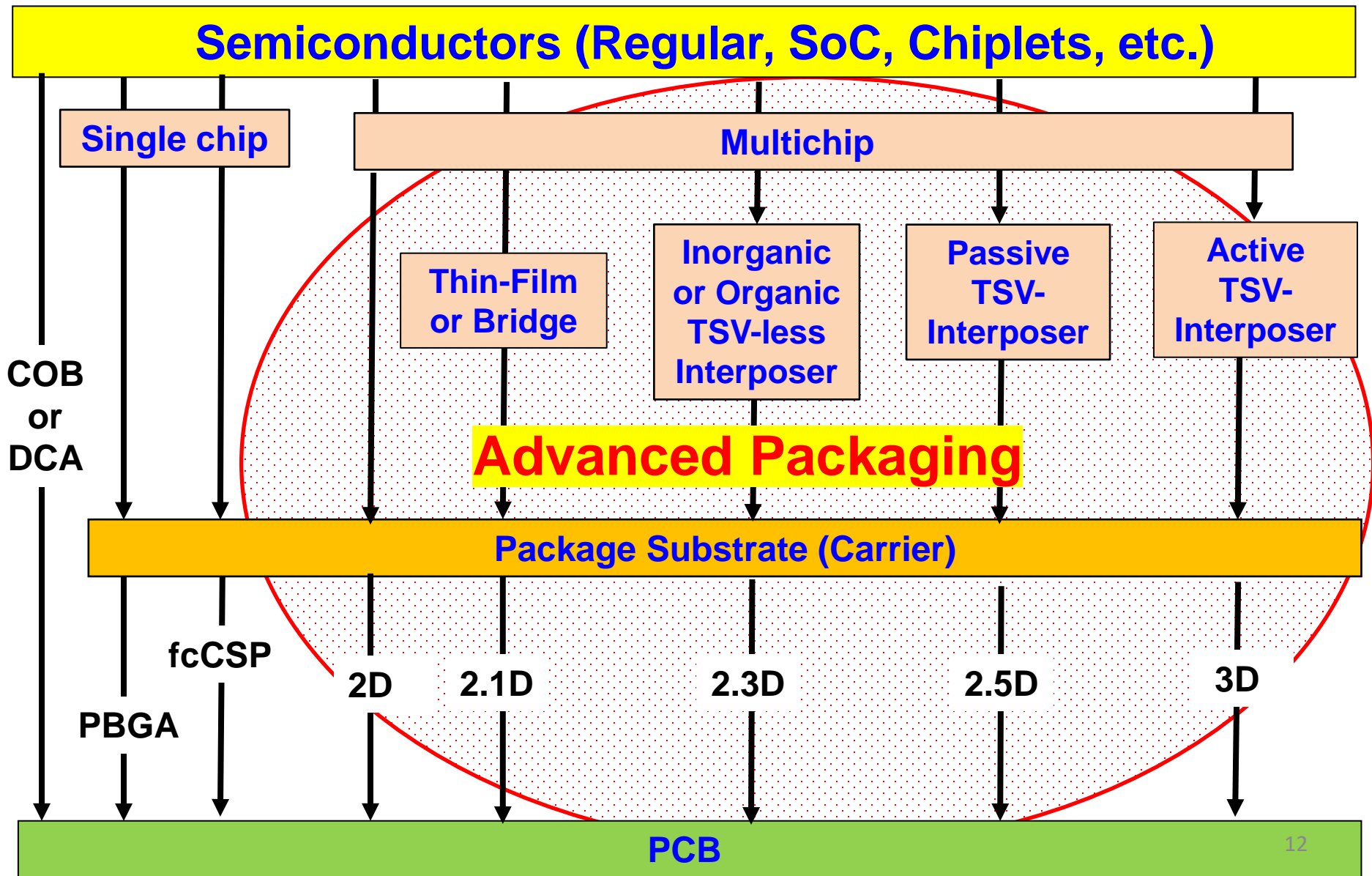Package Substrate

Solder Bumps   Solder Balls

PCB

Ni-plated Cu Lid

Underfill

Chip

Package Substrate
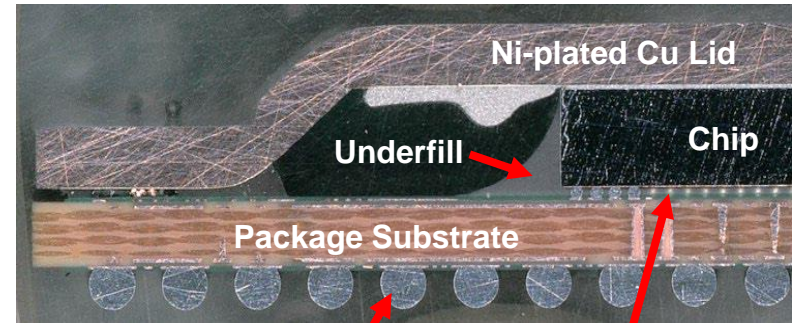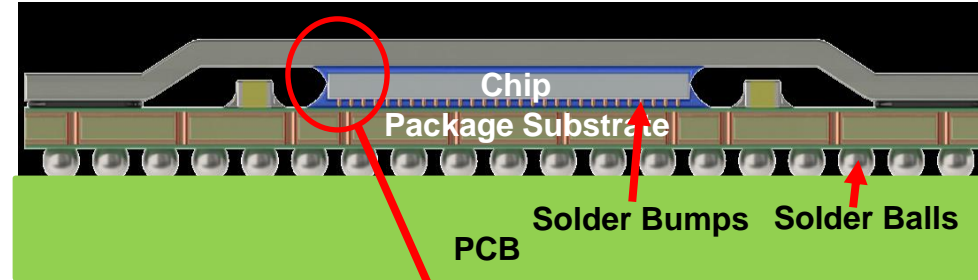
Solder Balls

Solder Bumps

DCA

fcBGA

Groups of Advanced Packaging:
2D, 2.1D, 2.3D, 2.5D, and 3D IC integration

Semiconductors (Regular, SoC, Chiplets, etc.)

Single chip

Multichip

Thin-Film or Bridge

Inorganic or Organic TSV-less Interposer

Passive TSV-Interposer

Active TSV-Interposer

COB or DCA

Advanced Packaging

Package Substrate (Carrier)

fcCSP

2D   **2.1D**   **2.3D**   **2.5D**   **3D**

PBGA

PCB

12

Advanced Packaging Ranking According to Their Density and Performance

Electrical Performance (vertical axis) vs. Interconnect Density (horizontal axis):

- Bumpless Chiplets 3D IC Integration
- Bumpless 3D IC Integration
- µBump Chiplets 3D IC Integration
- µBump 3D IC Integration
- 2.5D (C2 or µBump) IC Integration
- 2.5D (C4 or solder bump) IC Integration
- 2.3D Fan-Out (Chip-Last) IC Integration
- 2.3D Flip Chip IC Integration
- 2.3D Fan-Out (Chip-First) IC Integration
- 2.1D Fan-Out IC Integration with Bridge
- 2.1D Flip Chip IC Integration with Bridge
- 2.1D Flip chip IC Integration
- 2D Fan-Out (Chip-Last) IC Integration
- PoP, SiP
- 2D Flip Chip IC Integration
- 2D Fan-Out (Chip-First) IC Integration

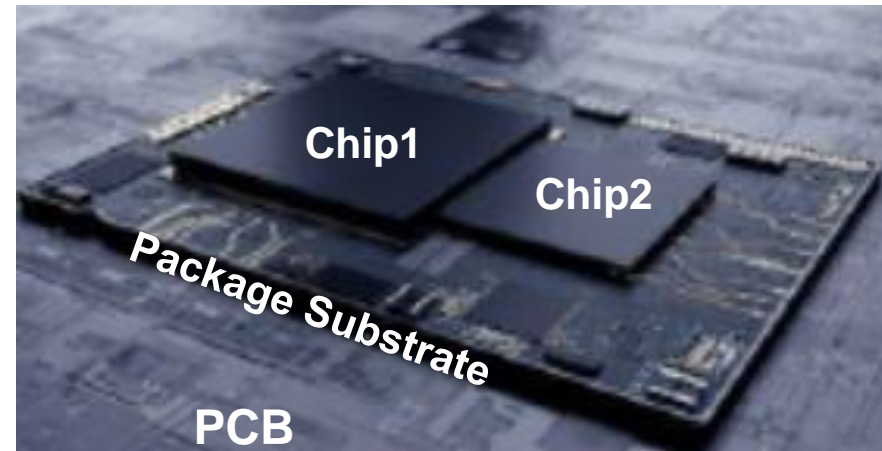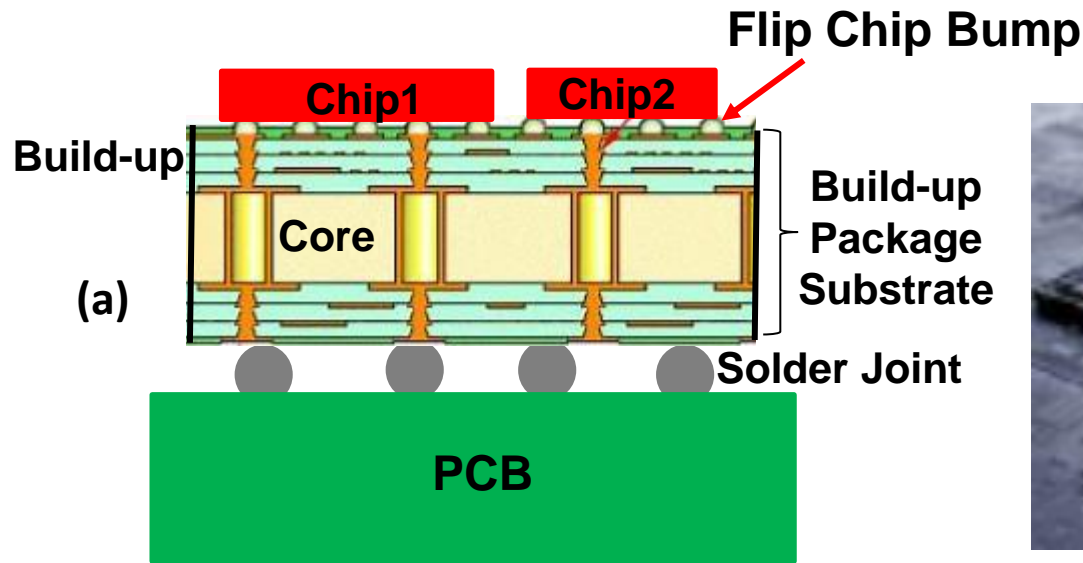Semiconductor Advanced Packaging, 2021

Advanced Packaging

➢ **2D IC Integration**
➢ **2.1D IC Integration**
➢ **2.3D IC Integration**
➢ **2.5D IC Integration**
➢ **3D IC Integration**

2D IC Integration

➢ **2D (Flip Chip) IC Integration**

➢ **2D (Fan-Out) IC Integration**
  - **Chip-First die Face-Down**
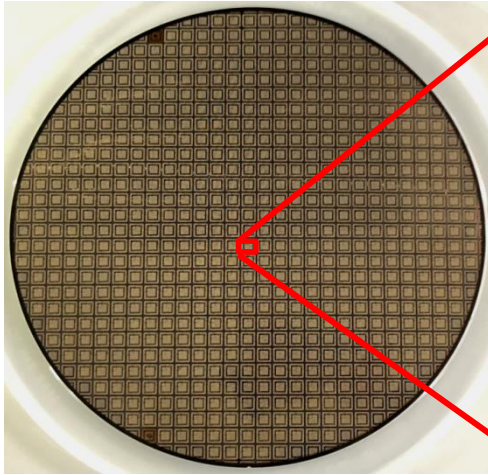 - **Chip-First die Face-Up**
  - **Chip-Last (RDL-First)**

# 2D (Flip Chip / Wirebond) IC Integration

Flip Chip Bump

Chip1 **Chip2**

Build-up

Build-up Package Substrate

Core

(a)

Solder Joint

PCB

Chip1
Chip2
Package Substrate
PCB

Encapsulation

Flip Chip Bonding **Wire Bonding**

IC

Cap

MEMS

(b)

Build-up Package Substrate

Solder Ball

PCB

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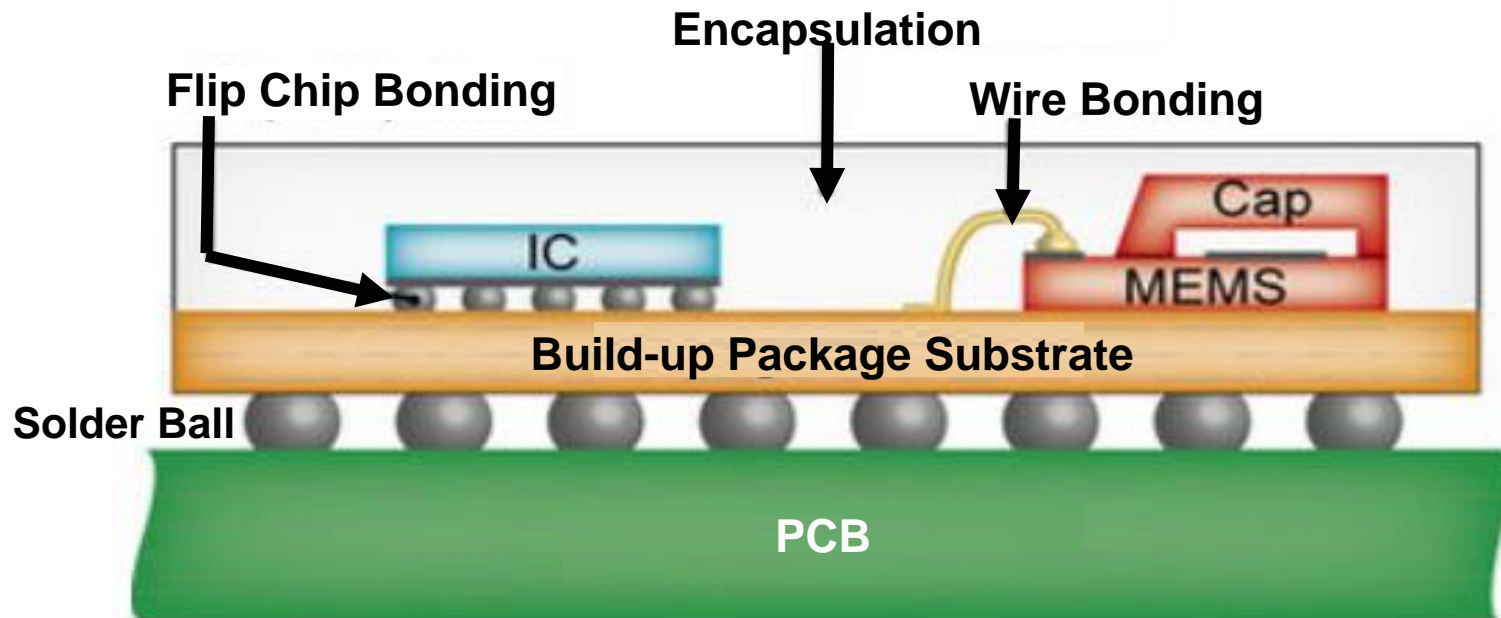
2D (Fan-Out) IC Integration: Chip-First (Die Face-Down)

300mm reconstituted wafer

10mmx10mm SiP

CHIP   CHIP

CHIP   CHIP

10mm

10mm

3mm x 3mm   3mm x 3mm
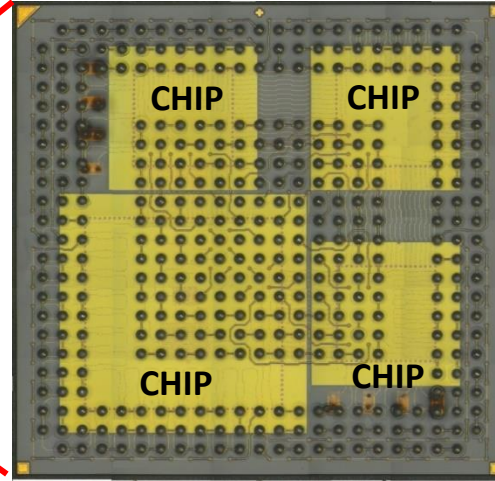
5mm x 5mm   3mm x 3mm
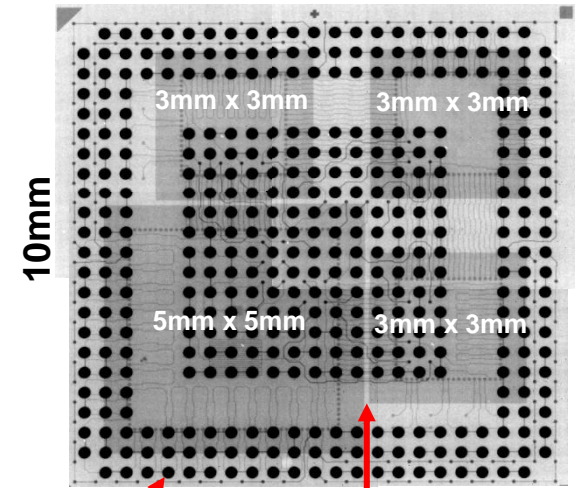
405 Solder Ball   **100µm-Gap**

CHIP

RDL1

RDL2
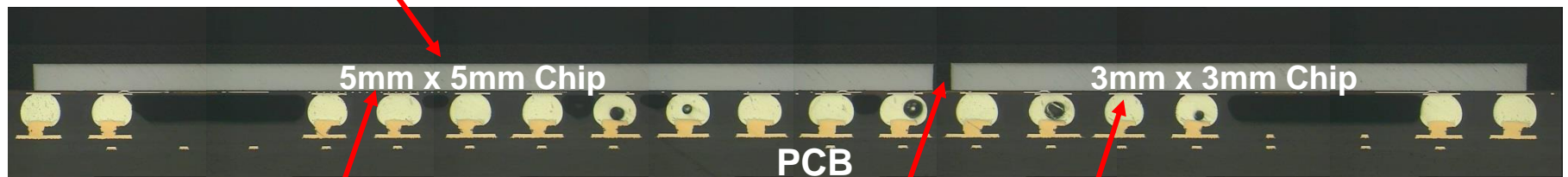
Solder Ball
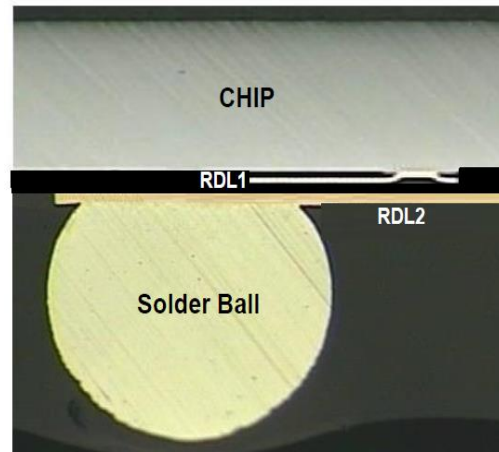
There is no substrate which is replaced by RDLs (redistributed-Layers)
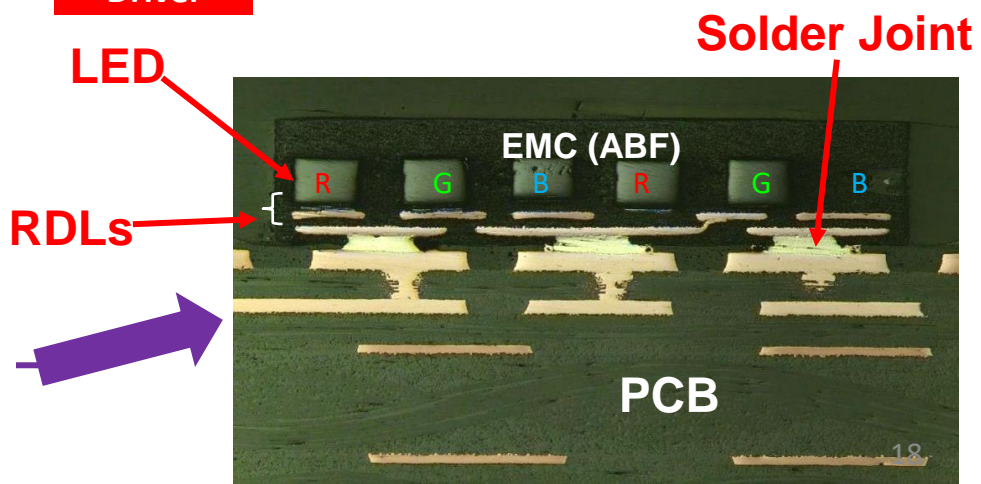
EMC

5mm x 5mm Chip   3mm x 3mm Chip
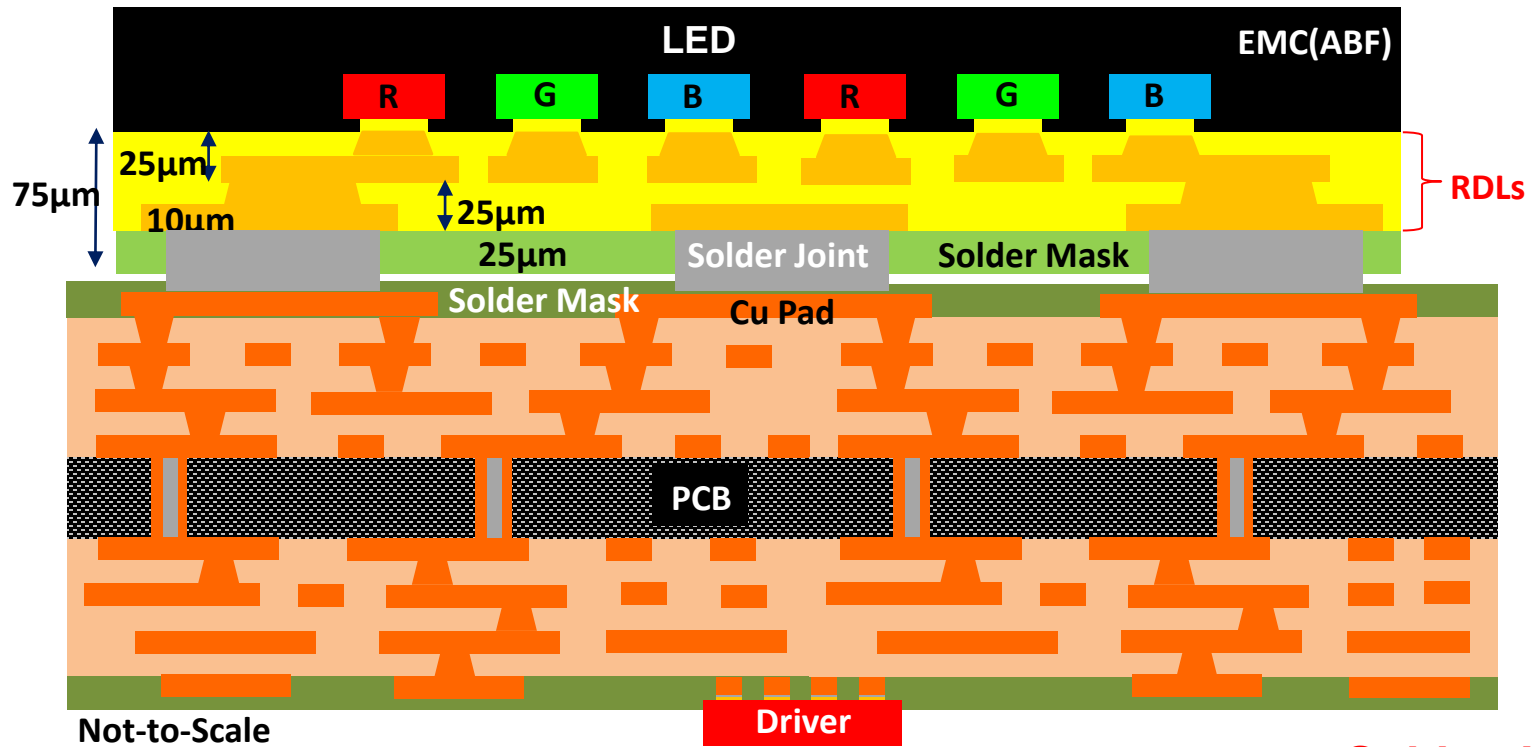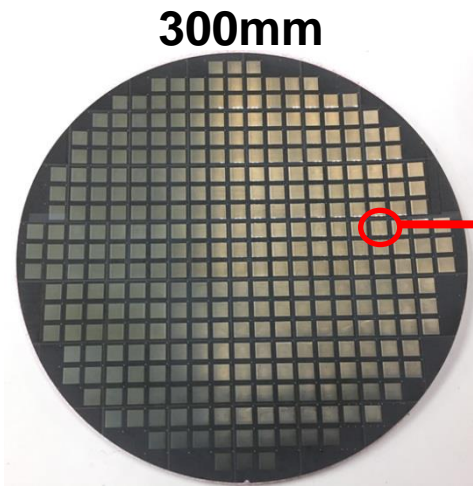
PCB

RDLs   **100µm Gap**   **Solder Joint**

Heterogeneous Integration of Mini-LEDs for RGB-display (Chip-First Die Face-Down)

LED   EMC(ABF)

R   G   B   R   G   B

25μm

75μm

10μm   25μm

RDLs

25μm   Solder Joint   Solder Mask

Solder Mask   Cu Pad

PCB

Not-to-Scale

Driver

Solder Joint

LED

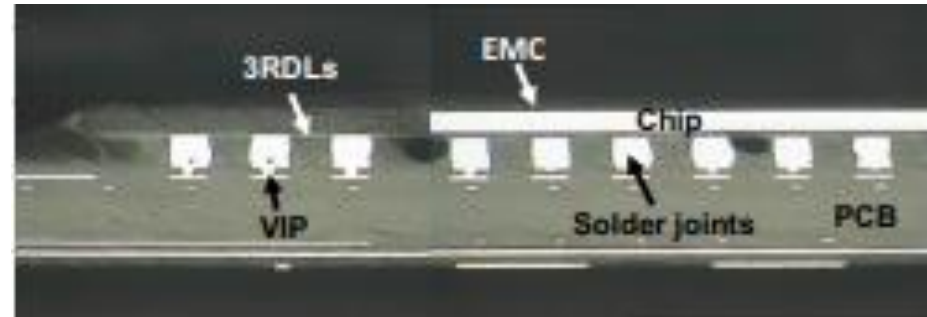EMC (ABF)
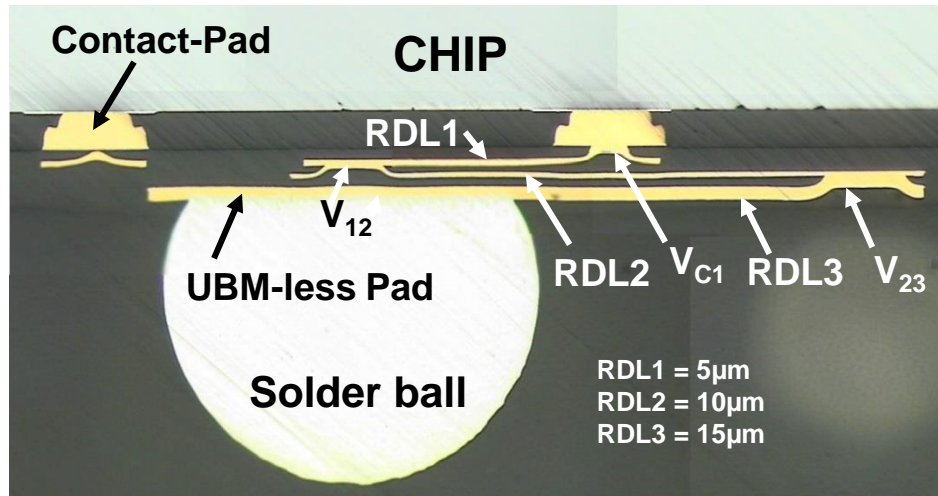
R   G   B   R   G   B

RDLs

PCB

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Fan-Out Chip-First (Die Face-Up)

300mm
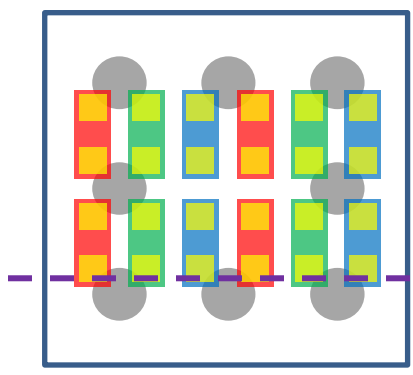
**Reconstituted Wafer
(325 packages)**

(13.42mm x 13.42mm)

**Chip
(10mm x 10mm)**

Package

Solder balls on package

RDLs

Chip corner

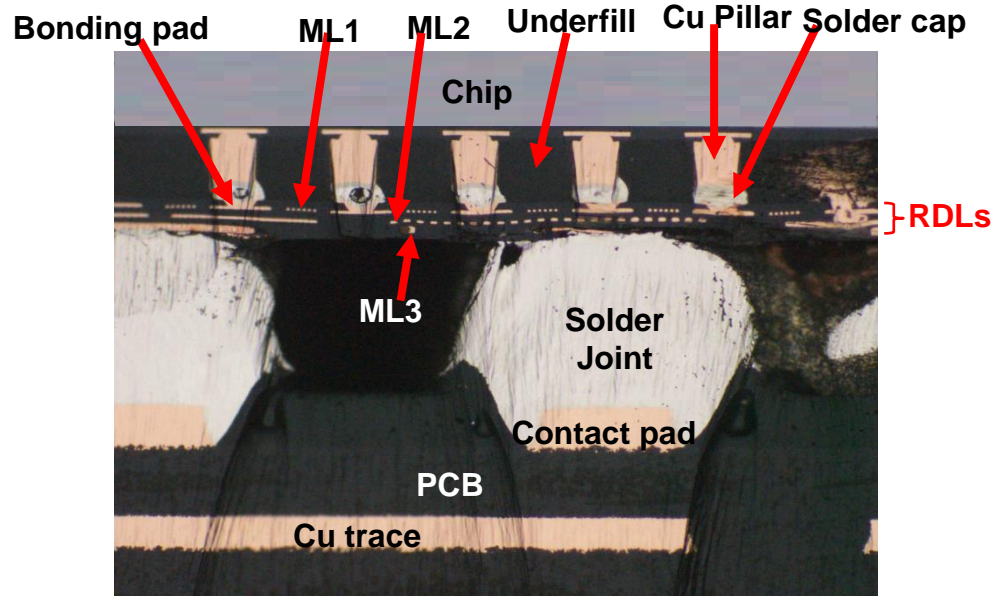**Pads on package for TMV**

Contact-Pad

CHIP

RDL1

V_{12}

UBM-less Pad

RDL2 V_{C1} RDL3 V_{23}

Solder ball

RDL1 = 5μm
RDL2 = 10μm
RDL3 = 15μm

3RDLs   EMC   Chip

VIP   Solder joints   PCB

19
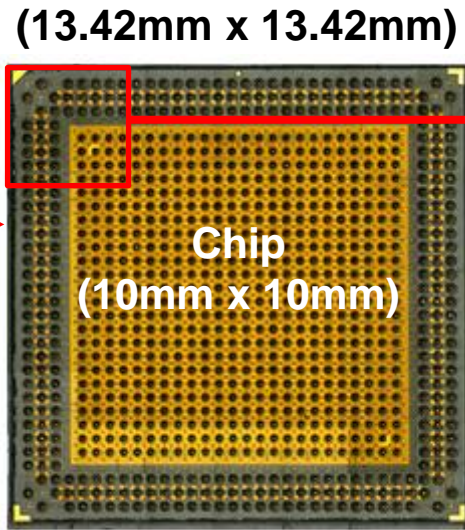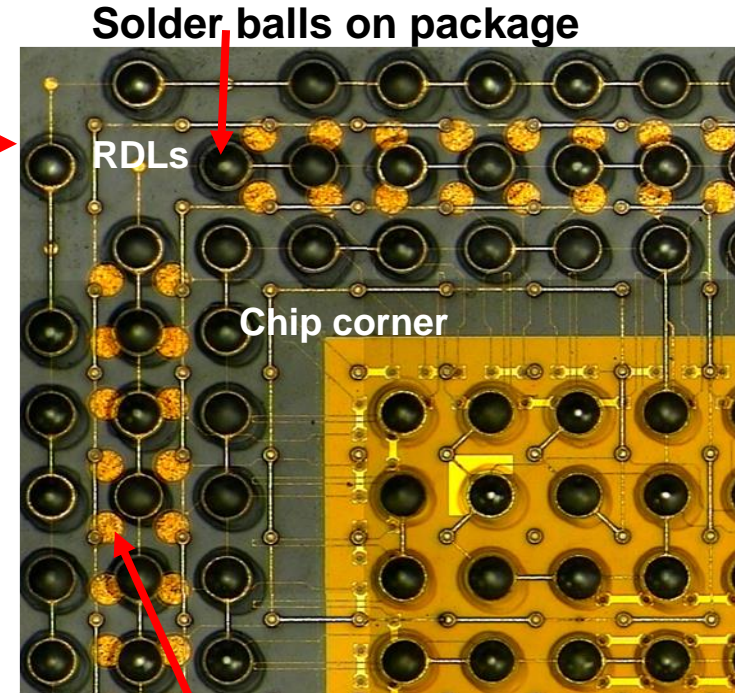
Chip-Last (RDL-First) Fan-Out Panel-Level Packaging

20mm

20mm

Chip 2B (5 x 7)

Chip 1 (10 x 10)

Chip 2A (5 x 7)

EMC

Chip 1

Chip 2

Cu pillar

Solder Cap

Cu Pad

RDL1 (2/2μm)

RDL2 (5/5μm)

RDL3 (10/10μm)

Solder Joints

PCB

Chip 2B

Chip 1

Chip 2A

Bonding pad   ML1   ML2   Underfill   Cu Pillar   Solder cap

Chip

RDLs

ML3

Solder Joint

Contact pad

PCB

Cu trace

20
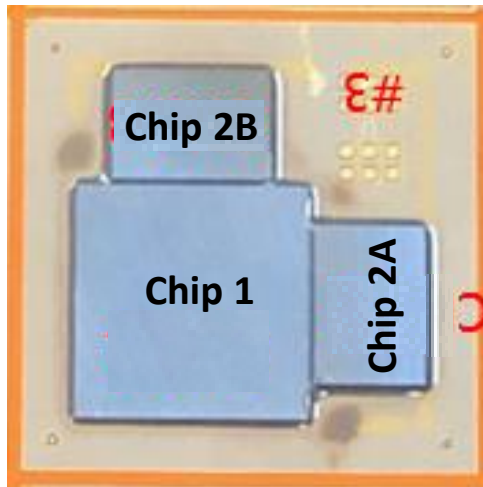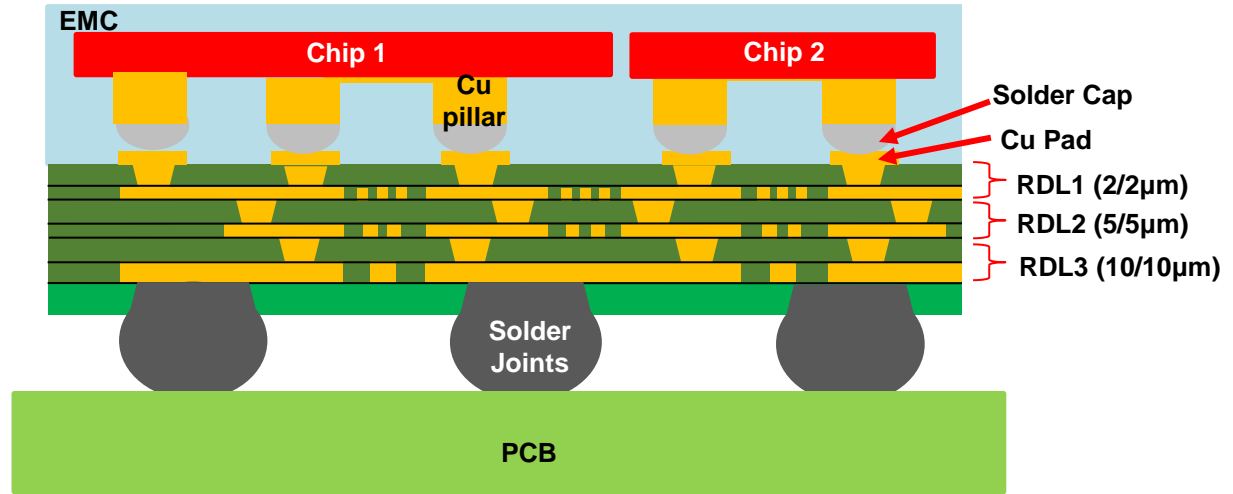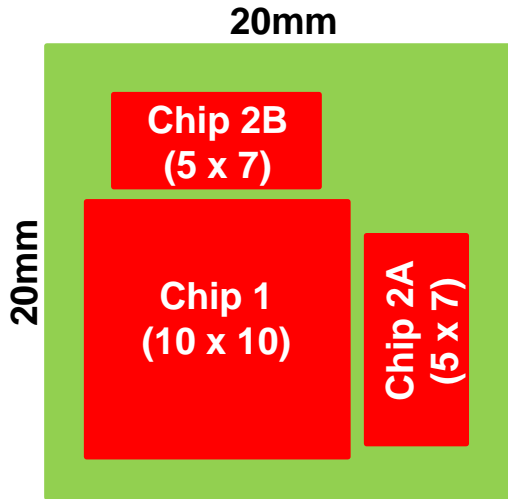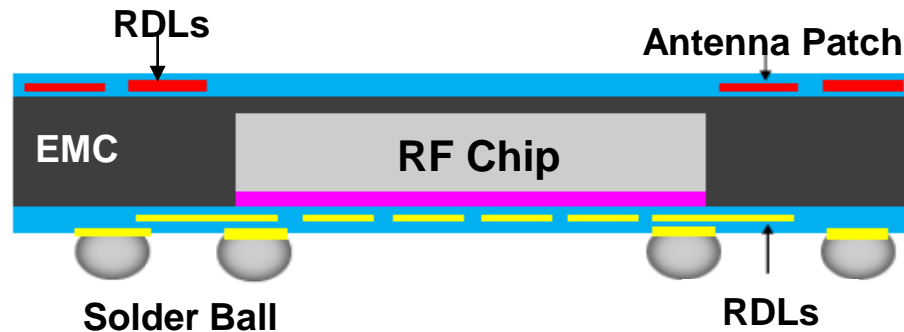
Antenna-in-Packaging (AiP)

IBM (ECTC2014) RF Flip Chips on Organic Substrate with Patch Antenna Array

- Patch antenna array
- Multi-chip Package
- C4
- RF ICs
- Power, ground and signals
- Pogo-pin interposer
- BGA balls
- Board
- Back-cover with air inlet
- Air
- Thermal hole and vias
- IC1 IC2
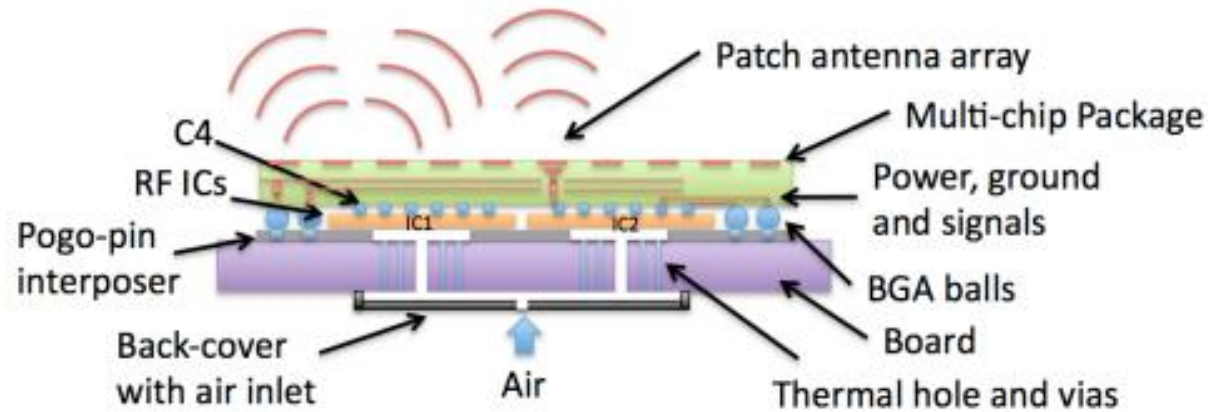
TSMC (ECTC2018) RF Flip Chips in Fan-Out EMC with Patch Antenna Array (InFO_AiP)

- RDLs
- Antenna Patch
- EMC
- RF Chip
- Solder Ball
- RDLs

THE TRANSMISSION LOSS FOR RDL AND SUBSTRATE TRACE AT 28 AND 38GHZ

Frequency	InFO RDLs	Substrate Trace
28GHz	0.175dB/mm	0.288dB/mm
38GHz	0.225dB/mm	0.377dB/mm

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TSMC's AiP Patent: US 10,312,112 (June 4, 2019)
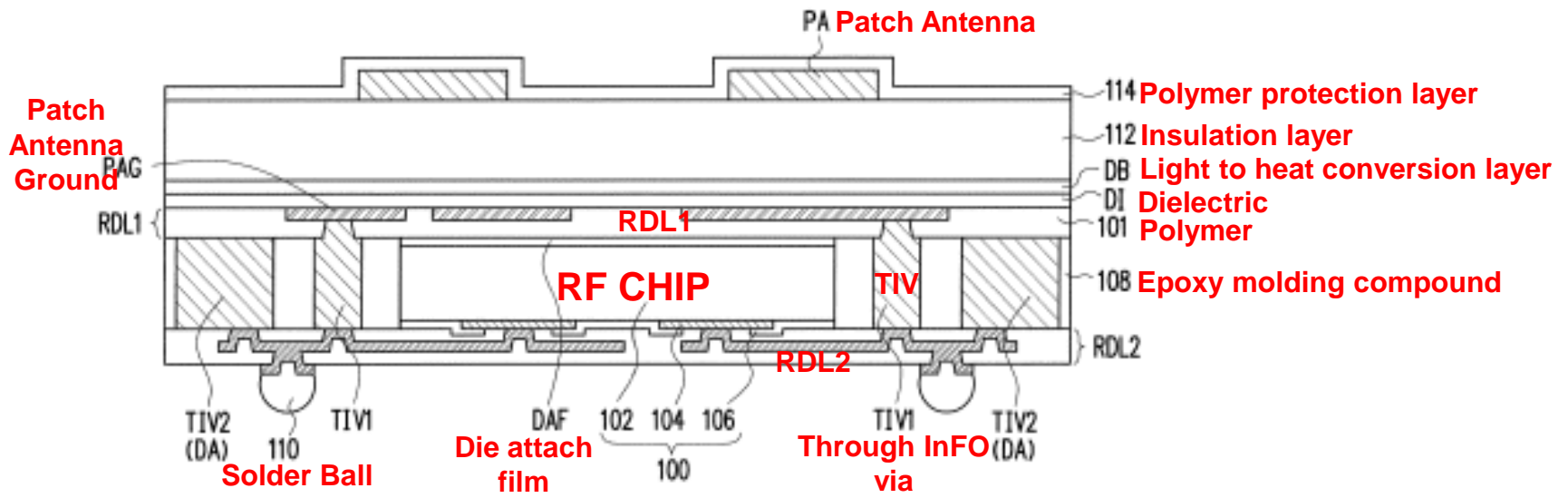
Fan-Out chip-first die Face-Up Process

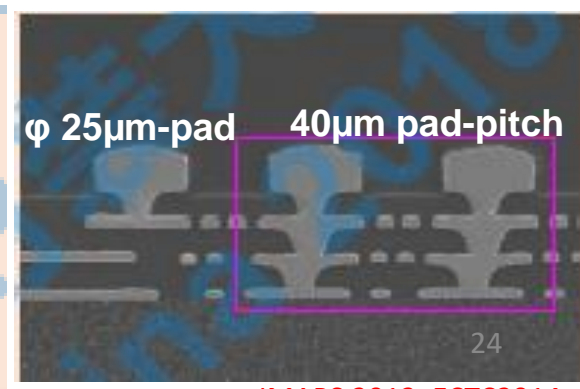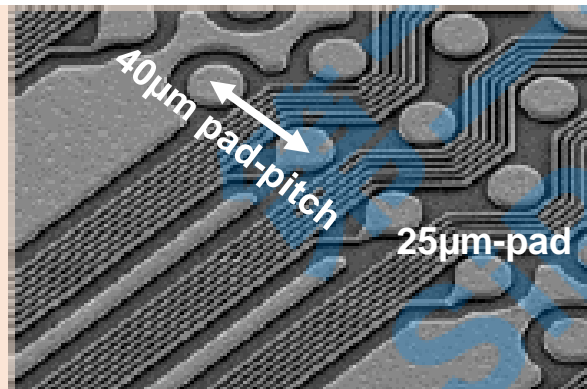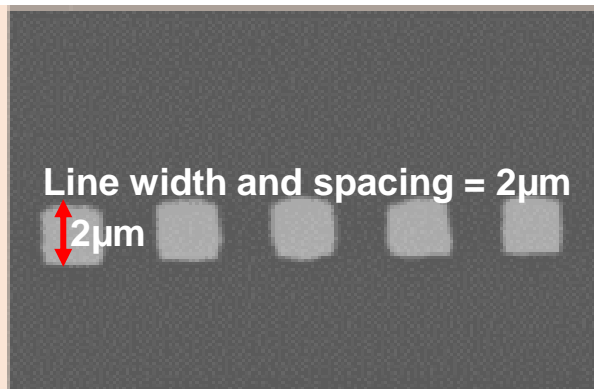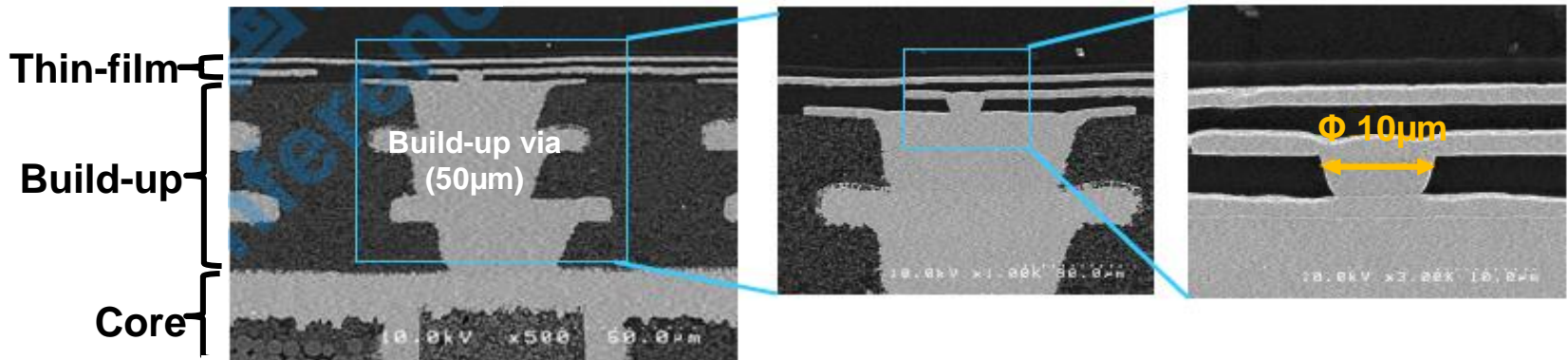# Unimicron's Heterogeneous Integration of Baseband and AiP Patent: TW 1,209,218 (November 1, 2020)
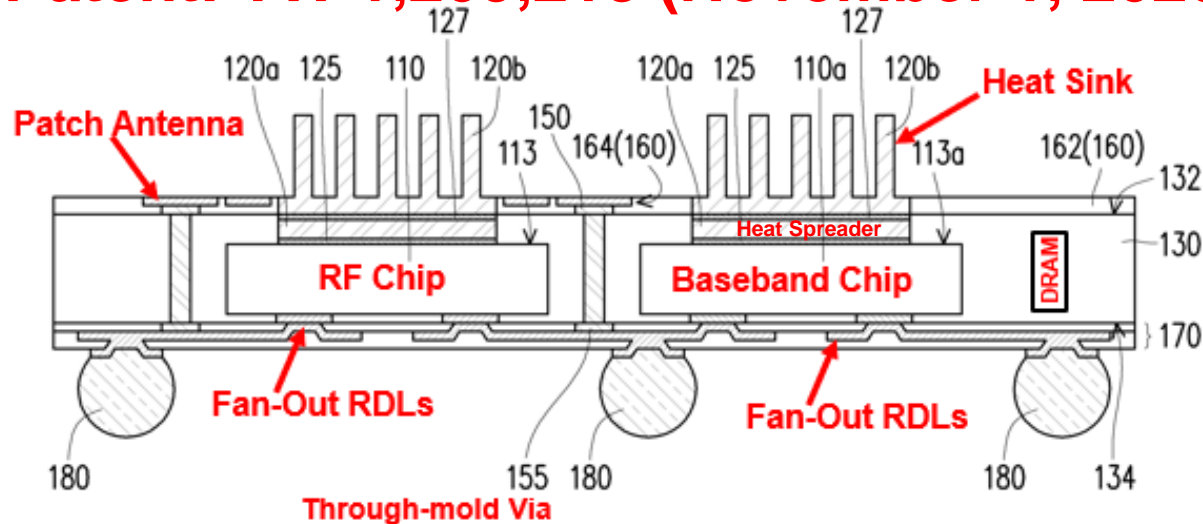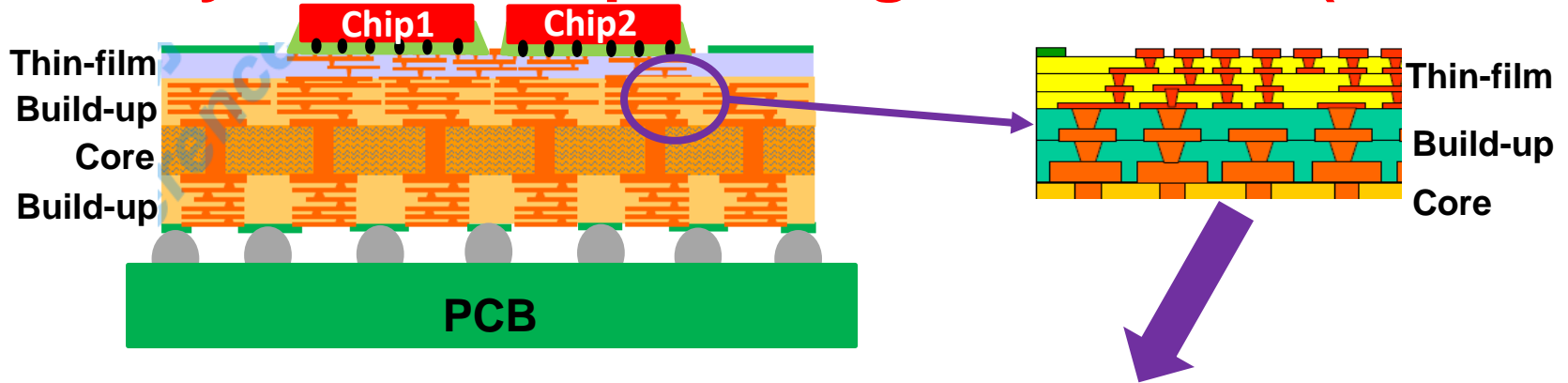

Fan-Out chip-first die Face-Down Process

2.1D IC Integration

➢ **Shinko's integrated thin-film high-density organic package (i-THOP)**

➢ **JECT's ultra format organic substrate (uFOS)**

2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (Shinko)

Thin-film
Build-up
Core
Build-up

Chip1 Chip2

PCB

Thin-film
Build-up
Core

Thin-film
Build-up via (50µm)
Core

Φ 10µm

Line width and spacing = 2µm
2µm

40µm pad-pitch
25µm-pad

φ 25µm-pad
40µm pad-pitch

24

2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (JCET)

uFOS

ABF/PP RDL2

E-STF

Chip 1   Chip 2

E-stiffener

PCB

8.23
1.04
2.78m
2.48m
8.23
Unit: µm
.4mm x4.00k SE(M)   10.0um

Carrier

Surface Treatment

PI Coating

Metal Formation

PI Coating

Laser via drill

Metal formation and laser via drill

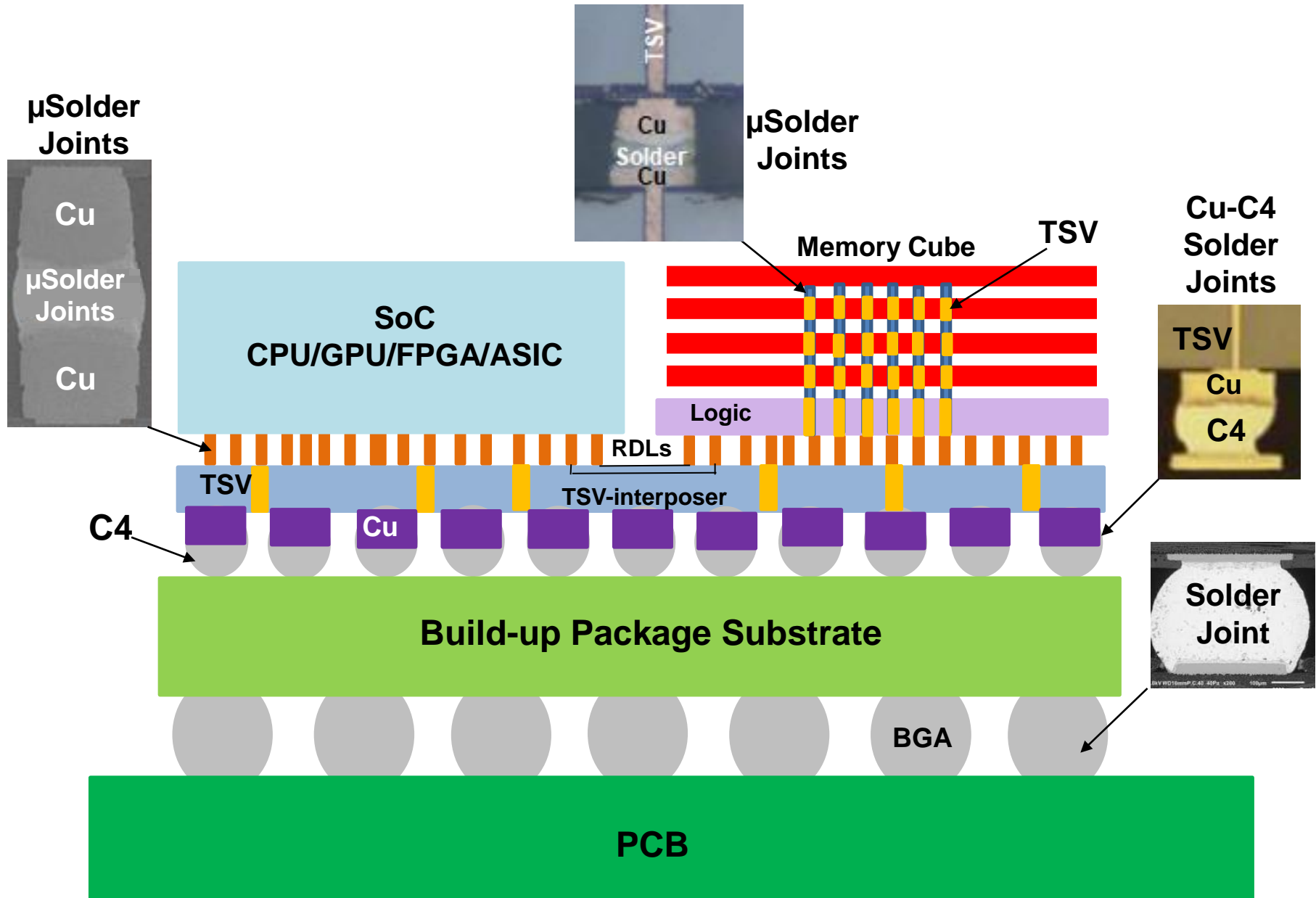Carrier removal

Backside Laser via

ENIG Finish
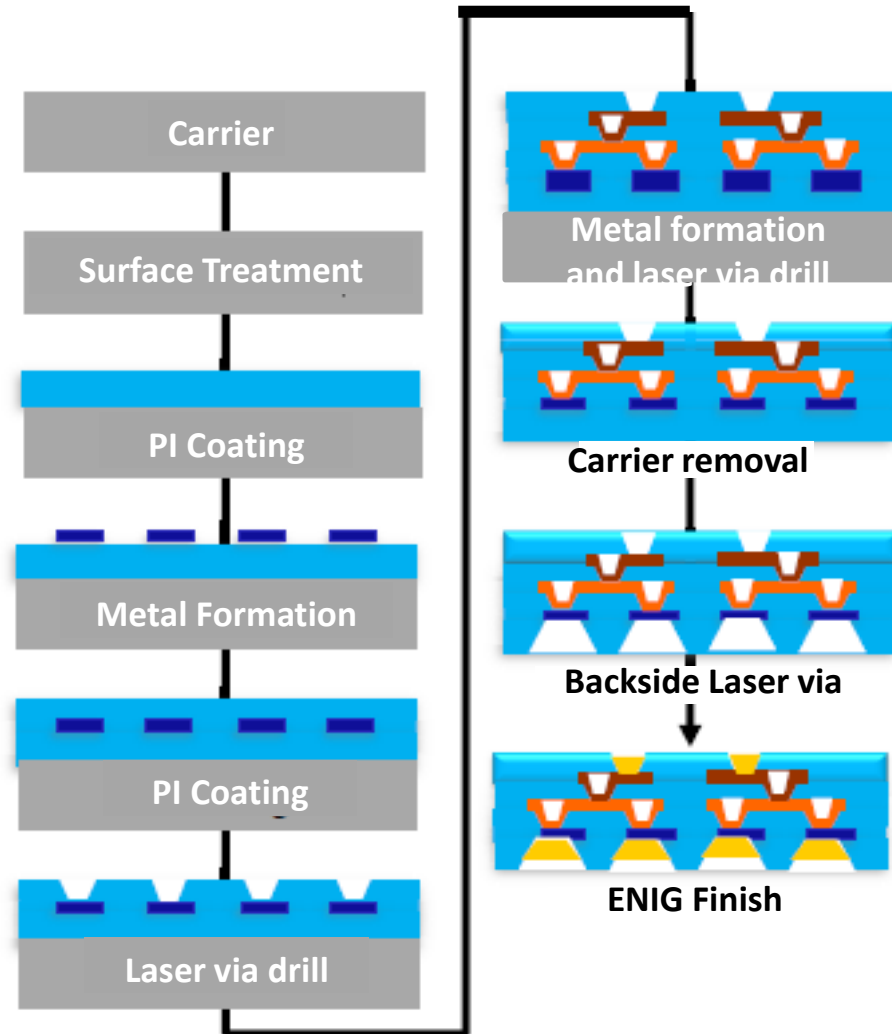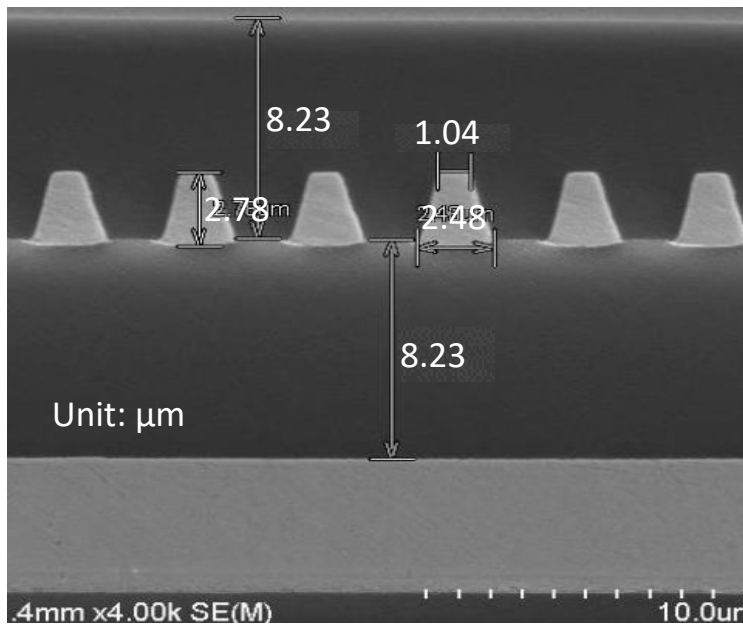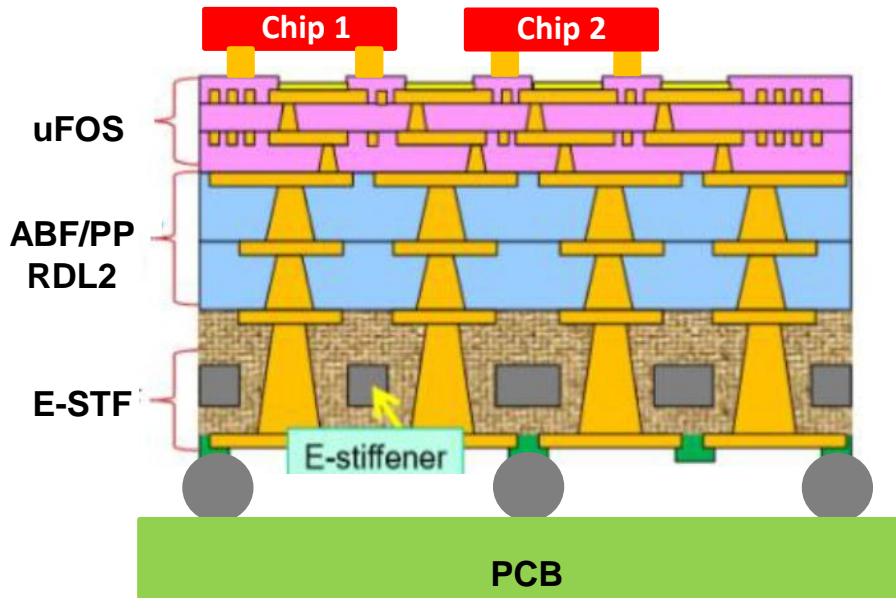
➤ **uFOS (ultra format organic substrate)**
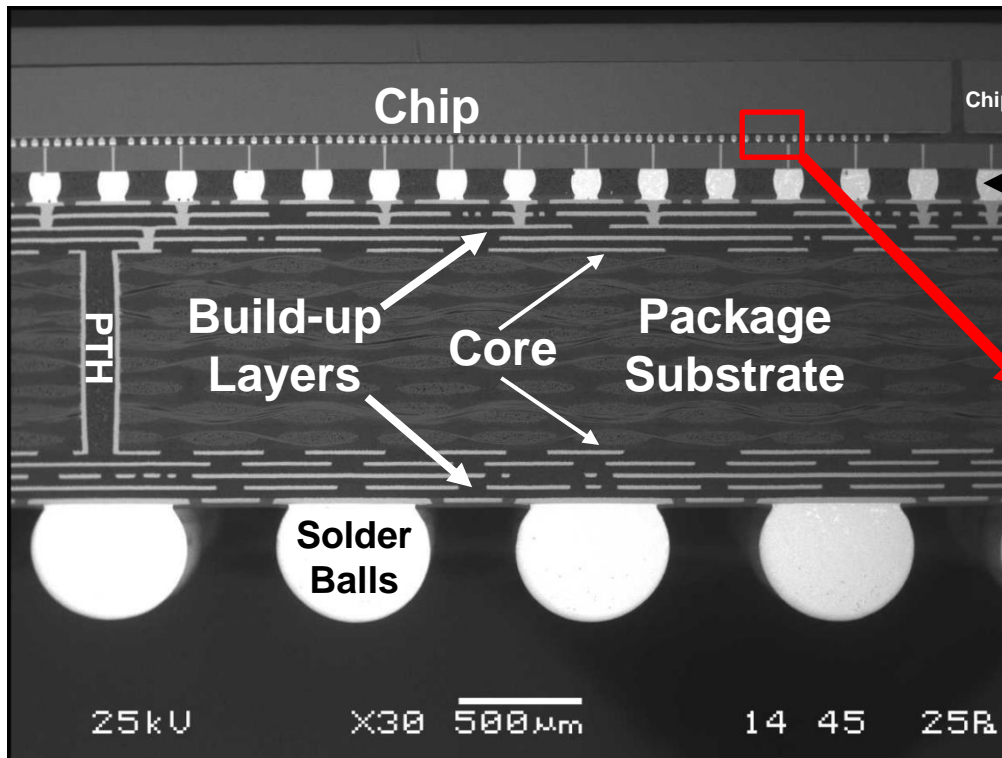➤ **e-STF (embedded stiffness)**

25

2.5D IC Integration

➢ **Examples: TSMC, Xilinx, AMD, Nvidia, Samsung**

➢ **TSV-less 2.5D by Samsung**

➢ **2.5D heterogeneous integration of PIC (photonic IC) and EIC (electronic IC)**

2.5D IC Integration

μSolder Joints

Cu

μSolder Joints

Cu

μSolder Joints

Cu
Solder
Cu

TSV

Memory Cube

TSV

Cu-C4 Solder Joints

TSV

Cu

C4

SoC
CPU/GPU/FPGA/ASIC

Logic

RDLs

TSV

TSV-interposer

C4

Cu

Build-up Package Substrate

Solder Joint

BGA

PCB
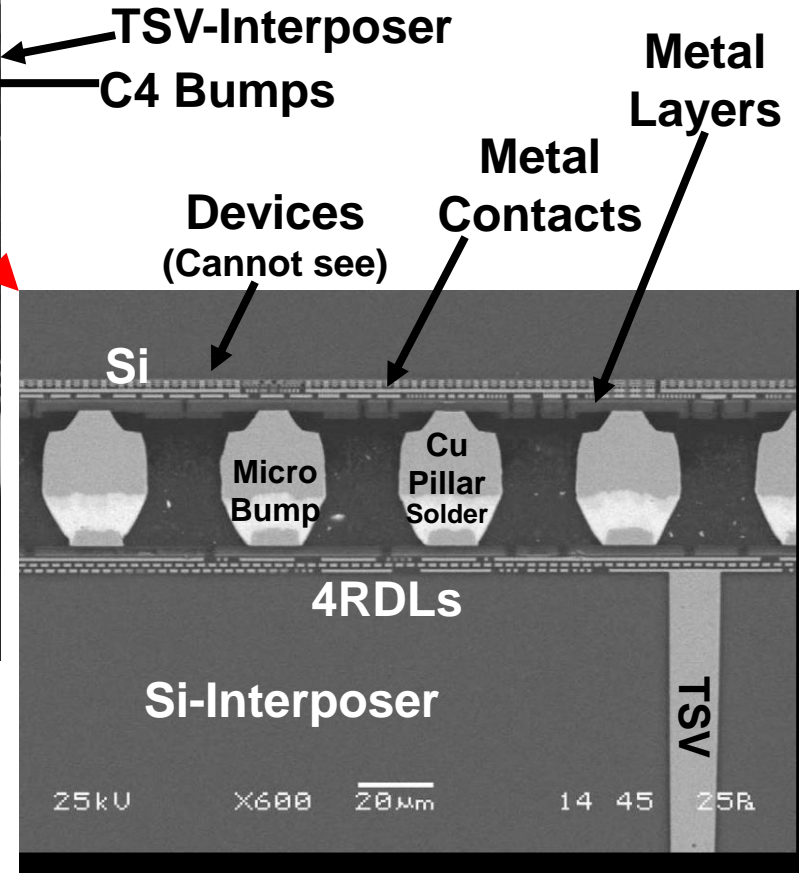
Semiconductors for HPC applications driven by AI and 5G

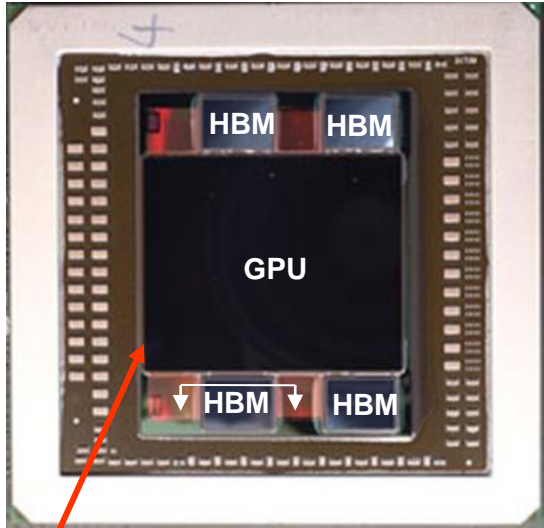# Xilinx/TSMC's 2.5D IC Integration with FPGA

CoWoS
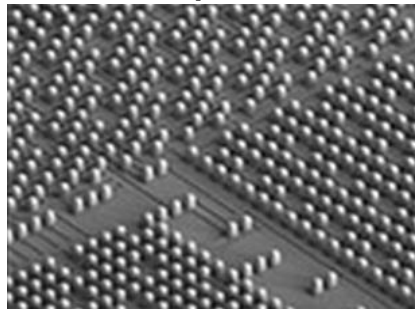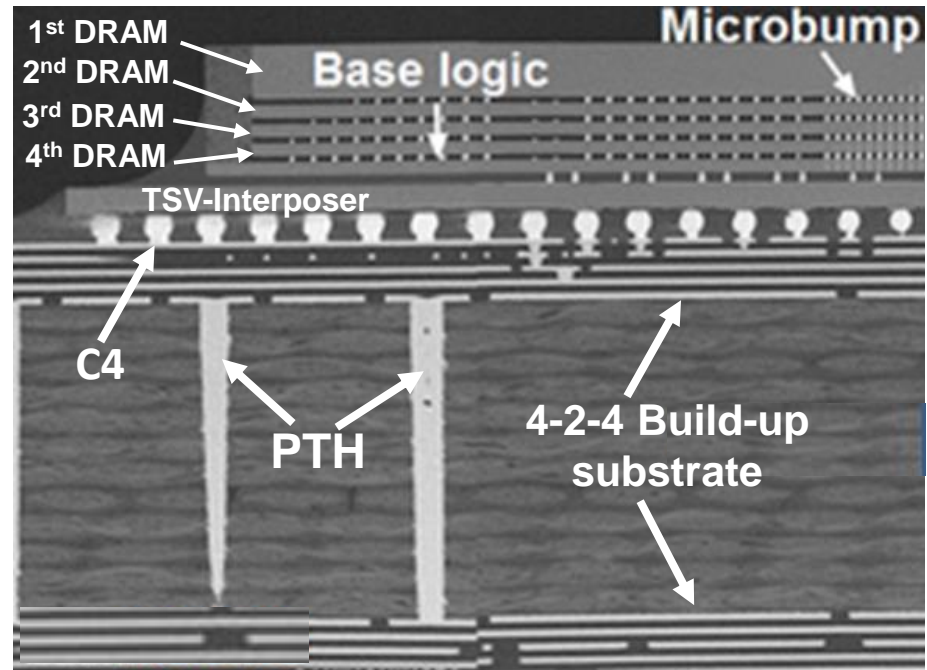(chip on wafer on substrate)

Homogeneous Integration on Si-substrate

➤RDLs: 0.4µm-pitch line width and spacing
➤Each FPGA has >50,000 µbumps on 45µm pitch
➤Interposer is supporting >200,000 µbumps

AMD's GPU (Fiji), Hynix's HBM, and UMC's Interposer

TSV-Interposer

Cu-Pillar with solder Cap

Solder

Cu

1st DRAM
2nd DRAM
3rd DRAM
4th DRAM

Base logic

Microbump

TSV-Interposer

C4

PTH

4-2-4 Build-up substrate

GPU with microbumps

TSV

C4
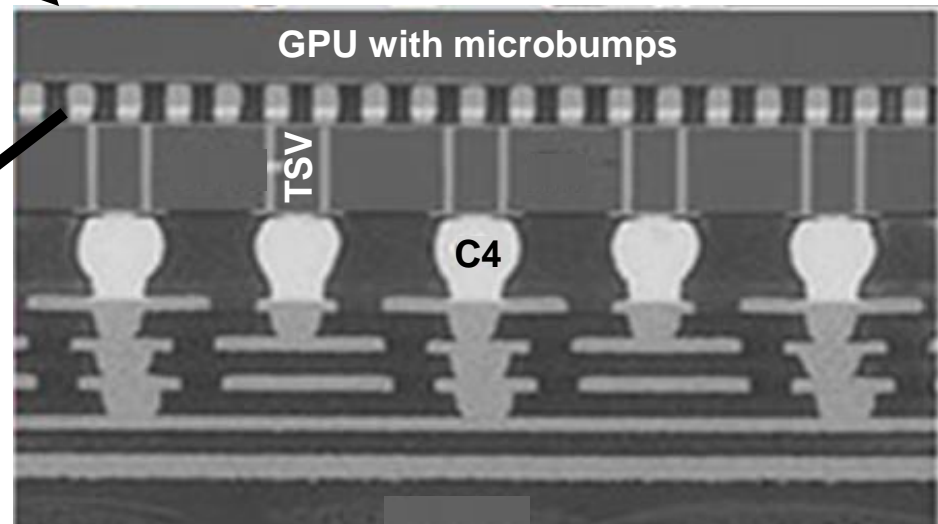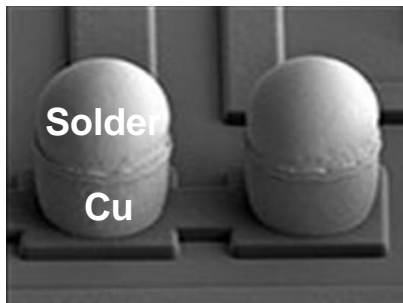
TSV-Interposer

Build-up organic substrate

29

NVidia's P100 with TSMC's CoWoS-2 and Samsung's HBM2
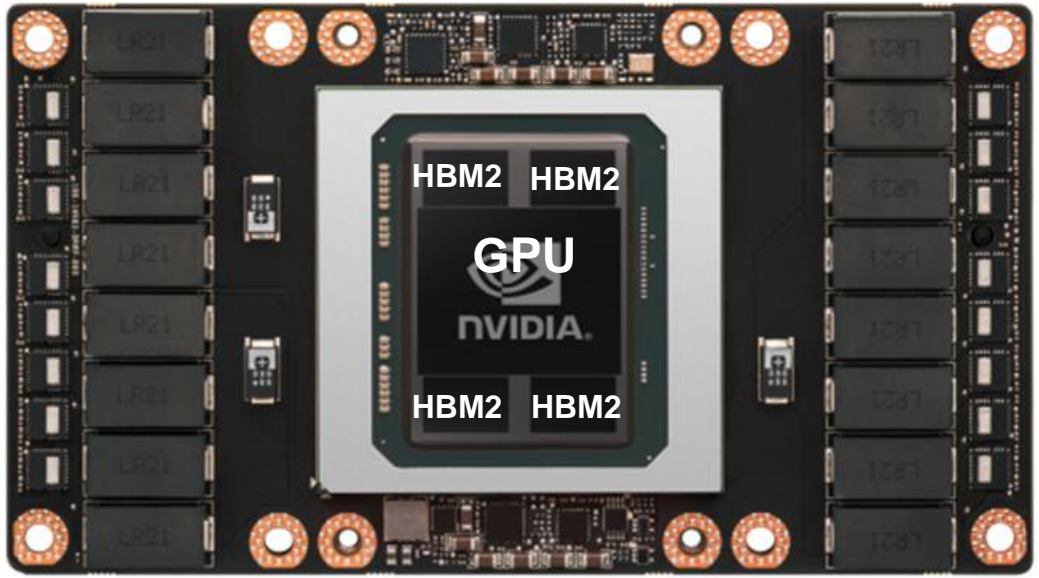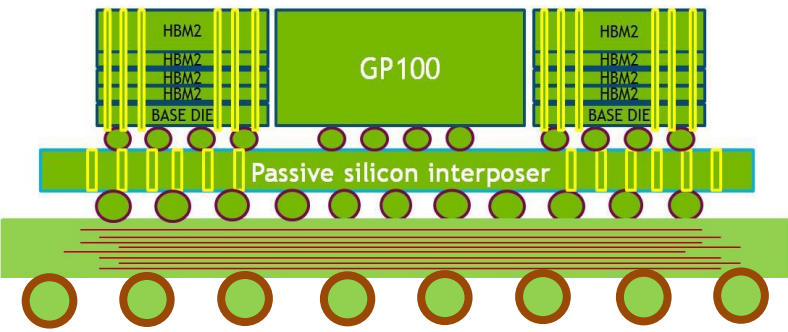
HBM2 by Samsung
4DRAMs

Base logic die

TSV Interposer
(CoWoS-2)

C4 bump

HBM2

GPU
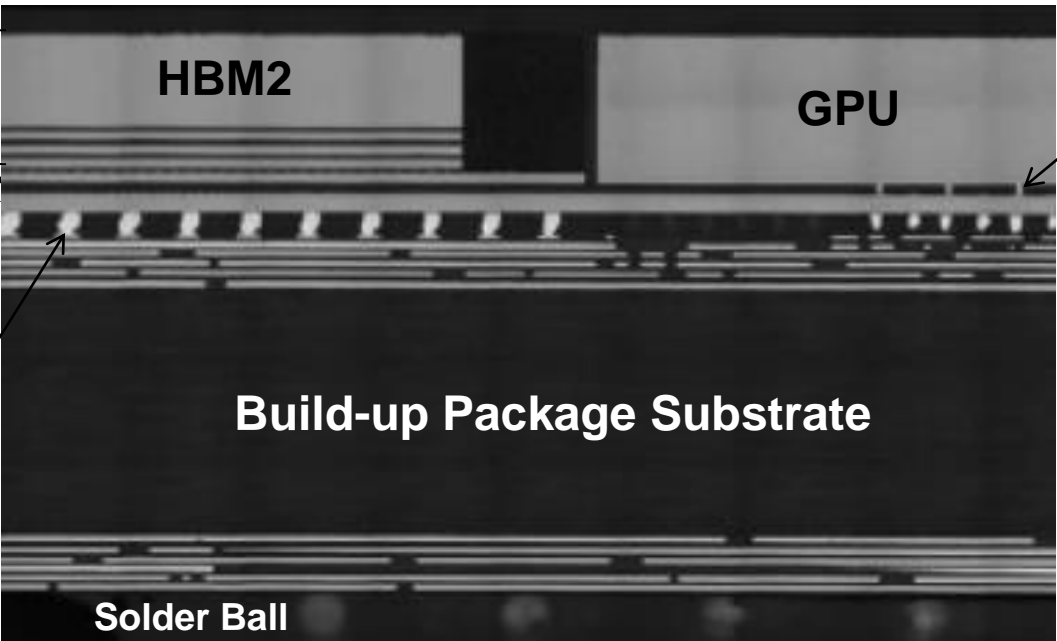
µbump

Build-up Package Substrate

Solder Ball

Samsung's Interposer-Cube4 (I-Cube4) (2.5D IC Integration)

TSV Interposer

HBM

HBM

SoC

HBM

HBM

Package Substrate

Top View

Bottom View

HBM

SoC

DRAM

TSV

µbump

µbump

TSV-Interposer

C4 bump

Cross-section View

Package Substrate

Solder Ball

PCB
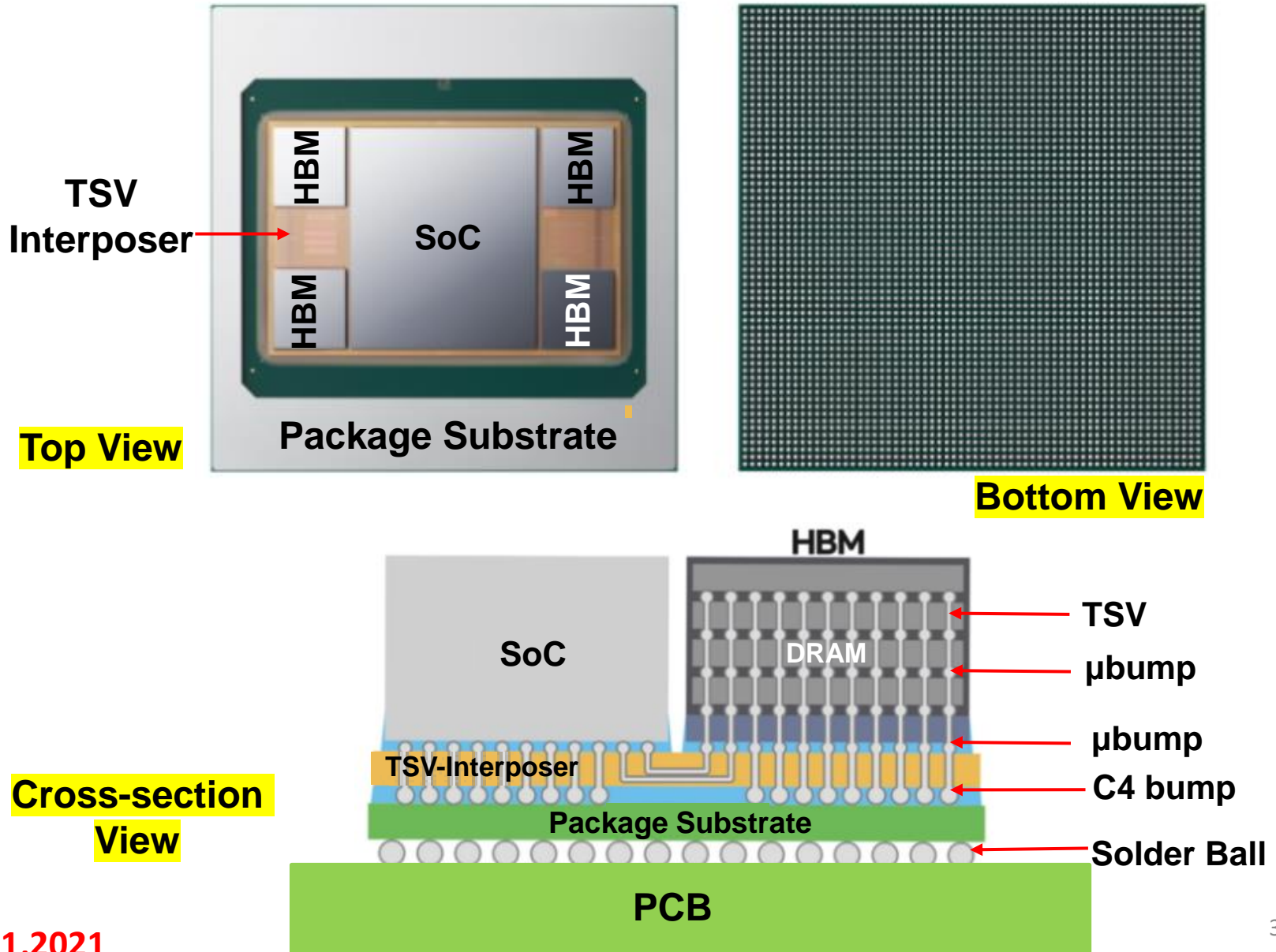
2.5D Integration Hybrid Substrate Cube (H-Cube) Solution for High Performance Applications

Samsung Announcement November 11, 2021
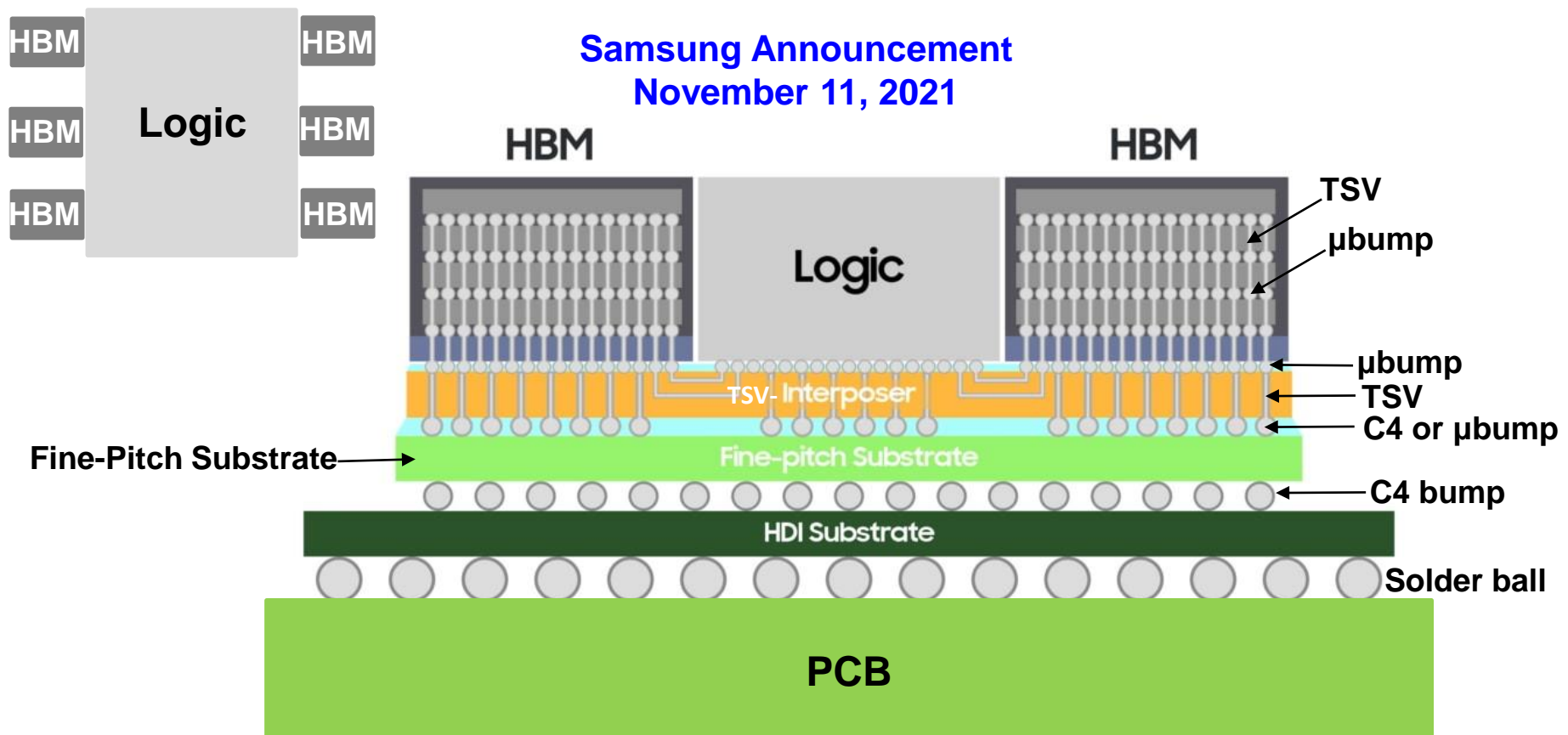
H-Cube Concept

When integrating six or more HBMs, the difficulty in manufacturing the large-area substrate increases rapidly, resulting in decreased efficiency. Samsung solved this problem by applying a hybrid substrate structure in which HDI substrates that are easy to implement in large-area are overlapped under a high-end fine-pitch substrate. By decreasing the pitch of solder ball, which electrically connects the chip and the substrate, by 35% compared to the conventional ball pitch, the size of fine-pitch substrate can be minimized, while adding HDI substrate (module PCB) under the fine-pitch substrate to secure connectivity with the system board.

November 2021

Novel 2.5D RDL Interposer Packaging: A Key Enabler for the New Era of Heterogenous Chip Integration (R-Cube)

Min Jung Kim, Seok Hyun Lee, Kyoung Lim Suk, Jae Gwon Jang, Gwang-Jae Jeon, Ju-il Choi, Hyo Jin Yun, Jongpa Hong, Ju-Yeon Choi, Won Jae Lee, SukHyun Jung, Won Kyoung Choi and Dae-Woo Kim Test & System Package (TSP), Samsung Electronics Co., Ltd, Cheonan-si, Chungcheongnam-do, South Korea, South Korea mj3076.kim@samsung.com
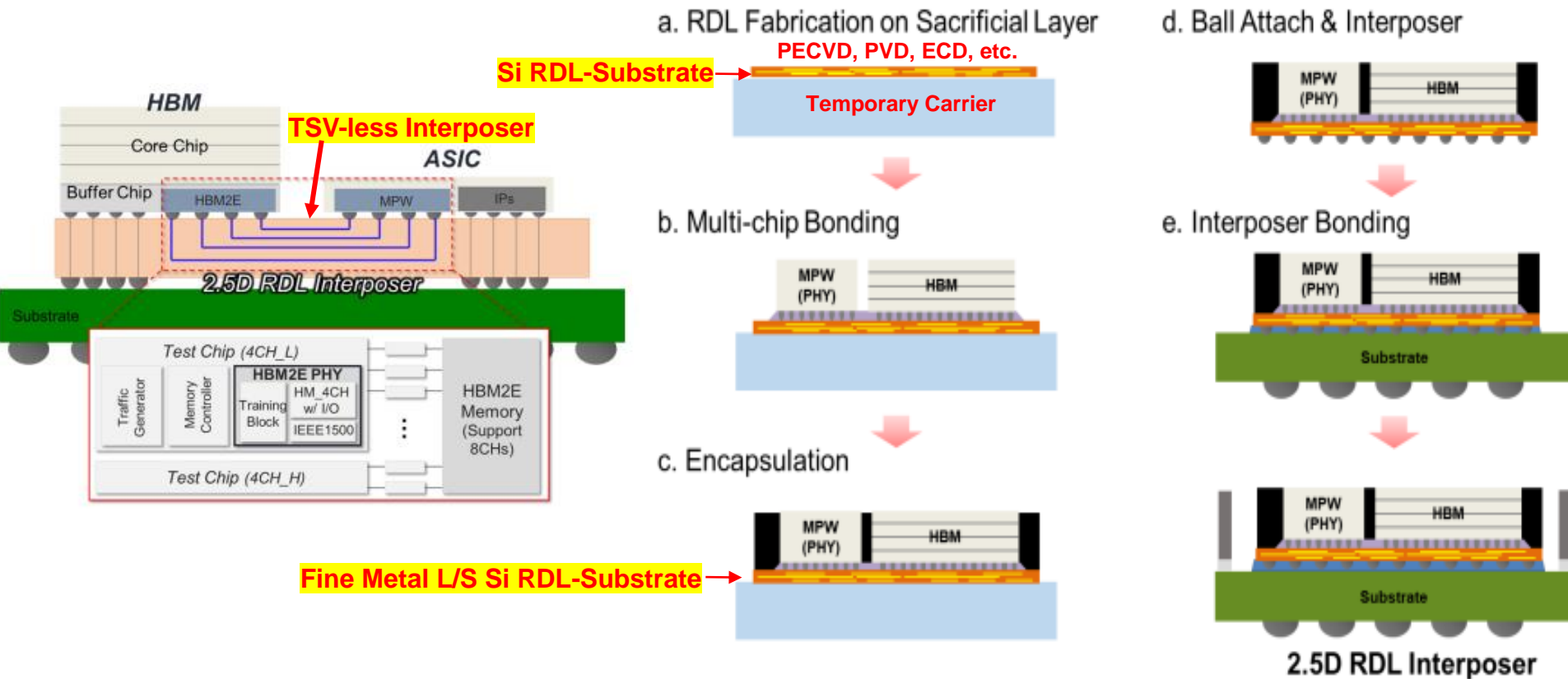
2.5D Heterogeneous Integration of EIC and PIC Devices
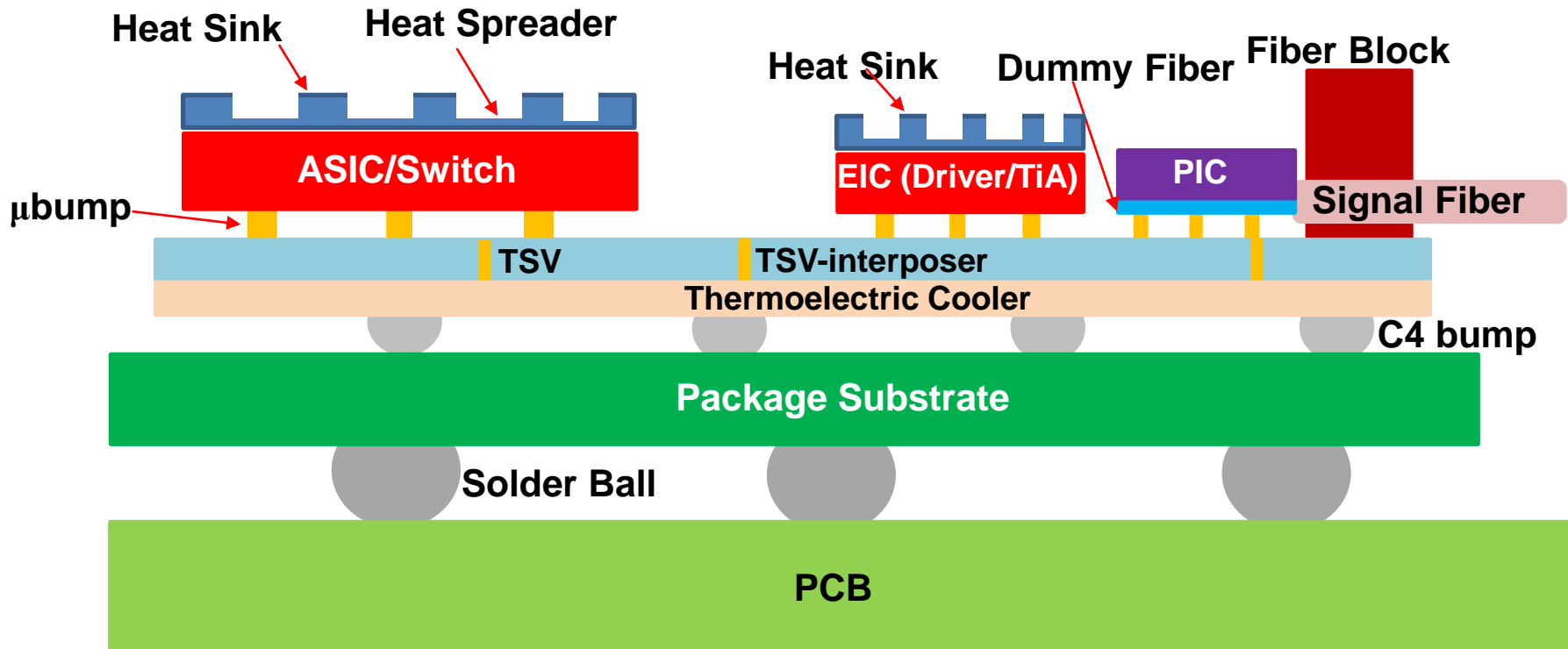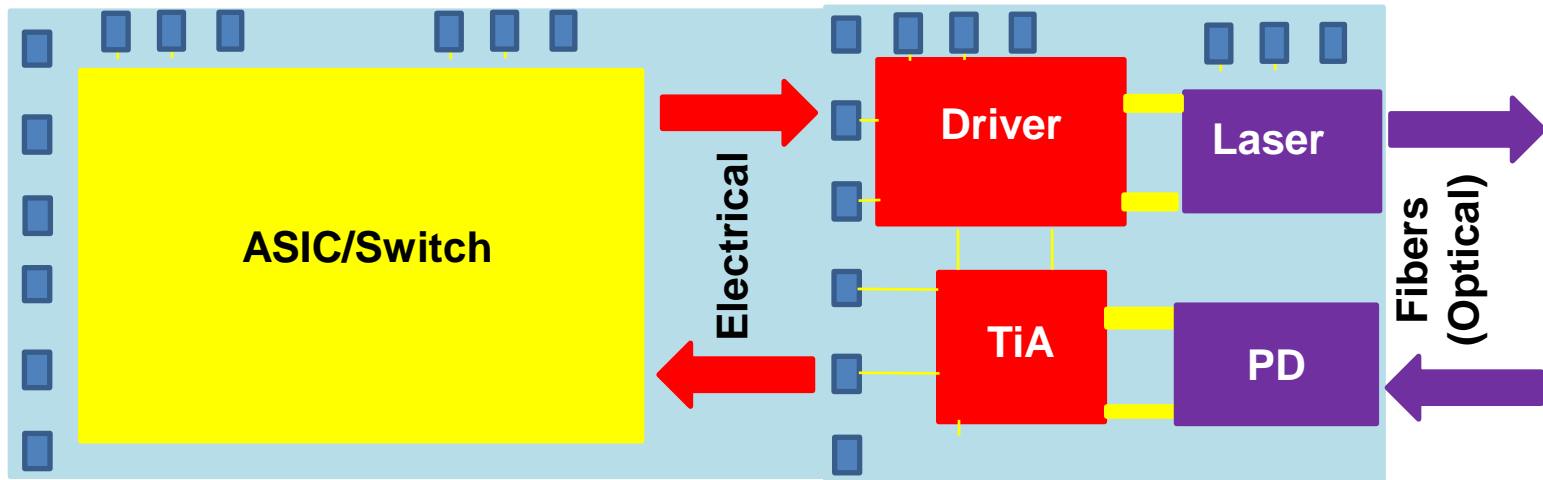
2.3D IC Integration

➢ **Chip-First (either face-up or face-down)**

➢ **Chip-Last (RDL-First)**

2.1D, 2.3D, and 2.5D IC Integration

Fine Metal L/S RDL-Substrate = Thin-Film Layer

Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions

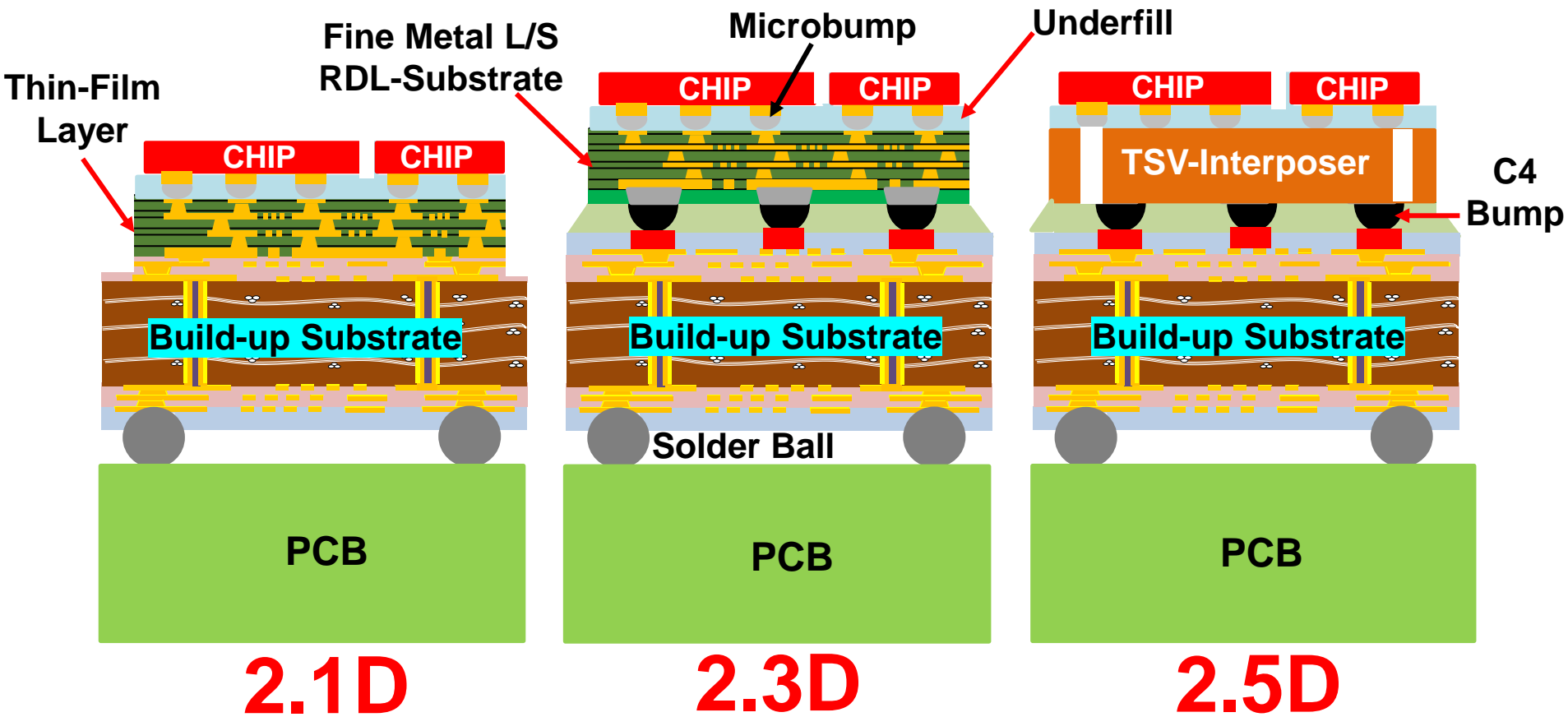**Seung Wook Yoon, Patrick Tang, Roger Emigh, Yaojian Lin, Pandi C. Marimuthu, and Raj Pendse**
STATSChipPAC Ltd., 5 Yishun Street 23, Singapore 768442

Chip-First

TSV interposer — μbump — Underfill-1 — Underfill-2 — Logic — Analog — C4 bump — Solder Ball — Organic Substrate
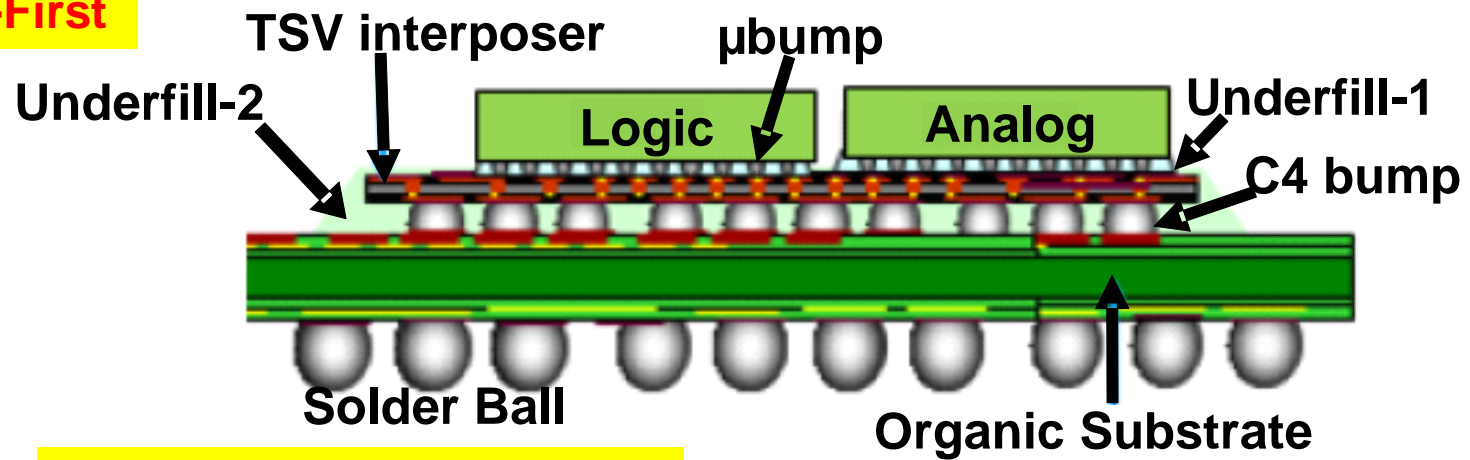
> The μbump, underfill-1, and TSV-interposer are eliminated.
> The RDLs are made by fan-out technology.

EMC — RDLs — Underfill-2 — Logic — Analog — C4 bump — Solder Ball — Organic Substrate
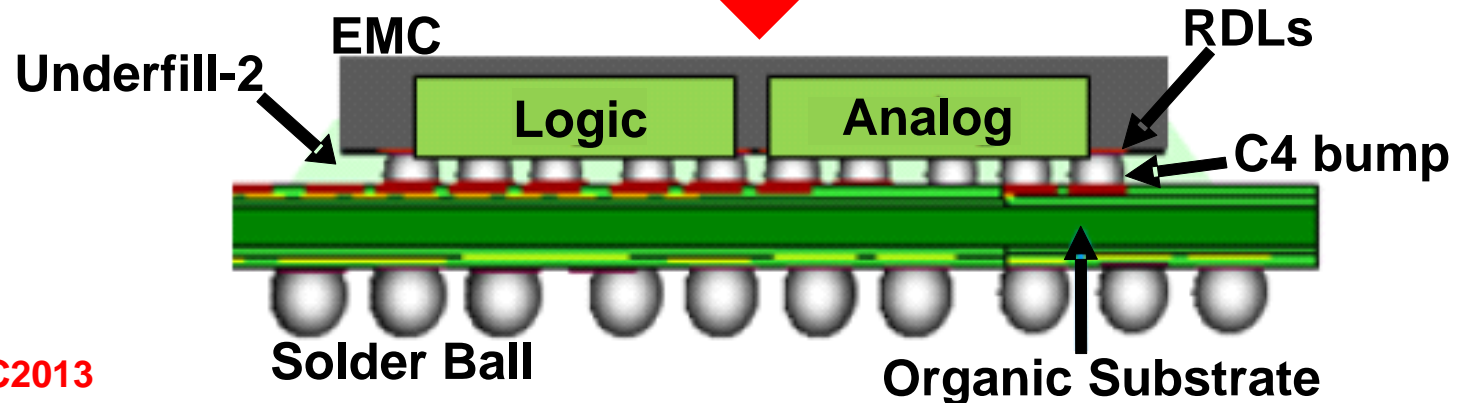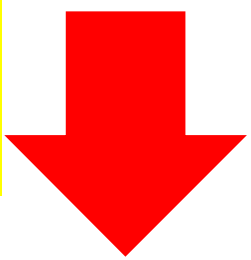
Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

John H Lau, Gary Chang-Fu Chen, Jones Yu-Cheng Huang, Ricky Tsun-Sheng Chou, Channing Cheng-Lin Yang, Hsing-Ning Liu, and Tzvy-Jang Tseng

Unimicron Technology Corporation,
Taoyuan City, Taiwan
John_Lau@unimicron.com

Chip-Last

EMC

Chip 1 **Chip 2**

Solder Cap Pad

µbump **Underfill** Cu

DL01
ML1
DL12
ML2
DL23
ML3

RDL1 (2µm)
RDL2
RDL3

C4 bump **Underfill**

Solder Mask **Pad**

Build-up Package Substrate

Solder Mask

Solder Ball

Not-to-scale

Underfill

Chip 1 Chip 2

Fine L/S RDL-substrate

Build-up substrate

CHIP

Solder **Cu-pillar**

C4 RDLs Underfill

Build-up Layers

Build-up Package Substrate

38
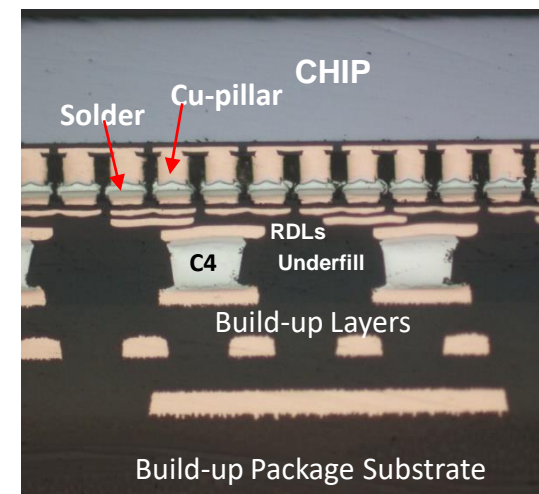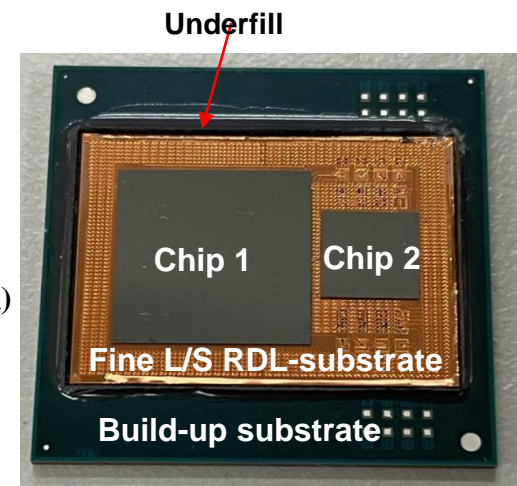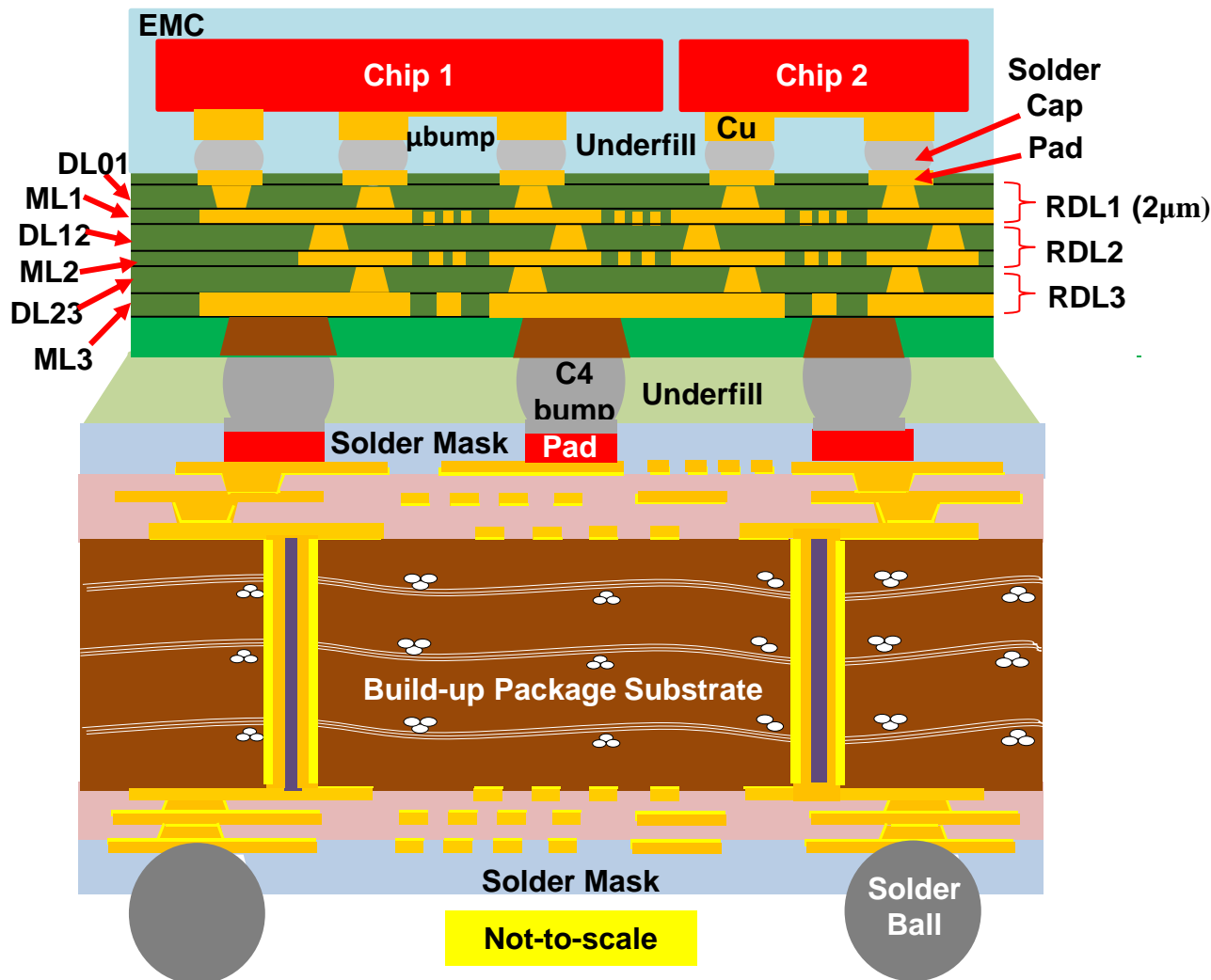
High-Density Hybrid Substrate for Heterogeneous Integration

Chia-Yu Peng , John H. Lau , Life Fellow, IEEE, Cheng-Ta Ko, Paul Lee, Eagle Lin, Kai-Ming Yang, Puru Bruce Lin, Tim Xia, Leo Chang, Ning Liu, Curry Lin, Tzu Nien Lee, Jason Wong, Mike Ma, Tzyy-Jang Tseng

Unimicron

Chip-Last

Flip chip with µbump

Fine metal L/S RDL-substrate

Interconnect-Layer

Build-up substrate or HDI

Solder Ball

20mm

20mm

Chip 2B

Chip 1

Chip 2A

Underfill

Hybrid Substrate

CHIP 1

CHIP 2A

Cu-pillar Solder

Underfill

RDLs

ML1 ML2

PAD

Via filled with conductive paste

Interconnect-Layer

8-Layer HDI

2.3D Heterogeneous Integration of EIC and PIC Devices

Chip-Last

ASIC/Switch

Driver

Laser

Electrical

Electrical

TiA

PD

Fibers (Optical)

EMC

Underfill

µbump

Heat Sink

Heat Sink

ASIC/Switch

EIC (Driver/TiA)

PIC (Laser/PD)

Fiber

Fine metal L/S RDL-substrate

Fiber Block

C4 bump

C4 bump

Package Substrate

Solder Ball

PCB

3D IC Integration

- ➢ **3D IC Packaging (without TSVs)**

- ➢ **3d IC Integration (with TSVs)**
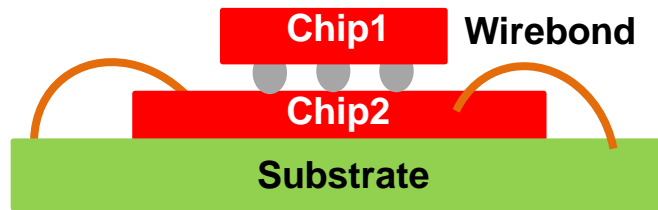
3D IC Packaging (without TSVs)

3D IC Packaging

(a)

Wirebond
Wirebond
Memory3
Memory2
Memory1
Substrate

(b)

Chip1
Wirebond
Chip2
Substrate

(c)

Wirebond
Chip1
Chip2
Substrate

(d)

Chip1
Chip2
Substrate

(e)

Memory
Memory
Chip
Package Substrate
PCB

(f)

EMC
Memory
Memory
EMC
Chip
Fan-out RDLs
PCB

43
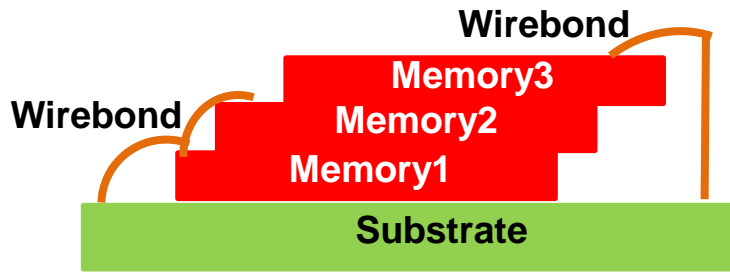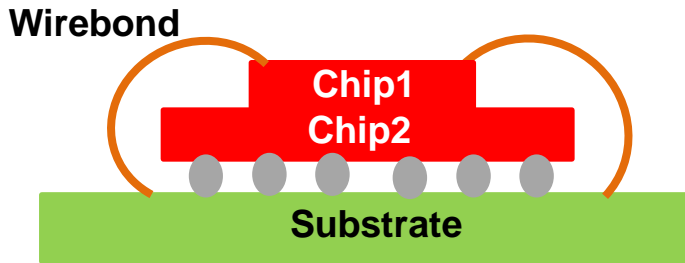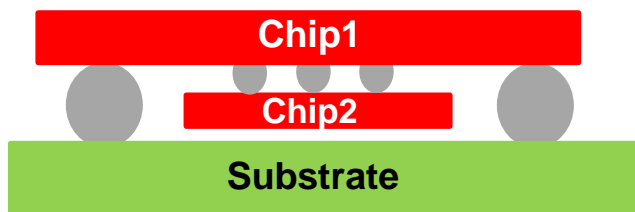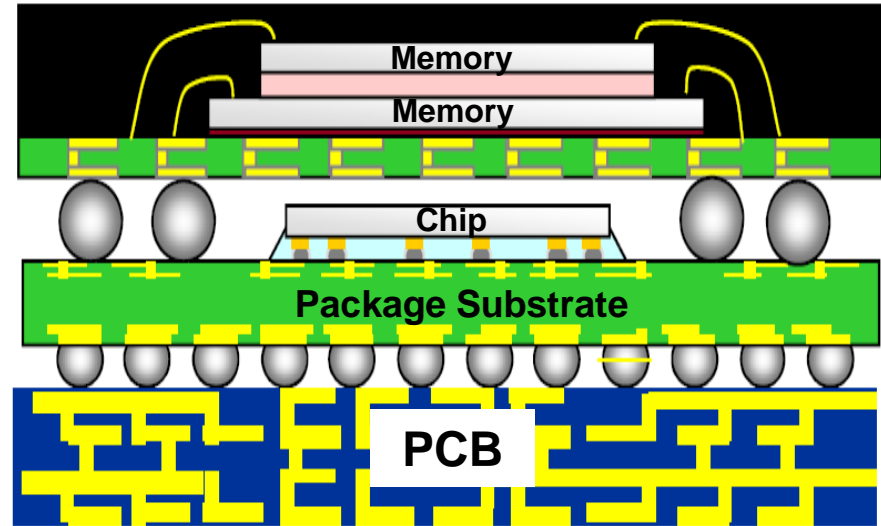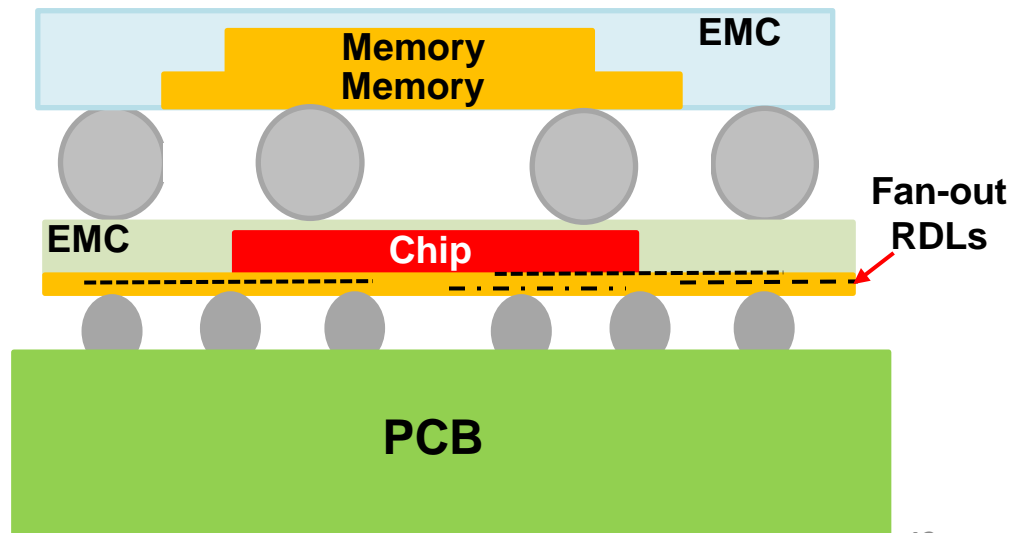
3D (Wirebonding) IC Packaging

(a) Top Chip, Bottom Chip, Wires, Substrate

(b) Chip, Chip, Chip, Wires — CPK LEI 15.0kV x70 100μm WD26mm

(c) 1.1 mm — 16 Samsung 48L V-NAND die (40μm-thick), Wires, Coreless substrate, Solder ball
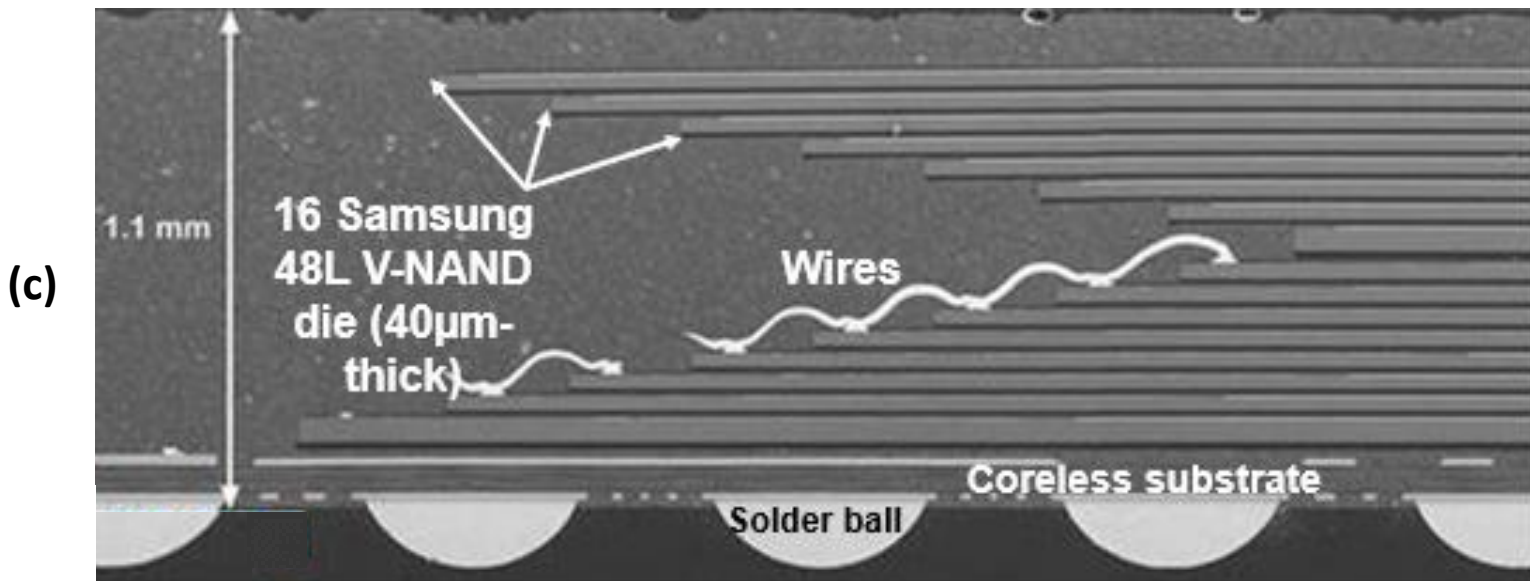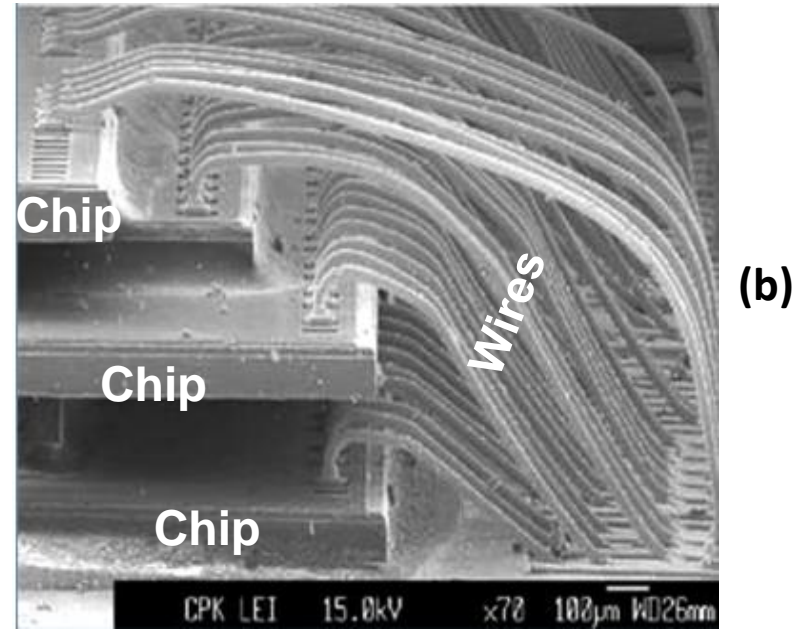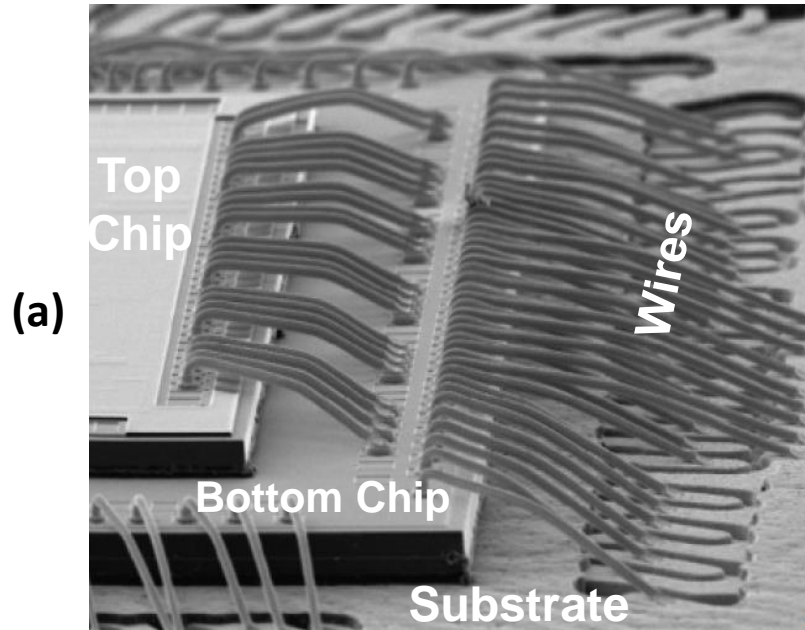
3D (Flip Chip and Wirebond) Packaging

8mm x 9mm x 580μm

(a)

- Wirebond
- Mold
- DRAM
- Baseband AP
- 3L ETS
- PCB
- Cu-Pillar with solder cap

- DRAM (75μm)
- Die attach (20μm)
- Baseband AP (75μm)
- Wirebond
- 115μm
- Molded Underfill
- Solder
- 0.35mm

(b)

- Heat spreader/sink (optional)
- SoC/Logic
- Memory
- Solder Ball
- Rigid or Flex Substrate

- Underfill
- Daughter die
- Mother die

45
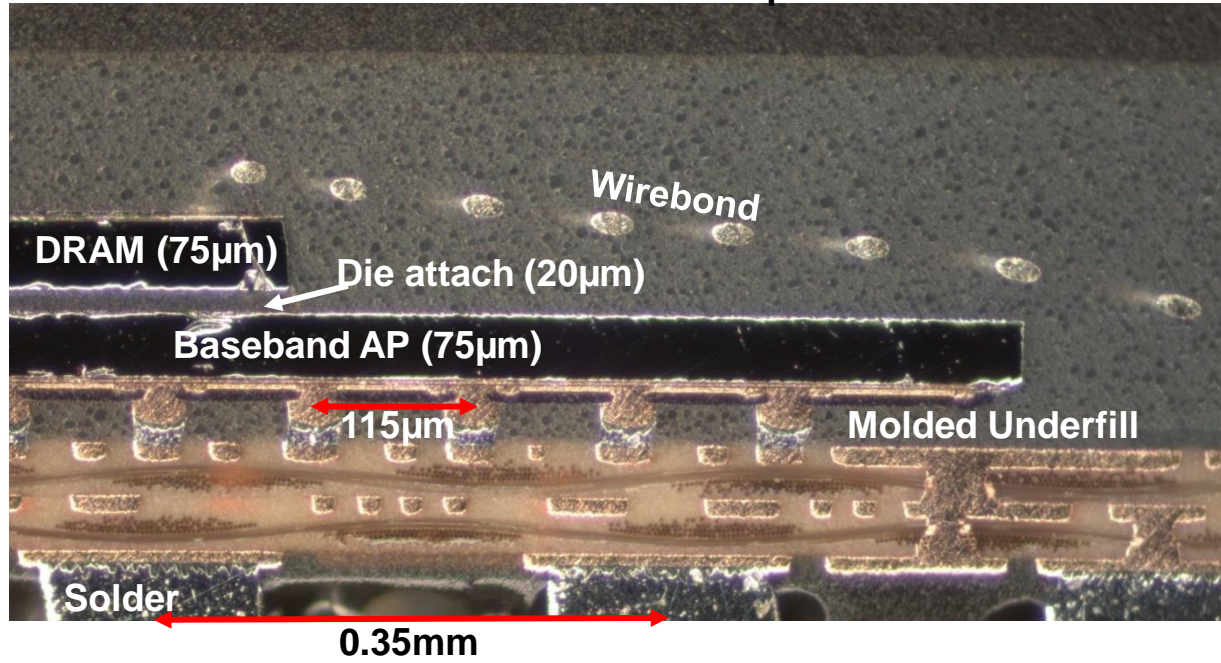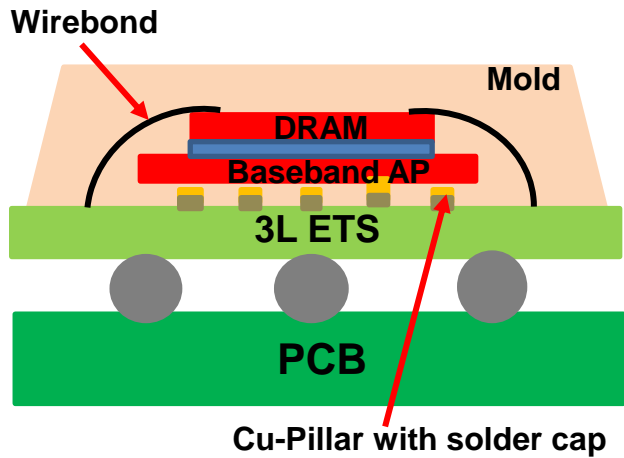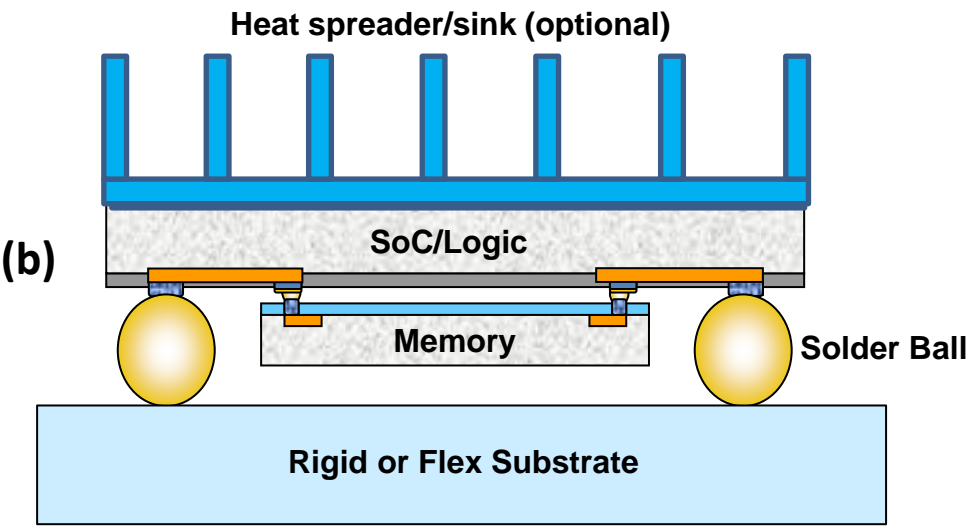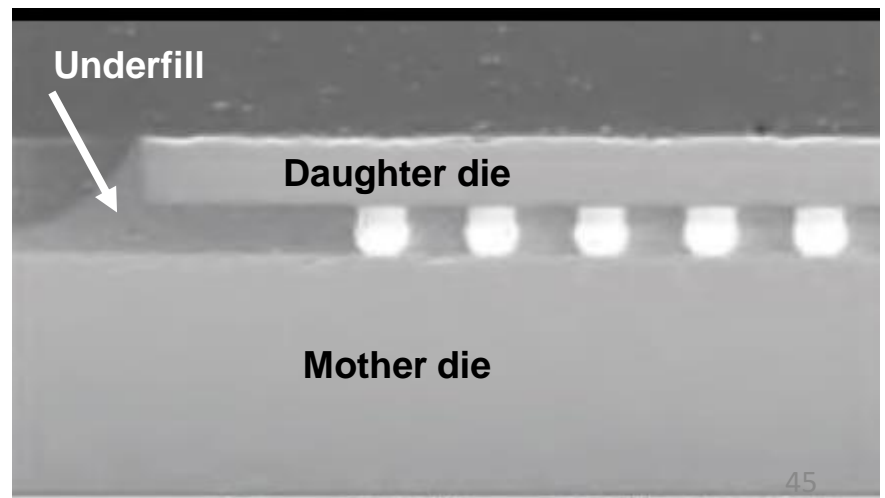
3D (PoP with flip chip) IC Packaging (Qualcomm)

Overmold memory package

25GBps LPDDR3 (cross-stack with Ag wires)

Chip

Chip

Coreless substrate

Upper substrate

504 Solder joints between package

1-2-1 build-up substrate

Shinko's MCeP®

Overmold flip chip package

Qual Snapdragon 805
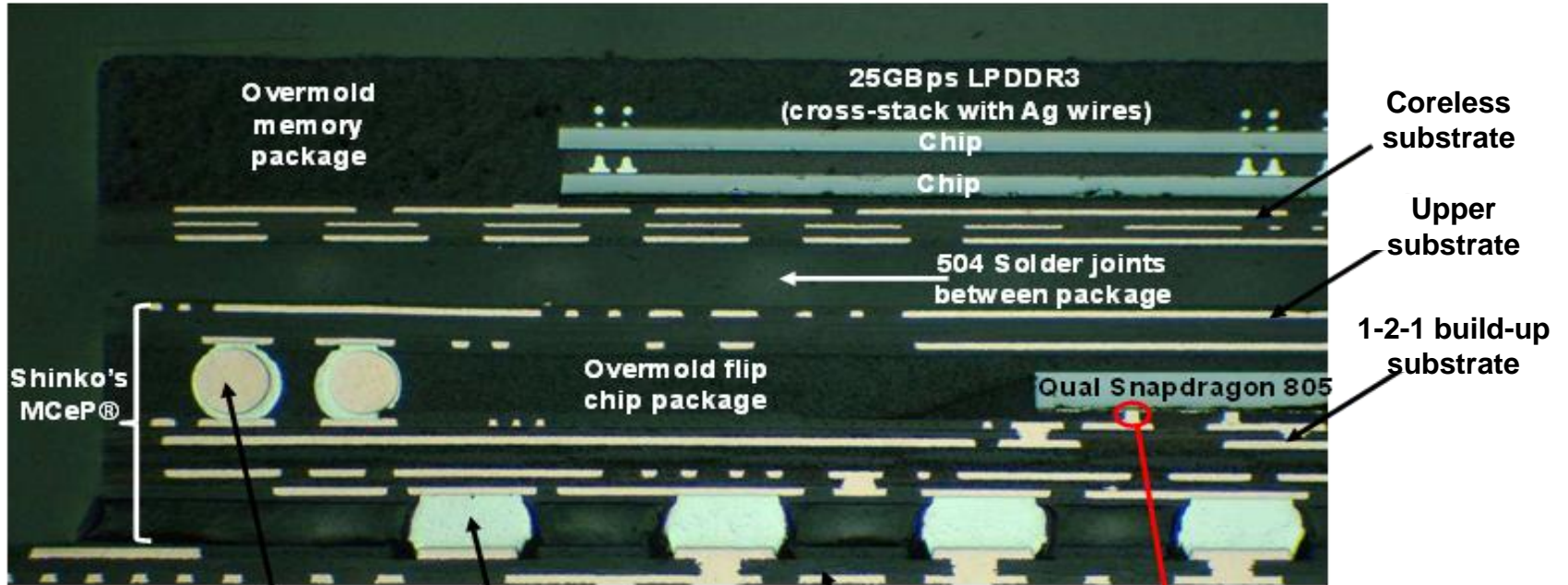
408 Cu core balls **994 Solder balls** **PCB**

TC-NCP Solder

Cu Pillar

Lead

Snapdragon 805 Processor:
❑ **10.9mm x 11mm x 95μm**
❑ **CuSnAg bumps @110μm pitch**
❑ **30μm bump-height after TC-NCP**

Mold Resin

Cu Core Solder Ball

Shinko's MCeP

Upper Substrate

Embedded Layer

Bottom substrate
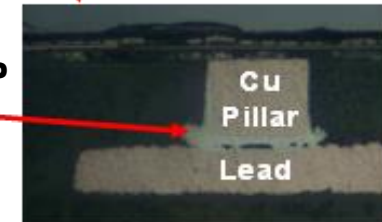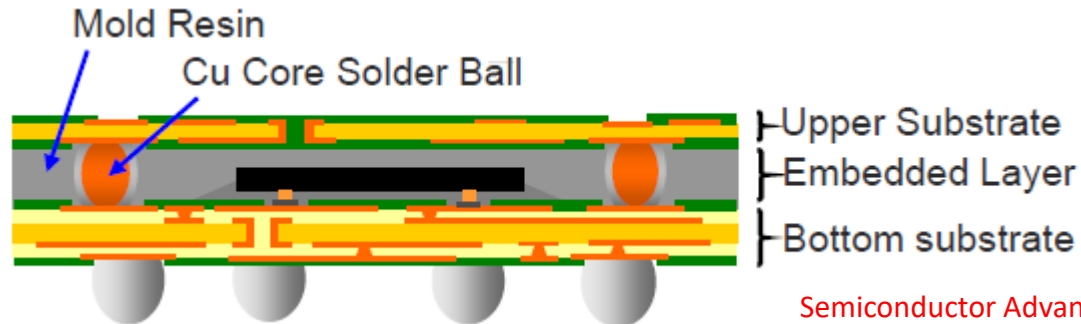
3D PoP: Apple/TSMC InFO (Integrated fan-Out) for the iPhone Application Processor (Chip-First Die Face-up)

SoC
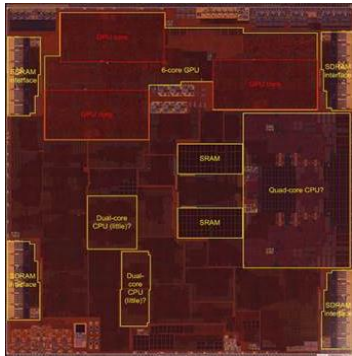
11.6mm x 10.8mm x 165μm

PoPzzz

APL0598 339S0176

GKBC40HI 1213

15.5mm x 14.4mm

K3PE7E700F - XGC2

tsmc

3SC0091 1222

15.5mm x 14.4mm x 825μm

3-Layer Coreless Package Substrate

Wirebond

Molding

Memory   Memory

Solder Ball   Underfill

EMC   AP A10   TIV

3RDLs

Solder Ball

Wire bond   Over mold (~170μm)

LPDDR4 Memory (105μm)

Coreless substrate

Underfill

A10 AP (165μm)

3RDLs
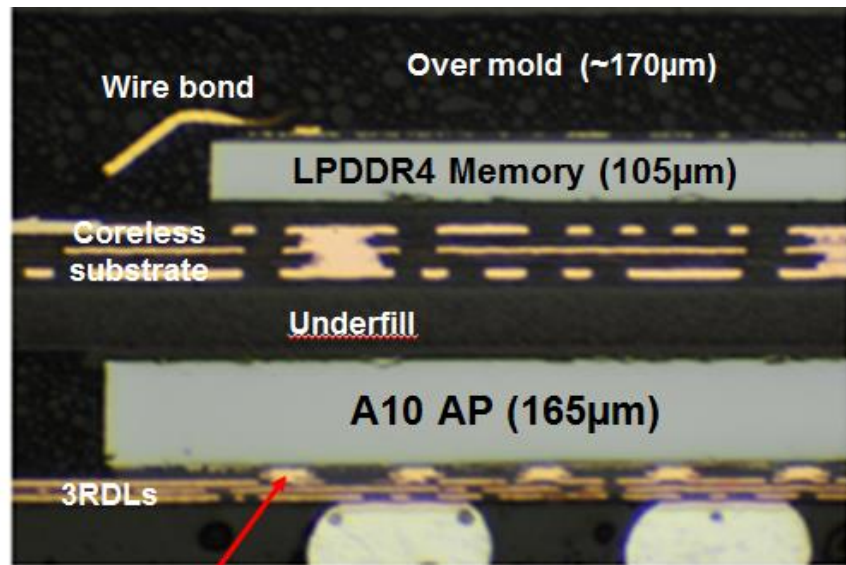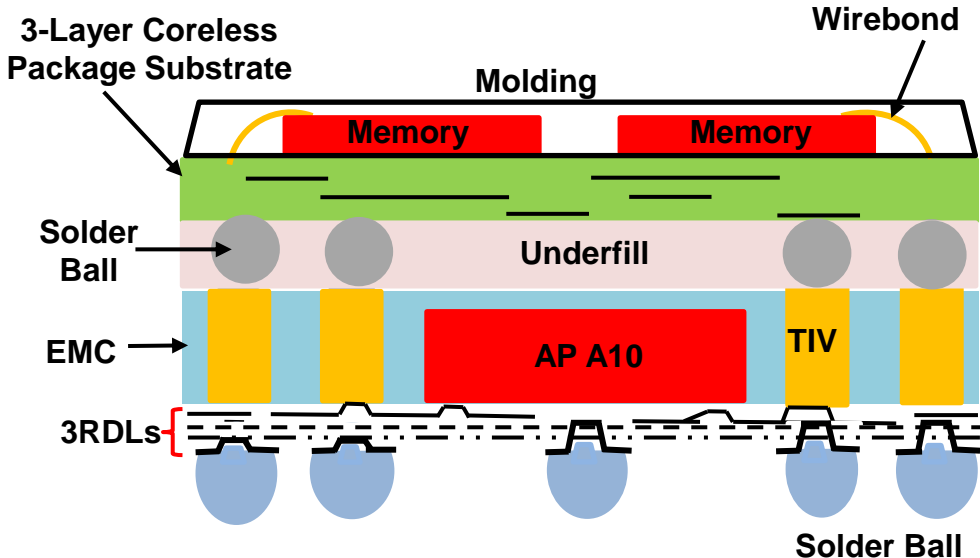
Contact Pad   ~1300 solder balls at 0.4mm pitch

Shipped in 2016

Mobile DRAM   SYSTEMPlus CONSULTING

3L Coreless substrate

Underfill   386 balls at 0.3mm pitch   Solder Ball

DAF

AP A10   EMC   TIV (Through InFO Via)

RDLs   Solder Ball

Underfill

~1300 solder balls at 0.4mm pitch

PCB

47
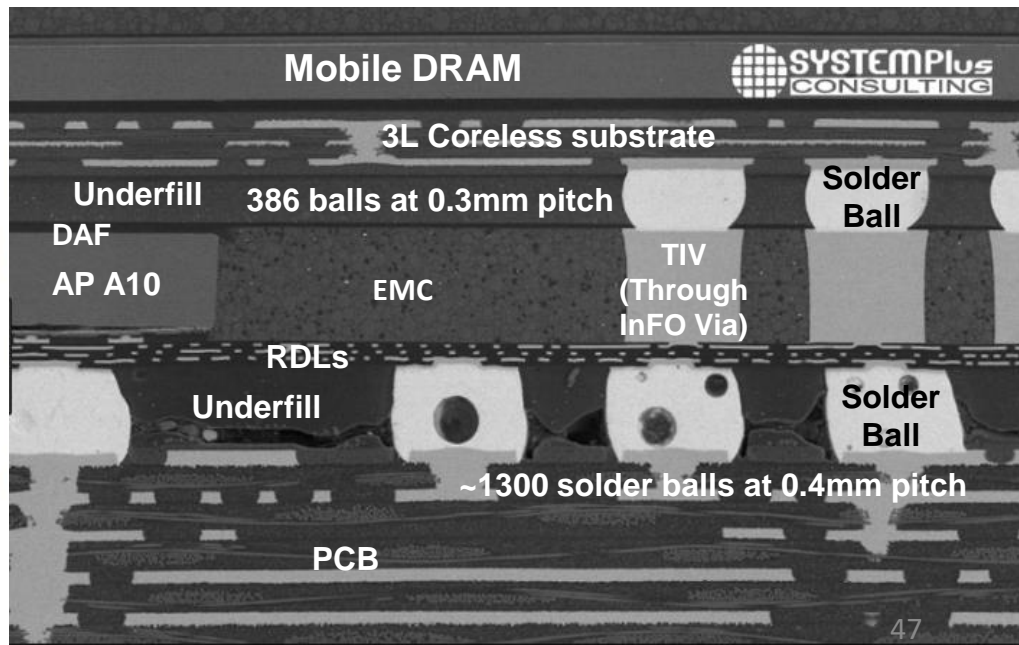
3D (PoP with Fan-Out) Packaging (Apple/TSMC)

AP SoC

9.9mm x 8.4mm

PoP

A12

13.4mm x 14.4mm

3-Layer Coreless Package Substrate

Over Mold

Wirebond

Memory   Memory

Solder Ball

Underfill

EMC

A12 AP

TIV

RDLs

Solder bumped flip chip IPD

Solder Ball

3-Layer Coreless Package Substrate

Memories cross-stacked with wirebonds

EMC

EMC

PCB

A12 AP

Solder balls at 0.35mm-pitch

RDLs

Solder bumped flip chip IPD

A12 AP (150µm)

RDLs

Solder balls
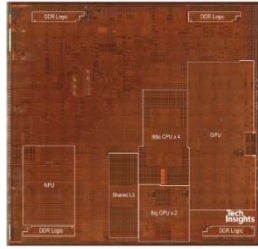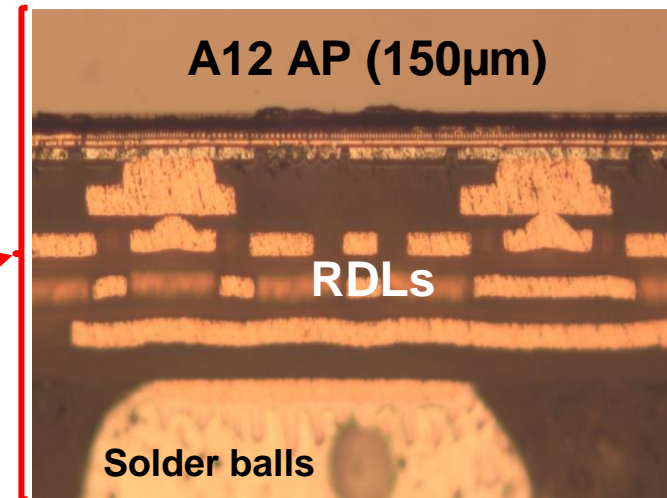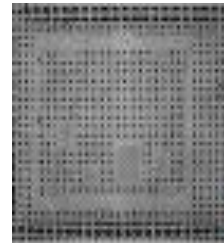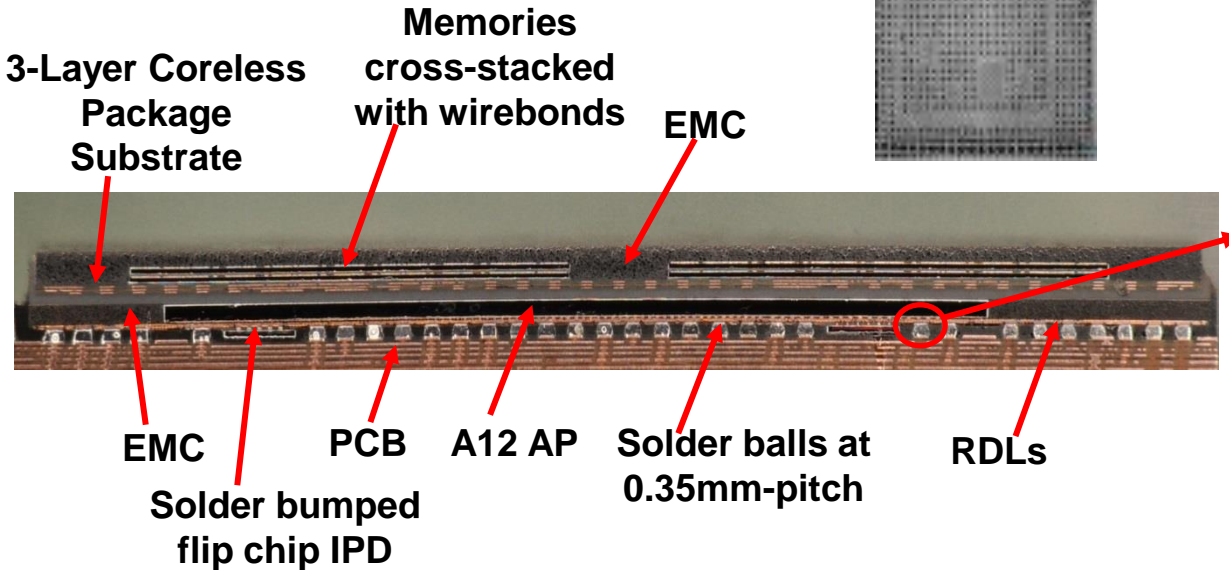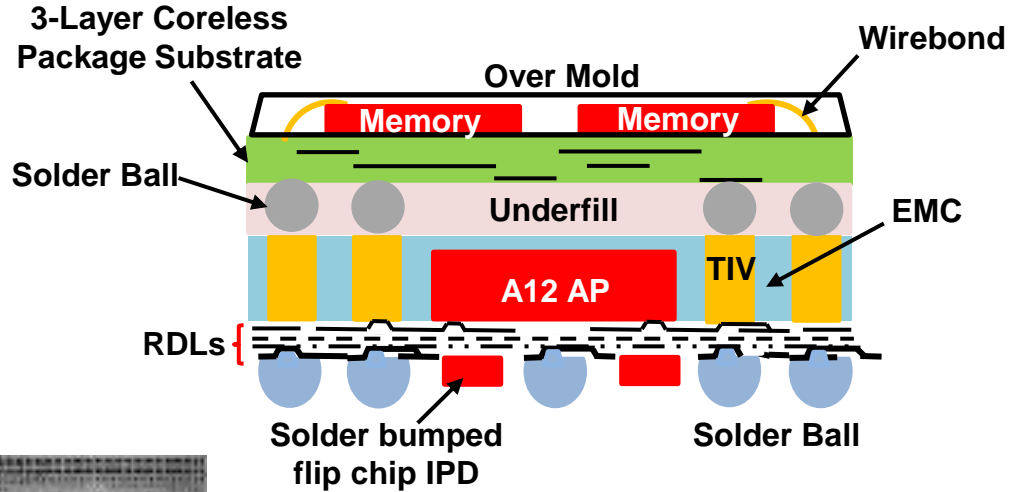
3D (PoP with Fan-Out) IC Packaging (Samsung)

8mm x 9.5mm x 1mm

Memory ePoP
2DRAM, 2NAND, 1Controller

3L Package substrate (90μm)

3L Organic Substrate

ABF

Underfill   Solder Ball   ABF

AP   PMIC   4RDLs

Solder Ball

PCB

Package substrate   Underfill   ABF   Memory ePoP   RDL   Solder Ball

3L Organic Substrate   AP (5mmx3mm)   Solder Ball   RDL   PMIC   ABF
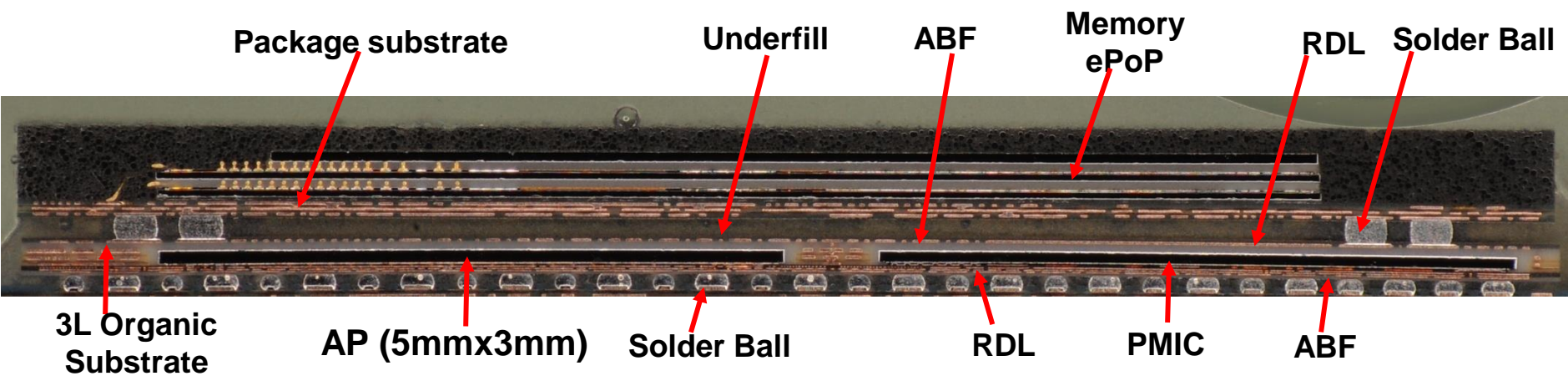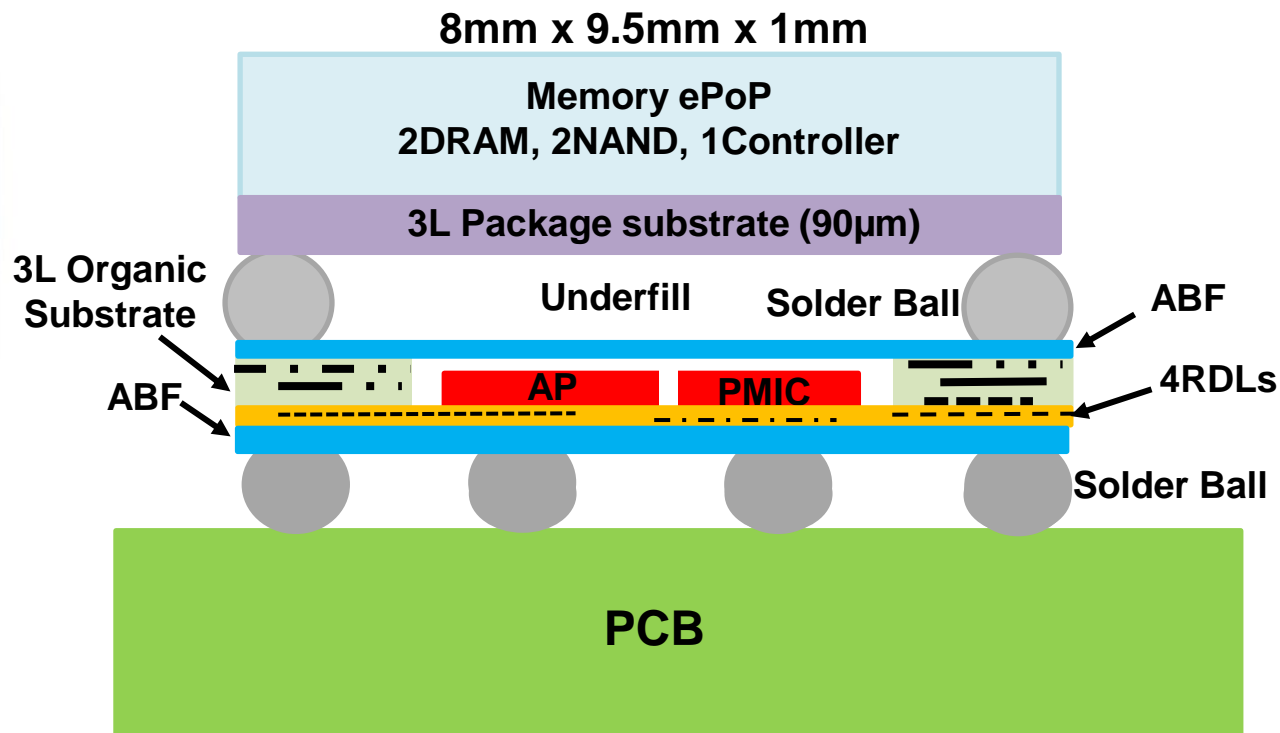
3D IC Integration (with TSVs)

3D IC Integration

Underfill

DRAM4

DRAM3

DRAM2

DRAM1

μbump

TSV

Logic Base Chip

(a)

Memory

μbump

TSV

CPU/
Logic

Package Substrate

(b)

Bumpless

Chip

Chip

TSV

(c)
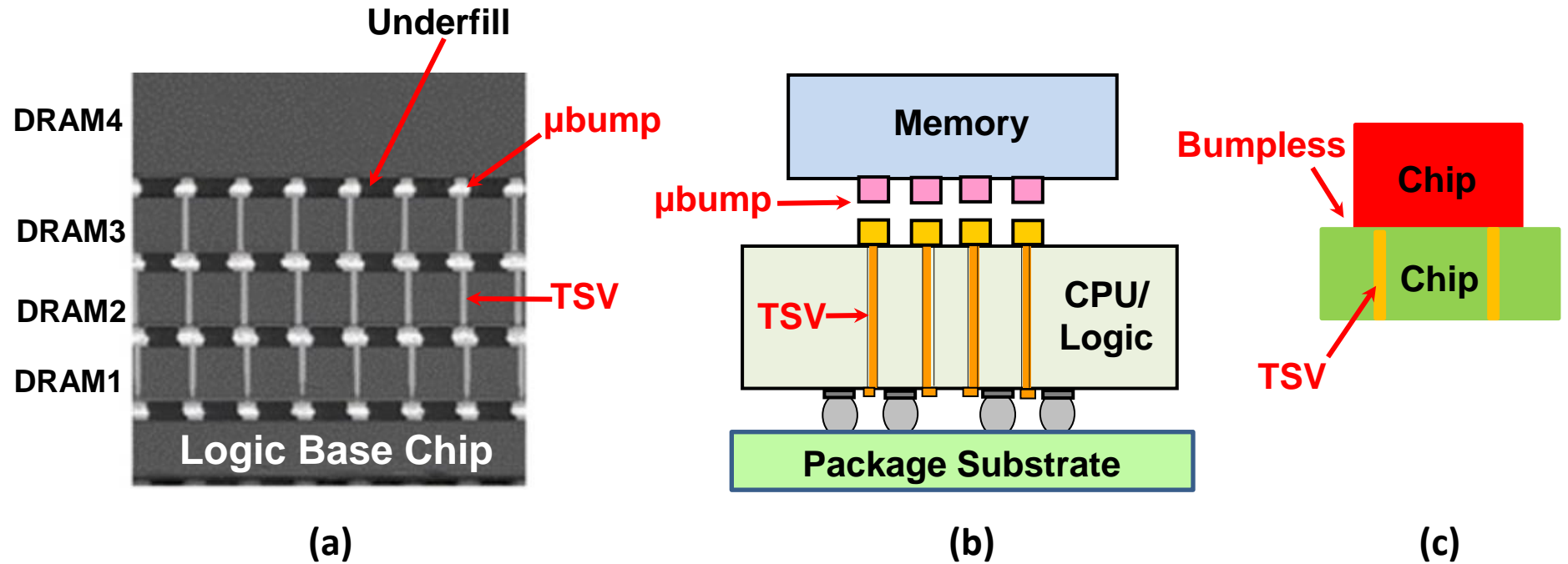
3D IC Integration with Active Interposer (High Bandwidth Memory)

DRAM4

DRAM3

DRAM2

DRAM1

Logic Base Chip

HBM (high bandwidth memory)

TSV

µSolder Joint

DRAM8

DRAM7

DRAM6

DRAM5

DRAM4

DRAM3

DRAM2

DRAM1

Logic Base Chip

HBM2

HBM2E (HBM2 Evolutionary)

DRAM

TSV

µbump (Cu + solder)

NCF (Underfill)
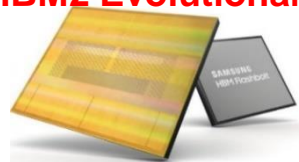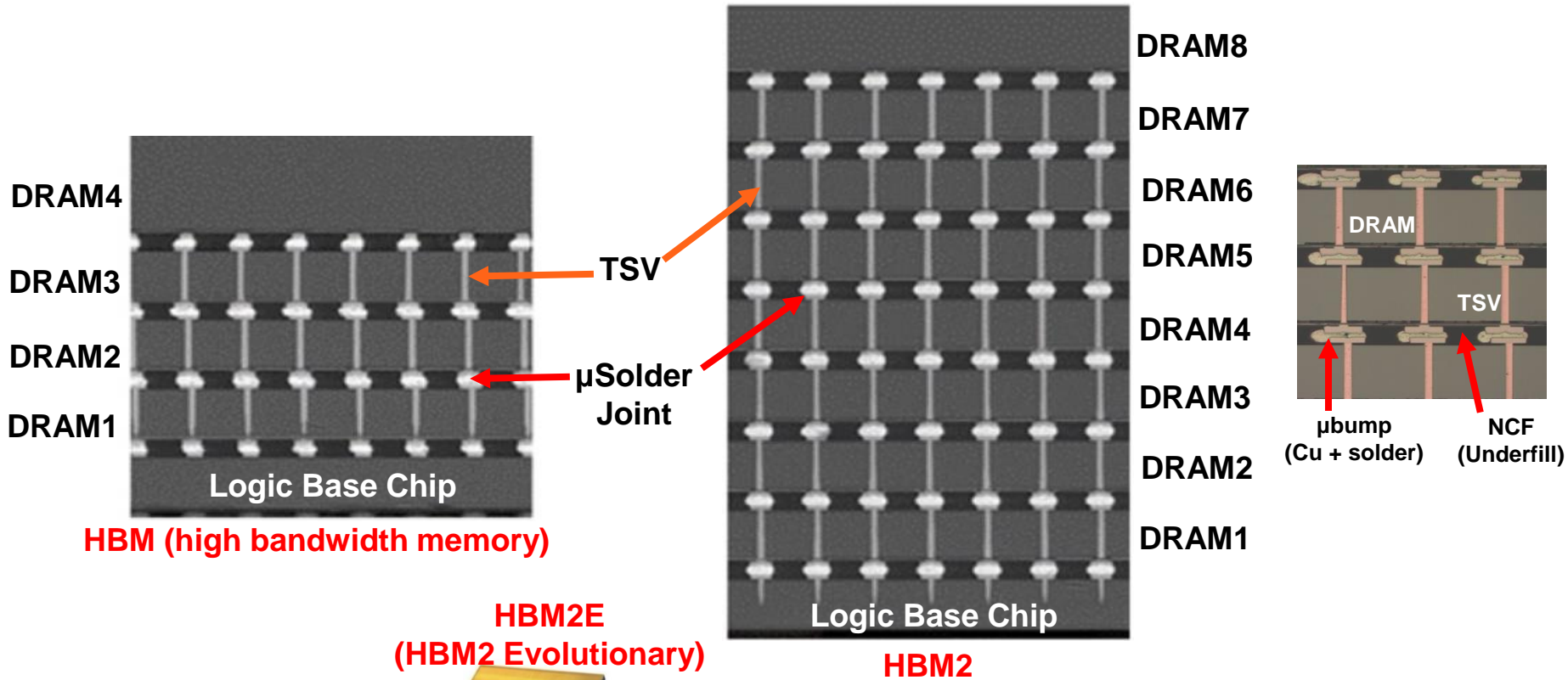
	HBM	HBM2 (Original)	HBM2/HBM2E (Current)	HBM3 (Upcoming)
Max Pin Transfer Rate	1Gbps	2Gbps	2.4Gbps	?
Max Capacity	4GB	8GB	24GB	64GB
Max Bandwidth	128GBps	256GBps	307GBps	512GBps

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Intel 3D IC Integration – FOVEROS Technology

Lakefield

10mm

10mm

Memory LP-DD4 4x16 Big CPU

Small CPU | Small CPU | Small CPU | Small CPU

1.5M L2 | 0.5M MLC

Uncore / CCF / 4M LLC / IDP / IOP

Graphics Gen 11-LP 64EU | Display Gen 11.5 | Imaging IPU5.5

P-Unit | SVID | JTAG

Clock | Fuse / DRNG | Debug

MIPI DSI DPHY1.2 | DP 1.4 | MIPI CSI2 DPHY1.2

FOVEROS TECHNOLOGY

3D face-face chip stacking for heterogeneous integration

Compute Chip | Memory, Modem, …

FTF Micro-Bumps

Thru-Silicon

Solder Bumps

Vias

Active Interposer

Package Substrate

intel

3D IC Integration

Chip-to-Active TSV-Interposer (Samsung X-Cube)

3D IC Integration

3D Heterogeneous Integration of EIC and PIC Devices

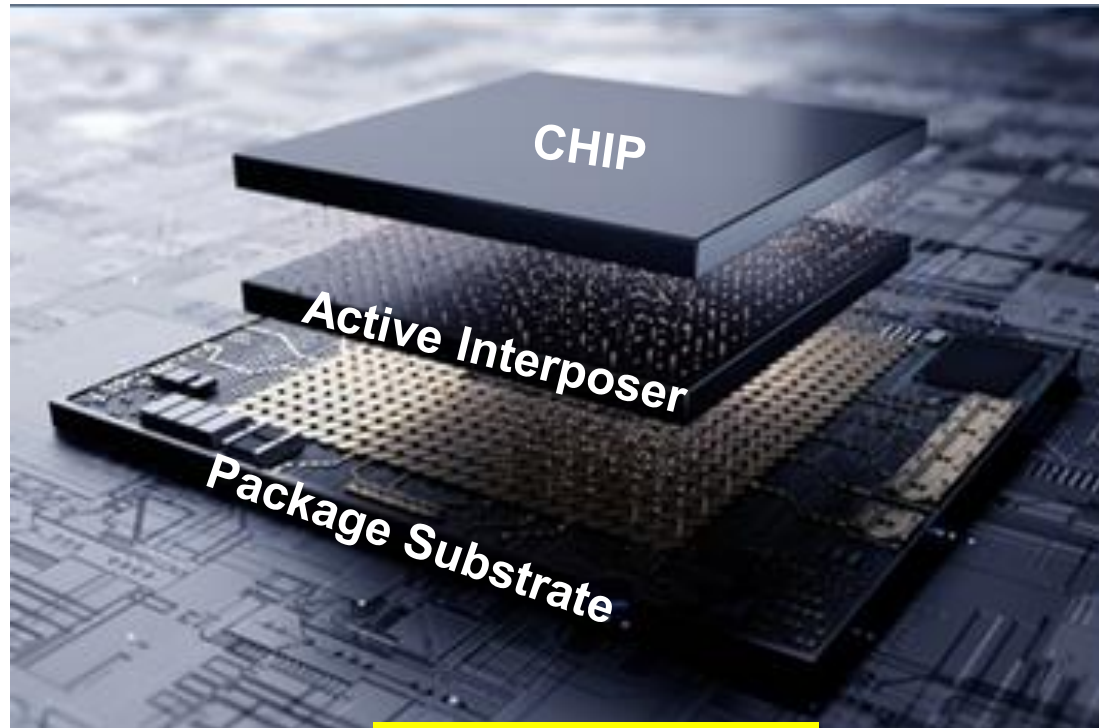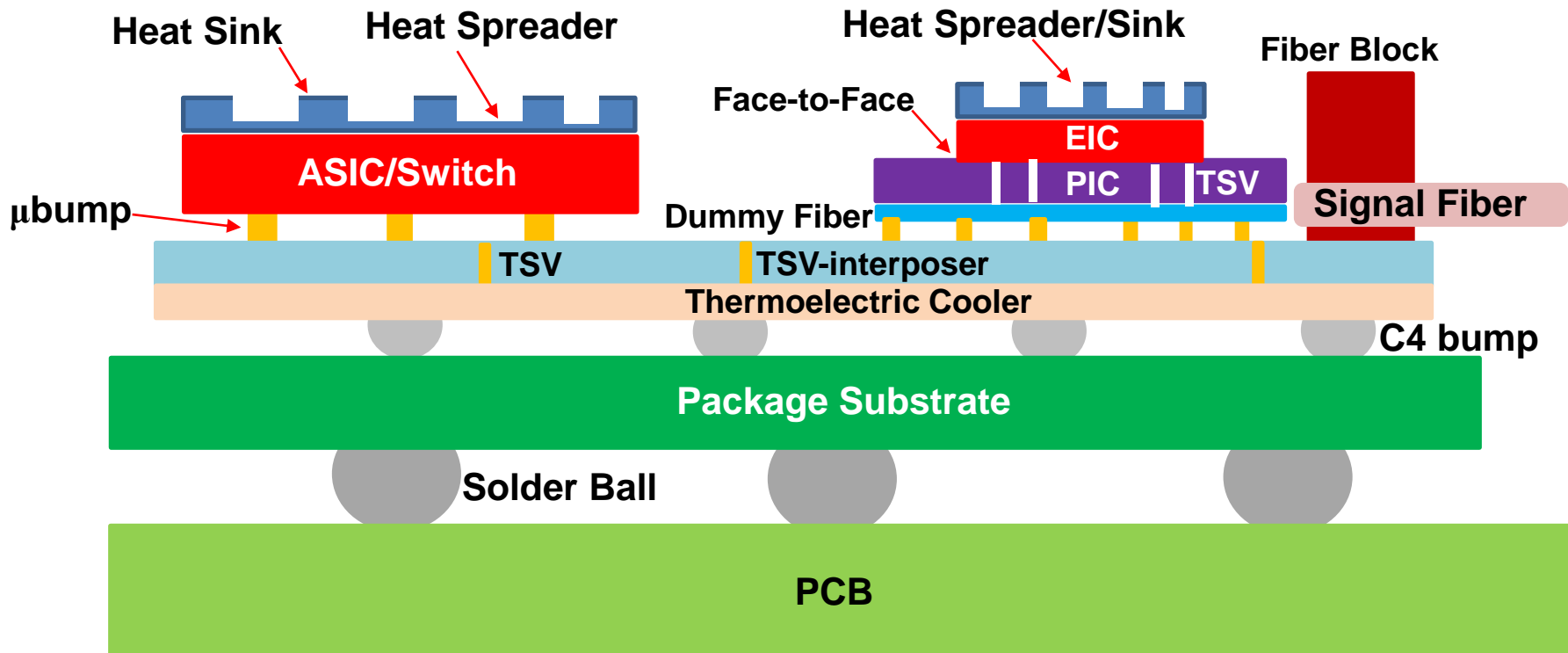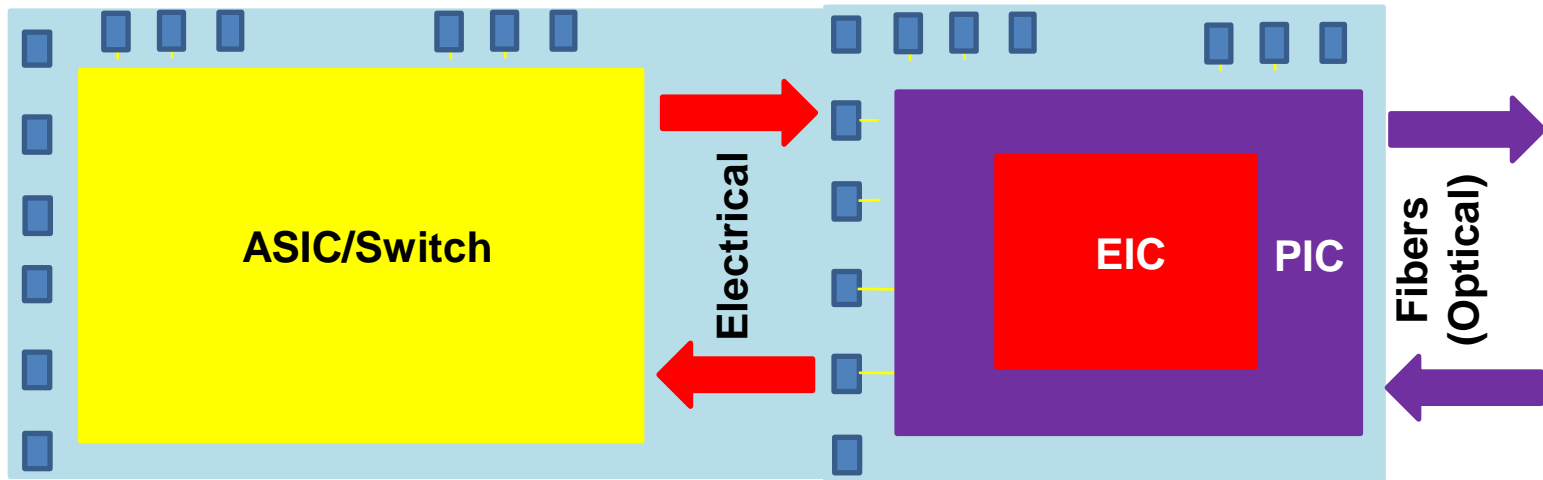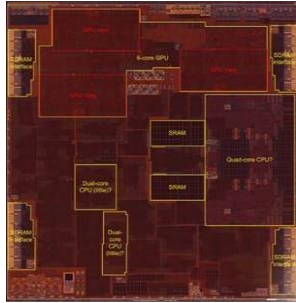# System-on-Chip (SoC)

Moore's Law - Apple's Application Processors (AP): SoC (System-on-Chip) - A10, A11, A12, A13, A14, and A15
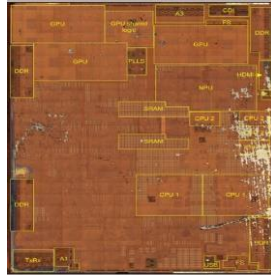
A10

A10 consists of:
- 6-core GPU (graphics processor unit)
- 2 dual-core CPU (central processing unit)
- 2 blocks of SRAMs (static random access memory), etc.
- **16nm process technology**
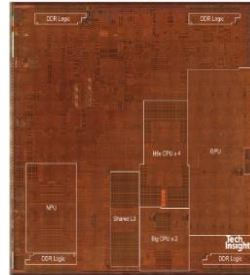- Transistors = 3 billion
- Chip area = 125mm²

A11

A11 consists of:
- More functions, e.g., 2-core Neural Engine for Face ID
- Apple designed tri-core GPU
- **10nm process technology**
- Transistors = 4.3 billion
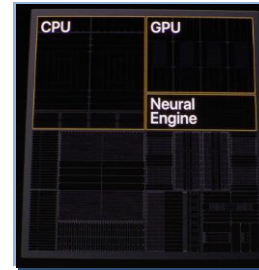- Chip area = 89mm²

A12

A12 consists of:
- Eight-core Neural Engine with AI capabilities
- Four-core GPU (faster)
- Six-core CPU (better performance)
- **7nm process technology**
- Transistors = 6.9 billion
- Chip area = 83mm²

A13

A13 consists of:
- Eight-core Neural Engine with Machine Learning
- Four-core GPU (20% faster > A12)
- Six-core CPU (20% faster and 35% save energy > A12)
- **7nm process technology with EUV**
- Transistors = 8.5 billion
- Chip area = 98.5mm²

A14
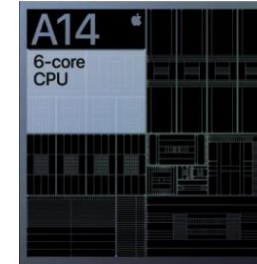
A14 consists of:
- 16-core Neural Engine with Machine Learning (11 trillion/s, 10 times faster > A13)
- Four-core GPU (30% faster > A13)
- Six-core CPU (40% faster > A13)
- **5nm process technology with EUV**
- Transistors = 11.8 billion
- Chip area = 88mm²

A15
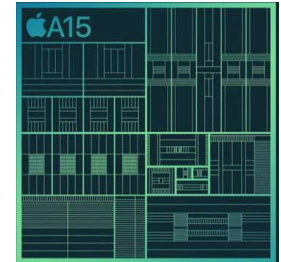
A15 consists of:
- 16-core Neural Engine to speed up AI tasks with Machine Learning (15.8 trillion/s)
- Four-core GPU, but 5-core for iPhone Pro and 13Pro Max
- Six-core CPU (faster > A14)
- **5nm process technology with EUV**
- Transistors = 15 billion
- Image signal processor

Apple Application Processors vs. Transistors vs. Process Technologies (The Power of Moore's Law)
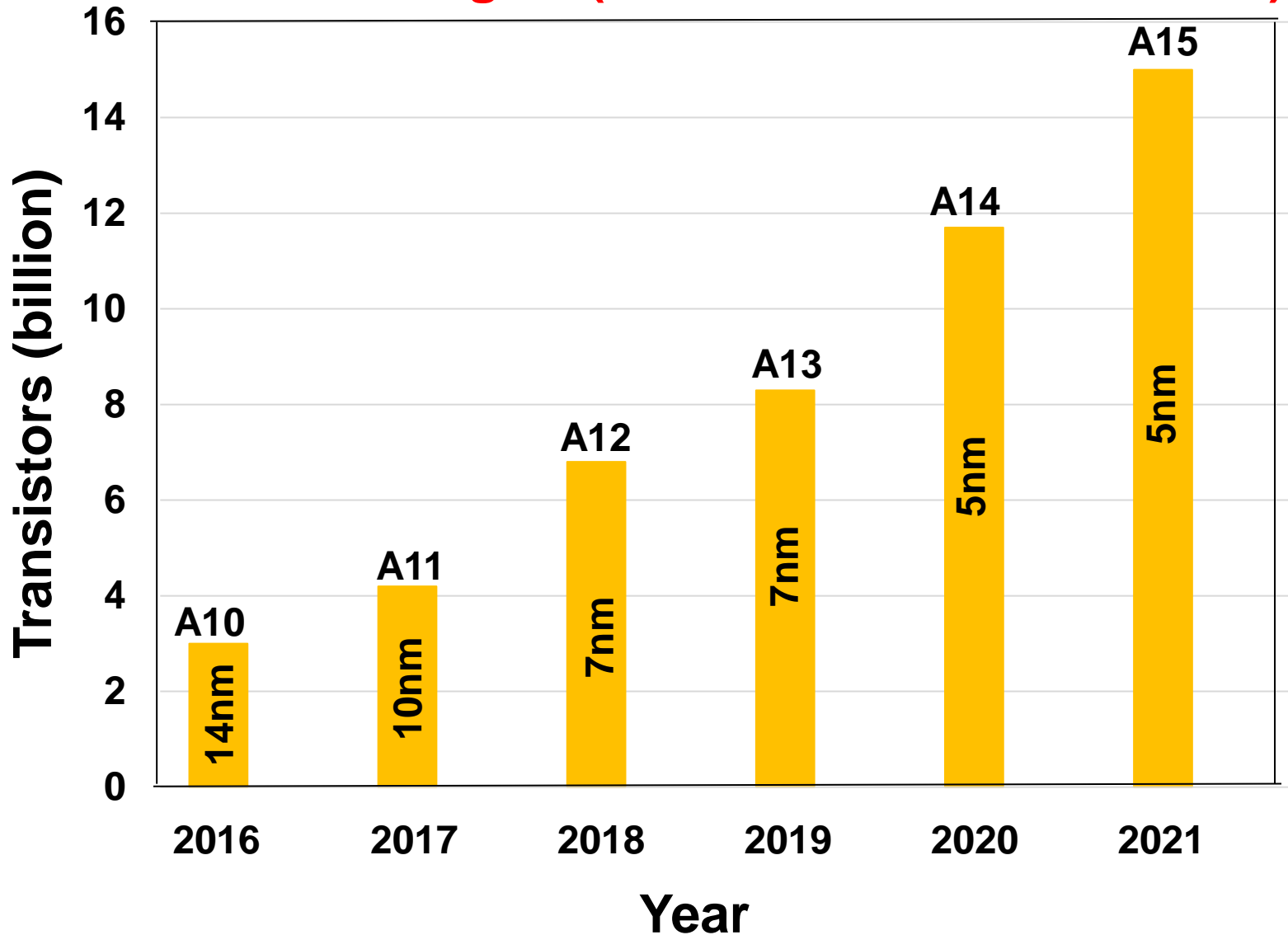
It is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC.

Design Cost for Advanced Nodes in Semiconductors
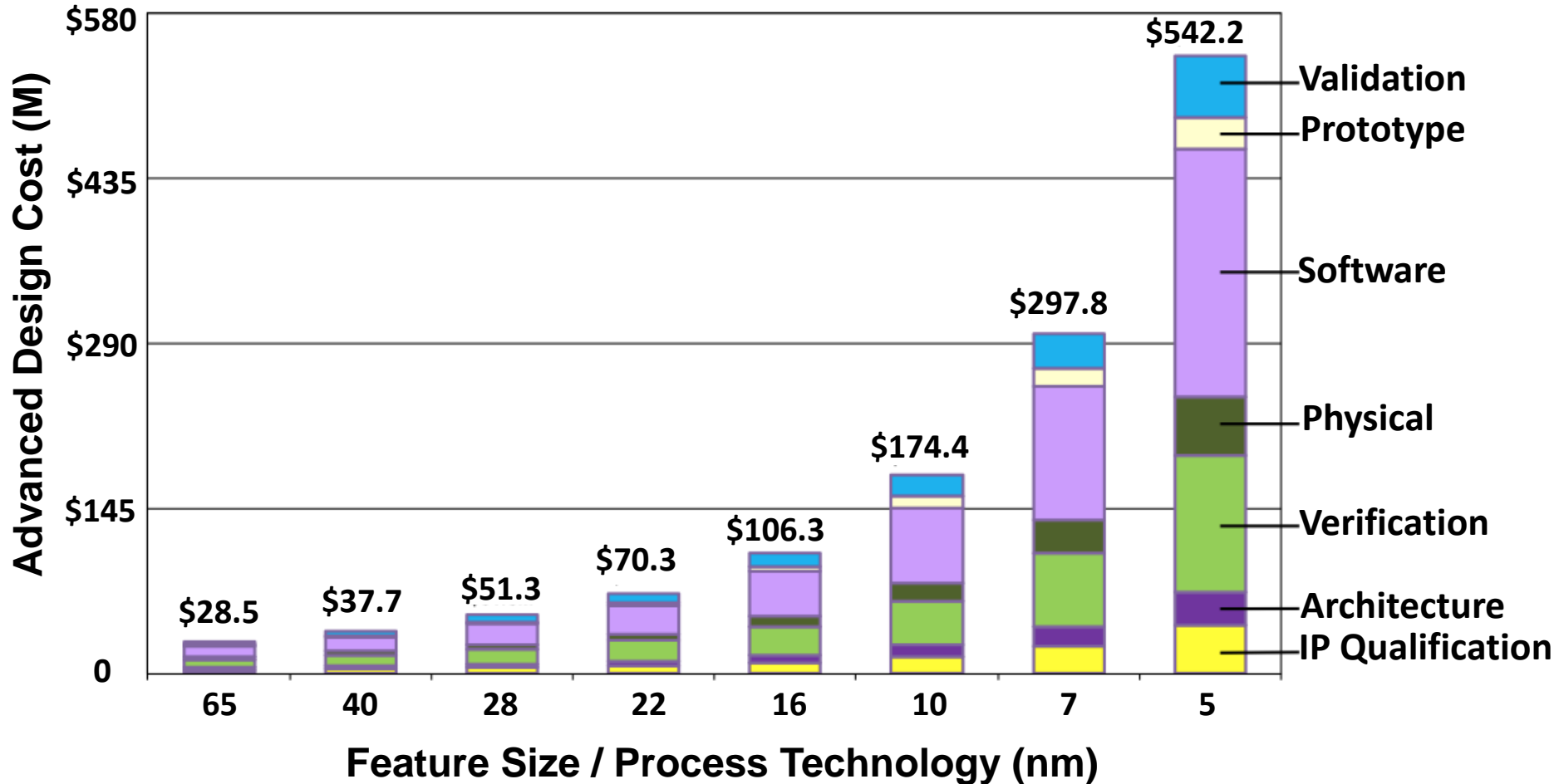
It will take another $1 billion for 5nm process development.

Yield (Cost) per Wafer vs. Chip Size for SoC and Chiplets
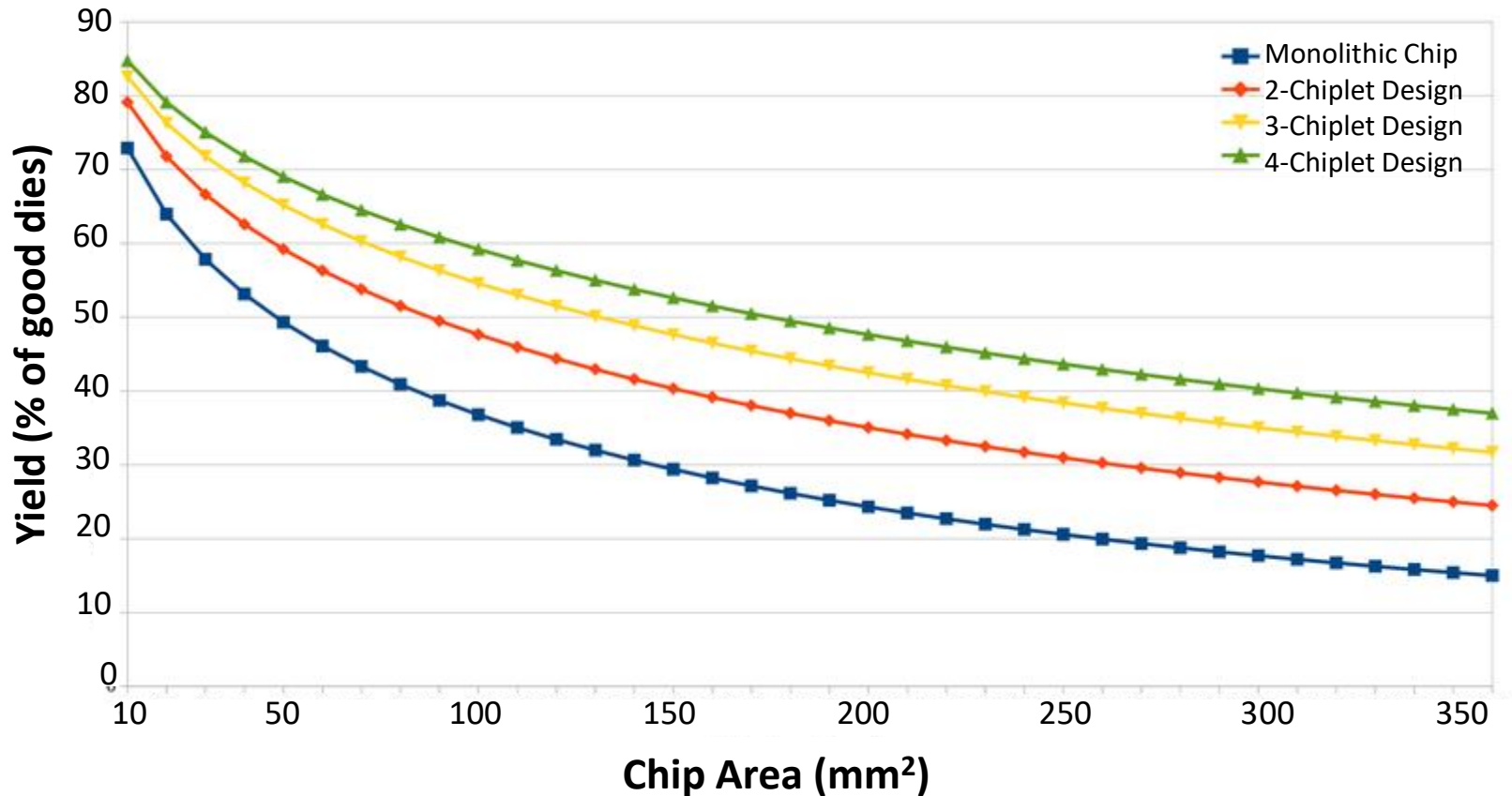
Chiplet Design and Heterogeneous Integration Packaging

➢ **Chip partition and integration**

➢ **Chip split and integration**

➢ **Multiple System and Integration**

Chiplet Design and Heterogeneous Integration Packaging

Chip partition and integration (Driven by cost and technology optimization)

I/O	I/O
Logic	
I/O	I/O

SoC

Partition →

I/O
Logic

Chiplet Designs

→

µBump, Bumpless, CoW, WoW

Frontend Chiplets Integration (Optional), e.g., SoIC

→

Heterogeneous Integration Packaging

Backend Chiplets Packaging Integration on the same substrate
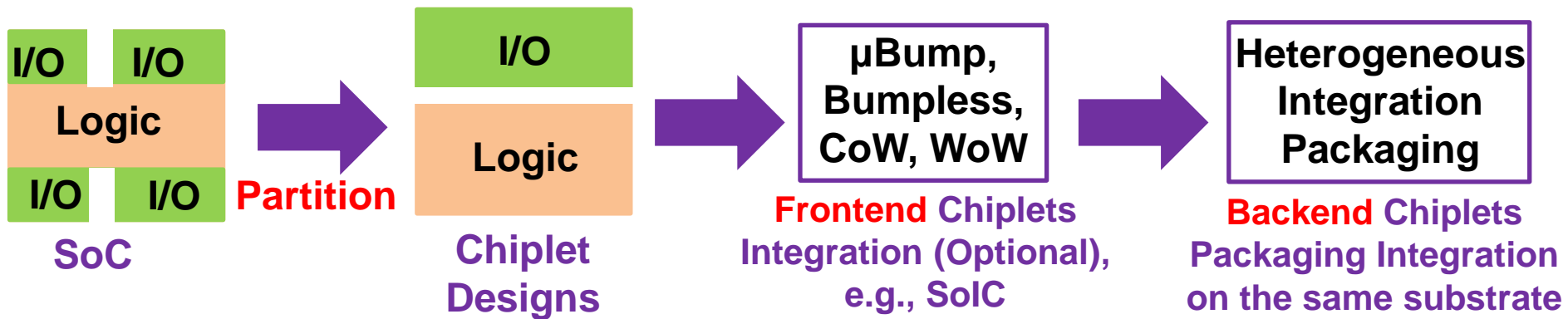
Chiplet Design and Heterogeneous Integration Packaging

Chip split and integration (Driven by cost and yield)

Logic	→	Logic1 Logic2 Logic3	→	µBump, Bumpless, CoW, WoW	→	Heterogeneous Integration Packaging
SoC	**Split**	**Chiplet Designs**		**Frontend Chiplets Integration (Optional), e.g., SoIC**		**Backend Chiplets Packaging Integration on the same substrate**
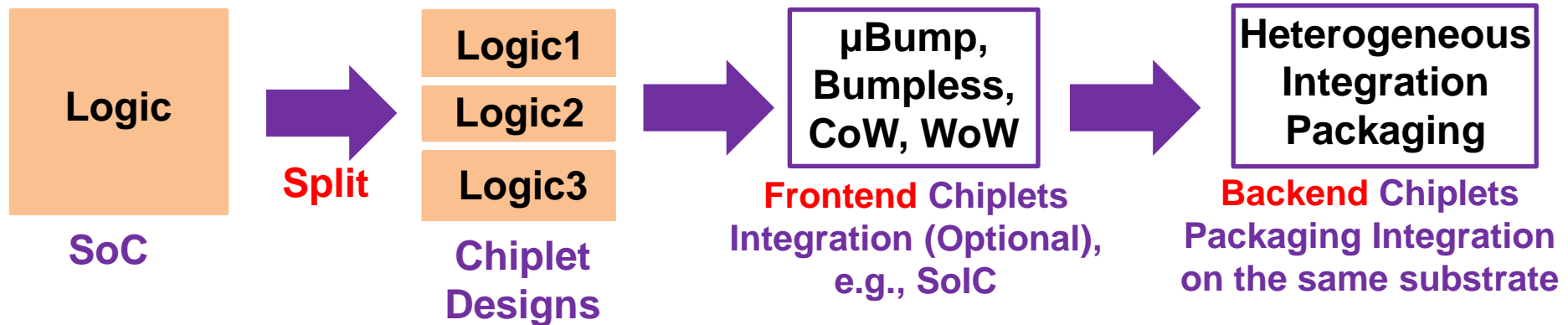
Chiplet Design and Heterogeneous Integration Packaging

Chiplet Design and Heterogeneous Integration Packaging with TSV-Interposer

Multiple System and Integration (1)

2.5D IC Integration

SoC CPU/GPU/FPGA/ASIC

HBM

DRAM

Logic

RDL

TSV

Cu

TSV-interposer

Microbump

Cu-C4 bump

Build-up Package Substrate

PCB

DRAM/HBM

Substrate

SoC Substrate

PCB
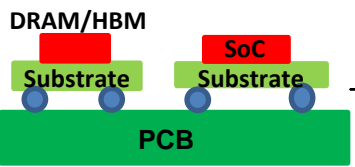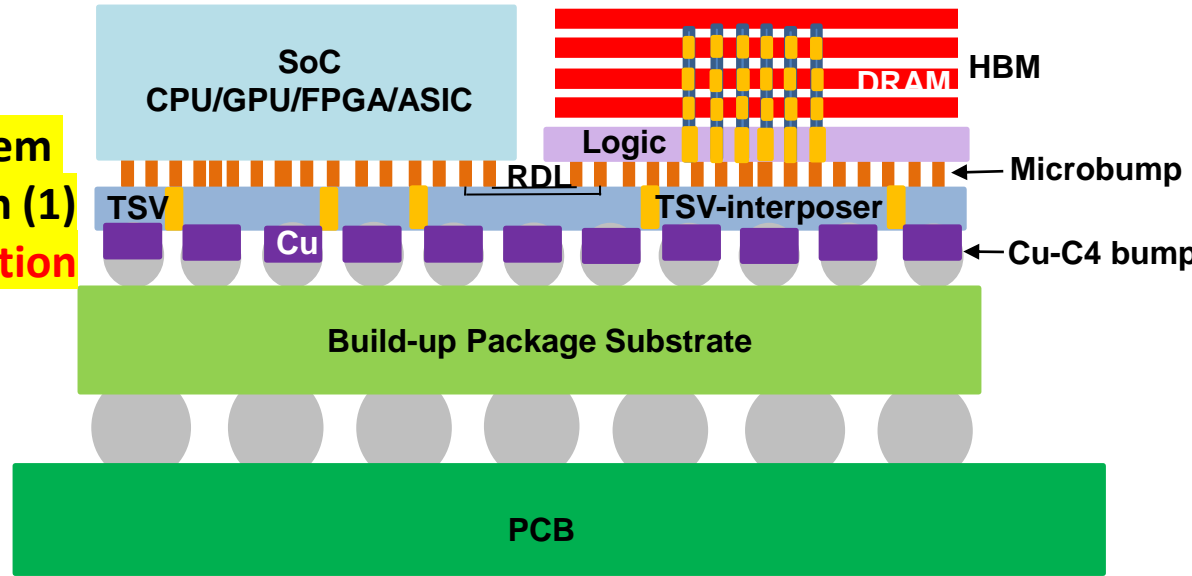
Chiplet Design and Heterogeneous Integration Packaging with Fan-Out RDL-Substrate

Multiple System and Integration (2)

2.3D IC integration

SoC CPU/GPU/FPGA/ASIC

HBM

DRAM

Logic

Microbump

Cu

Fan-out RDL-interposer

Cu-C4 bump

Build-up Package Substrate

PCB

64

Chiplet Design and Heterogeneous Integration Packaging

- **Chip (CPU)**
- **FAB-1**
- **5nm**
- **12"-wafer**

- **Chip (I/O)**
- **FAB-2**
- **90nm**
- **8"-wafer**

- **Chip (GPU)**
- **FAB-3**
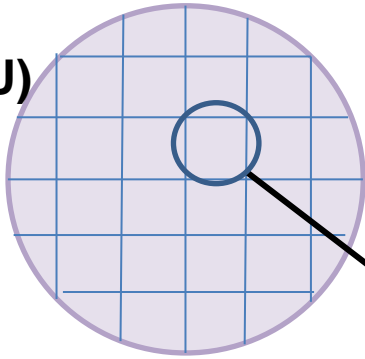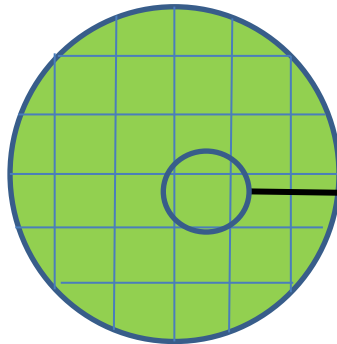- **7nm**
- **12"-wafer**

Chip (CPU)

Chip (I/O)

Chip (GPU)

Heterogeneous integration or SiP

Packaged memory stack

| CPU 1 |
| CPU 2 |

PBGA Memory Stack

I/O

GPU 1

GPU 2

- **Time-to-market**
- **Less IP issues**
- **Flexibility**
- **Low cost alternative than SoC**
- **Optimized signal integrity and power**
- **Better thermal performance**

Heterogeneous integration uses packaging technology to integrate dissimilar chiplets, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.

Heterogeneous Integration, Springer, 2019

Chiplet Design and Heterogeneous Integration Packaging Comparing with SoC: Advantages and Disadvantages

➤ **The key advantages of chiplets heterogeneous integration are:**
  ➤ **(1) yield improvement (lower cost) during manufacturing;**
  ➤ **(2) faster time-to-market;**
  ➤ **(3) cost reduction during design;**
  ➤ **(4) better thermal performance;**
  ➤ **(5) reusable of IP;**
  ➤ **(6) modularization.**

➤ **The key disadvantages are:**
  ➤ **(1) additional area for interfaces;**
  ➤ **(2) higher packaging costs;**
  ➤ **(3) more complexity and design effort;**
  ➤ **(4) past methodologies are less suitable for chiplets.**

Examples on Chiplet Design and Heterogeneous Integration Packaging

➢ **Xilinx**

➢ **AMD**

➢ **Intel**

➢ **TSMC**

➢ **Nvidia**

➢ **Samsung**

Xilinx's Chiplet Design and Heterogeneous Integration Packaging
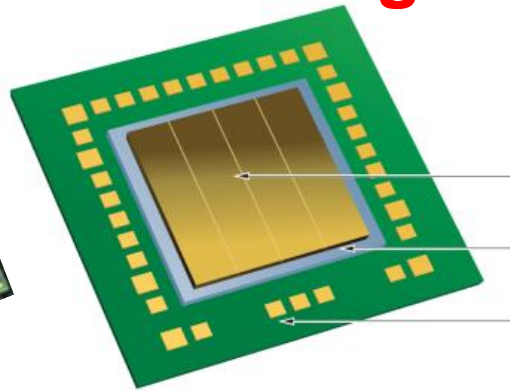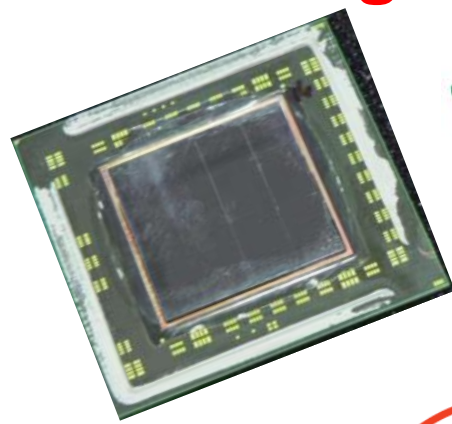
For better manufacturing yield (to save cost), a very large SoC has been split into 4 smaller chips.

High-Bandwidth, Low-Latency Connections (10,000+)

Microbumps

Through Silicon Vias (TSV)

C4 Bumps
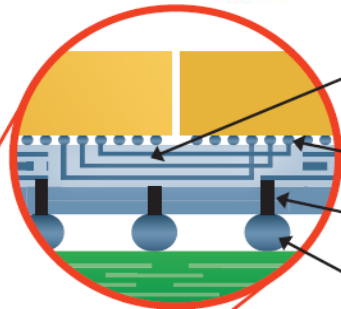
The key function of the RDLs on the interposer is to perform lateral communications between the chips.

| Slice 1 | Slice 2 | Slice 3 | Slice 4 |

28 nm FPGA Die Slices

Silicon Interposer With 4 RDLs

Package Substrate

BGA Solder Balls
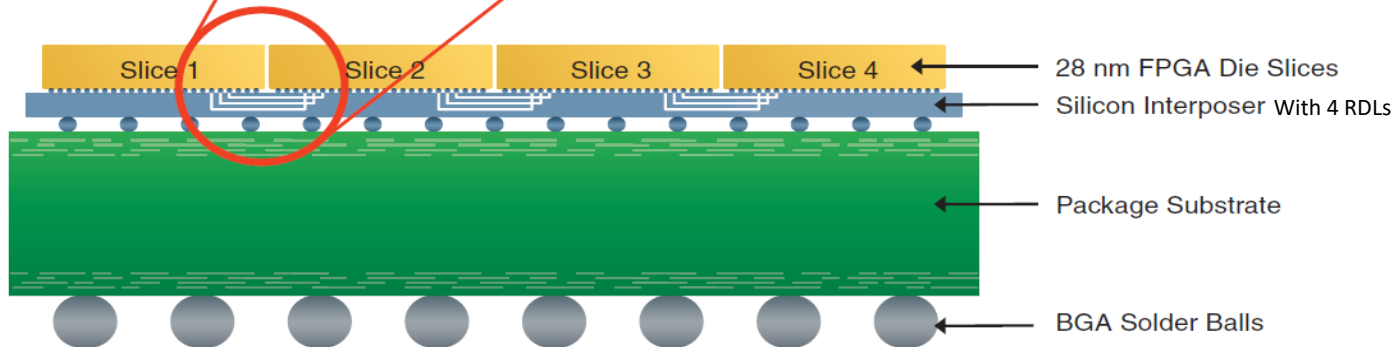
Shipped in 2013

AMD's Chiplet Design and Heterogeneous Integration Packaging

Extreme-performance yield computing (EPYC)

2D IC Integration

9-2-9 package substrate

> ➢ **The I/O and CCD (core complex die or CPU compute die) are partitioned**
> ➢ **The CCD is split into two chiplets (7nm process technology)**
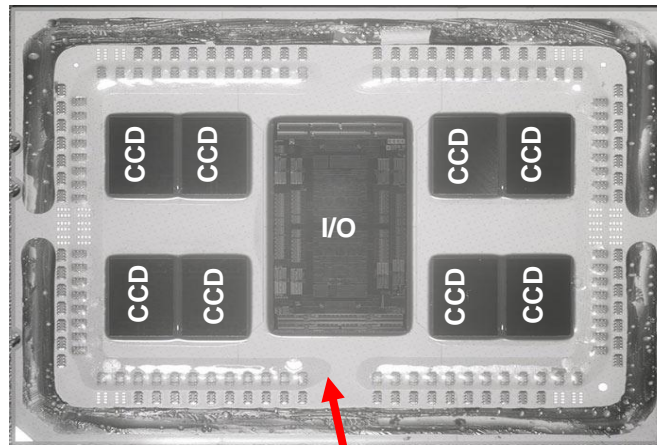> ➢ **The I/O chip is with 14nm process technology**

Shipped in 2019

AMD's Future Chiplet Design and Heterogeneous Integration Packaging

3D IC Integration

ENGINEERING THE 3D CHIPLET ARCHITECTURE

- Structural Silicon
- 64MB L3 Cache Die
- Direct Cu-Cu Bonding
- TSVs For Si-to-Si communication
- Up to 8-Core "Zen 3" CCD

ADVANCED PACKAGING

AMD
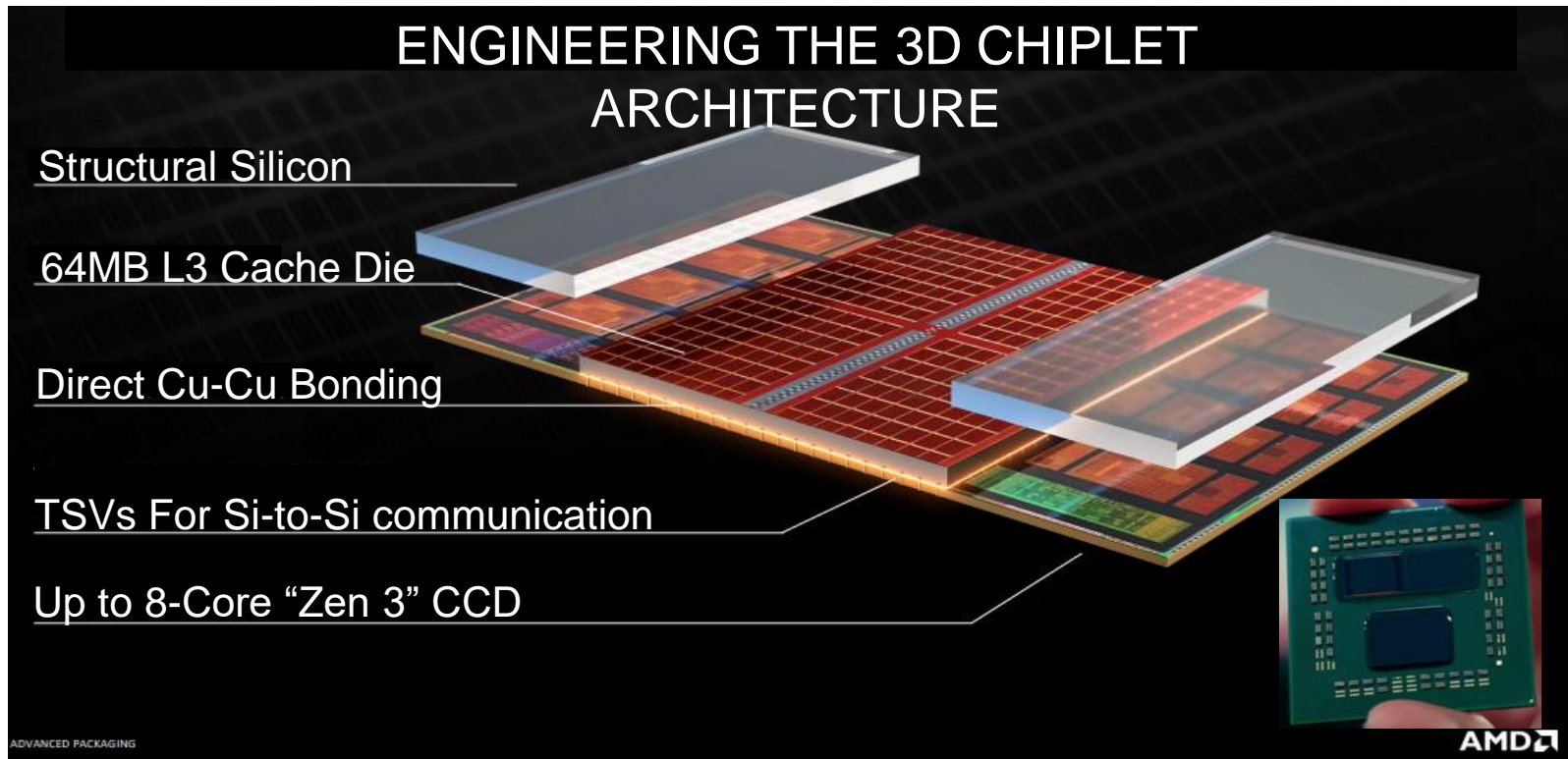
➢ **AMD's RYZEN 9 5900X Prototype chip for gaming**
➢ **Same 7nm process technology as RYZEN, but using 3D chiplet copper-to-copper bumpless hybrid bonding**

Intel's Chiplet Design and Heterogeneous Integration Packaging
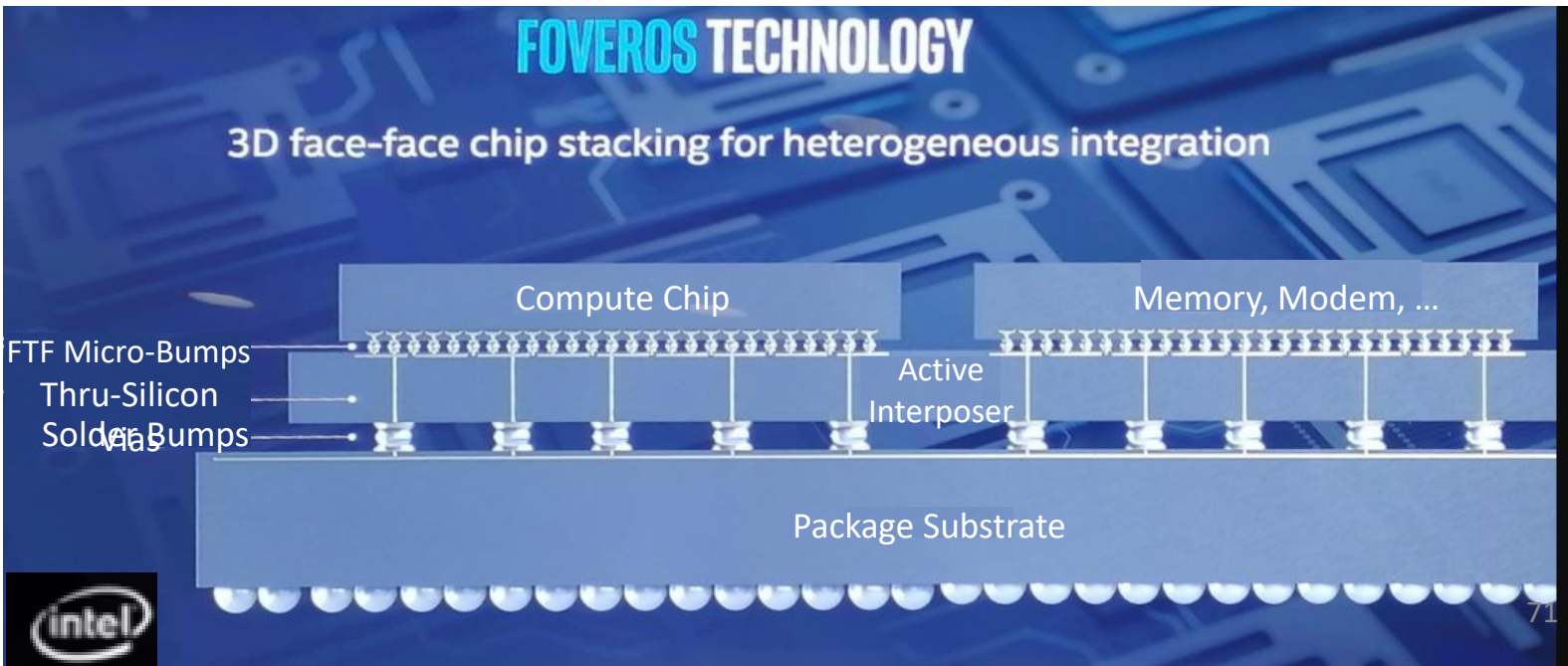
10mm

Lakefield

(a) 10mm

3D IC Integration

> ➤ **The memory and graphics are partitioned**
> ➤ **The large CPU is split into 5 smaller CPUs (10nm process technology)**
> ➤ **All the tiles (or chiplets) are attached on an active interposer**

(b)

FOVEROS TECHNOLOGY

3D face-face chip stacking for heterogeneous integration

Compute Chip   Memory, Modem, …

FTF Micro-Bumps
Thru-Silicon Vias
Solder Bumps

Active Interposer

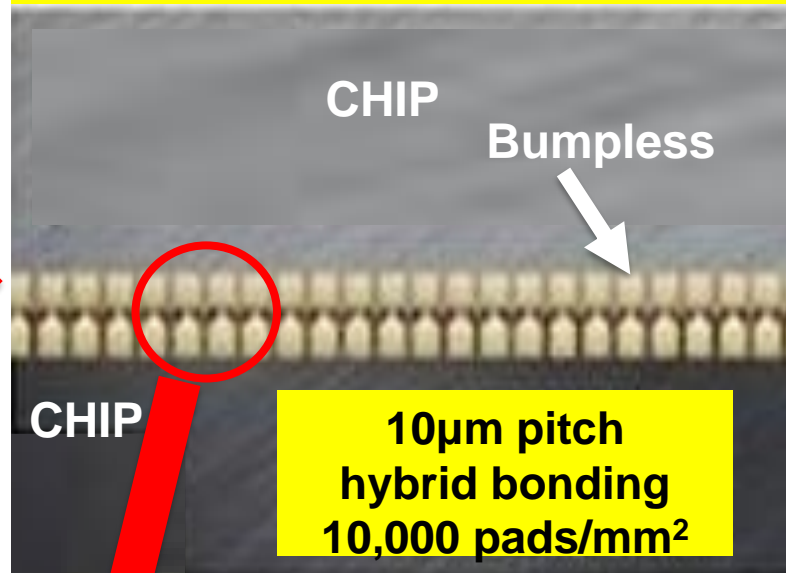Package Substrate

(intel)

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Shipped in 2020

Intel's Future Chiplet Design and Heterogeneous Integration Packaging:- FOVEROS Direct

FOVEROS (Micro Bumps)
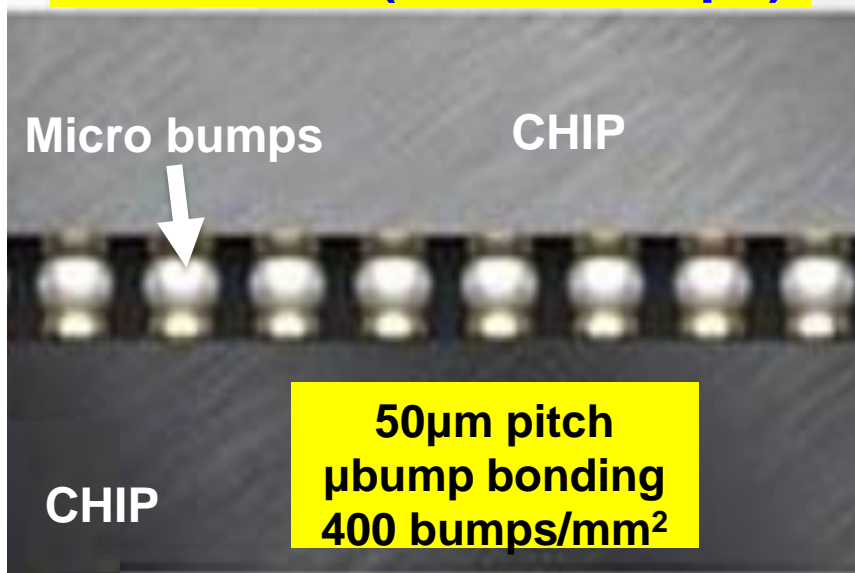
Micro bumps

CHIP

CHIP
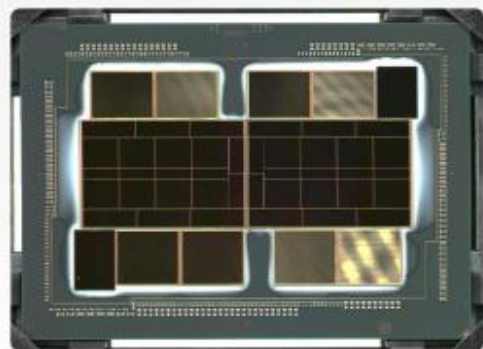
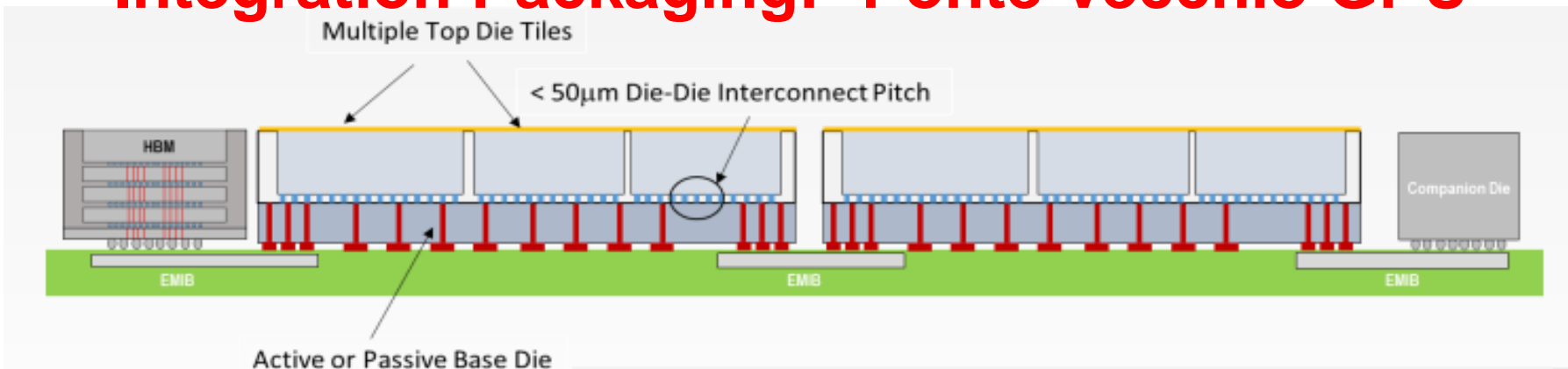**50μm pitch μbump bonding 400 bumps/mm²**

FOVEROS Direct

CHIP

Bumpless

CHIP

10μm pitch hybrid bonding 10,000 pads/mm²

Top Die

Bottom Die

FOVEROS Direct

Top Die

Cu

Cu-Cu Bonding

Bottom Die

Cu
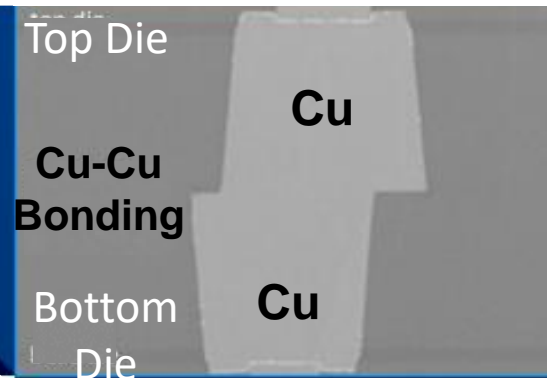
Intel's Future Chiplet Design and Heterogeneous Integration Packaging:- Ponte Vecchio GPU

Multiple Top Die Tiles

< 50µm Die-Die Interconnect Pitch

HBM

Companion Die

EMIB

EMIB

EMIB

Active or Passive Base Die

IHS

HBM

Top Die

Base Die

EMIB

Substrate

➤ **47 Chiplets (16 HPC)**
➤ **Max. size = 41mm²**

Compute Tile

Rambo Tile **(8)**

Foveros

Base Tile **(2)**

(650mm²)

HBM Tile **(8)**

Xᵉ Link Tile **(2)**

Multi Tile Package

EMIB Tile **(11)**

77.5mm x 62.5mm
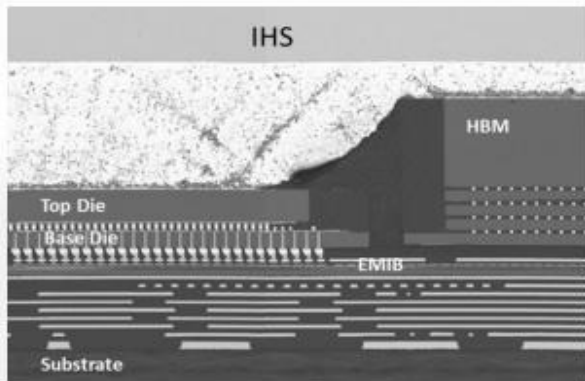
TSMC's Chiplets Bonding, Density, and Performance

(a)

(b)

(c)
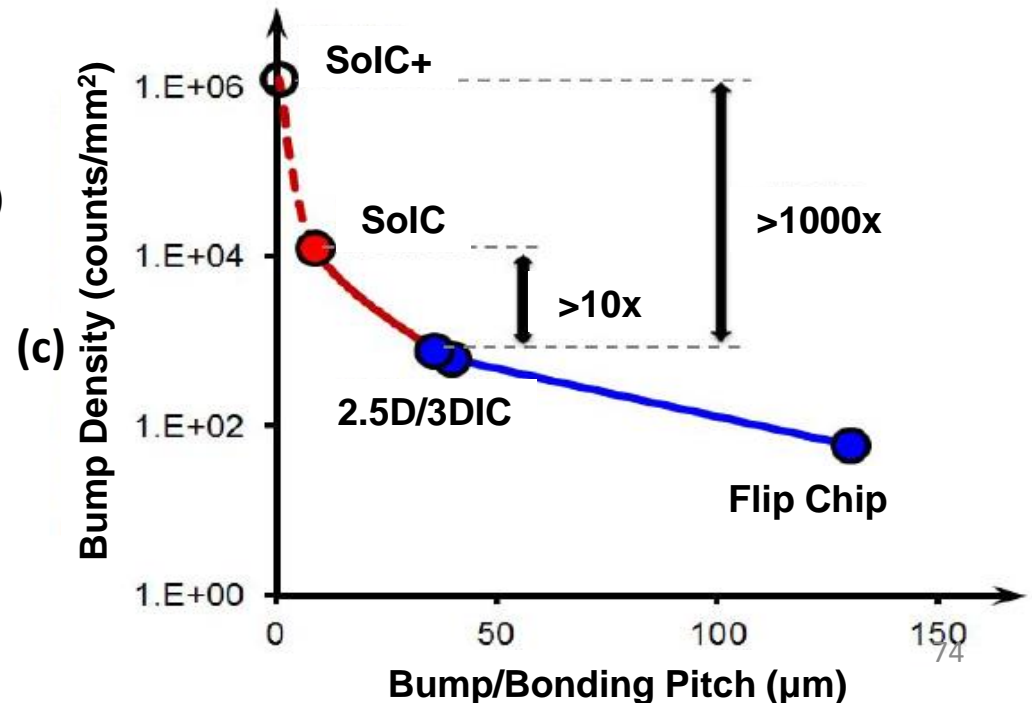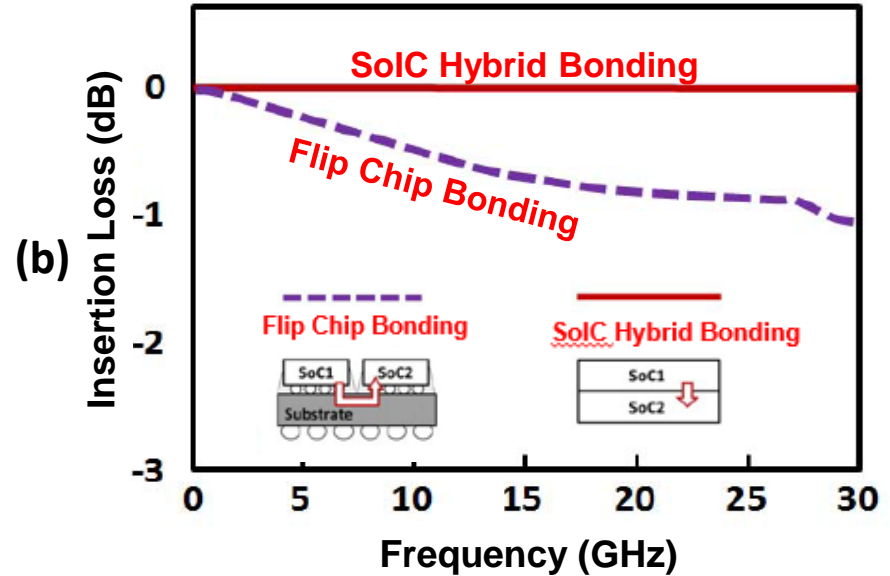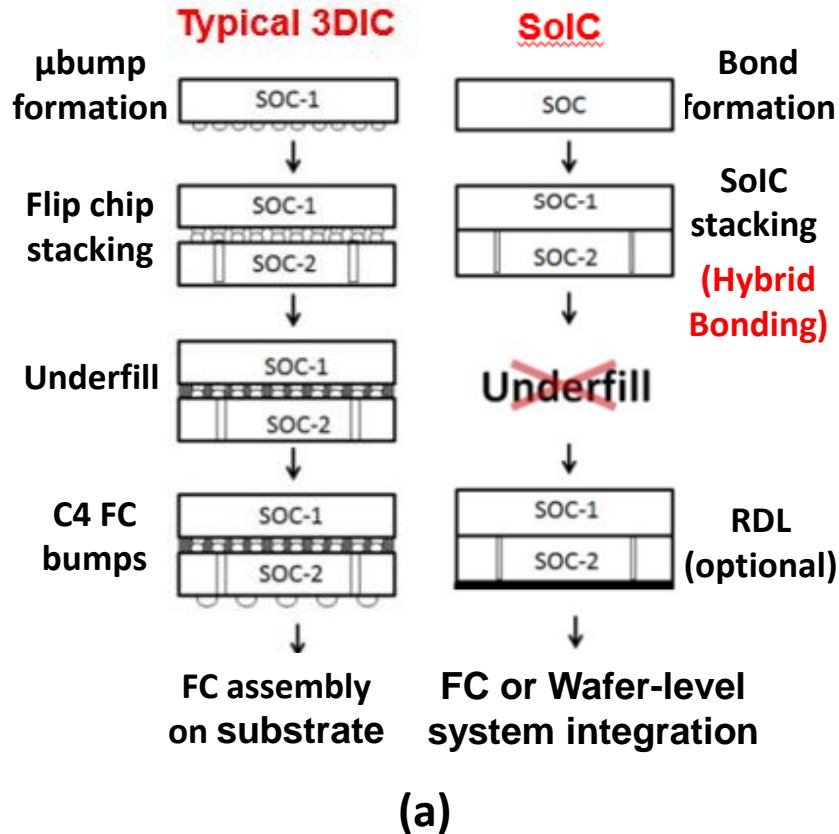
TSMC's Chiplet Design and Heterogeneous Integration Packaging
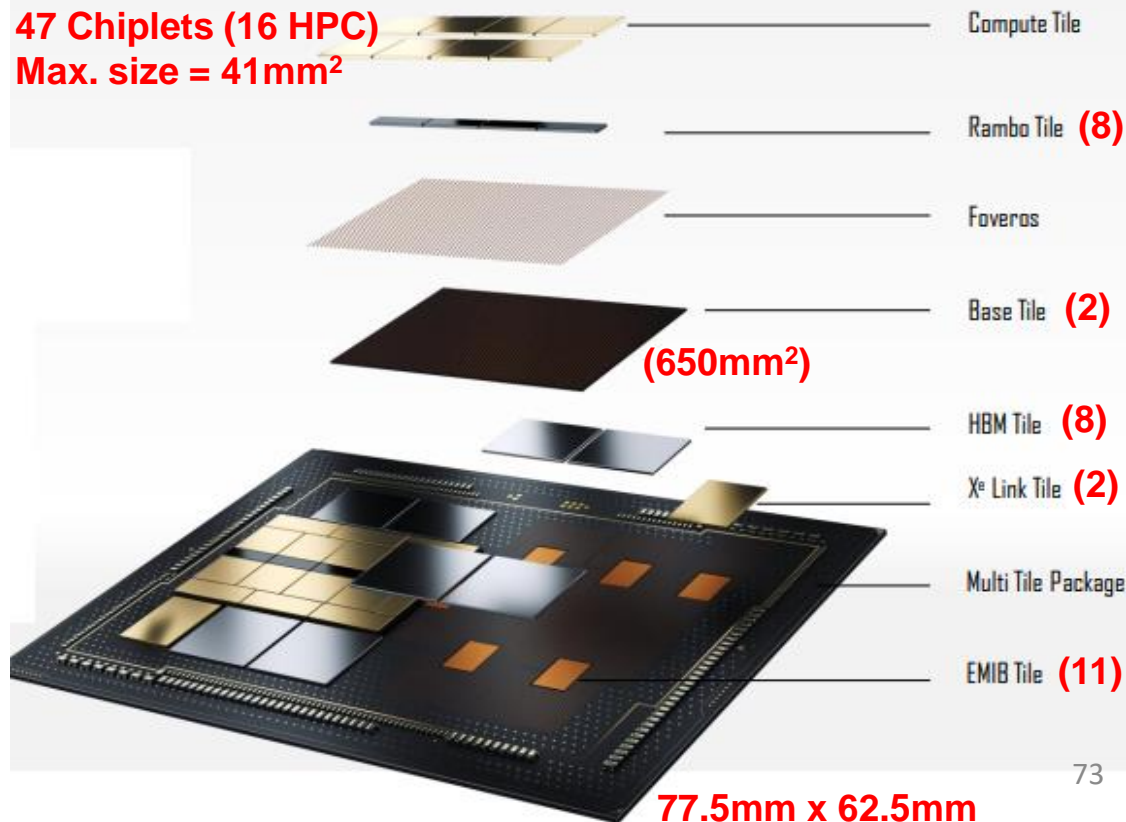

CoWoS with SoIC

HBM · SoC-1 · SoC-2 · SoC-3 · TSV · Interposer · Package Substrate · PCB

InFO PoP with SoIC

DRAM · SoC-1 · SoC-2 · SoC-3 · Fan-Out RDLs · PCB

Classification of Heterogeneous Integration Packaging

- **Chip (CPU)**
- **FAB-1**
- **5nm**
- **12"-wafer**

- **Chip (I/O)**
- **FAB-2**
- **90nm**
- **8"-wafer**

- **Chip (GPU)**
- **FAB-3**
- **7nm**
- **12"-wafer**

Chip (CPU)

Chip (I/O)

Chip (GPU)

Heterogeneous integration or SiP
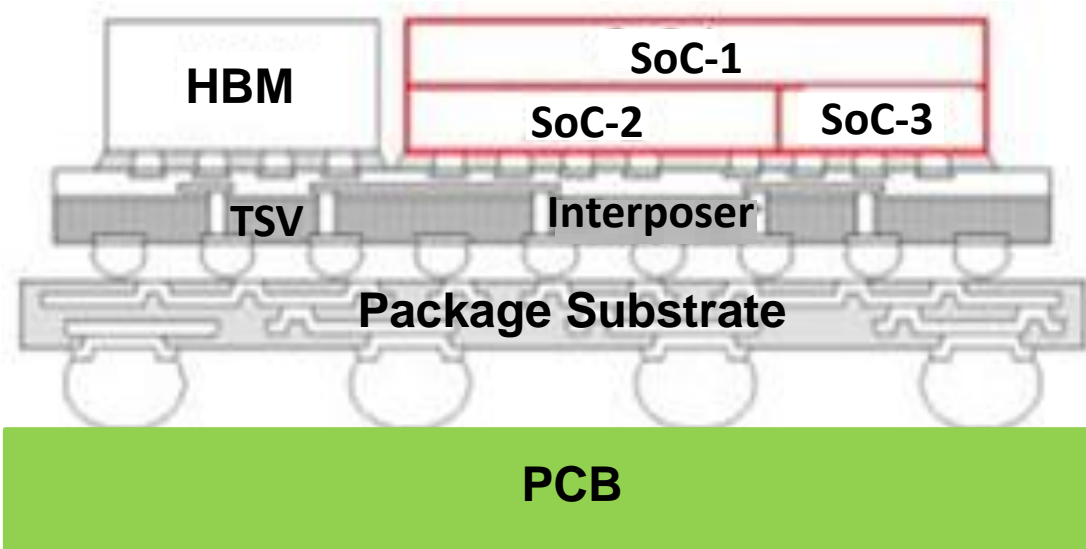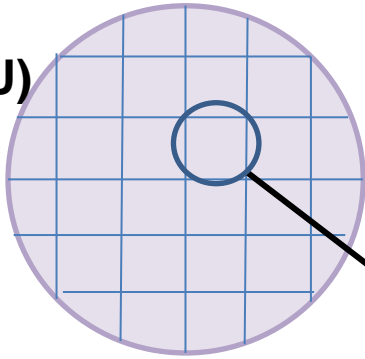
Packaged memory stack

CPU 1

CPU 2

PBGA Memory Stack

I/O

GPU 1

GPU 2

- **Time-to-market**
- **Less IP issues**
- **Flexibility**
- **Low cost alternative than SoC**
- **Optimized signal integrity and power**
- **Better thermal performance**

Heterogeneous integration uses packaging technology to integrate dissimilar chiplets, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.

Classification of Heterogeneous Integrations

➢ **Heterogeneous Integrations on Organic Substrates**

➢ **Heterogeneous Integrations on Silicon Substrates (TSV Interposers)**

➢ **Heterogeneous Integrations on TSV-less Interposers**

➢ **Heterogeneous Integrations on Fan-Out RDL Substrates**

➢ **Heterogeneous Integrations on Ceramic Substrates**

Amkor Automotive SiP (System-in-Package)

- Large singulated body SiP
- Infotainment & ADAS
- Autonomous driving
- Computers in a car
- Increasing trend in designs
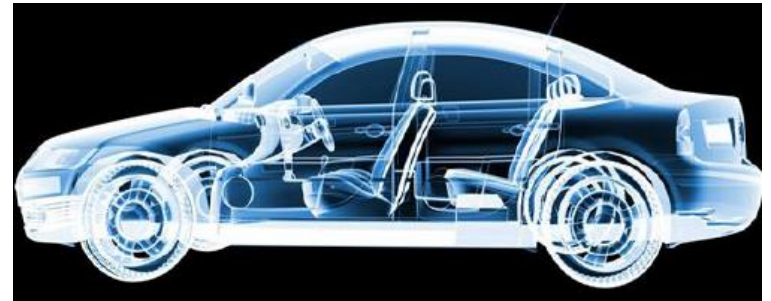
42.5 x 42.5 mm, Infotainment,
Processor + DDR

55 x 72 mm, Network
Switch, ASIC + Memory

Heterogeneous Integration on organic-substrate

The Apple Watch is SiP and was Assembled by ASE (Universal Scientific Industrial – Shanghai)

Smartwatch

Apple Application Processor with SK Hynix LPDDR4 SDRAM

Toshiba NAND Flash

Broadcom BCM15920 Custom Sensing ASIC

Broadcom BCM59356 Wireless Charging Power Management Unit

Apple 338S00348W2 Chip

Qualcomm MDM9635M LTE Modem with Samsung K4P1G324EH SDRAM

Apple/Dialog PMIC

Qualcomm PMD9645 PMIC
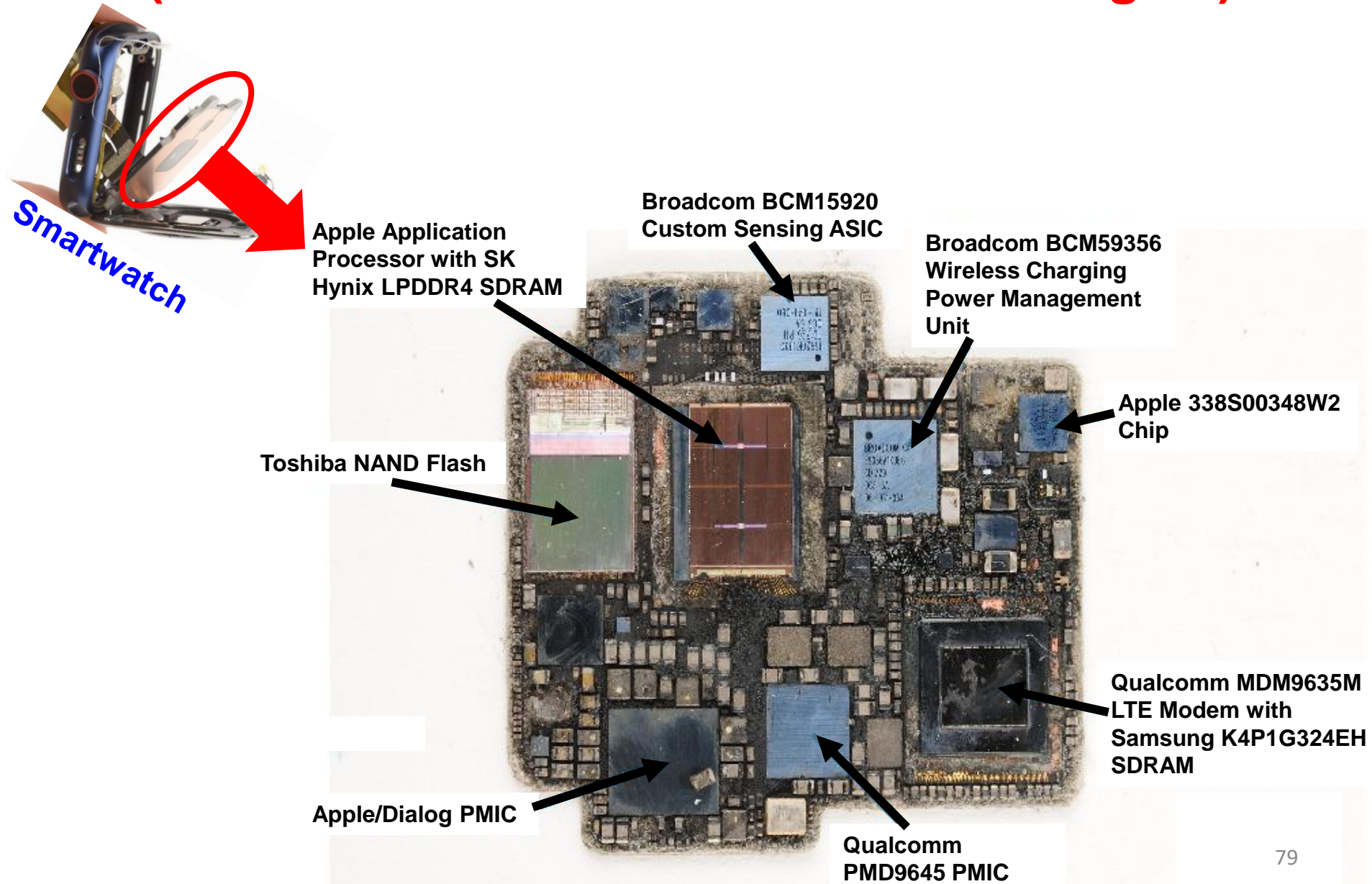
Three Substrate-Like PCBs (SiPs) in iPhone
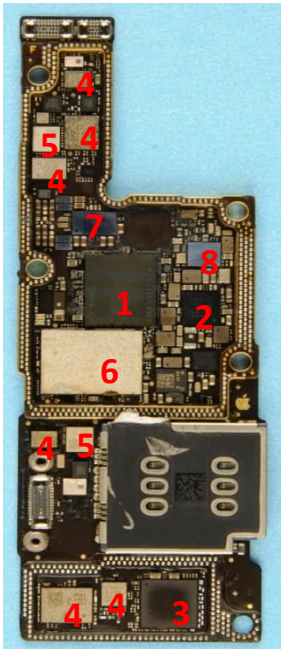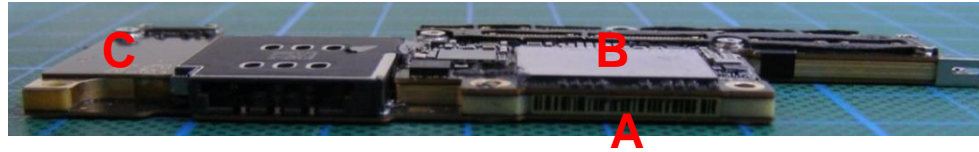
[1] Intel Baseband Chipset
[2] Intel PM IC
[3] Intel RF Transceiver
[4] Skyworks RF FEM
[5] Murata RF FEM (front-end module)
[6] USI WiFi/BT Module
[7] Broadcom Wireless Charger
[8] NXP NFC Controller

Rear PCB (A)
- 8L HDI, 4mSAP layers, 16cm^2
- Single-Sided Assembly
- Baseband, RF, WiFi/BT
- All components face inward

[1] Apple A12 Chipset
[2] Flash Memory
[3] Power Manager
[4] ST Power Manager
[5] Power Manager
[6] TI Battery Charger
[7] Audio Codec
[8] Audio Amplification
[9] Avago RF FEM
[10] Skyworks RF FEM

Front PCB 1 (B)
- 10L HDI, 6 mSAP layers, 10cm^2
- Double-Sided Assembly
- A12 CPU, Memory, Connectors
- A12 CPU faces inward
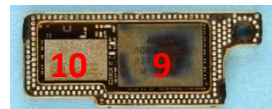
Front PCB 2 (C)
- 6L HDI, 2 mSAP layers, 2cm^2
- Double-Sided Assembly
- RF FEM, Connectors
- RF FEM face inward

Classification of Heterogeneous Integrations

➢ **Heterogeneous Integrations on Organic Substrates**

➢ **Heterogeneous Integrations on Silicon Substrates (Passive TSV-Interposers and Active TSV-Interposers)**

➢ **Heterogeneous Integrations on TSV-less Interposers**

➢ **Heterogeneous Integrations on Fan-Out RDL-Substrates**

➢ **Heterogeneous Integrations on Ceramic Substrates**

Xilinx's HPC Applications Driven by AI and 5G (Passive TSV-Interposer)

Package Substrate

TSV-Interposer

C4-Cu Solder Joint

μSolder Joint

Cu
Ni
SnAg
SnAg
Ni
Cu

Mold Compound

Cu
C4

Si-interposer

Underfill

Cracking

Si-interposer

Underfill

Cu

Intel 3D IC Integration – FOVEROS Technology (Active TSV-Interposer)

Lakefield
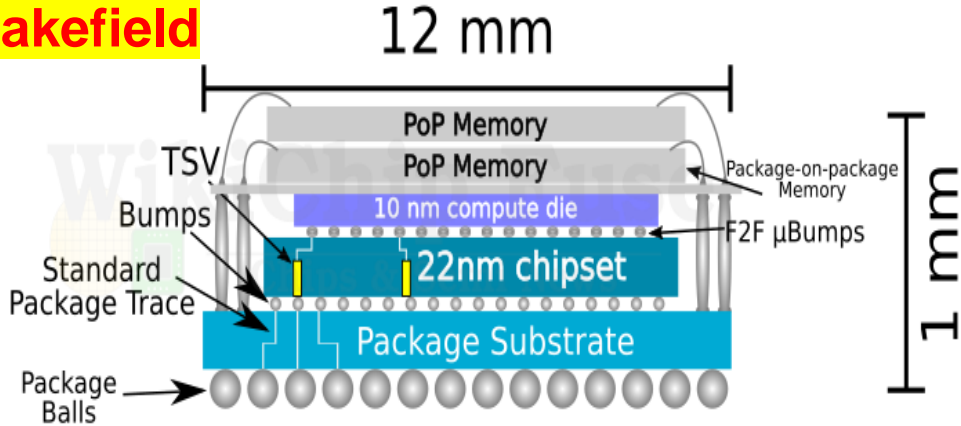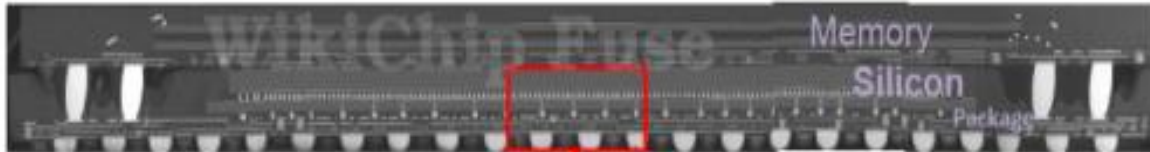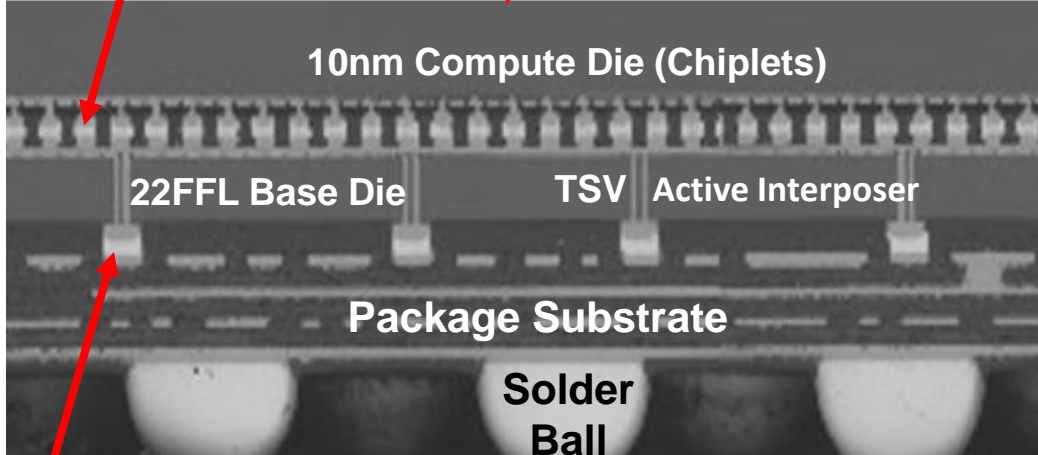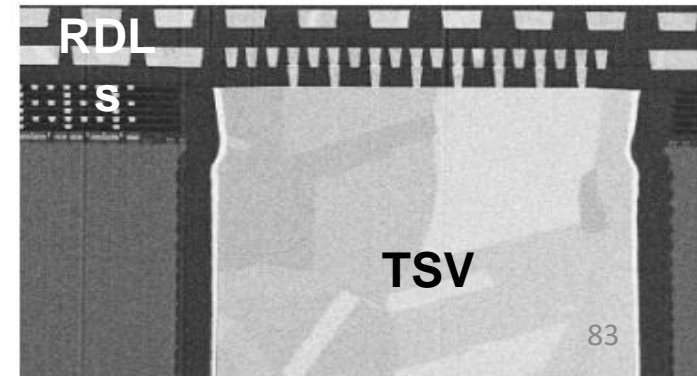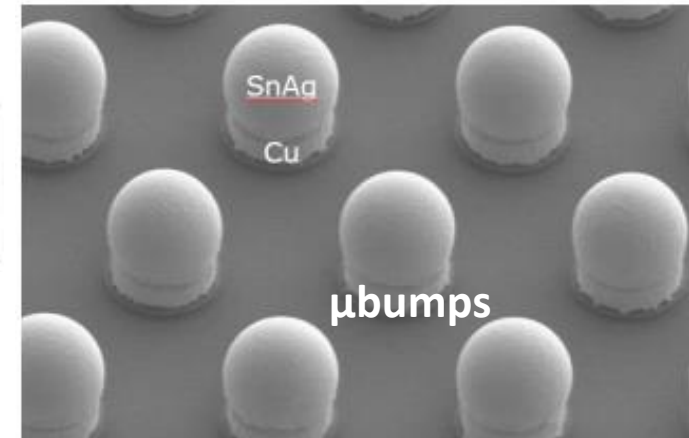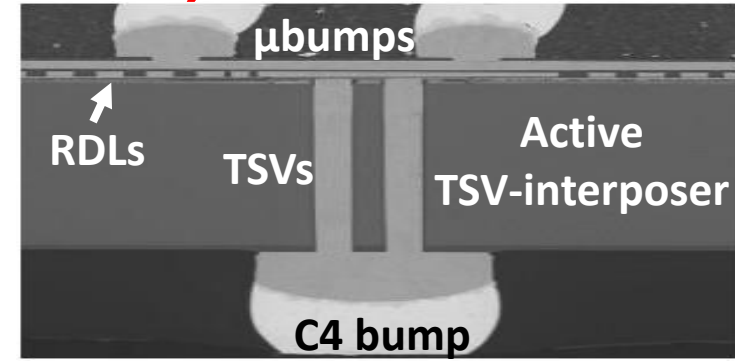
12 mm

PoP Memory
PoP Memory
TSV
Package-on-package Memory
Bumps
10 nm compute die
F2F µBumps
22nm chipset
Standard Package Trace
Package Substrate
Package Balls
1 mm

3D IC Integration

Memory
Silicon
Package

µbump

10nm Compute Die (Chiplets)
22FFL Base Die   TSV   Active Interposer
Package Substrate
Solder Ball

C4 bump

µbumps
RDLs   **TSVs**   **Active TSV-interposer**
C4 bump

SnAg
Cu
µbumps

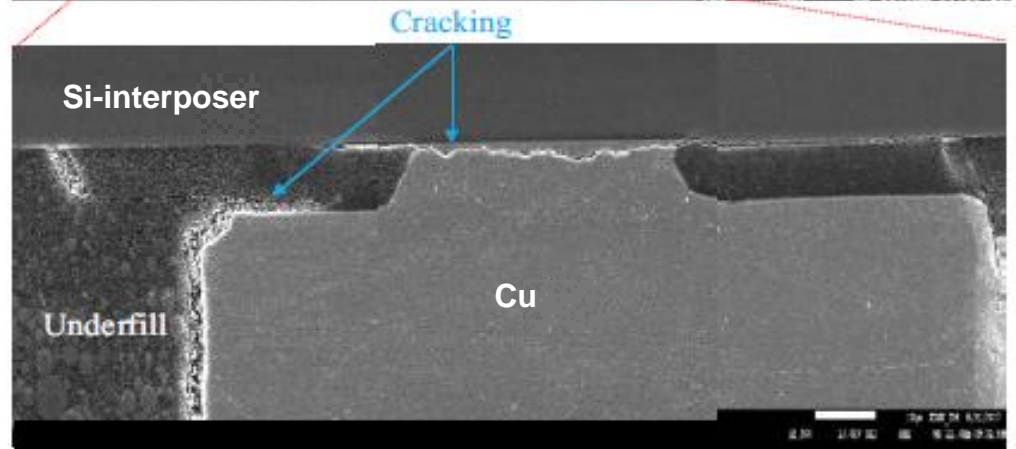**RDLs**
TSV

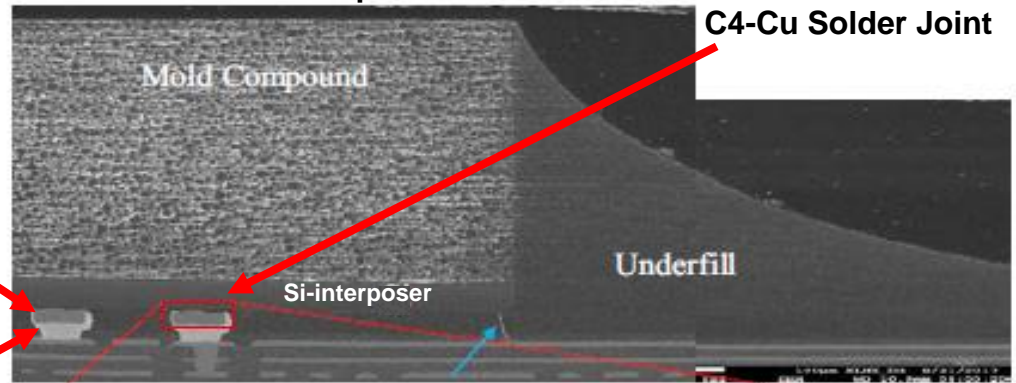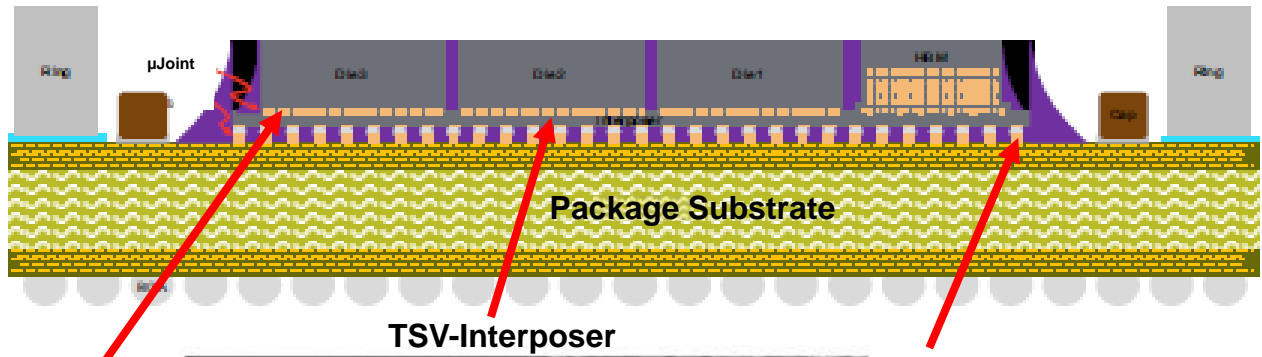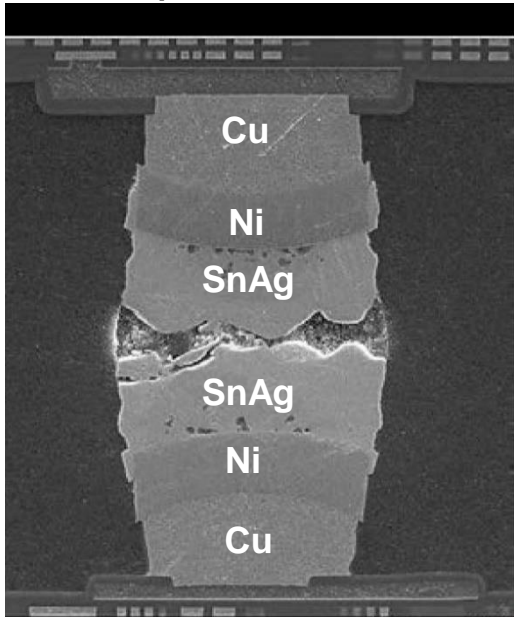Semiconductor Advanced Packaging, 2021

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Classification of Heterogeneous Integrations

➢ **Heterogeneous Integrations on Organic Substrates**

➢ **Heterogeneous Integrations of Silicon Substrates (TSV Interposers)**

➢ **Heterogeneous Integrations on TSV-less Interposer (e.g., Bridges – lateral communication between chiplets)**

➢ **Heterogeneous Integrations on Fan-Out RDL-Substrates**

➢ **Heterogeneous Integrations on Ceramic Substrates**

Lateral Communications (Bridges) between Chiplets

➢ **Bridge Embedded in Build-up Package Substrate**

➢ **Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)**

➢ **Flexible Bridge**

Bridge Embedded in Build-up Package Substrate

Intel's EMIB Patent and Agilex Module

C4 or C2 bumps

CHIP   CHIP   CHIP

102   110   102   110   102

106   108

Embedded Bridge   104   Embedded Bridge

Package Substrate

Solder Ball   112

Intel's Embedded Multi-die Interconnect Bridge (EMIB) in package substrate

CHIP1   CHIP2

EMIB

C2 bump

C4 bump

CHIP1   C2 bump   CHIP2

EMIB

Organic Package Substrate

PCB

Intel® Agilex™ FPGA

Not-to-scale

Intel's FPGA (Agilex) with EMIB

FPGA

C4 bumps

Microbumps

Micro Solder Joint

C4 Solder Joint

C4 Solder Joint

Micro Solder Joint

HBM

RDL

FPGA

RDL

HBM

EMIB

Package Substrate

EMIB

Via

Solder Joint

PCB
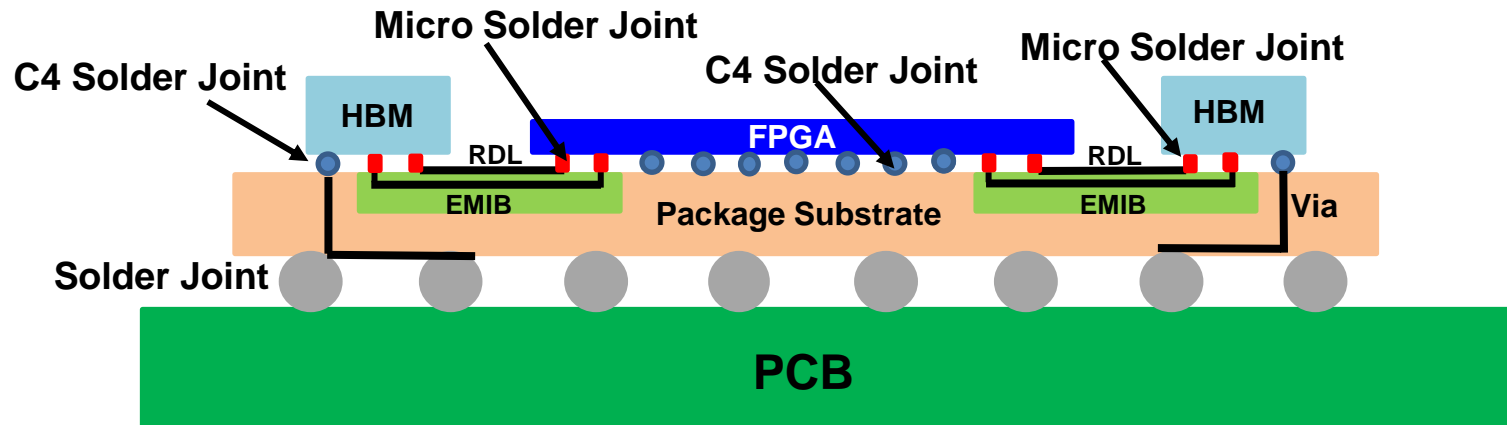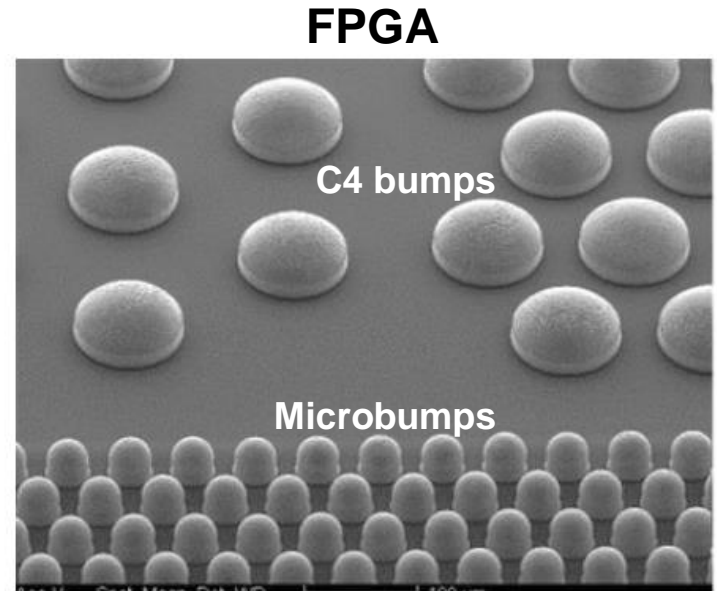
Intel's EMIB
(Embedded Multi-die Interconnect Bridge)

C4 (controlled collapse chip connection) bumps and C2 (Cu-pillar + solder cap) bump on chip

C4 bump

C2 bump
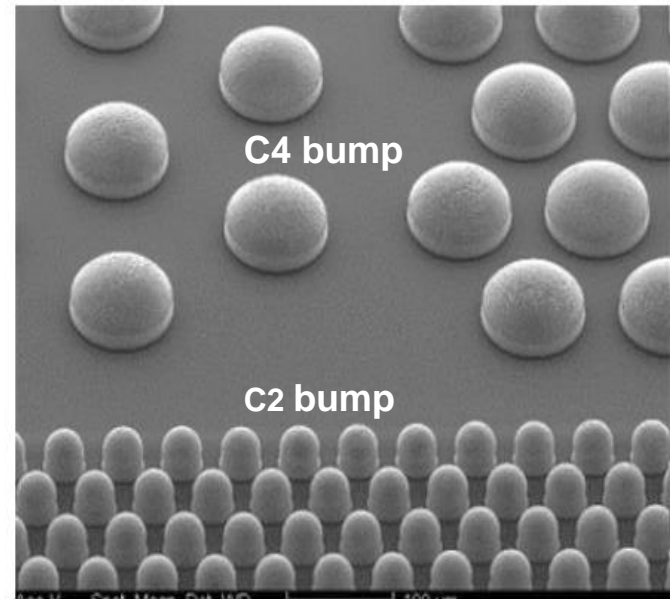
CHIP

- ➤ **The minimum metal L/S/H is 2μm.**
- ➤ **The dielectric layer thickness is 2μm.**
- ➤ **The bridge size is from 2mm x 2mm to 8mm x 8mm**
- ➤ **Usually, there are ≤ 4 RDLs.**

Chip 1 C2 bump C4 bump

Die 2 Chip 2

EMIB

Embedded Multi-die Interconnect Bridge

EMIB Package Substrate

89
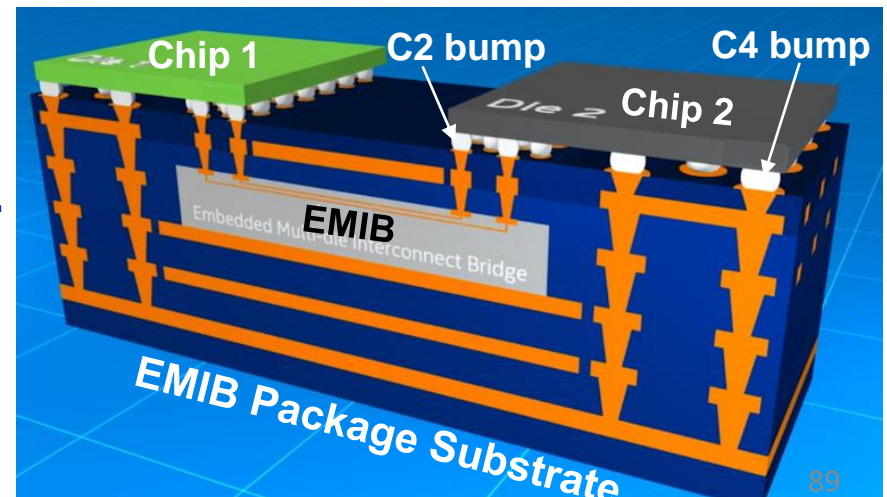
IBM's Direct Bonded Heterogeneous Integration (DBHi) Si Bridge
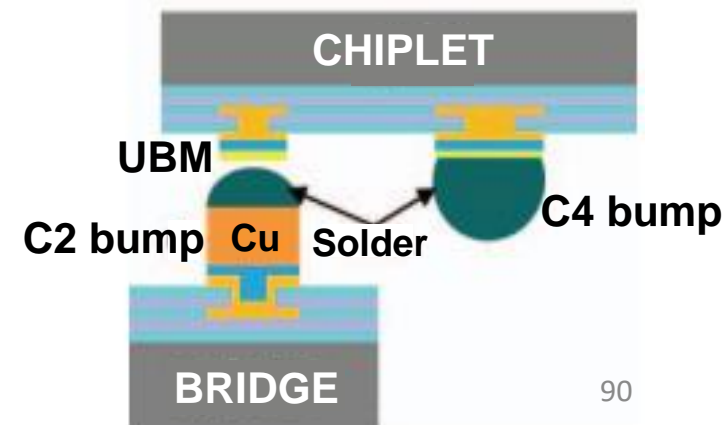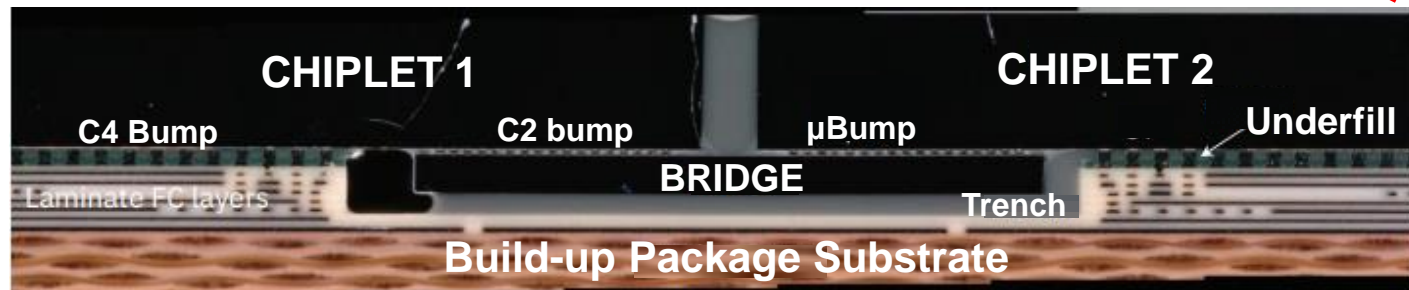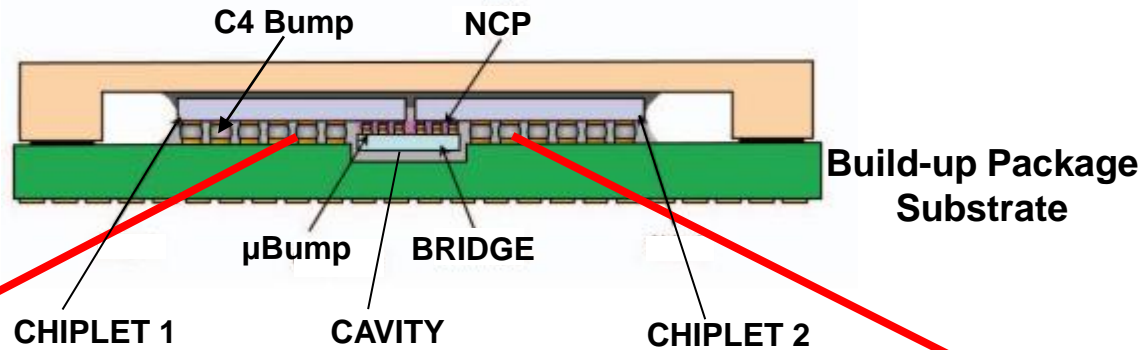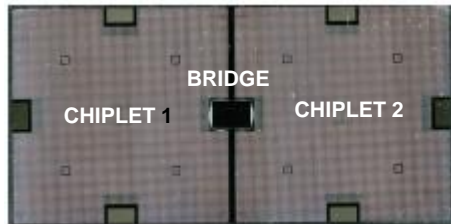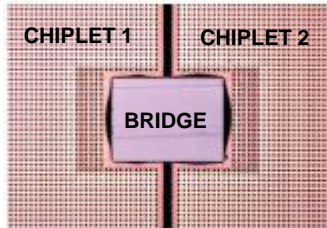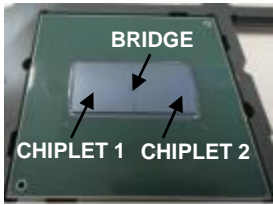
Differences between Intel's EMIB and IBM's DBHi

➢ **For Intel's EMIB, there are two different (C4 and C2) bumps on the chiplets (and there are no bumps on the bridge), while for IBM's DBHi, there are C4 bumps on the chiplets and C2 bumps on the bridge.**

EMIB

C4 bump

C2 bump

CHIPLET

DBHi

CHIPLET

UBM

C2 bump Cu Solder

C4 bump
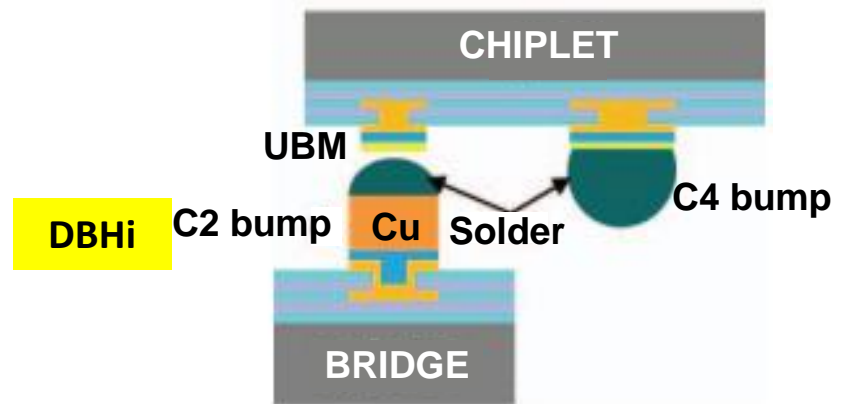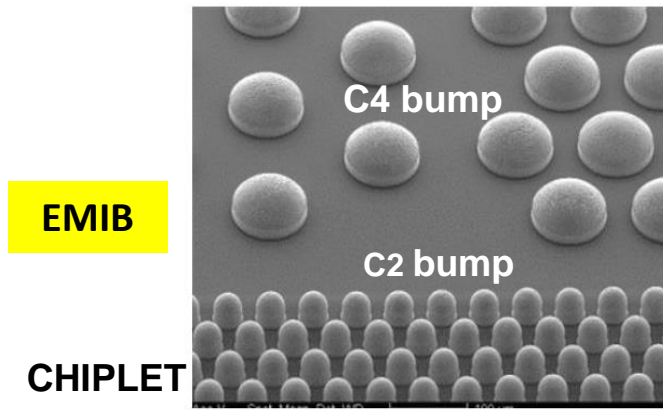
BRIDGE

➢ **For Intel's EMIB, the bridge is embedded in the cavity of a build-up substrate with a die-attach material and then laminated with another build-up layer on top. Therefore, the substrate fabrication is very complicated. For IBM's DBHi, the substrate is just a regular build-up substrate with a cavity on top.**

EMIB

Chip 1 C2 bump C4 bump

Die 2 Chip 2

Embedded Multi-die Interconnect Bridge

EMIB

EMIB Package Substrate

DBHi

Package Substrate with cavity
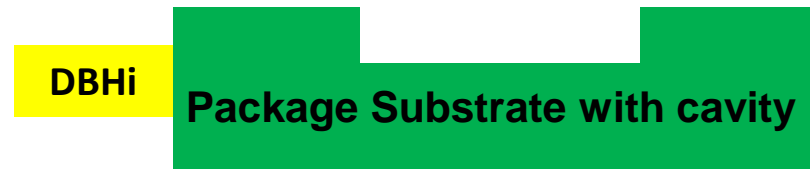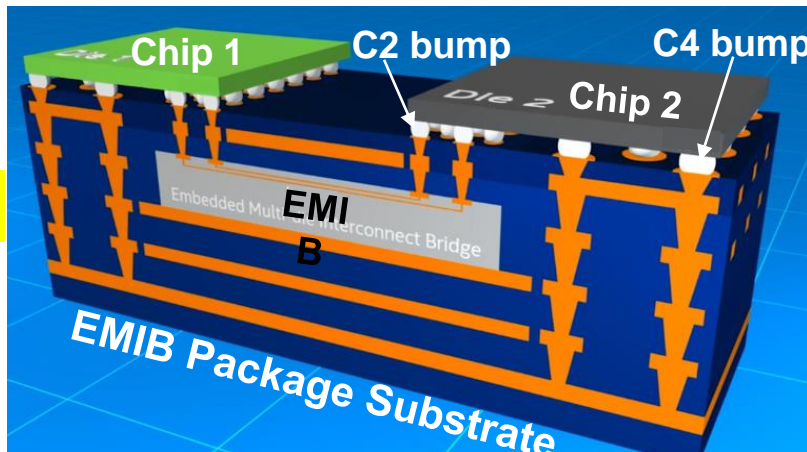
IBM's DBHi Key Process Steps

Bridge

C4 bump

C2 bump

Chip 1

Bridge

Chip 1 **NCP/TCB**

Chip 1 **Chip 2**

Bridge **NCP/TCB**

Organic Substrate with cavity

BRIDGE

C4 bump

C2 bump

UBM

CHIPLET

Chip 1 **Chip 2**

Bridge

C4 bump reflow on substrate

Underfill is optional

Organic Package Substrate with cavity
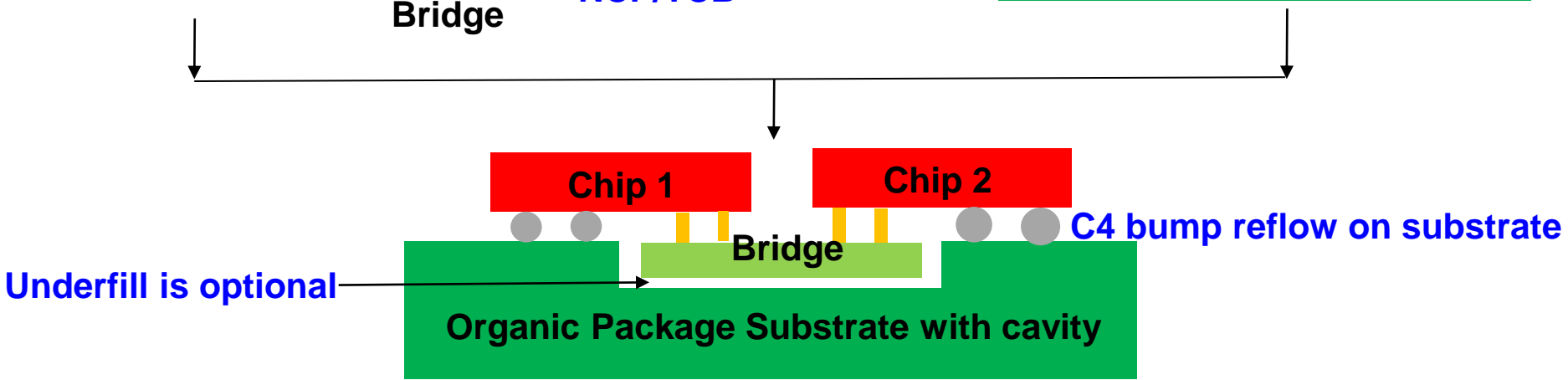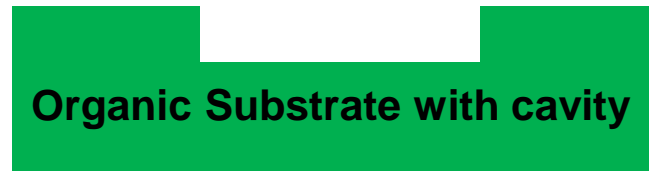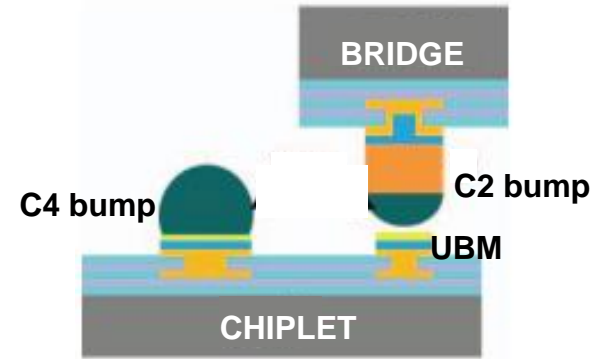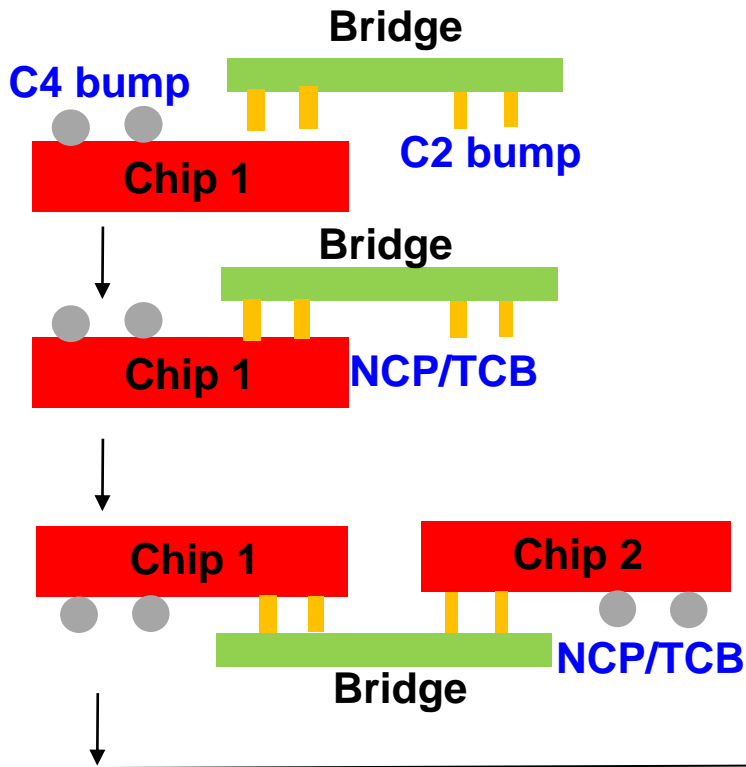
Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)

Applied Materials' Fan-out Chip (Bridge)
First Face-up Process
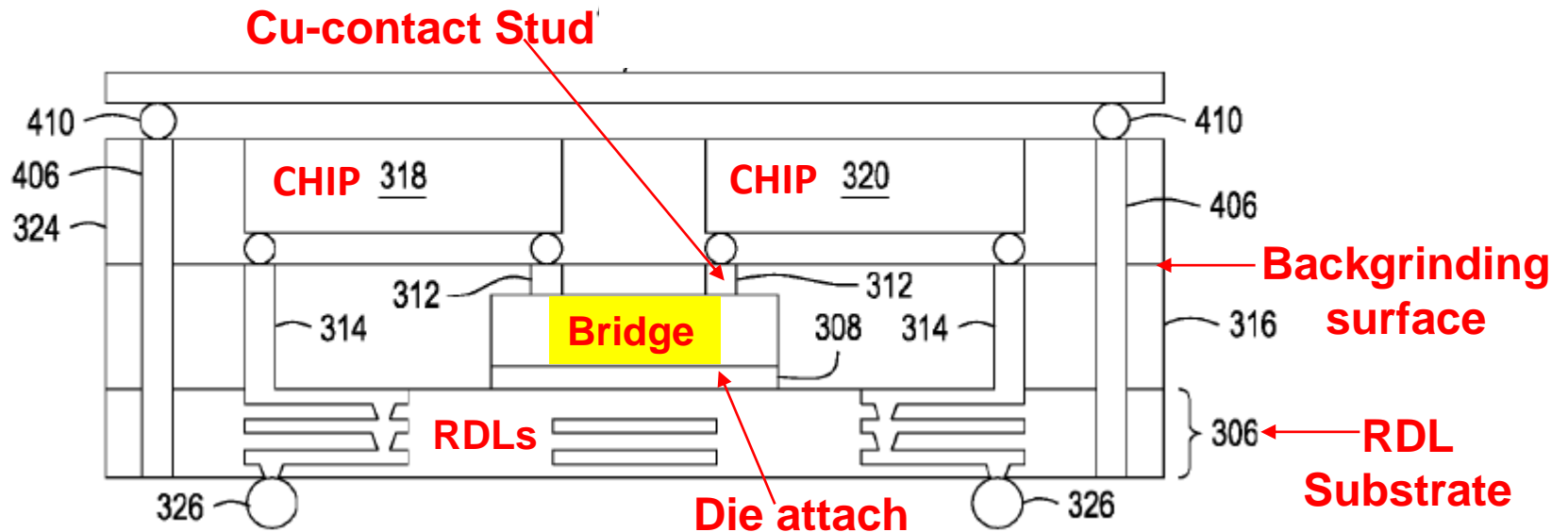
US patent 10,651,126 (filed on December 8, 2017)

TSMC's LSI (Local Silicon Interconnect)

Fan-out Chip (Bridge) First Face-up Process

InFO_LSI
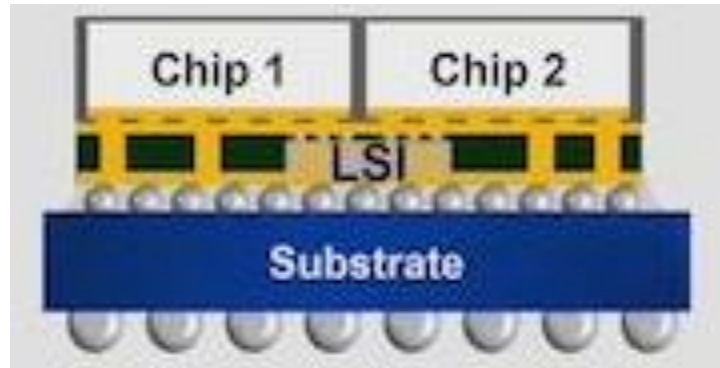
CoWoS_LSI
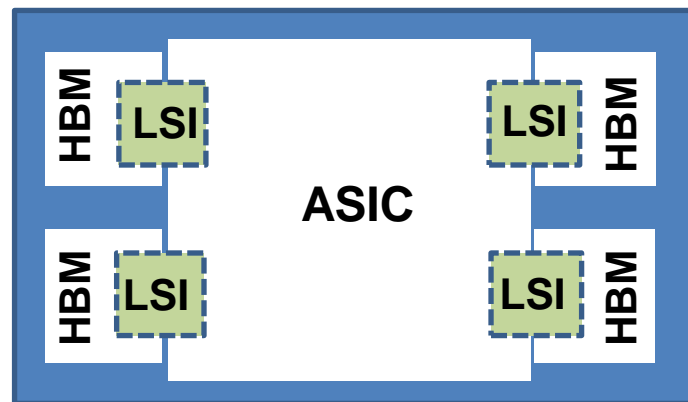
Apple's UltraFusion
(M1 Ultra = M1 Max + M1 Max + Si Bridge)
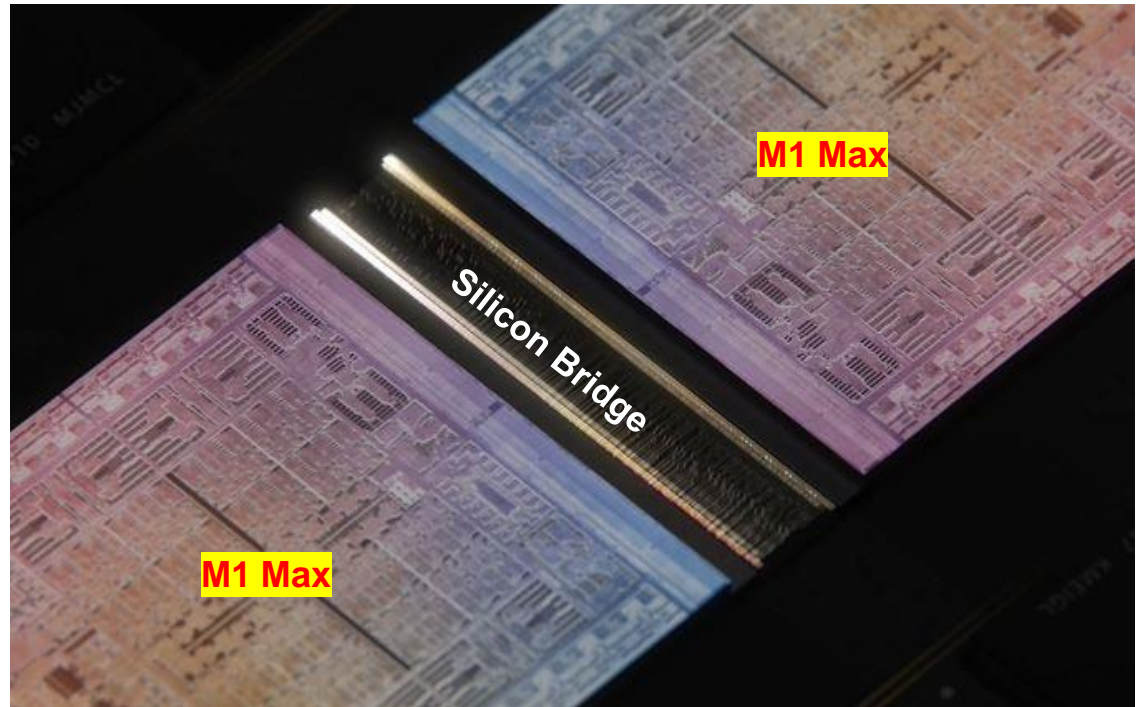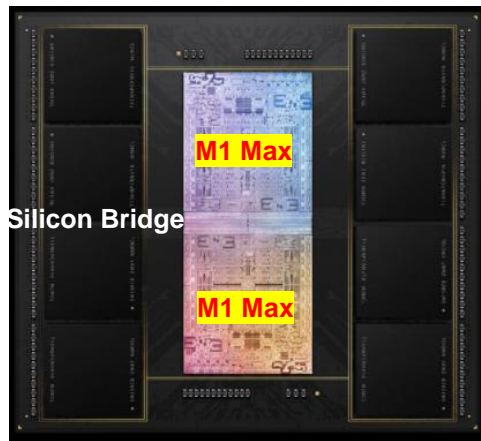
UltraFusion — Apple's innovative packaging architecture that interconnects the die of two M1 Max chips to create a system on a chip (SoC) with unprecedented levels of performance and capabilities

March 8, 2022

Unimicron's Fan-out Chip (Bridge) First Face-down Process
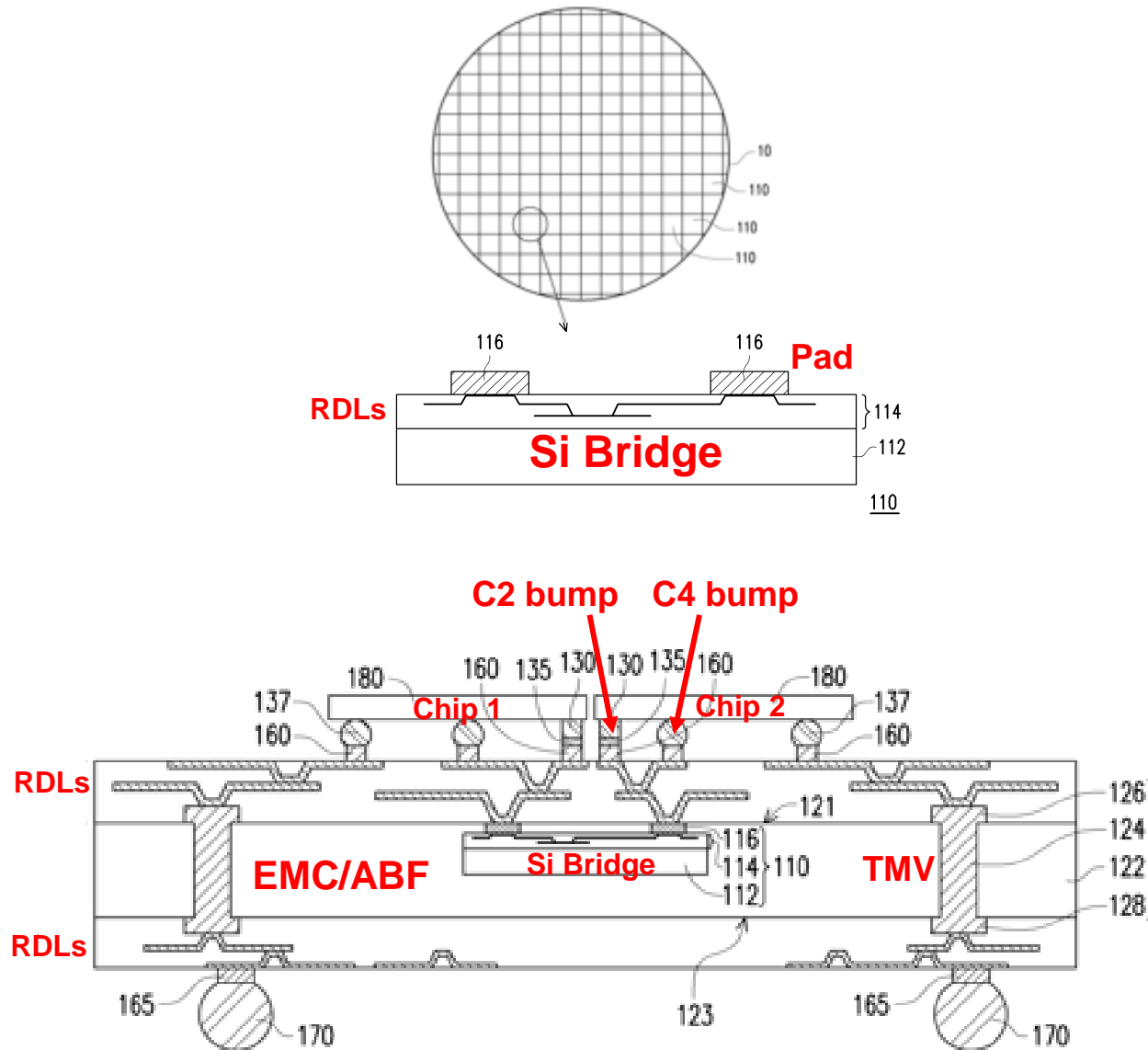
U.S. patent was filed on May 7, 2021

Advanced HDFO Packaging Solutions for Chiplets Integration in HPC Application

Lihong Cao Teck Lee[1] , Yungshun Chang[1] , SimonYL Huang[1] , JY On[1] , Emmal Lin[1] and Owen Yang[1]
Advanced Semiconductor Engineering Inc. (US) Inc., Austin, TX 78704. USA 1 Corporate R&D Center, Advanced Semiconductor Engineering Inc., Kaohsiung, Taiwan (R.O.C)
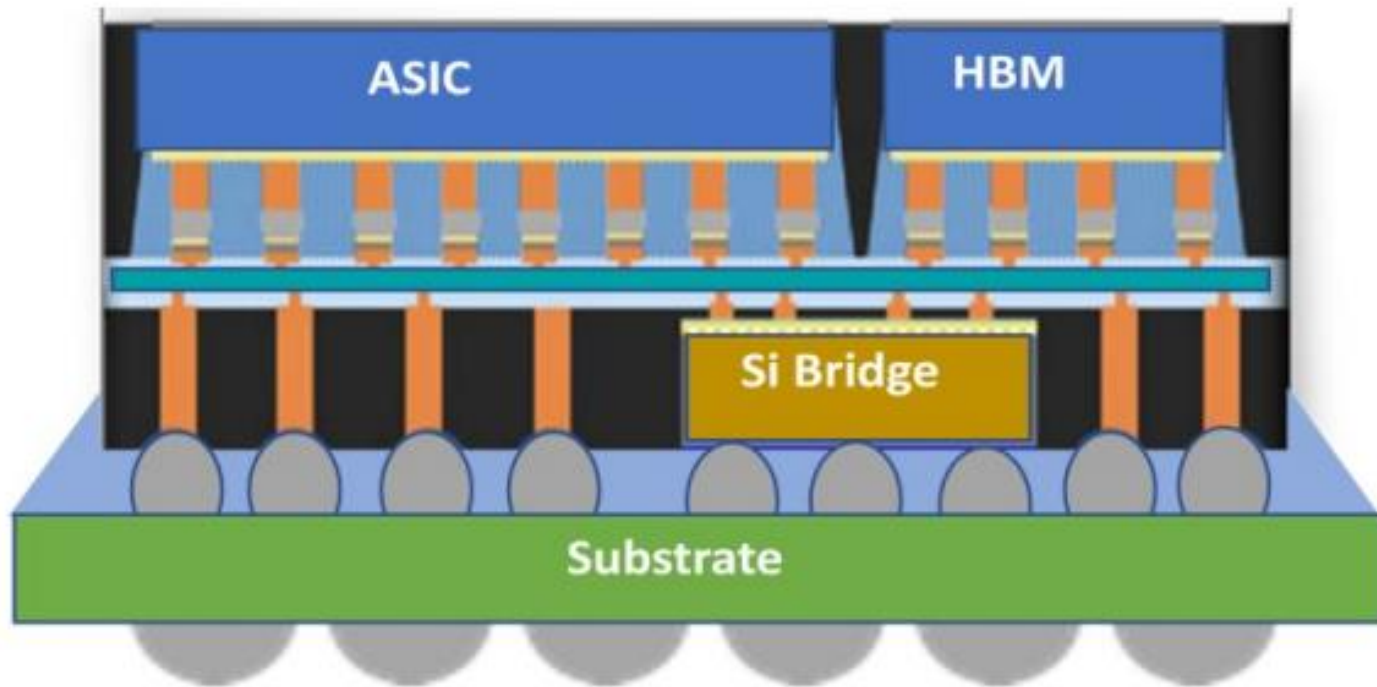
sFOCoS (Stacked Si bridge Fan-Out Chip-on-Substrate)

S-Connect Fan-out Interposer For Next Gen Heterogeneous Integration

JiHun Lee, GamHan Yong, MinSu Jeong, JongHyun Jeon, DongHoon Han, MinKeon Lee , WonChul Do, EunSook Sohn, Mike Kelly, Dave Hiner JinYoung Khim
Research & Development Amkor Technology Korea Incheon, Korea JinYoung.Khim@amkor.co.k

(a) ASIC or processor
(b) HBM
(c) integrated passive device or active device
(d) **bridge die for ASIC to memory interconnection**
(e) Package substrate
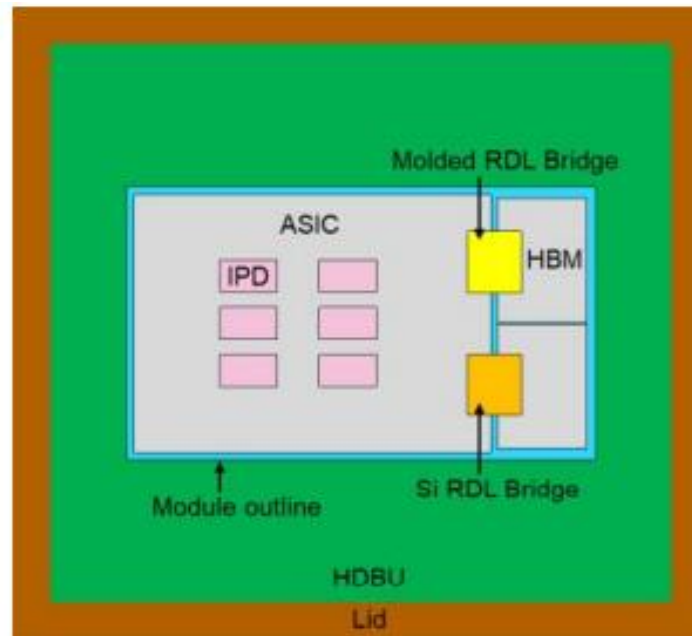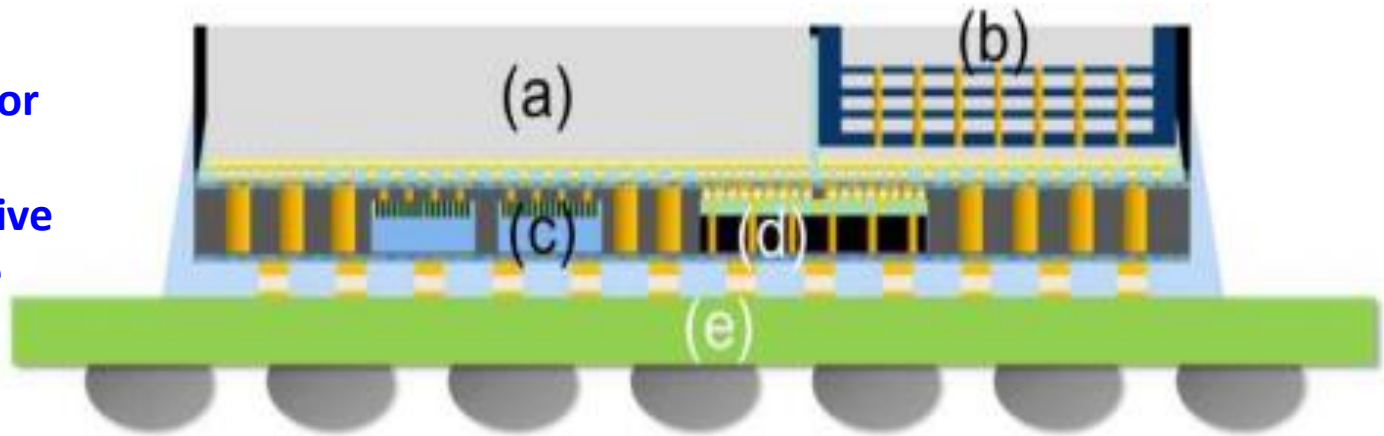
Electrical Performances of Fan-Out Embedded Bridge (FO-EB)

JinWei You, Jay Li, David Ho, Jackson Li, Ming Han Zhuang, David Lai, C. Key Chung, Yu-Po Wang

Siliconware Precision Industries Co. Ltd Taichung, Taiwan jinweiyou@spil.com.tw
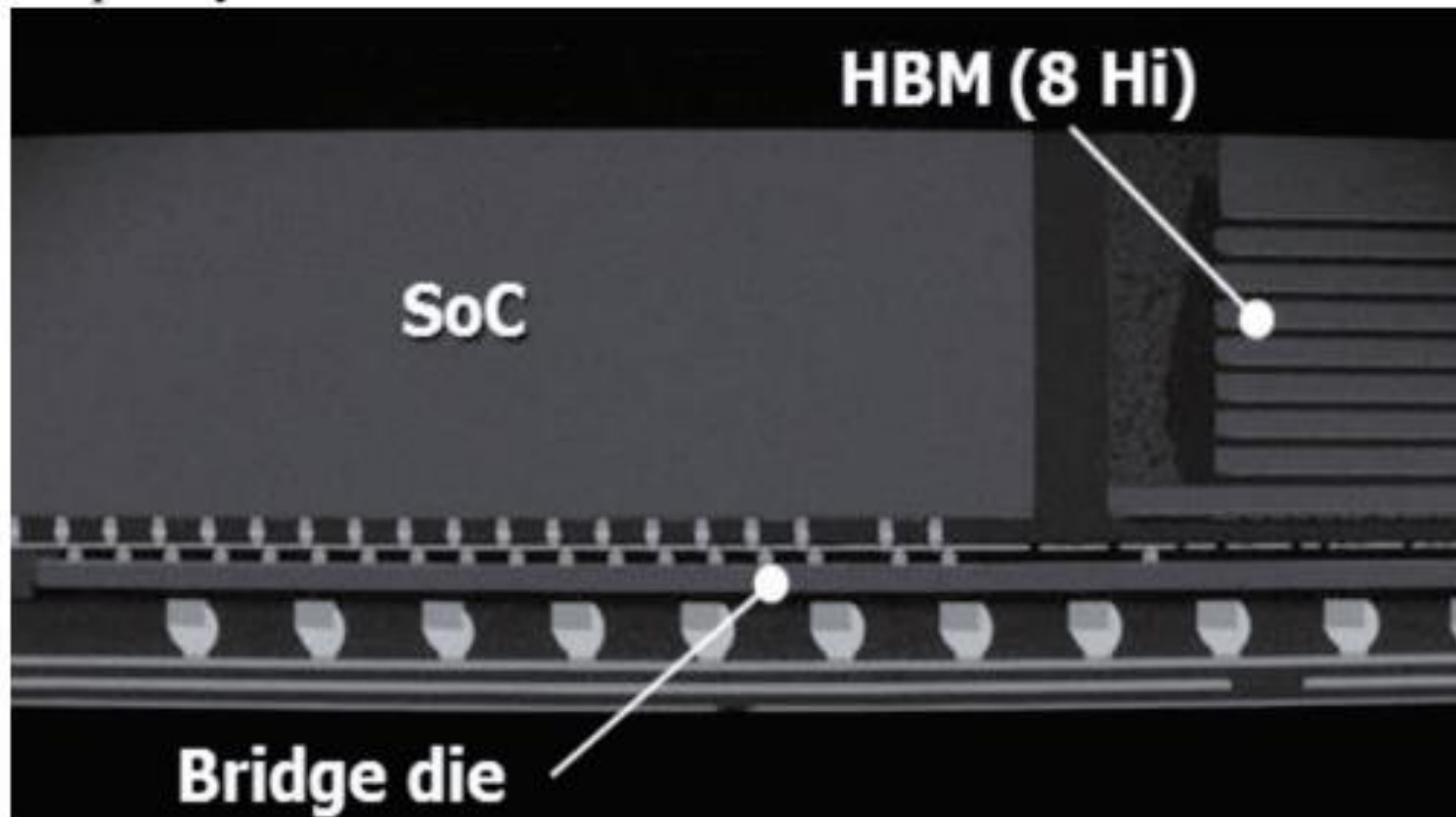
Heterogeneous Integration with Embedded Fine Interconnect (EFI)

Chai Tai Chong, Lim Teck Guan, David Ho, Han Yong, Chong Ser Choong, Sharon Lim Pei Siang, Surya Bhattacharya Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research) 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634 chaitac@ime.a-star.edu.sg, +65-6770-5425
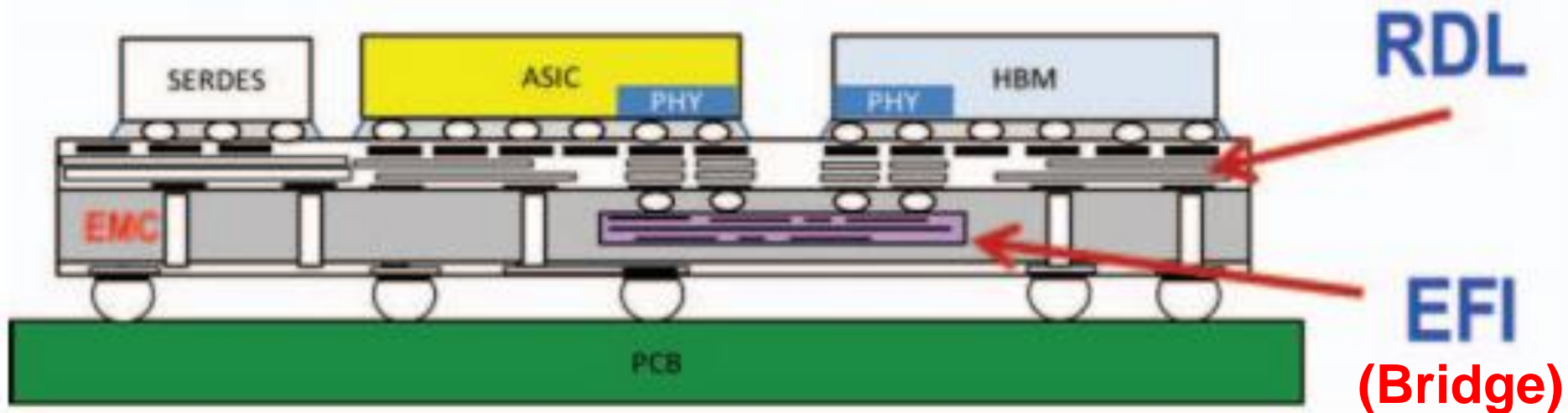
IEEE/ECTC June 2021

Flexible Bridge

Flexible Bridge

MOUNTING, INTERCONNECT AND COMMUNICATION STRUCTURE 106

PROXIMITY COMMUNICATION STRUCTURE 108

FLEXIBLE BRIDGE 100

BASE CHIP 102

NEIGHBORING CHIP 104

BASE CHIP 102

NEIGHBORING CHIP 104

FLEXIBLE BRIDGE 100
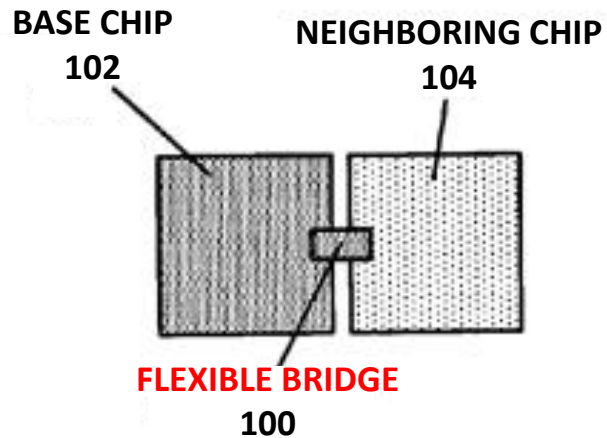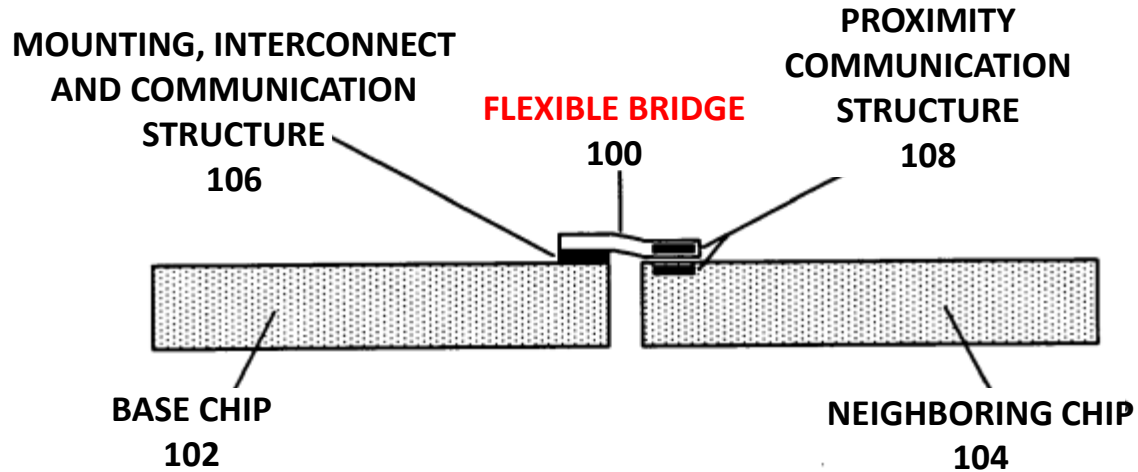
U.S. 2006/0095639 A1 was filed by SUN Microsystems

Classification of Heterogeneous Integrations

➢ **Heterogeneous Integrations on Organic Substrates**

➢ **Heterogeneous Integrations of Silicon Substrates (TSV Interposers)**

➢ **Heterogeneous Integrations on TSV-less Interposer (Bridges)**

➢ **Heterogeneous Integrations on Chip-First and Chip-Last Fan-Out RDL-Substrates (interposer) – 2.3D IC Integration**

➢ **Heterogeneous Integrations on Ceramic Substrates**

Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate (FOCoS)

Yuan-Ting Lin, Wei-Hong Lai, Chin-Li Kao, Jian-Wen Lou, Ping-Feng Yang, Chi-Yu Wang, and Chueh-An Hseih*

Advanced Semiconductor Engineering (ASE), Inc.
e-mail: Adren_Hsieh@aseglobal.com

Chip-First

CoWoS

ASE's FOCoS

EMC
Die1
Die2
TSV-interposer + RDLs
Package Substrate
Microbumps + Underfill
C4 bumps
Solder Balls
Underfill

EMC
Die1
Die2
RDLs
Package Substrate
Underfill
Solder Balls
C4 bumps

EMC
Chip1
Chip2
RDLs
C4 bumps
Package Substrate
Solder Balls
Underfill

EMC
Chip1
Chip2
RDLs
C4 bumps
RDLs
Package Substrate
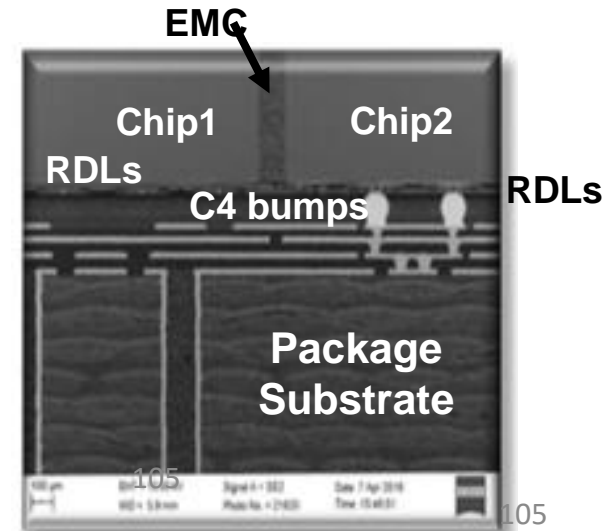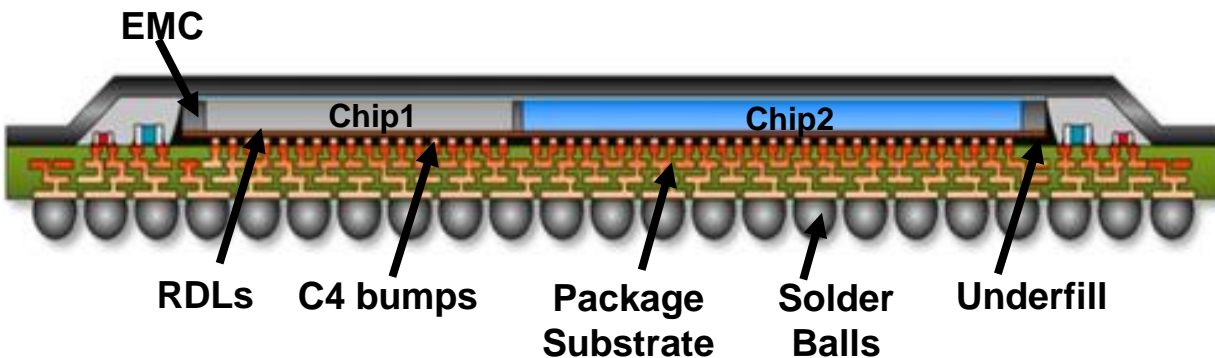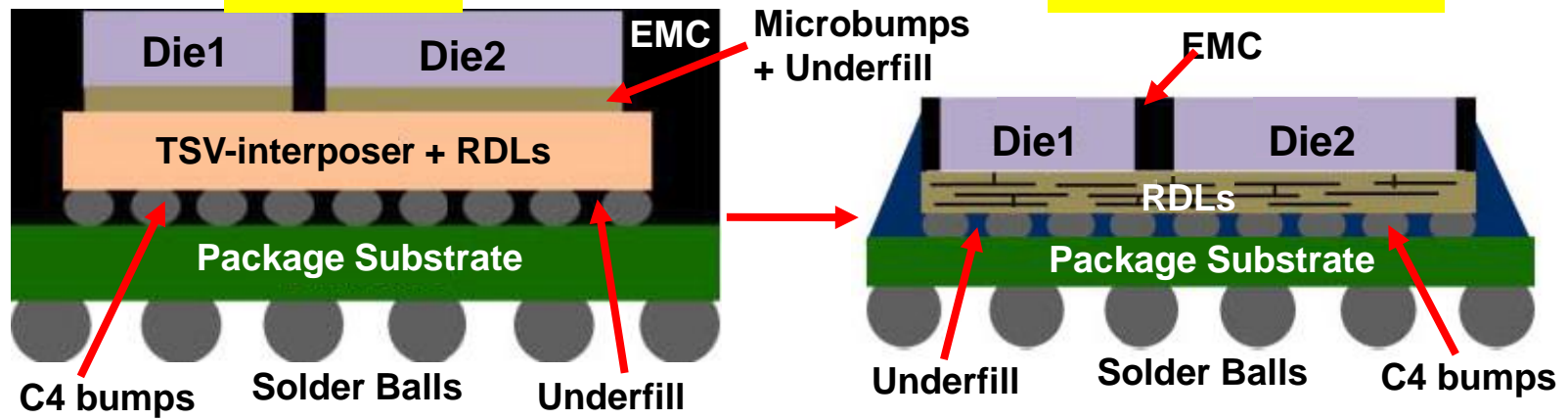
Heterogeneous Integration with Multilayer Fan-Out RDL Interposer

Yi-Hang Lin, M.C.Yew, M.S. Liu ,S.M. Chen, T.M. Lai, P.N. Kavle, C.H. Lin, T.J. Fang, C.S. Chen, C.T. Yu, K.C. Lee, C.K. Hsu, P.Y. Lin, F.C Hsu and Shin-Puu Jeng*

TSMC, No.6, Creation Rd. II, Hsinchu Science Park, Hsinchu, Taiwan (R.O.C.) 30077

Email: *spjeng@tsmc.com
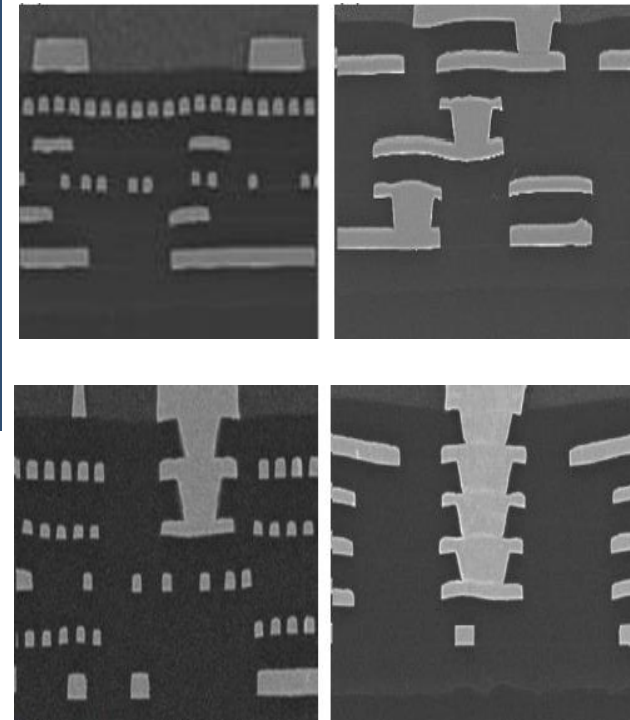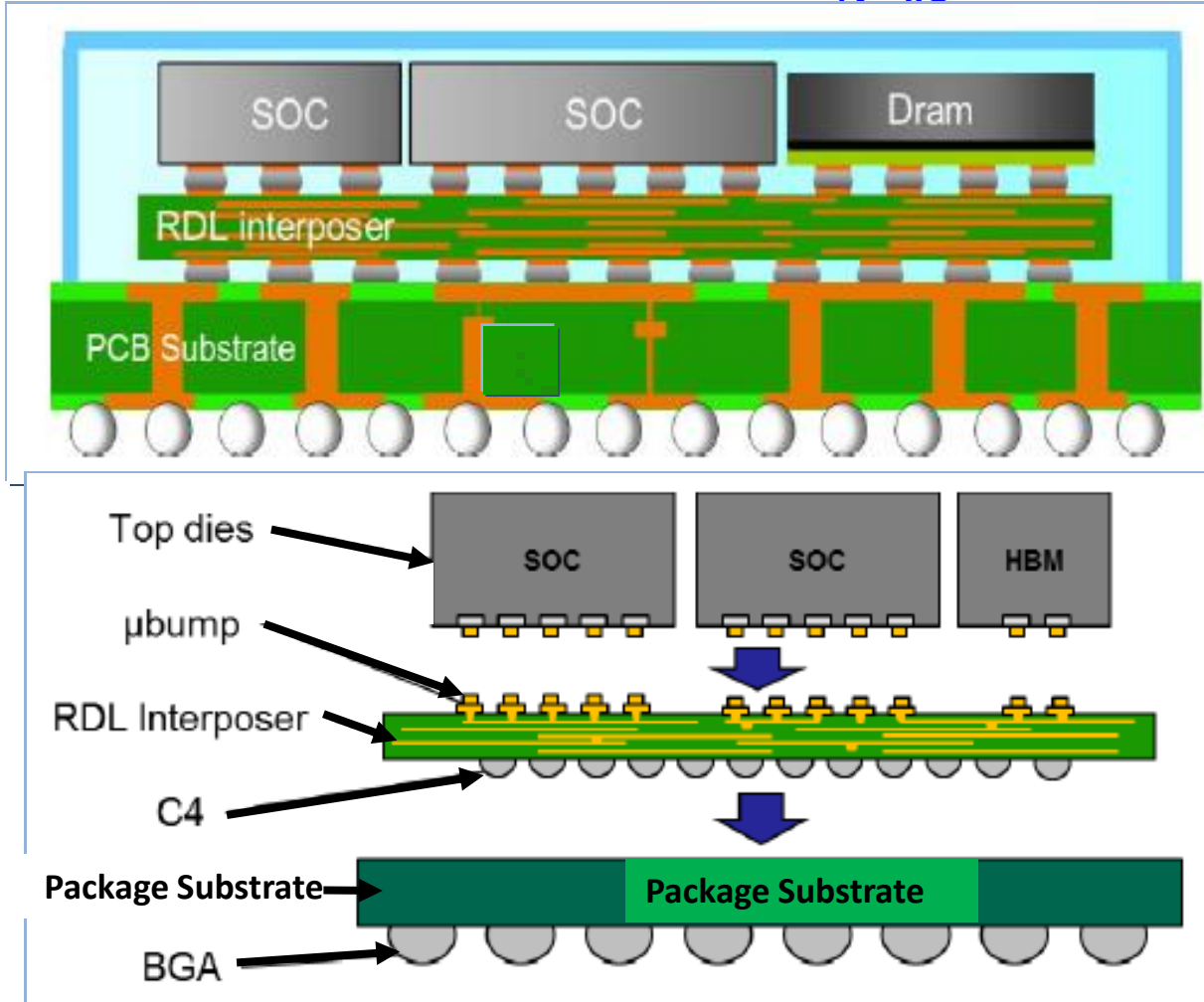
Chip-Last

Classification of Heterogeneous Integrations

➢ **Heterogeneous Integrations on Organic Substrates**

➢ **Heterogeneous Integrations of Silicon Substrates (TSV Interposers)**

➢ **Heterogeneous Integrations on TSV-less Interposer (Bridges)**

➢ **Heterogeneous Integrations on Fan-Out RDL-Substrates**

➢ **Heterogeneous Integrations on Ceramic Substrates**

MCM (Multichip Module) on Ceramic Substrate
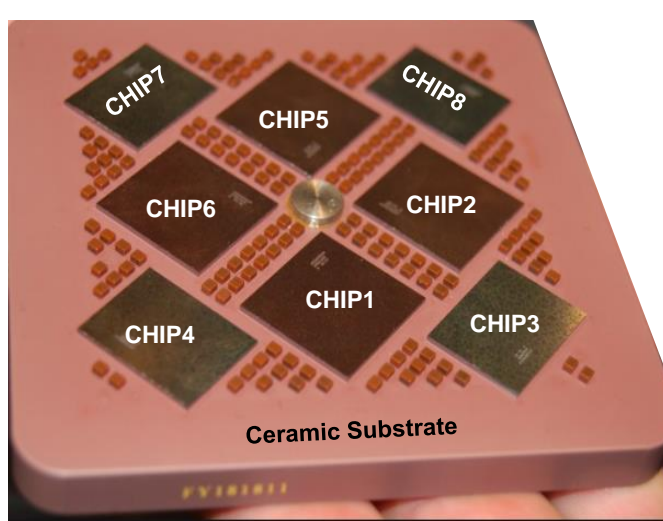
MCM on Ceramic Substrate

IBM 9121 TCM
(Thermal Conduction Module)

- ➢ **TCM weighs 2.2Kg**
- ➢ **Contains up to 121 chips about 8-10mm square**
- ➢ **Each chip has a spring-loaded Cu piston to remove heat**
- ➢ **Up to 10W dissipation per chip**
- ➢ **Up to 600W dissipation per TCM**
  Ceramic substrate has:
  - ❑ **63 layers**
  - ❑ **Up to 400m of wirings**
  - ❑ **Up to 2 million vias**
- ➢ **5Kg air-cooled heatsink to remove heat from TCM**

How to Select Substrate for Heterogeneous Integration Packaging?

➢ **It depends on the applications.**

➢ **The most important indicator (selection criterion) is the metal line width and spacing of the RDLs for the substrates being used for the heterogeneous integrations.**

➢ **Also, low loss dielectric materials for high-speed and high-frequency are very important.**

Heterogeneous Integrated Substrates (Next 5 Years)
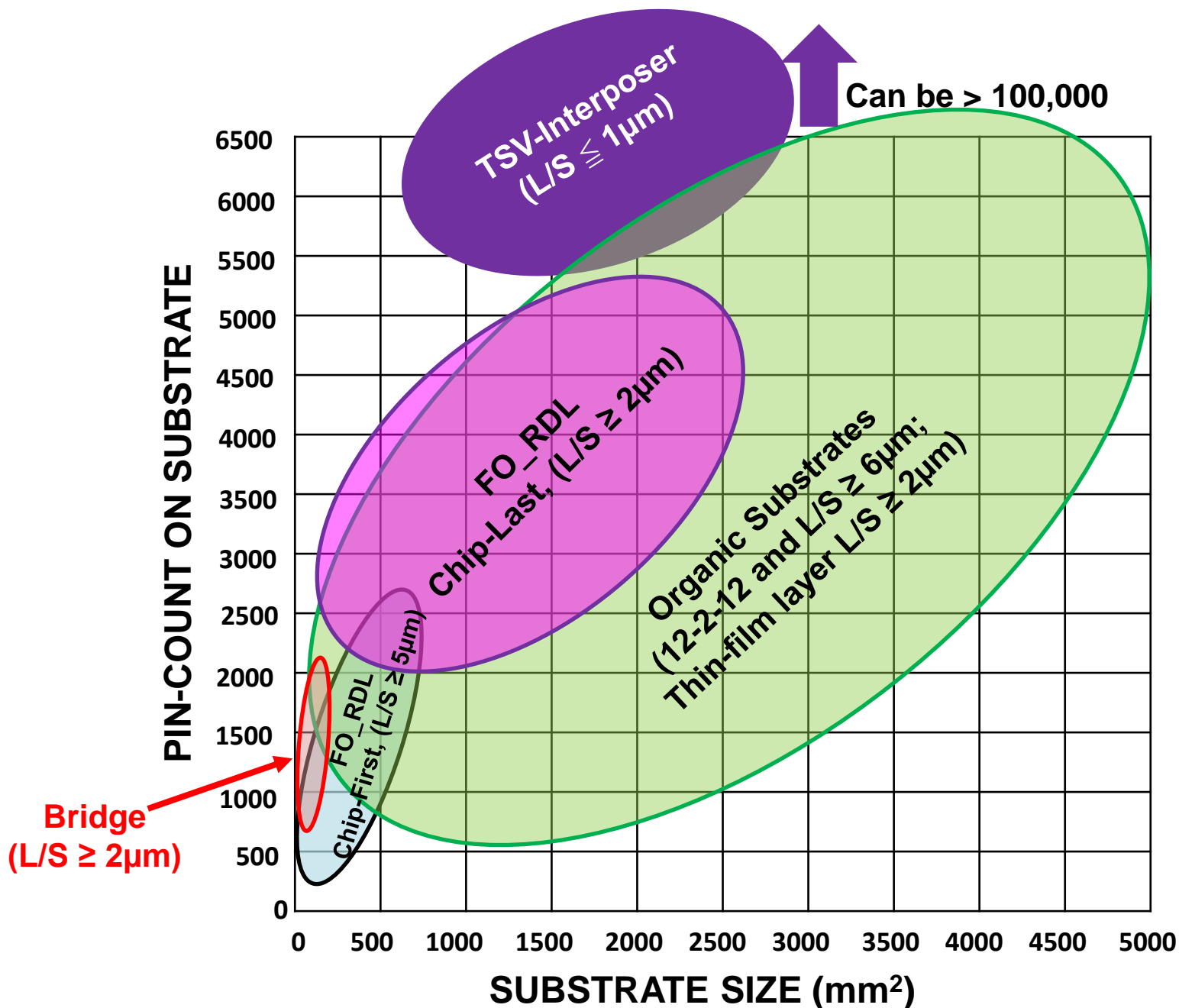
Hybrid Substrates for HPC and Data Center Applications Driven by AI and 5G/6G

➢ **Hybrid Substrate = Inorganic Substrate + Organic Substrate**

➢ **Inorganic Substrate made from PECVD, PVD, Stepper, ECD, CMP, etc.**

➢ **Organic Substrate made from PID, PVD, LDI, ECD, etc.**

C4 Bump or Solder Ball — 195

175 — 171 — 170

RDL22

Organic Substrate

Fine Metal L/S RDL-substrate
➢ Photoimageable Dielectric (≥ 3µm)
➢ 2µm ≤ Metal L/S ≤ 10µm

RDL21

Inorganic Substrate

Ultra-Fine Metal L/S RDL-substrate
➢ SiO_2 Dielectric (~ 1µm)
➢ Metal L/S < 2µm

RDL12
RDL11

118
189 — Microbump/Bumpless
187 — 113 — 190

185 — CHIP
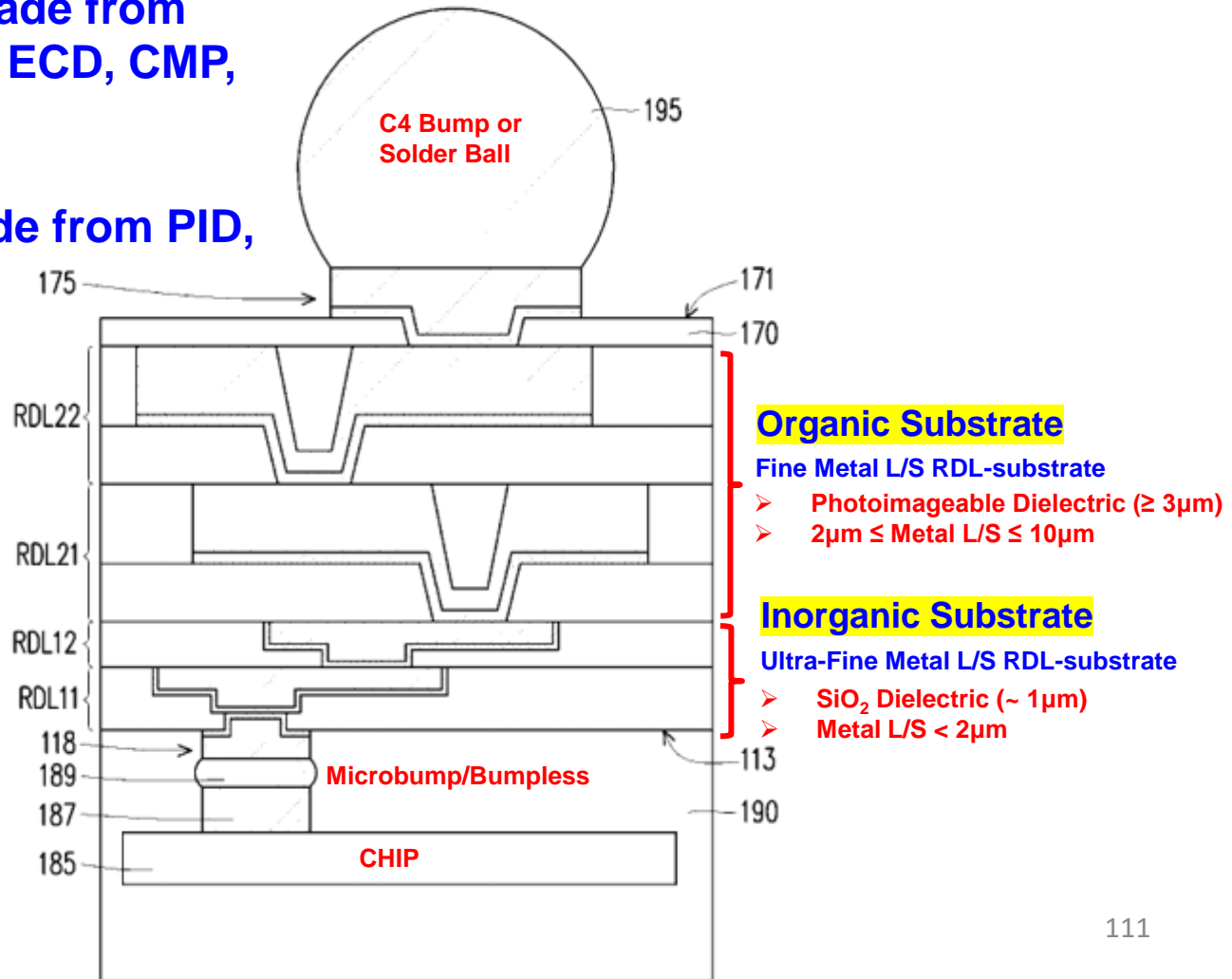
Roadmap for Df (Dissipation Factor or Loss Tangent) and Dk (Dielectric Constant or Permittivity)

Semiconductor Advanced Packaging, 2021
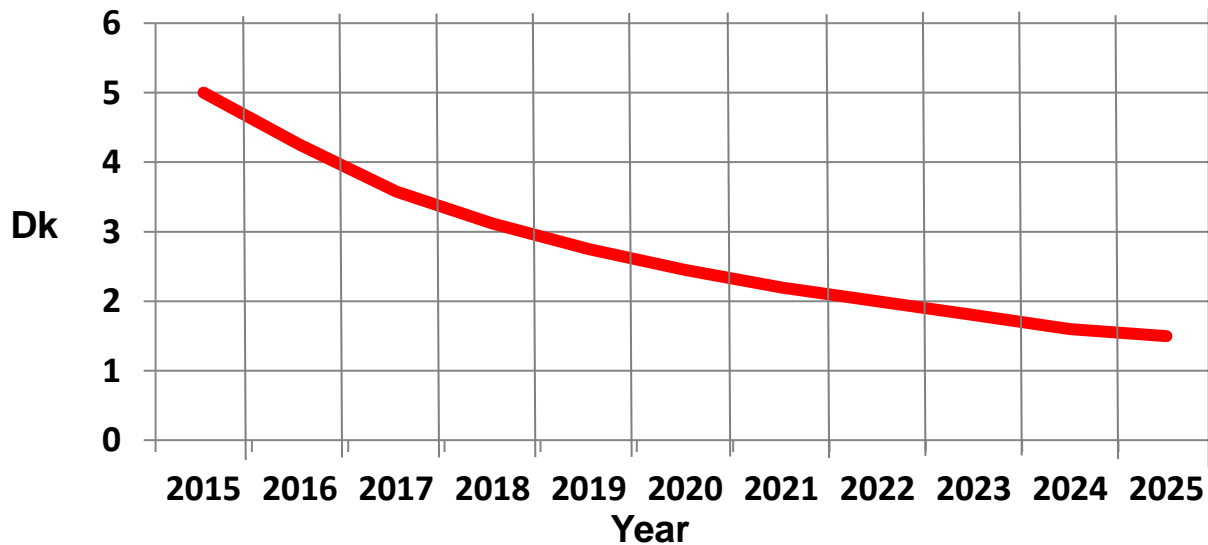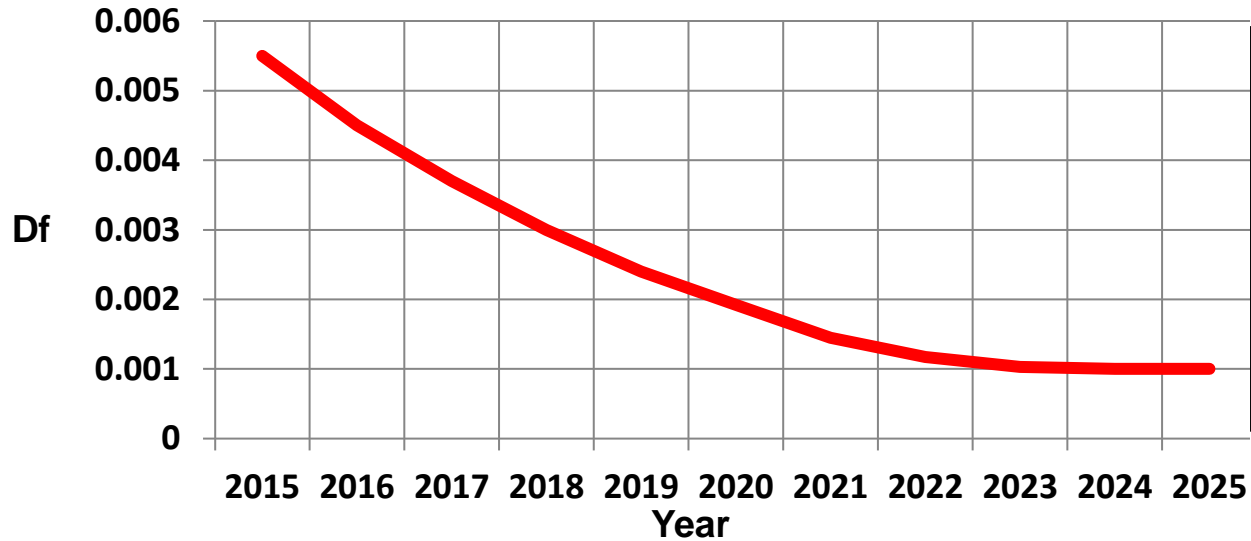
Bumpless Cu-Cu Hybrid Bonding

Key Process Steps (Fundamental) of Hybrid Bonding

Metal (Cu) recess = 3nm Plasma surface Activation (a)

Silicon
BEOL
Metal | Oxide | Metal

Oxide
Metal | Metal
BEOL
Silicon

Oxide to Oxide Initial Bond at Room Temperature (b)

Silicon
BEOL
Metal | Oxide | Metal
Metal | Oxide | Metal
BEOL
Silicon
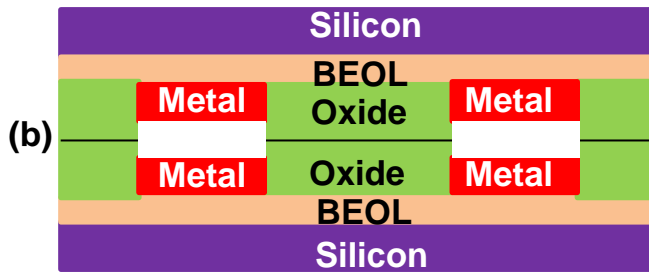
Heating Closes Dishing Gap (Metal CTE > Oxide CTE) (Optional) (c)

Silicon
BEOL
Metal | Oxide | Metal
Metal | Oxide | Metal
BEOL
Silicon
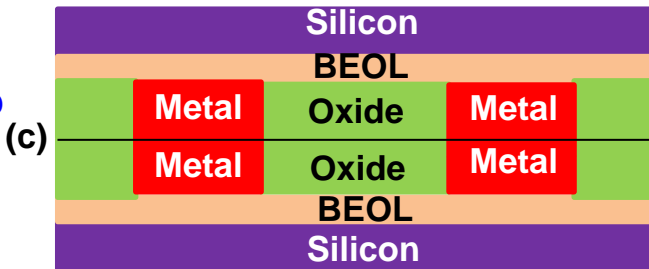
Annealing (300°C for 0.5h) w/o External Pressure (d)

Silicon
BEOL
BEOL
Silicon

The challenges (opportunities) of CoW hybrid bonding are:

- ➢ **CMP for metal recess, clean, and flat surface.**
- ➢ **the edge effects;**
- ➢ **contaminants;**
- ➢ **particles due to singulation;**
- ➢ **the requirement of higher accuracy pick and place machines;**
- ➢ **slightly larger pads to compensate the pick and place tolerance.**
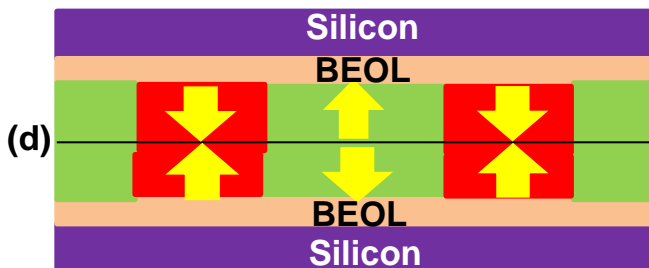
Sony's CMOS image sensor made by hybrid bonding

Processor Chip

BI-CIS Chip

Wirebonds

Processor Chip

Wirebonds

Microlens

BI-CIS Chip

SiO$_2$-SiO$_2$

Cu-Cu

Processor Chip

3µm

6µm

CMOS Image Sensor (CIS)

Pixels

Logic

Image Signal Processor (ISP)

CIS

SiO$_2$-SiO$_2$

Cu-Cu

Bonding Interface

ISP

Other Hybrid Bonding

FOVEROS Direct

CHIP

Bumpless

10μm pitch
hybrid bonding
10,000 pads/mm²

Intel

SoIC

SOC — Bond formation

SOC-1 / SOC-2 — SoIC stacking **(Hybrid Bonding)**

Underfill

SOC-1 / SOC-2 — RDL (optional)

TSMC

GRAPHCORE + tsmc

C4 (Bump) · C4 (Bump) · C4 (Bump) · C4 (Bump) · C4 (Bump) · C4 (Bump) · C4 (Bump)

UBM

DTC · BTSV · DTC · BTSV · DTC · BTSV · DTC · BTSV · DTC

BEOL

BEOL

Colossus Die

Bumpless Cu pads for hybrid bonding

RYZEN 9 5900X
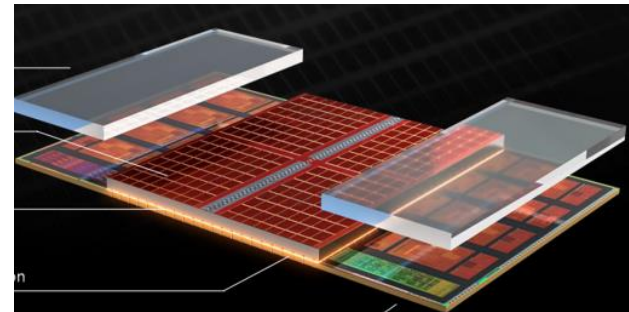
AMD/TSMC

Summary and Trends

➢ **Advanced packaging has been defined, and the kinds of advanced packaging have been ranked according to their interconnect density and electrical performance and grouped into 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration.**

➢ **The 2D IC integration, such as SiP, is and still will be used the most.**

➢ **The challenge of 2.1D IC integration (with thin film layers on build-up package substrate) is (warpage) manufacturing yield.**

➢ **The 2.3D IC integration is creeping into production.**

➢ **For extreme high-performance and high-density applications, 2.5D IC integration is the solution.**

➢ **The 3D IC integration are already in volume production for mobile processors, and they will be used for more different kinds of products.**

➢ **Fan-outs, such as chip-first (face-down) and chip-first (face-up), have been in HVM for consuming products. Chip-first (face-down) is and will still be used the most. Chip-last or RDL-first is not in HVM yet but it will be soon.**

Summary and Trends

➢ More than **75%** of the flip-chip applications are with C4 bumps mass reflowed on organic package substrates and CUF (capillary underfill) (SiP).

➢ **TCB** (thermocompression bonding) of C2 bumps with small-force and CUF is getting traction because of the interest in using thin chips and thin organic substrates.

➢ No more than **25%** of the flip-chip applications are for silicon-to-silicon, such as CoC, CoW, and WoW.

➢ Roadmaps of **Df** and **Dk** for low-loss dielectric materials of advanced packaging have been provided.

➢ The **TSV-interposer integration** platform for **PIC** and **EIC** of high-speed and high-bandwidth applications is getting lots of tractions. A couple of examples have been provided.

➢ A heterogeneous integration of **AiP** and **baseband chipset** with heat spreader/sink by chip-first with die face-down packaging for high performance and compact 5G millimeter wave system integration has been proposed.

Summary and Trends

➢ **SoCs with finer feature sizes are and will be here to stay. Chiplets design and heterogeneous integration packaging provide alternatives to SoCs, especially for advanced nodes.**

➢ **The key advantages of chiplets heterogeneous integration are:**
  ➢ **(1) yield improvement (lower cost) during manufacturing,**
  ➢ **(2) time-to-market,**
  ➢ **(3) cost reduction during design,**
  ➢ **(4) better thermal performance,**
  ➢ **(5) reusable of IP,**
  ➢ **(6) modularization.**

➢ **The key disadvantages are:**
  ➢ **(1) additional area for interfaces,**
  ➢ **(2) higher packaging costs,**
  ➢ **(3) more complexity and design effort,**
  ➢ **(4) past methodologies are less suitable for chiplets.**

Summary and Trends

➤ **Bridge technology** such as **EMIB** for chiplets' horizontal communication in **organic substrate** has been in production. Recently, there are many publications on **bridges embedded in EMC.**

➤ More than **75%** of heterogeneous integration are on organic substrate (**SiP** by **SMT** and **flip chip on board**) and no more than **25%** are on other substrates.

➤ **Hybrid bonding** can be applied to extremely fine pitch (as low as **4μm**) pads and used for very high-density and high-performance applications.

➤ Hybrid bonding is only suitable for **silicon-to-silicon** assembly such as CoC, CoW, and WoW.
   ➤ Because of the throughput issue, **CoC** bonding will not be popular.
   ➤ Because of the chip-size and yield issues, **WoW** bonding is limited even it will be used more than today.
   ➤ Because of the flexibility, **CoW** will be the mainstream.

120

Some Recent Advanced Packaging Publications by the Lecturer and his Colleagues

1. Lau, J. H., "Recent Advances and Trends in Advanced Packaging", *IEEE Transactions on CPMT*, Vol. 12, No. 2, February 2022, pp. 228-252.
2. Lau, J. H., G. Chen, J. Huang, et al., "Hybrid Substrate by Fan-Out RDL-First Panel-Level Packaging, *IEEE Transactions on CPMT*, Vol. 11, No. 8, August 2021, pp. 1301-1309.
3. Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", *ASME Transactions, Journal of Electronic Packaging*, Vol. 143, June 2021, pp. 1-36.
4. Lau, J. H., C. Ko, C. Lin, et al., "Fan-Out Panel-Level Packaging of Mini-LED RGB Display", *IEEE Transactions on CPMT*, Vol. 11, No. 5, May 2021, pp. 739-747.
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Thank You Very Much for Your Attention!