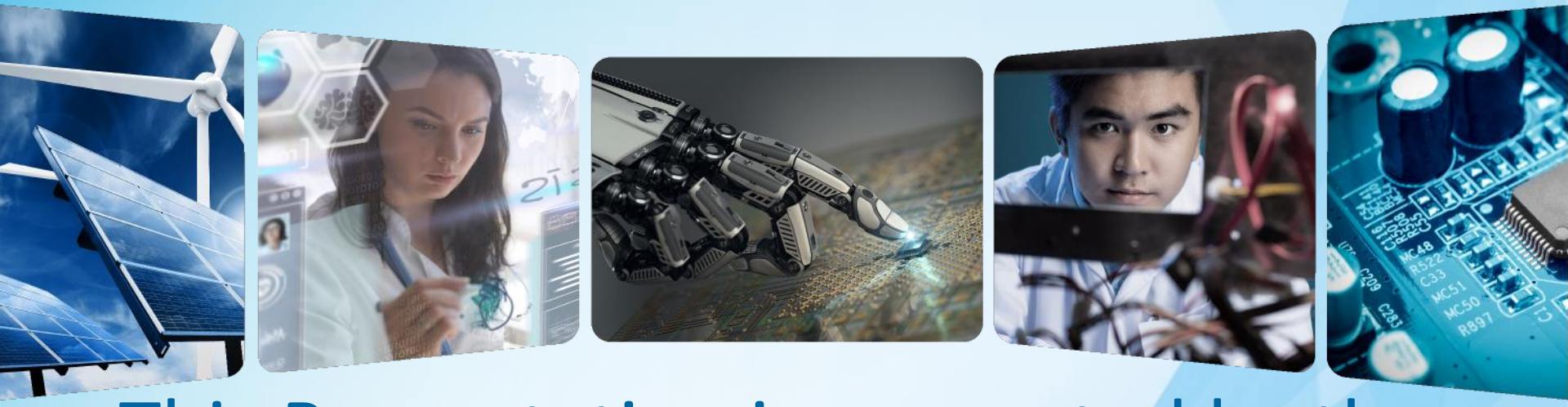
Recent Advances and Trends in Advanced Packaging

John H Lau
Unimicron Technology Corporation
john_lau@unimicron.com
IEEE EPS Binghamton Chapter, April 13, 2022



This Presentation is supported by the IEEE Electronics Packaging Society's Distinguished Lecturer Program

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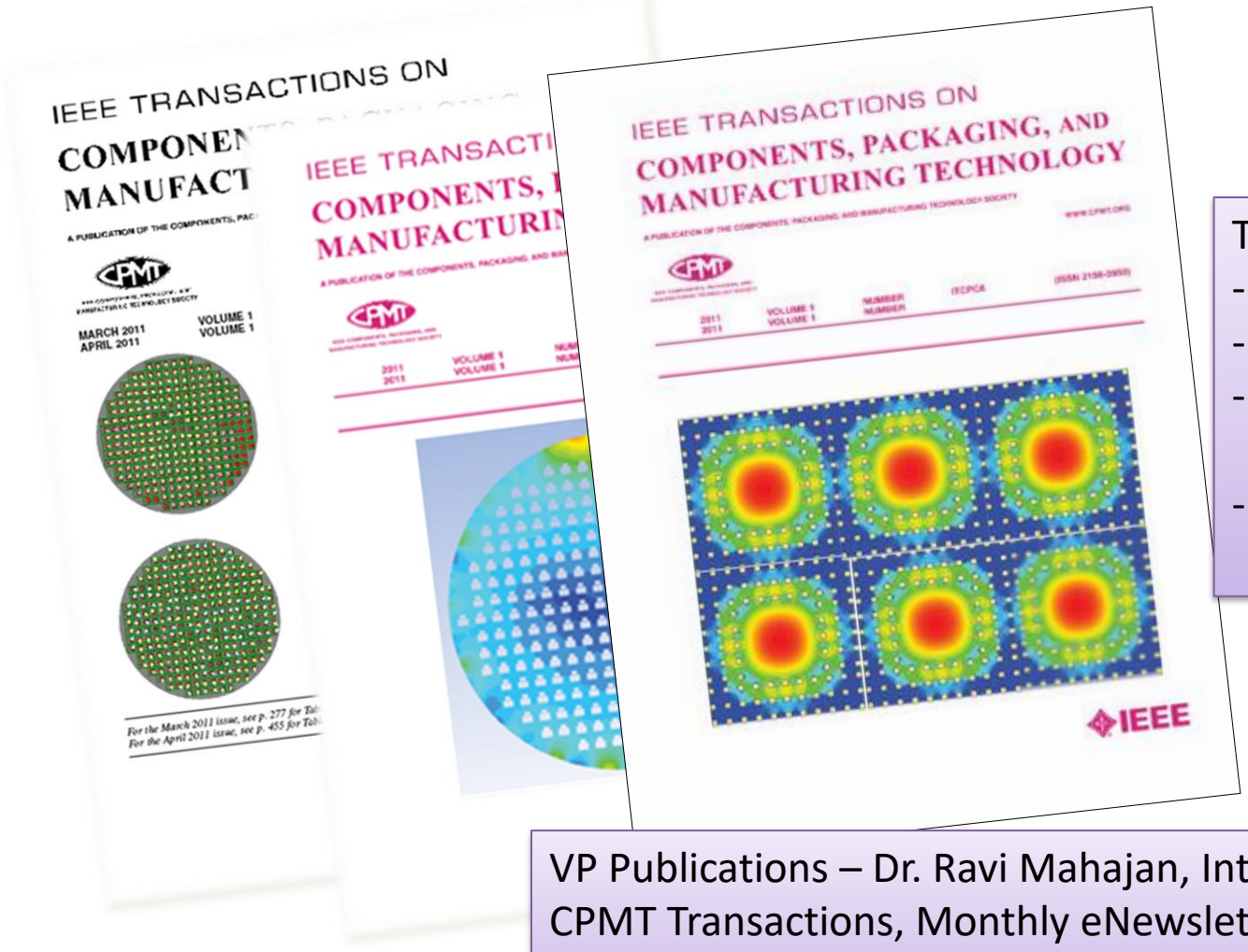
Peer-Reviewed Technical Publication



Transactions on CPMT
- 595 submissions (2020)
- 240 papers published
- Impact Factor: ~ 1.7 (2020)
- Xplore Usage: 40,000+

VP Publications – Dr. Ravi Mahajan, Intel
CPMT Transactions, Monthly eNewsletter, and Bi-Annual printed Newsletter

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IEEE Electronics Packaging Award

(IEEE Technical Field Award)

Outstanding Sustained Technical Contribution Award

Electronics Manufacturing Technology

David Feldman Outstanding Contribution

Exceptional Technical Achievement

Outstanding Young Engineer

Transactions Best Papers

Regional Contributions

PhD Fellowship

IEEE ELECTRONICS PACKAGING SOCIETY

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  - 2.1D IC Integration
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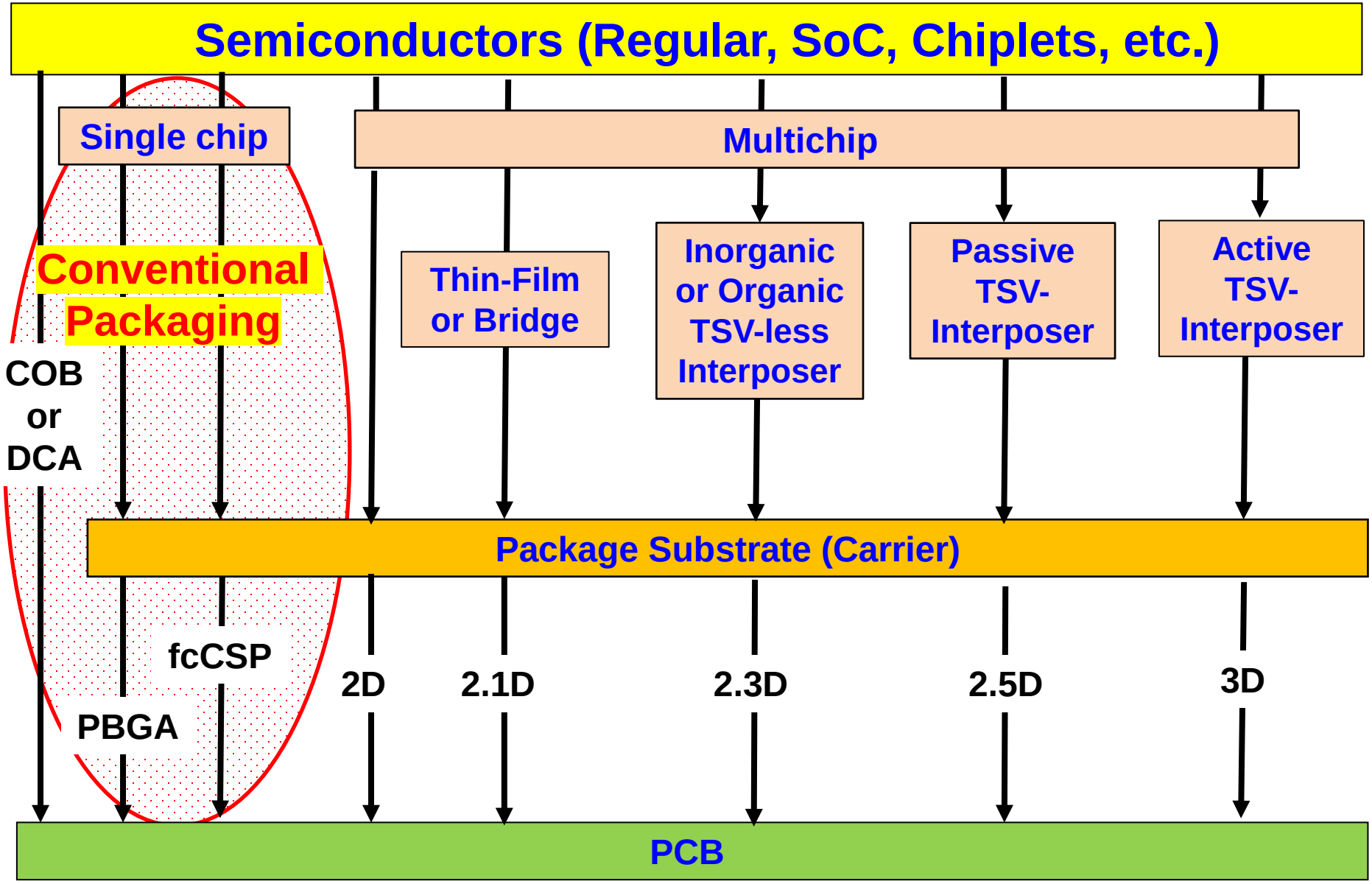
  - 2.5D IC Integration
  - 3D IC Integration
- Chiplet Design and Heterogeneous Integration (HI) Packaging
  - Chip partition and integration
  - Chip split and integration
  - Multiple System and Integration
  - HI on Organic Substrates (SiP)
  - HI on Silicon Substrates (Passive/Active TSV-Interposers)
  - Lateral Communication between Chiplets (e.g., Bridges)
  - HI on Fan-Out (Chip-First) RDL-Substrates/Interposers
  - HI on Fan-Out (Chip-Last) RDL-Substrates/Interposers
  - HI on Ceramic Substrates
- Summary
- Q&A

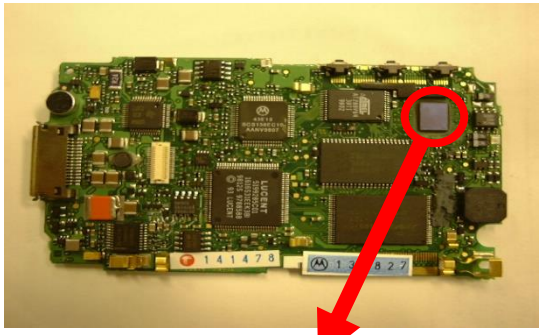
The Biggest Difference between Chiplet and Heterogeneous Integration:

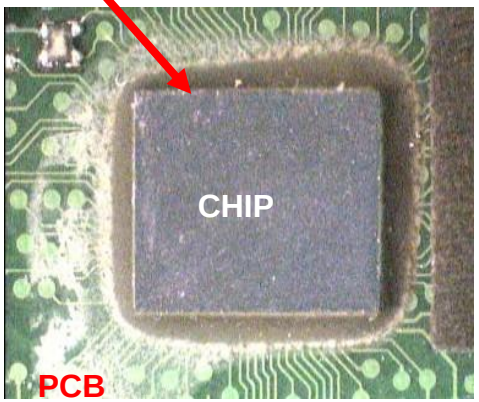
- **Chiplet is a Chip Design Method**
- **Heterogeneous Integration is a Chip Packaging Method**

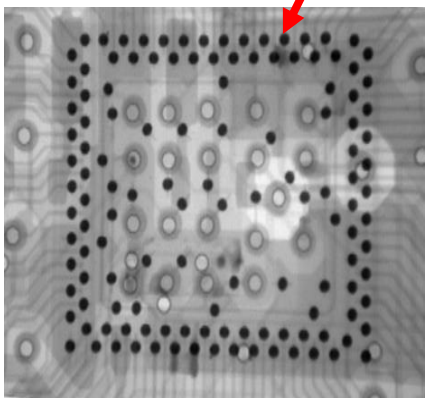
Semiconductor Packaging Technologies



Conventional Packaging: Direct Chip Attach (DCA) and Flip Chip Ball Grid Array (fcBGA)

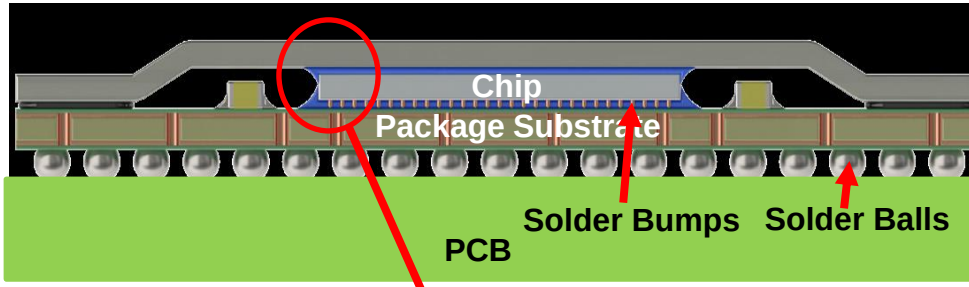


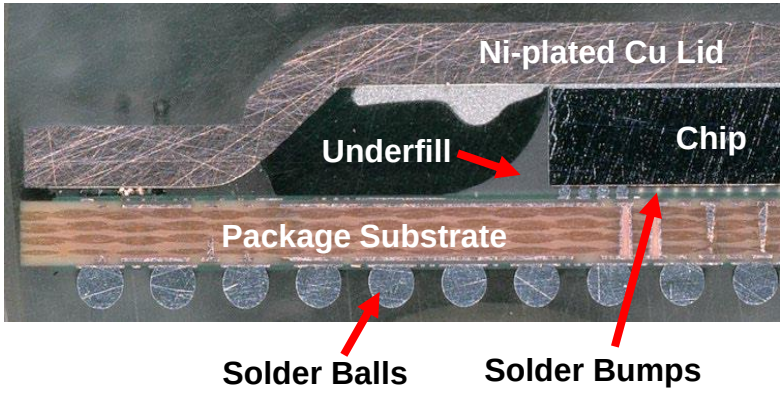




X-ray showing solder joints

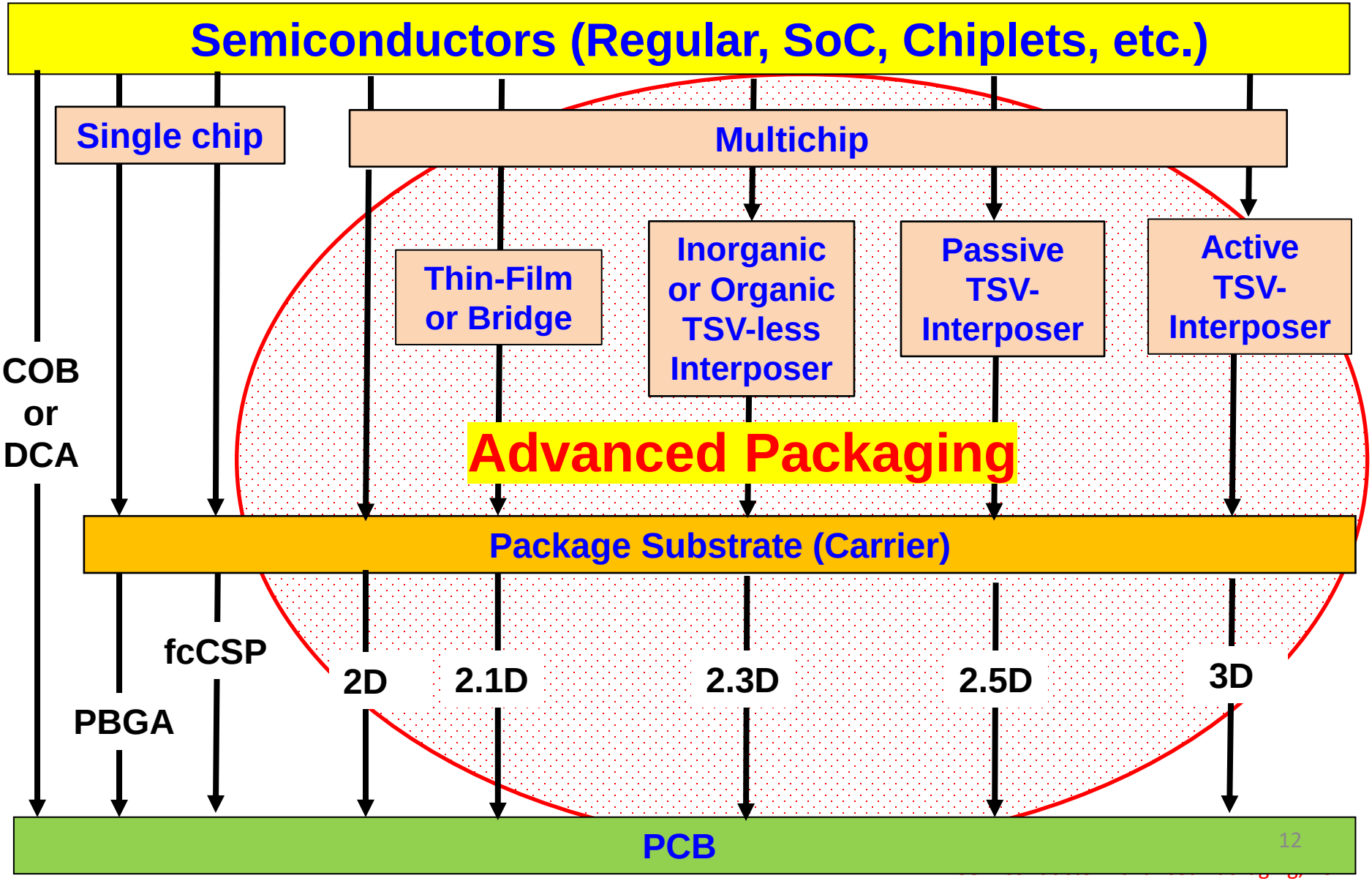
DCA



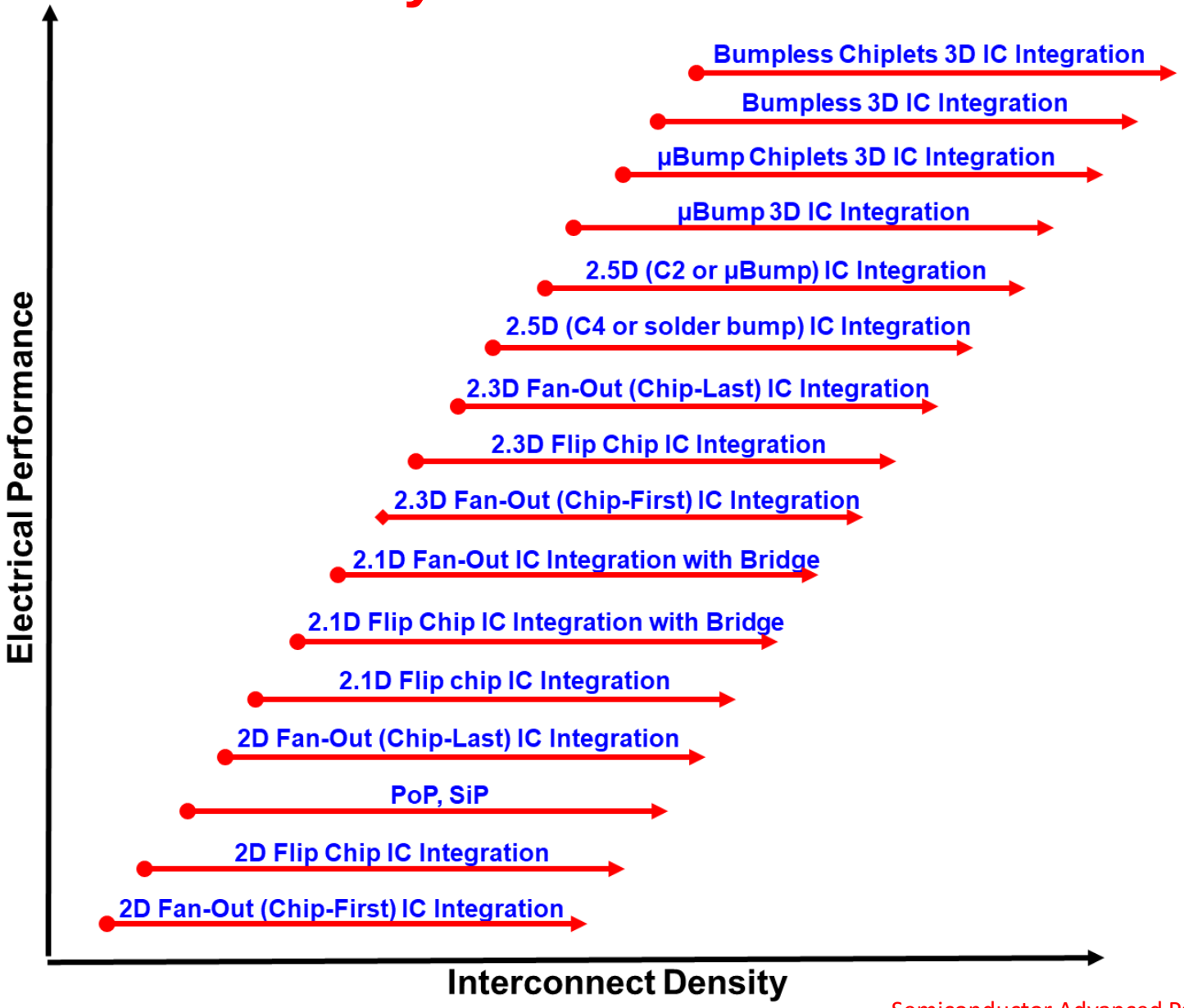


fcBGA

Groups of Advanced Packaging: 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration



Advanced Packaging Ranking According to Their Density and Performance



Semiconductor Advanced Packaging, 2021

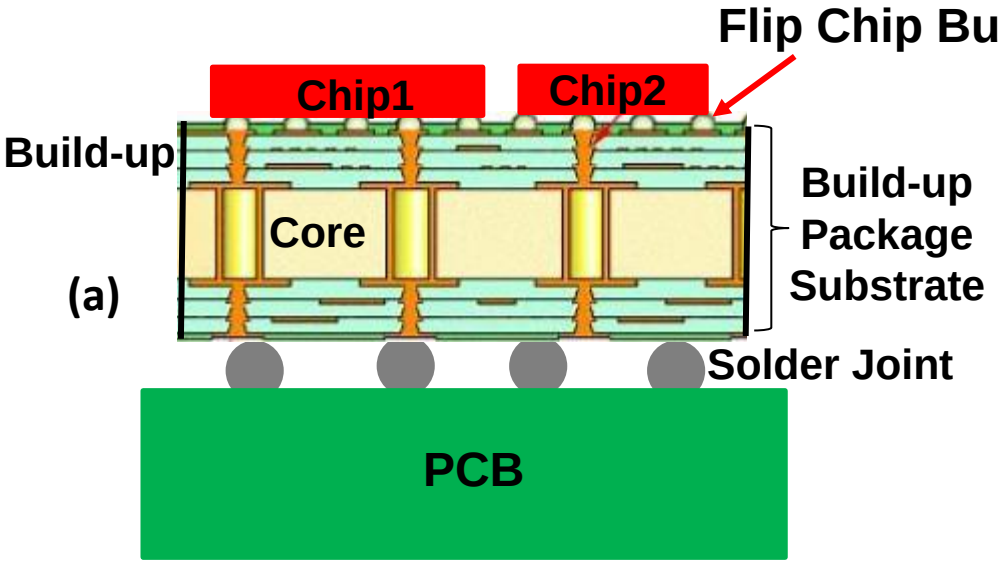
Advanced Packaging

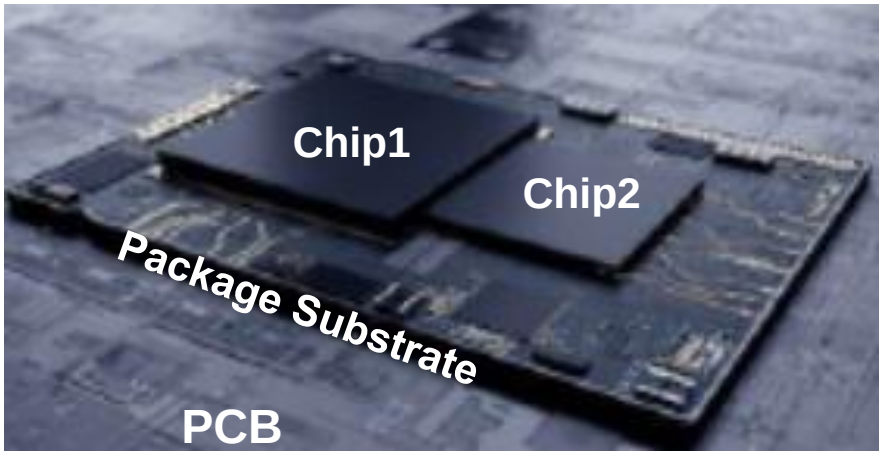
- 2D IC Integration
- 2.1D IC Integration
- 2.3D IC Integration
- 2.5D IC Integration
- 3D IC Integration

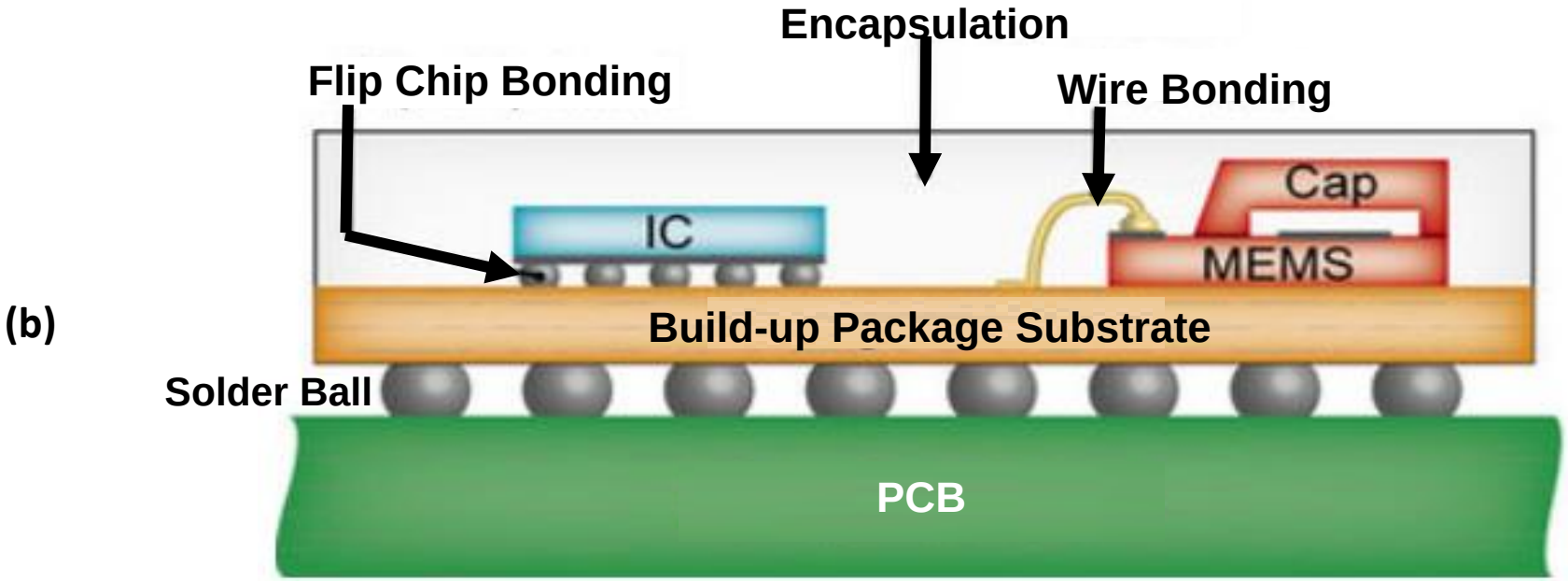
2D IC Integration

- 2D (Flip Chip) IC Integration
- 2D (Fan-Out) IC Integration
  - Chip-First die Face-Down
  - Chip-First die Face-Up
  - Chip-Last (RDL-First)

2D (Flip Chip / Wirebond) IC Integration



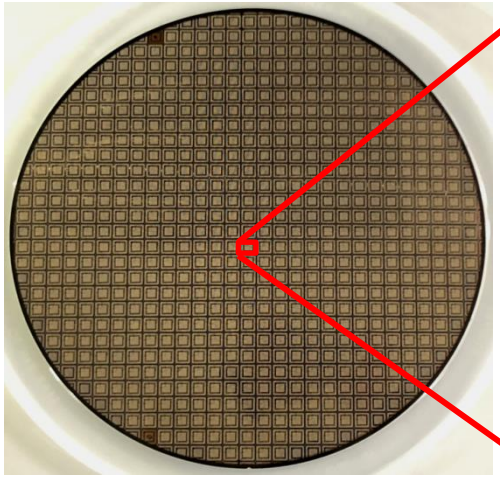




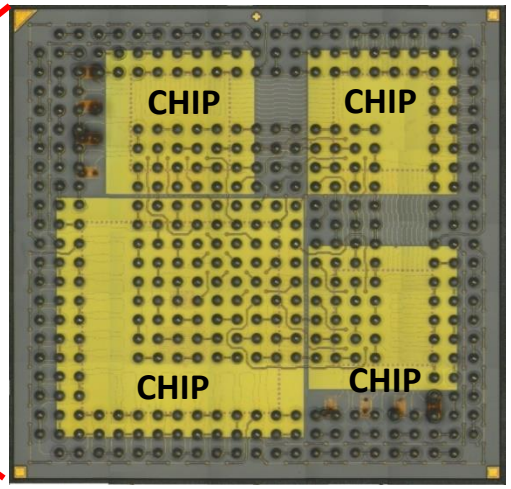
Semiconductor Advanced Packaging, 2021

2D (Fan-Out) IC Integration: Chip-First (Die Face-Down)

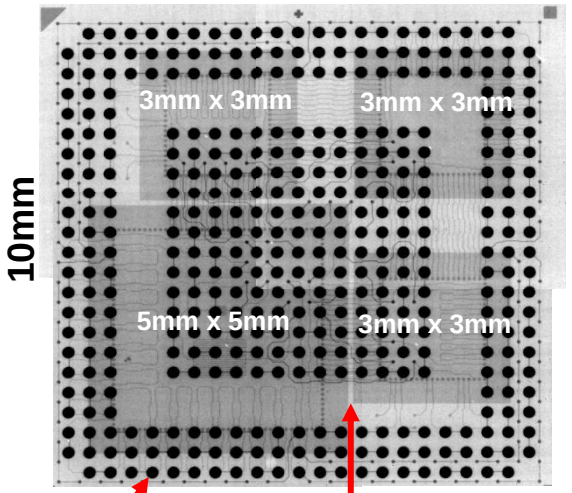
300mm reconstituted wafer



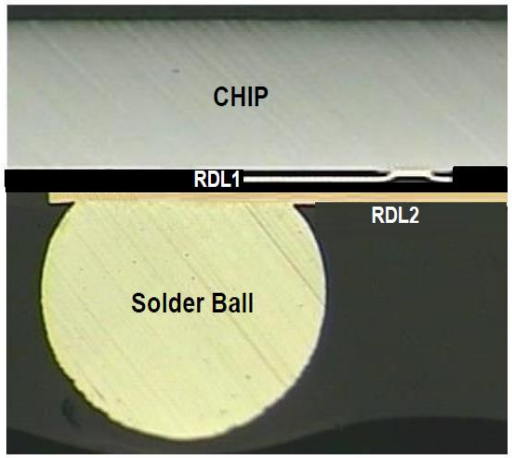
10mmx10mm SiP



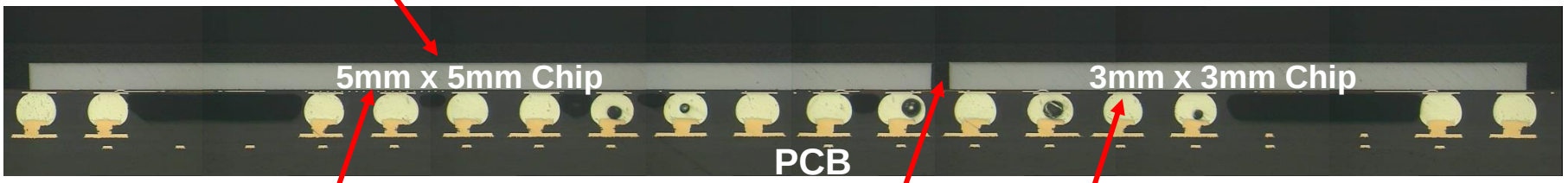
10mm



405 Solder Ball 100μm-Gap

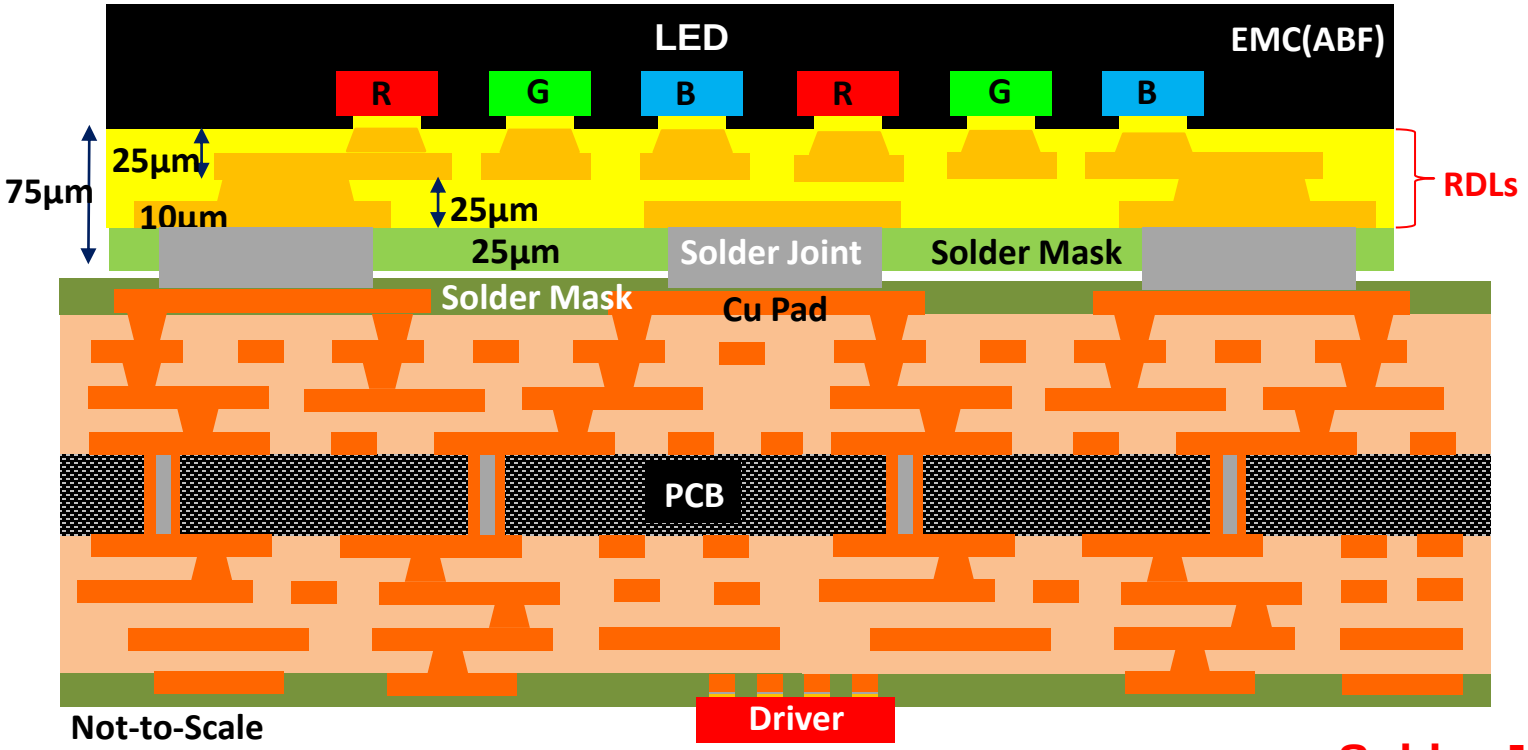


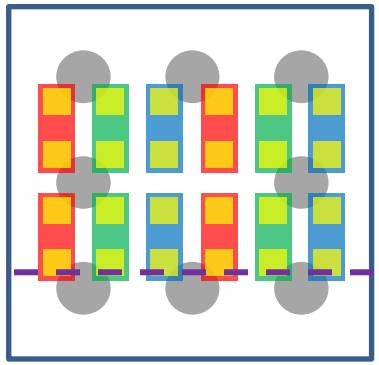
There is no substrate which is replaced by RDLs (redistributed-Layers)

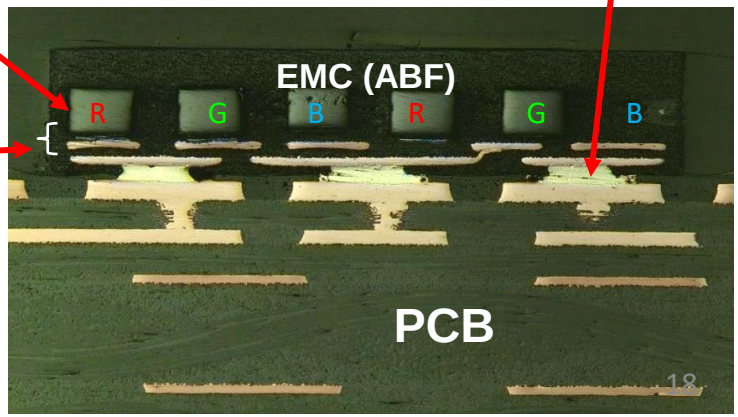


IEEE Trans. on CPMT, 2018

Heterogeneous Integration of Mini-LEDs for RGB-display (Chip-First Die Face-Down)

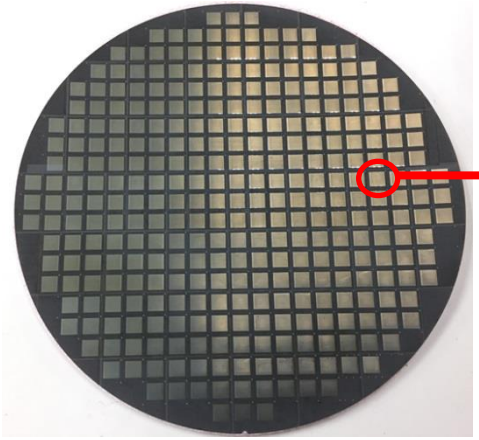




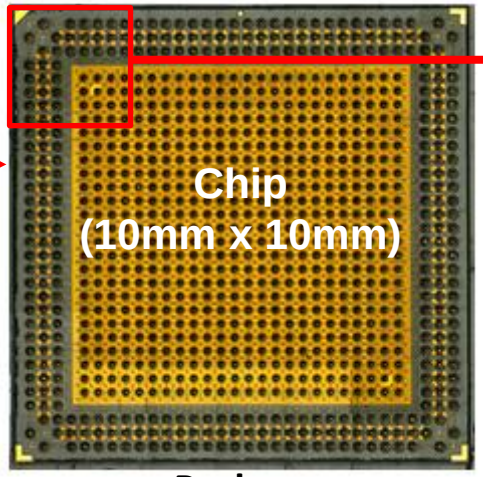


IEEE Trans. on CPMT, 2021

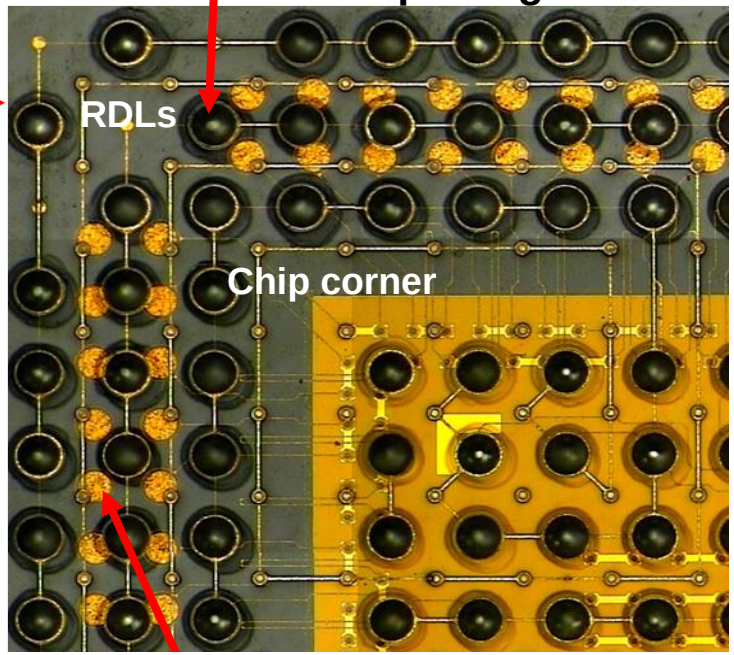
Fan-Out Chip-First (Die Face-Up)



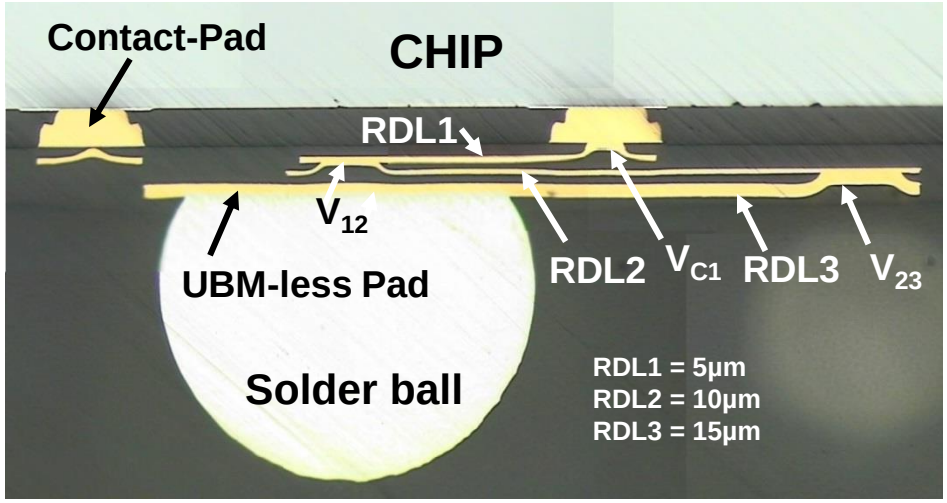
Reconstituted Wafer
(325 packages)

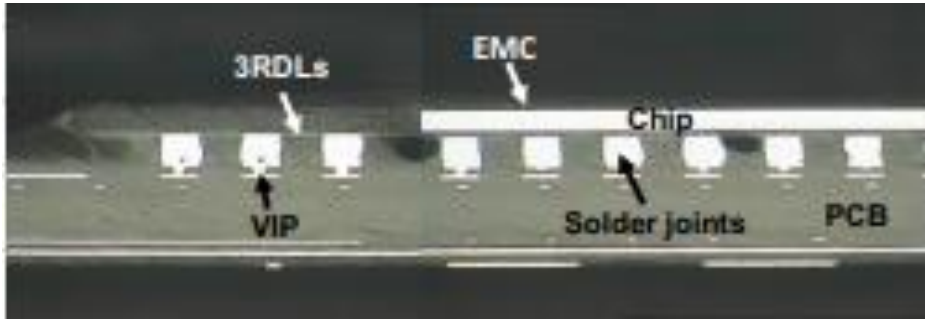


Package



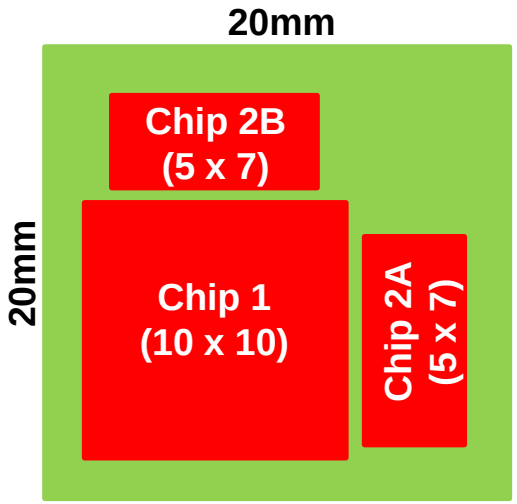
Pads on package for TMV

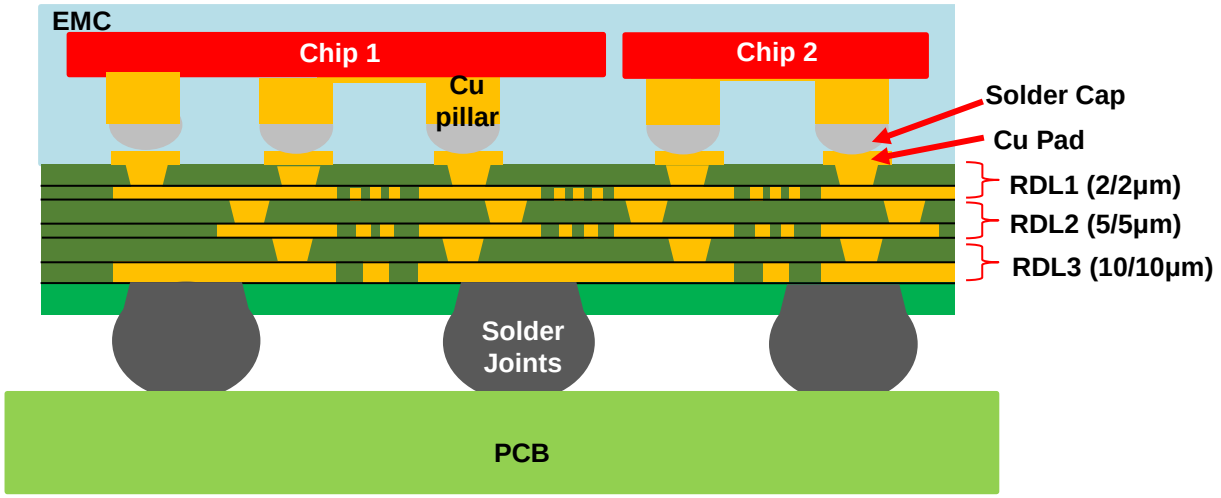


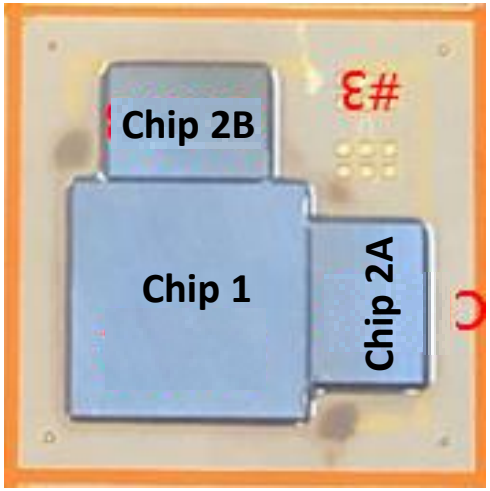


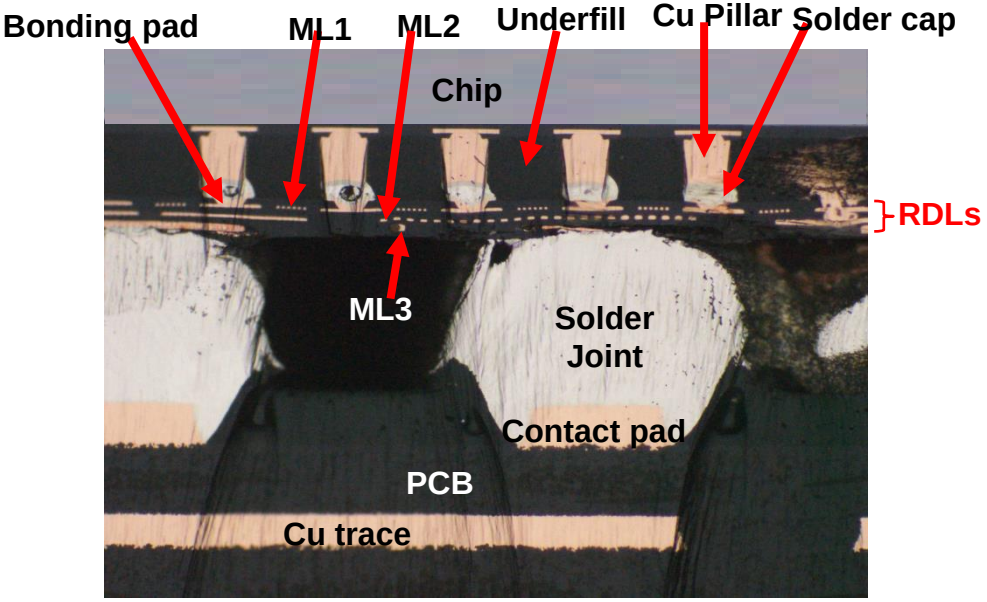
IEEE Trans., CPMT, JUN 2018

Chip-Last (RDL-First) Fan-Out Panel-Level Packaging





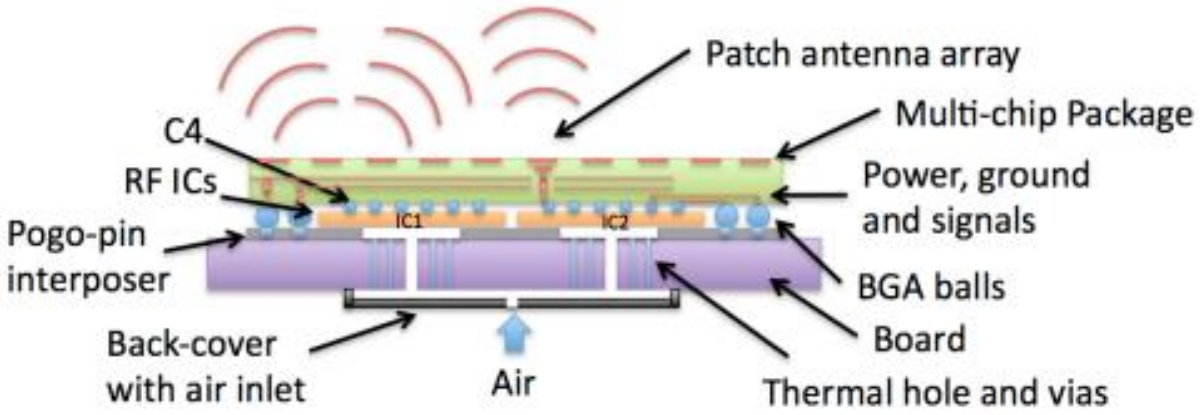




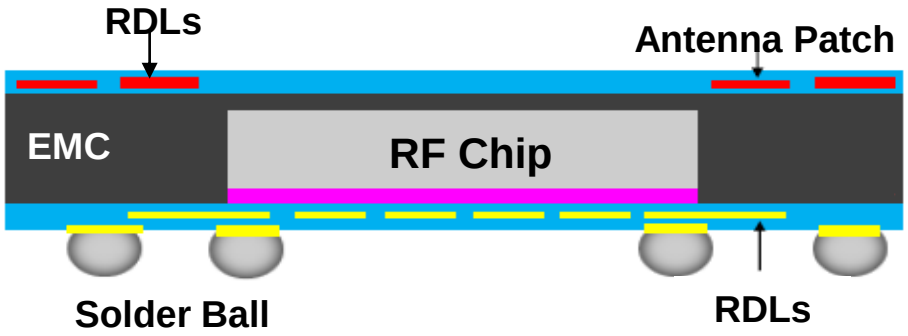
IEEE Trans. on CPMT, JUL 2020

Antenna-in-Packaging (AiP)

IBM (ECTC2014) RF Flip Chips on Organic Substrate with Patch Antenna Array



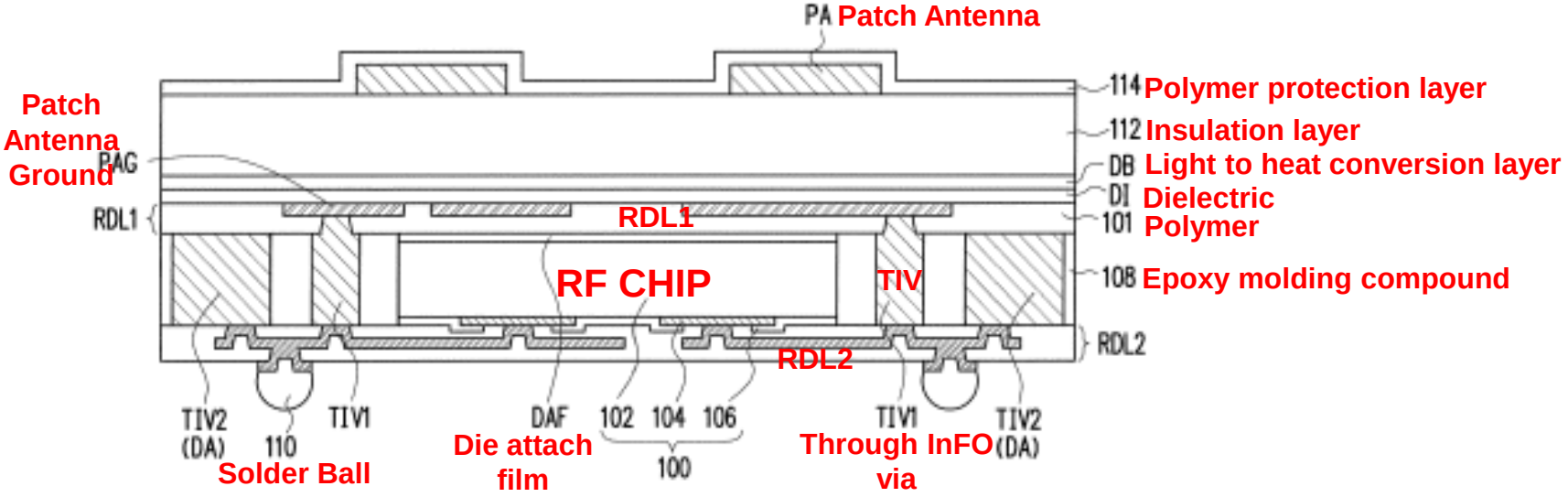
TSMC (ECTC2018) RF Flip Chips in Fan-Out EMC with Patch Antenna Array (InFO_AiP)



THE TRANSMISSION LOSS FOR RDL AND SUBSTRATE TRACE AT 28 AND 38GHZ

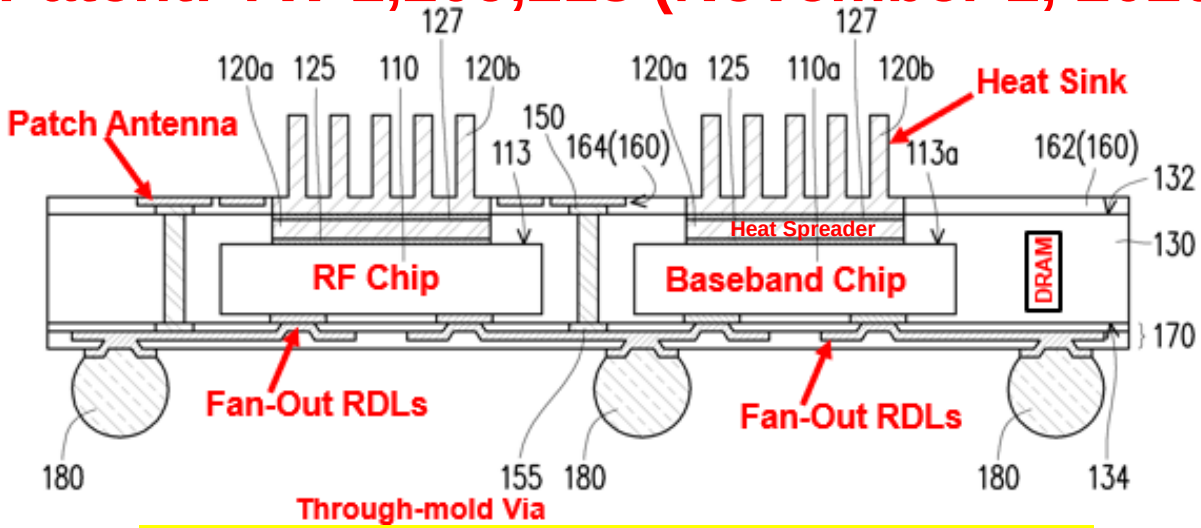
Frequency	InFO RDLs	Substrate Trace
28GHz	0.175dB/mm	0.288dB/mm
38GHz	0.225dB/mm	0.377dB/mm

TSMC's AiP Patent: US 10,312,112 (June 4, 2019)



Fan-Out chip-first die Face-Up Process

Unimicron's Heterogeneous Integration of Baseband and AiP Patent: TW 1,209,218 (November 1, 2020)

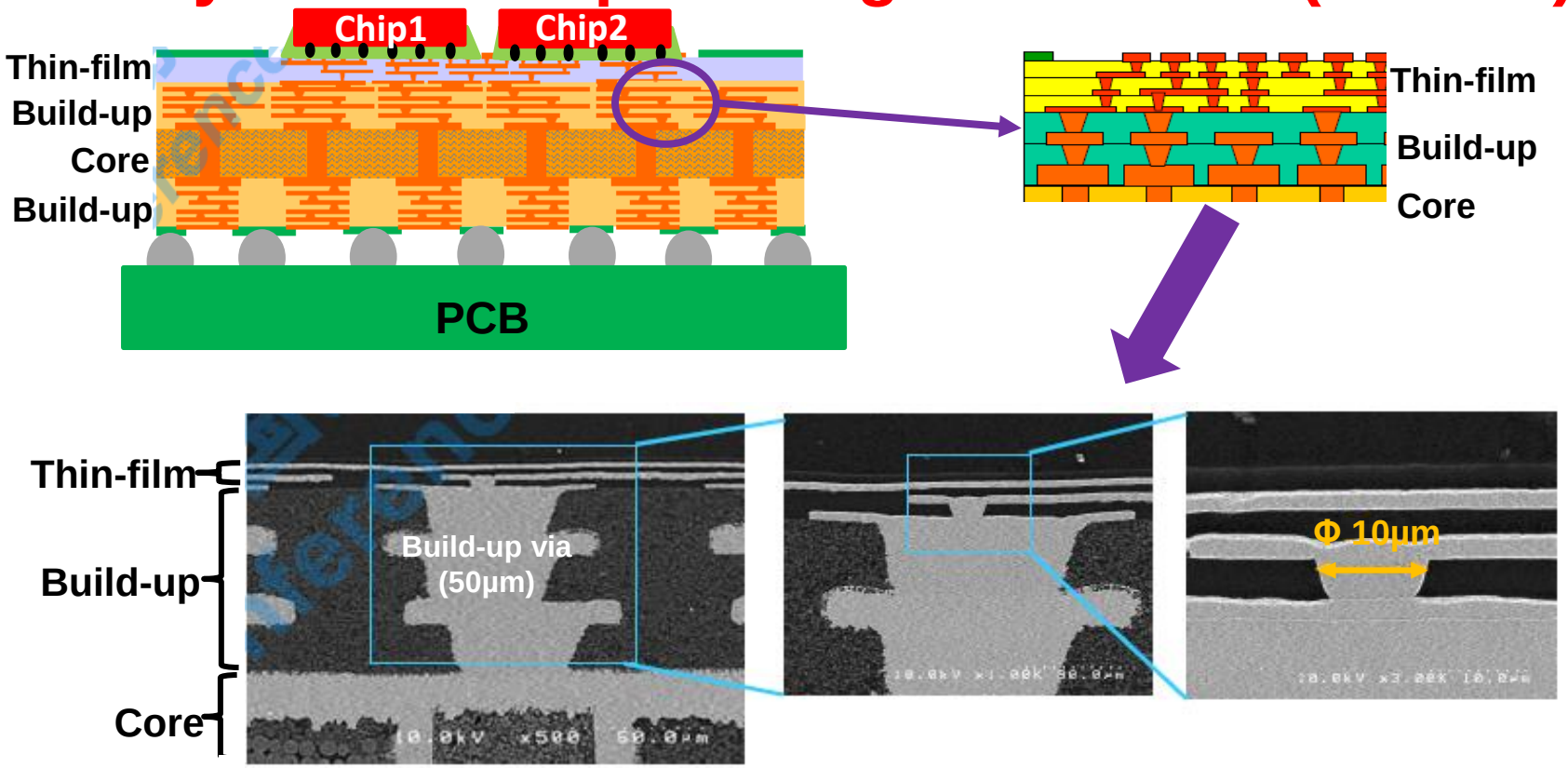


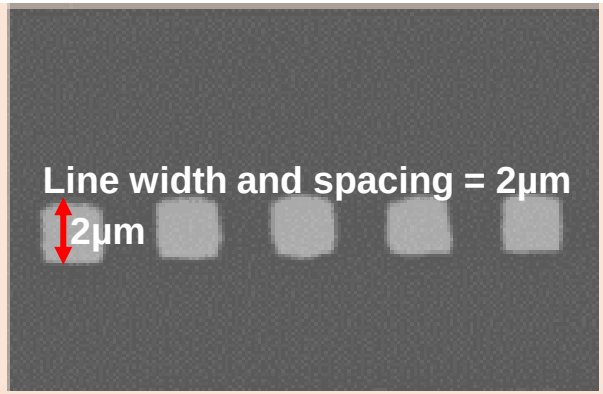
Fan-Out chip-first die Face-Down Process

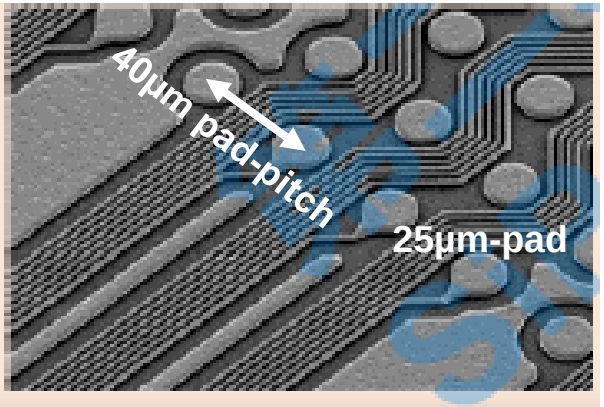
2.1D IC Integration

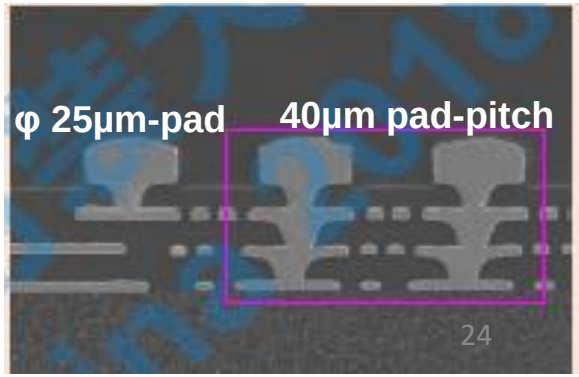
- **Shinko's integrated thin-film high-density organic package (i-THOP)**
- **JECT's ultra format organic substrate (uFOS)**

2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (Shinko)

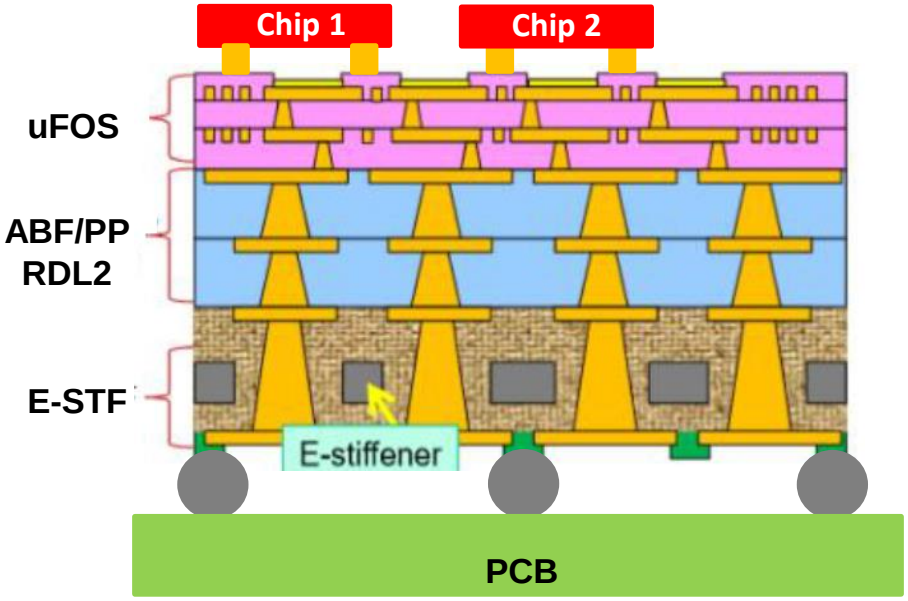


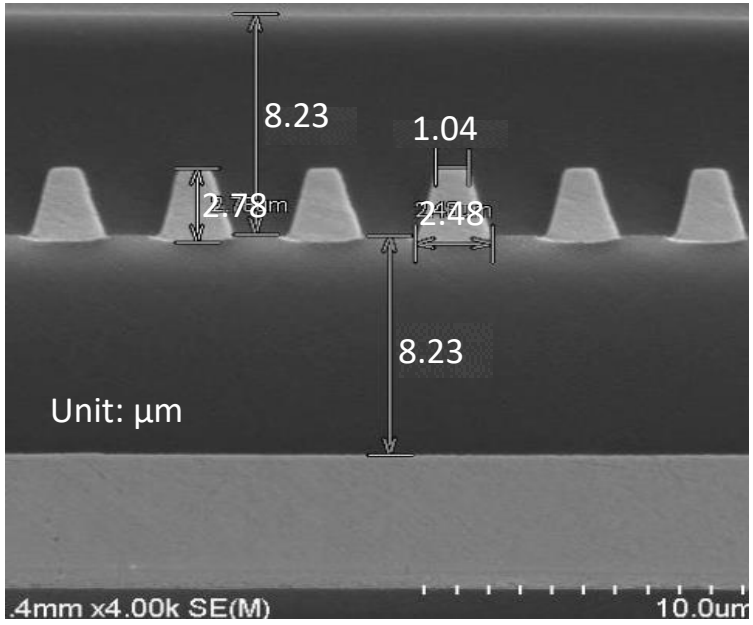


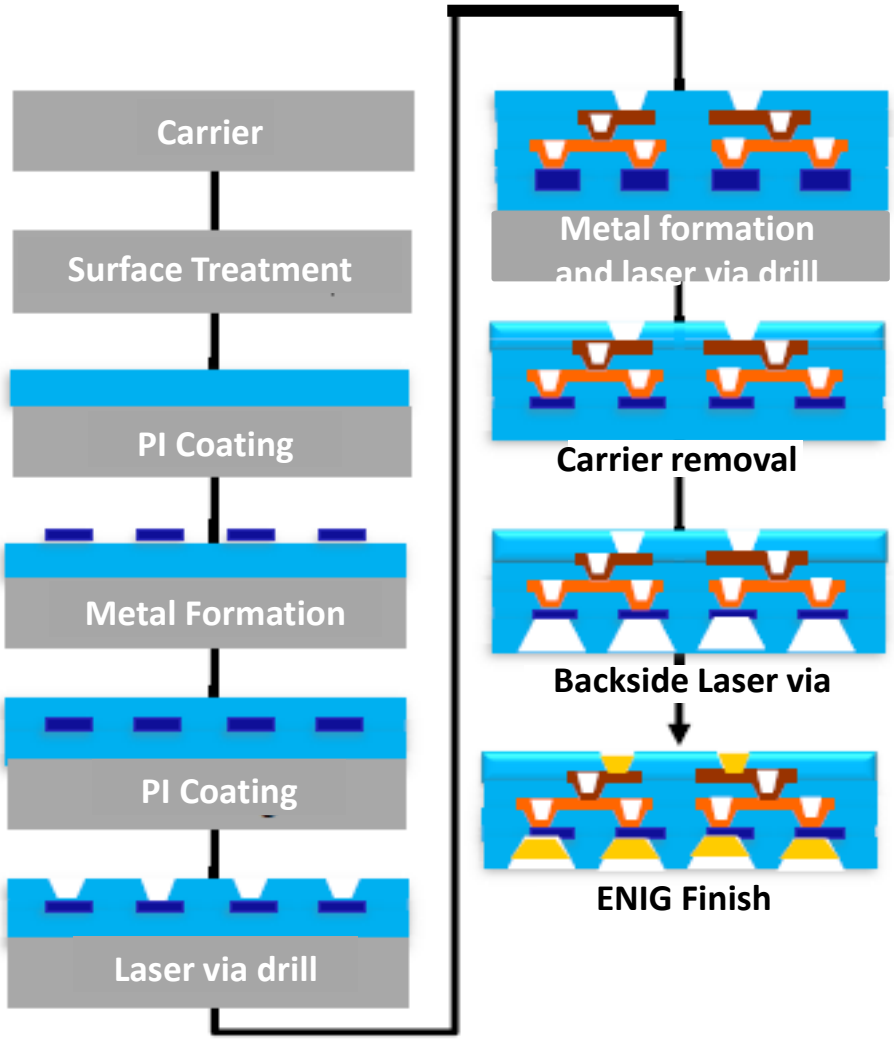




2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (JCET)





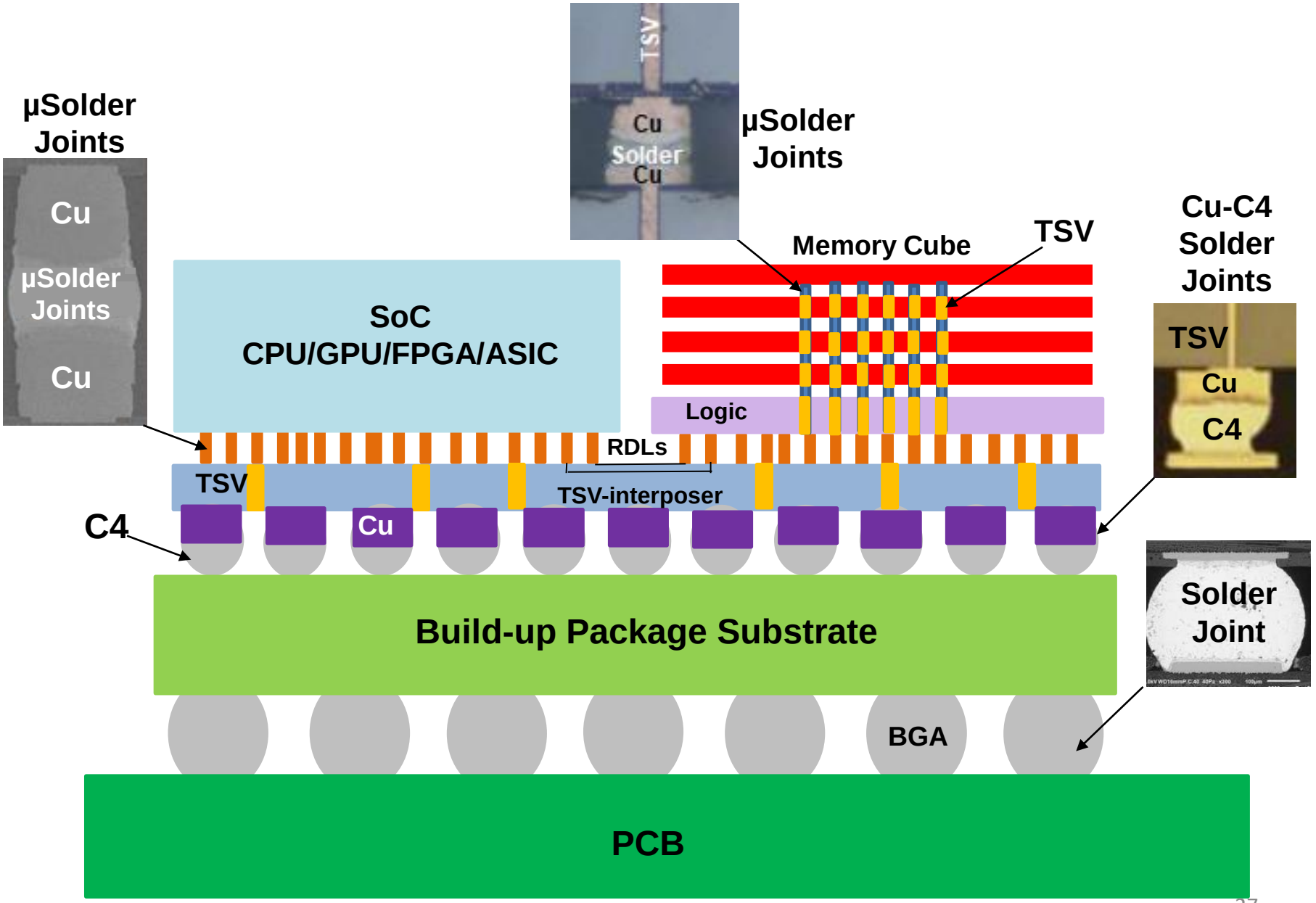


- uFOS (ultra format organic substrate)
- e-STF (embedded stiffness)

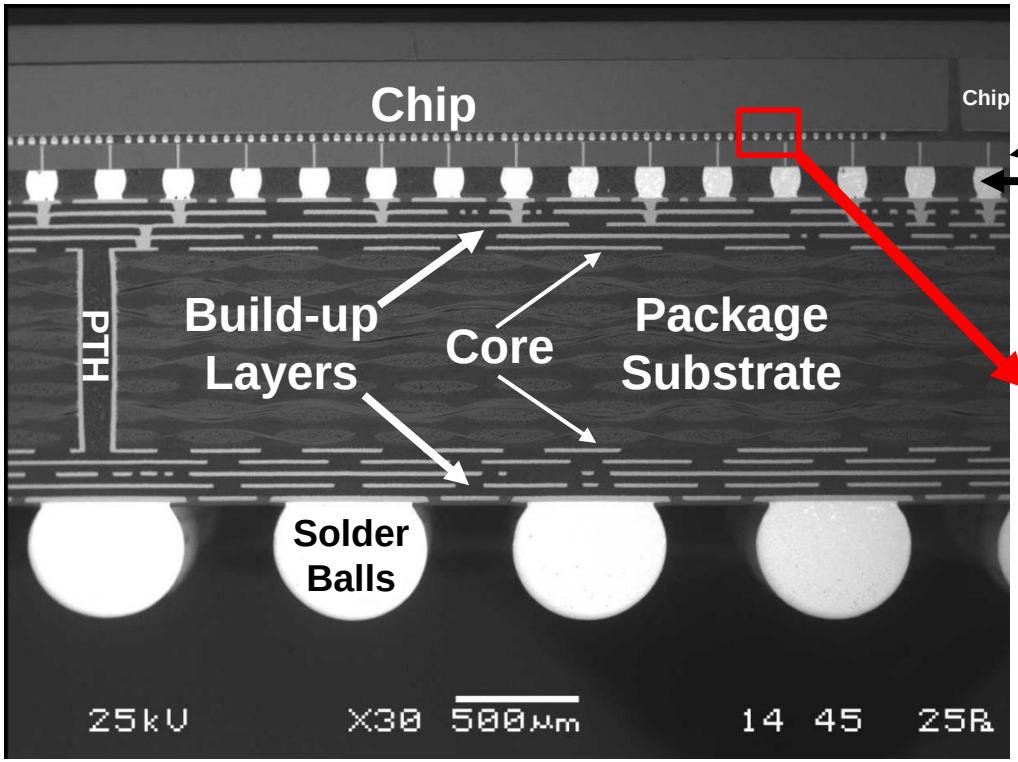
2.5D IC Integration

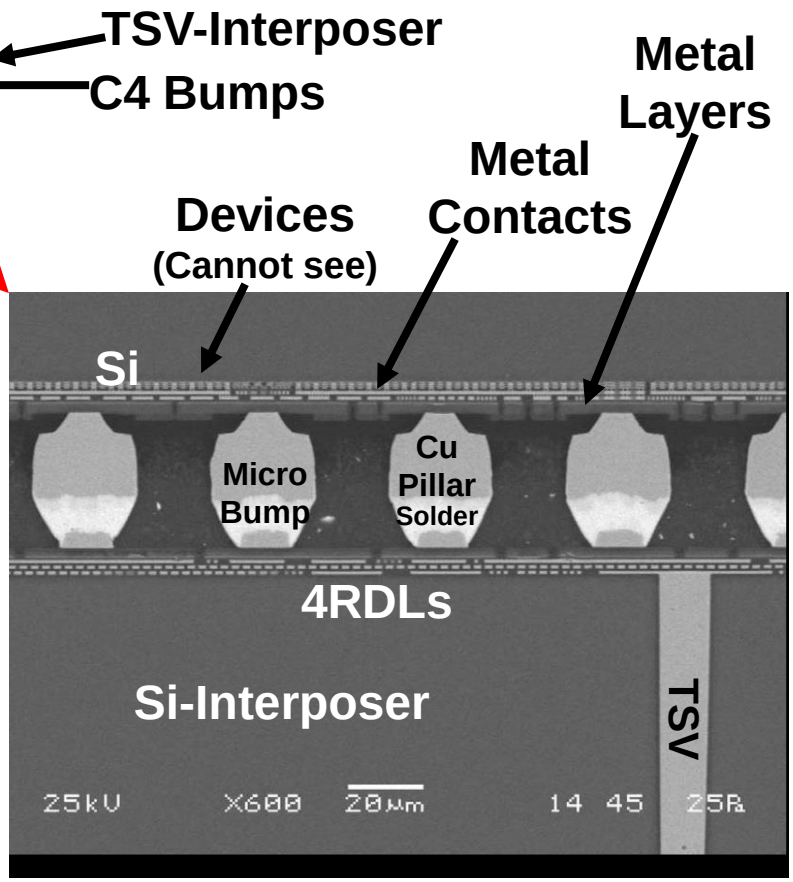
- **Examples: TSMC, Xilinx, AMD, Nvidia, Samsung**
- **TSV-less 2.5D by Samsung**
- **2.5D heterogeneous integration of PIC (photonic IC) and EIC (electronic IC)**

2.5D IC Integration



Xilinx/TSMC's 2.5D IC Integration with FPGA



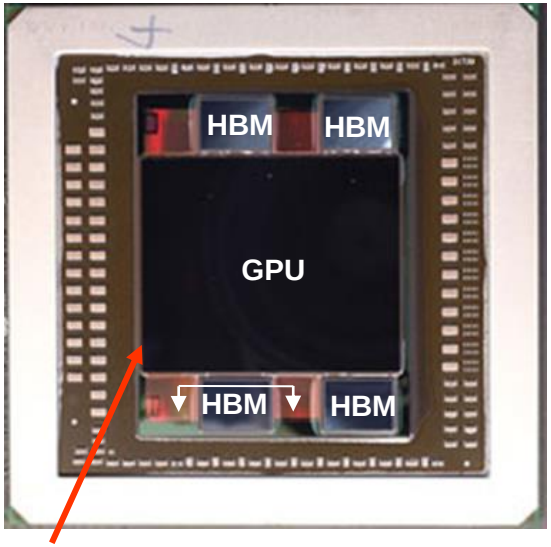


CoWoS
(chip on wafer on substrate)

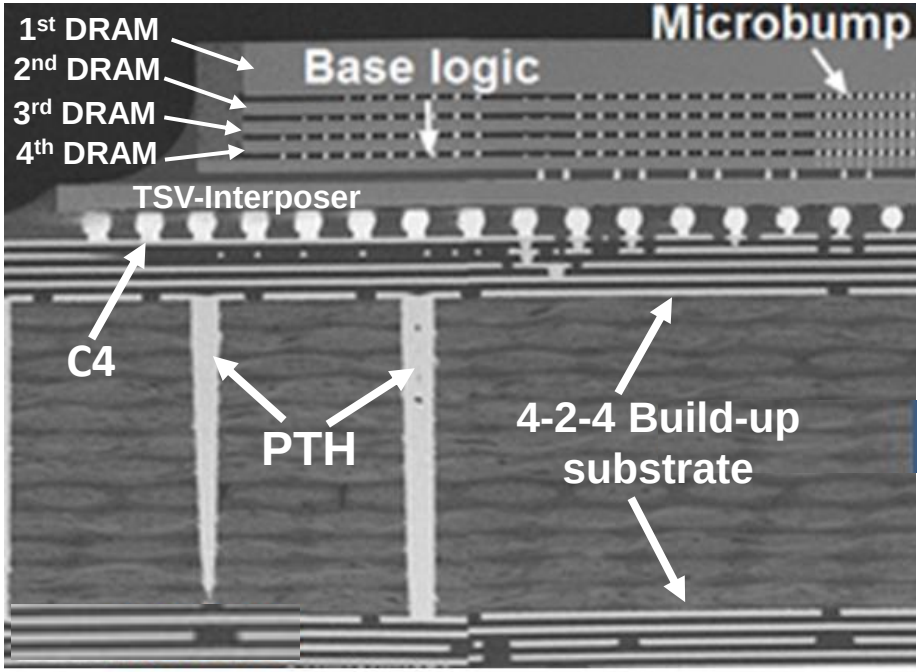
Homogeneous Integration on Si-substrate

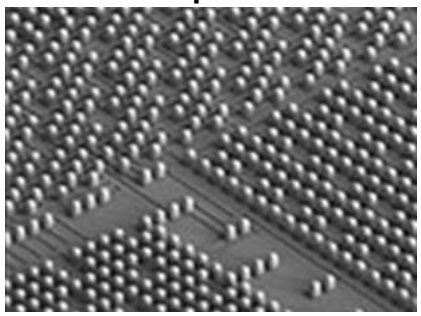
- RDLs: 0.4µm-pitch line width and spacing
- Each FPGA has >50,000 µbumps on 45µm pitch
- Interposer is supporting >200,000 µbumps

AMD's GPU (Fiji), Hynix's HBM, and UMC's Interposer

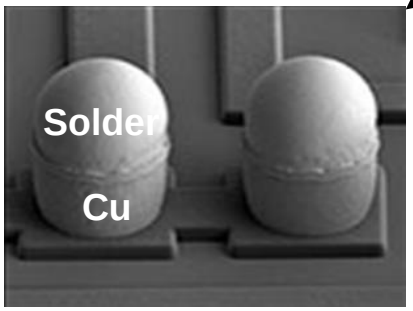


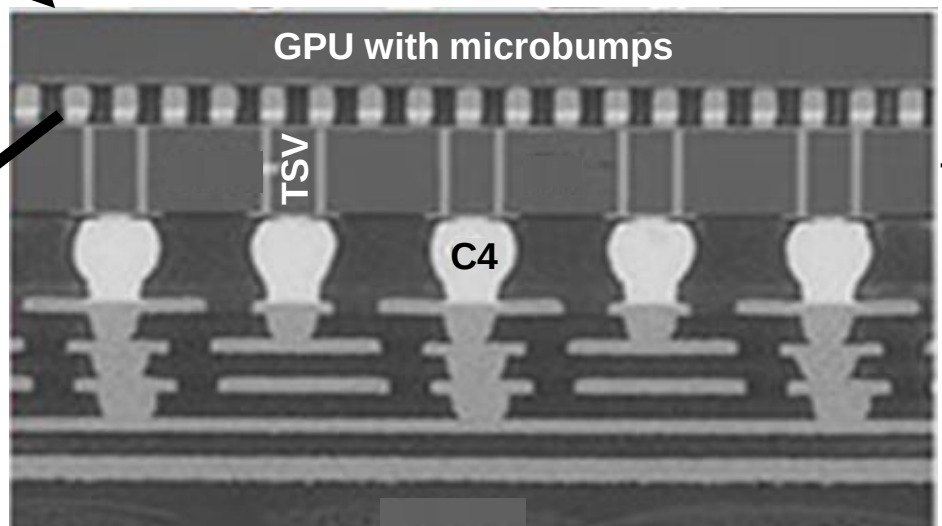
TSV-Interposer





Cu-Pillar with solder Cap

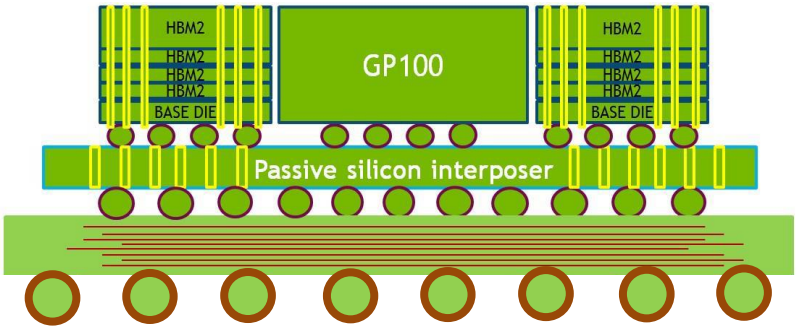


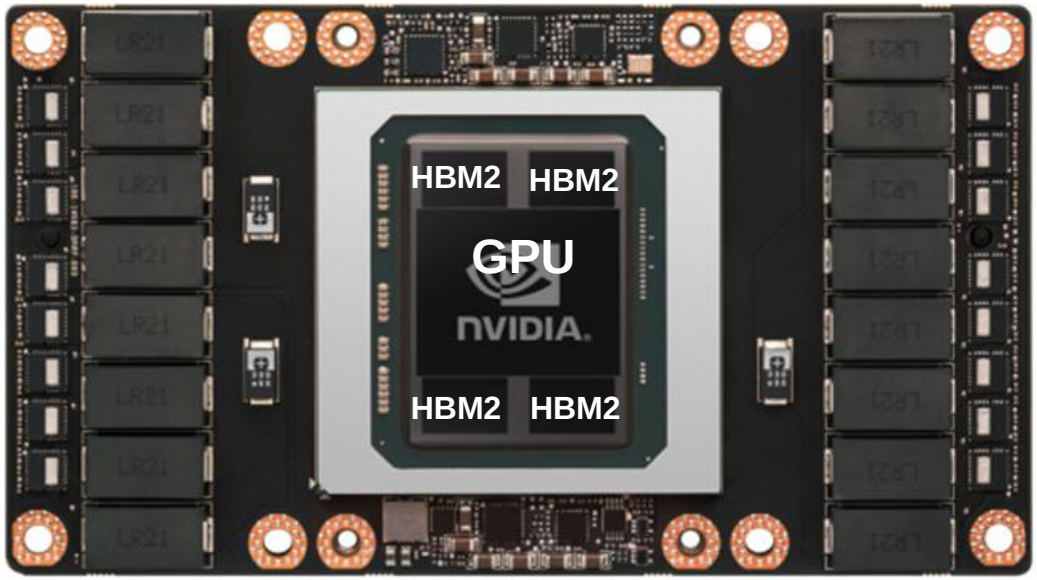


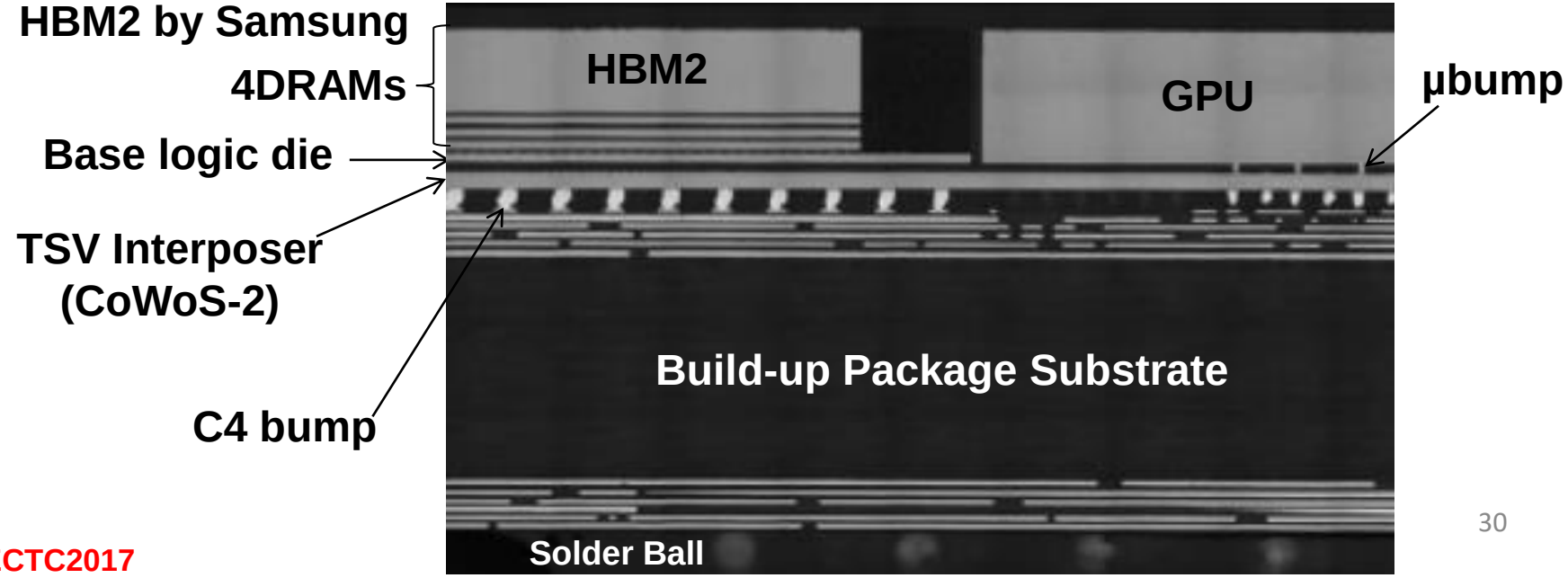
TSV-Interposer

Build-up organic substrate

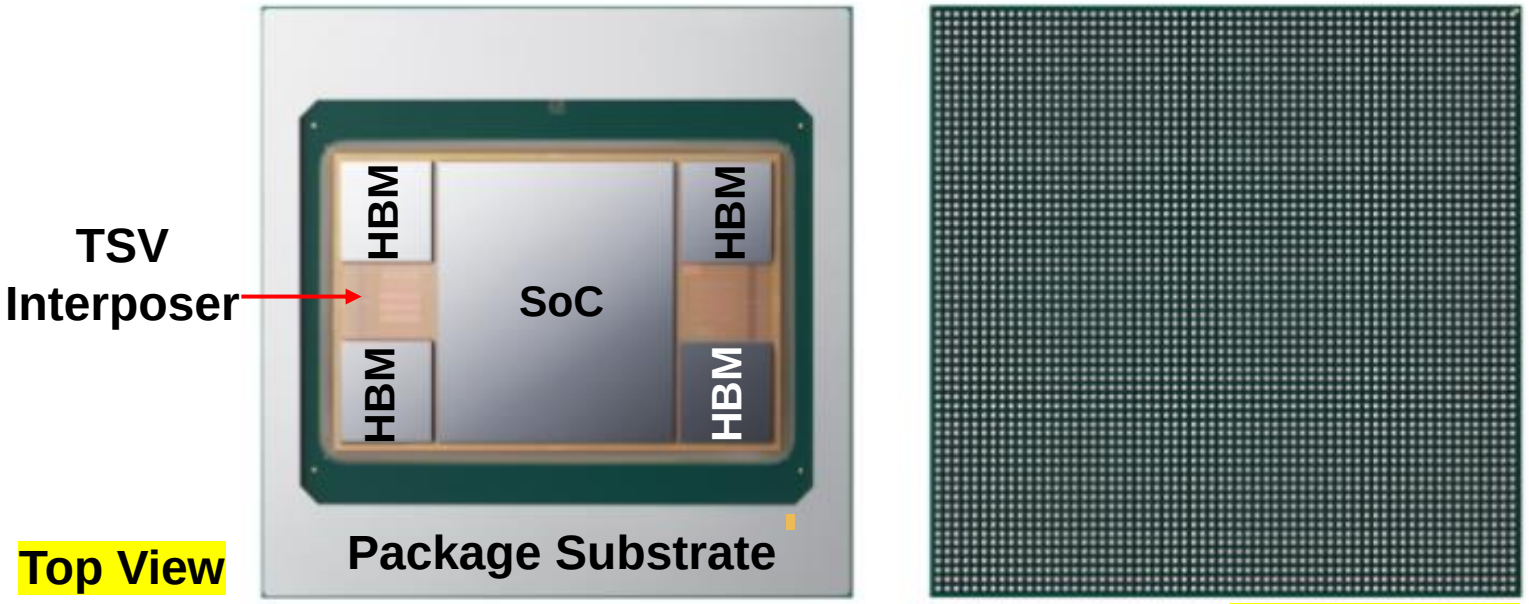
NVidia's P100 with TSMC's CoWoS-2 and Samsung's HBM2

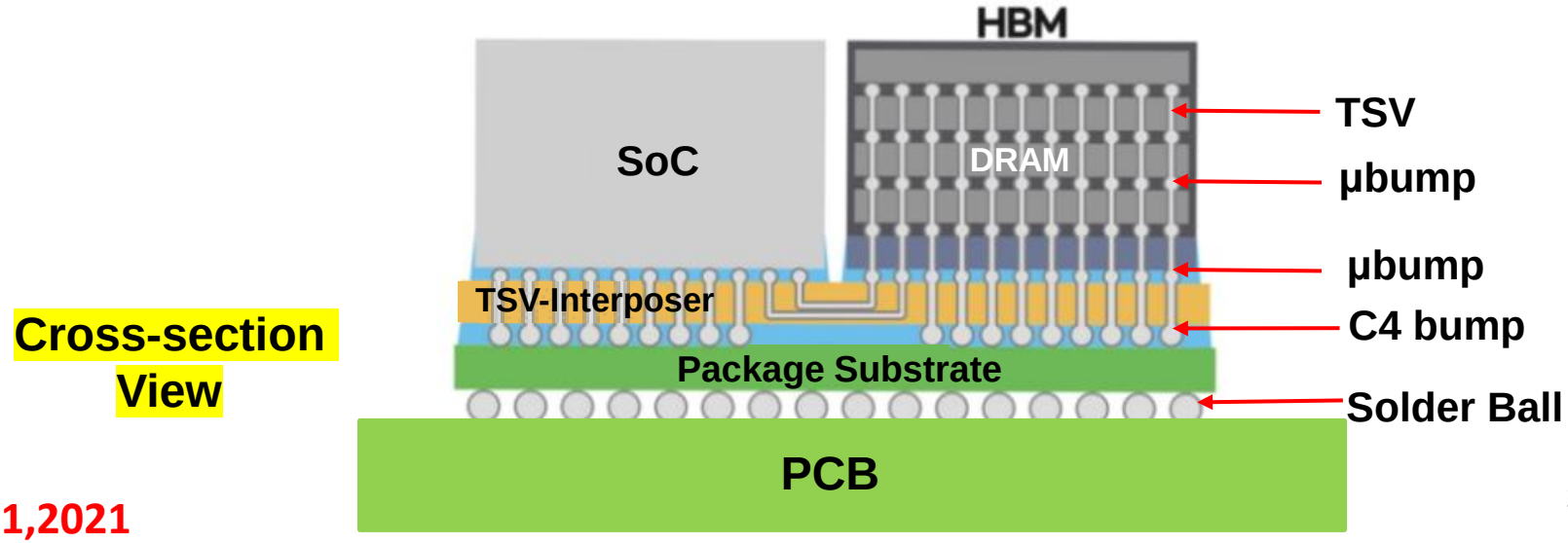




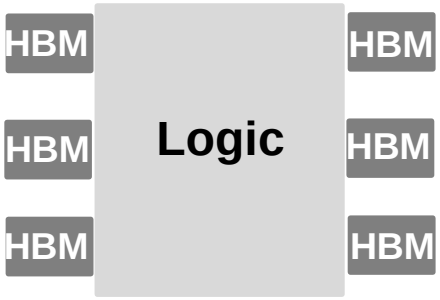


Samsung's Interposer-Cube4 (I-Cube4) (2.5D IC Integration)

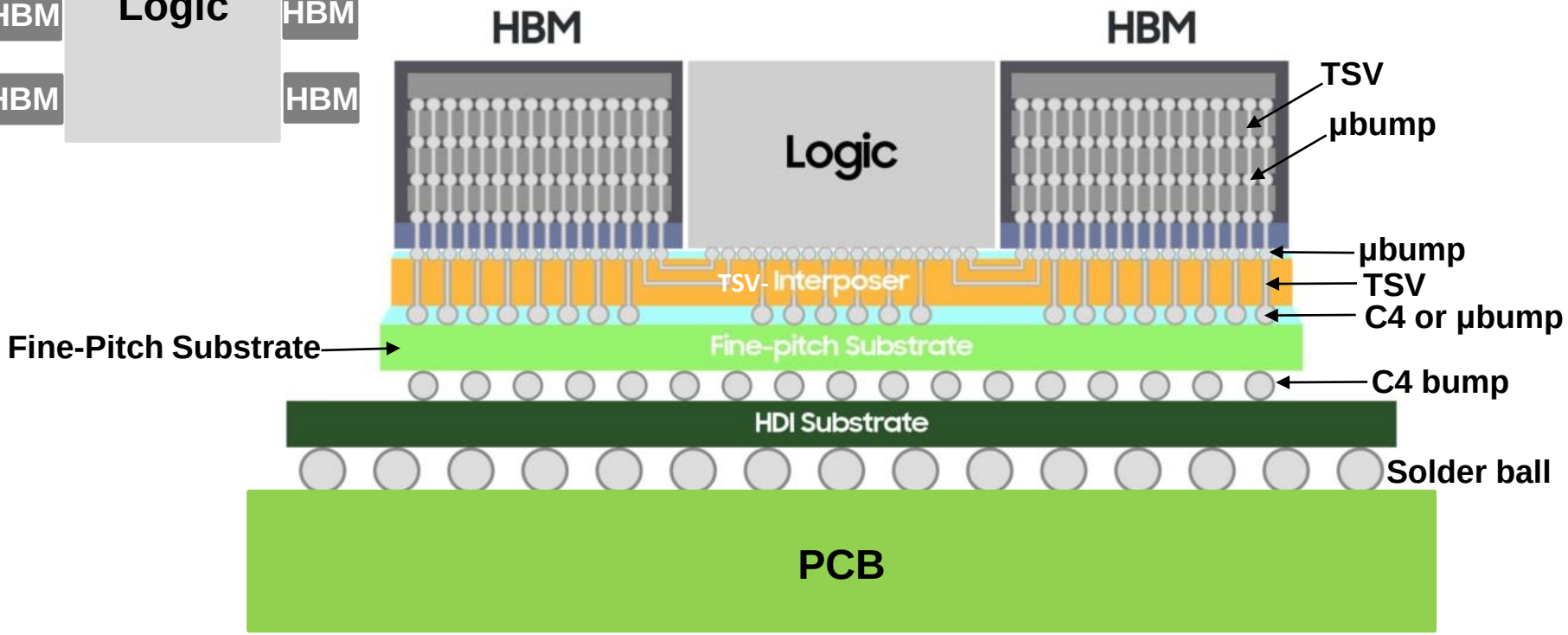




2.5D Integration Hybrid Substrate Cube (H-Cube) Solution for High Performance Applications



Samsung Announcement
November 11, 2021



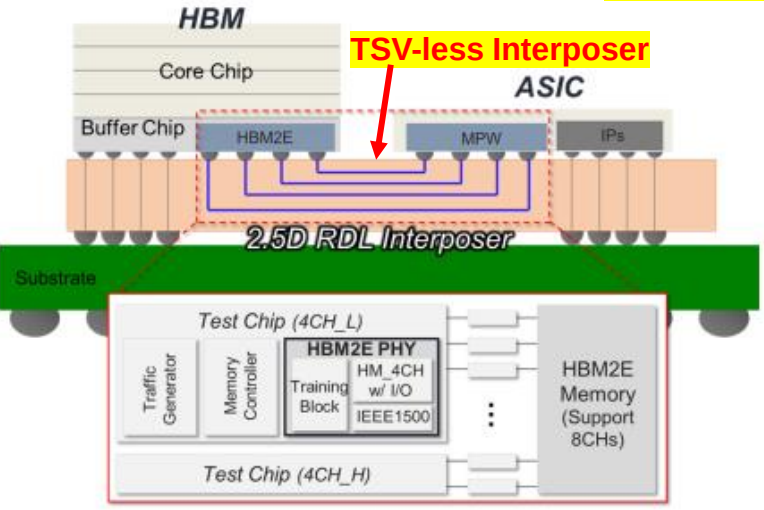
H-Cube Concept

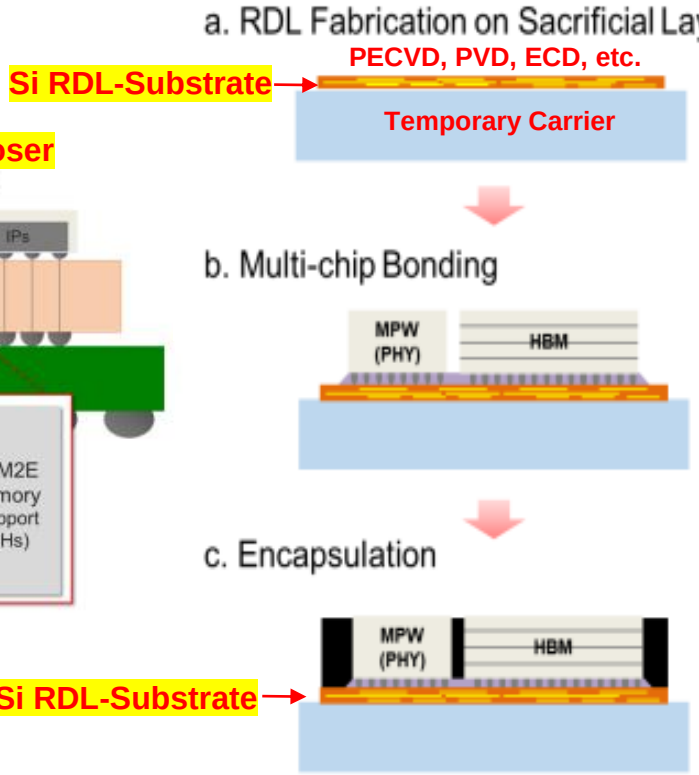
When integrating six or more HBMs, the difficulty in manufacturing the large-area substrate increases rapidly, resulting in decreased efficiency. Samsung solved this problem by applying a hybrid substrate structure in which HDI substrates that are easy to implement in large-area are overlapped under a high-end fine-pitch substrate. By decreasing the pitch of solder ball, which electrically connects the chip and the substrate, by 35% compared to the conventional ball pitch, the size of fine-pitch substrate can be minimized, while adding HDI substrate (module PCB) under the fine-pitch substrate to secure connectivity with the system board.

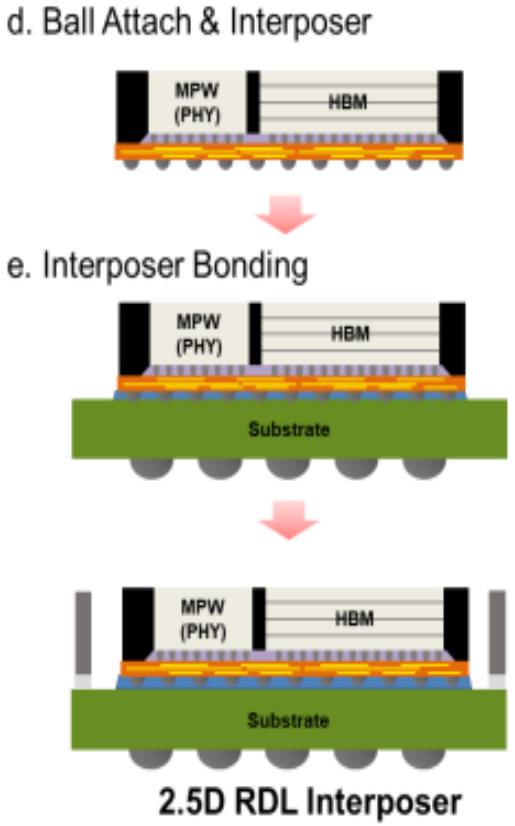
November 2021

Novel 2.5D RDL Interposer Packaging: A Key Enabler for the New Era of Heterogenous Chip Integration (R-Cube)

Min Jung Kim, Seok Hyun Lee, Kyoung Lim Suk, Jae Gwon Jang, Gwang-Jae Jeon, Ju-il Choi, Hyo Jin Yun, Jongpa Hong, Ju-Yeon Choi, Won Jae Lee, SukHyun Jung, Won Kyoung Choi and Dae-Woo Kim Test & System Package (TSP), Samsung Electronics Co., Ltd, Cheonan-si, Chungcheongnam-do, South Korea, South Korea mj3076.kim@samsung.com

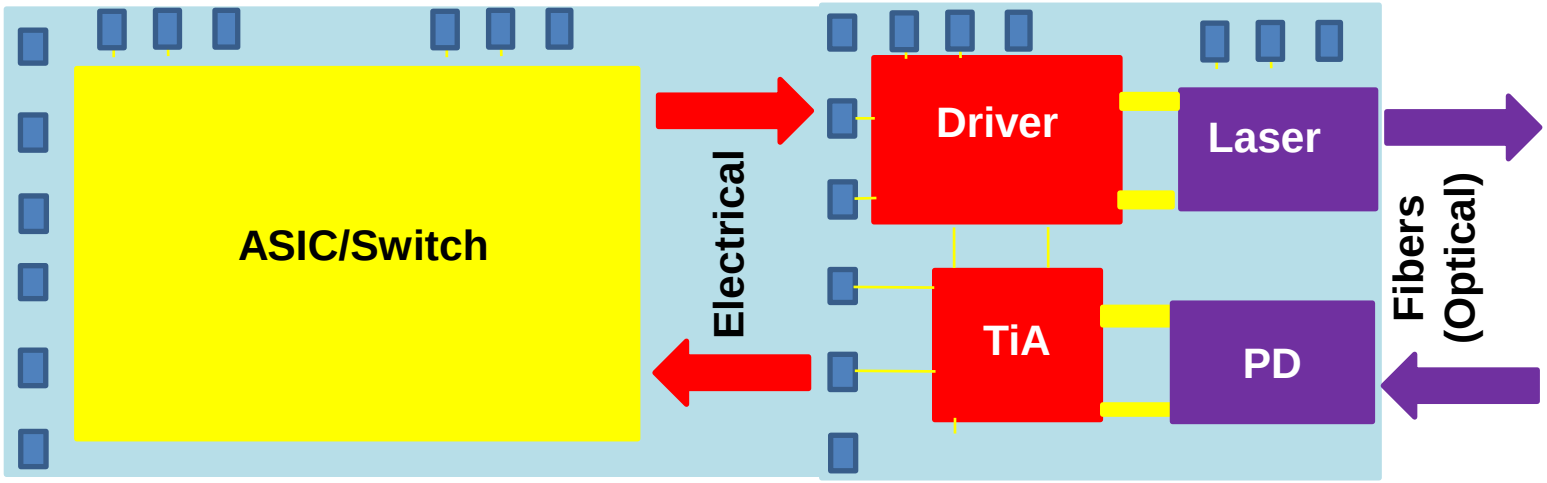


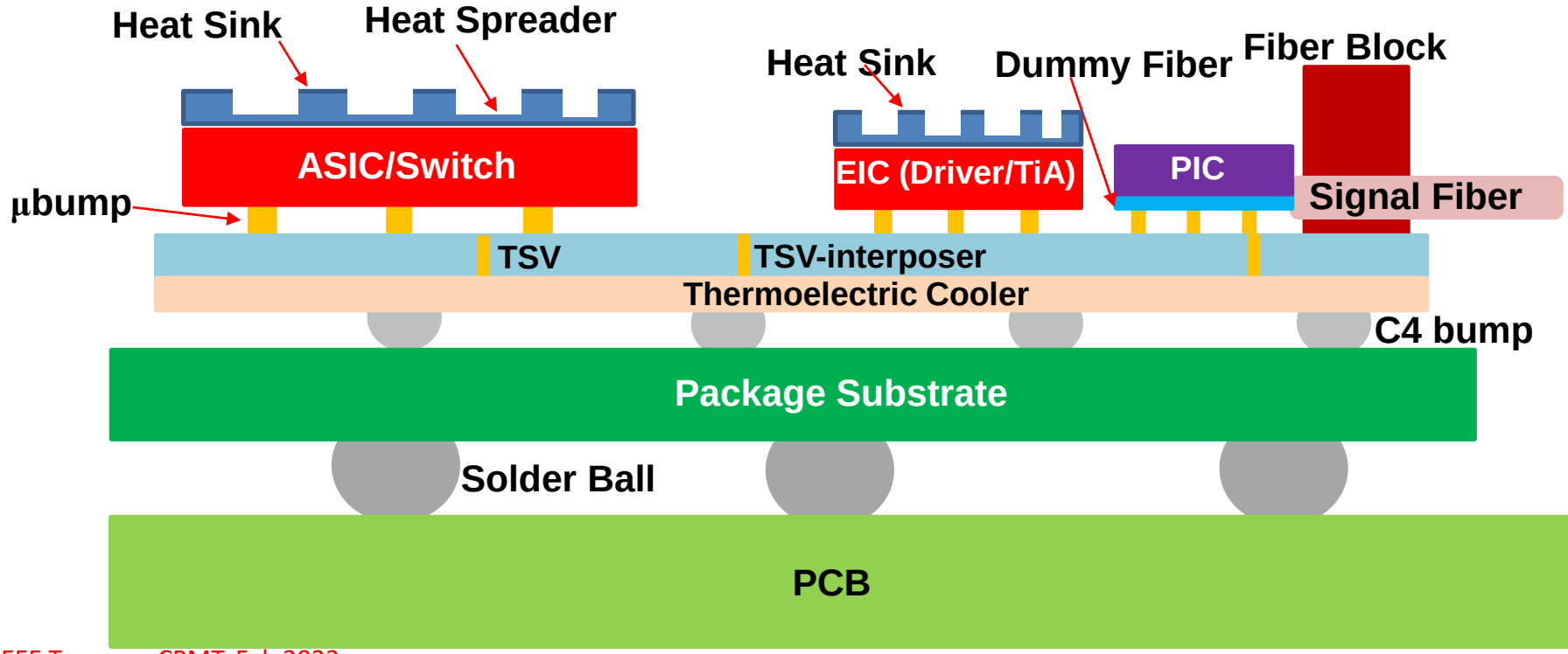




ECTC2021, IWLPC2022

2.5D Heterogeneous Integration of EIC and PIC Devices

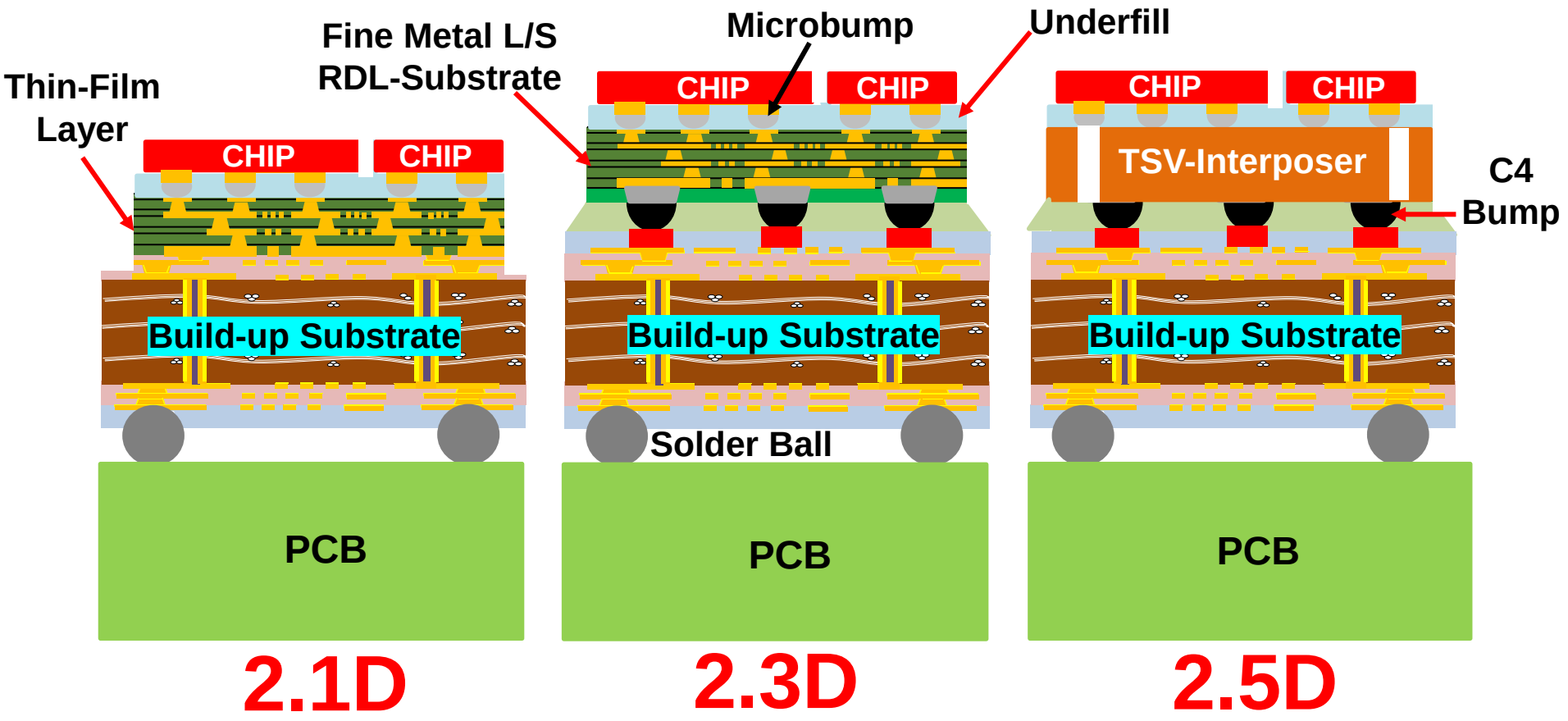




2.3D IC Integration

- **Chip-First (either face-up or face-down)**
- **Chip-Last (RDL-First)**

2.1D, 2.3D, and 2.5D IC Integration

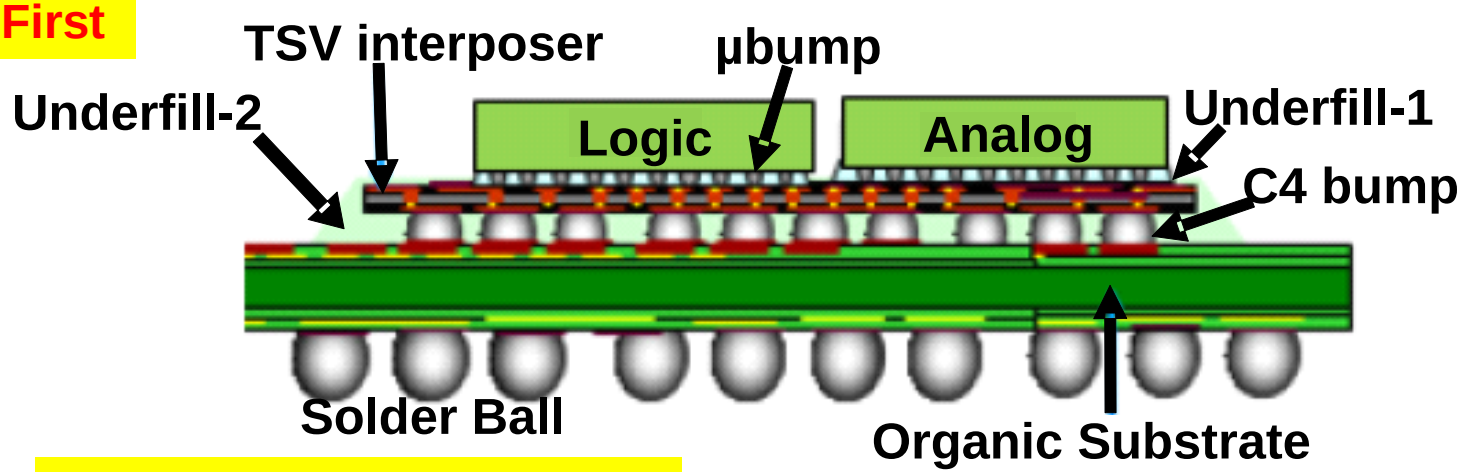


Fine Metal L/S RDL-Substrate = Thin-Film Layer

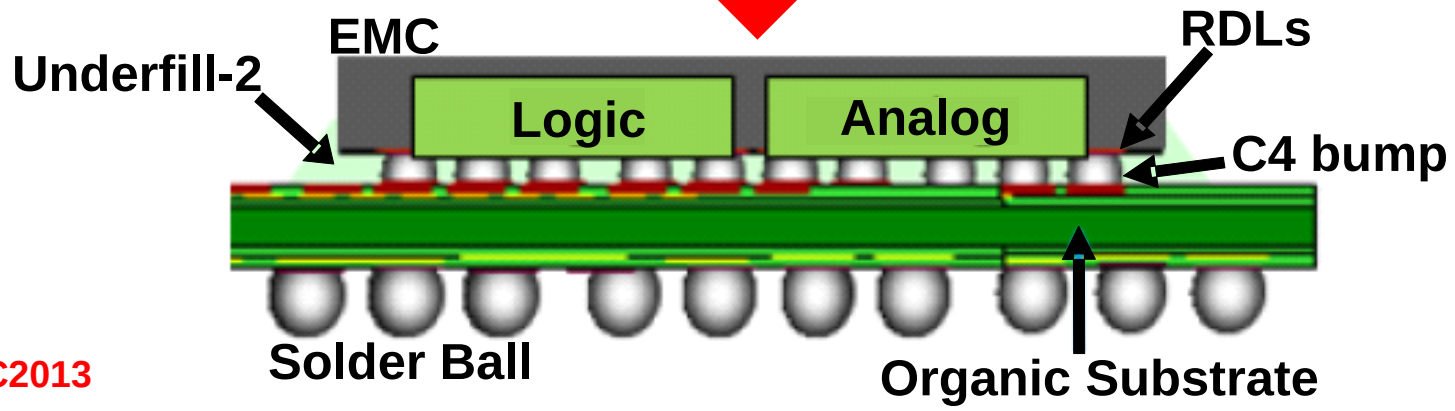
Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions

Seung Wook Yoon, Patrick Tang, Roger Emigh, Yaojian Lin, Pandi C. Marimuthu, and Raj Pendse
STATSChipPAC Ltd., 5 Yishun Street 23, Singapore 768442

Chip-First



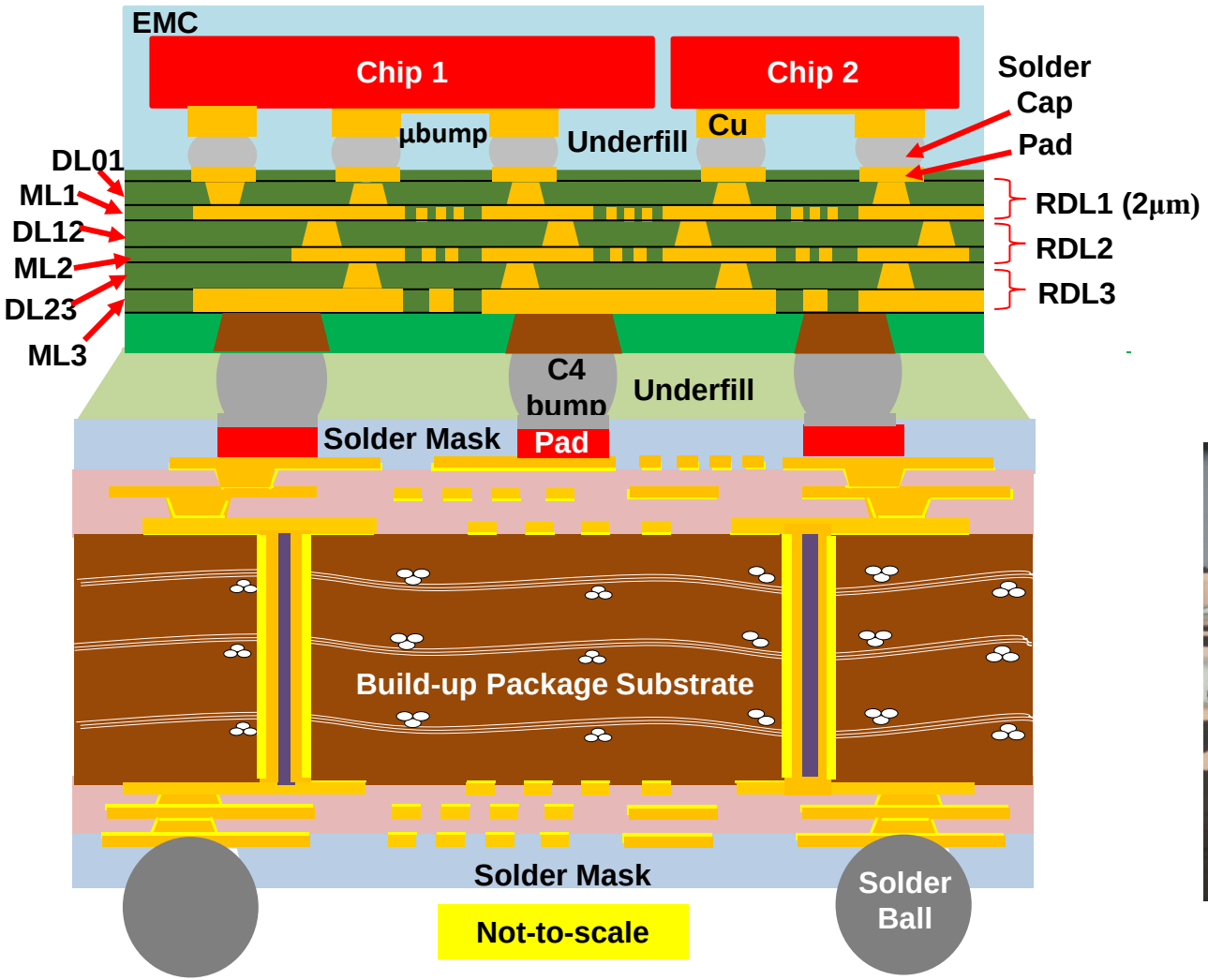
- The µbump, underfill-1, and TSV-interposer are eliminated.
- The RDLs are made by fan-out technology.

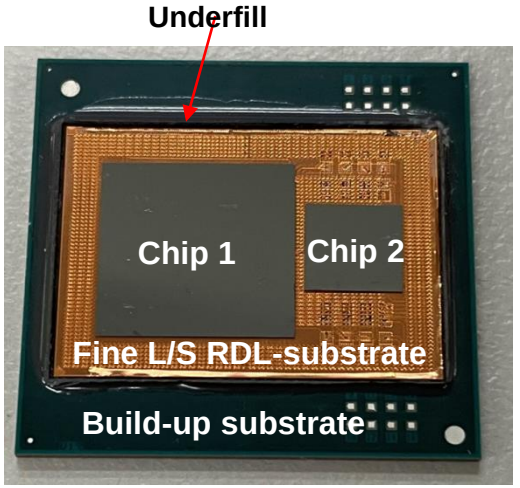


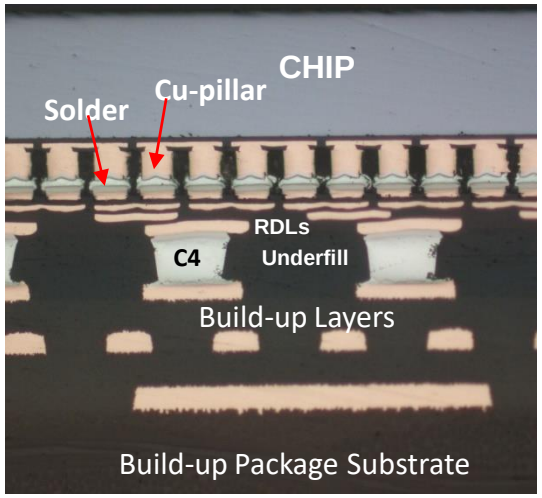
Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

John H Lau, Gary Chang-Fu Chen, Jones Yu-Cheng Huang, Ricky Tsun-Sheng Chou, Channing Cheng-Lin Yang, Hsing-Ning Liu, and Tzvy-Jang Tseng
Unimicron Technology Corporation,
Taoyuan City, Taiwan
John_Lau@unimicron.com

Chip-Last





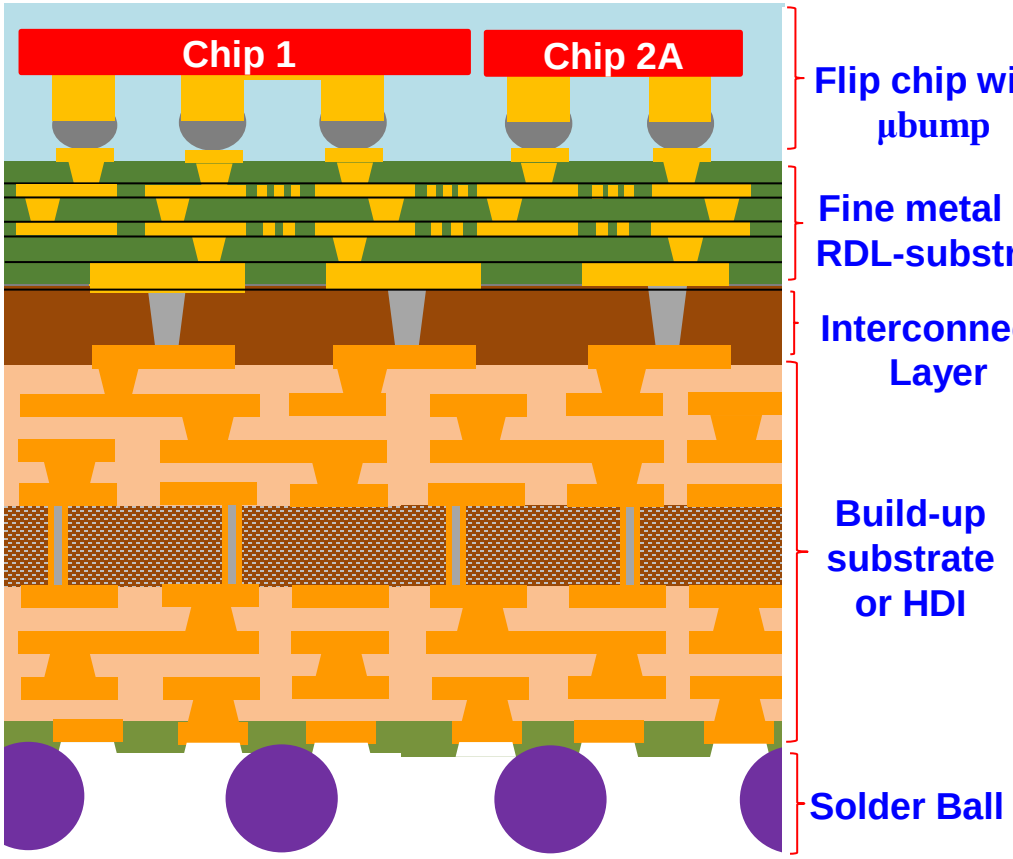


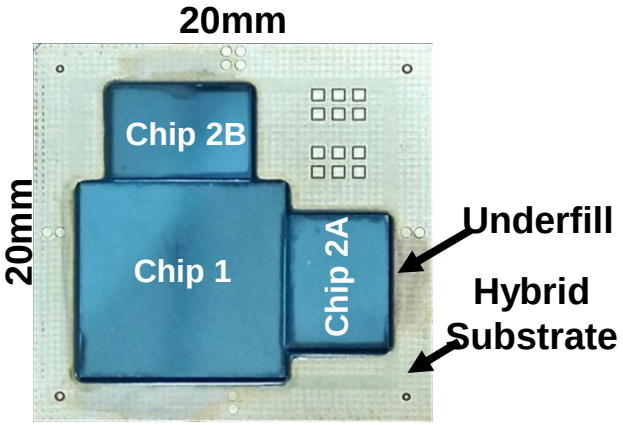
IEEE Transactions on CPMT, August 2021

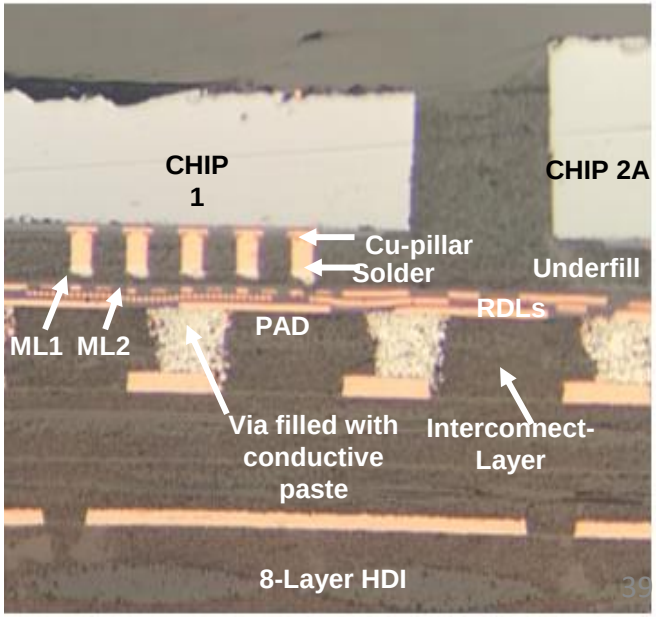
High-Density Hybrid Substrate for Heterogeneous Integration

Chia-Yu Peng , John H. Lau , Life Fellow, IEEE, Cheng-Ta Ko, Paul Lee, Eagle Lin, Kai-Ming Yang, Puru Bruce Lin, Tim Xia, Leo Chang, Ning Liu, Curry Lin, Tzu Nien Lee, Jason Wong, Mike Ma, Tzyy-Jang Tseng
Unimicron

Chip-Last

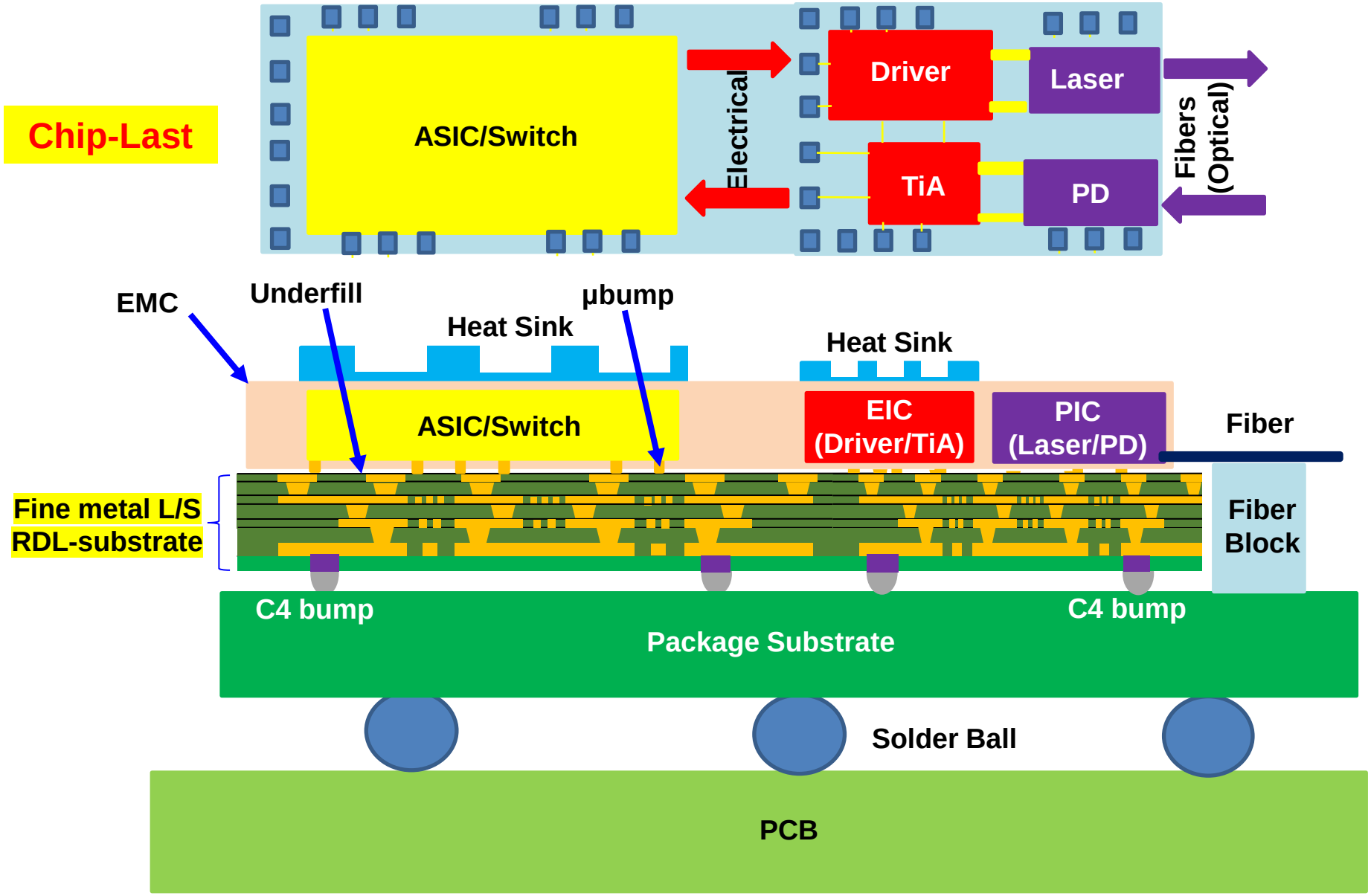






IEEE Transactions on CPMT, March 2022

2.3D Heterogeneous Integration of EIC and PIC Devices

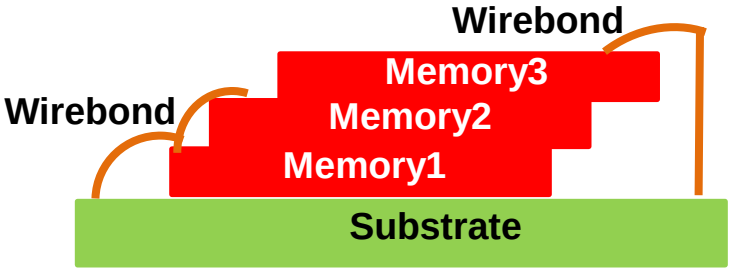


3D IC Integration

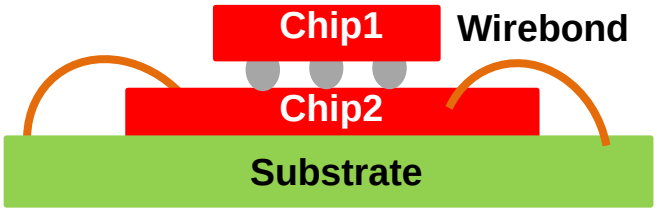
- **3D IC Packaging (without TSVs)**
- **3d IC Integration (with TSVs)**

3D IC Packaging (without TSVs)

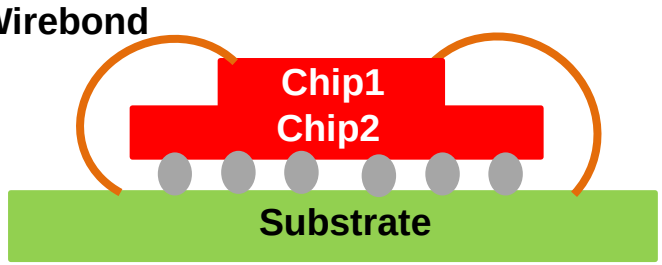
3D IC Packaging



(a)



(b)



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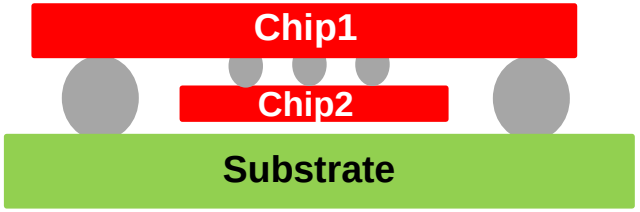

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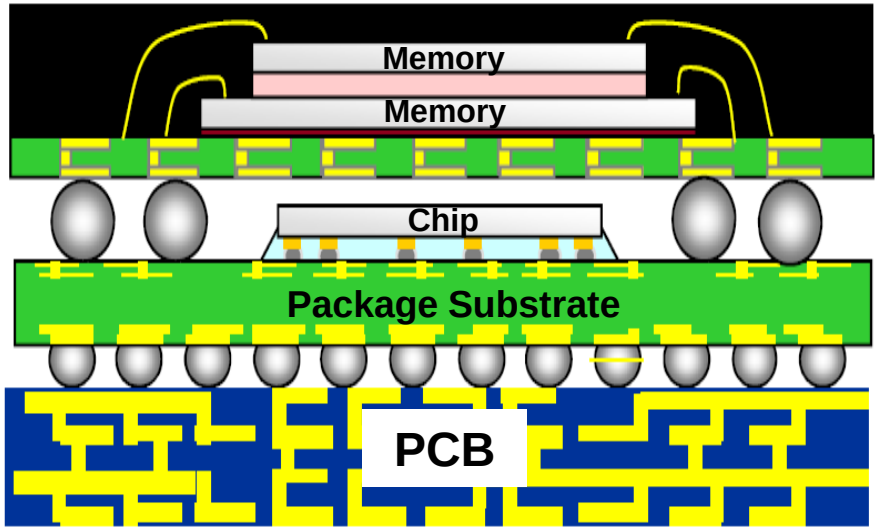

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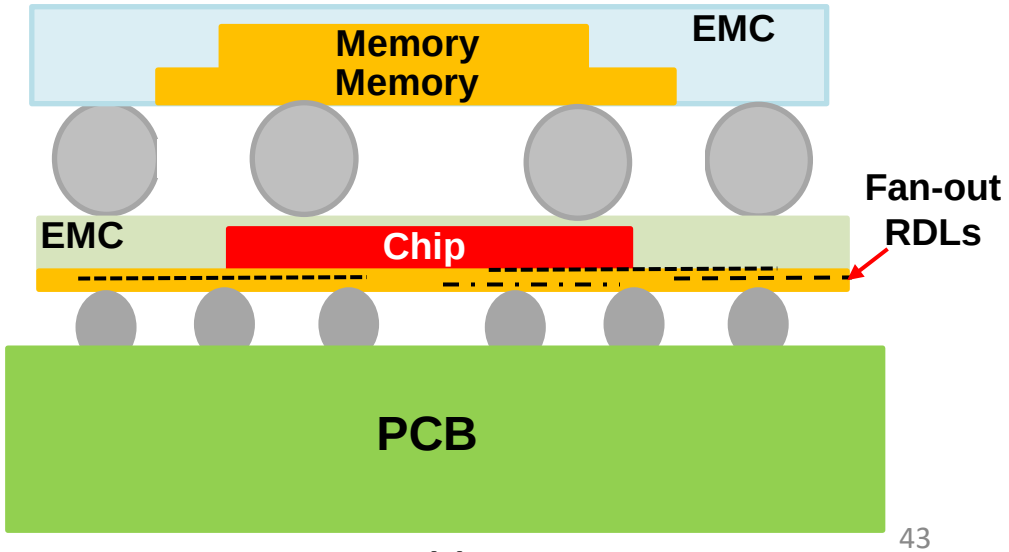
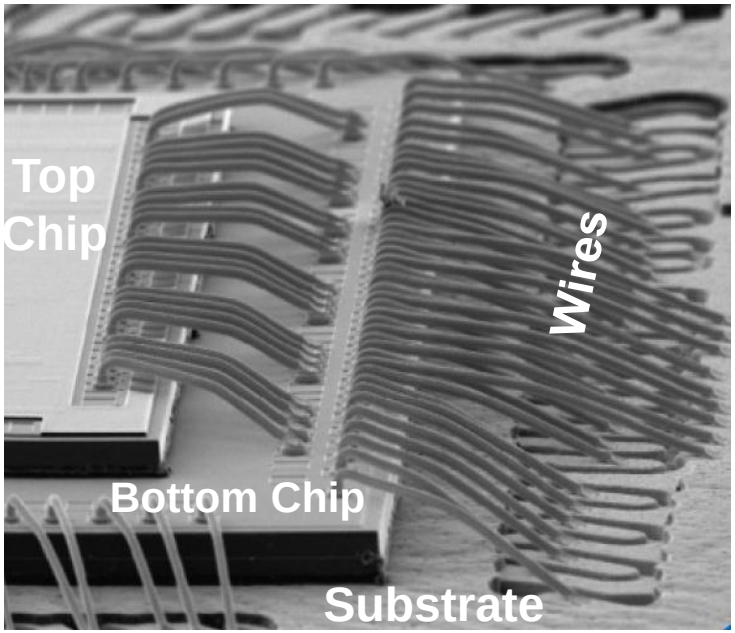
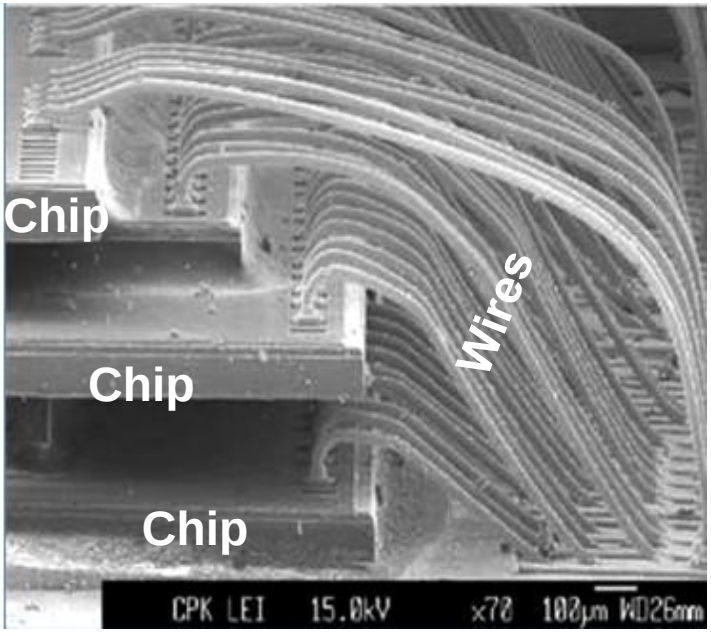


(f)

3D (Wirebonding) IC Packaging

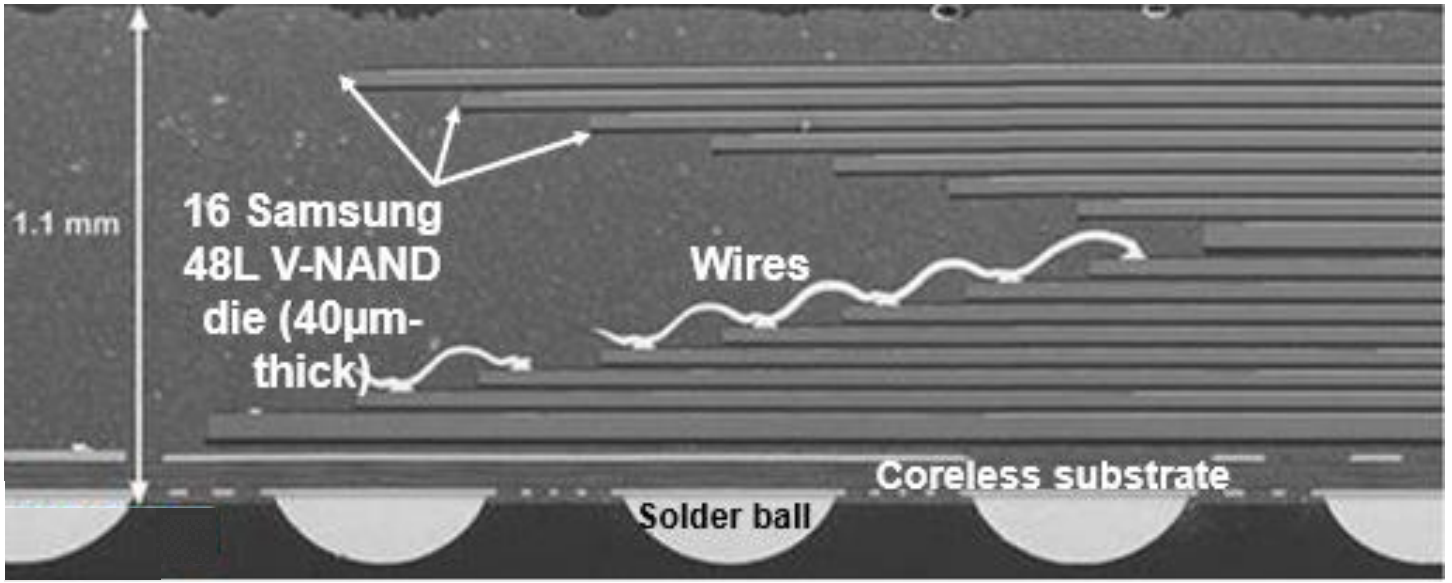
(a)





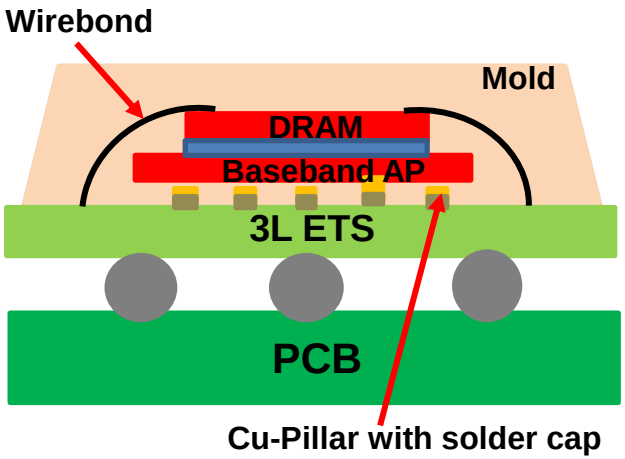
(b)

(c)



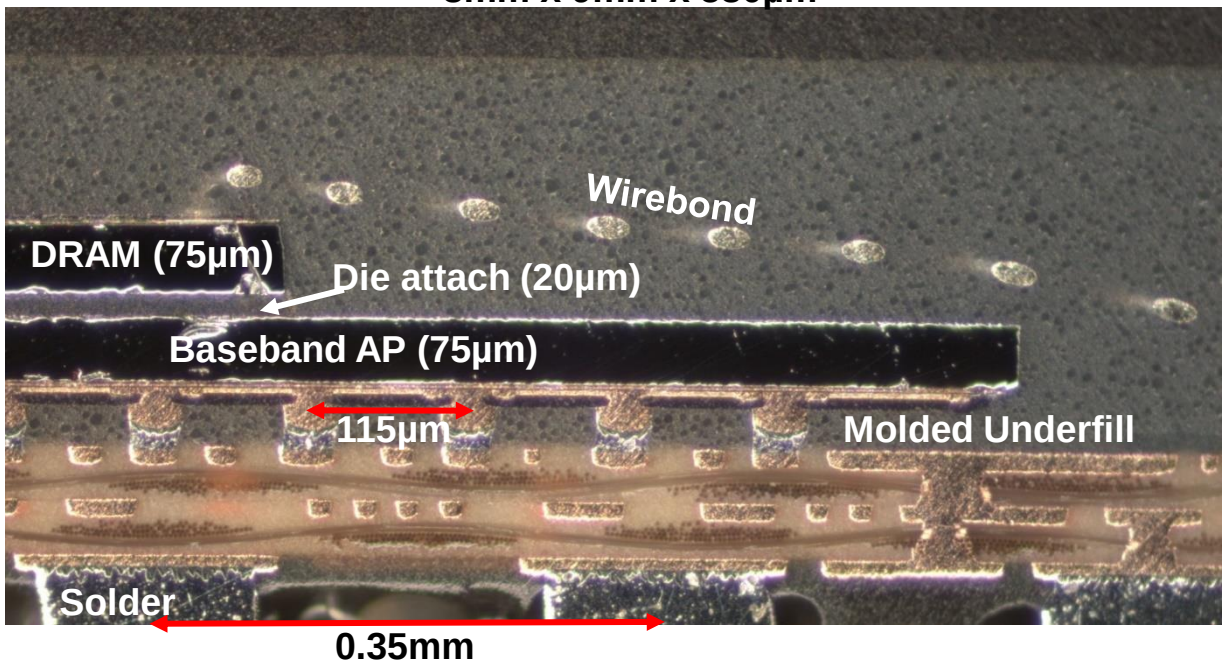
Semiconductor Advanced Packaging, 2021

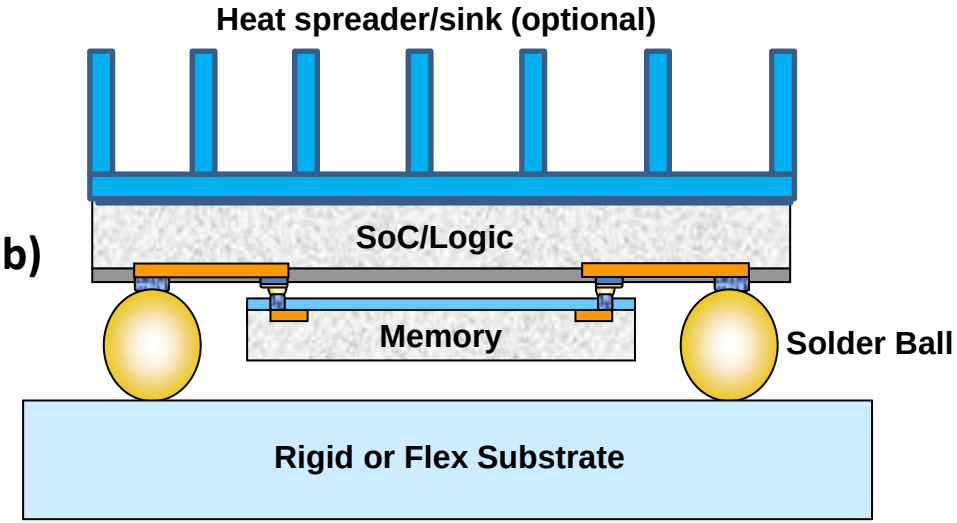
3D (Flip Chip and Wirebond) Packaging



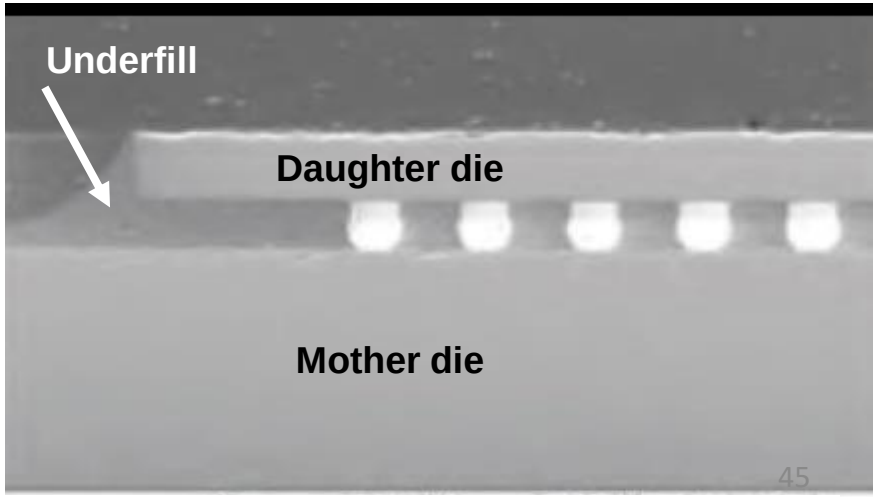
(a)

8mm x 9mm x 580µm



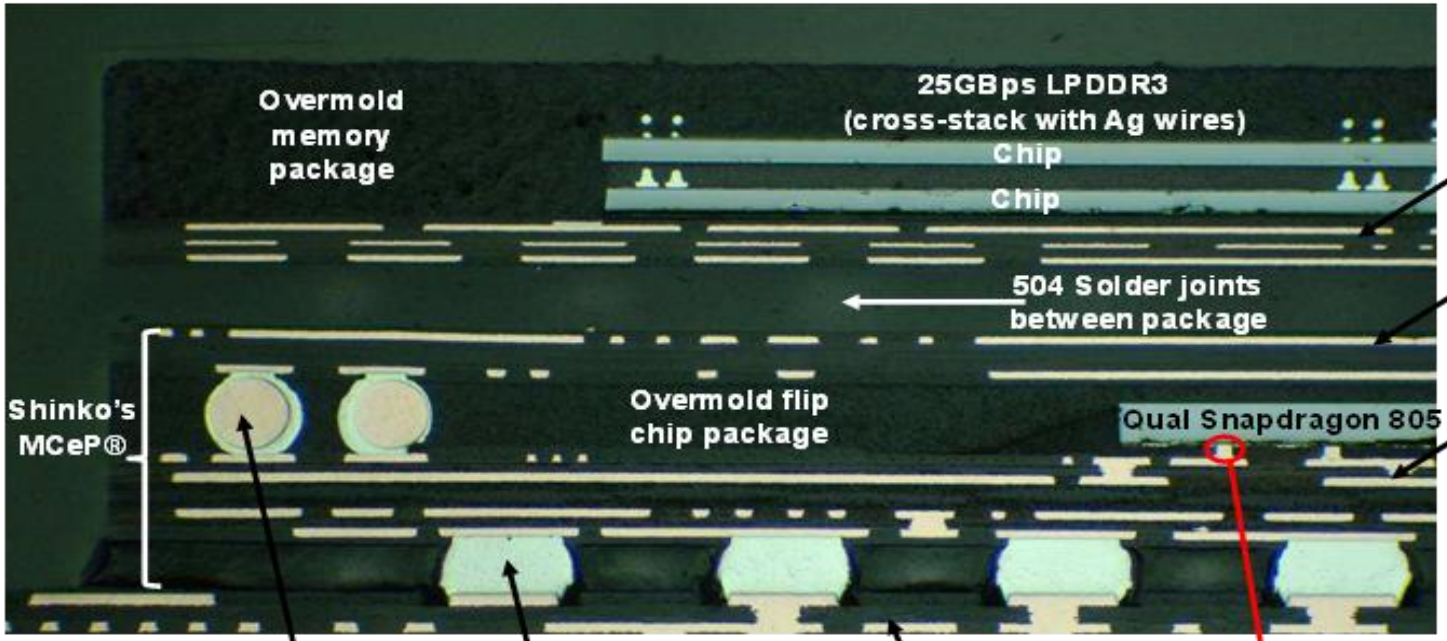


(b)



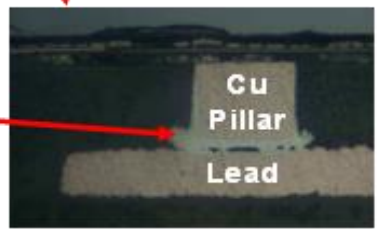
Semiconductor Advanced Packaging, 2021

3D (PoP with flip chip) IC Packaging (Qualcomm)

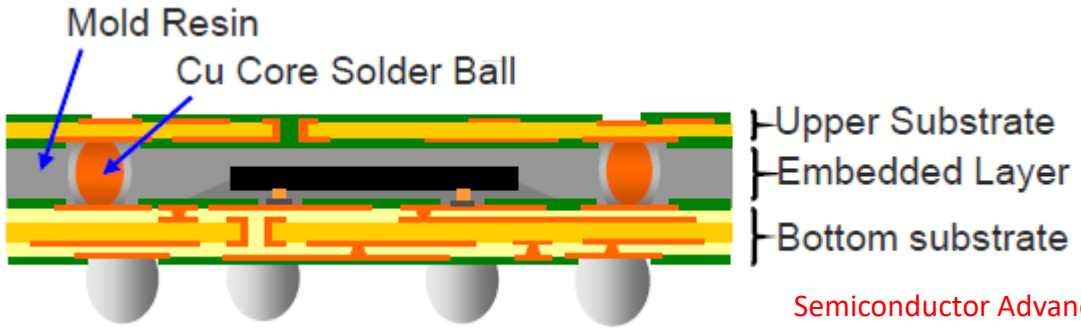


Snapdragon 805 Processor:

- ❑10.9mm x 11mm x 95µm
- ❑CuSnAg bumps @110µm pitch
- ❑30µm bump-height after TC-NCP



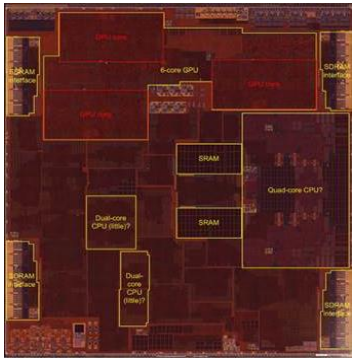
Shinko's MCeP



Semiconductor Advanced Packaging, 2021

3D PoP: Apple/TSMC InFO (Integrated fan-Out) for the iPhone Application Processor (Chip-First Die Face-up)

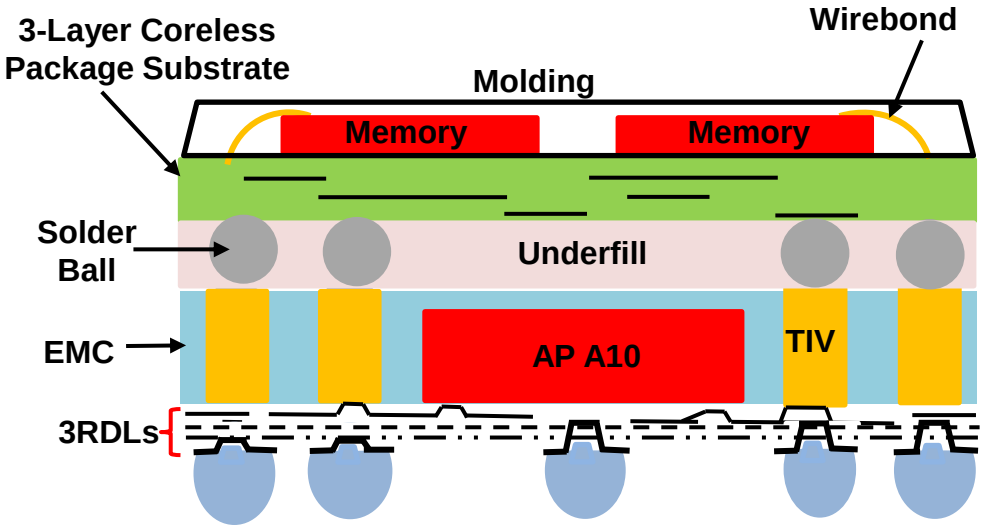
SoC

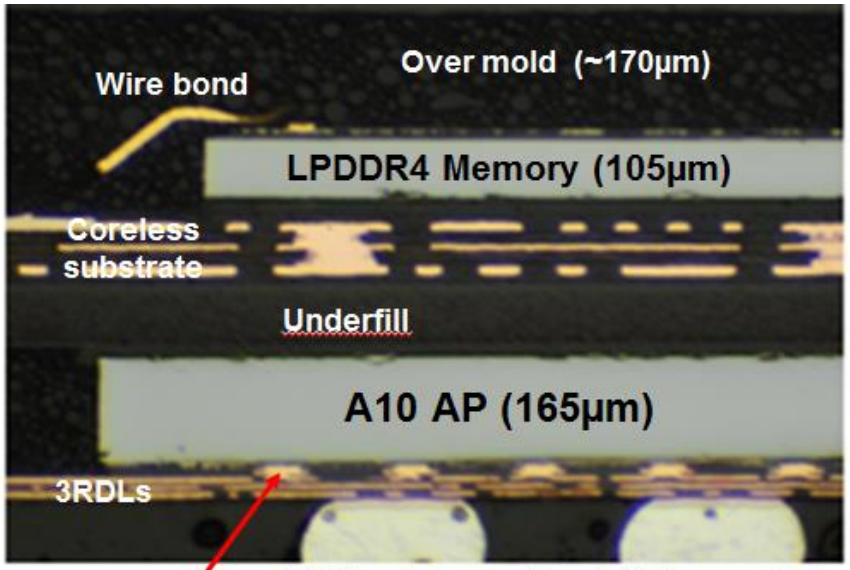


11.6mm x 10.8mm x 165µm

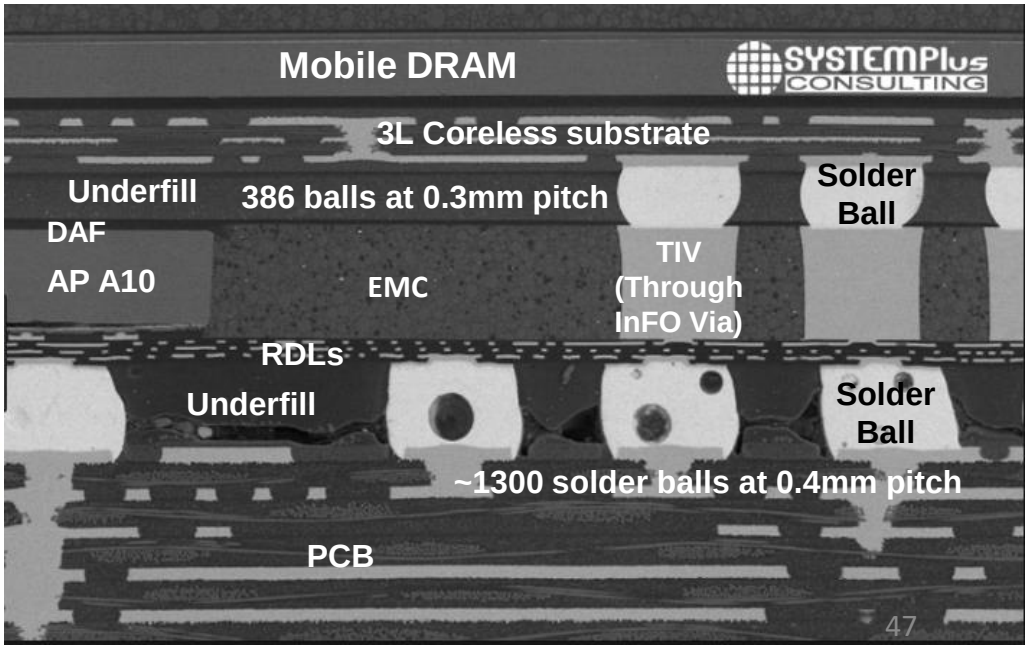
PoPzzz

15.5mm x 14.4mm x 825µm





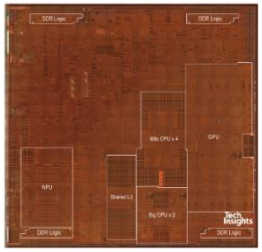
Shipped in 2016



FOWLP, 2018

3D (PoP with Fan-Out) Packaging (Apple/TSMC)

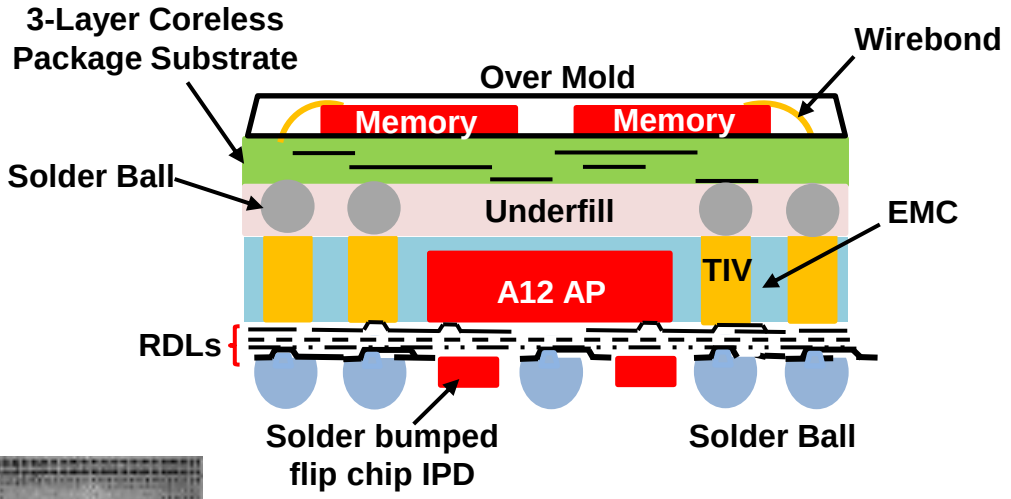
AP SoC

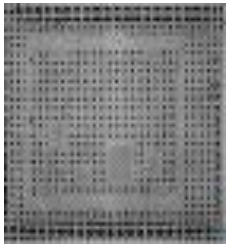


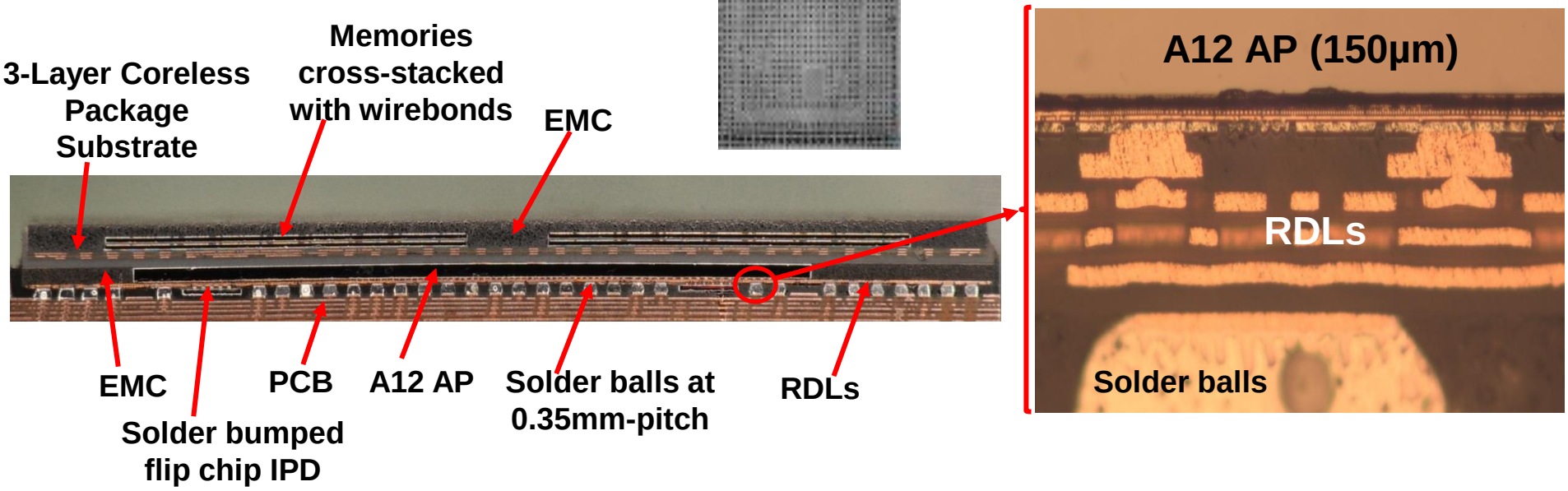
9.9mm x 8.4mm

PoP

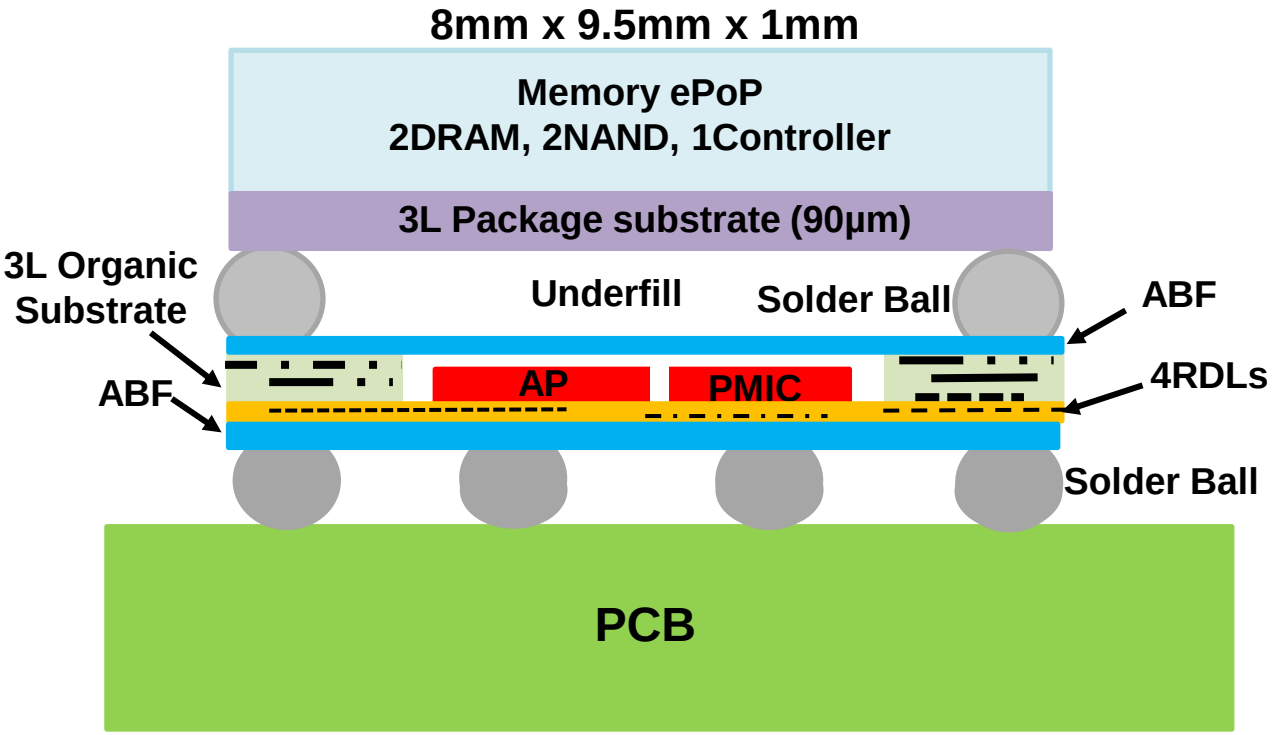
13.4mm x 14.4mm

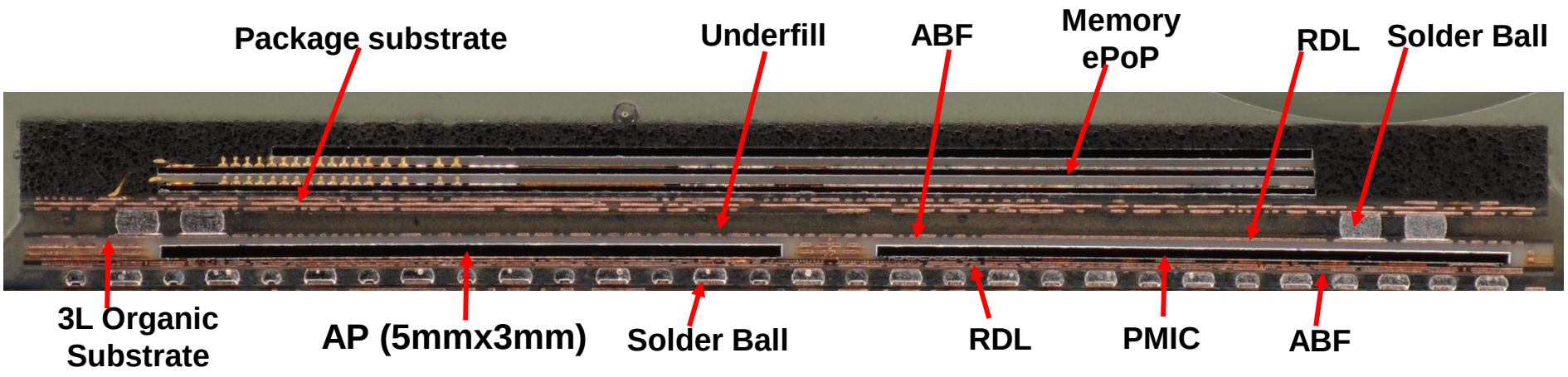






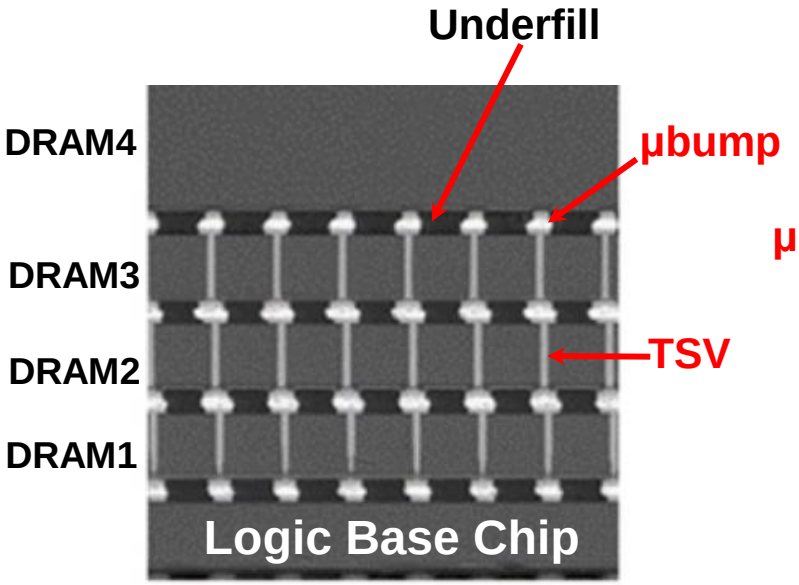
3D (PoP with Fan-Out) IC Packaging (Samsung)



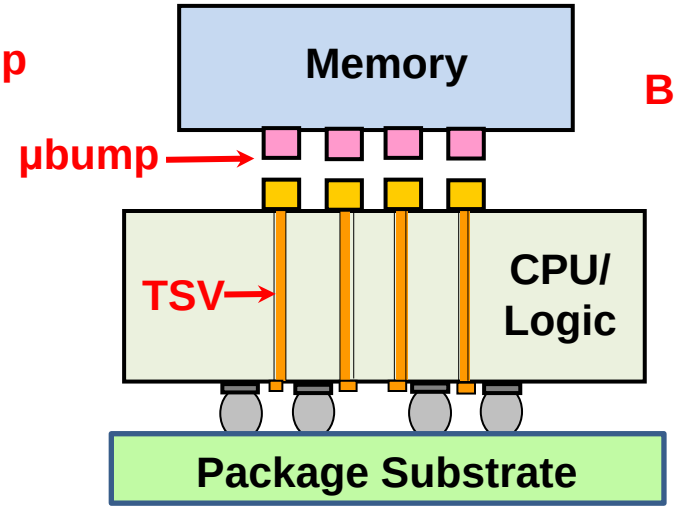


3D IC Integration (with TSVs)

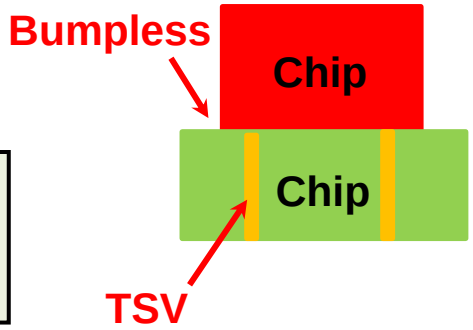
3D IC Integration



(a)

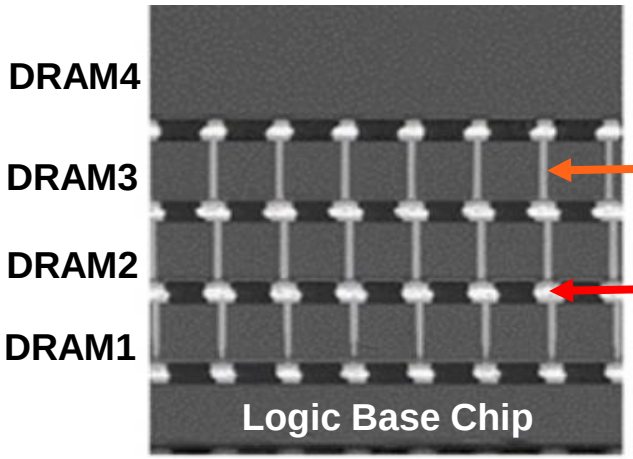


(b)

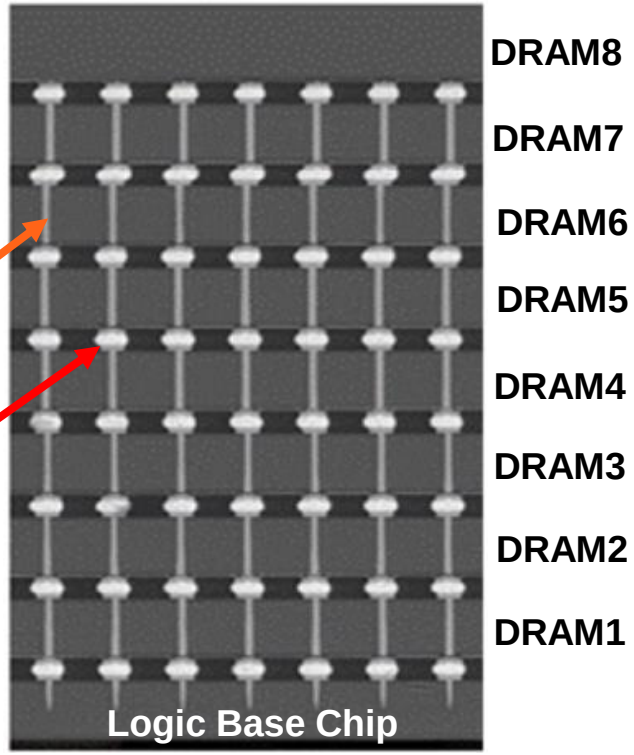


(c)

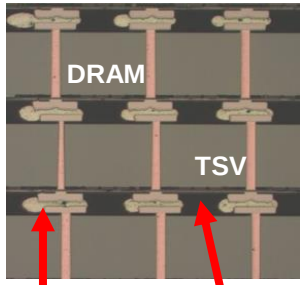
3D IC Integration with Active Interposer (High Bandwidth Memory)



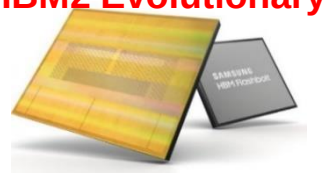
HBM (high bandwidth memory)



HBM2



HBM2E (HBM2 Evolutionary)

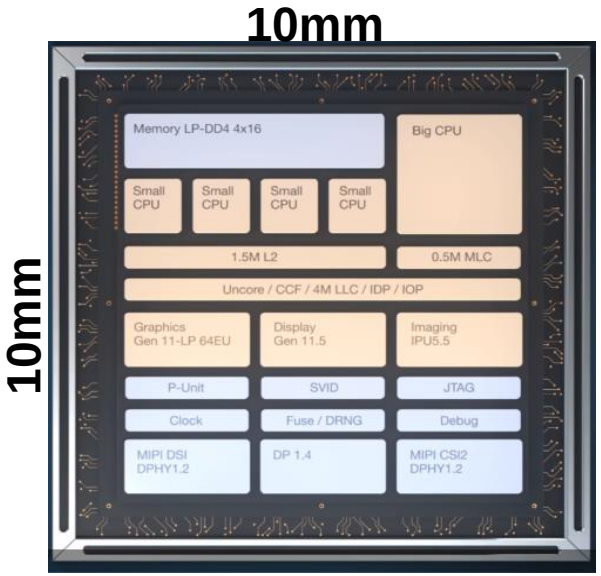


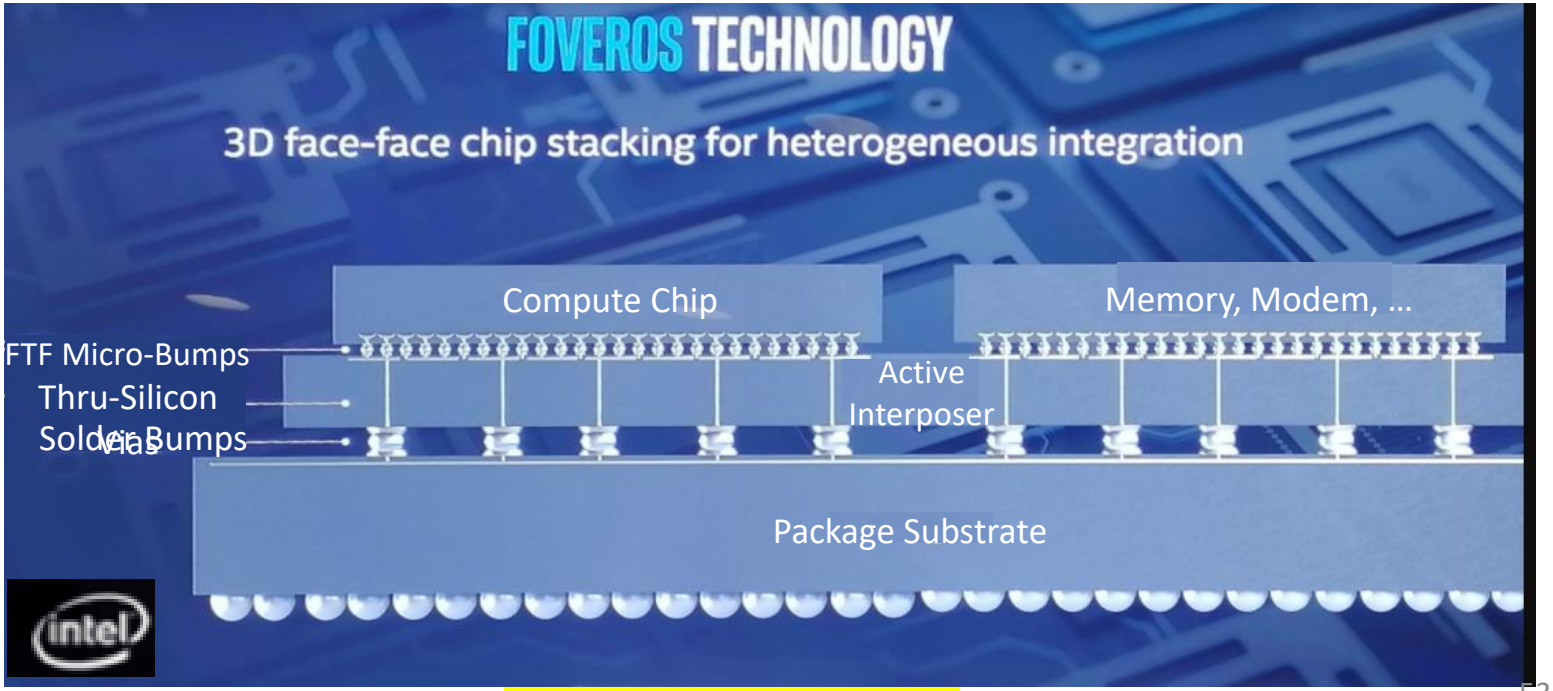
	HBM	HBM2 (Original)	HBM2/HBM2E (Current)	HBM3 (Upcoming)
Max Pin Transfer Rate	1Gbps	2Gbps	2.4Gbps	?
Max Capacity	4GB	8GB	24GB	64GB
Max Bandwidth	128GBps	256GBps	307GBps	512GBps

Semiconductor Advanced Packaging, 2021

Intel 3D IC Integration – FOVEROS Technology

Lakefield

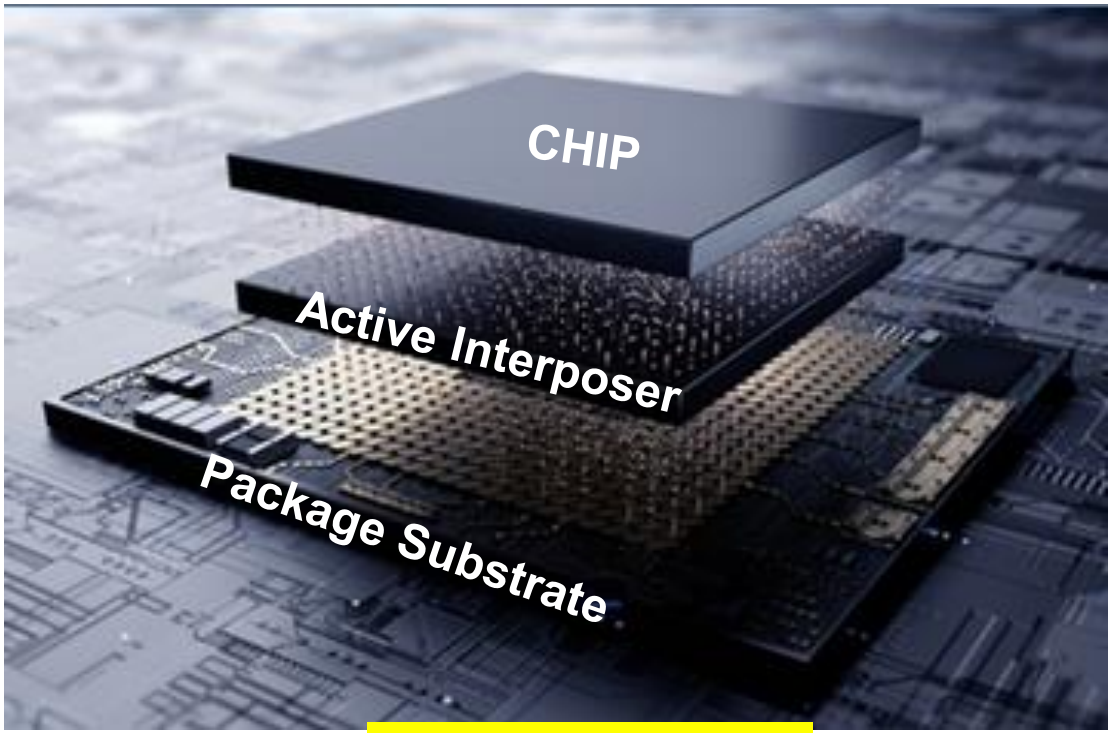




3D IC Integration

Semiconductor Advanced Packaging, 2021

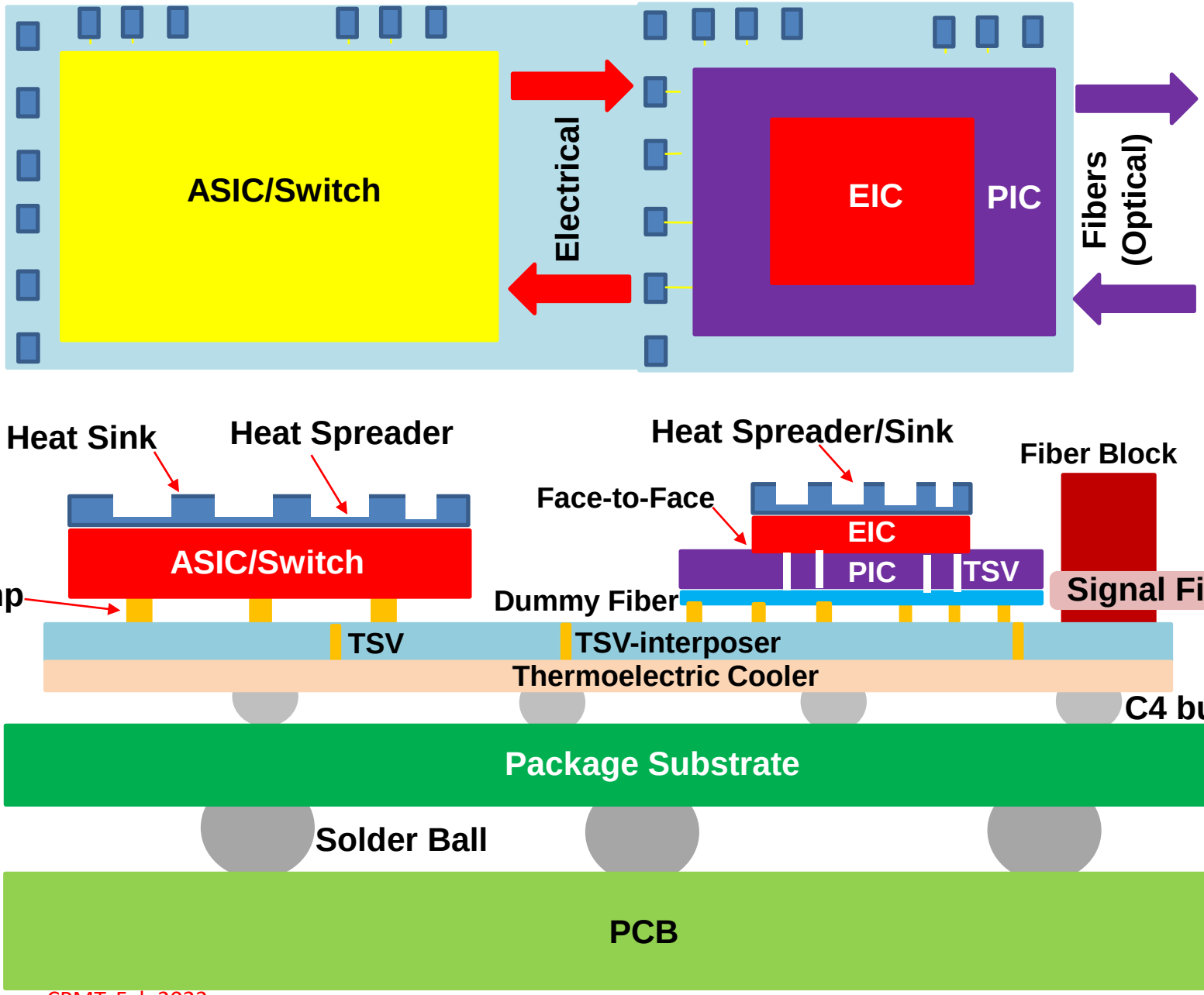
Chip-to-Active TSV-Interposer (Samsung X-Cube)



3D IC Integration

IEEE Hot Chip Conference2020.

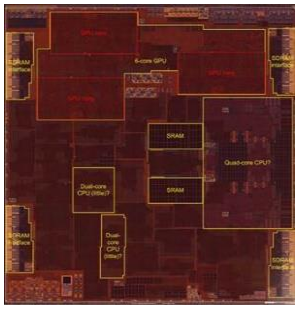
3D Heterogeneous Integration of EIC and PIC Devices



System-on-Chip (SoC)

Moore's Law - Apple's Application Processors (AP): SoC (System-on-Chip) - A10, A11, A12, A13, A14, and A15

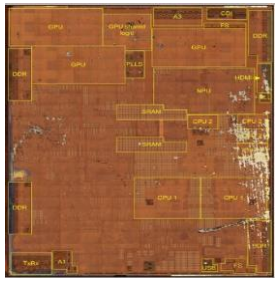
A10



A10 consists of:

- 6-core GPU (graphics processor unit)
- 2 dual-core CPU (central processing unit)
- 2 blocks of SRAMs (static random access memory), etc.
- 16nm process technology
- Transistors = 3 billion
- Chip area = 125mm^2

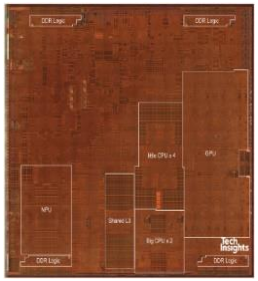
A11



A11 consists of:

- More functions, e.g., 2-core Neural Engine for Face ID
- Apple designed tri-core GPU
- 10nm process technology
- Transistors = 4.3 billion
- Chip area =89mm^2

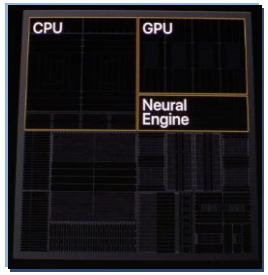
A12



A12 consists of:

- Eight-core Neural Engine with AI capabilities
- Four-core GPU (faster)
- Six-core CPU (better performance)
- 7nm process technology
- Transistors = 6.9 billion
- Chip area = 83mm^2

A13



A13 consists of:

- Eight-core Neural Engine with Machine Learning
- Four-core GPU (20% faster > A12)
- Six-core CPU (20% faster and 35% save energy > A12)
- 7nm process technology with EUV
- Transistors = 8.5 billion
- Chip area = 98.5mm^2

A14

A14 consists of:

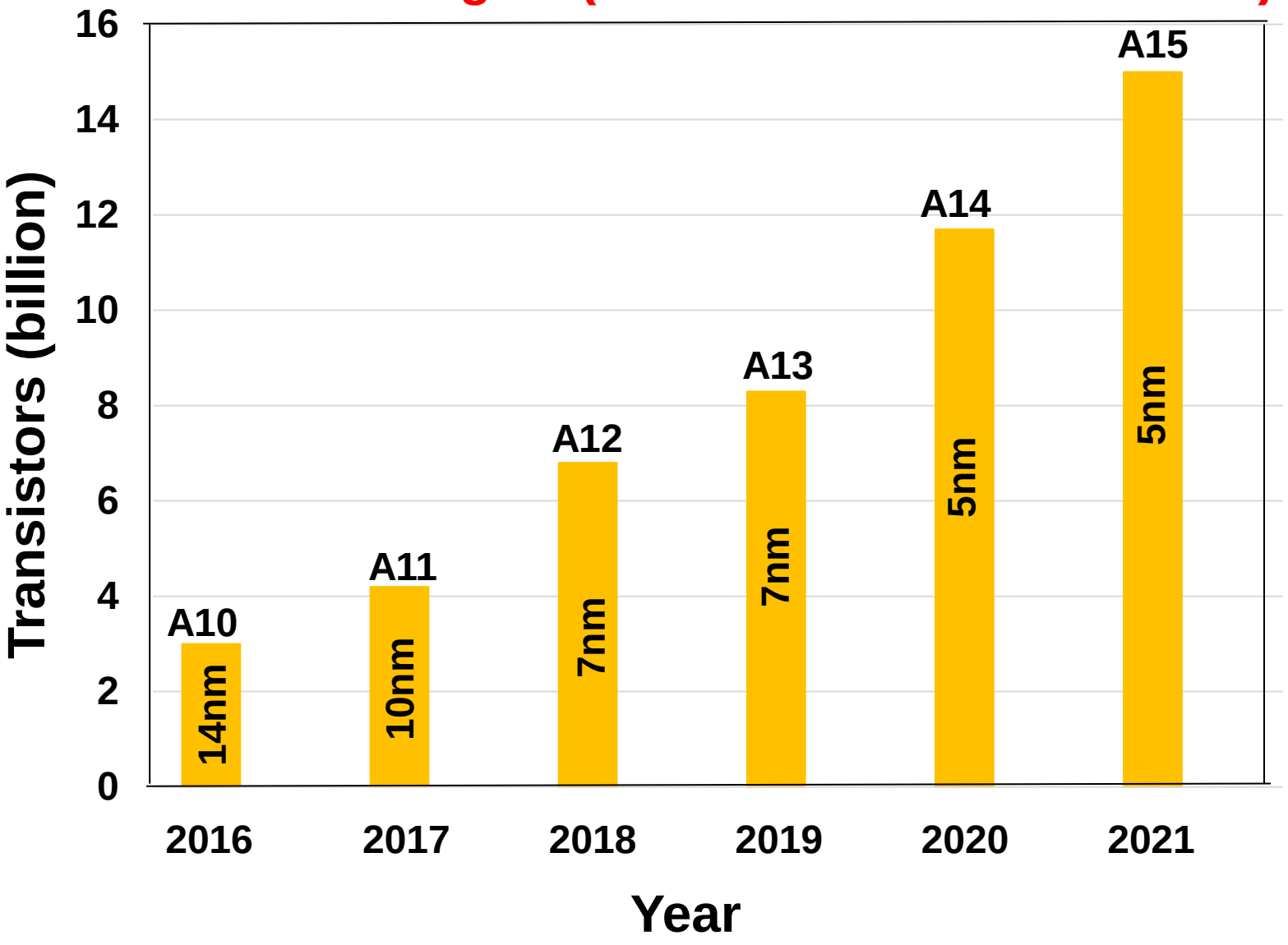
- 16-core Neural Engine with Machine Learning (11 trillion/s, 10 times faster > A13)
- Four-core GPU (30% faster > A13)
- Six-core CPU (40% faster > A13)
- 5nm process technology with EUV
- Transistors = 11.8 billion
- Chip area = 88mm^2

A15

A15 consists of:

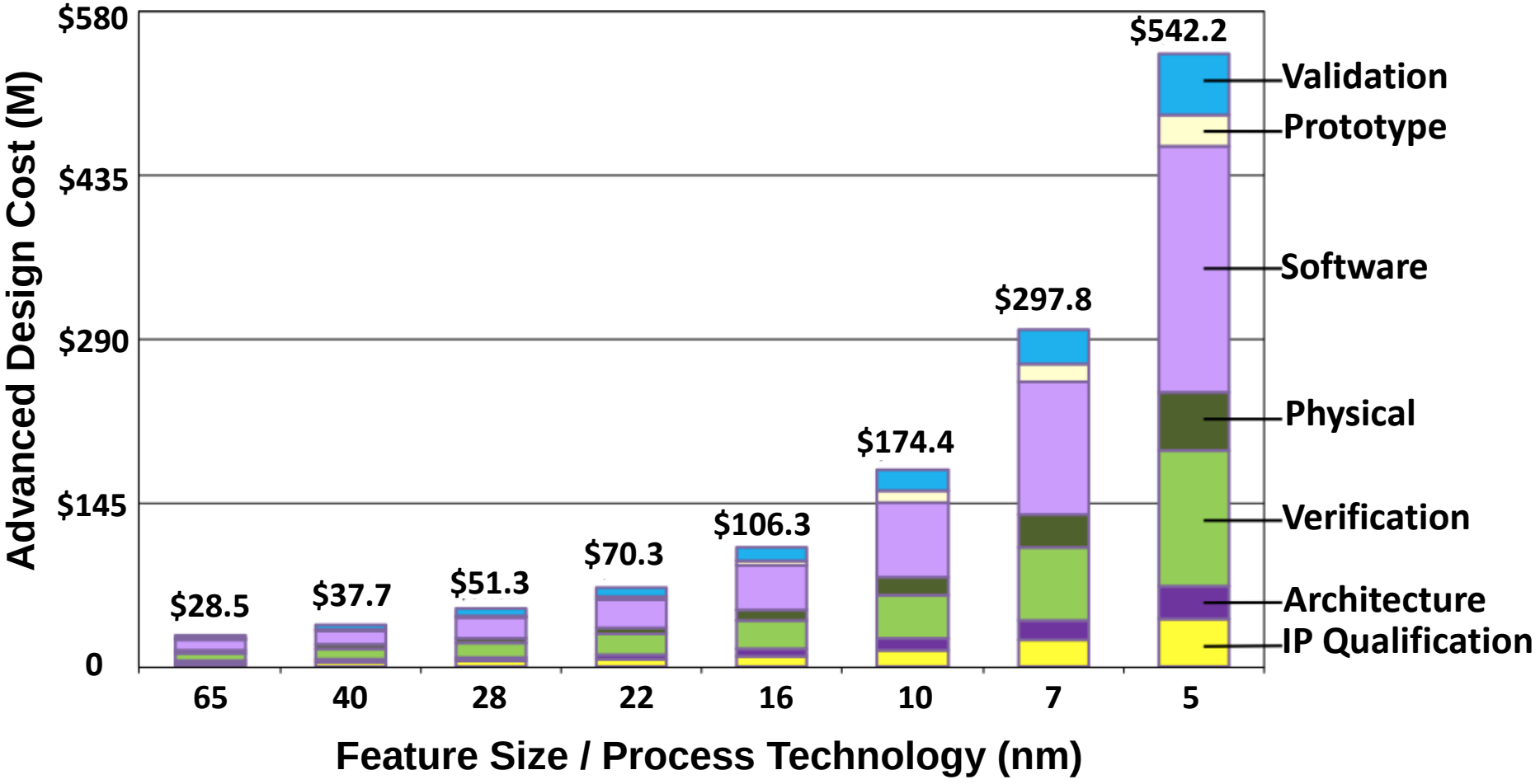
- 16-core Neural Engine to speed up AI tasks with Machine Learning (15.8 trillion/s)
- Four-core GPU, but 5-core for iPhone Pro and 13Pro Max
- Six-core CPU (faster > A14)
- 5nm process technology with EUV
- Transistors = 15 billion
- Image signal processor

Apple Application Processors vs. Transistors vs. Process Technologies (The Power of Moore's Law)



It is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC.

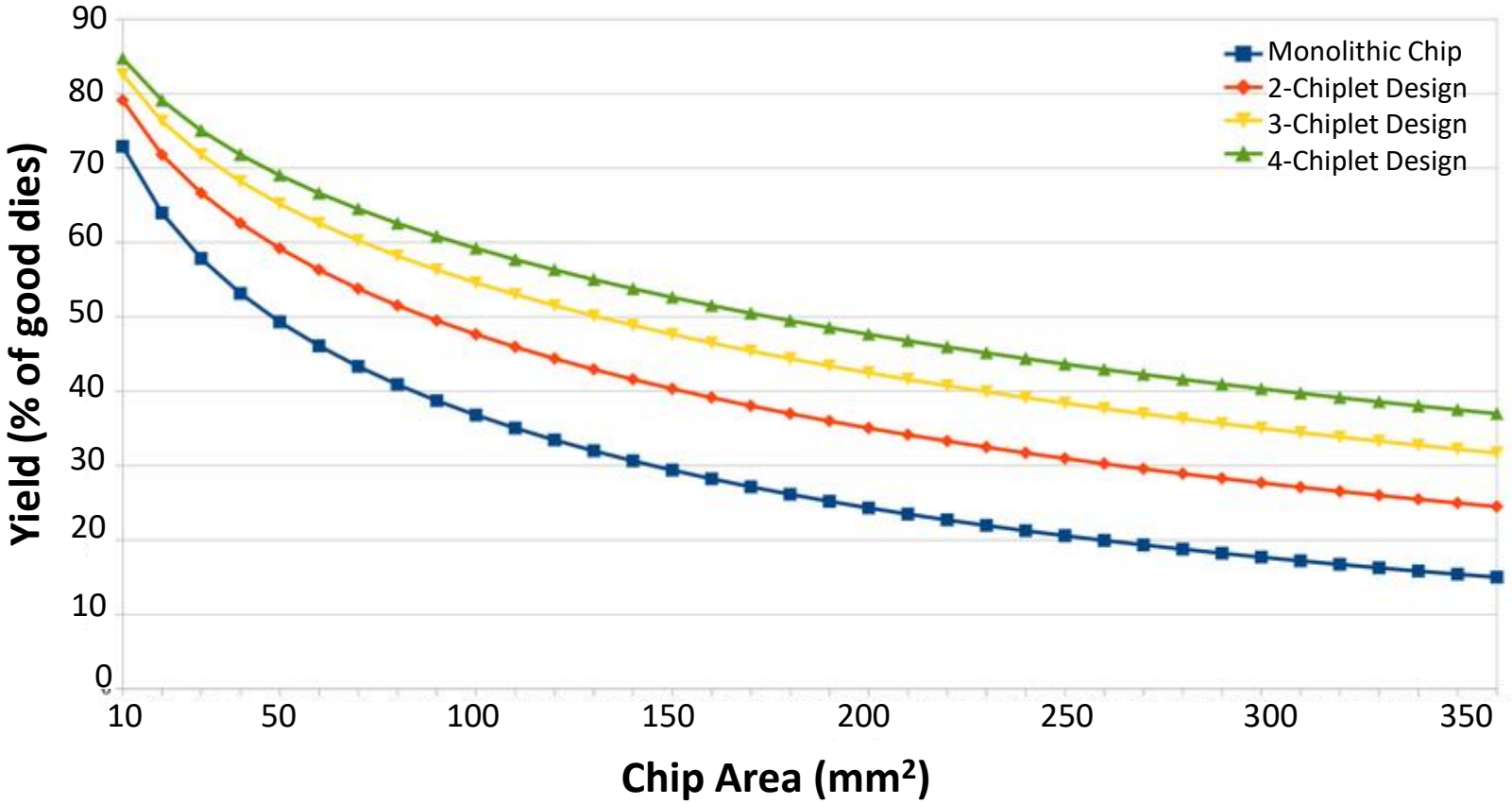
Design Cost for Advanced Nodes in Semiconductors



It will take another $1 billion for 5nm process development.

Sources: International Business Strategies

Yield (Cost) per Wafer vs. Chip Size for SoC and Chiplets



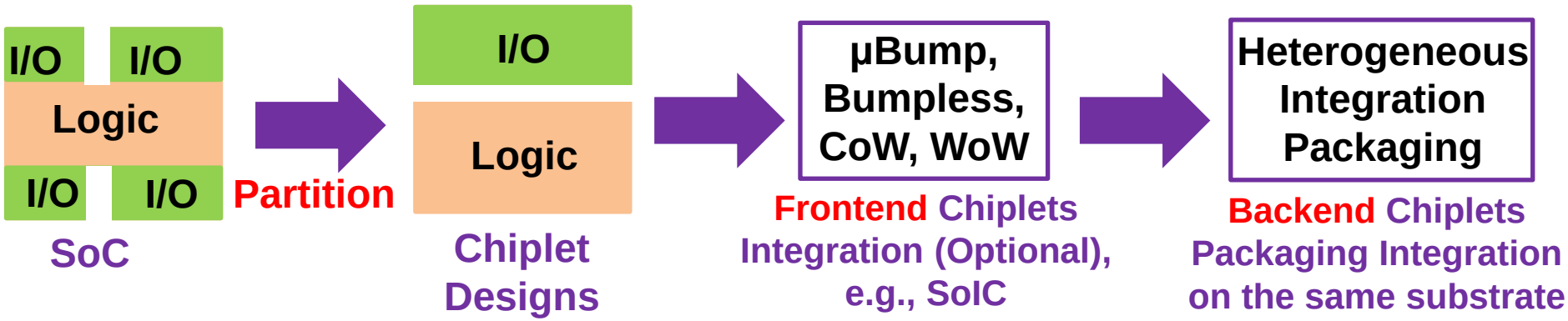
Sources: https://en.wikichip.org/wiki/chiplet, March 27, 2020.

Chiplet Design and Heterogeneous Integration Packaging

- **Chip partition and integration**
- **Chip split and integration**
- **Multiple System and Integration**

Chiplet Design and Heterogeneous Integration Packaging

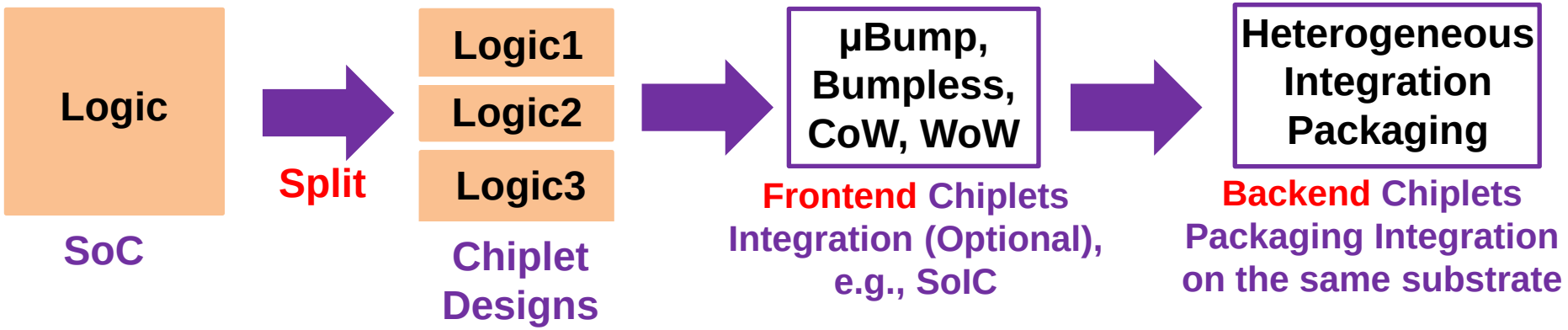
Chip partition and integration (Driven by cost and technology optimization)



Semiconductor Advanced Packaging, Springer, 2021

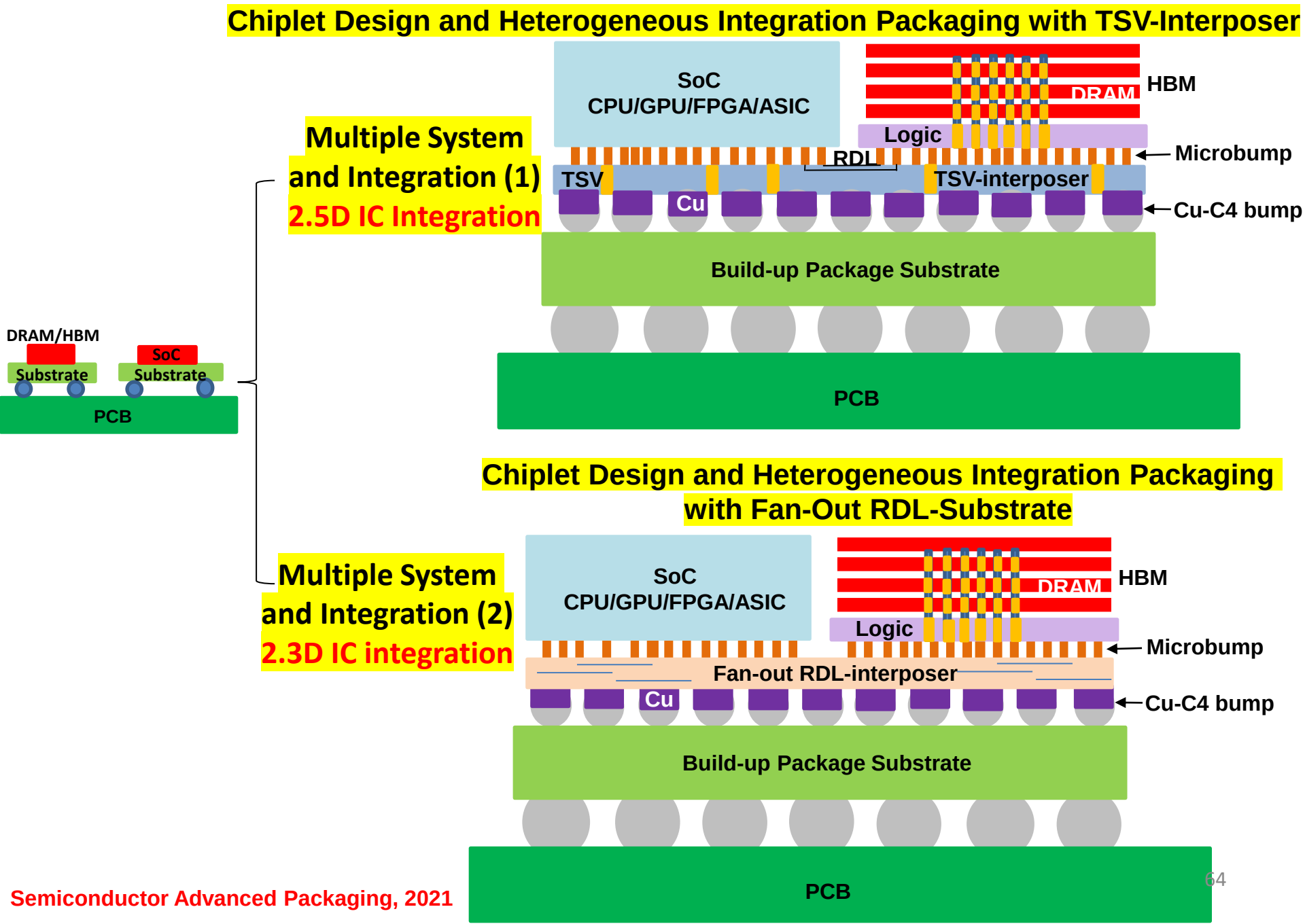
Chiplet Design and Heterogeneous Integration Packaging

Chip split and integration (Driven by cost and yield)



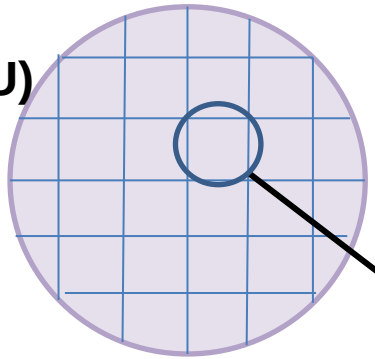
Semiconductor Advanced Packaging, Springer, 2021

Chiplet Design and Heterogeneous Integration Packaging



Chiplet Design and Heterogeneous Integration Packaging

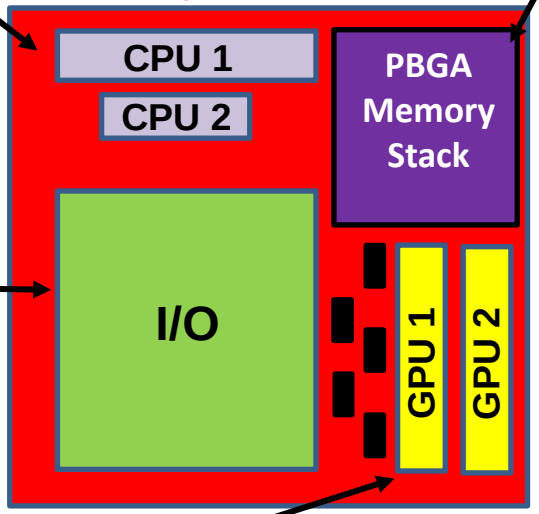
- Chip (CPU)
- FAB-1
- 5nm
- 12”-wafer



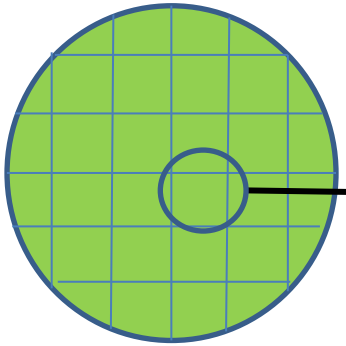
Chip (CPU)

Heterogeneous integration or SiP

Packaged memory stack

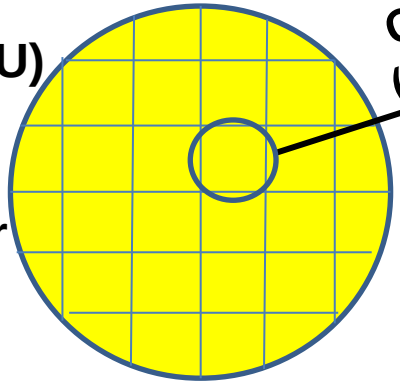


- Chip (I/O)
- FAB-2
- 90nm
- 8”-wafer



Chip (I/O)

- Chip (GPU)
- FAB-3
- 7nm
- 12”-wafer



Chip (GPU)

- Time-to-market
- Less IP issues
- Flexibility
- Low cost alternative than SoC
- Optimized signal integrity and power
- Better thermal performance

Heterogeneous integration uses packaging technology to integrate dissimilar chiplets, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.

Heterogeneous Integration, Springer, 2019

Chiplet Design and Heterogeneous Integration Packaging Comparing with SoC: Advantages and Disadvantages

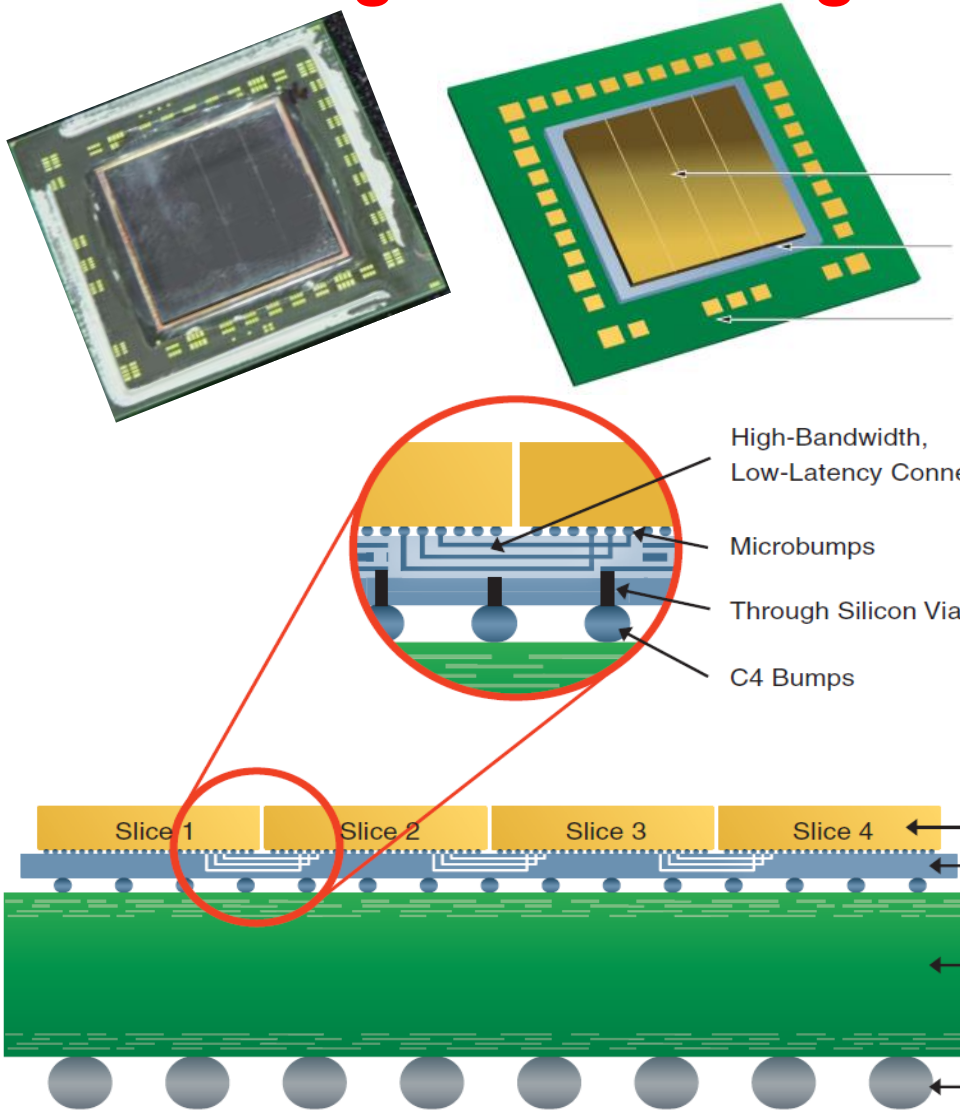
- The key advantages of chiplets heterogeneous integration are:
  - (1) yield improvement (lower cost) during manufacturing;
  - (2) faster time-to-market;
  - (3) cost reduction during design;
  - (4) better thermal performance;
  - (5) reusable of IP;
  - (6) modularization.

- The key disadvantages are:
  - (1) additional area for interfaces;
  - (2) higher packaging costs;
  - (3) more complexity and design effort;
  - (4) past methodologies are less suitable for chiplets.

Examples on Chiplet Design and Heterogeneous Integration Packaging

- Xilinx
- AMD
- Intel
- TSMC
- Nvidia
- Samsung

Xilinx's Chiplet Design and Heterogeneous Integration Packaging



For better manufacturing yield (to save cost), a very large SoC has been split into 4 smaller chips.

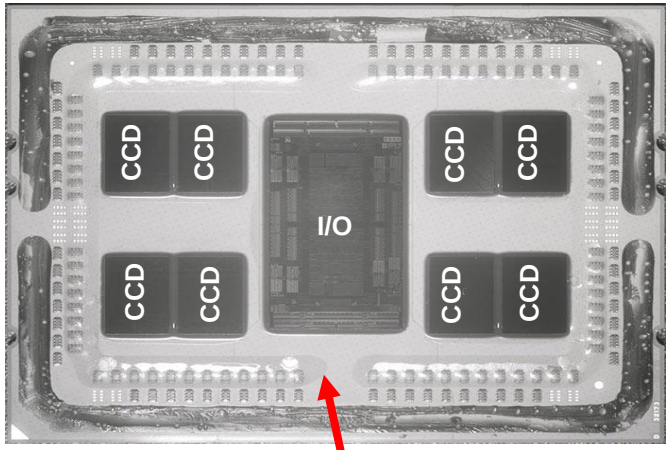
The key function of the RDLs on the interposer is to perform lateral communications between the chips.

Shipped in 2013

AMD's Chiplet Design and Heterogeneous Integration Packaging

Extreme-performance yield computing (EPYC)

2D IC Integration



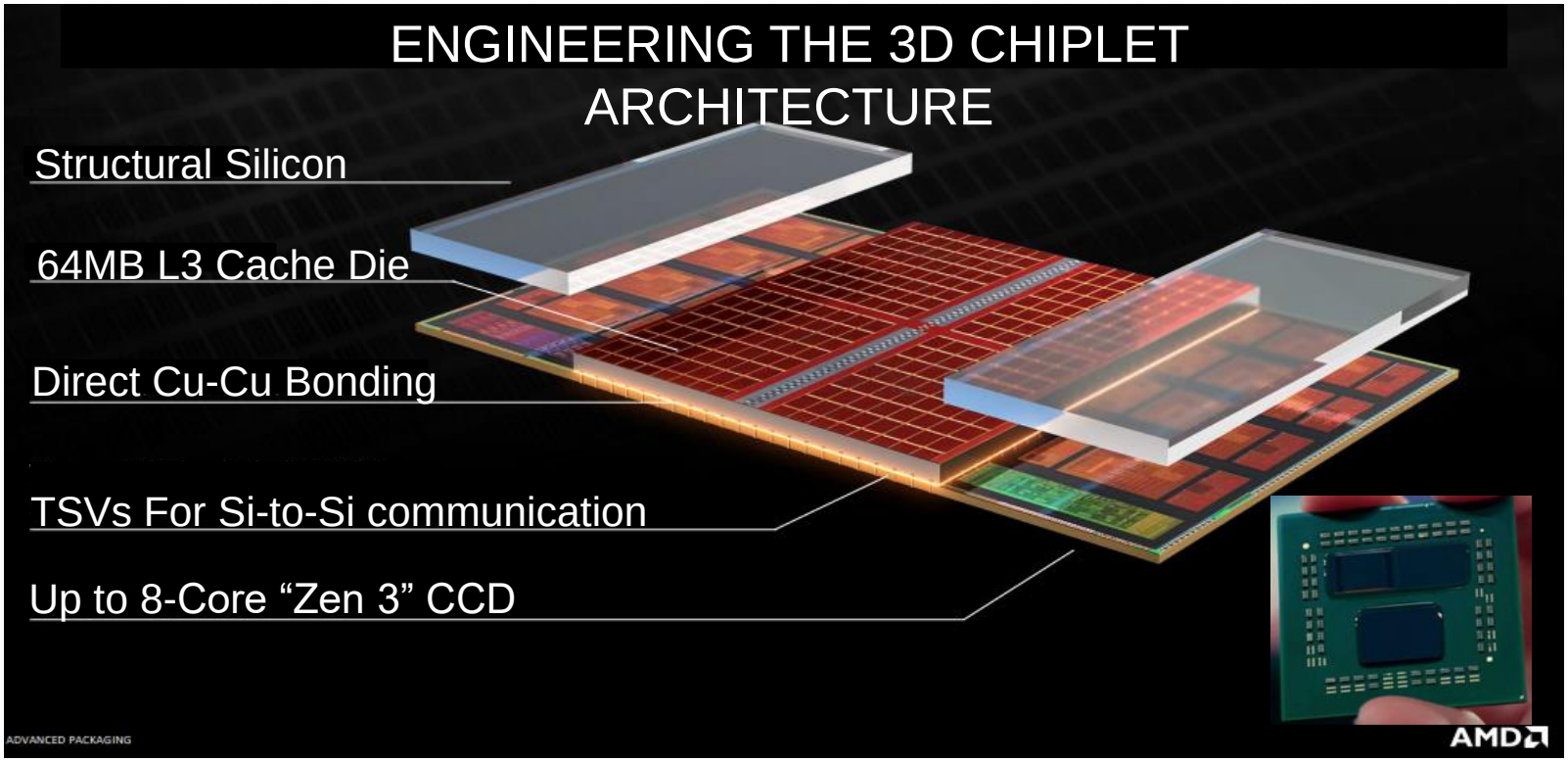
9-2-9 package substrate

- **The I/O and CCD (core complex die or CPU compute die) are partitioned**
- **The CCD is split into two chiplets (7nm process technology)**
- **The I/O chip is with 14nm process technology**

Shipped in 2019

AMD's Future Chiplet Design and Heterogeneous Integration Packaging

3D IC Integration



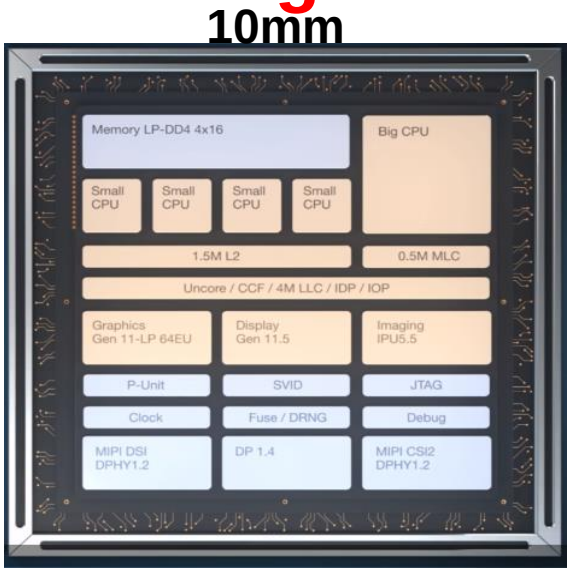
- **AMD's RYZEN 9 5900X Prototype chip for gaming**
- **Same 7nm process technology as RYZEN, but using 3D chiplet copper-to-copper bumpless hybrid bonding**

IEEE Hot Chip Conference, August 2021

Intel's Chiplet Design and Heterogeneous Integration Packaging

Lakefield

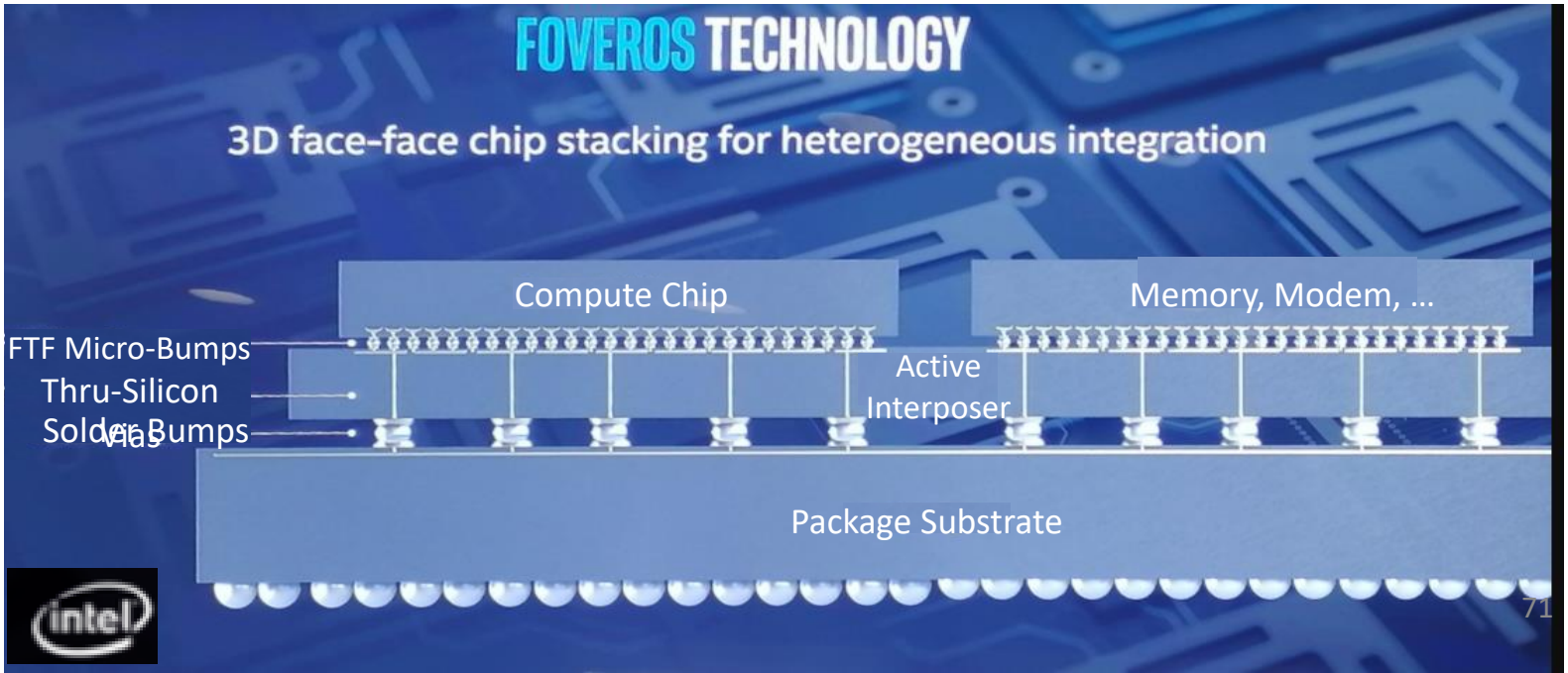
(a)



3D IC Integration

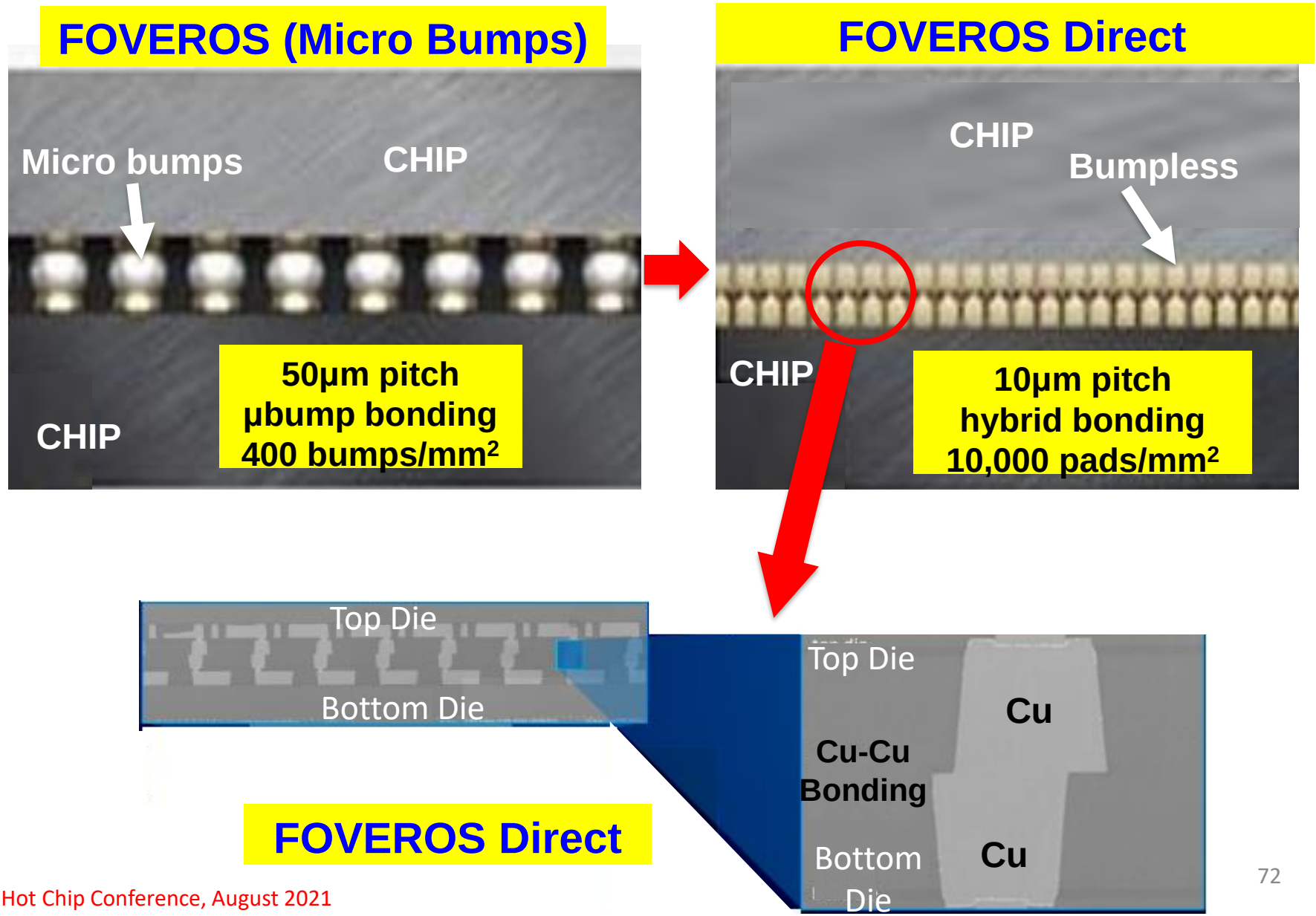
- **The memory and graphics are partitioned**
- **The large CPU is split into 5 smaller CPUs (10nm process technology)**
- **All the tiles (or chiplets) are attached on an active interposer**

(b)

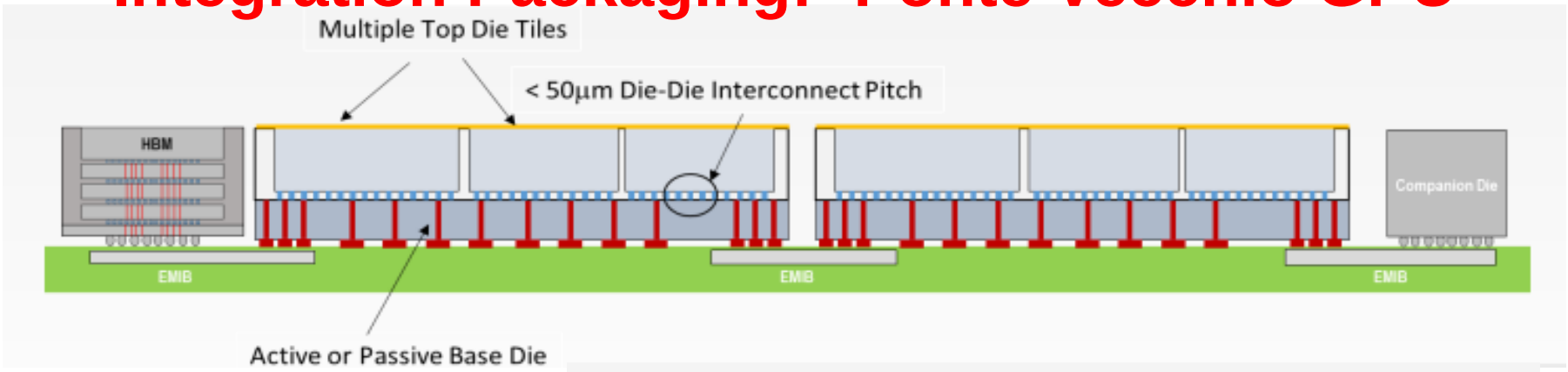


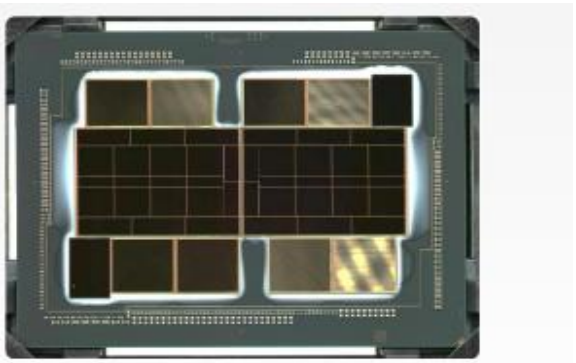
Shipped in 2020

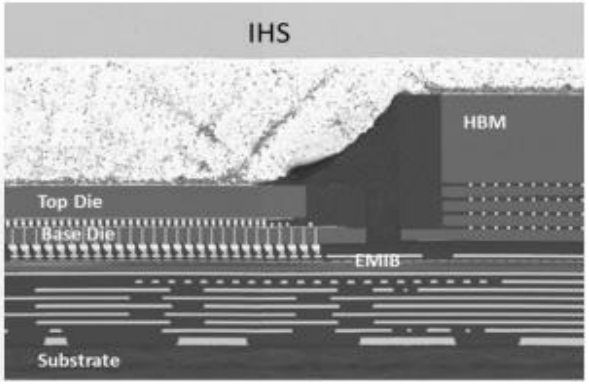
Intel's Future Chiplet Design and Heterogeneous Integration Packaging:- FOVEROS Direct



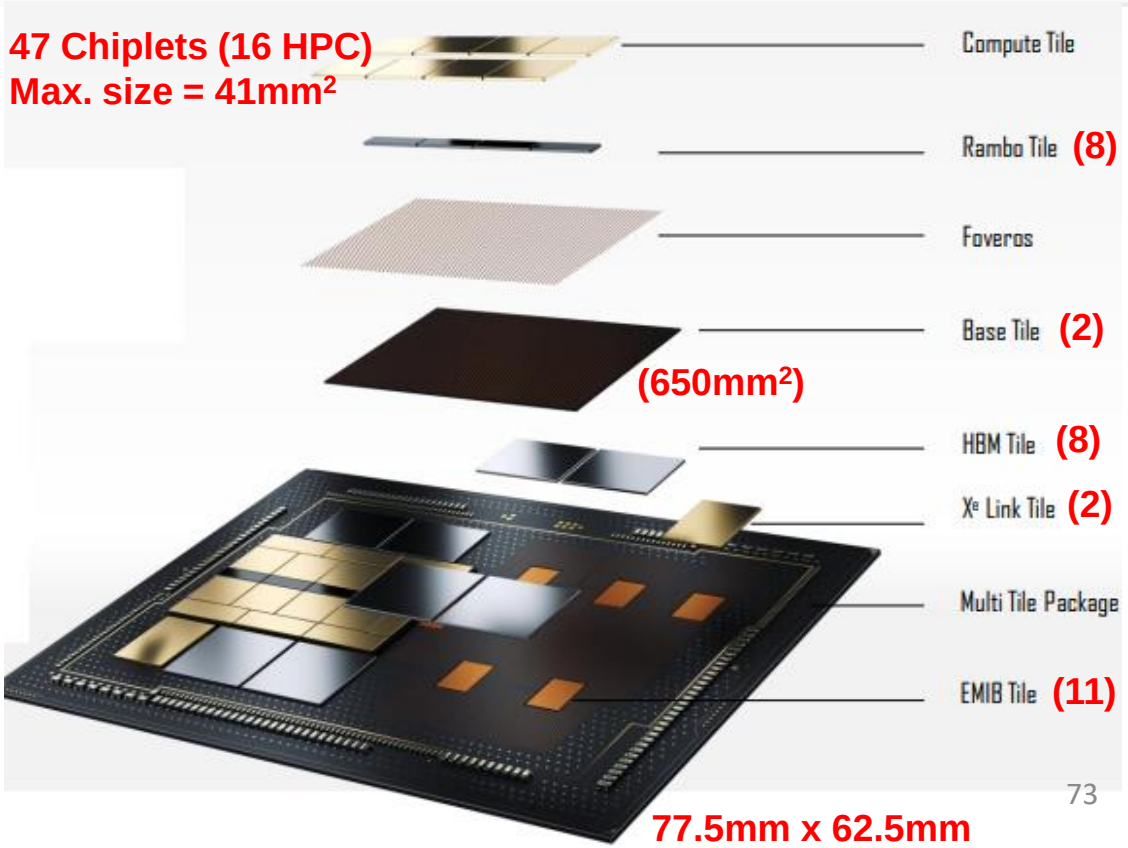
Intel's Future Chiplet Design and Heterogeneous Integration Packaging:- Ponte Vecchio GPU





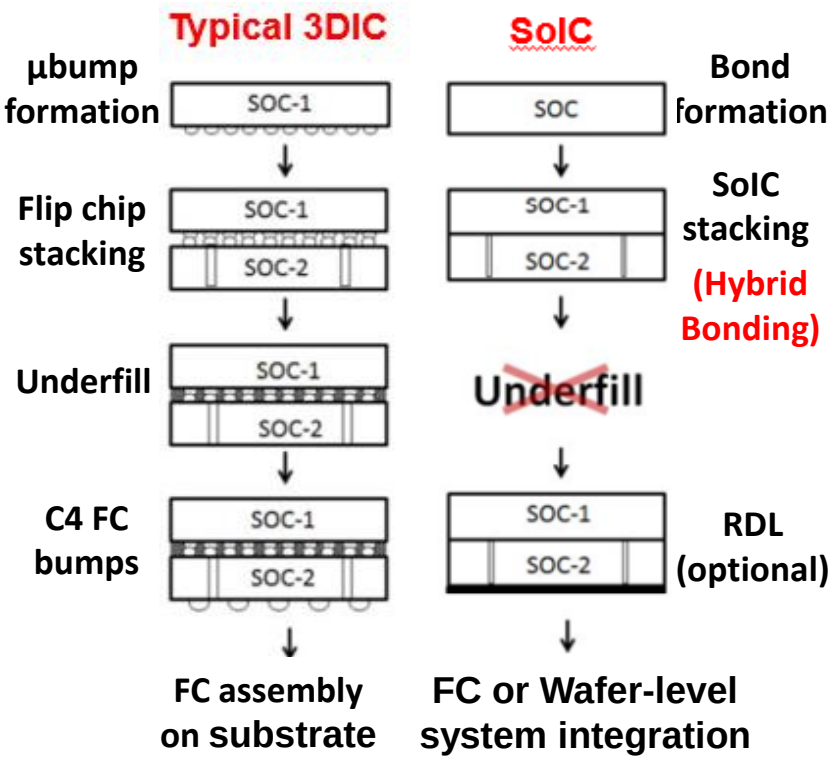


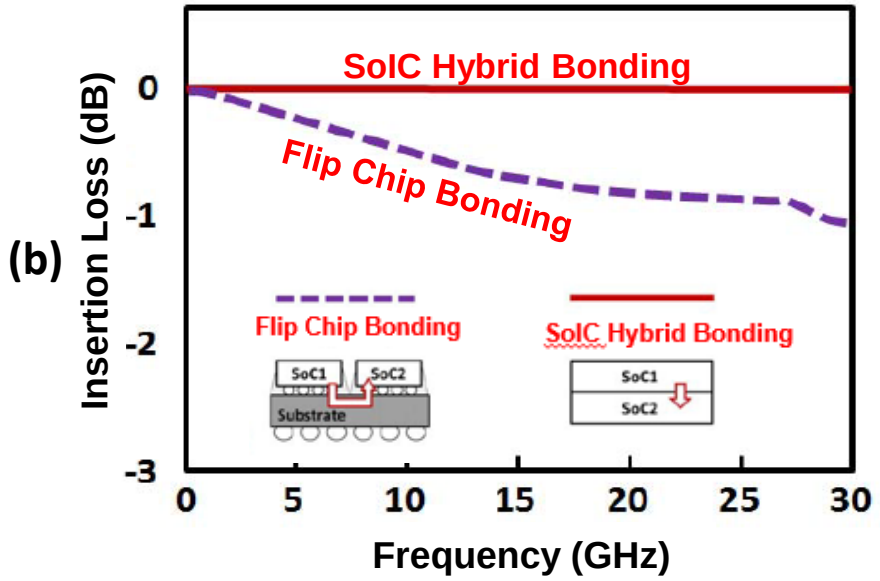
- 47 Chiplets (16 HPC)
- Max. size = 41mm²

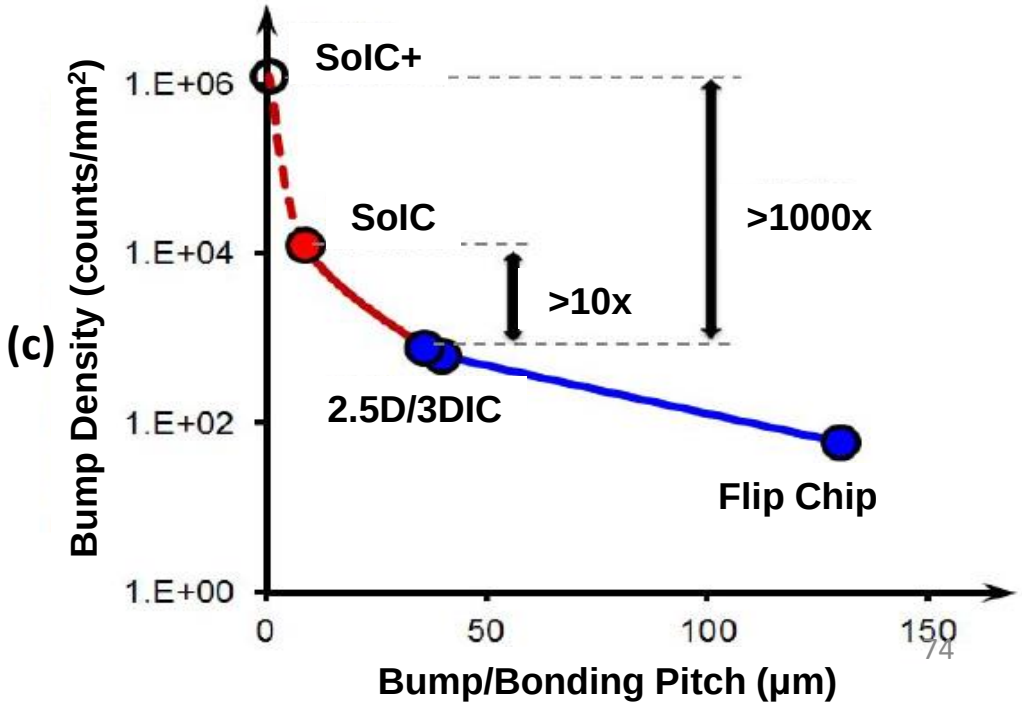


IEEE Hot Chip Conference, August 2021

TSMC's Chiplets Bonding, Density, and Performance



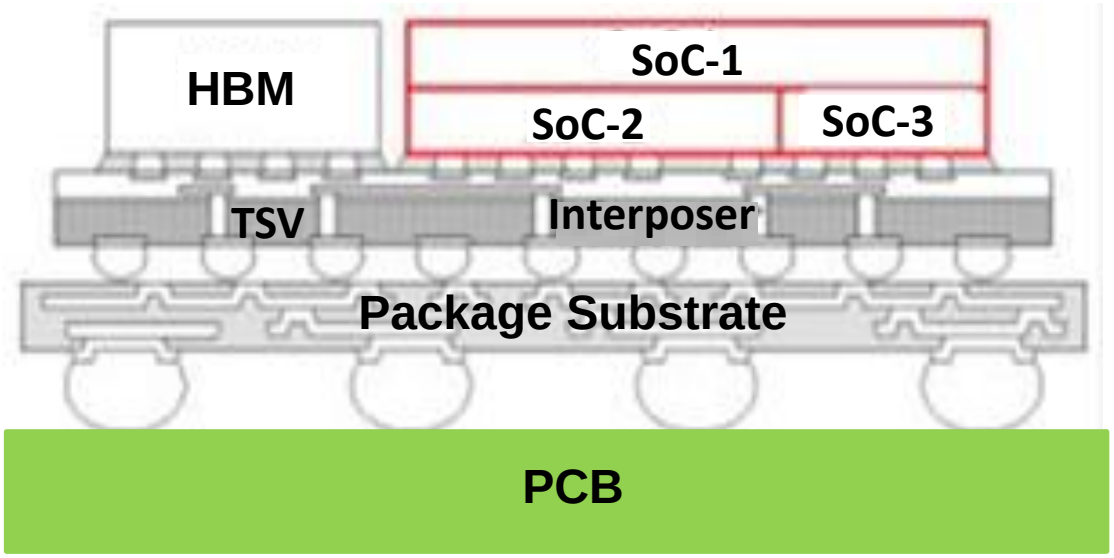




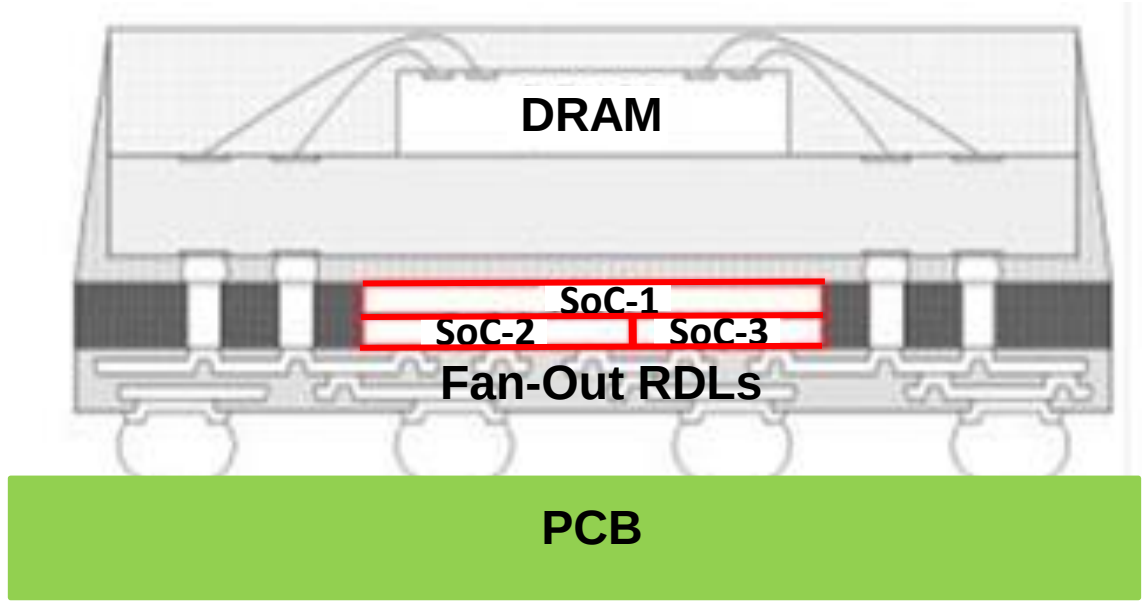
IEEE/ECTC2020 and 2021

TSMC's Chiplet Design and Heterogeneous Integration Packaging

CoWoS with SoIC



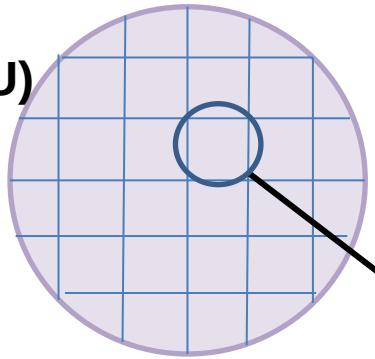
InFO PoP with SoIC



IEEE/ECTC2020 and 2021

Classification of Heterogeneous Integration Packaging

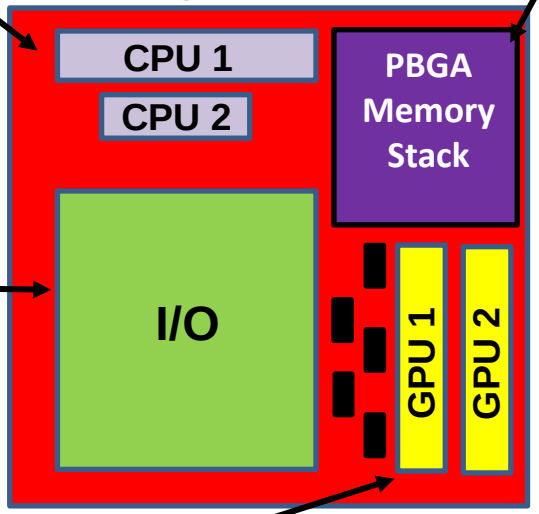
- Chip (CPU)
- FAB-1
- 5nm
- 12”-wafer



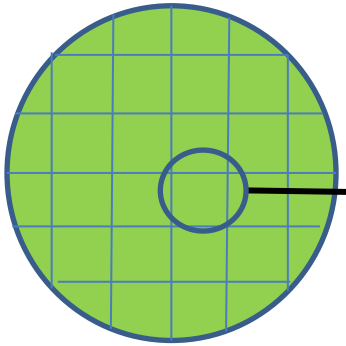
Chip (CPU)

Heterogeneous integration or SiP

Packaged memory stack

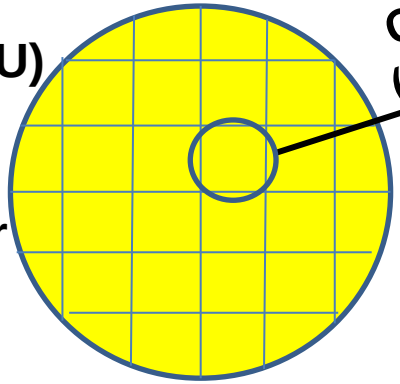


- Chip (I/O)
- FAB-2
- 90nm
- 8”-wafer



Chip (I/O)

- Chip (GPU)
- FAB-3
- 7nm
- 12”-wafer



Chip (GPU)

- Time-to-market
- Less IP issues
- Flexibility
- Low cost alternative than SoC
- Optimized signal integrity and power
- Better thermal performance

Heterogeneous integration uses packaging technology to integrate dissimilar chiplets, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.

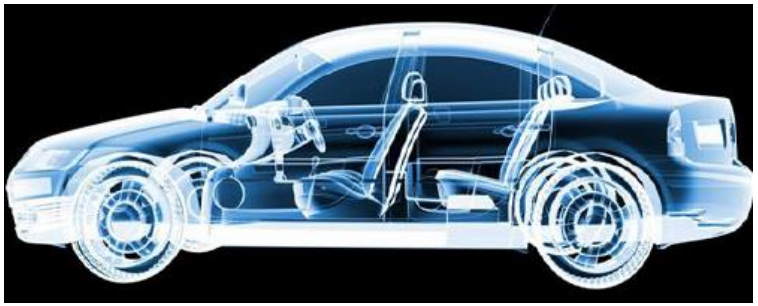
Heterogeneous Integration, Springer, 2019

Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations on Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposers
- Heterogeneous Integrations on Fan-Out RDL Substrates
- Heterogeneous Integrations on Ceramic Substrates

Amkor Automotive SiP (System-in-Package)

- Large singulated body SiP
- Infotainment & ADAS
- Autonomous driving
- Computers in a car
- Increasing trend in designs



42.5 x 42.5 mm, Infotainment, Processor + DDR

55 x 72 mm, Network Switch, ASIC + Memory

Heterogeneous Integration on organic-substrate

The Apple Watch is SiP and was Assembled by ASE (Universal Scientific Industrial – Shanghai)

Apple Application Processor with SK Hynix LPDDR4 SDRAM

Broadcom BCM15920 Custom Sensing ASIC

Broadcom BCM59356 Wireless Charging Power Management Unit

Apple 338S00348W2 Chip

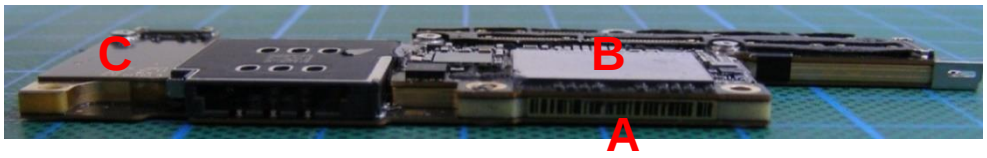
Toshiba NAND Flash

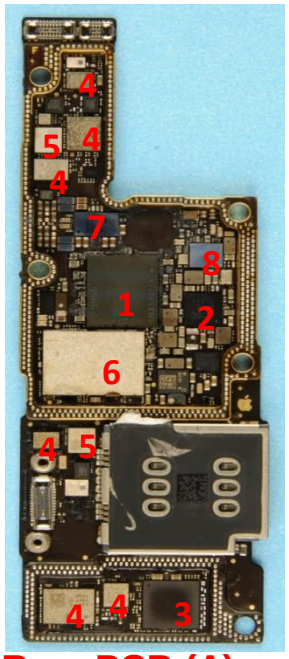
Qualcomm MDM9635M LTE Modem with Samsung K4P1G324EH SDRAM

Apple/Dialog PMIC

Qualcomm PMD9645 PMIC

Three Substrate-Like PCBs (SiPs) in iPhone

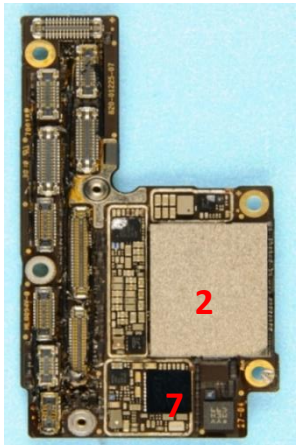


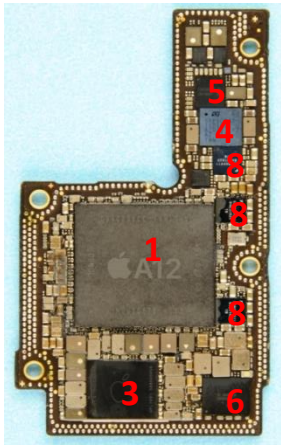


[1] Intel Baseband Chipset
[2] Intel PM IC
[3] Intel RF Transceiver
[4] Skyworks RF FEM
[5] Murata RF FEM (front-end module)
[6] USI WiFi/BT Module
[7] Broadcom Wireless Charger
[8] NXP NFC Controller

Rear PCB (A)

- 8L HDI, 4mSAP layers, 16cm²
- Single-Sided Assembly
- Baseband, RF, WiFi/BT
- All components face inward

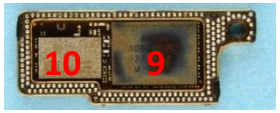




[1] Apple A12 Chipset
[2] Flash Memory
[3] Power Manager
[4] ST Power Manager
[5] Power Manager
[6] TI Battery Charger
[7] Audio Codec
[8] Audio Amplification
[9] Avago RF FEM
[10] Skyworks RF FEM

Front PCB 1 (B)

- 10L HDI, 6 mSAP layers, 10cm²
- Double-Sided Assembly
- A12 CPU, Memory, Connectors
- A12 CPU faces inward



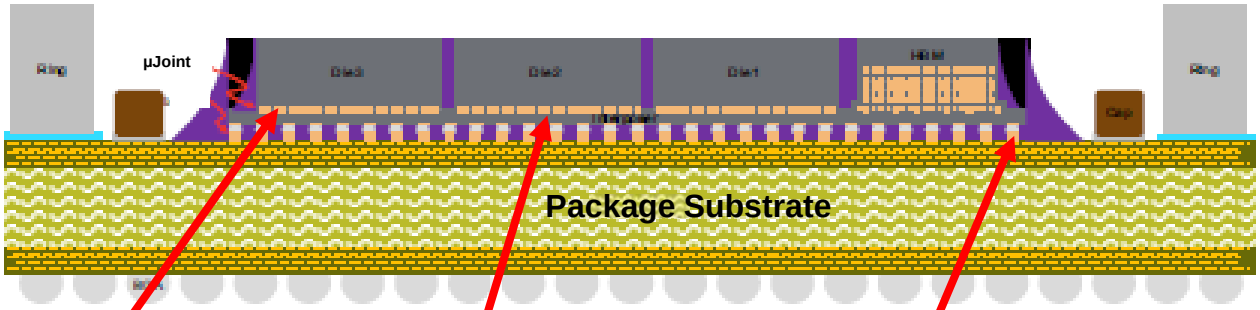
Front PCB 2 (C)

- 6L HDI, 2 mSAP layers, 2cm²
- Double-Sided Assembly
- RF FEM, Connectors
- RF FEM face inward

Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations on Silicon Substrates (Passive TSV-Interposers and Active TSV-Interposers)
- Heterogeneous Integrations on TSV-less Interposers
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

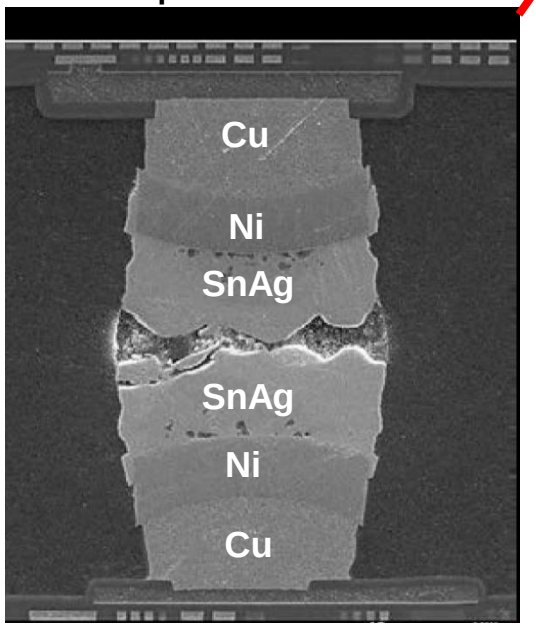
Xilinx's HPC Applications Driven by AI and 5G (Passive TSV-Interposer)

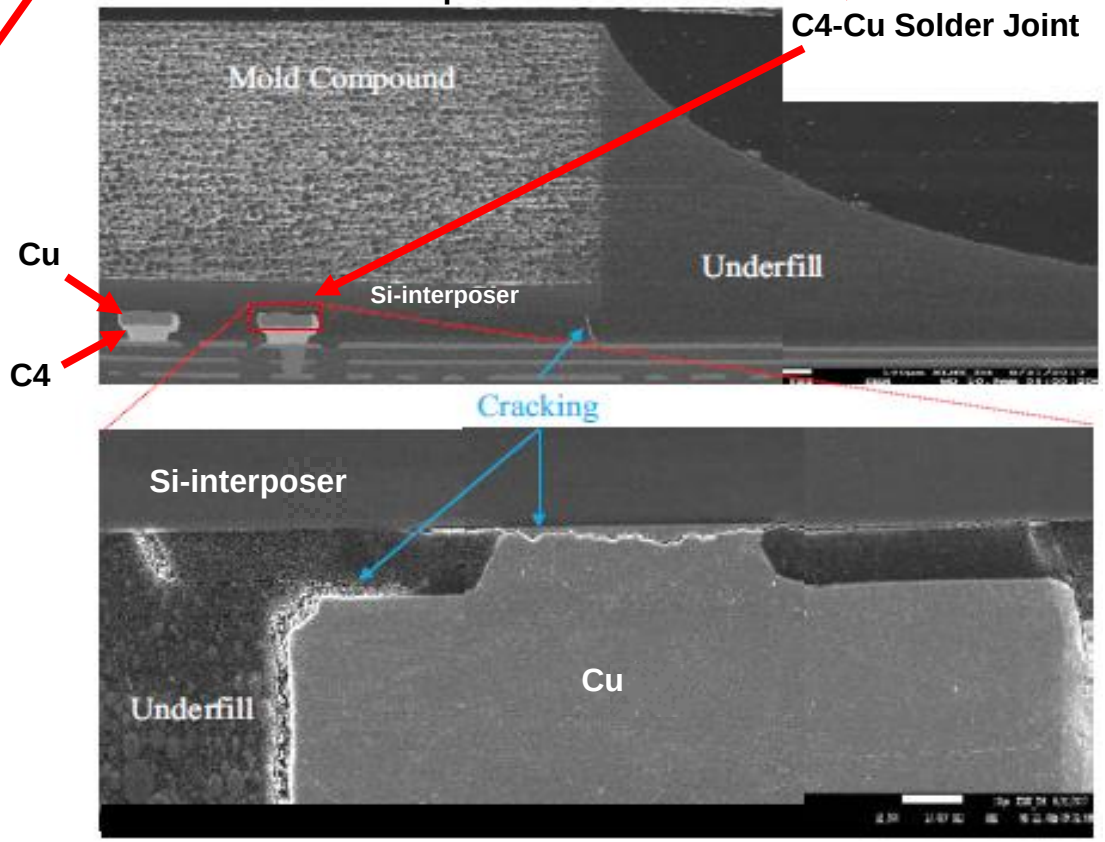


TSV-Interposer

C4-Cu Solder Joint

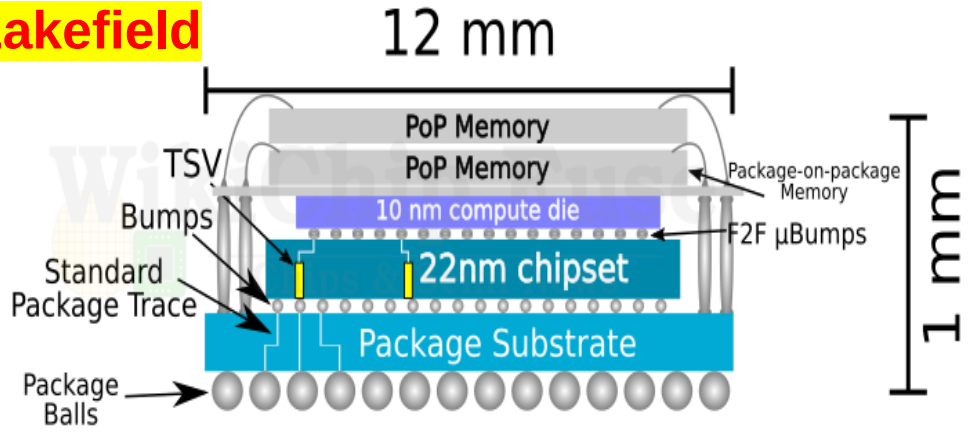
µSolder Joint

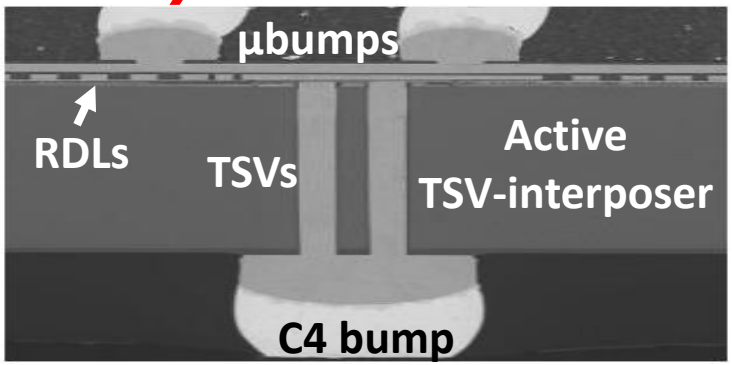




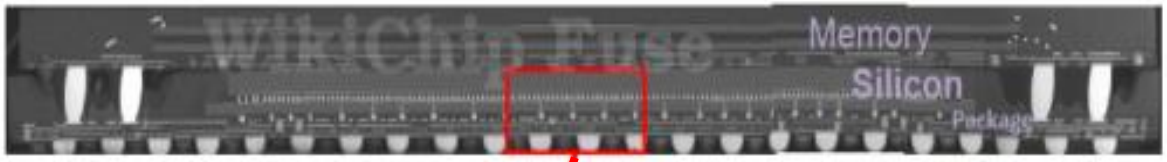
Intel 3D IC Integration – FOVEROS Technology (Active TSV-Interposer)

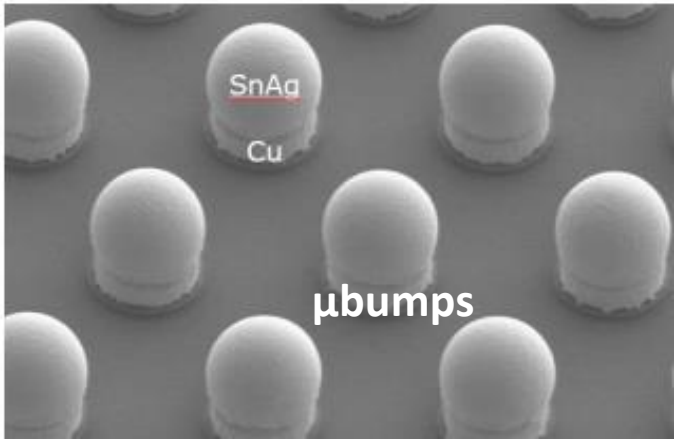
Lakefield



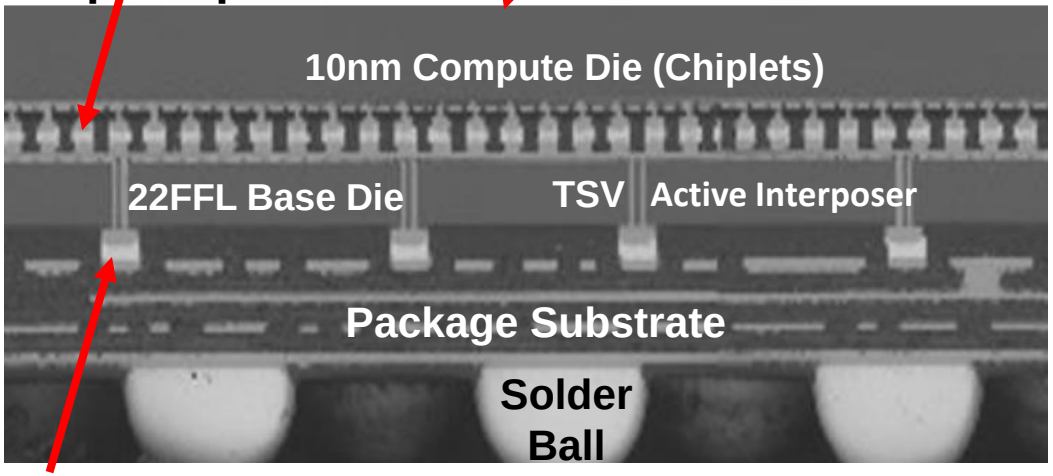


3D IC Integration

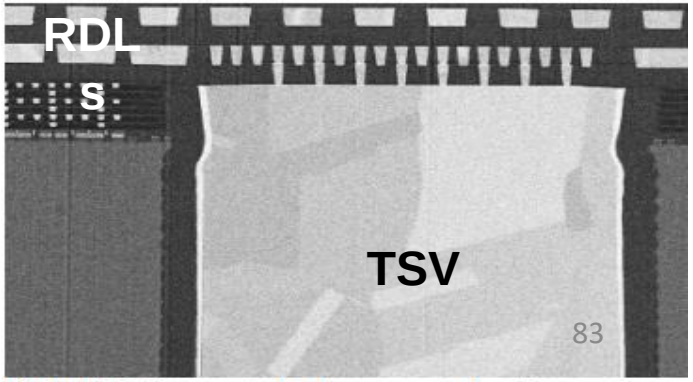




µbump



C4 bump



Semiconductor Advanced Packaging, 2021

Classification of Heterogeneous Integrations

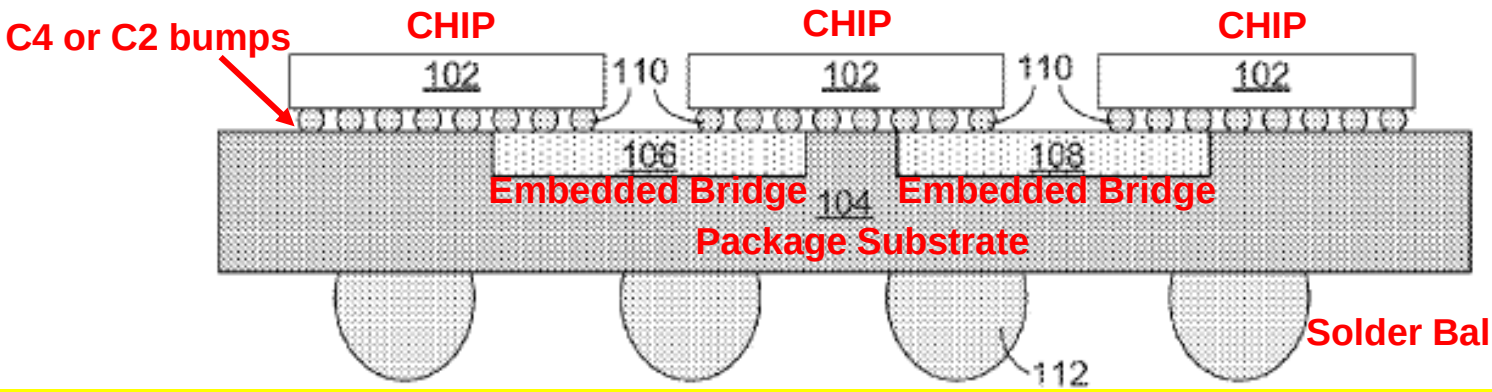
- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposer (e.g., Bridges – lateral communication between chiplets)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

Lateral Communications (Bridges) between Chiplets

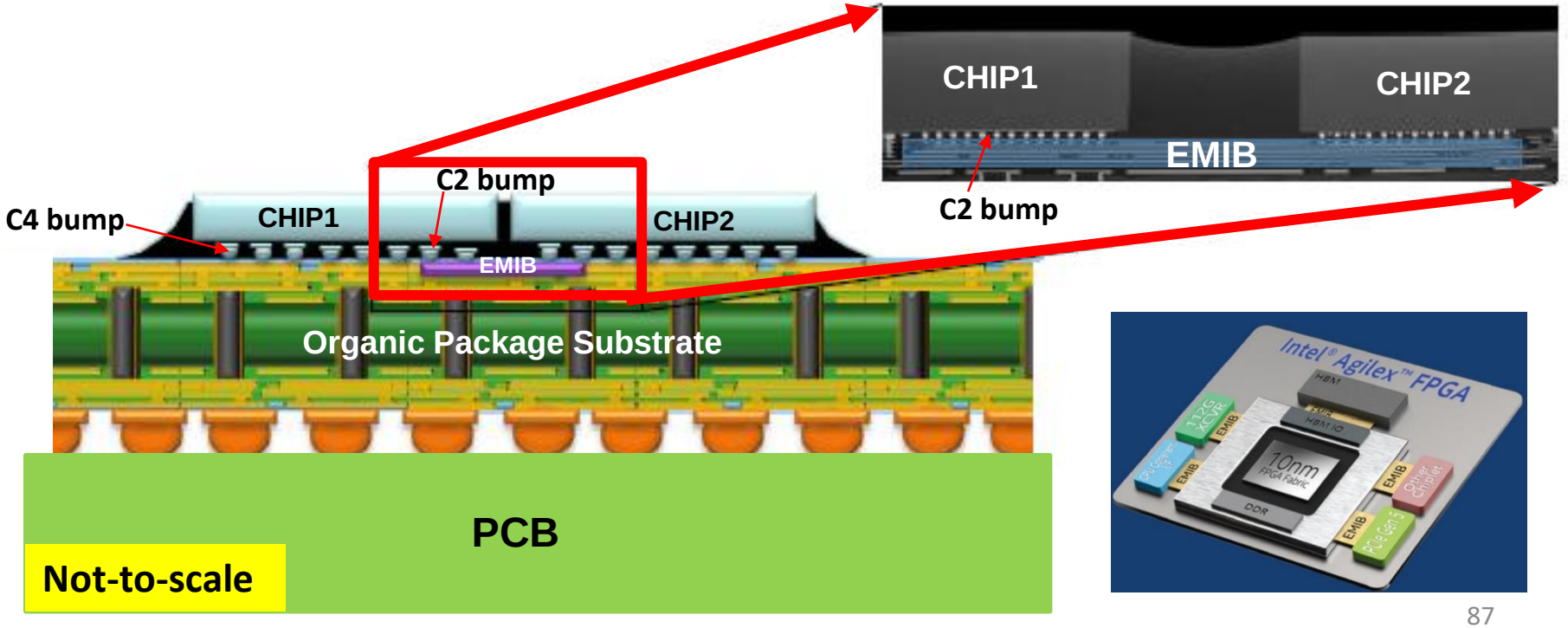
- **Bridge Embedded in Build-up Package Substrate**
- **Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)**
- **Flexible Bridge**

Bridge Embedded in Build-up Package Substrate

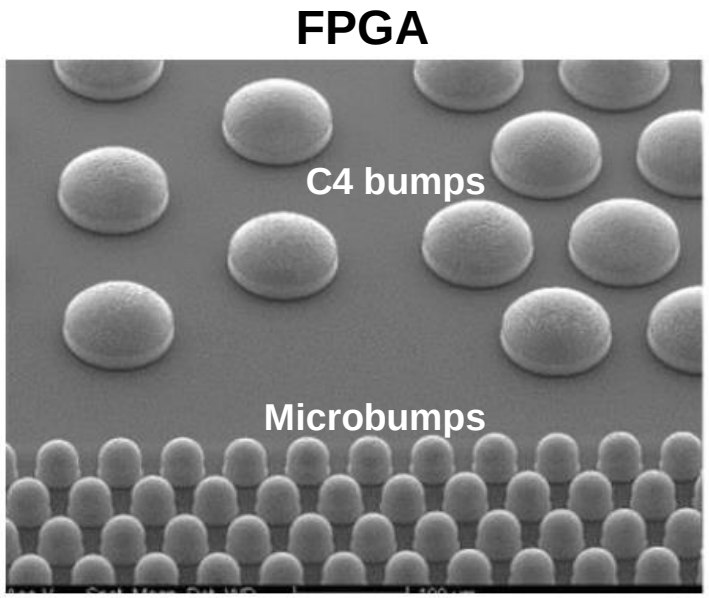
Intel's EMIB Patent and Agilex Module

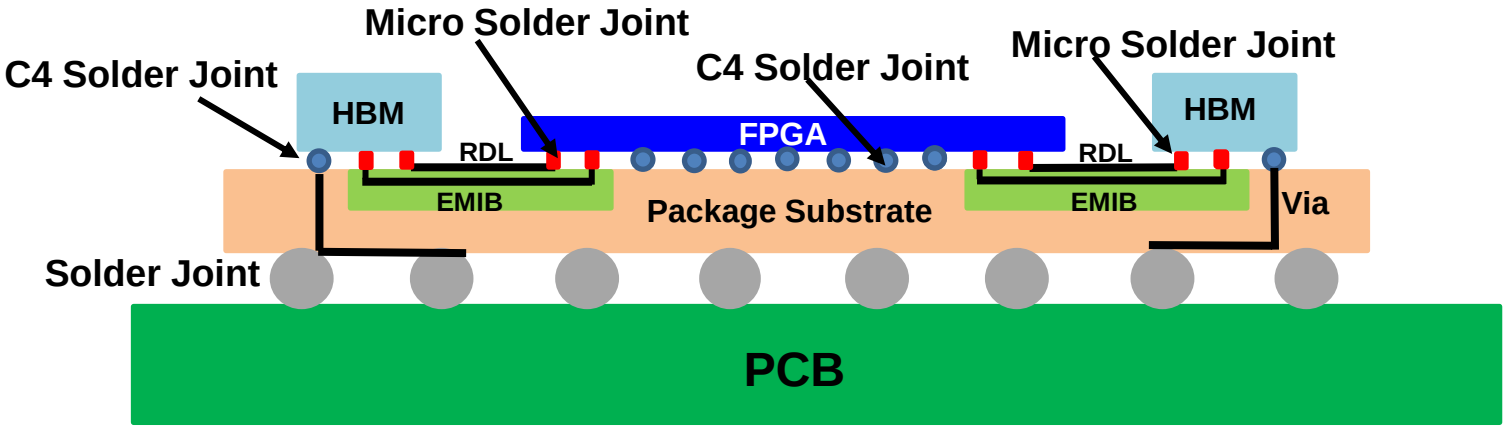


Intel's Embedded Multi-die Interconnect Bridge (EMIB) in package substrate



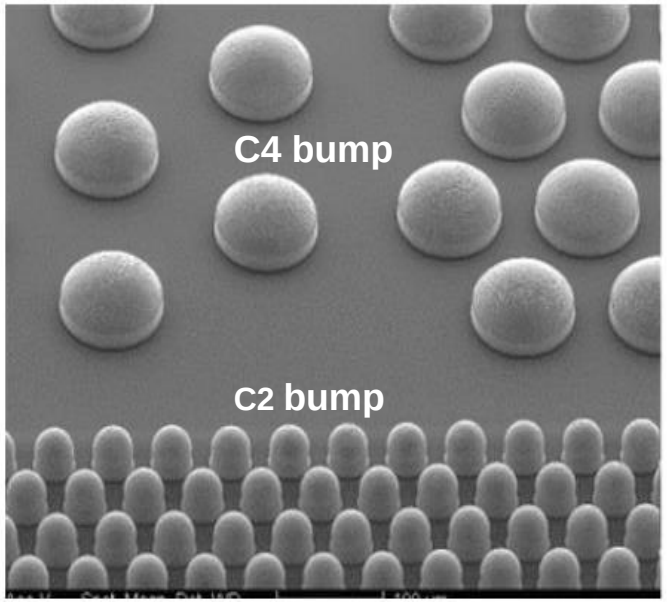
Intel's FPGA (Agilex) with EMIB





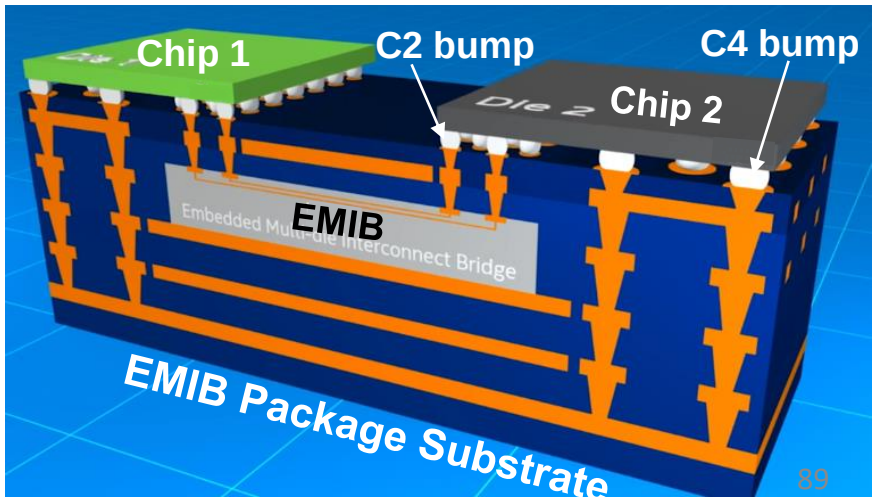
Intel's EMIB (Embedded Multi-die Interconnect Bridge)

C4 (controlled collapse chip connection) bumps and C2 (Cu-pillar + solder cap) bump on chip

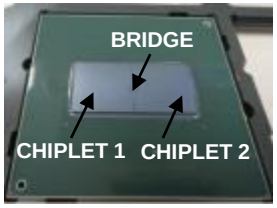


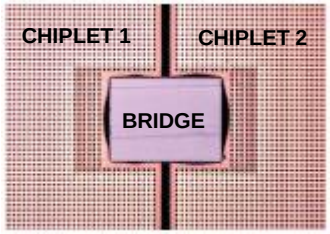
CHIP

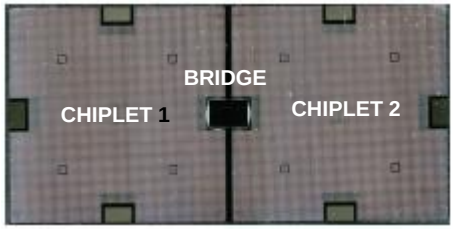
- The minimum metal L/S/H is 2μm.
- The dielectric layer thickness is 2μm.
- The bridge size is from 2mm x 2mm to 8mm x 8mm
- Usually, there are ≤ 4 RDLs.

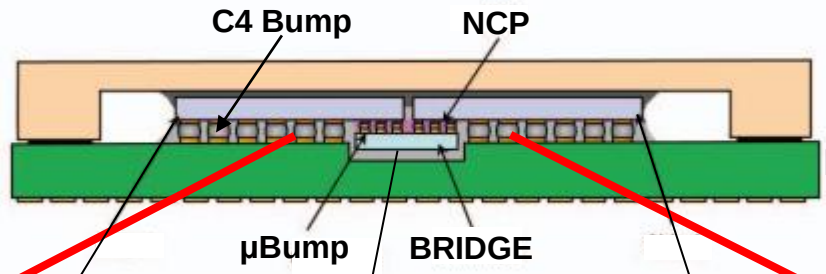


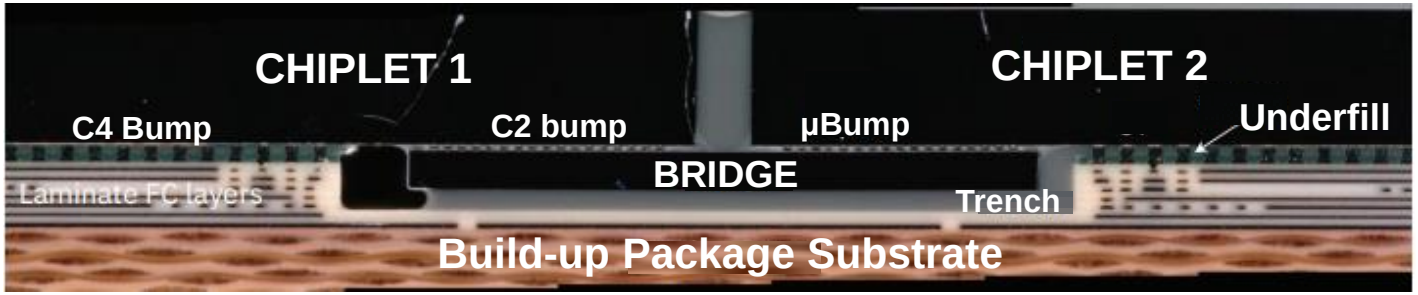
IBM's Direct Bonded Heterogeneous Integration (DBHi) Si Bridge

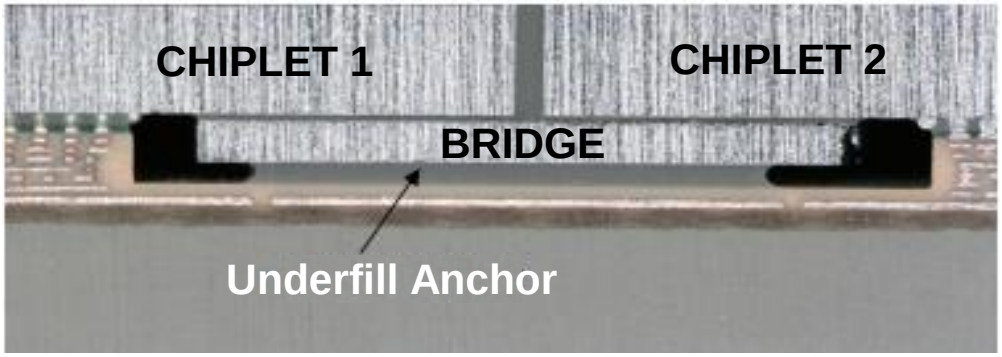


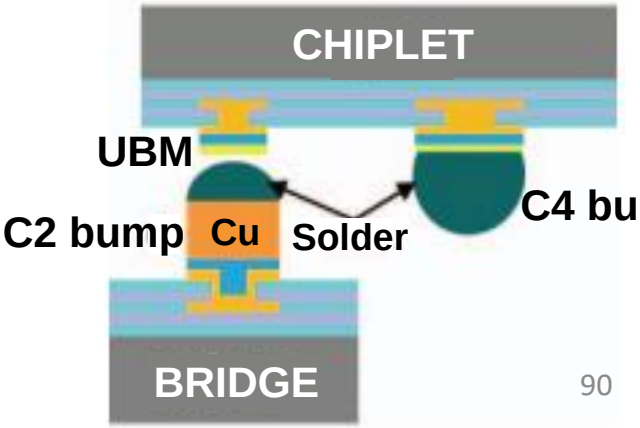








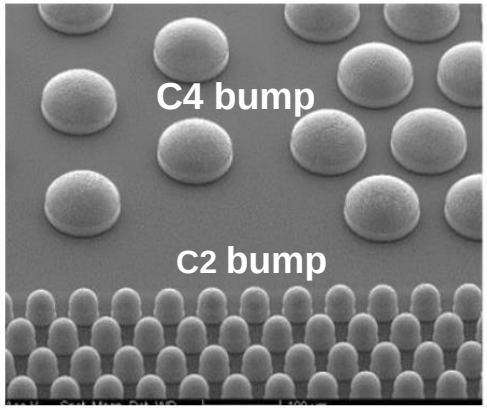




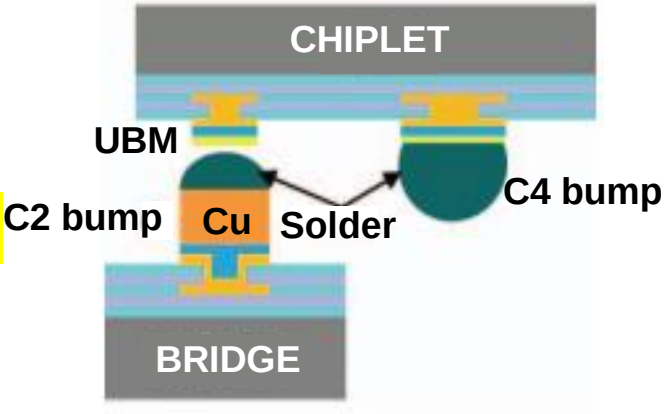
Differences between Intel's EMIB and IBM's DBHi

- For Intel's EMIB, there are two different (C4 and C2) bumps on the chiplets (and there are no bumps on the bridge), while for IBM's DBHi, there are C4 bumps on the chiplets and C2 bumps on the bridge.

EMIB

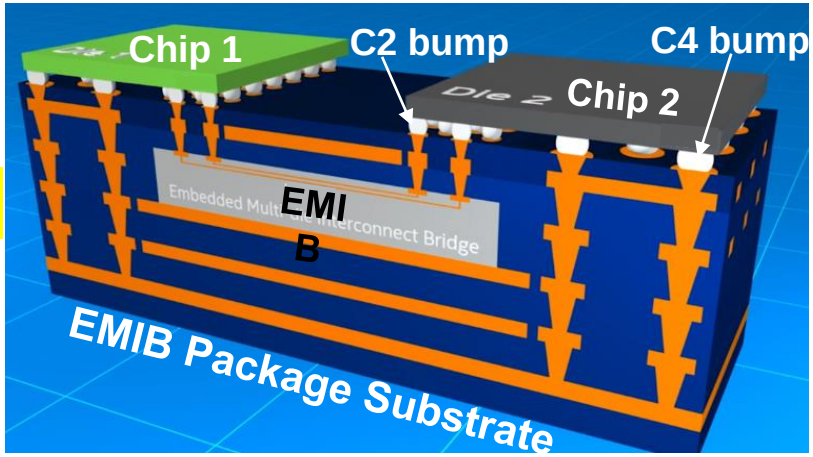


DBHi

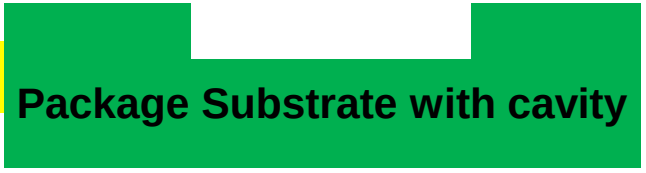


- For Intel's EMIB, the bridge is embedded in the cavity of a build-up substrate with a die-attach material and then laminated with another build-up layer on top. Therefore, the substrate fabrication is very complicated. For IBM's DBHi, the substrate is just a regular build-up substrate with a cavity on top.

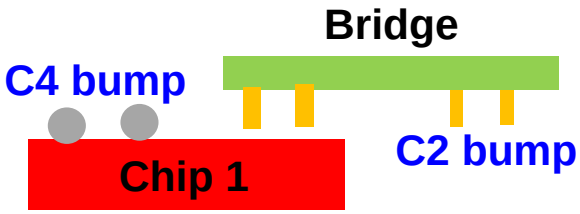
EMIB

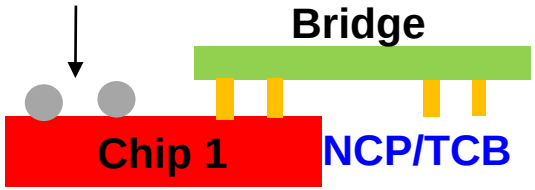


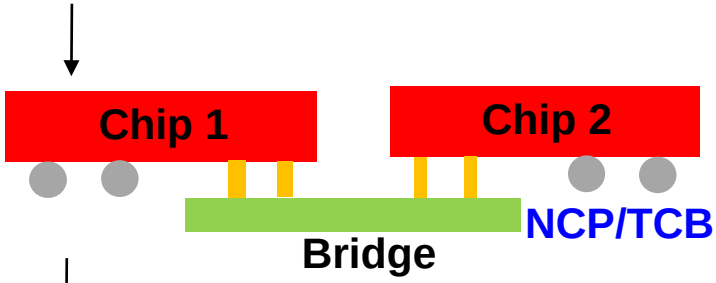
DBHi

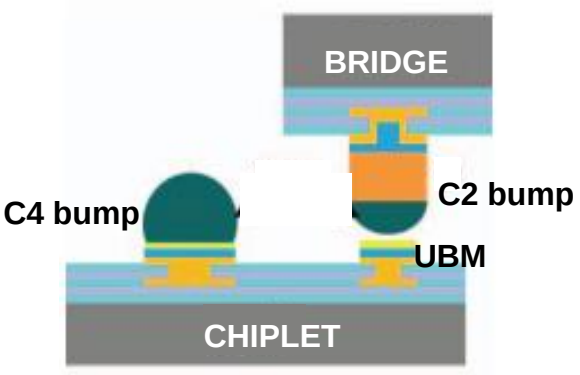


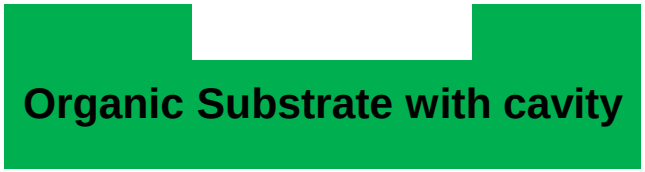
IBM's DBHi Key Process Steps

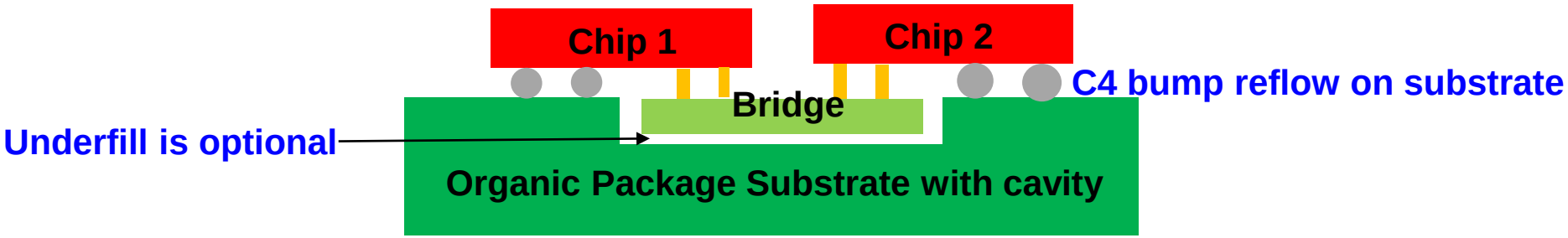






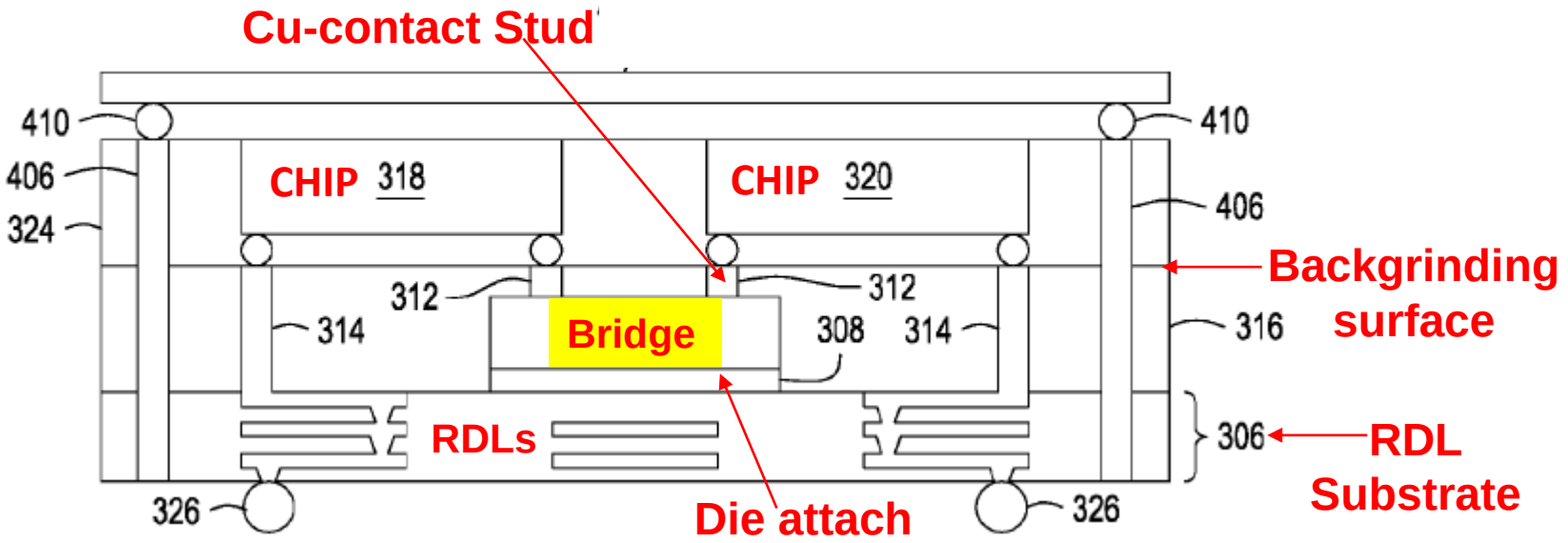






Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)

Applied Materials' Fan-out Chip (Bridge) First Face-up Process

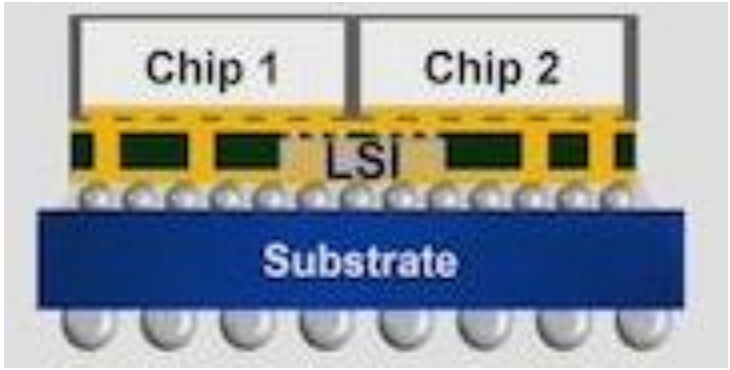


US patent 10,651,126 (filed on December 8, 2017)

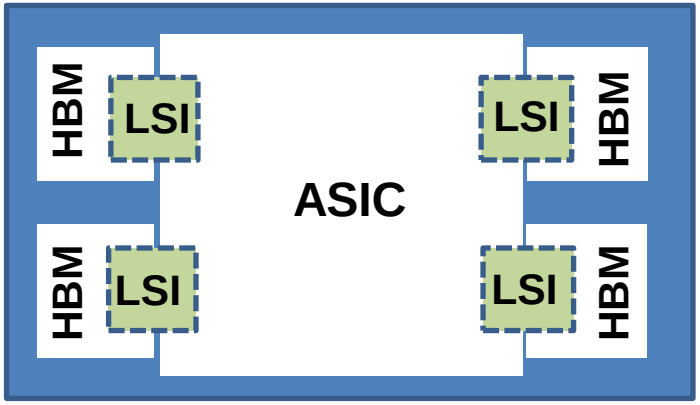
TSMC's LSI (Local Silicon Interconnect)

Fan-out Chip (Bridge) First Face-up Process

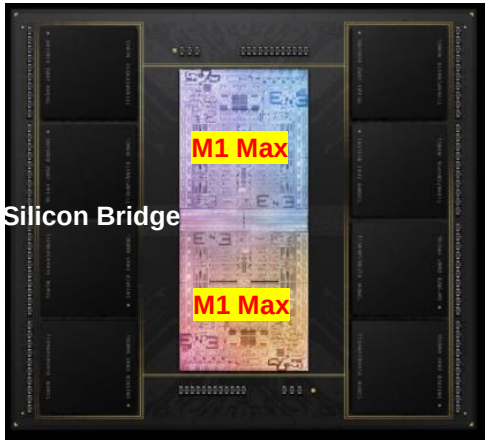
InFO_LSI

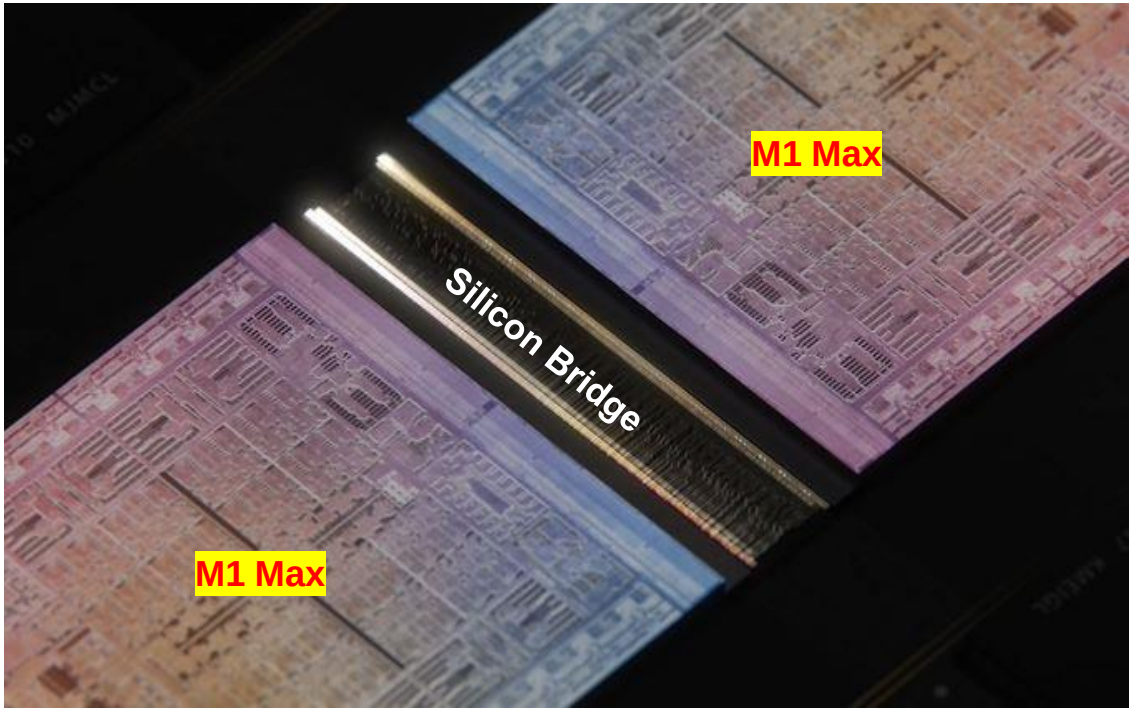


CoWoS_LSI



Apple's UltraFusion
(M1 Ultra = M1 Max + M1 Max + Si Bridge)

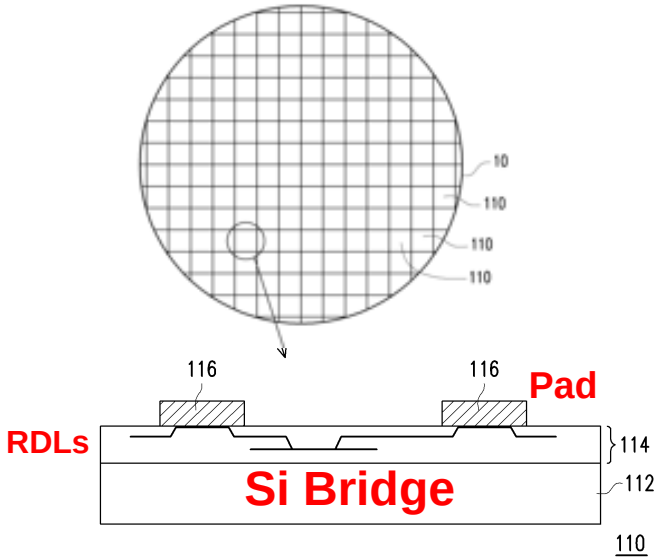


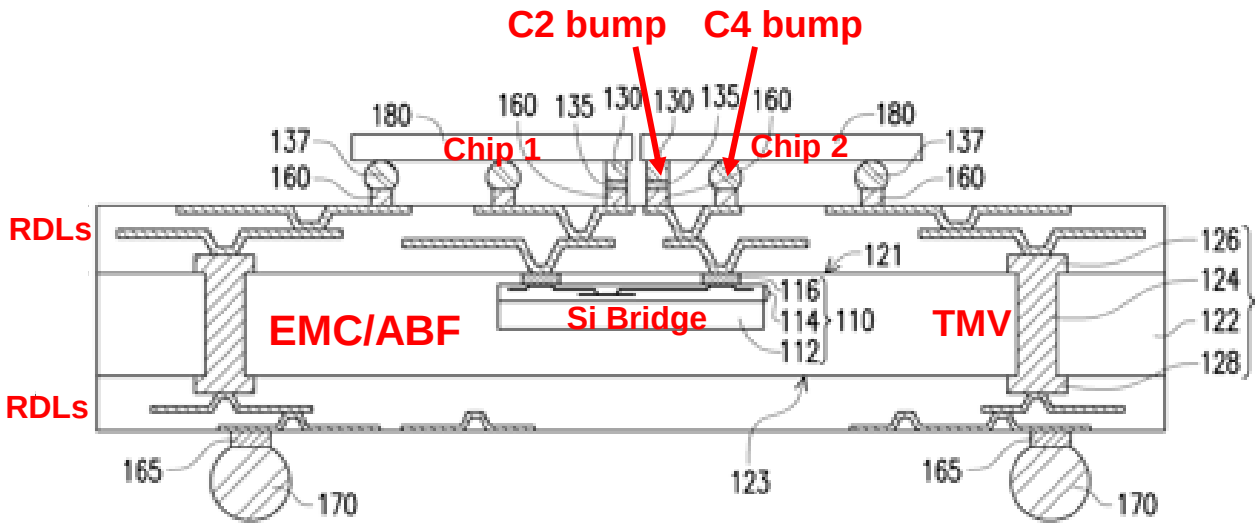


UltraFusion — Apple's innovative packaging architecture that interconnects the die of two M1 Max chips to create a system on a chip (SoC) with unprecedented levels of performance and capabilities

March 8, 2022

Unimicron's Fan-out Chip (Bridge) First Face-down Process

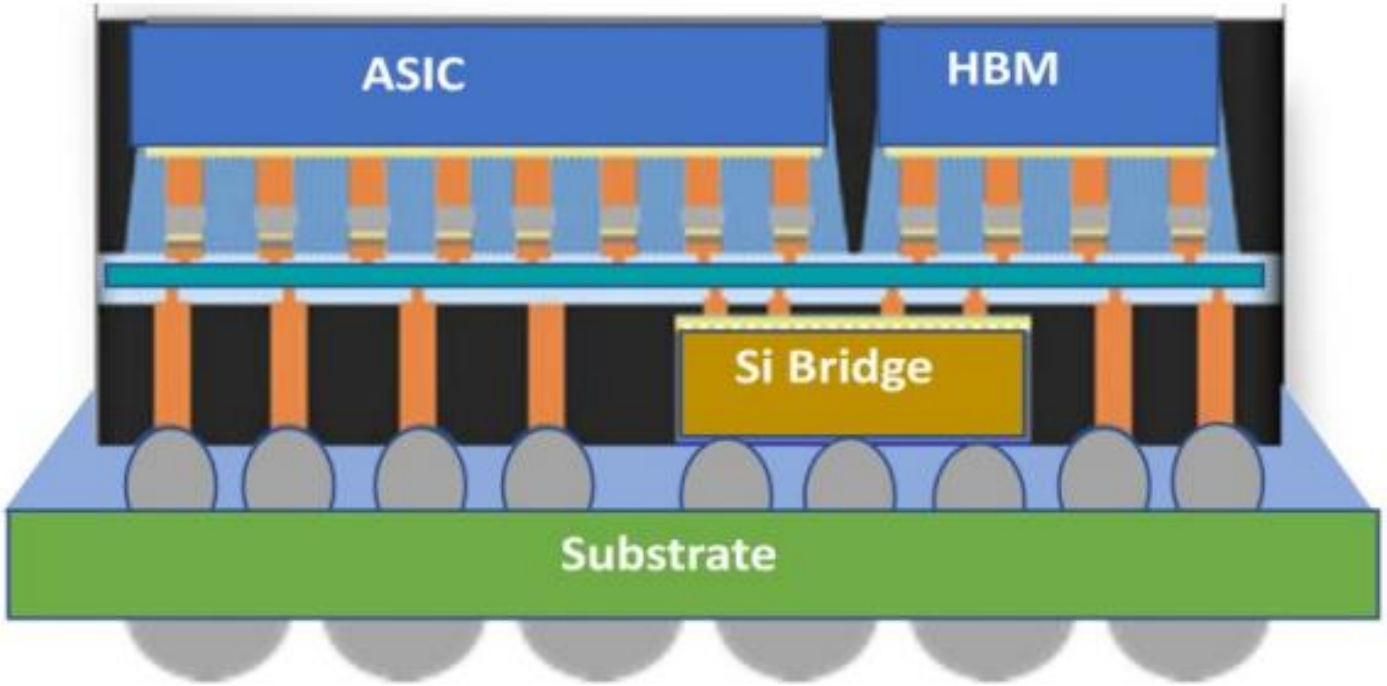




U.S. patent was filed on May 7, 2021

Advanced HDFO Packaging Solutions for Chiplets Integration in HPC Application

Lihong Cao Teck Lee1 , Yungshun Chang1 , SimonYL Huang1 , JY On1 , Emmal Lin1 and Owen Yang1
Advanced Semiconductor Engineering Inc. (US) Inc., Austin, TX 78704. USA 1 Corporate R&D Center, Advanced Semiconductor Engineering Inc., Kaohsiung, Taiwan (R.O.C)

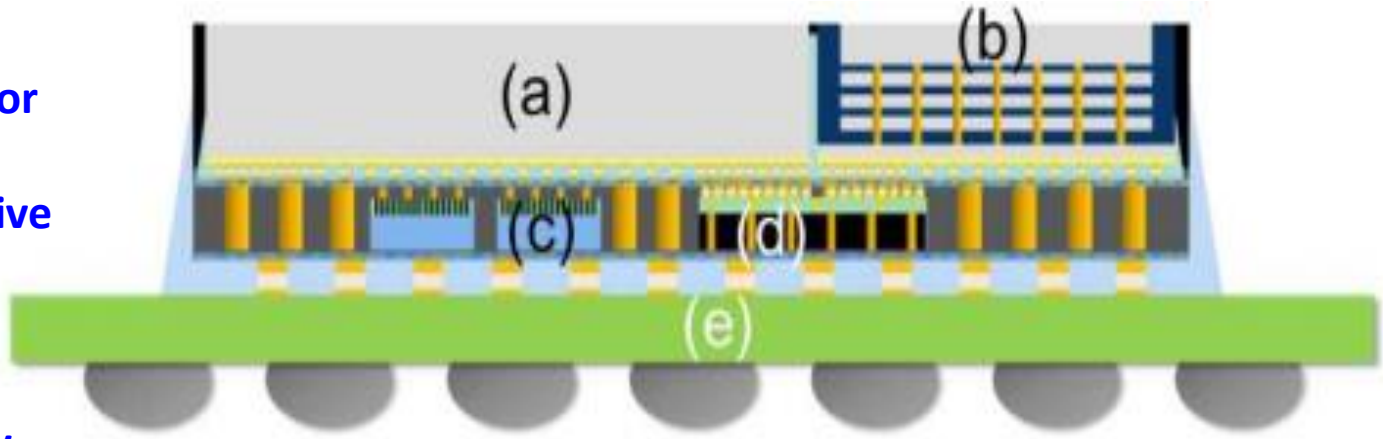


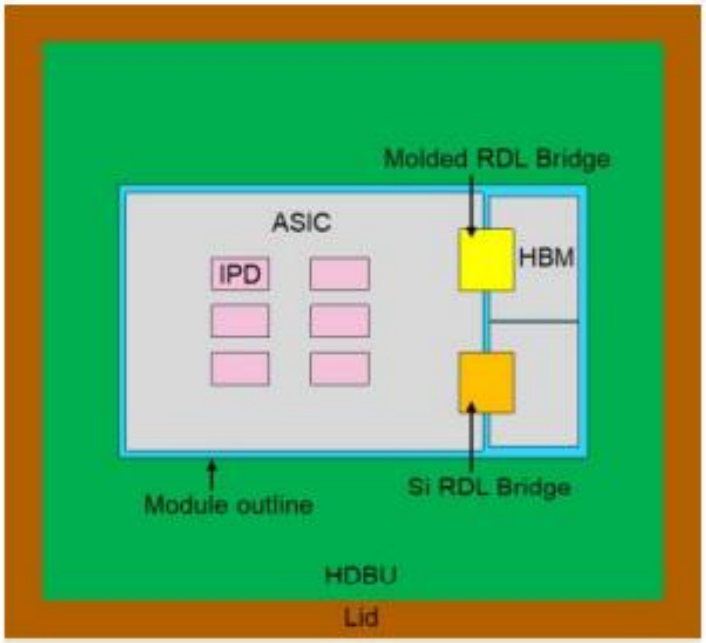
sFOCoS (Stacked Si bridge Fan-Out Chip-on-Substrate)

S-Connect Fan-out Interposer For Next Gen Heterogeneous Integration

JiHun Lee, GamHan Yong, MinSu Jeong, JongHyun Jeon, DongHoon Han, MinKeon Lee , WonChul Do, EunSook Sohn, Mike Kelly, Dave Hiner JinYoung Khim
Research & Development Amkor Technology Korea Incheon, Korea JinYoung.Khim@amkor.co.k

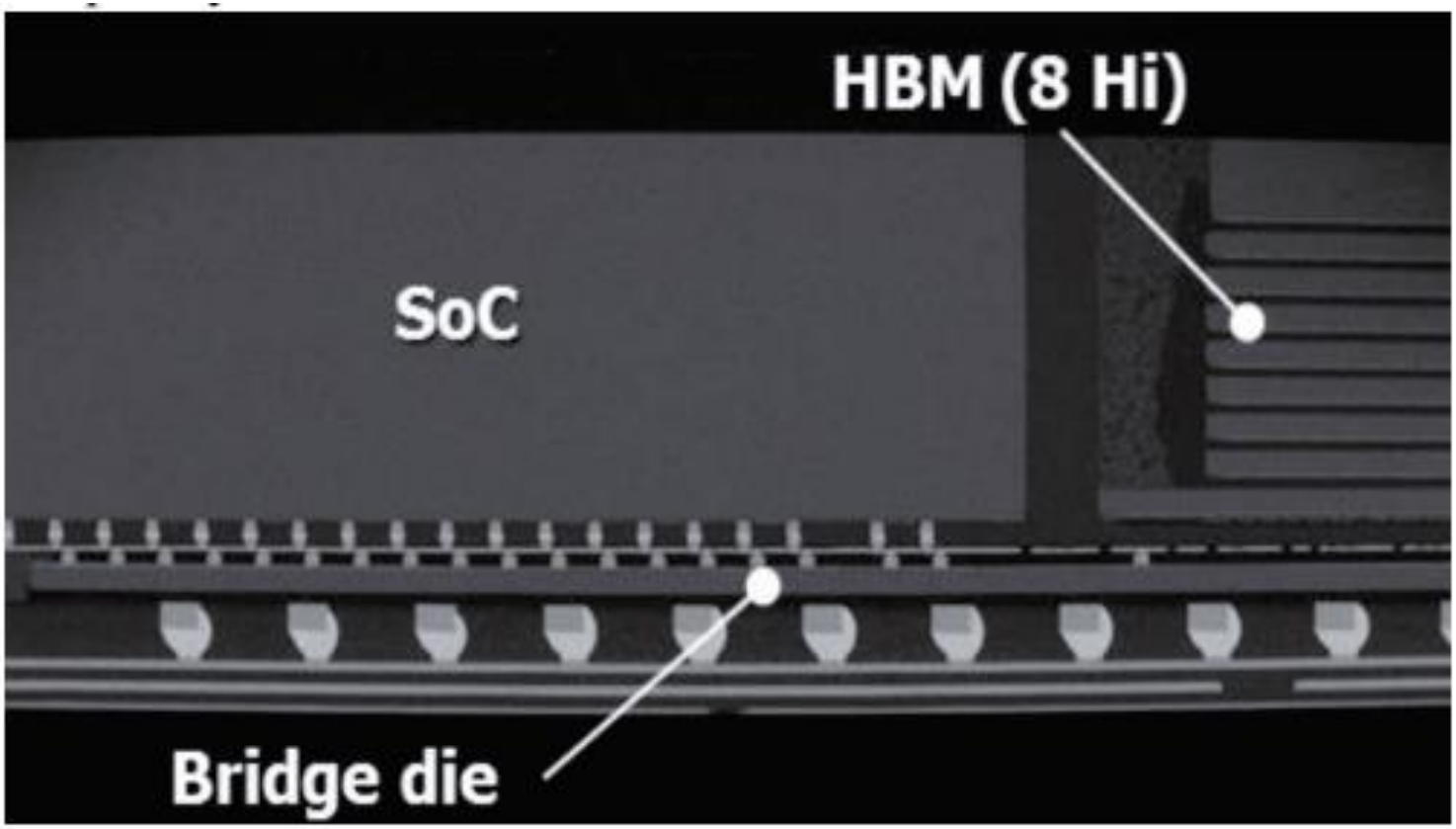
(a) ASIC or processor
(b) HBM
(c) integrated passive device or active device
(d) bridge die for ASIC to memory interconnection
(e) Package substrate





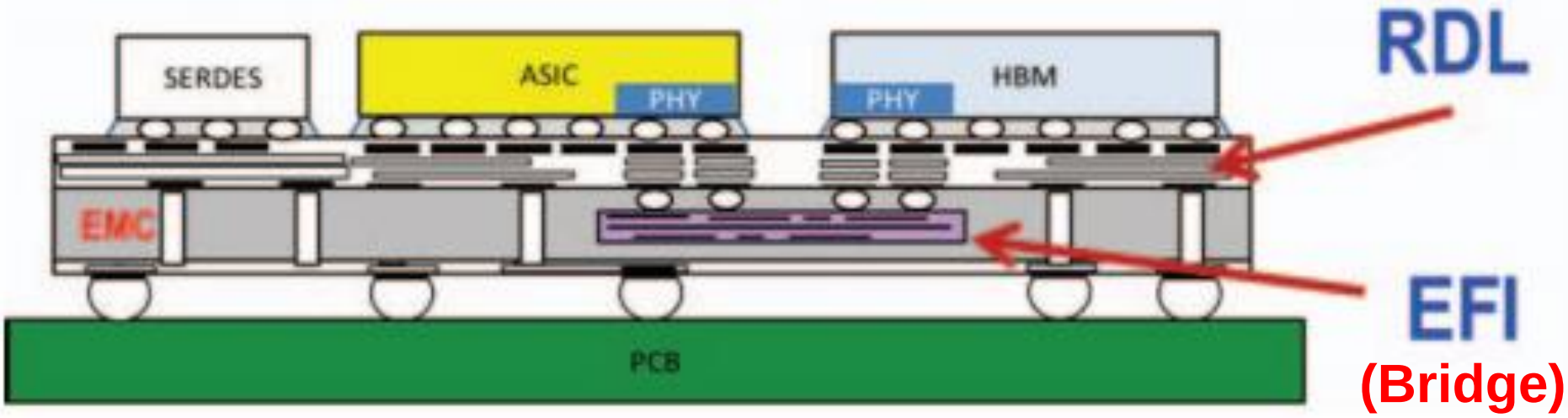
Electrical Performances of Fan-Out Embedded Bridge (FO-EB)

JinWei You, Jay Li, David Ho, Jackson Li, Ming Han Zhuang, David Lai, C. Key Chung, Yu-Po Wang
Siliconware Precision Industries Co. Ltd Taichung, Taiwan jinweiyou@spil.com.tw



Heterogeneous Integration with Embedded Fine Interconnect (EFI)

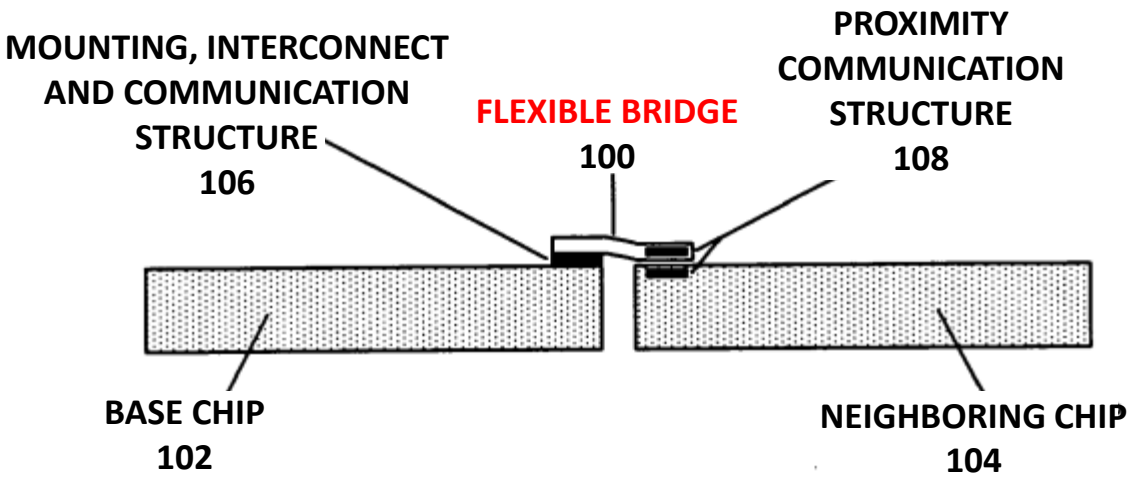
Chai Tai Chong, Lim Teck Guan, David Ho, Han Yong, Chong Ser Choong, Sharon Lim Pei Siang, Surya Bhattacharya Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research) 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634 chaitac@ime.a-star.edu.sg, +65-6770-5425

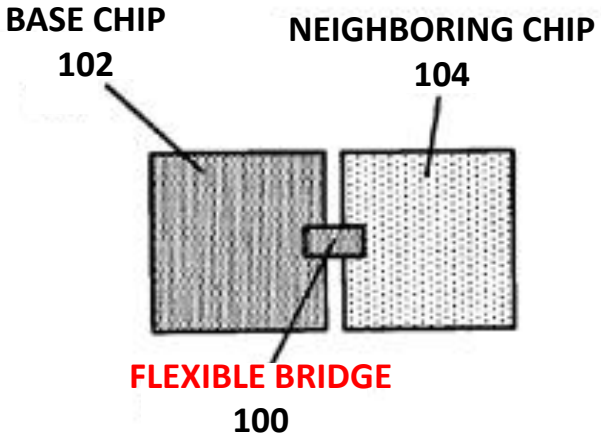


IEEE/ECTC June 2021

Flexible Bridge

Flexible Bridge





U.S. 2006/0095639 A1 was filed by SUN Microsystems

Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposer (Bridges)
- Heterogeneous Integrations on Chip-First and Chip-Last Fan-Out RDL-Substrates (interposer) – 2.3D IC Integration
- Heterogeneous Integrations on Ceramic Substrates

Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate (FOCoS)

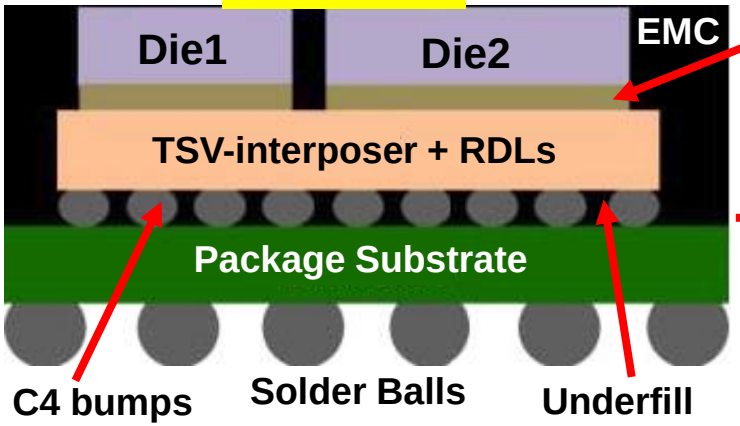
Yuan-Ting Lin, Wei-Hong Lai, Chin-Li Kao, Jian-Wen Lou, Ping-Feng Yang, Chi-Yu Wang, and Chueh-An Hseih*

Advanced Semiconductor Engineering (ASE), Inc.

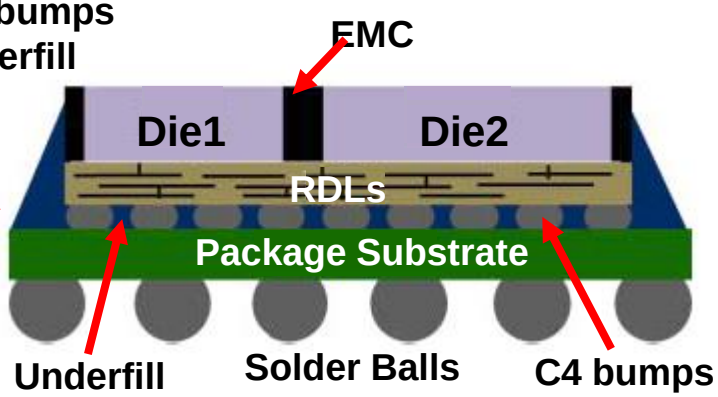
e-mail: Adren_Hsieh@aseglobal.com

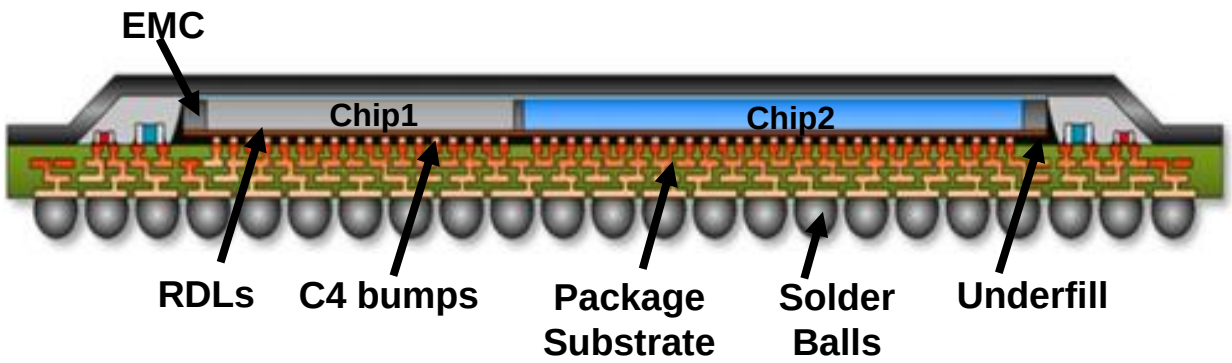
Chip-First

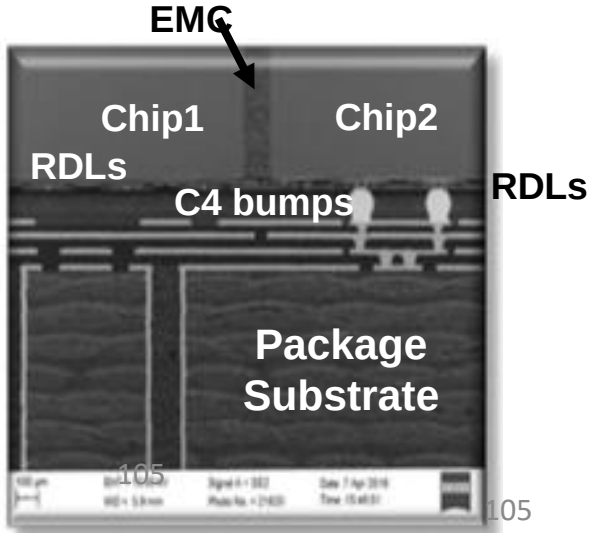
CoWoS



ASE's FOCoS







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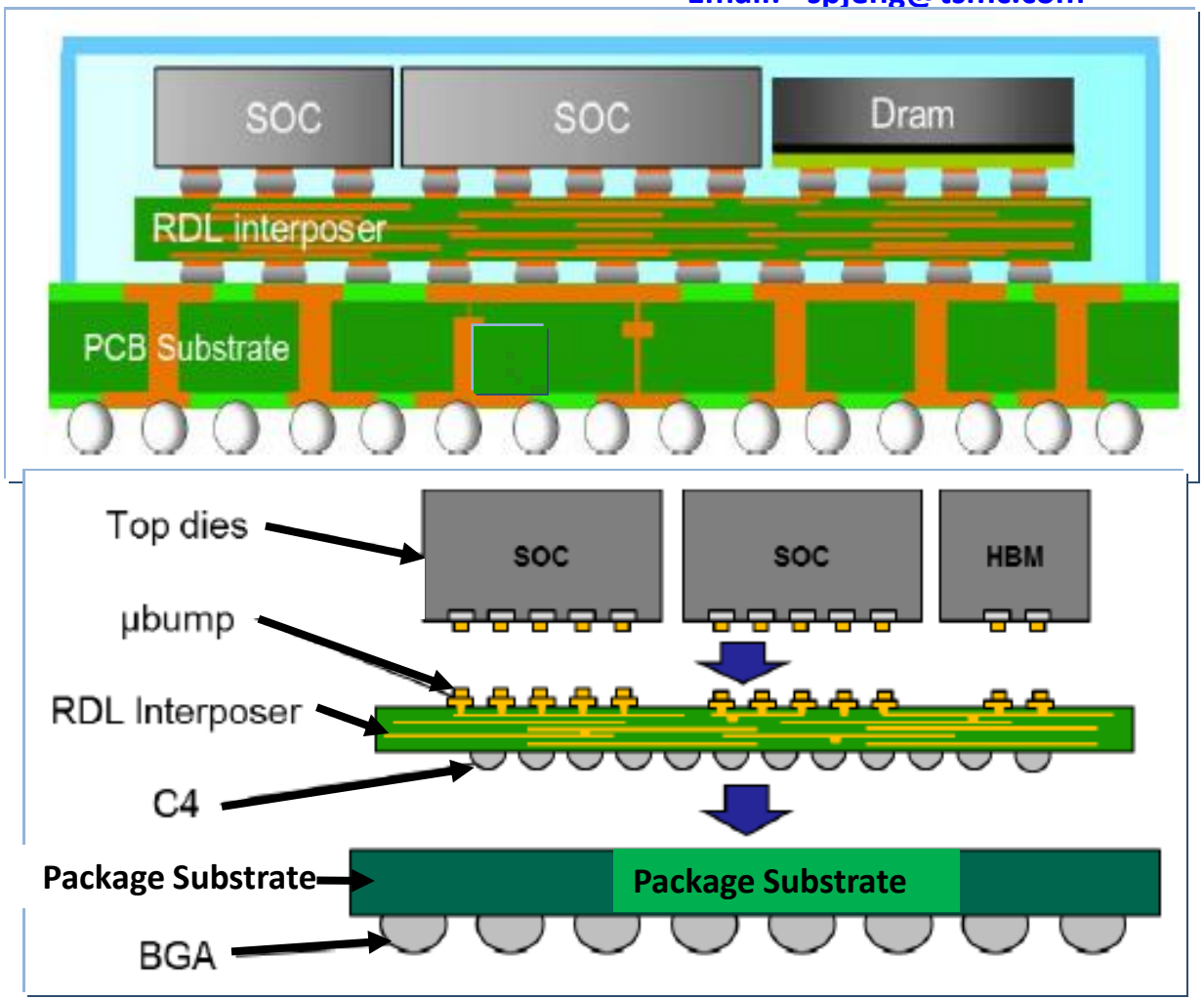
Heterogeneous Integration with Multilayer Fan-Out RDL Interposer

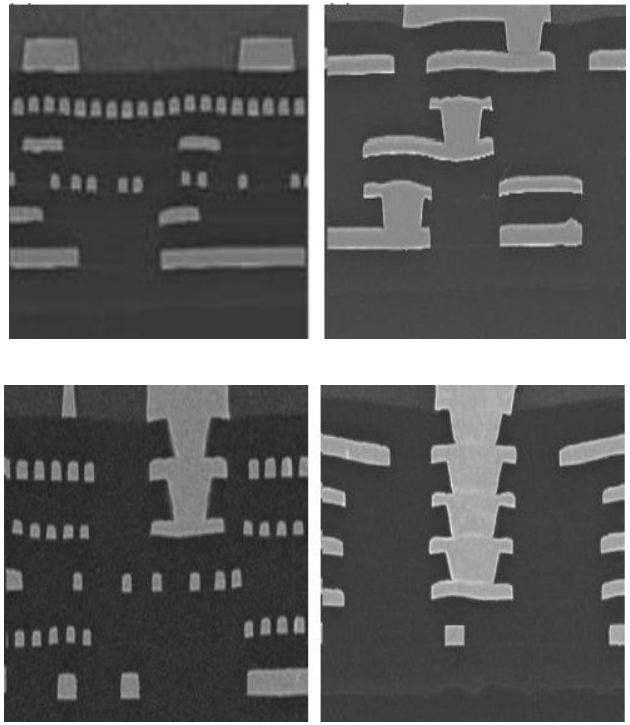
Yi-Hang Lin, M.C.Yew, M.S. Liu ,S.M. Chen, T.M. Lai, P.N. Kavle, C.H. Lin, T.J. Fang, C.S. Chen, C.T. Yu, K.C. Lee, C.K. Hsu, P.Y. Lin, F.C Hsu and Shin-Puu Jeng*

Chip-Last

TSMC, No.6, Creation Rd. II, Hsinchu Science Park, Hsinchu, Taiwan (R.O.C.) 30077

Email: *spjeng@tsmc.com

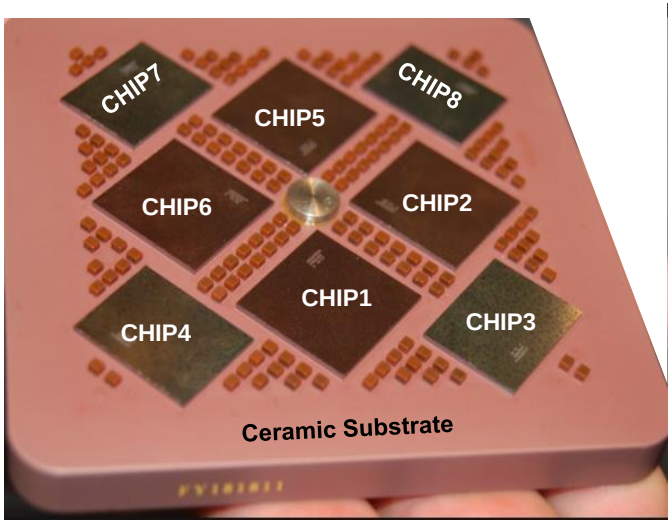




Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposer (Bridges)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

MCM (Multichip Module) on Ceramic Substrate



MCM on Ceramic Substrate

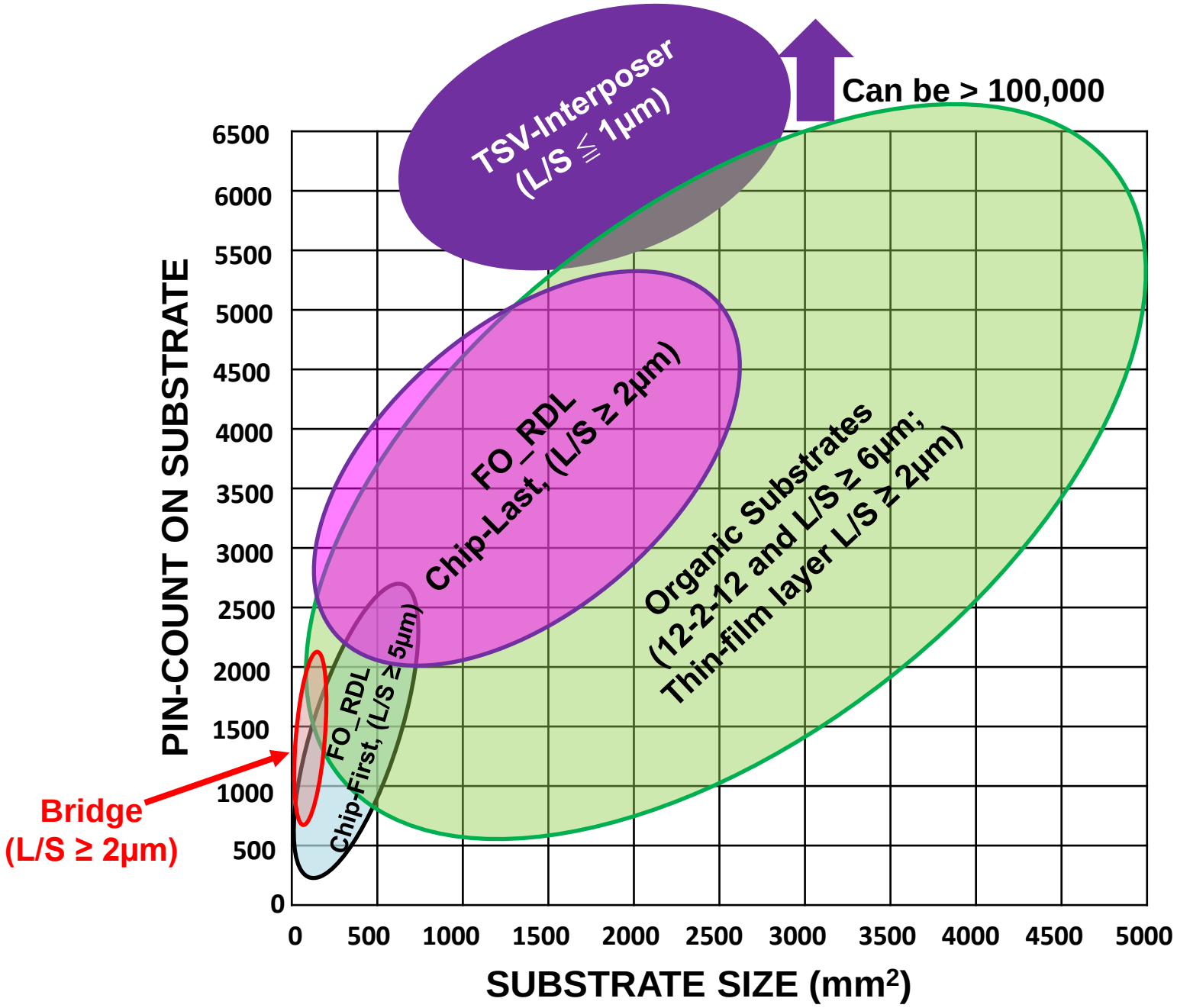
IBM 9121 TCM
(Thermal Conduction Module)

- TCM weighs 2.2Kg
- Contains up to 121 chips about 8-10mm square
- Each chip has a spring-loaded Cu piston to remove heat
- Up to 10W dissipation per chip
- Up to 600W dissipation per TCM
  Ceramic substrate has:
  - 63 layers
  - Up to 400m of wirings
  - Up to 2 million vias
- 5Kg air-cooled heatsink to remove heat from TCM

How to Select Substrate for Heterogeneous Integration Packaging?

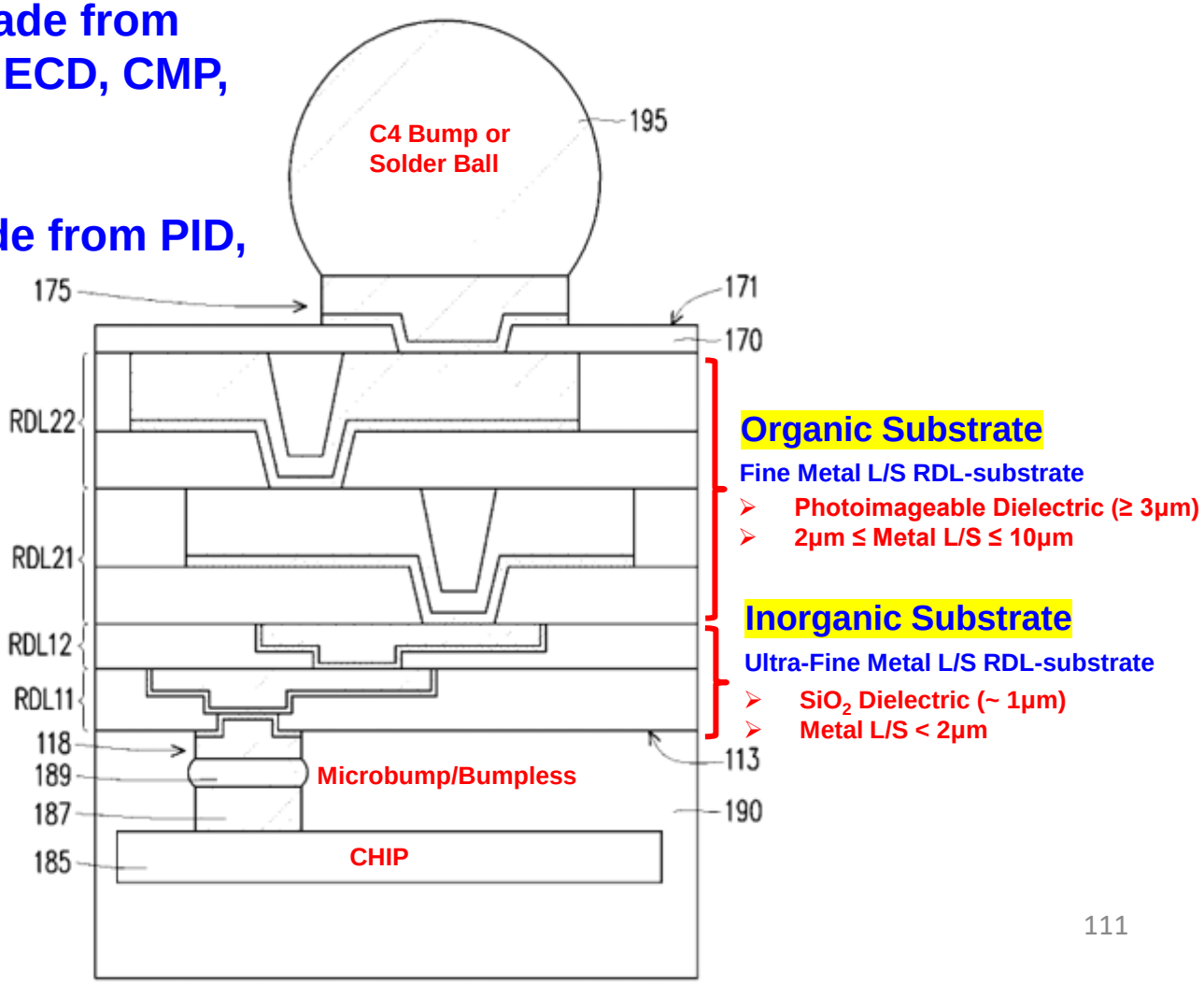
- It depends on the applications.
- The most important indicator (selection criterion) is the metal line width and spacing of the RDLs for the substrates being used for the heterogeneous integrations.
- Also, low loss dielectric materials for high-speed and high-frequency are very important.

Heterogeneous Integrated Substrates (Next 5 Years)

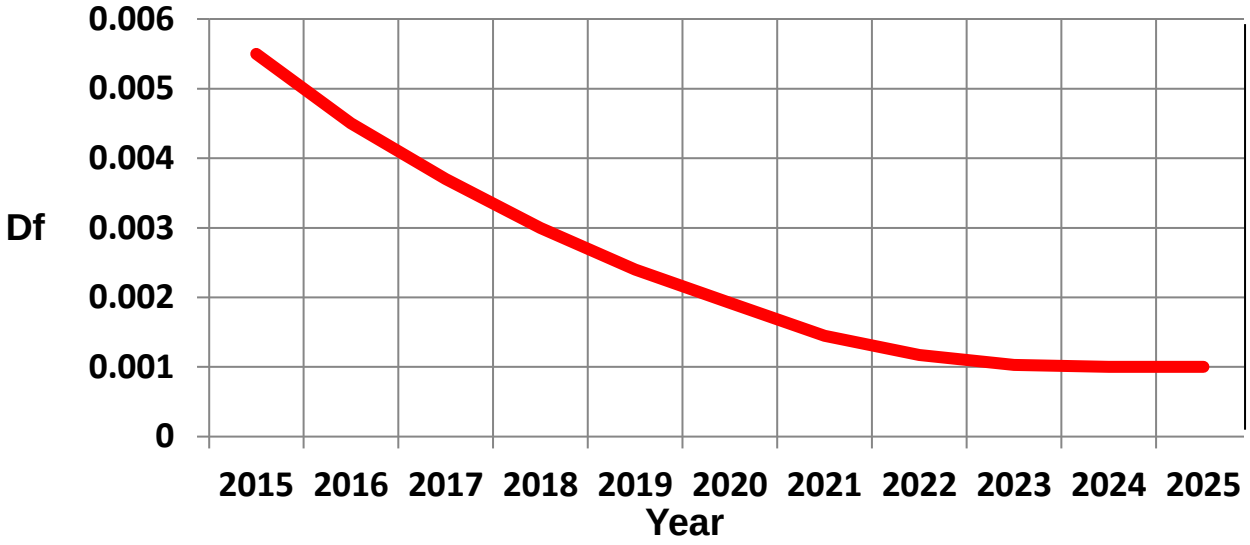


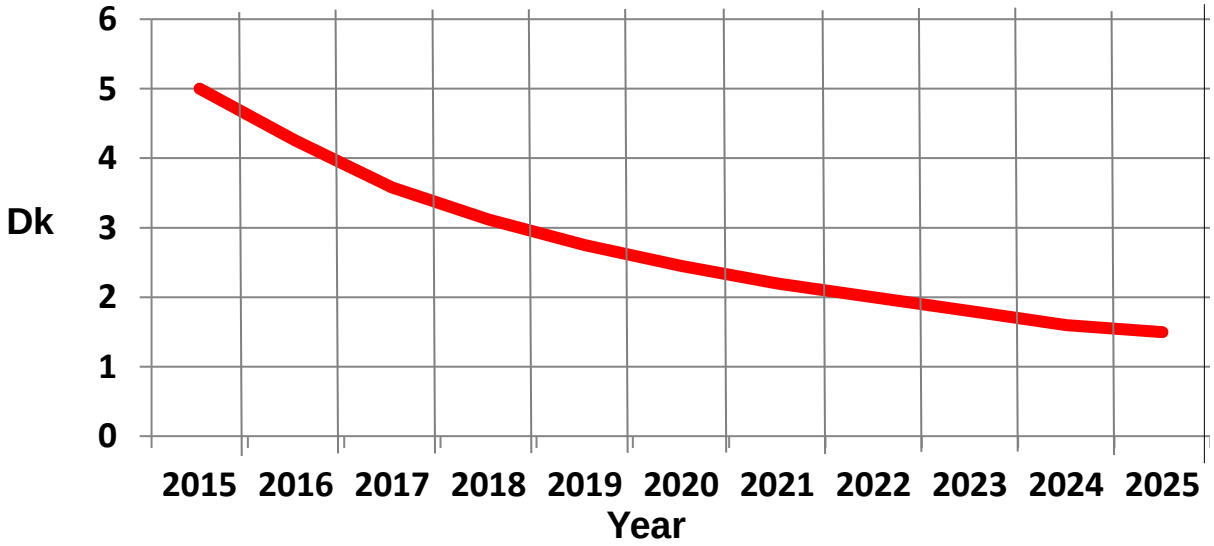
Hybrid Substrates for HPC and Data Center Applications Driven by AI and 5G/6G

- Hybrid Substrate = Inorganic Substrate + Organic Substrate
- Inorganic Substrate made from PECVD, PVD, Stepper, ECD, CMP, etc.
- Organic Substrate made from PID, PVD, LDI, ECD, etc.



Roadmap for Df (Dissipation Factor or Loss Tangent) and Dk (Dielectric Constant or Permittivity)





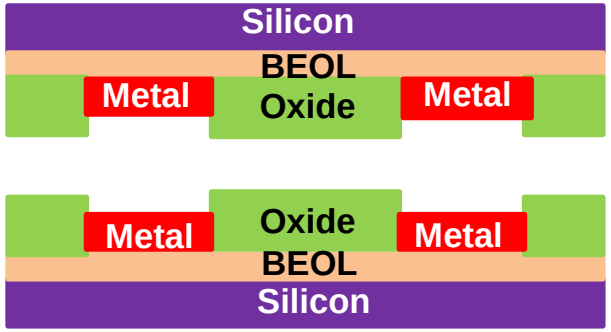
Semiconductor Advanced Packaging, 2021

Bumpless Cu-Cu Hybrid Bonding

Key Process Steps (Fundamental) of Hybrid Bonding

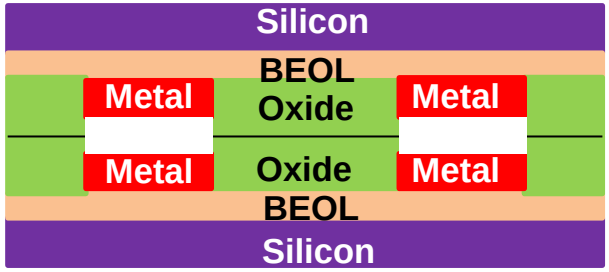
Metal (Cu) recess = 3nm
Plasma surface Activation

(a)



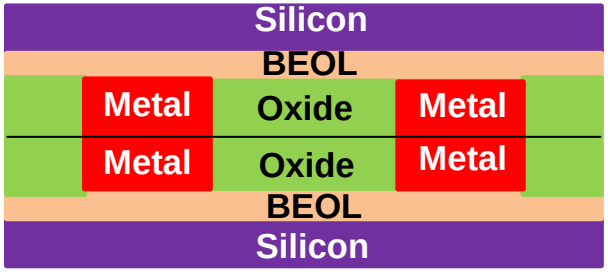
Oxide to Oxide Initial Bond
at Room Temperature

(b)



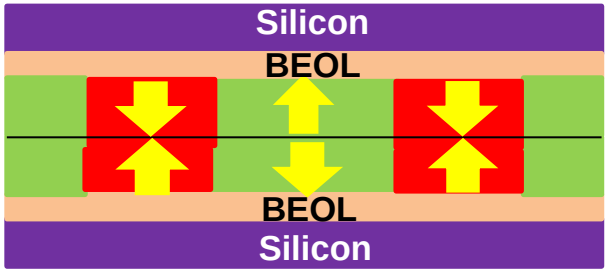
Heating Closes Dishing Gap
(Metal CTE > Oxide CTE)
(Optional)

(c)



Annealing (300°C for 0.5h)
w/o External Pressure

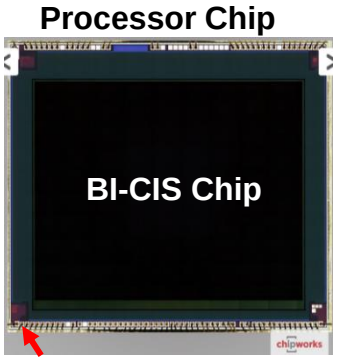
(d)

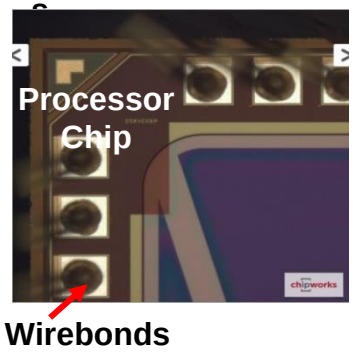


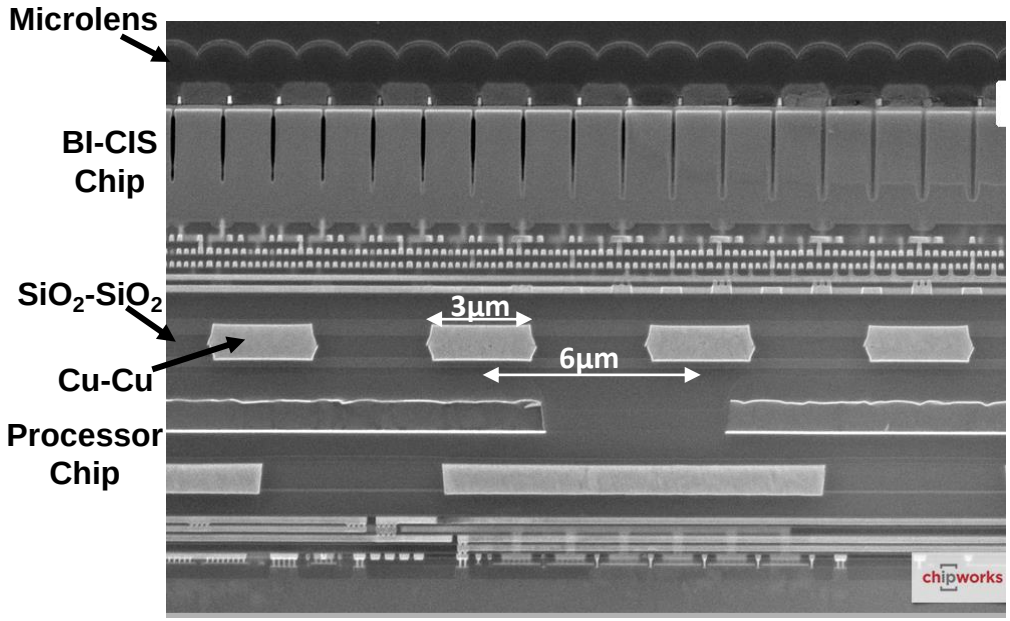
The challenges (opportunities) of CoW hybrid bonding are:

- CMP for metal recess, clean, and flat surface.
- the edge effects;
- contaminants;
- particles due to singulation;
- the requirement of higher accuracy pick and place machines;
- slightly larger pads to compensate the pick and place tolerance.

Sony's CMOS image sensor made by hybrid bonding







CMOS Image Sensor (CIS)

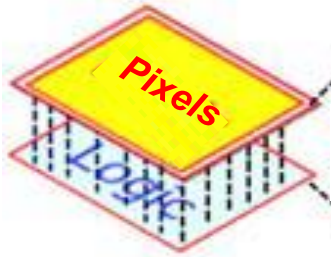
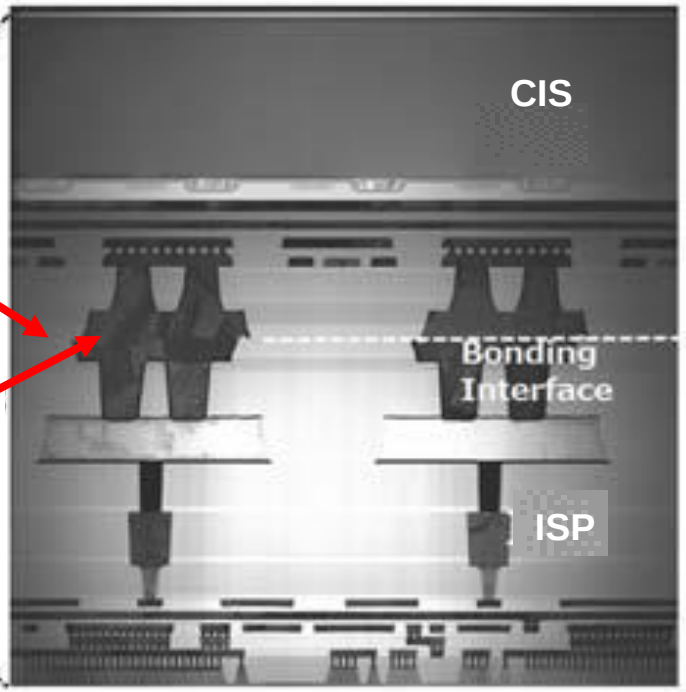
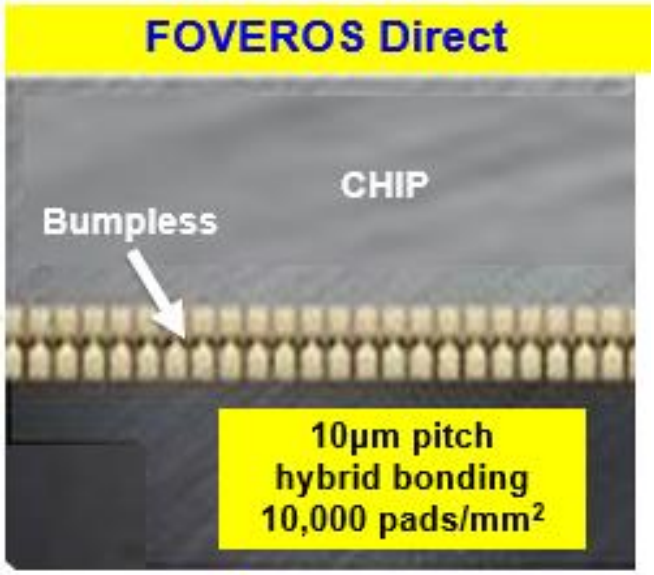


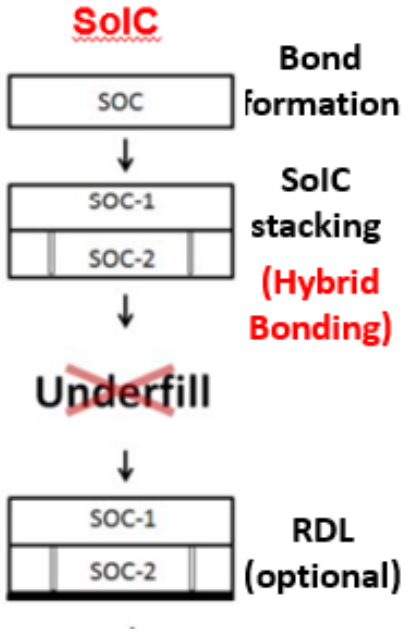
Image Signal Processor (ISP)



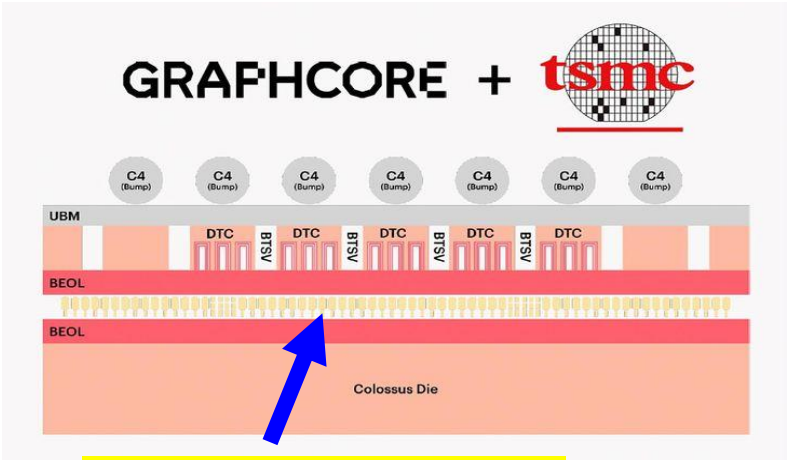
Other Hybrid Bonding



Intel

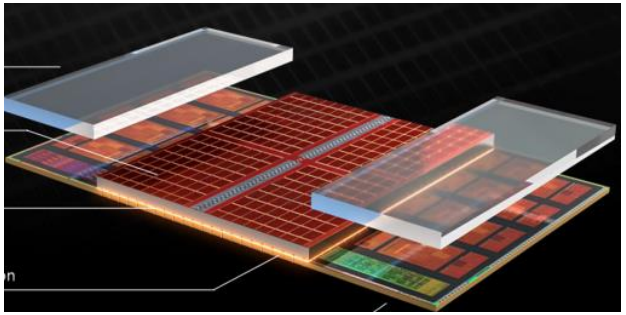


TSMC



Bumpless Cu pads for hybrid bonding

RYZEN 9 5900X



AMD/TSMC

IEEE SPECTRUM Mar 2022

Summary and Trends

- Advanced packaging has been defined, and the kinds of advanced packaging have been ranked according to their interconnect density and electrical performance and grouped into 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration.
- The 2D IC integration, such as SiP, is and still will be used the most.
- The challenge of 2.1D IC integration (with thin film layers on build-up package substrate) is (warpage) manufacturing yield.
- The 2.3D IC integration is creeping into production.
- For extreme high-performance and high-density applications, 2.5D IC integration is the solution.
- The 3D IC integration are already in volume production for mobile processors, and they will be used for more different kinds of products.
- Fan-outs, such as chip-first (face-down) and chip-first (face-up), have been in HVM for consuming products. Chip-first (face-down) is and will still be used the most. Chip-last or RDL-first is not in HVM yet but it will be soon.

Summary and Trends

- More than 75% of the flip-chip applications are with C4 bumps mass reflowed on organic package substrates and CUF (capillary underfill) (SiP).
- TCB (thermocompression bonding) of C2 bumps with small-force and CUF is getting traction because of the interest in using thin chips and thin organic substrates.
- No more than 25% of the flip-chip applications are for silicon-to-silicon, such as CoC, CoW, and WoW.
- Roadmaps of Df and Dk for low-loss dielectric materials of advanced packaging have been provided.
- The TSV-interposer integration platform for PIC and EIC of high-speed and high-bandwidth applications is getting lots of tractions. A couple of examples have been provided.
- A heterogeneous integration of AiP and baseband chipset with heat spreader/sink by chip-first with die face-down packaging for high performance and compact 5G millimeter wave system integration has been proposed.

Summary and Trends

- SoCs with finer feature sizes are and will be here to stay. Chiplets design and heterogeneous integration packaging provide alternatives to SoCs, especially for advanced nodes.

- The key advantages of chiplets heterogeneous integration are:
  - (1) yield improvement (lower cost) during manufacturing,
  - (2) time-to-market,
  - (3) cost reduction during design,
  - (4) better thermal performance,
  - (5) reusable of IP,
  - (6) modularization.

- The key disadvantages are:
  - (1) additional area for interfaces,
  - (2) higher packaging costs,
  - (3) more complexity and design effort,
  - (4) past methodologies are less suitable for chiplets.

Summary and Trends

- **Bridge technology such as EMIB for chiplets' horizontal communication in organic substrate has been in production. Recently, there are many publications on bridges embedded in EMC.**

- **More than 75% of heterogeneous integration are on organic substrate (SiP by SMT and flip chip on board) and no more than 25% are on other substrates.**

- **Hybrid bonding can be applied to extremely fine pitch (as low as 4μm) pads and used for very high-density and high-performance applications.**

- **Hybrid bonding is only suitable for silicon-to-silicon assembly such as CoC, CoW, and WoW.**
  - **Because of the throughput issue, CoC bonding will not be popular.**
  - **Because of the chip-size and yield issues, WoW bonding is limited even it will be used more than today.**
  - **Because of the flexibility, CoW will be the mainstream.**

Some Recent Advanced Packaging Publications by the Lecturer and his Colleagues

1. Lau, J. H., "Recent Advances and Trends in Advanced Packaging", *IEEE Transactions on CPMT*, Vol. 12, No. 2, February 2022, pp. 228-252.
2. Lau, J. H., G. Chen, J. Huang, et al., "Hybrid Substrate by Fan-Out RDL-First Panel-Level Packaging, *IEEE Transactions on CPMT*, Vol. 11, No. 8, August 2021, pp. 1301-1309.
3. Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", *ASME Transactions, Journal of Electronic Packaging*, Vol. 143, June 2021, pp. 1-36.
4. Lau, J. H., C. Ko, C. Lin, et al., "Fan-Out Panel-Level Packaging of Mini-LED RGB Display", *IEEE Transactions on CPMT*, Vol. 11, No. 5, May 2021, pp. 739-747.
5. Lau, J. H., *Semiconductor Advanced Packaging*, Springer, New York, 2021.
6. Lau, J. H., C. Ko, K. Yang, et al., "Panel-Level Fan-Out RDL-first Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125-1137.
7. Lau, J. H., C. Ko, T. Tseng, et al., "Panel-Level Chip-Scale Package with Multiple Diced Wafers", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1110-1124.
8. Lau, J. H., and N. C . Lee, *Assembly and Reliability of Lead-Free Solder Joints*, Springer, New York, 2020.
9. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1-27.
10. Lau, J. H., *Heterogeneous Integration*, Springer, New York, 2019.
11. Lau, J. H., M. Li, M. Li, et al., "Fan-out wafer-level packaging for heterogeneous integration," *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.
12. Lau, J. H., M. Li, Q. Li, et al., "Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT*. Vol. 8, Issue 6, June 2018, pp. 991-1002.
13. Lau, J. H., M. Li, Y. Li, et al., "Warpage Measurements and Characterizations of FOWLP with Large Chips and Multiple RDLs", *IEEE Transactions on CPMT*, Vol. 8, Issue 10, October 2018, pp. 1729-1737.
14. Lau, J. H., *Fan-Out Wafer-Level Packaging*, Springer, New York, 2018.
15. Lau, J. H., M. Li, D. Tian, et al., "Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT*, Vol. 7, Issue 10, October 2017, pp. 1729-1738.
16. Lau, J. H., "Recent Advances and New Trends in Flip Chip Technology", *ASME Transactions, Journal of Electronic Packaging*, September 2016, Vol. 138, Issue 3, pp. 1-23.
17. Lau, J. H., *3D IC Integration and Packaging*, McGraw-Hill, New York, 2016.
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Thank You Very Much for Your Attention!