Electrical Design of Advanced Packaging in Computing Systems

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For presentation on 15 June 2022

IEEE EPS Distinguished Lecture

Computer System Packaging Design

- Fundamentals of Electrical Design of Computer Systems
- The challenges that provide opportunity for engineering ingenuity
- Example: Processor socket challenge – Bandwidth, Frequency
- Heterogeneous Integration addressing today's challenges
  - Heterogeneous Integration Roadmap (HIR)
- Opportunity to learn more and contribute to the community

Challenges: Drivers for advancing systems

- Historic Drivers
  - Moore's Law
  - Dennard Scaling
- Current Reality – enabled by
  - 3D Devices
  - 3D Packaging
  - Advanced interconnect
  - Heterogeneous Integration

Dennard Scaling

TABLE I

SCALING RESULTS FOR CIRCUIT PERFORMANCE

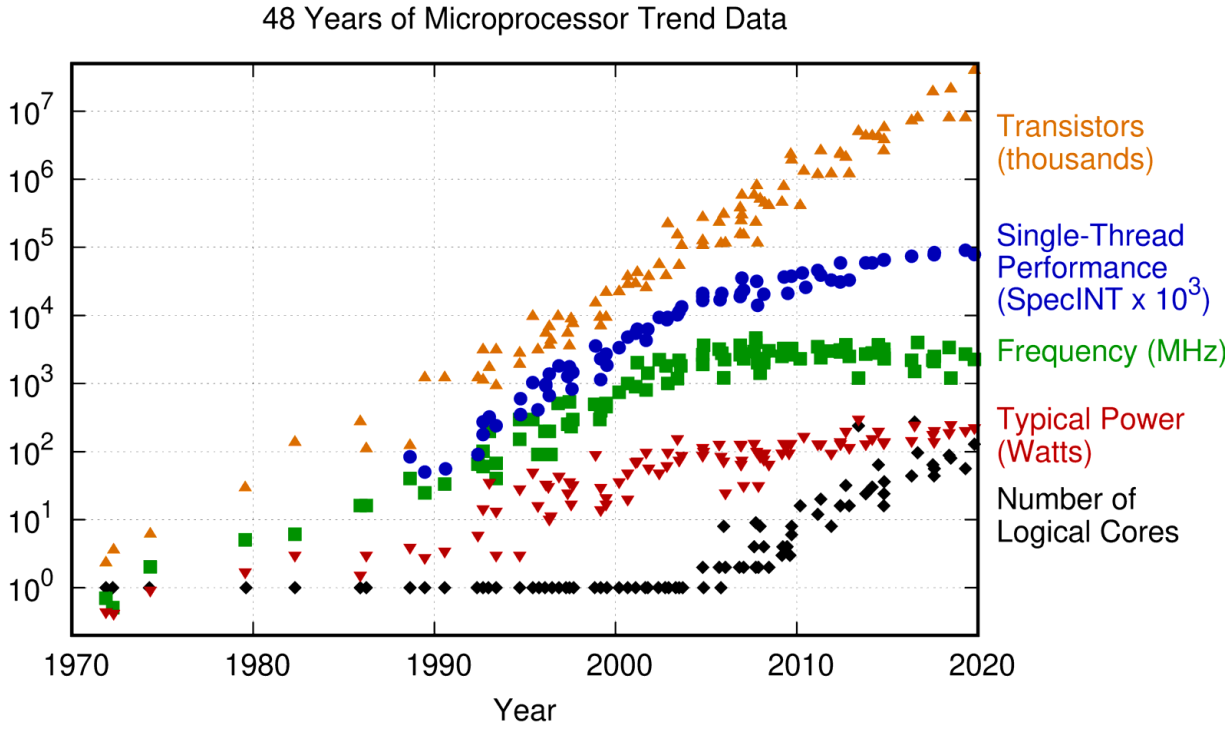
Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

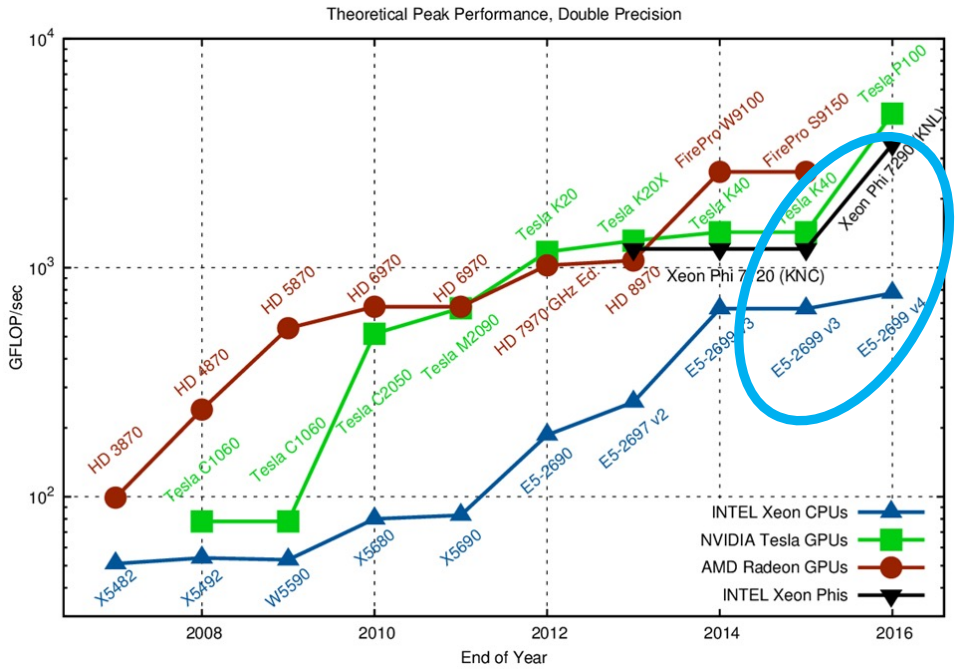
R. H. Dennard, F. H. Gaensslen, H. -N. Yu, V. L. Rideout, E. Bassous and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," in IEEE Journal of Solid-State Circuits, vol. 9, no. 5, pp. 256-268, Oct. 1974, doi: 10.1109/JSSC.1974.1050511.

Scaling Trends

From HIR Chapter 2
Kanad Ghose, Dale Becker, Co-Chairs

HETEROGENEOUS INTEGRATION ROADMAP





Hardware Trends:

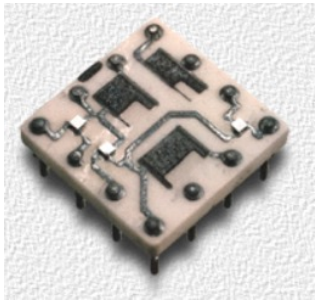
- Everything is getting intrinsically power and memory constrained; new applications are exacerbating the dependence on memory
- Accelerators are more energy-efficient than general-purpose designs, new memory technologies
- Heterogeneously integrated solutions have been making their mark for the past few years!

IBM Processor Packaging Integration – 50+ years

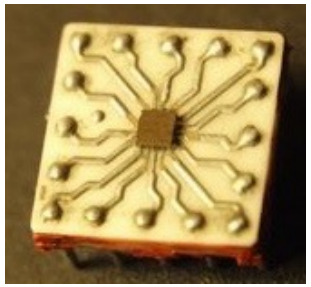
Courtesy: John Dux, IBM Ret'd

1964 to 1990's
Silicon & Pkg Integ.

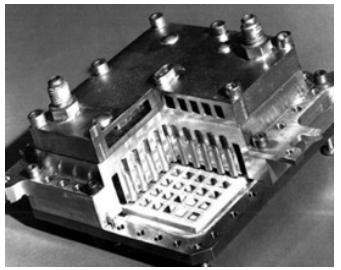
Complexity
- ⬆ Silicon
- ⬆ 1st Level Pkg
- PCB



S/360 - 1964

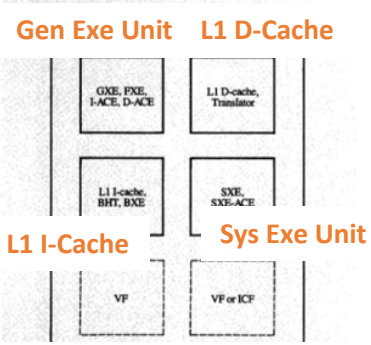


S/370 - 1970



S/3080 - 1980

S/ES9000 – 1990
Glass Ceramic/TF
4-6 TCMs/CPU



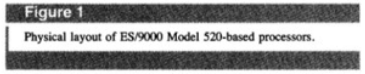
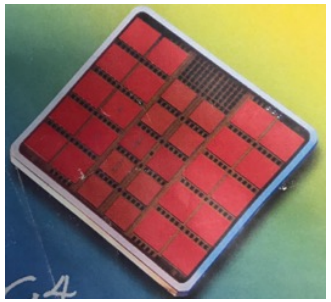


Figure 1
Physical layout of ES/9000 Model 520-based processors.

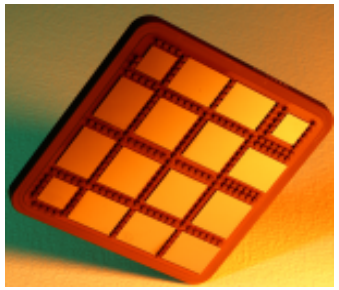
1990's- Present
Silicon Level Integration
Heterogeneous PCB Int

Complexity
- ⬆ Silicon
- 1st Level Pkg
- ⬆ PCB

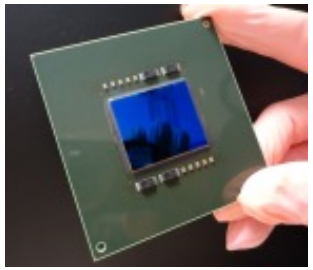
Courtesy, John Dux, IBM, Ret'd.



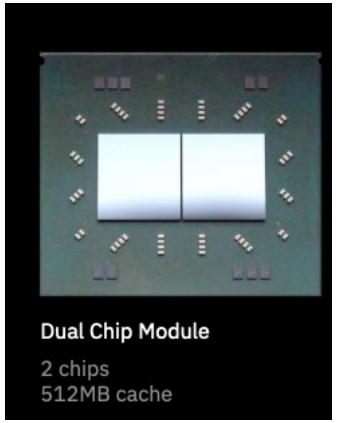
S/390 – 1997
CMOS
10 single core PU Chips / MCM



zSeries 990 – 2003
2 PUs/chip
System in Package



z13 - 2015
8 PUs/chip
System on Chip



z16 – 2022
Telum Processor

Today
Heterogeneous Pkg Int.

Complexity
- ⬆ Silicon
- ⬆ 1st Level Pkg
- ⬆ PCB

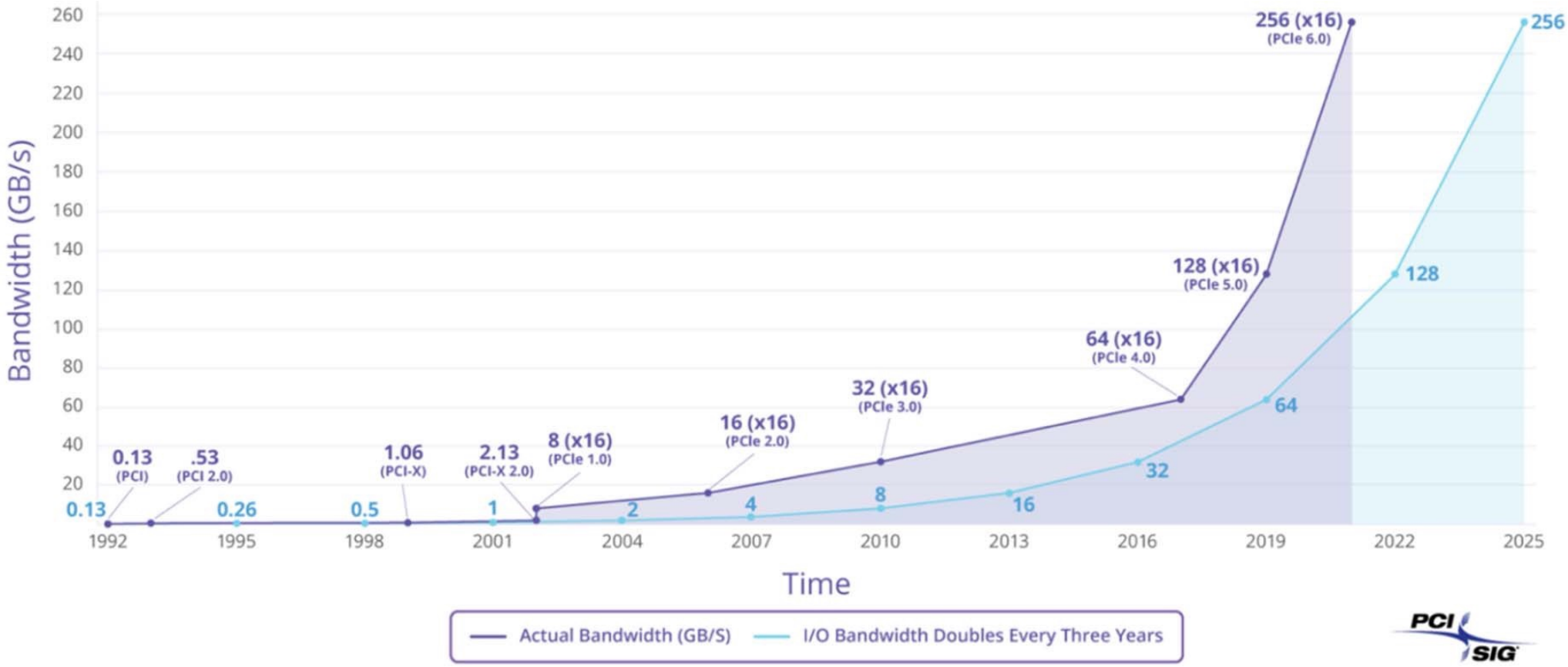
Ongoing Challenges for system packaging

To deliver the value propositions – Performance and Function

- Cost – development and product cost
- Physical form factor – Incremental changes
- Signal bandwidth density – Increasing quickly
- Voltage regulation (Power In) – Integrate closer to load
- Cooling (Power out) – Constant power density

A very visible measure of success in system packaging is the bandwidth achievable and the growth of bandwidth and bandwidth density with new generations of systems.

Example of signaling data rate growth - PCIe

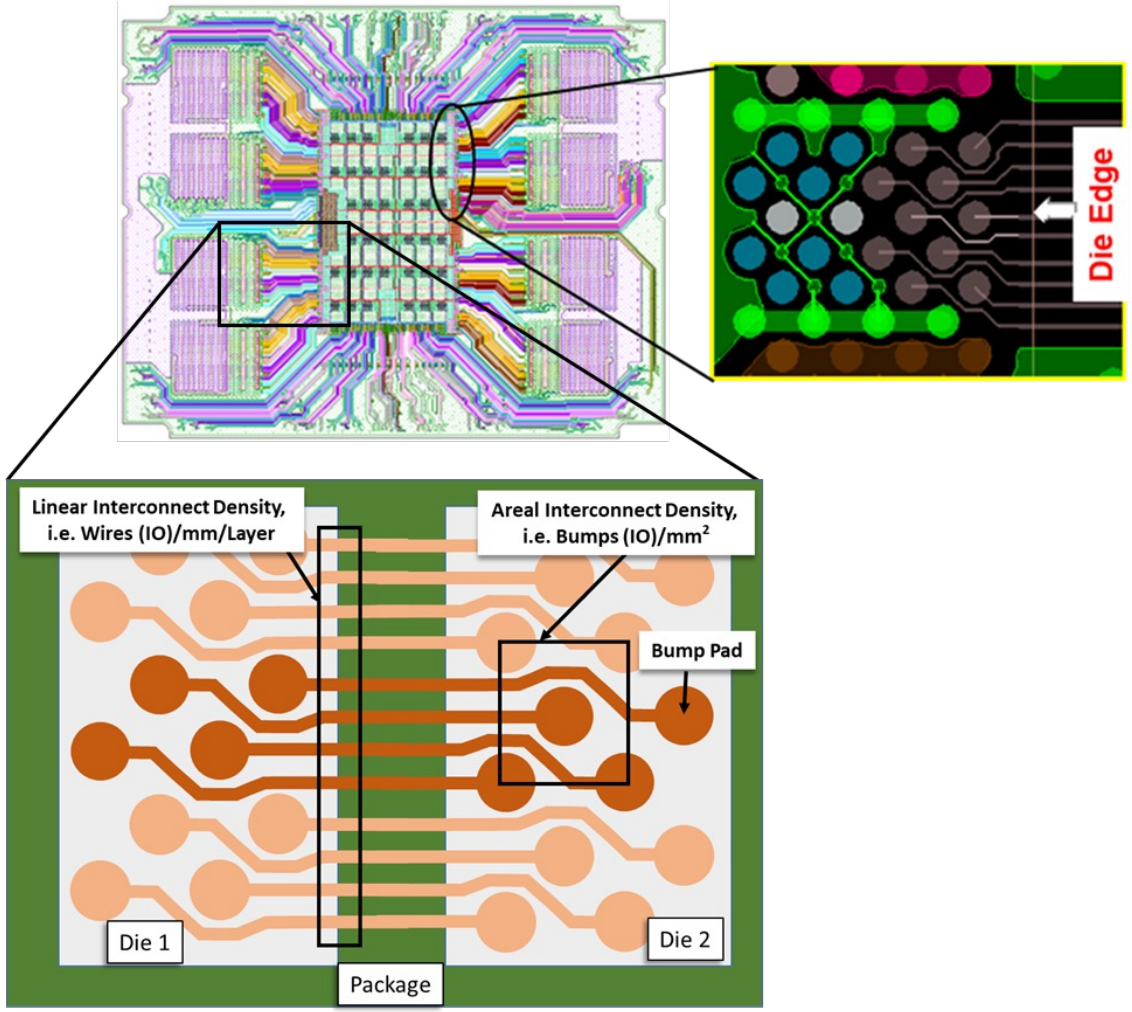


From HIR Chapter 2, Fig. 22, 2021 – Adapted from U. Pirzada, 2017 Hot Chips

Physical Metrics

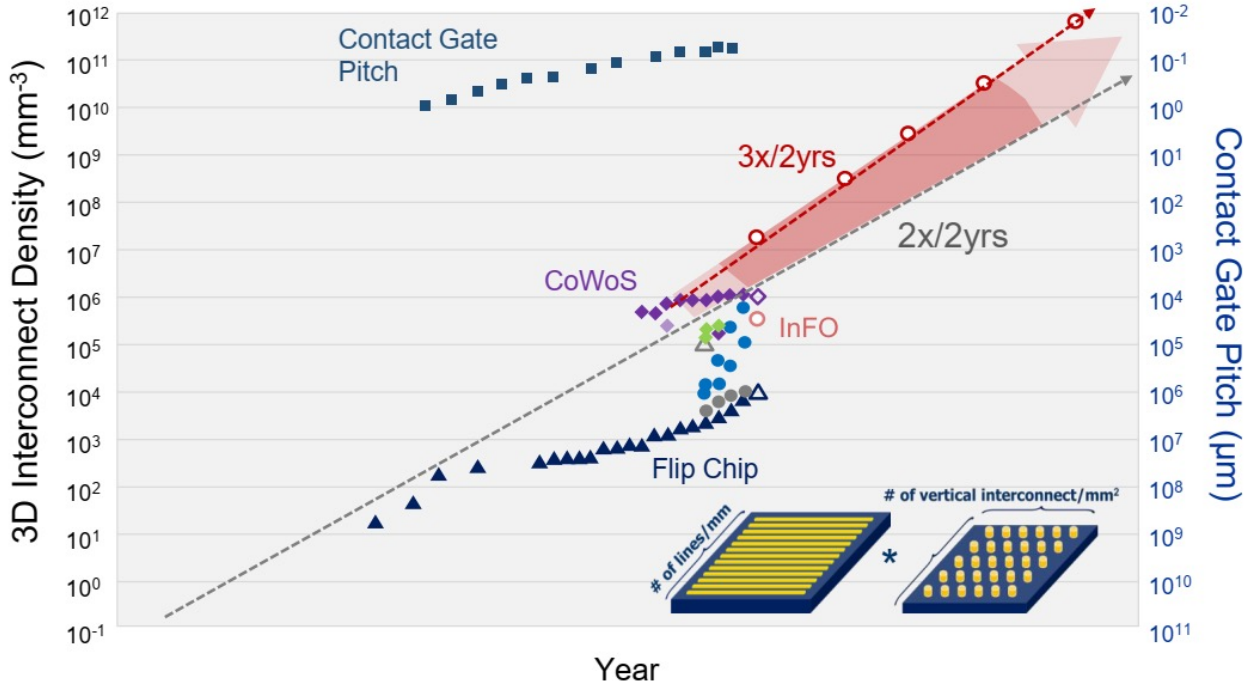
HIR Chapter 22: Ravi Mahajan, Chair
https://eps.ieee.org/images/files/HIR_2021/ch22_2D-3D.pdf

HETEROGENEOUS INTEGRATION ROADMAP



System Scaling – 3DID Roadmap

3D Interconnect Density: $\left(\frac{\#\ lines}{mm}\right) * \left(\frac{\#\ verticals}{mm^2}\right)$

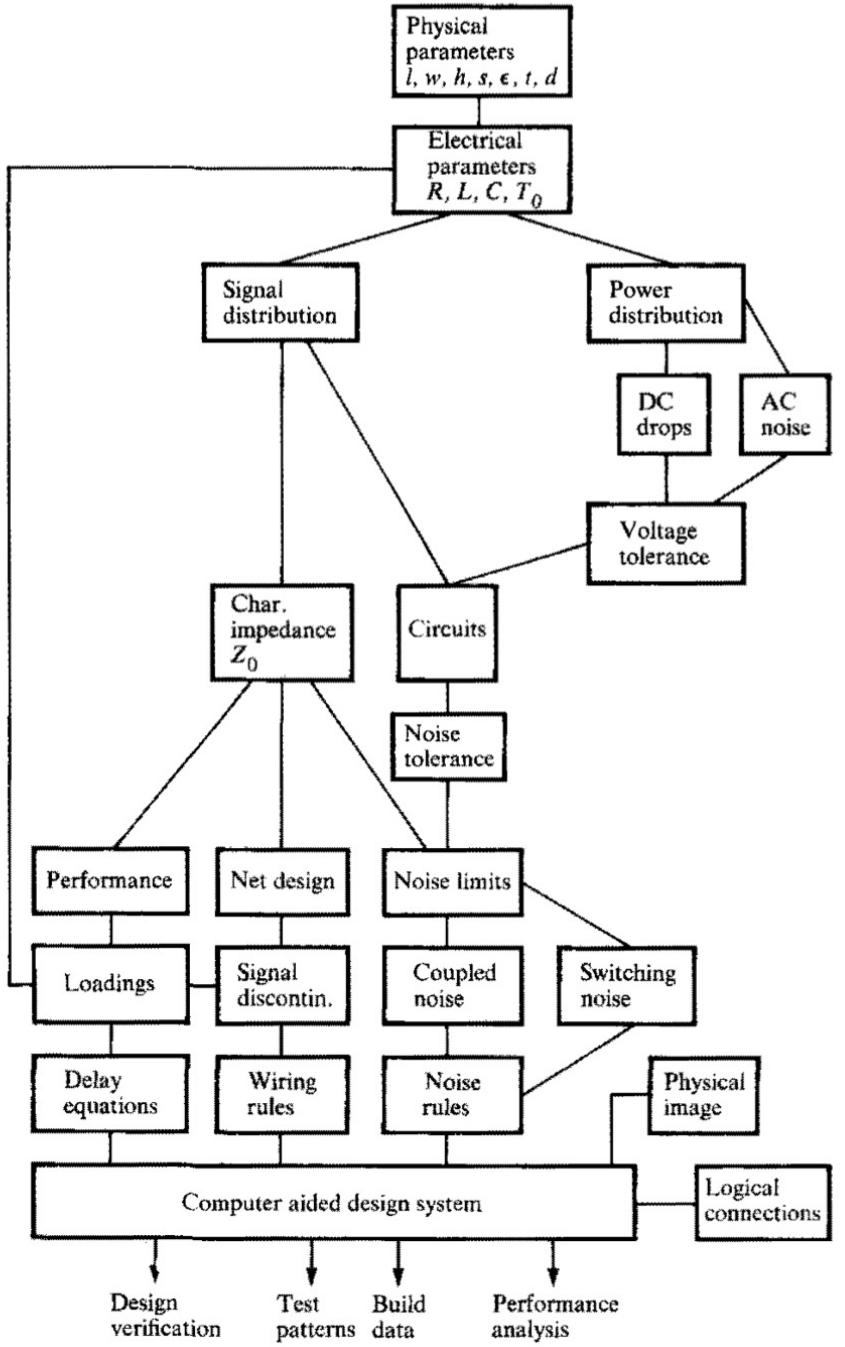


- D. Yu, 2019 Dec. IEDM Panel, San Francisco, Ca, USA
- D. Yu, 2020 May IEEE ECTC Keynote. 2020 Aug. TSMC Technology Symposium,

Fundamentals

- Methodology Input
  - Physical Parameters -> Electrical Parameters
- Signal Distribution and Power Distribution
- Design
  - Circuits
  - Net interconnections
- To
  - Achieve performance
  - With robust net design
  - Ensuring meeting the noise limits in the presence of non-ideal interconnects
- By creating
  - Design rules to meet wiring performance and noise criteria
- Methodology Output
  - Verified design, build data, performance analysis and test patterns

Figure 2 Procedure for the electrical design of a computer package.



E. E. Davidson, "Electrical Design of a High Speed Computer Package," in IBM Journal of Research and Development, vol. 26, no. 3, pp. 349-361, May 1982, doi: 10.1147/rd.263.0349.

Increasing Bandwidth by Generation

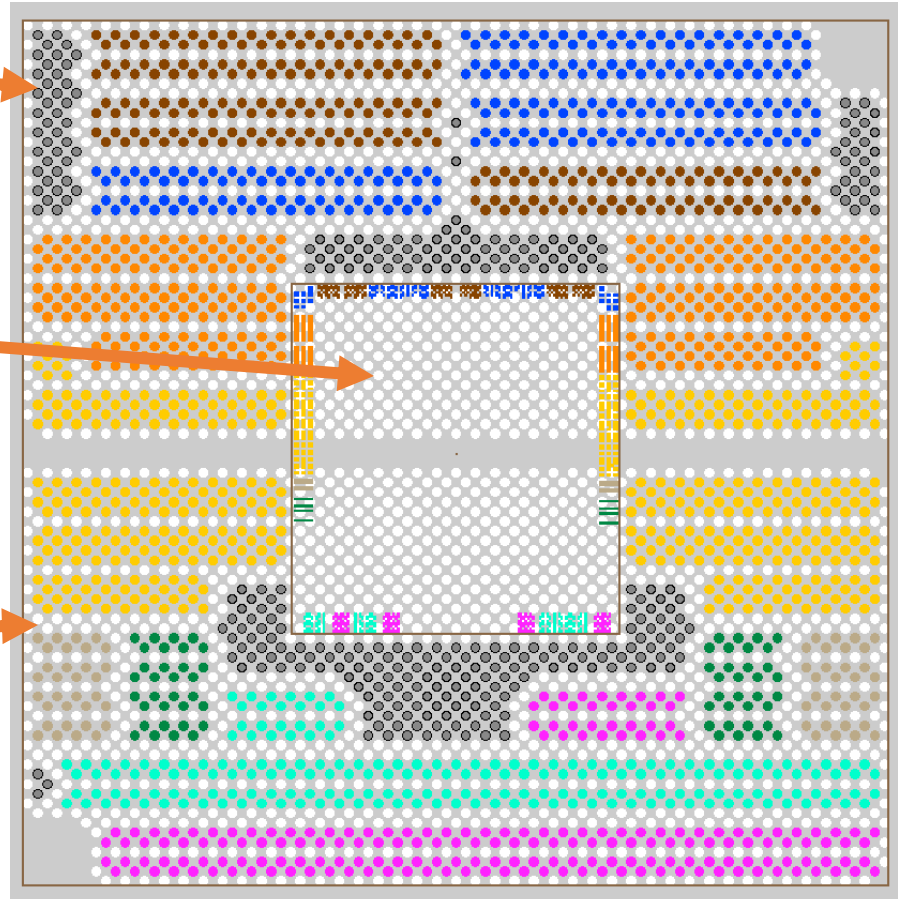
IBM Example

		POWER8 high-end package				*POWER9 high-end package*		
Bus	*No. of interfaces*	*Byte*	*Data rate per lane*	*Raw bandwidth*	*No. of interfaces*	*Byte*	*Data rate per lane*	*Raw bandwidth*
X-bus. chip-to-chip link	3	3x 8B drive/ 8B receive	4.8 Gb/s single-ended	230 GB/s	3	3x 4B drive/ 4B receive	16 Gb/s differential	384 GB/s
DMI memory link	8	8x 1B drive/ 2B receive	9.6 Gb/s differential	230 GB/s	8	8x 1B drive/ 2B receive	9.6 Gb/s differential	230 GB/s
A-bus SMP link	3	3x 2B drive/ 2B receive	6.4 Gb/s differential	76 GB/s	4	4x 2B drive/ 2B receive	25 Gb/s differential	400 GB/s
PCIe	2 Gen3	2x 2B drive/ 2B receive	Gen3 8 Gb/s differential	64 GB/s	3 Gen4	3x 2B drive/ 2B receive	Gen4 16 Gb/s differential	192 GB/s
Total bandwidth	600GB/s				1,206 GB/s			

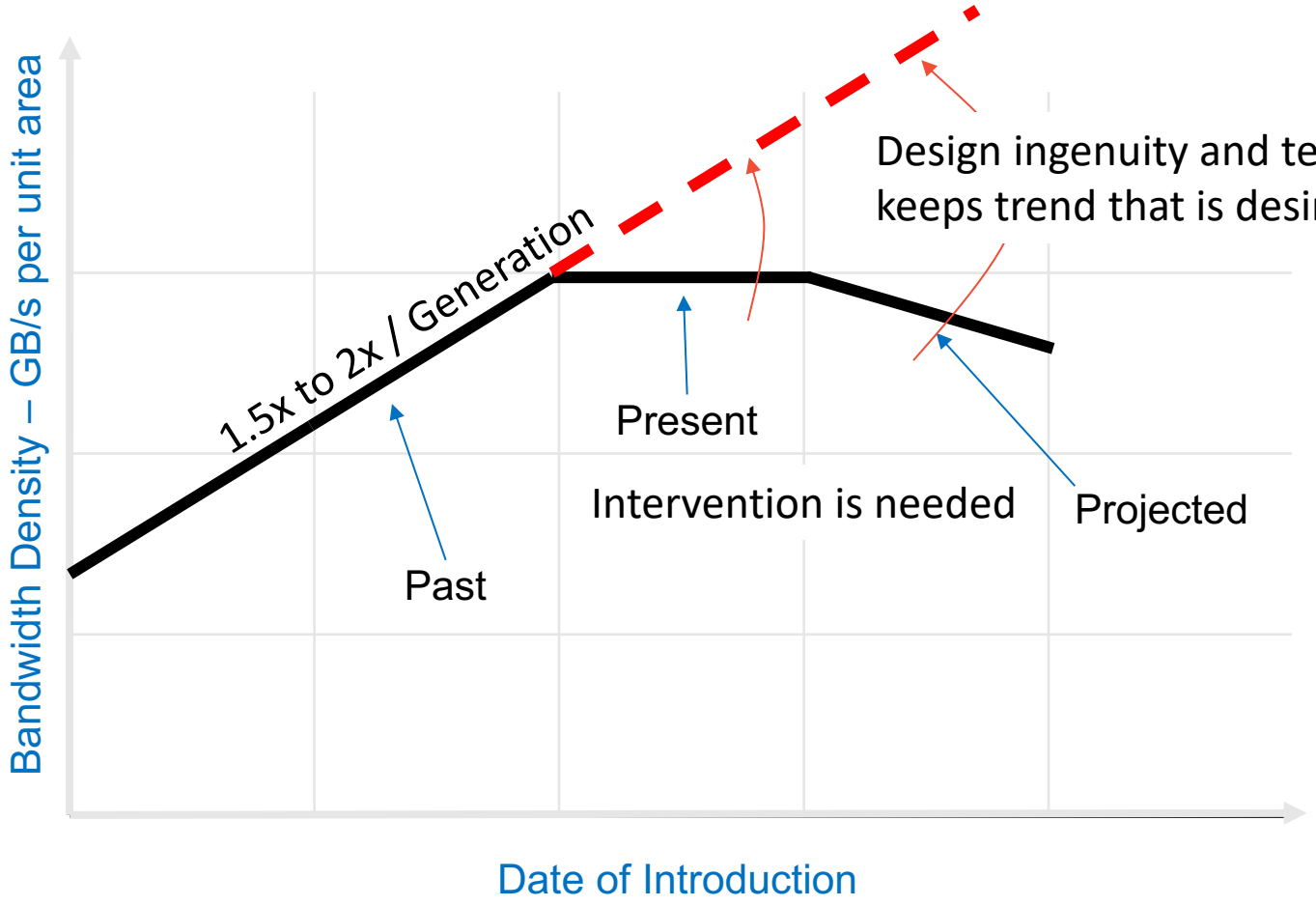
S. Chun et al., "IBM POWER9 package technology and design," in IBM Journal of Research and Development, vol. 62, no. 4/5, pp. 12:1-12:10, 1 July-Sept. 2018, doi: 10.1147/JRD.2018.2847178.

Socket Pin Assignment

- Signal Pins
  - More pins = more bandwidth
- Power Pins
  - Lower voltage levels require more pins due to higher current
- Reference Pins
  - Higher frequencies require better isolation between signal pins



Reaching a bandwidth breakpoint at the socket level

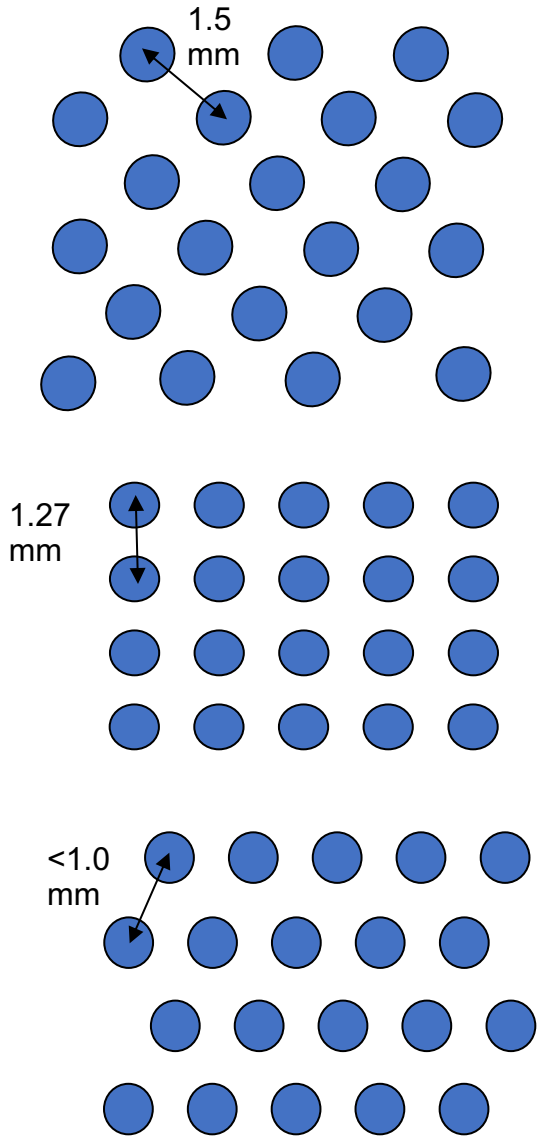


Maintain the trend

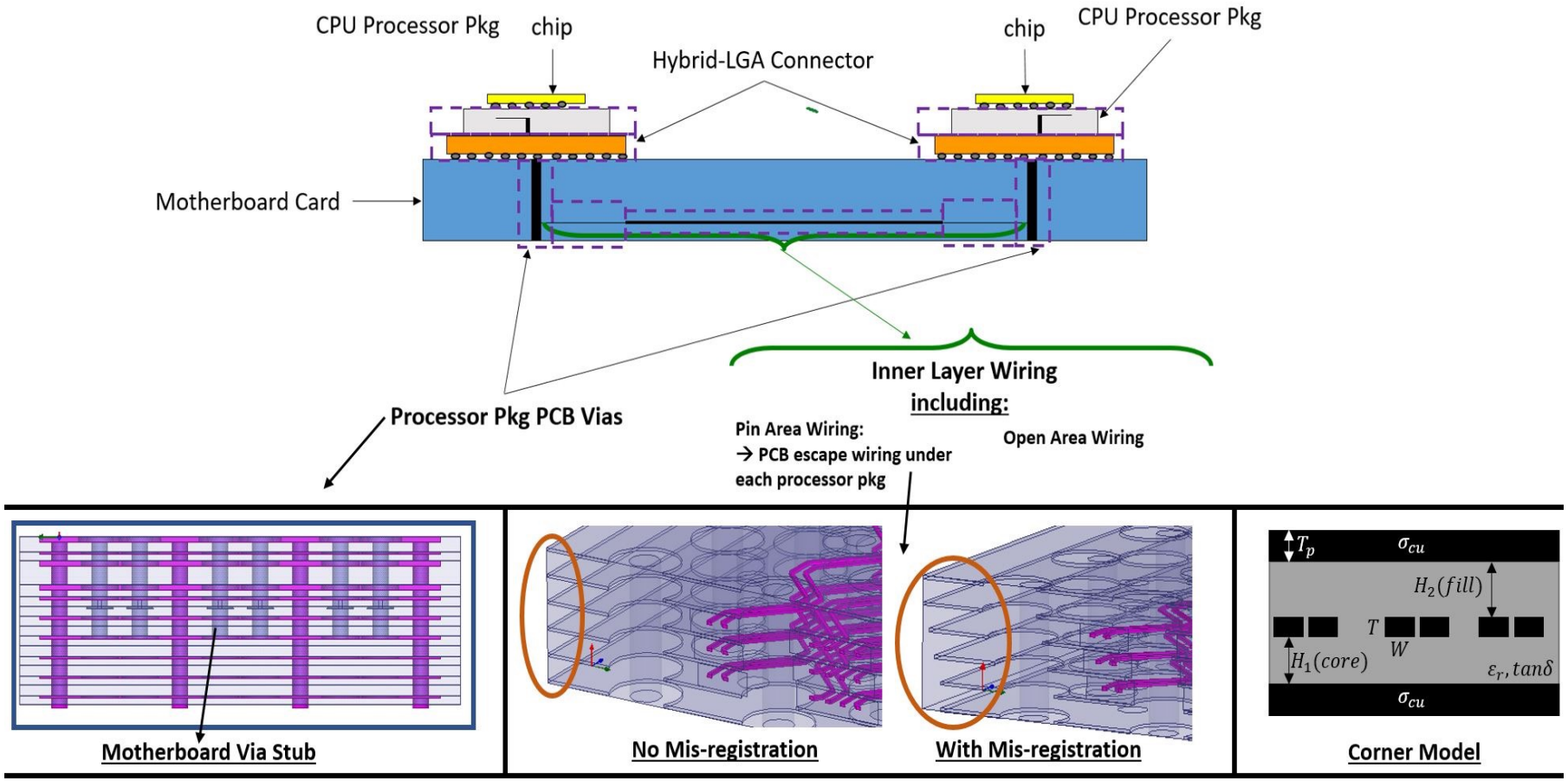
- Tighter pin field pitch - more contacts
- Larger substrates – more contacts to mitigate effect
- Maintain data rate growth with
  - Signaling technology
  - Circuit equalization
- Improve data rate capability with improved physical structures for Z_0, reflections, and crosstalk

Pin Density Increases Incrementally

- Over 20 years
  - 1.5 mm min pitch interstitial
  - 50 mil (1.27 mm) square
  - 1 mm square
  - 1 mm min pitch hexagonal
  - <1.0 mm min pitch hexagonal
- Sockets are pin limited
- Crosstalk needs to be managed
- Reflections need to be minimized



Components of a channel with hLGA

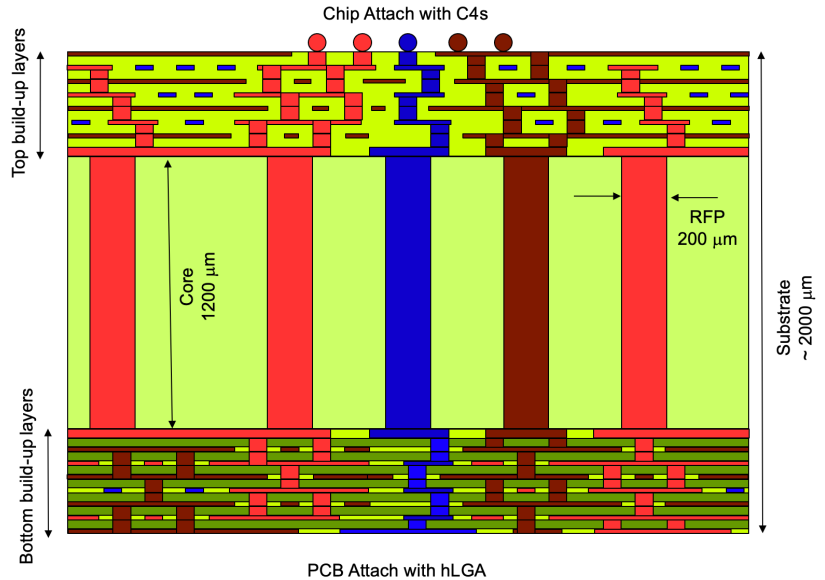


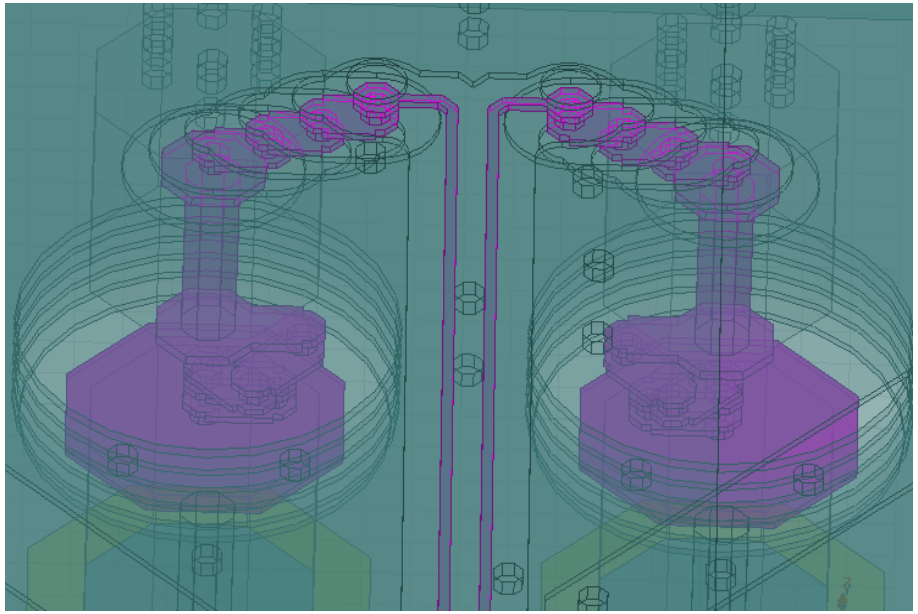
P9 XBUS high-speed channel topology

M. Swaminathan, H. M. Torun, H. Yu, J. A. Hejase and W. D. Becker, "Demystifying Machine Learning for Signal and Power Integrity Problems in Packaging," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 10, no. 8, pp. 1276-1

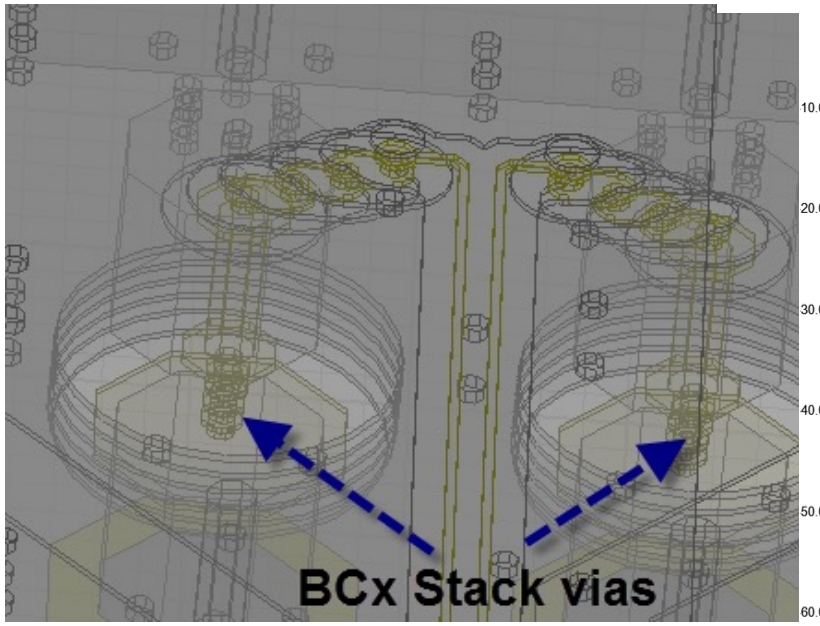
Package Design for Signal Integrity – PTH to BGA/LGA Pads

- Maximize signal bandwidth while meeting mechanical reliability requirements (Benefit of Stacked Vias on Bandwidth)
- Evaluate two options using ANSYS HFSS

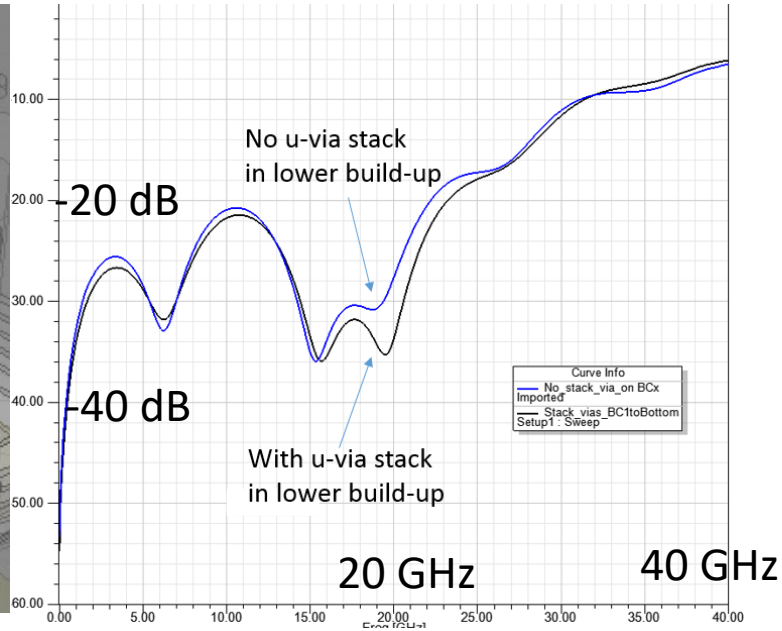




Staggered vias on bottom layers



Stacked vias on bottom layers

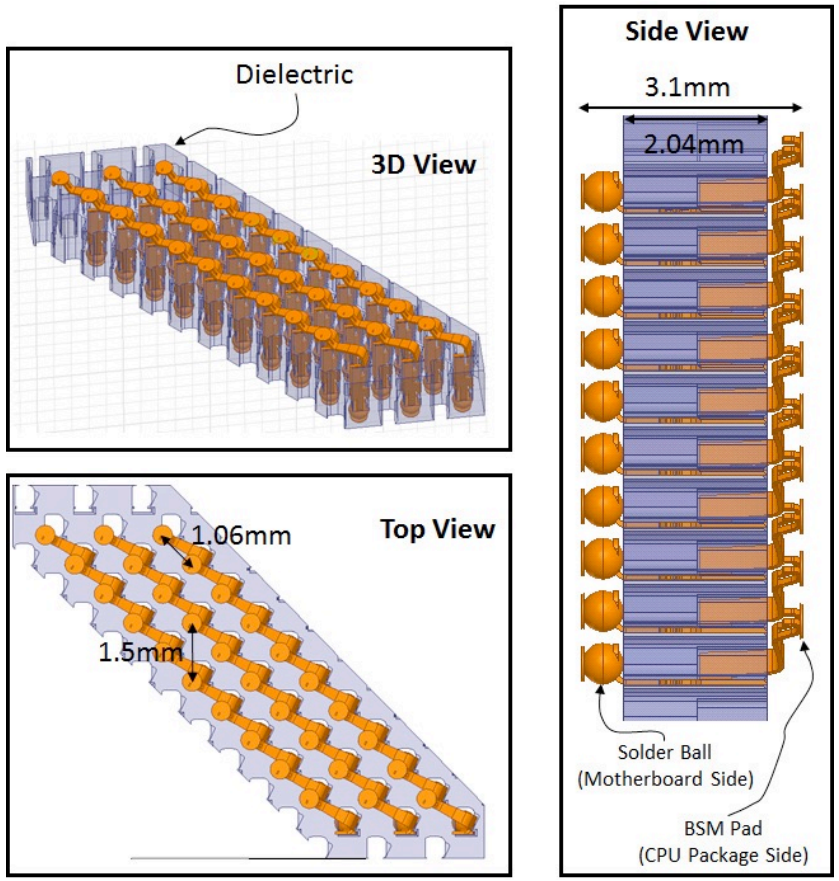


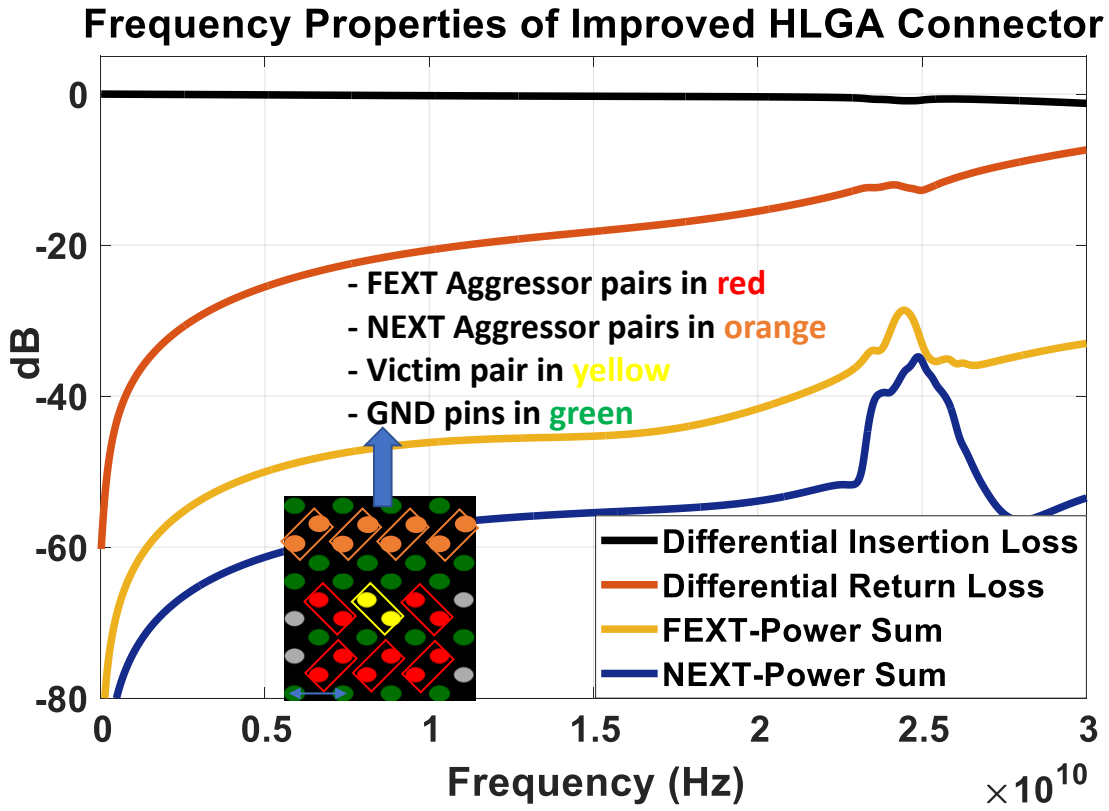
Return Loss Comparison

S. Chun et al., "Package and Printed Circuit Board Design of a 19.2 Gb/s Data Link for High-Performance Computing," 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), 2017, pp. 1701-1707, doi: 10.1109/ECTC.2017.170.

HLGA Socket Connector Design and Performance

Views of a sample HLGA connector section*
(for illustrative purposes only):



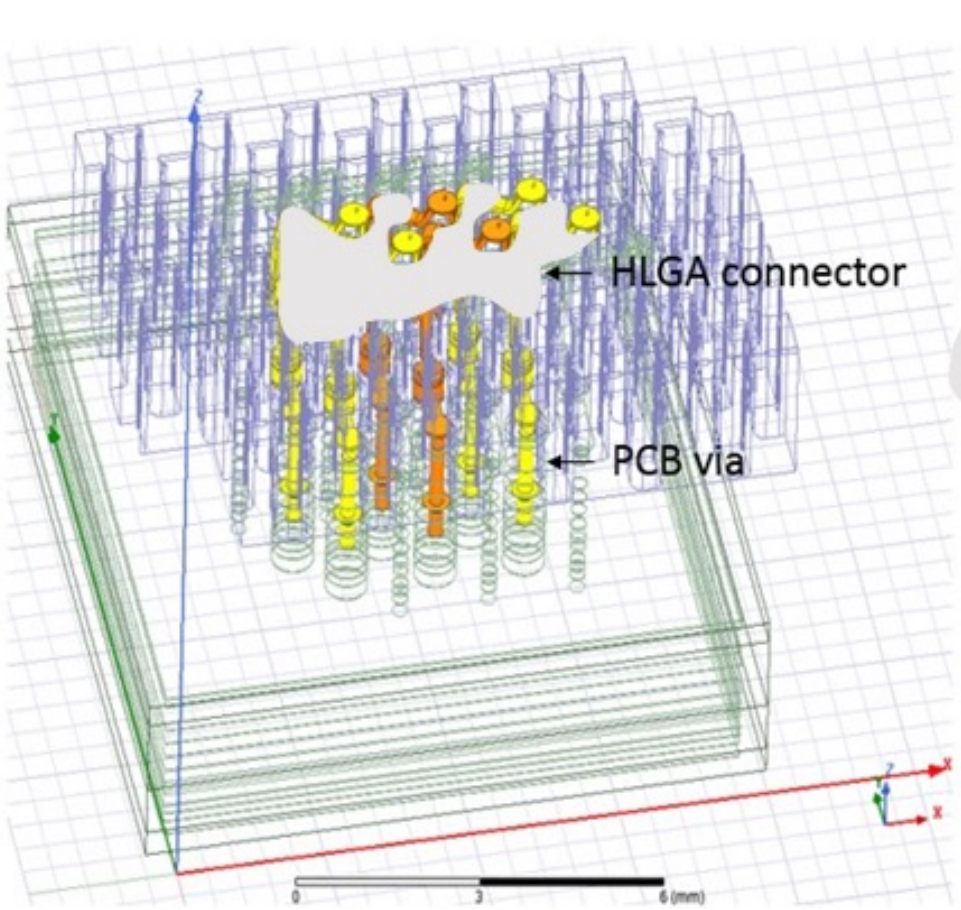


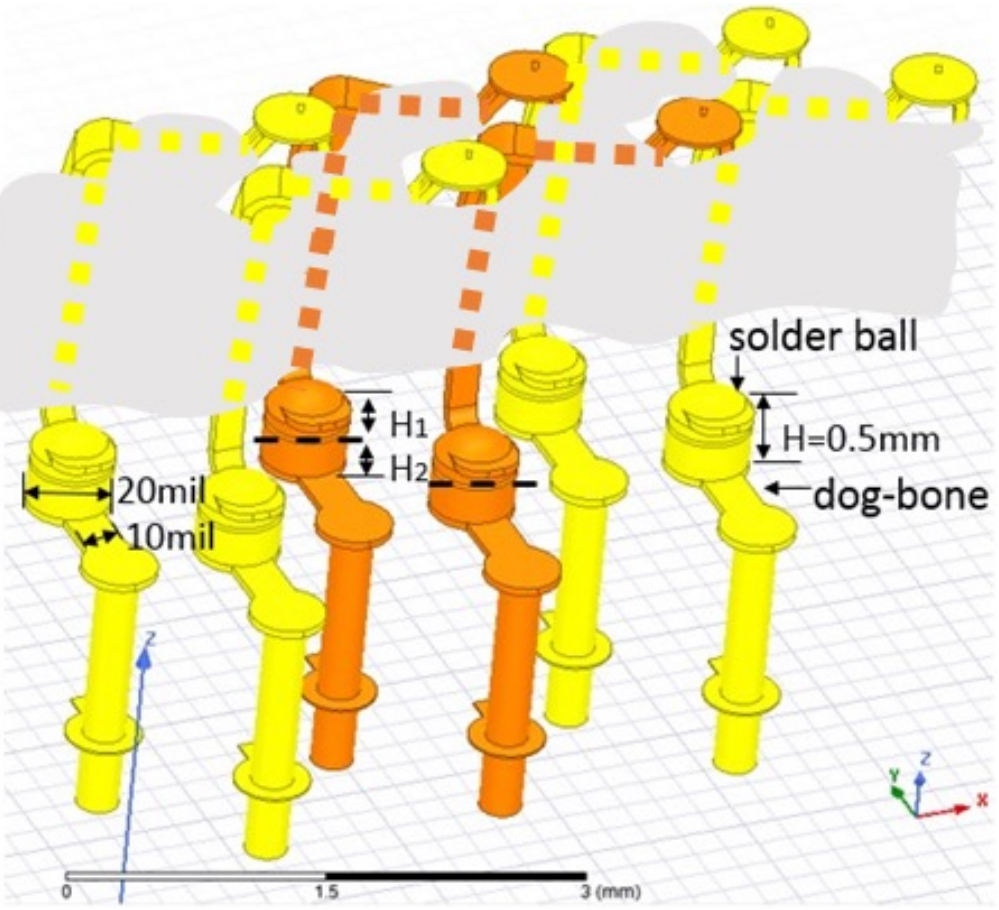
Differential IL < 0.4dB
Differential RL < 14 dB
FEXT Power sum < -38 dB
NEXT Power sum < -50 dB

up to 22 GHz

- J.A. Hejase et al., "A Hybrid Land Grid Array Socket Connector Design for Achieving Higher Signaling Data Rates", 2017 IEEE 26th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, 2017, pp. 1-3.
- P. R. Paladhi et al., "SI Model to Hardware Correlation on a 44 Gb/s HLGA Socket Connector," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2020, pp. 1-3, doi: 10.1109/EPEPS48591.2020.9231393.

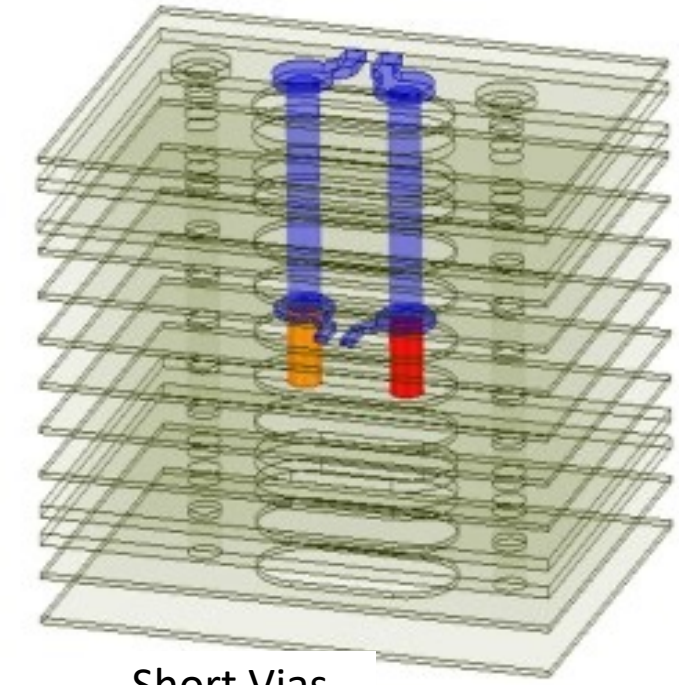
Socket Connector Routing to PCB Via



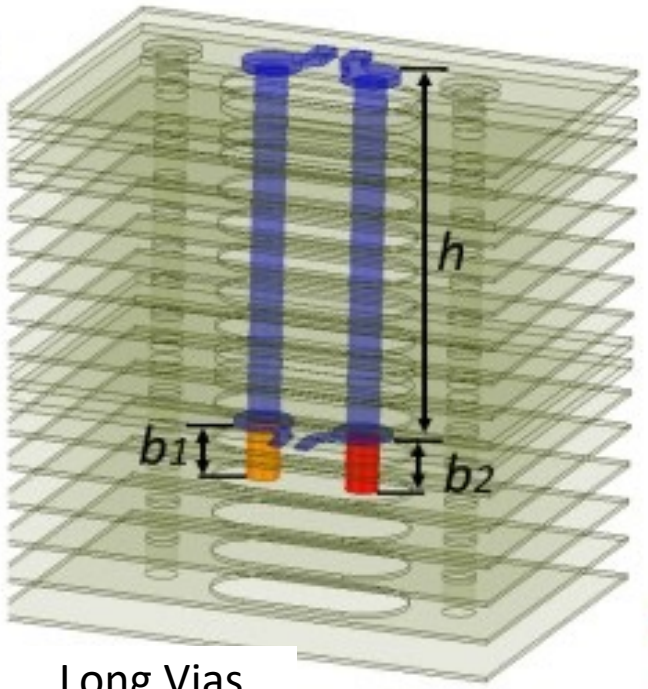


Y. Zhang, J. A. Hejase, J. C. Myers, J. J. Audet, W. D. Becker and D. M. Dreps, "3D Electromagnetic Modelling of Connector to PCB Via Transitions," 2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2018, pp. 99-101, doi: 10.1109/EPEPS.2018.8534304.

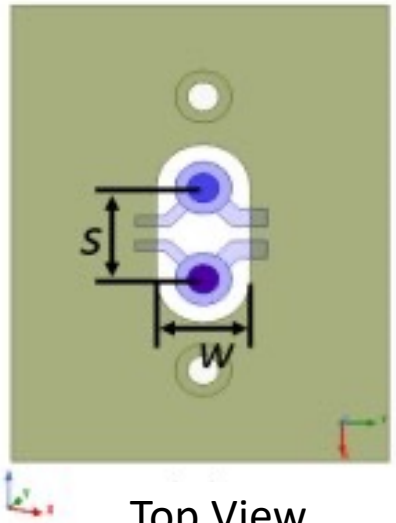
PCB Via Stub Control



Short Vias



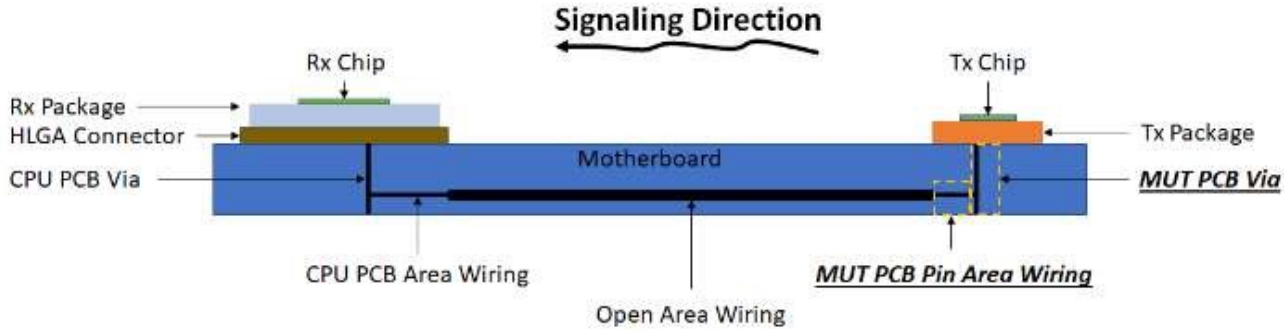
Long Vias

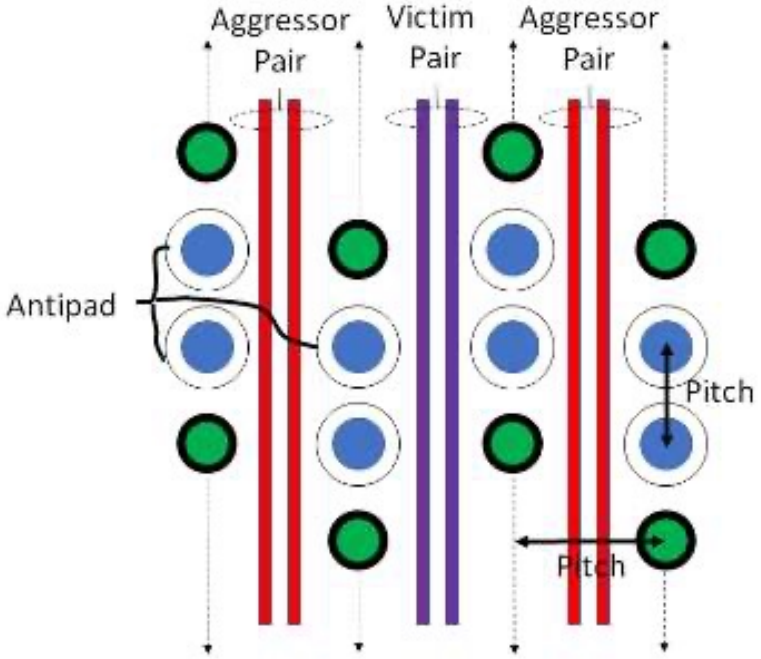


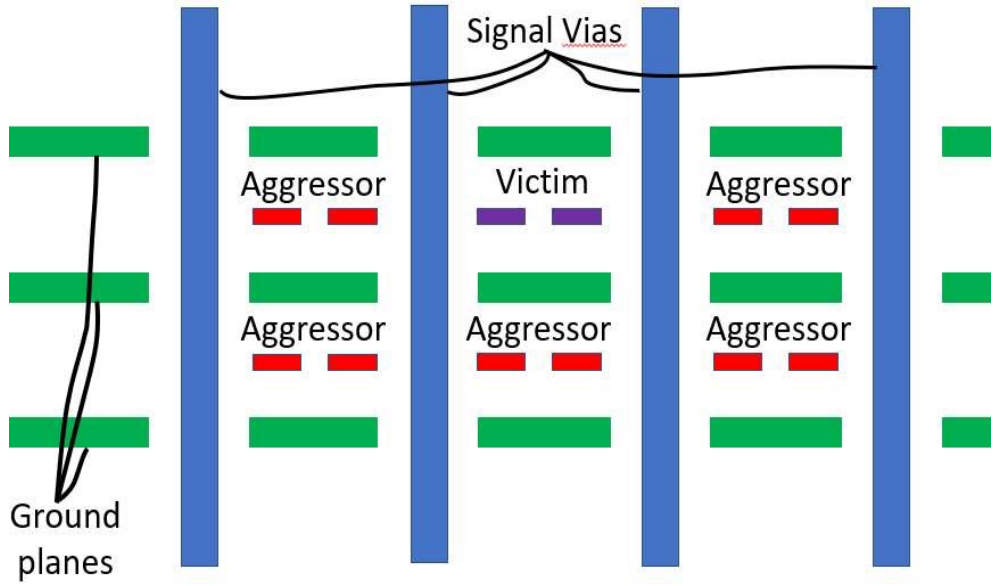
Top View

Y. Zhang, M. Bohra, N. Pham, P. R. Paladhi, W. D. Becker and D. M. Dreps, "Signal Integrity Characterization of Channels With Asymmetric Via Stubs," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2020, pp. 1-3, doi: 10.1109/EPEPS48591.2020.9231479.

Escape from PCB Via







J. C. Myers, J. A. Hejase, J. Tang, S. Chun, W. D. Becker and D. M. Dreps, "Signal Integrity Considerations of PCB Wiring in Tightly Pitched Module Pin Fields of High Speed Channels," 2019 IEEE 28th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2019, pp. 1-3, doi: 10.1109/EPEPS47316.2019.193216.

Socket Pin Projections

Link to Chapter 22:
https://eps.ieee.org/images/files/HIR_2021/ch22_2D-3D.pdf

- My Observations
  - Projected number of socket pins have grown dramatically in the last 5 years
    - Highlight 2025 projection below
- Opportunity
  - top of substrate escape
  - co-packaged optics
- Socket size will increase
- Adds to cooling challenge

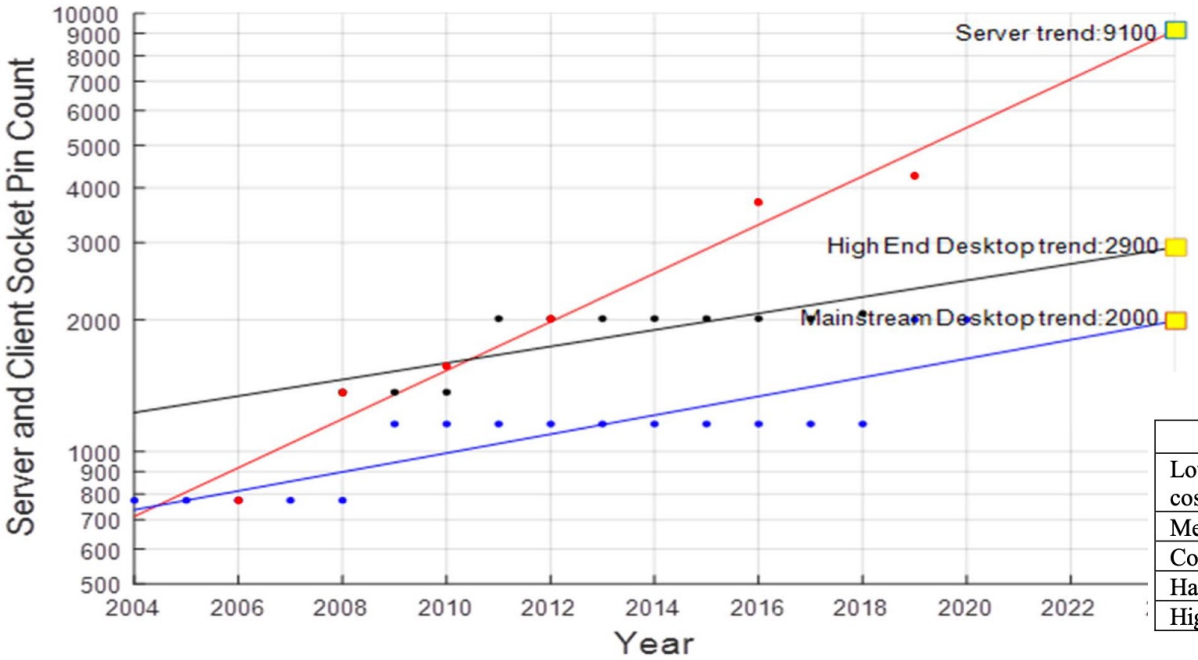


Figure 3: Near term trend graph based on actual pin count evolution. (Source: Intel)

Table 2a: Socket pin count projections from 2015 ITRS. [21]

	2019	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*	*2029*	*2030*
Low-end, Low-cost package	550	550	550	600	600	600	600	600	650	650	650	650
Memory (MCP)	260	280	280	280	280	280	280	280	280	280	280	280
Cost-performance	3200	3300	3400	3500	3600	3700	3800	3900	4000	4100	4200	4300
Harsh	693	728	764	803	843	860	877	894	911	928	945	962
High performance	5394	5651	5934	6231	6543	6855	7167	7479	7791	8103	8415	8727

Table 2b: Updated projections for socket pin count in the Cost-Performance and High-Performance segments.

	2019	2020	2021	2022	2025	2028	2031	2034
Cost performance	3200	3300	3400	3500	3800	4100	4400	4700
High performance	5125	5694	6302	6946	9105	11601	14434	17604

Co-Design Flow

HETEROGENEOUS INTEGRATION ROADMAP

VERTICAL

Bridge IC, Package, Board

Bridge System, Architecture, Layout

Bridge Synthesis, Analysis, Verification

Bridge Hardware, Software, Firmware

HORIZONTAL

Energy aware

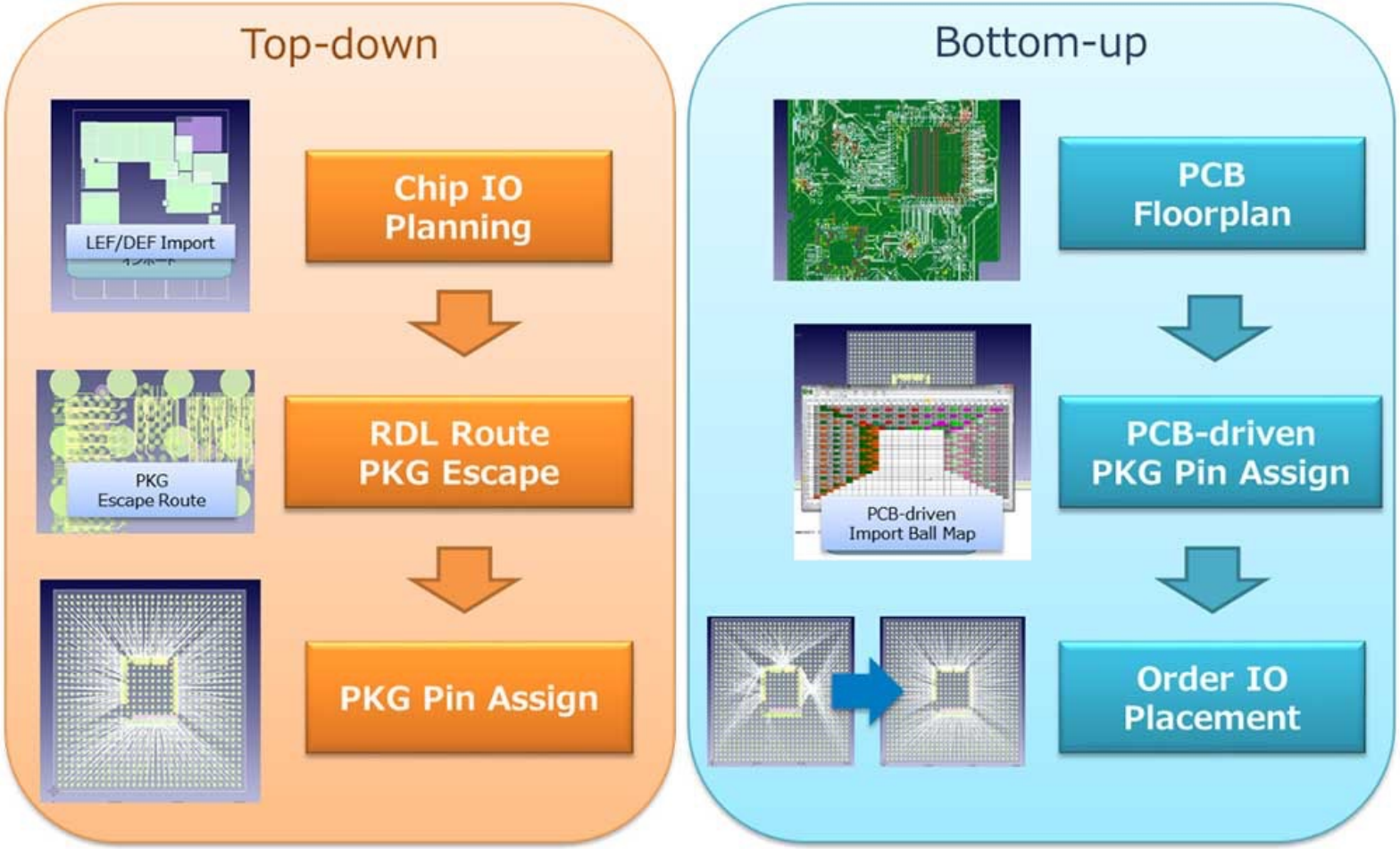
Signal/power integrity aware

Stress/thermal aware

Security aware

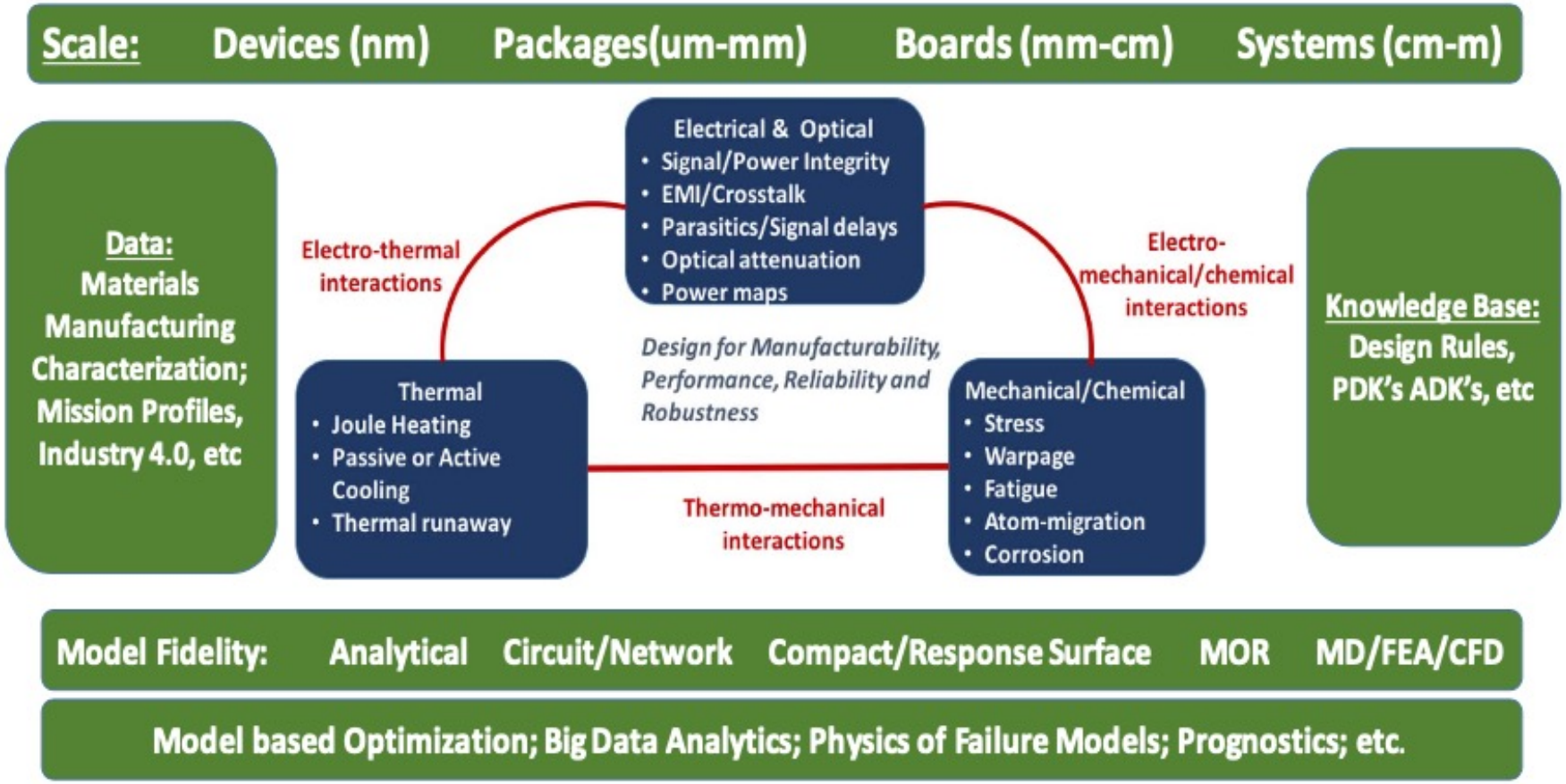
Testing aware

Link to chapter 13:
https://eps.ieee.org/images/files/HIR_2021/ch13_co-d.pdf



Modeling and Simulation

Link to chapter: https://eps.ieee.org/images/files/HIR_2021/ch14_ms.pdf

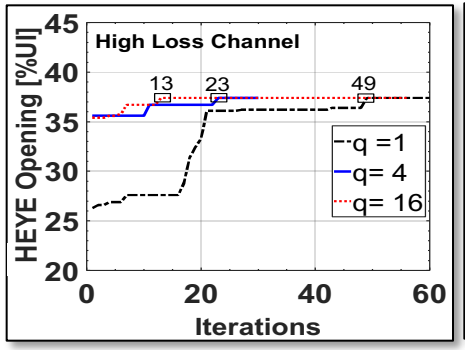


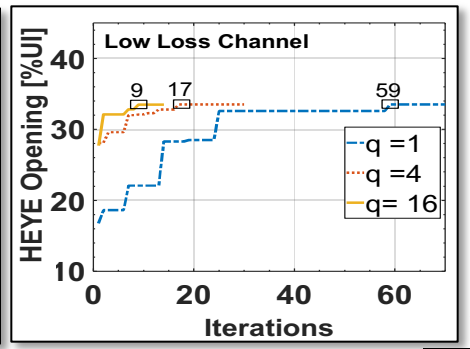
Chris Bailey, Chair

Parallel BAL-DO for RX Equalization Optimization-Results

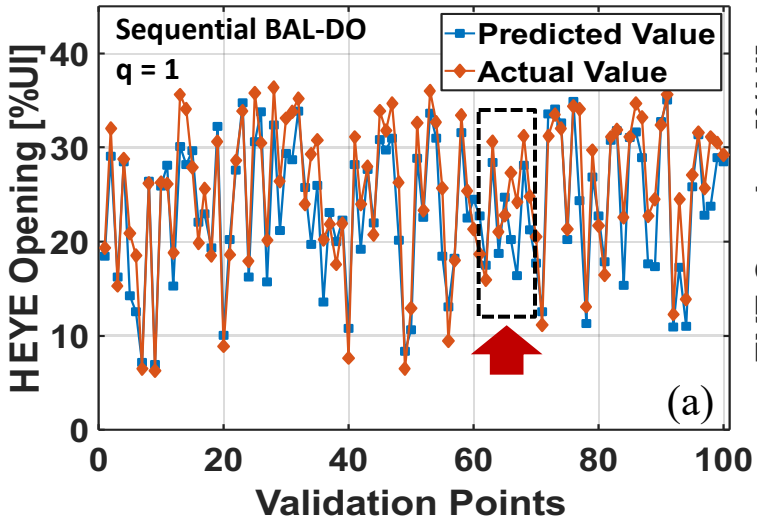
X. Yang et al.,
"Parallel Bayesian Active Learning using Dropout for Optimizing High-Speed Channel Equalization,"
2021 IEEE 30th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2021, pp. 1-3,
doi: 10.1109/EPEPS51341.2021.9609205.

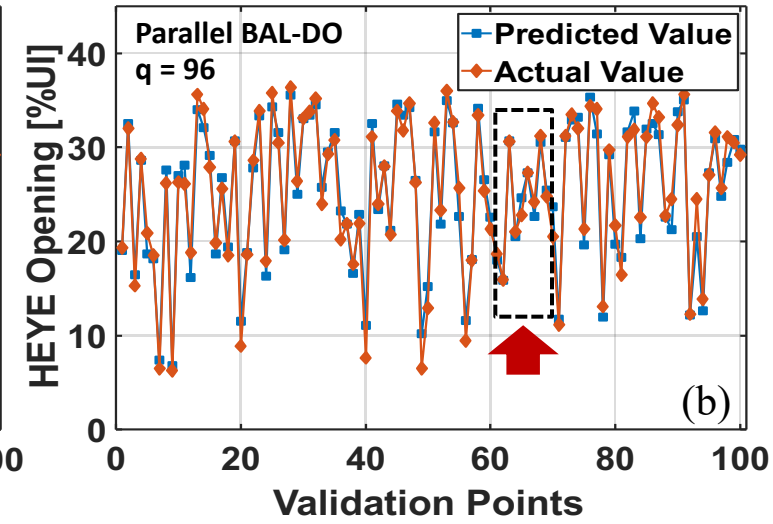
Rx Equalizations	# of settings
Long tail equalizer (LTE) gain	8
LTE zero	8
Continues time linear equalizer (CTLE) peaking 1	16
CTLE peaking 2	16
Total # of combinations	16384

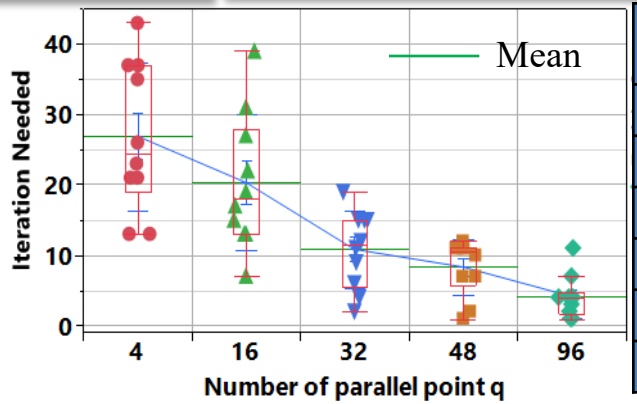




Uncertainty Prediction







Trend of iterations needed with different *q*

Parallel q Value	Iterations Needed (Mean)
1	49
4	26.9
16	20.3
32	10.8
48	8.3
96	4.1

	q=1	*q*=16	*q*=96
Data from iteration	52	16	7
Mean of absolute error	2.92 %UI	1.83 %UI	1.10 %UI
Std dev of absolute error	2.39 %UI	1.55 %UI	0.94 %UI

Opportunity for you - The HIR Chapters

HETEROGENEOUS INTEGRATION ROADMAP

✓Chapter 1 Overview	✓Chapter 2 High Performance Computing	Chapter 4 Medical	Chapter 5 Automotive
Chapter 6 Aerospace & Defense	Chapter 7 Mobile	Chapter 8 Single & Multi Chip	Chapter 9 Photonics
Chapter 11 MEMS	Chapter 12 5G	✓Chapter 13 Co Design	✓Chapter 14 Simulation
Chapter 15 Materials	Chapter 16 Emerging Devices	Chapter 17 Test	Chapter 18 Supply Chain
Chapter 19 Security	Chapter 20 Thermal	Chapter 21 SiP and Module	✓Chapter 22 Interconnects
Chapter 23 Wafer Level Packaging			

https://eps.ieee.org/hir

Participate - IEEE Technical Committee on EDMS

EDMS = Electrical Design, Modeling, and Simulation

https://cmte.ieee.org/eps-edms/

- To join the Technical Committee
  - Send email to EDMS-Chair@ieee.org
- Annual Conferences
  - SPI – Europe, May
  - EPEPS – North America, October
  - EDAPS – Asia, December
  - DTMES – Africa – It's great to see this started
- Benchmark Subcommittee
  - Provide benchmark designs for methodology development
- Distinguished Lecturers available
- See web site for more details

Summary

- Fundamentals of Electrical Design
  - Input: Physical parameters -> electrical models
  - Signal Distribution and Power Distribution are inter-related and inter-dependent
  - Advances in semiconductor technology drive system advances
  - Engineering ingenuity to minimize noise and reflections creates differentiated systems
  - Output: Verified design, build data, performance analysis, test patterns
- Engineering ingenuity
  - Cost-efficient design and trade-offs levering and driving technology development
- Example – Processor Socket with hybrid Land Grid Array (hLGA)
  - Bandwidth density increase of 1.5x to 2x per processor generation drives innovation
- Heterogeneous Integration of Packaging and the HIR Roadmap
  - Opportunity to apply design ingenuity to technology advances
- How you can get involved, learn, and give back to the community
  - HIR – Heterogeneous Integration Roadmap
  - IEEE EPS Society and the Technical Committee on Design, Modeling, and Simulation (EDMS)