Introducing...

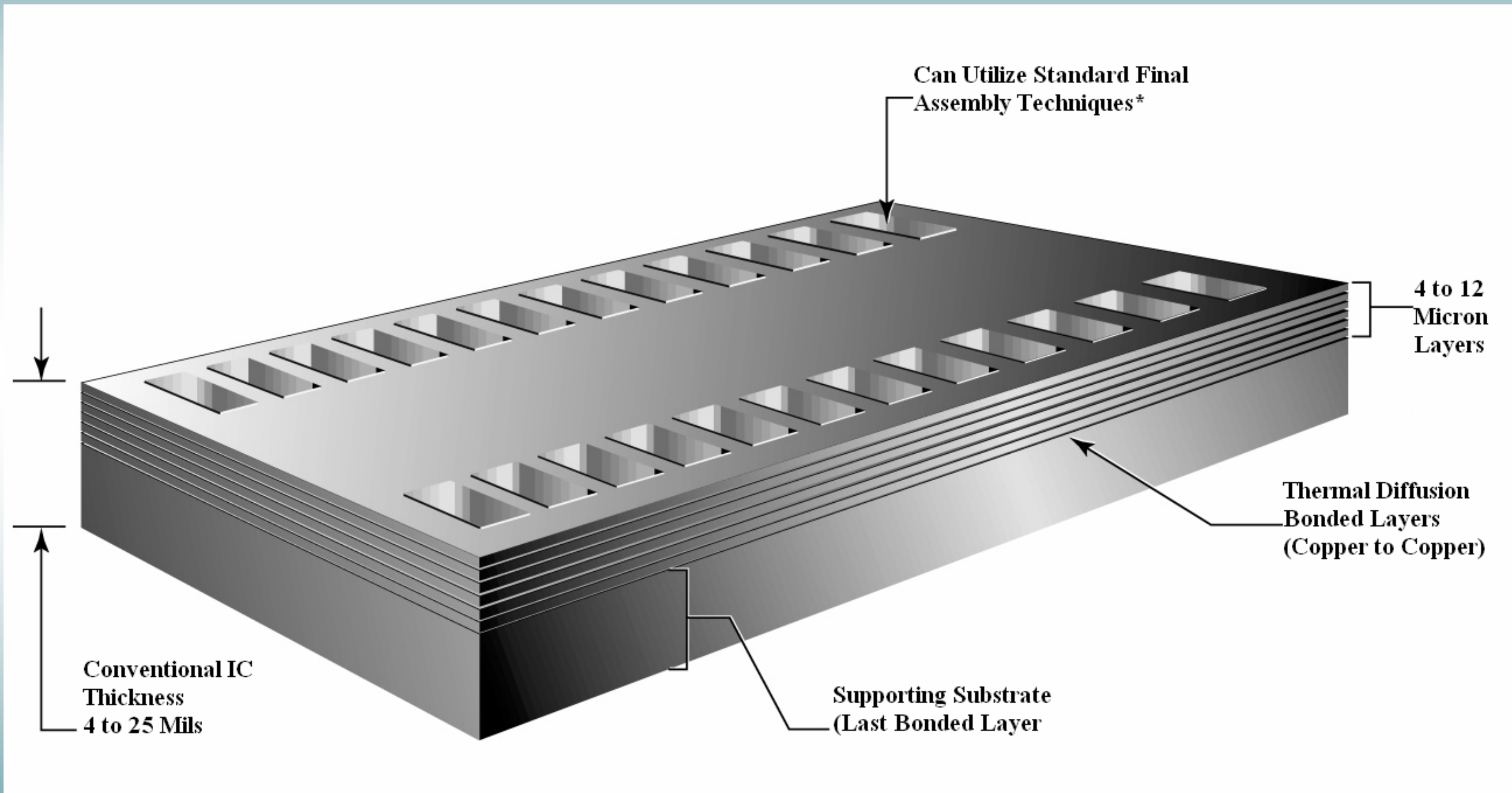
Wafer Level Stacking

The Brave New World of Very Advanced Packaging

Robert Patti

Tachyon Semiconductor

The Punch Line



TACHYON SEMICONDUCTOR

Advantages Of Wafer Level Stacking

- Density
- Speed
- Power
- Cost

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Tachyon's Competitive Advantage

	Today	Tachyon[1]
Access Time (nanoseconds)	45/6/6/6	8/4/4/4[2]
Density	256 Megabit	1 Gigabit
Cost	$0.204 per Megabyte	$0.10 per Megabyte[3]

Footnotes:

1 Chips are families; scalable capacity up / down

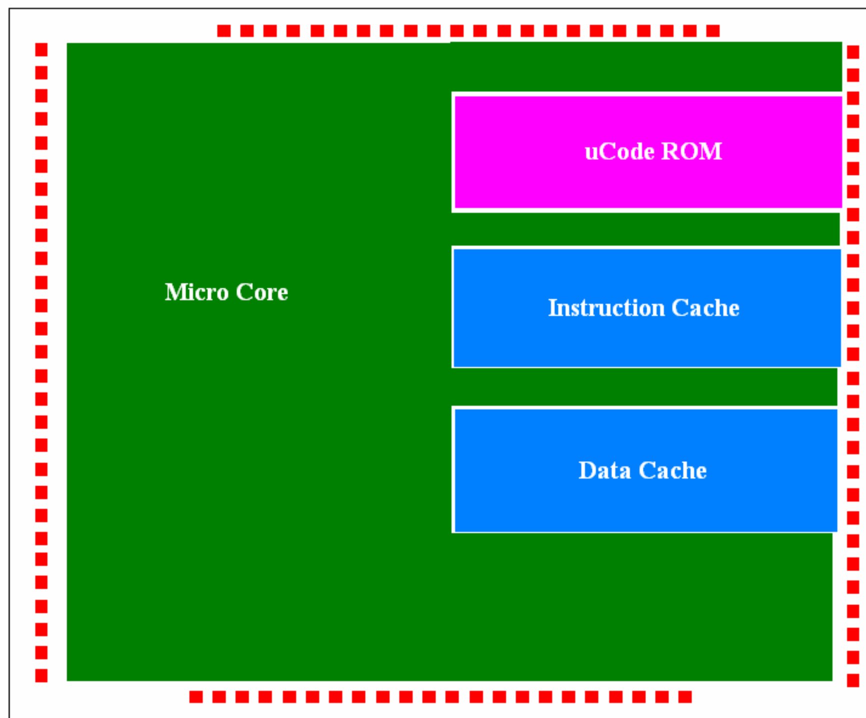
2 High speed interface

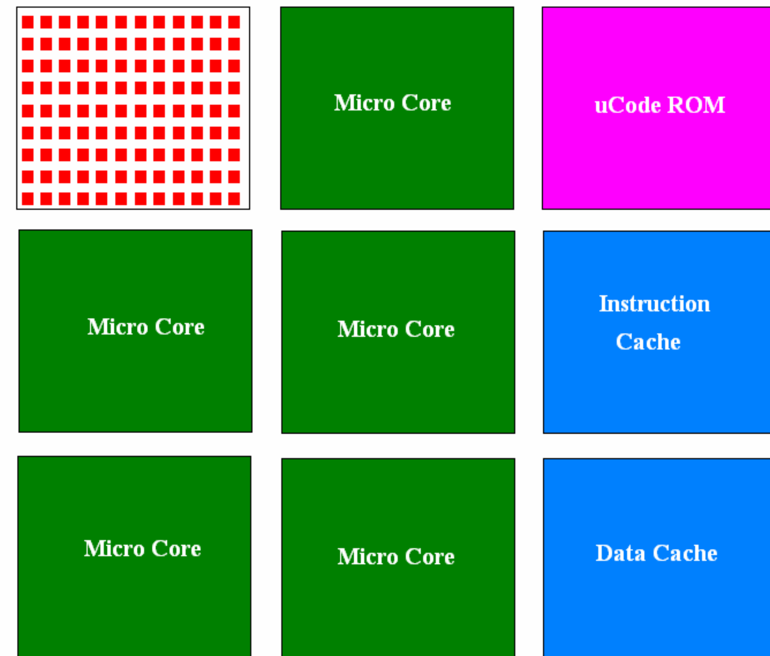
3 Tachyon's manufacturing cost; assumes same 0.18 µ process

Higher Density

- Process Differentiation
- Relative Die Size Shrinks by 1/nLayers

Assume a Microprocessor





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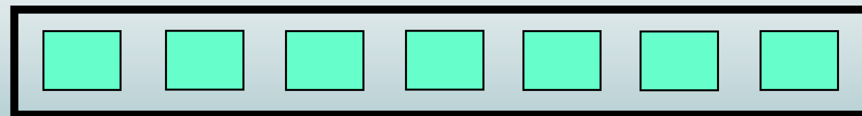
Conventional Stacking

– **Chip Scale Packaging** (“CSP”):
  - Make each single-layer chip
  - Wire them together
  - Connect on the edges

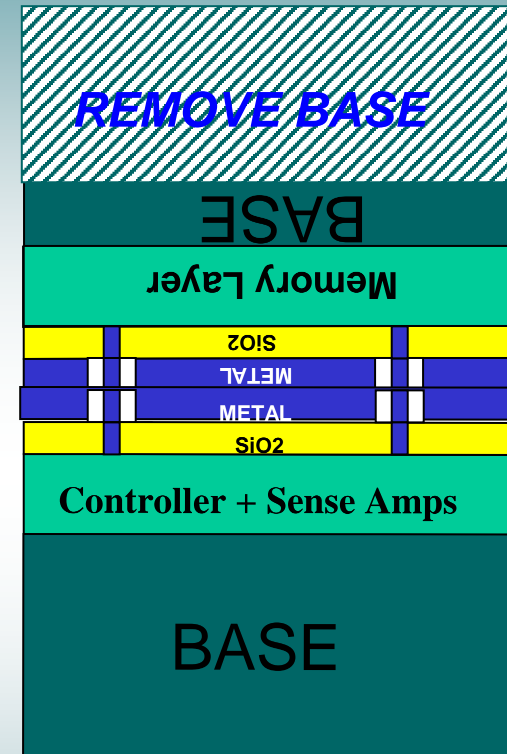
– **Multi-chip Carrier Modules** (“MCM”):
  - Bundle several chips together into a single package



Less than 1,000 interconnects possible with either approach

Tachyon Stacking

- Completely different approach:
  - Align & bond wafers
  - Connect wafers internally (VIAs)
  - Thin the active layer (12μ or less) (by backgrinding, spin etch, CMP)
  - Repeat process adding layers
  - Cut into chips

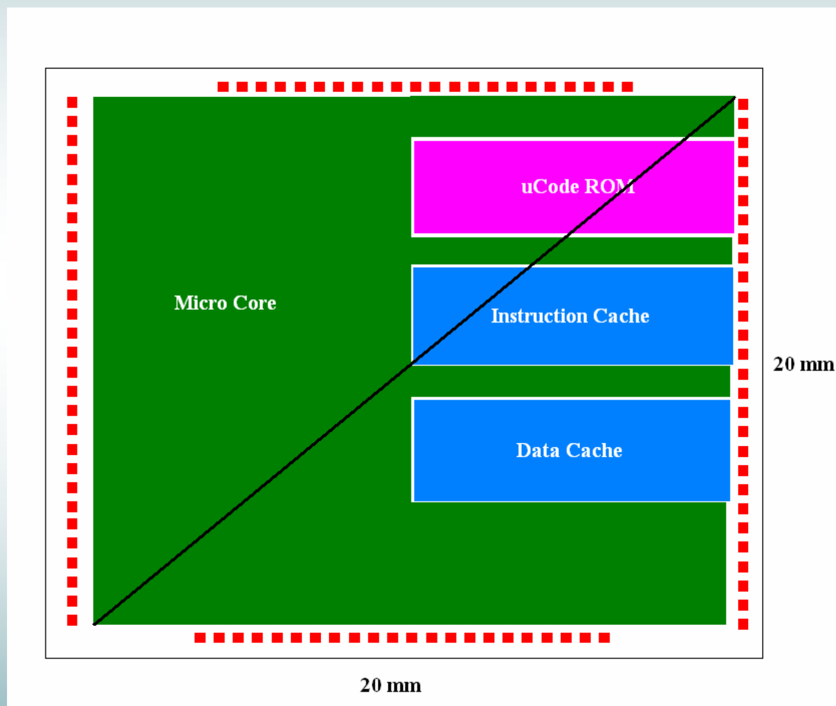


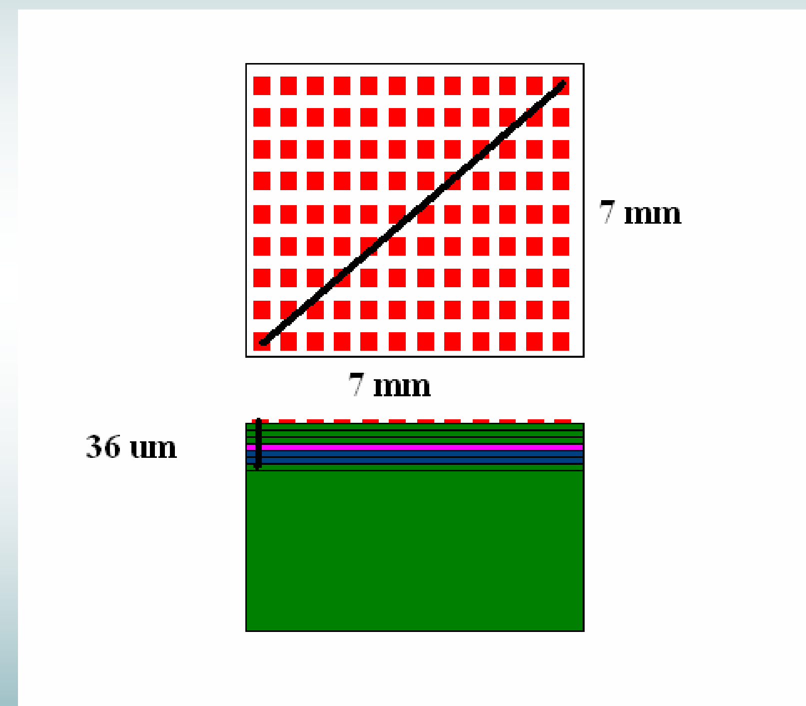
Hundreds of thousands of interconnects possible with this proprietary, patented stacking system.

Higher Speed

- Process Differentiation
- Lower I/O and Power/Ground Inductance
- Much Shorter Interconnect

Wire Length Reduction ------20/7 ………. 2.8x Faster





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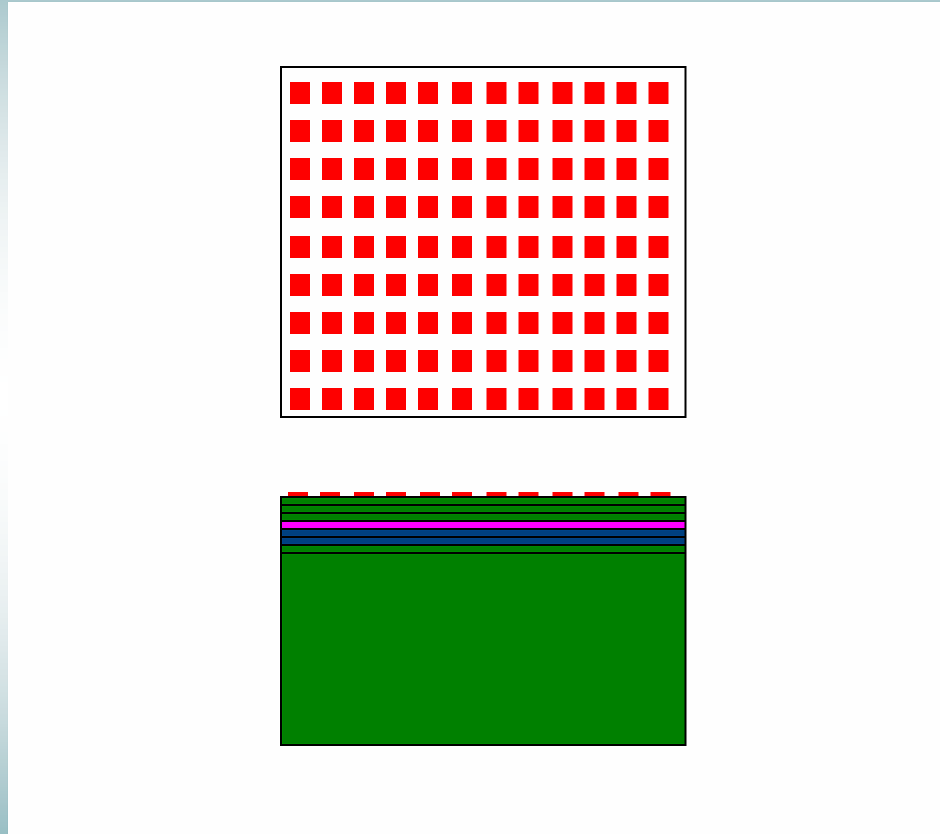
Lower Noise/Ground Bounce



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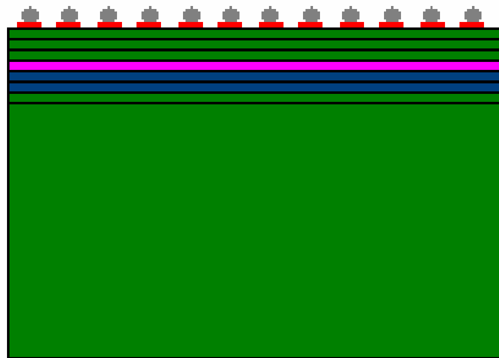
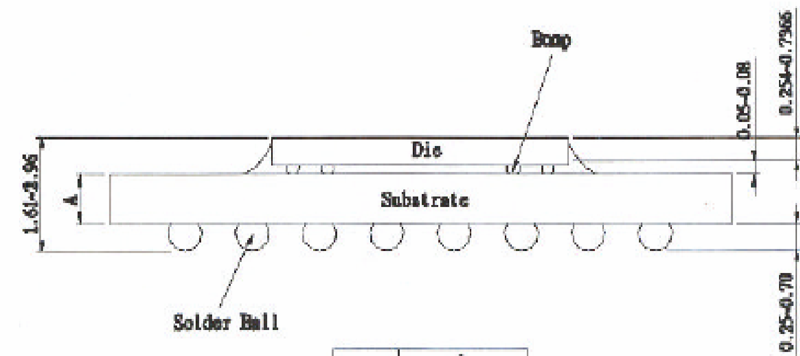


Cross-section of FC-BGA

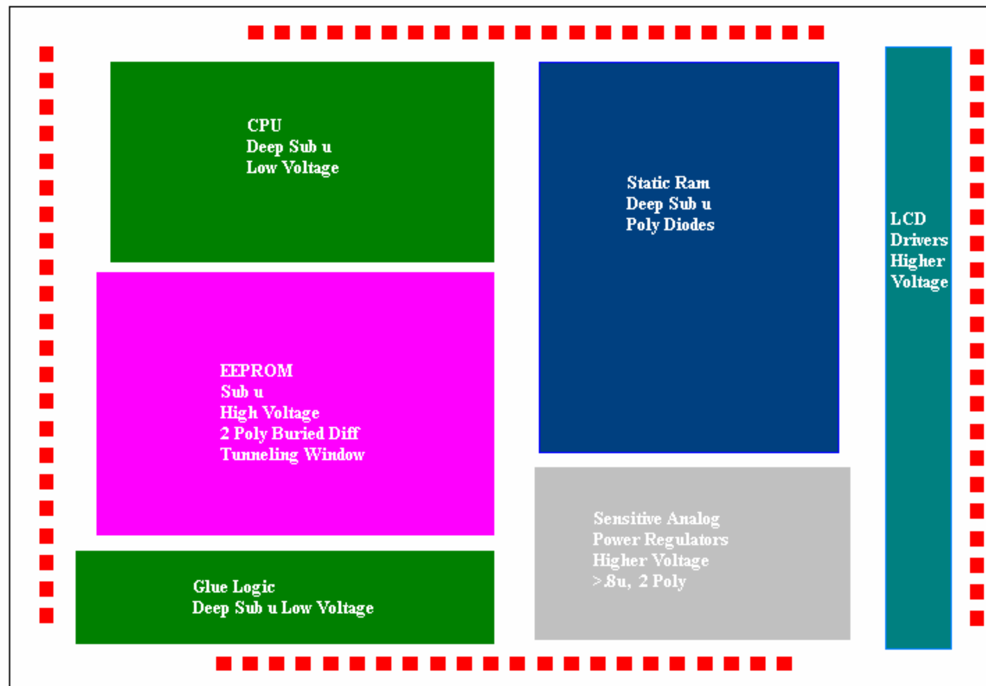


	A
1+2+1	1.0+/-0.1
2+2+2	1.1+/-0.1
3+2+3	1.2+/-0.1
2+4+2	1.436+/-0.1

Lower Power

- Process Differentiation
  - Can Mix Geometries
  - Can Mix Process Performance
    - Low Leakage verses Low Threshold
- Less Wire – Less Capacitance

Mixed Micron



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Lower Cost

- Process Differentiation
  - Allows Process Simplification
- Less Packaging
- In Some Cases -- Higher Yield

Stacking Problem

Stacking reduces yields:

Industry average = ±50% yield on memory wafers

Stacking compounds the yield problem:

Yield of an n-layer stack = $(0.5)^n$

Impact:

For a 4-layer (stacked) chip:

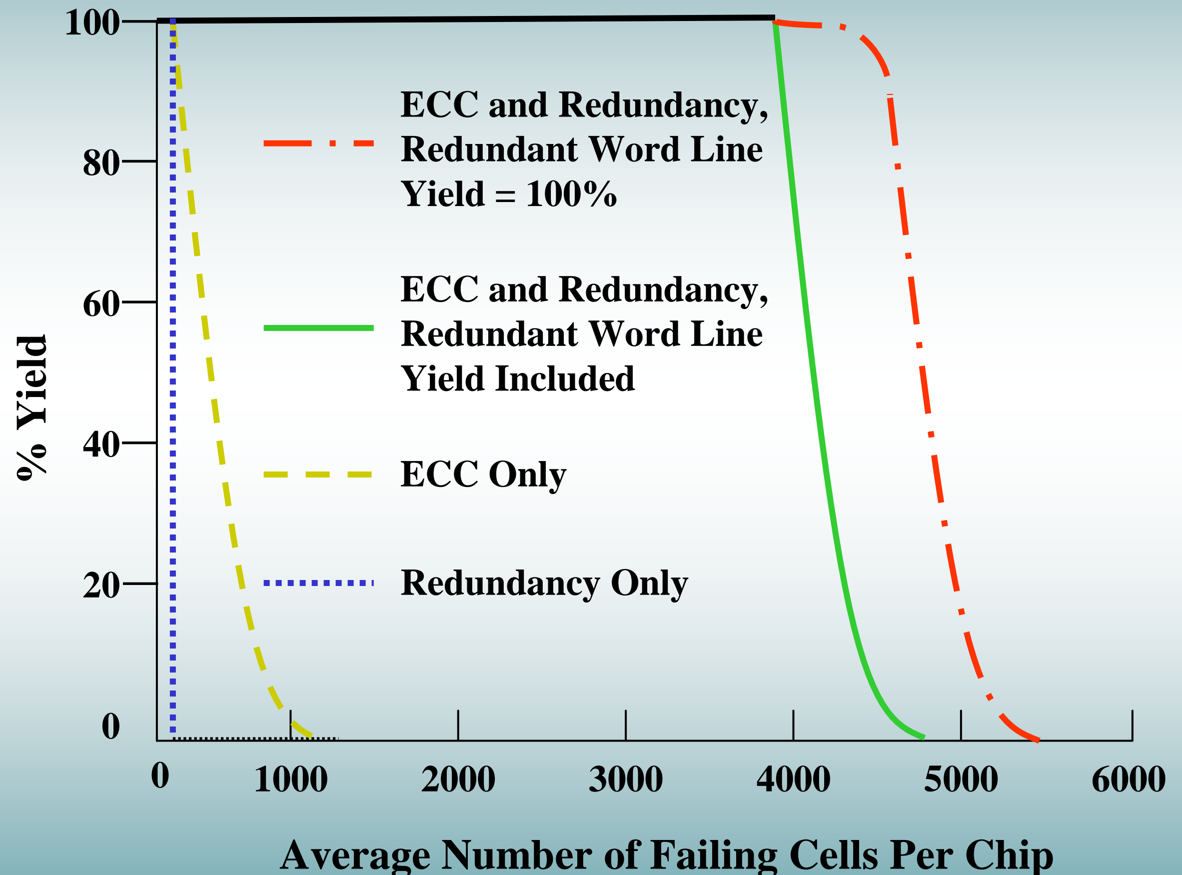
$$\frac{1}{16} = 6\% \text{ yield}$$

6% yield is not economically viable

Tachyon's Dynamic Reconfiguration

Tachyon's IP BiSTAR™ Delivers 97%+ Yields = Near doubling of fab capacity

Tachyon's wafers can tolerate higher numbers of failed cells because Tachyon's IP enables fine grain cell-by-cell re-mapping, rather than whole row or column trimming, to make repairs.



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Tachyon's IP Solves Yield Problems

Combine Tachyon's proprietary patented IP, called BiSTAR™:

- Self-test
- Error Correction
- Dynamic reconfiguration

Result:

Tachyon stacked wafers can tolerate >>10,000 bit errors per part.

(versus ~ 40 bit errors for competitors) and

produce ± **97% yields*** on a 32-layer stack

*Yield limitation based on predicted yield associated with controller wafer layer, and conservatively assumes 80% yield from mature .18μ Cu logic process.

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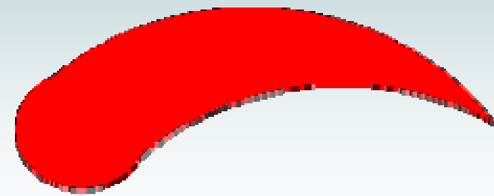
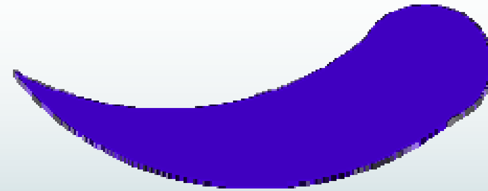


BiSTAR



BiSTAR ™ Technology

- Innovative way to improve the yield of highly parallel structures such as memory
- Basis: integration of intelligent self test, self repair
- Performs greater level of testing than normally available during normal chip or wafer level testing
- BiSTAR tests and compares < 300,000 nodes or bits/clock cycle; more than 1,000 times faster than can be achieved by any external memory tester

What Can BiSTAR Test & Repair?

- Bad memory cells
- Bad line drivers
- Bad sense amps
- Shorted word lines
- Shorted bitlines
- Leaky bits
- Bad secondary bus drivers
- Bad CAMS

BiSTAR HiRel for 3600/Forever

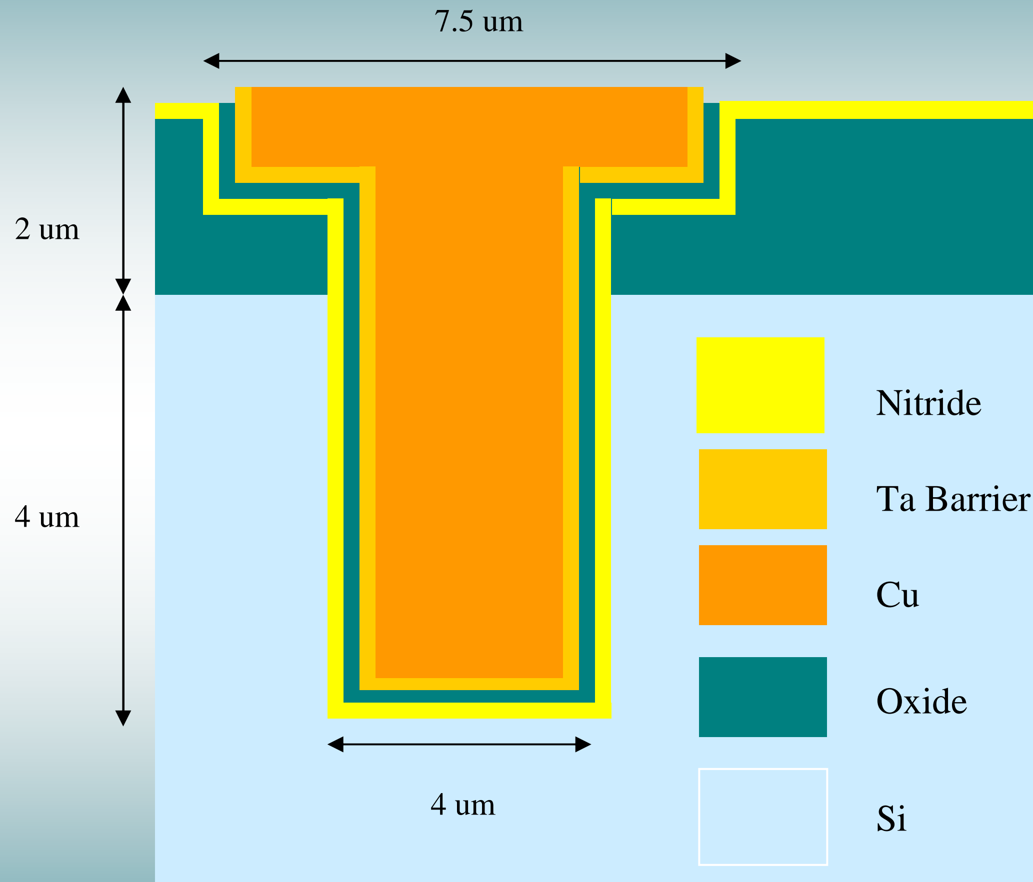
- Full test at every power on
- Dynamic reconfiguration and repair
- Internal ECC
- Self healing architecture
- Background memory scrubbing
- >2x bitline signal level
- SMBus compliant error and condition reporting
- Linked hot spare management capability

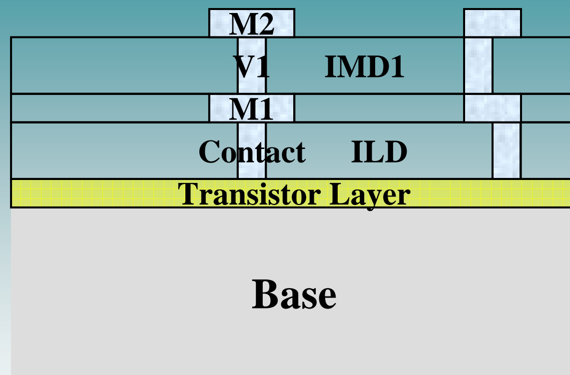
By The Numbers

- Comparator per bitline testing
- Peak internal bandwidth 60 Terabits/sec
- Maximum clock speed 200 MHz
- 192 full coverage nearest neighbor test
- 2 and 3 dimensional interaction test capable
- 20,000 spare rows
- 10,000 spare columns
- 4x internally semi hidden refresh
- Built in 66+ MIP CPU

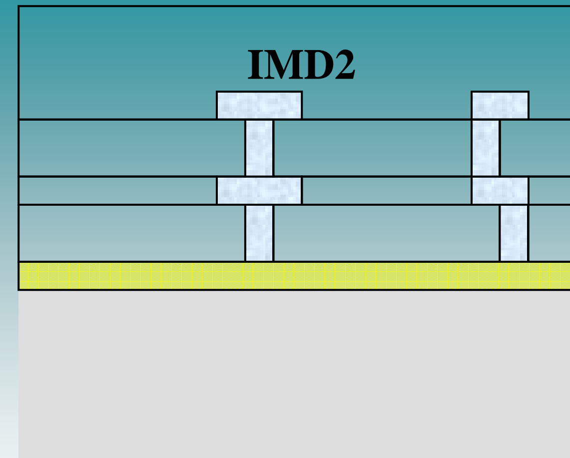
Stacking Process Update

Architecture of Super Via

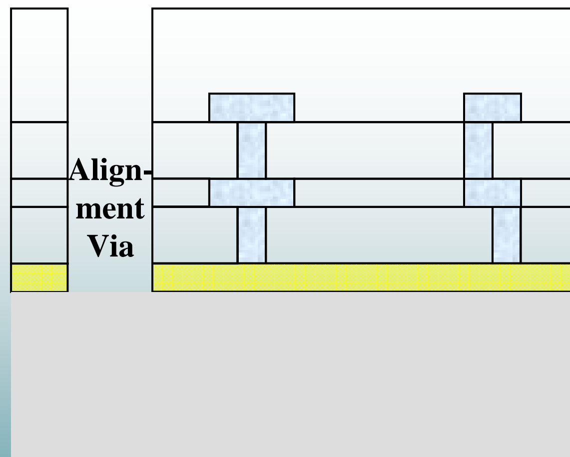




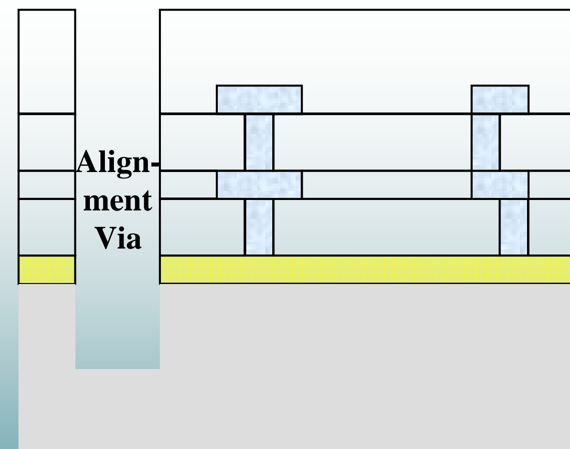
1. The process started with a product wafer having devices and 2-layer metal fabricated.



2. Firstly the wafer is deposited with IMD2 by HDP then the whole wafer is planarized.



3. An alignment via, with a size of ~ 2 μm, is masked and the whole stack of dielectric of ~ 4 μm is etched.



4. The Si Base is etched to a depth of from 4 to 9 μm, with part of the IMD2 as the hard-mask.

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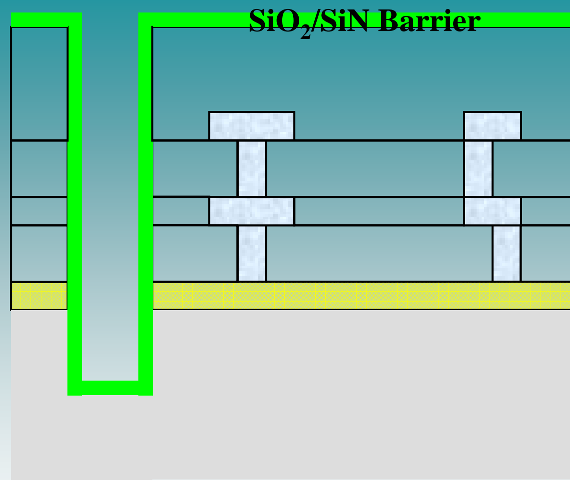
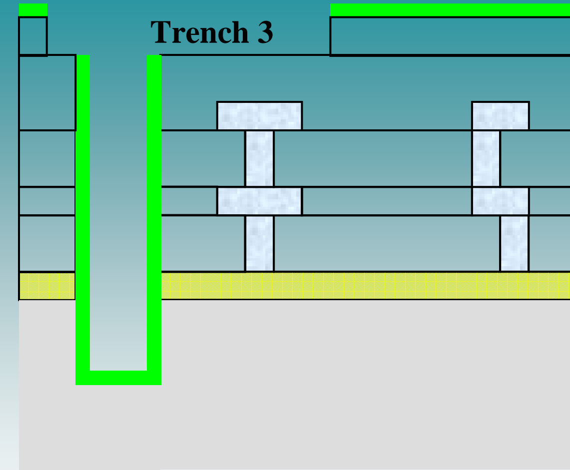
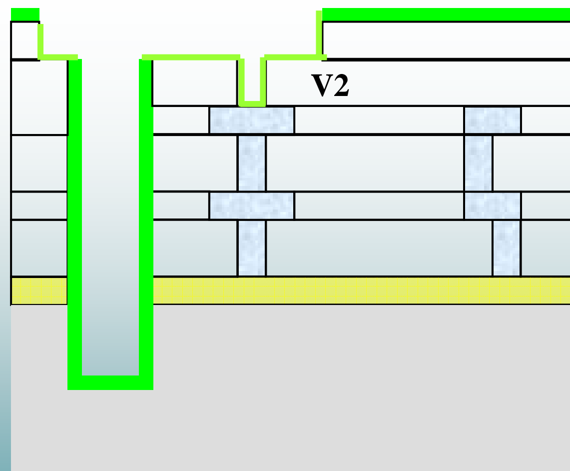


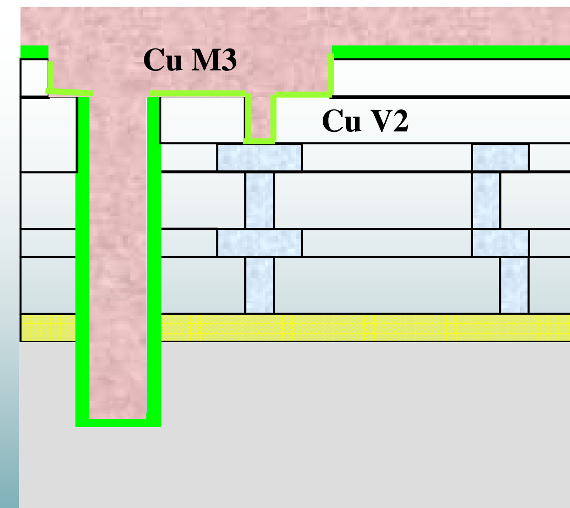
5. A layer of oxide (~0.05 to 0.10 μm) is deposited for insulation and then a layer of SiN (~0.05 to 0.10 μm) is deposited. SiN layer will act as a polish/etch stop and as an additional protection towards diffusion of Cu into Si.



6. The trench 3 of ~ 5 μm is masked and then etched (trench first dual damascene etching).



7. The Via 2 of ~ 2 μm is masked and etched.



8. Then Ta or TaN barrier and Cu seed is deposited, followed by Cu Electrochemical Plating (ECP).

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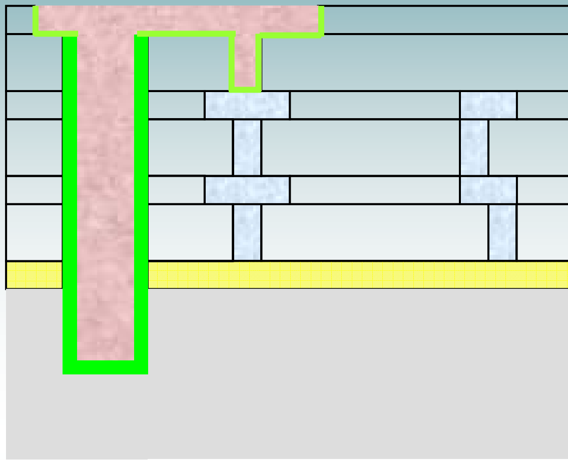
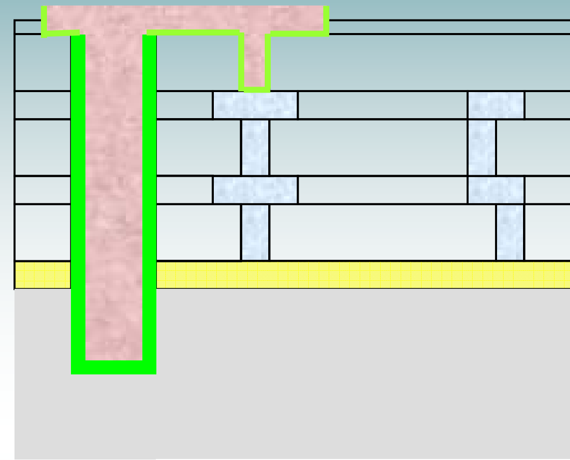


9. The excess Cu is removed by CMP.



10. Either the trench dielectric is recessed or Cu M3 is elevated by selective eletroless deposition.

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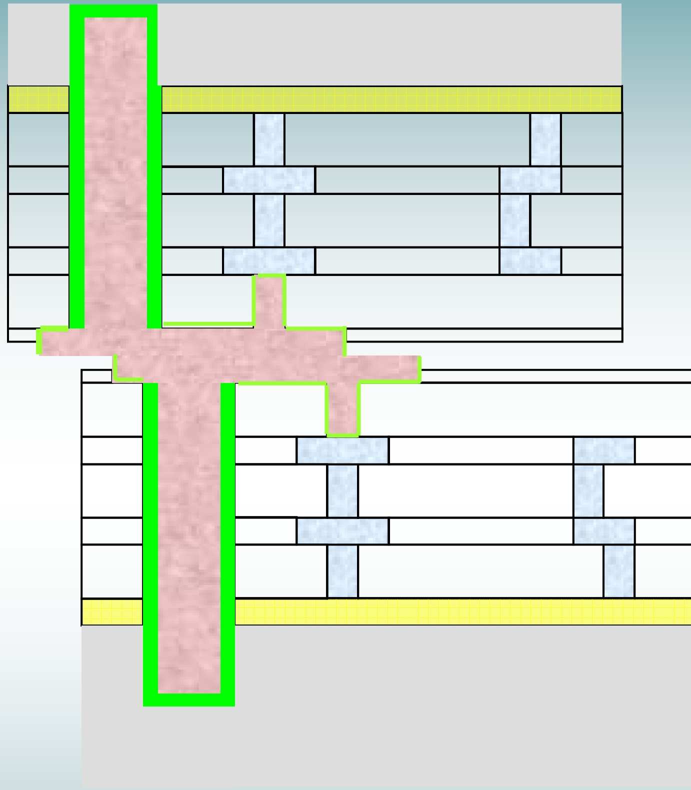
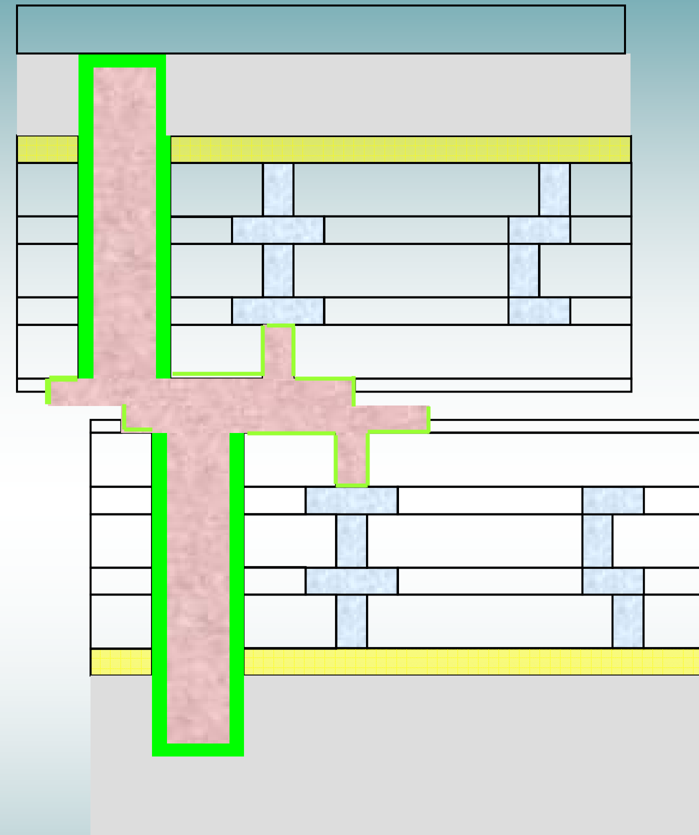
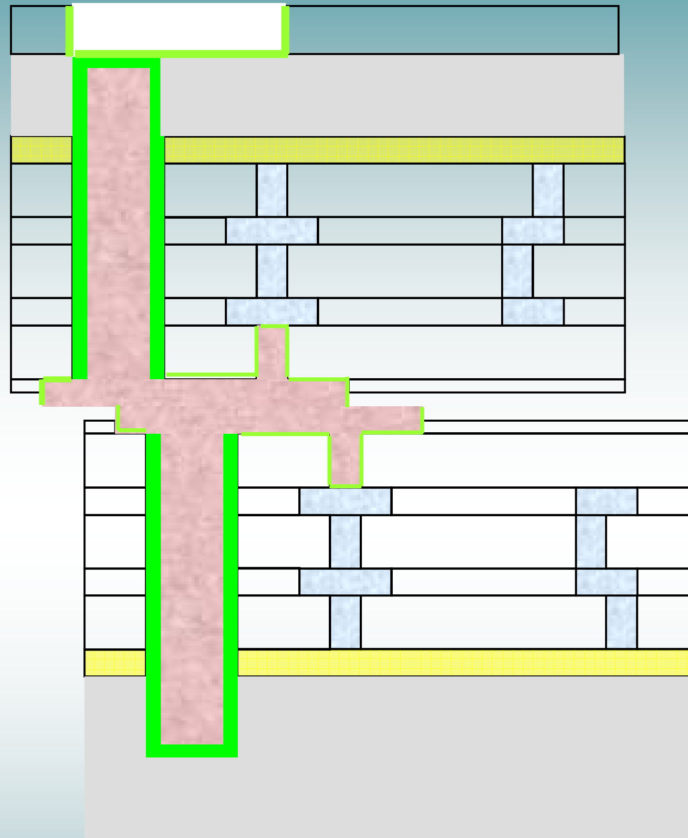


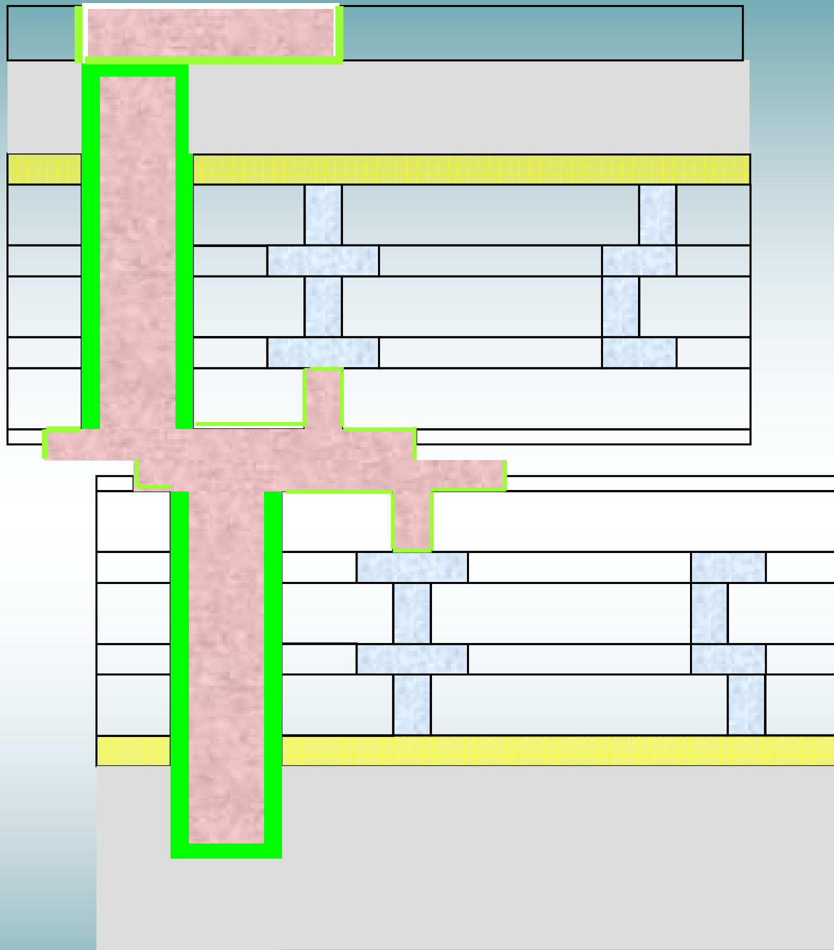
1. *Grind/Etch back silicon (bottom of the VIAS serve as stop layer*
2. *Thermal diffusion bonding*



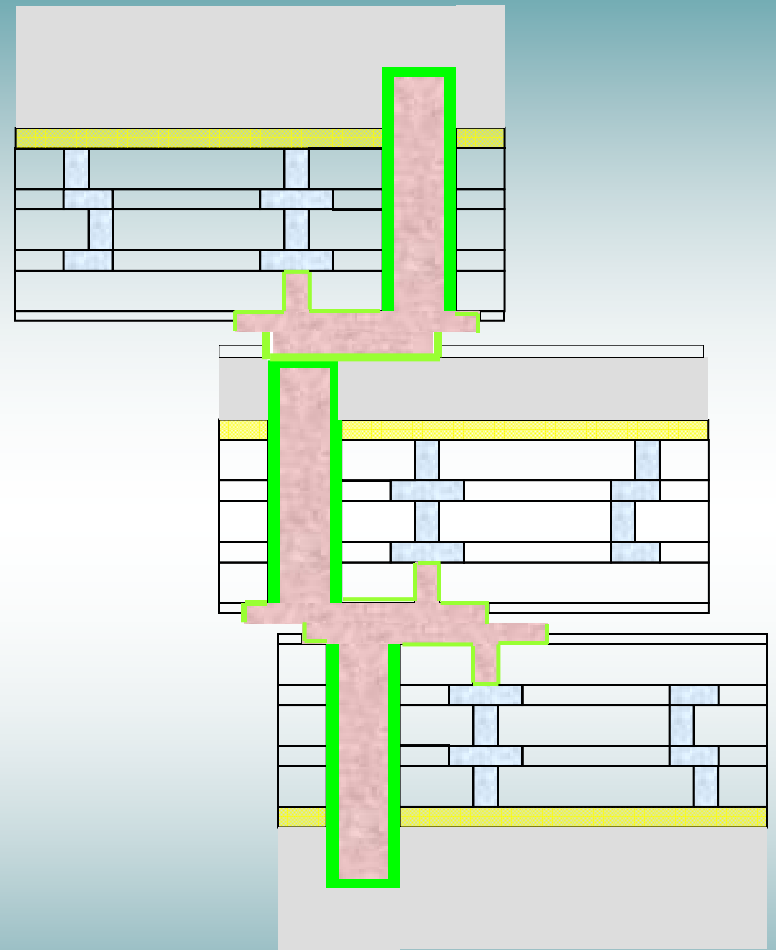
Insulator Oxide Deposition



1. *Print inverse metal (0) mask*
2. *Etch dielectric for the metal fill*



1. *Deposit Ta/TaN barrier and copper seed layers*
2. *ECP copper*
3. *CMP excess copper*



Recess dielectric or grow copper above the dielectric level and thermally bond the next wafer

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Tachyon Singapore Facilities/Equipment

Metrology Tool

Spin Rinse Dry Tool

Wafer-edge Sealer

Silicon Grinder

EVG Bonder

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Tachyon Singapore Facilities/Equipment

Site ready for
STS Etch Tool

Tachyon - IME Joint Development

TACHYON SEMICONDUCTOR

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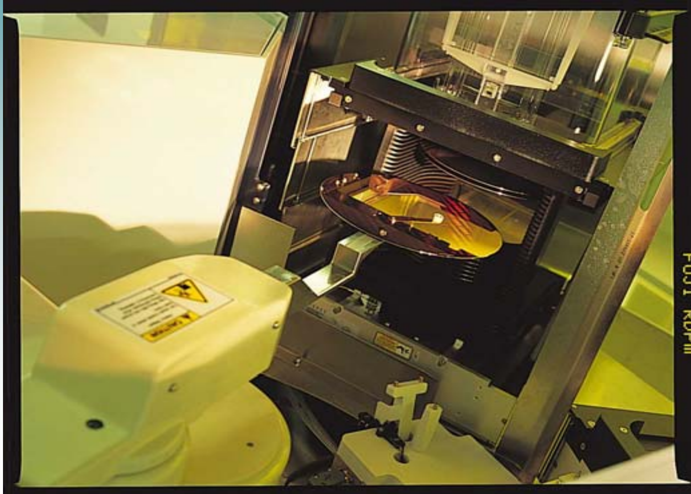


Electro Copper Plating

Chemical Mechanical Polishing

SEM Vision

Process Status

- 2 Mechanical test structures done
- Verified bond strength
  - 2Kg/sqmm
- Process range
  - Wide temperature range
  - Wide pressure range
  - Almost instant bonding
- Via defects <<10e-6
- Successful wafer thinning
- Alignment <1 micron

Process Continued

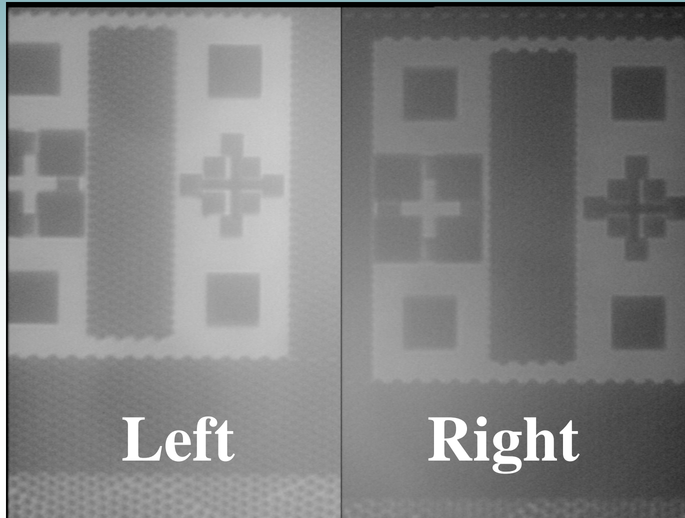
- Verified backside alignment
- New process allows .1 micron thinning control
- >10 micron via depth tested
- Trenched DRAM compatible

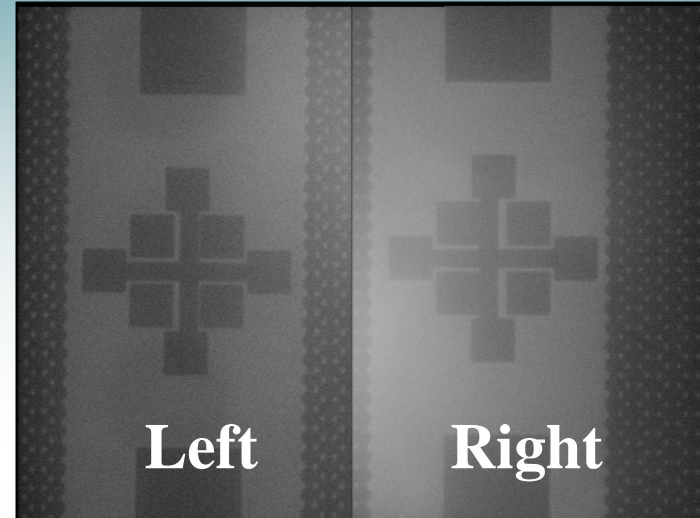
Wafer Align: Improvement with Modified Chuck

10X

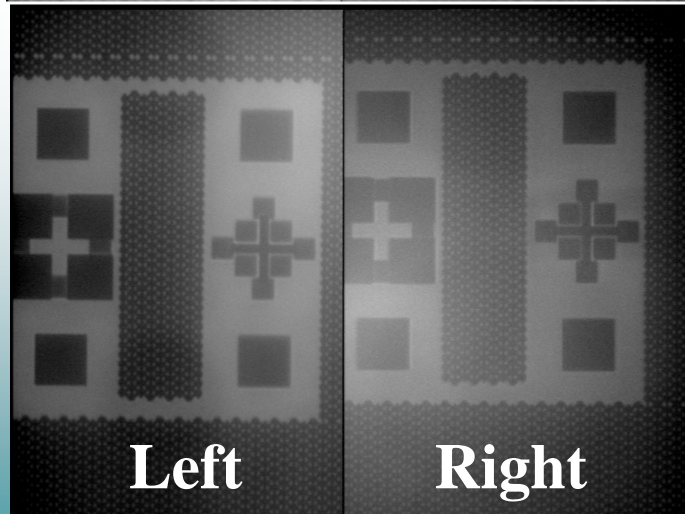
20X

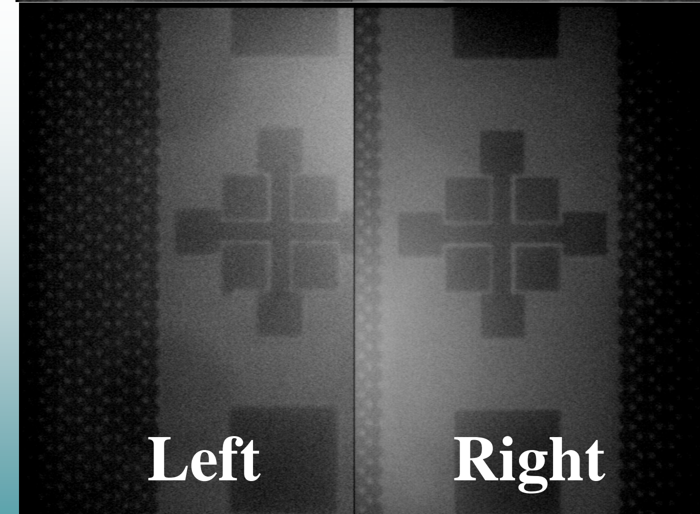
Old Chuck





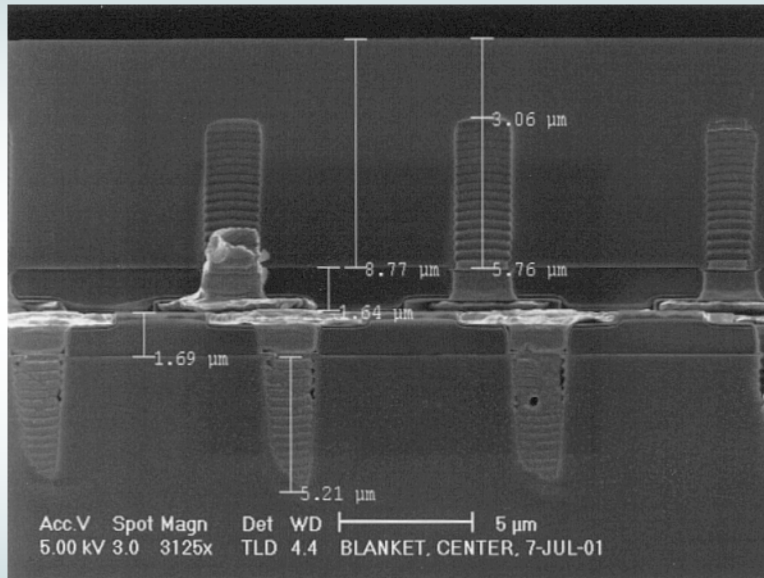
New Chuck



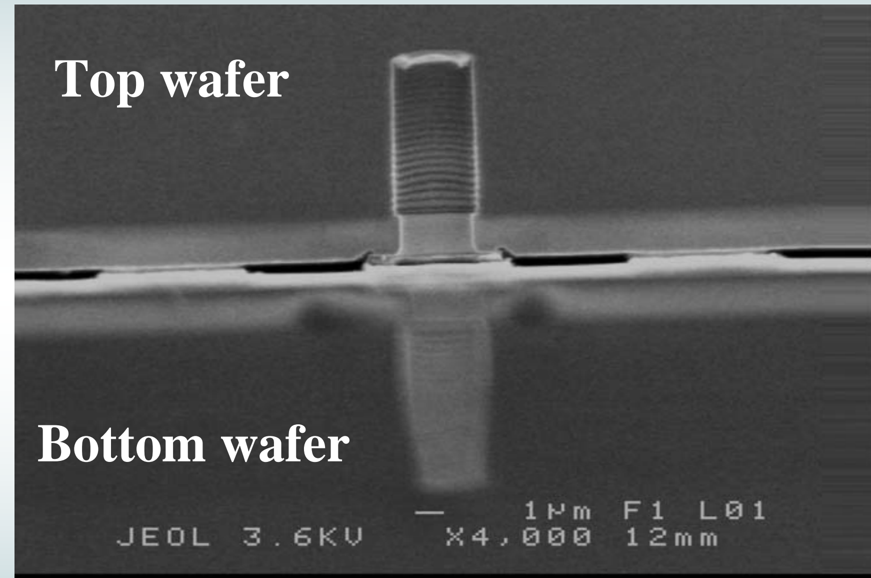


Wafer Align: Improvement with Modified Chuck

Old Chuck
Misalign=2.14um



New Chuck
Misalign=0.3um



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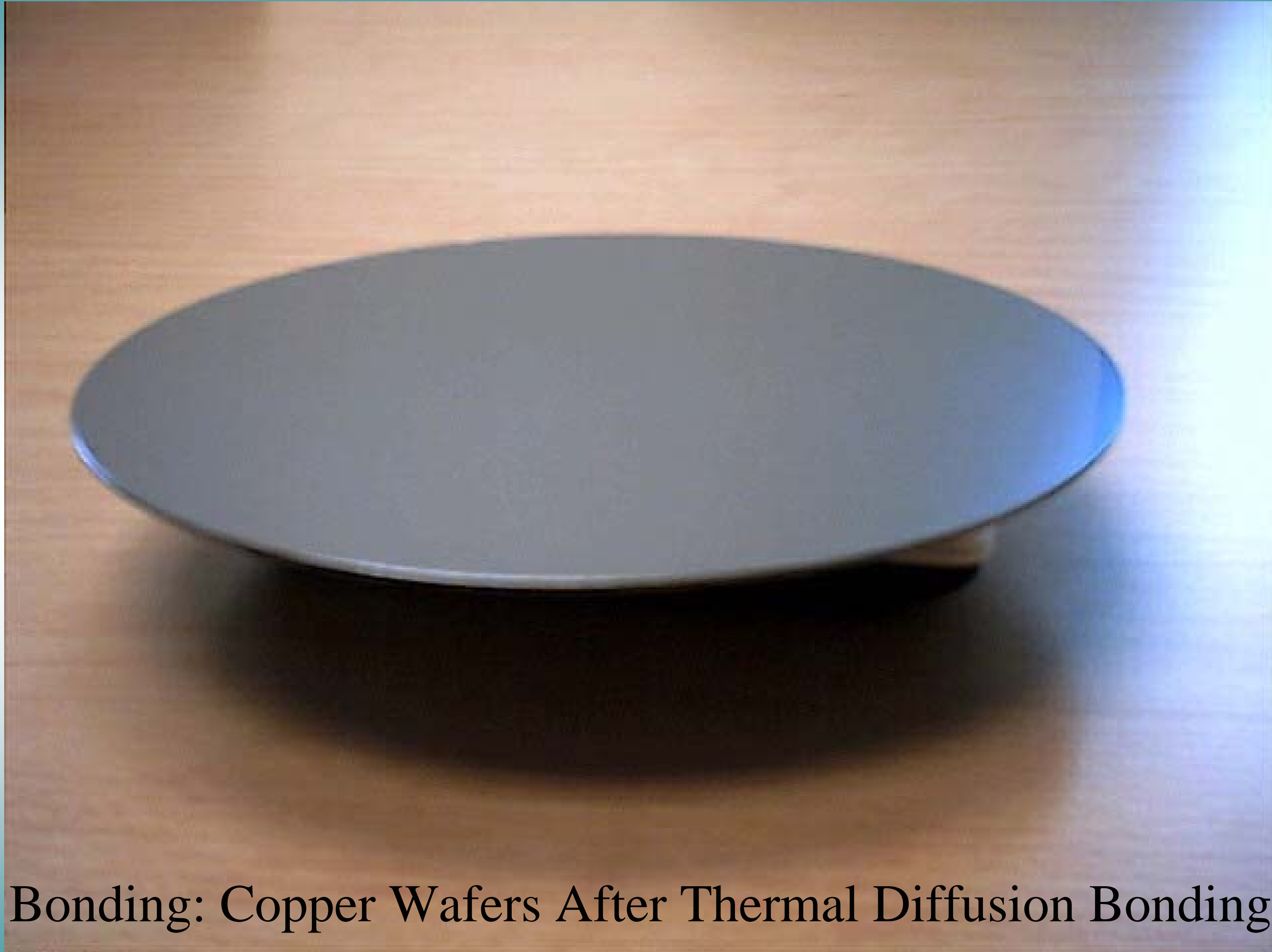
Stacking Process Update



Bonding: Copper Wafers After Thermal Diffusion Bonding

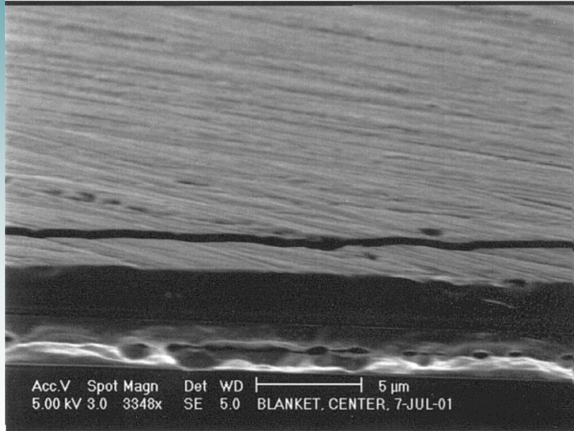
Stacking Process Update

Grinding: Bonded Copper Wafers after Grinding

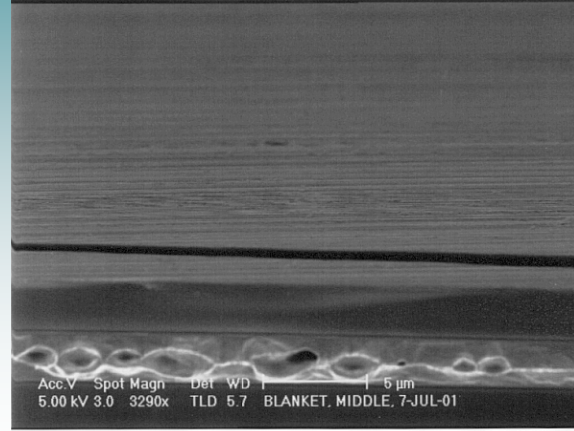
(20 µm Si remaining on the upper wafer)

Stacking Process Update

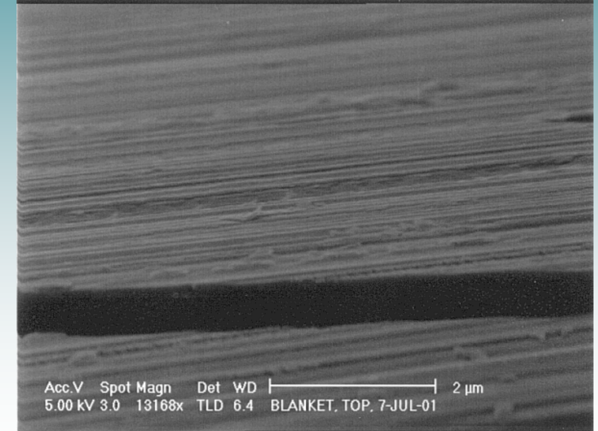
Grinding Striation at Center

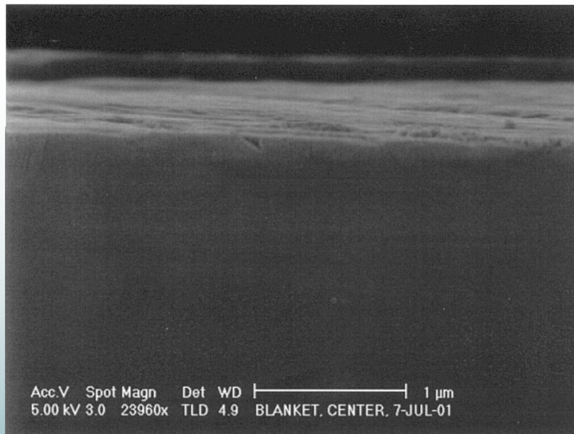


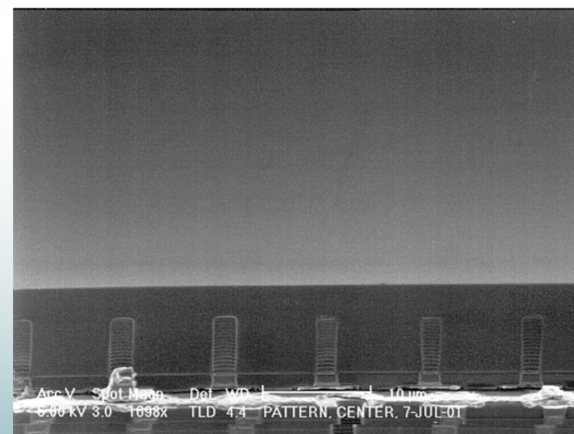
Grinding Striation at Middle



Grinding Striation at Top







Grinding striation vanishes after CMP on pattern wafer

Striation caused by grinding disappears after CMP, depth of striation not more than 0.10 µm

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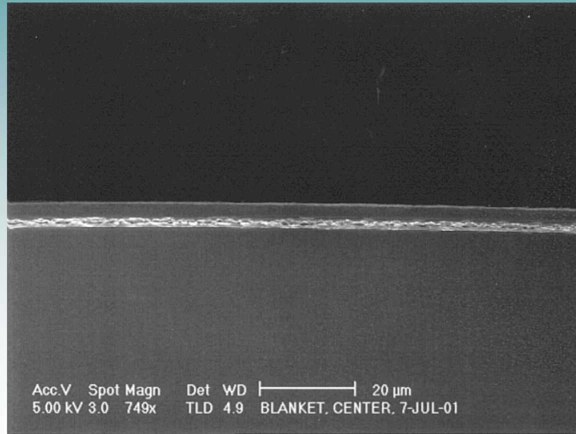
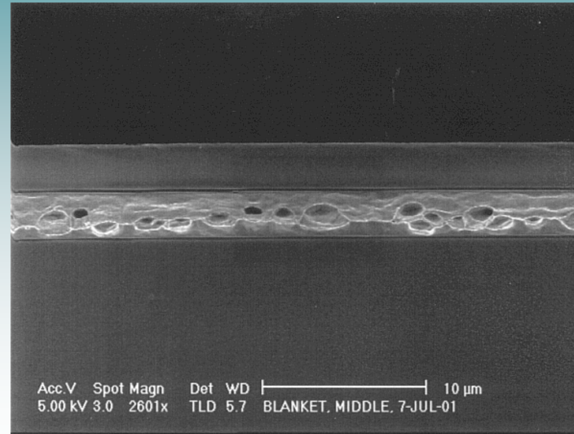
Stacking Process Update

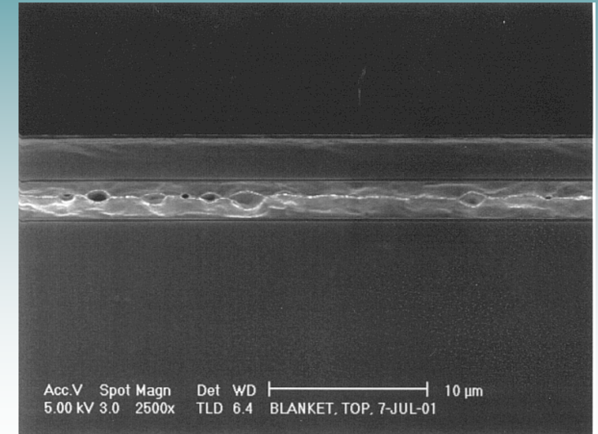
Center: Si remain = 2.70 µm

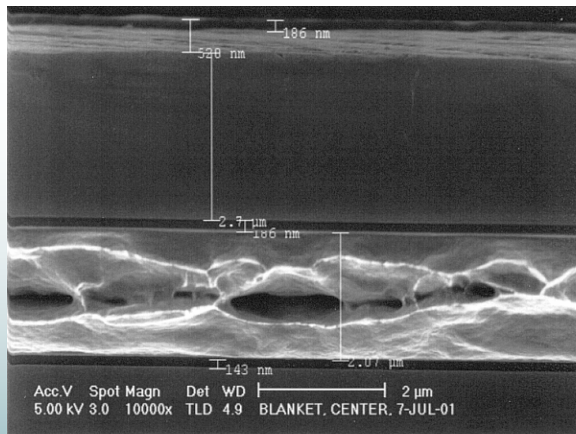


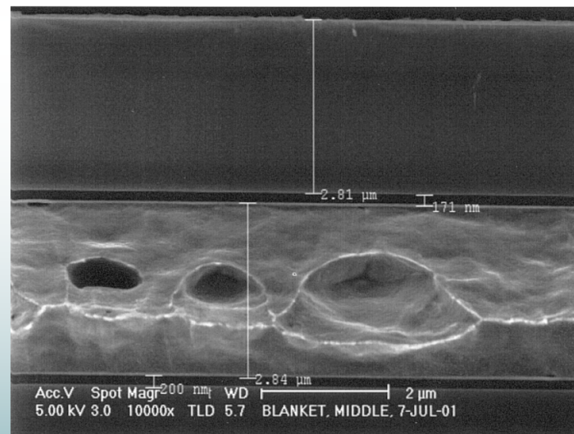
Middle: Si remain = 2.81 µm

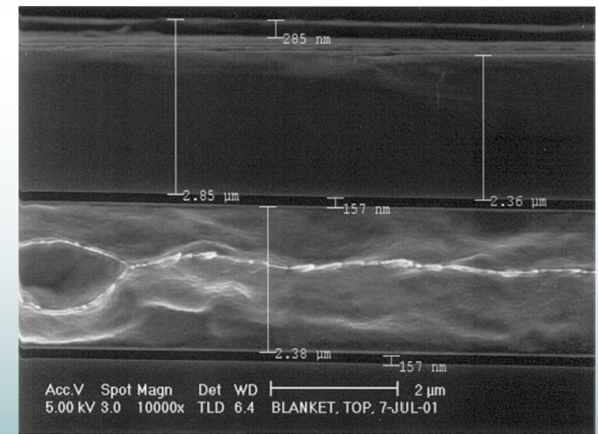


Top: Si remain = 2.36 µm









Blanket Cu ECP wafer stacking and grinding results:
Removal non-uniformity < 0.1 %, final Si remain within 0.5 µm

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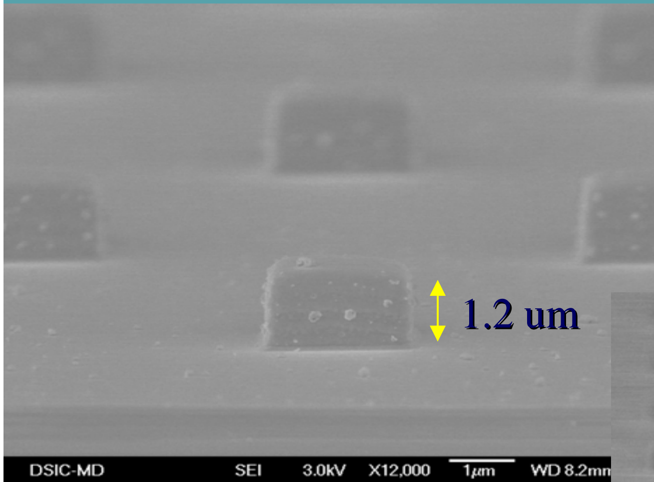
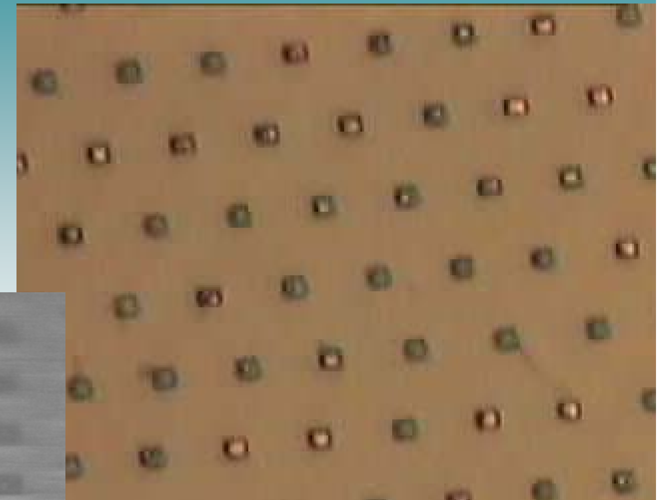
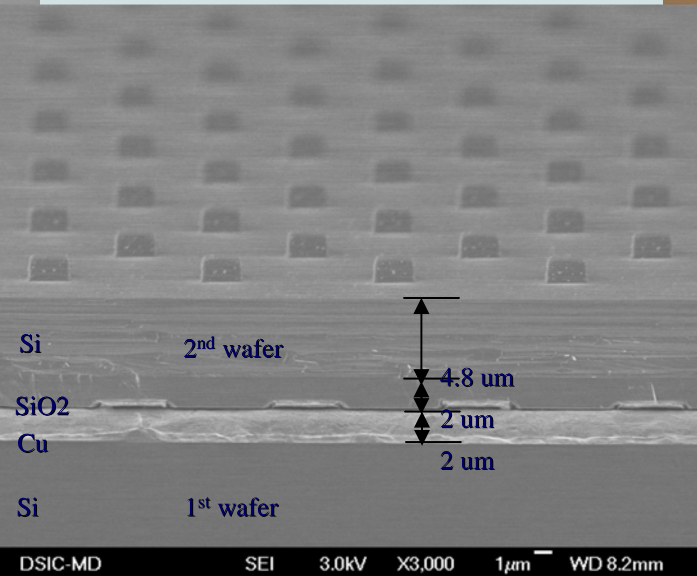
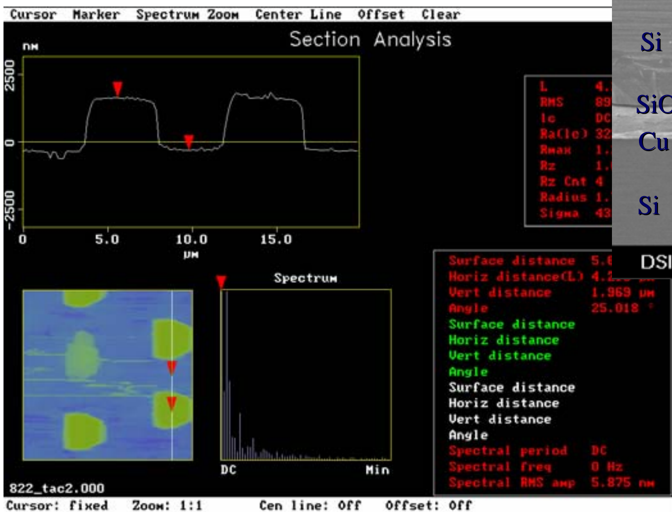
Stacking Process Update







Microscope View



Profiler View

Wet Etch: 1.2 μm Copper Via protruding

TACHYON SEMICONDUCTOR

Stacking Process Update

3rd Wafer Blanket Cu

Super Via

2nd Wafer pattern Cu

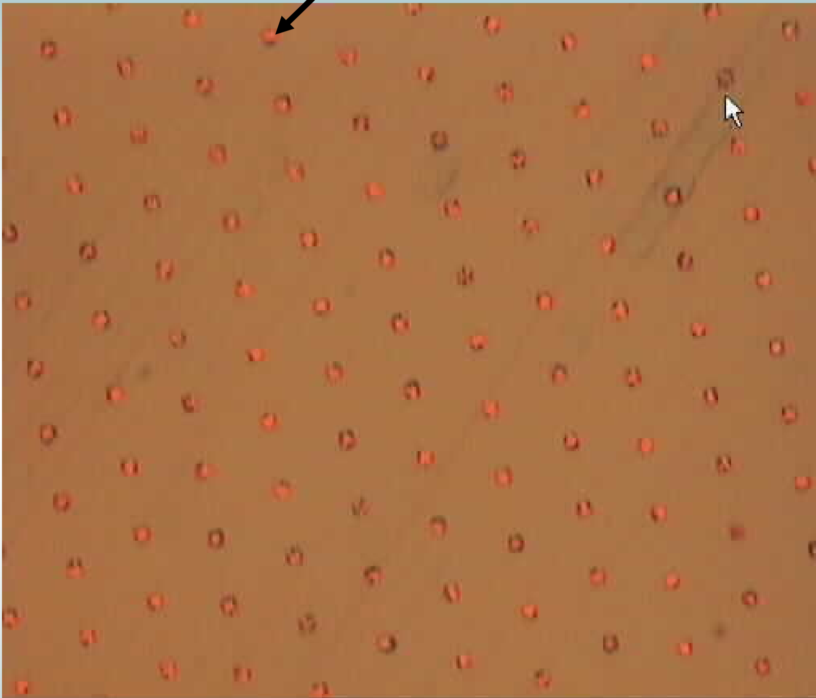
Top Metal Pad

1st Wafer Blanket Cu

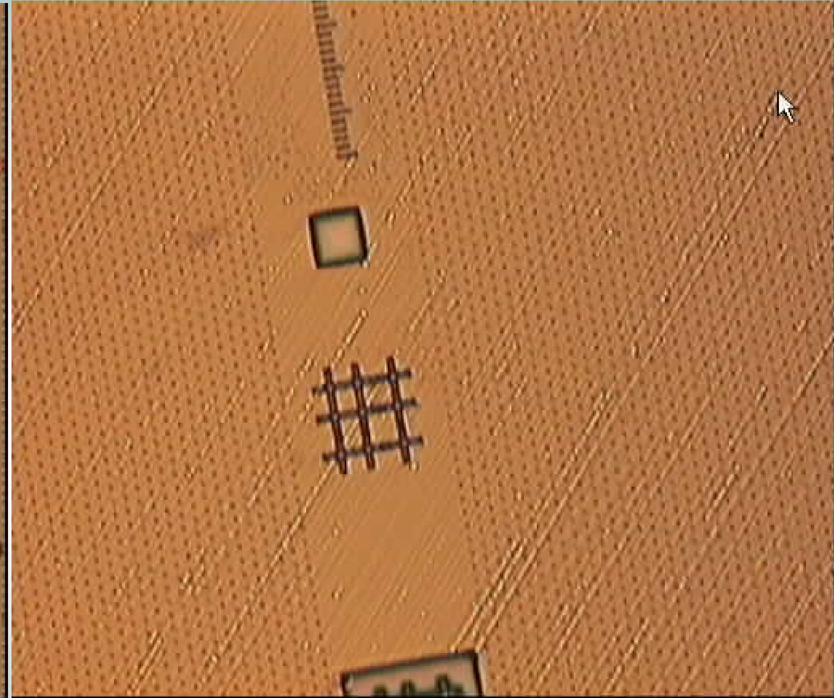
Three Cu Wafer Stacking

Alignment Mark Images

Just Etch : Copper stud is clearly revealed



High Mag



Low Mag

TACHYON SEMICONDUCTOR