"Optimization of Electrical Package Design and PCB Design for CSP Age"

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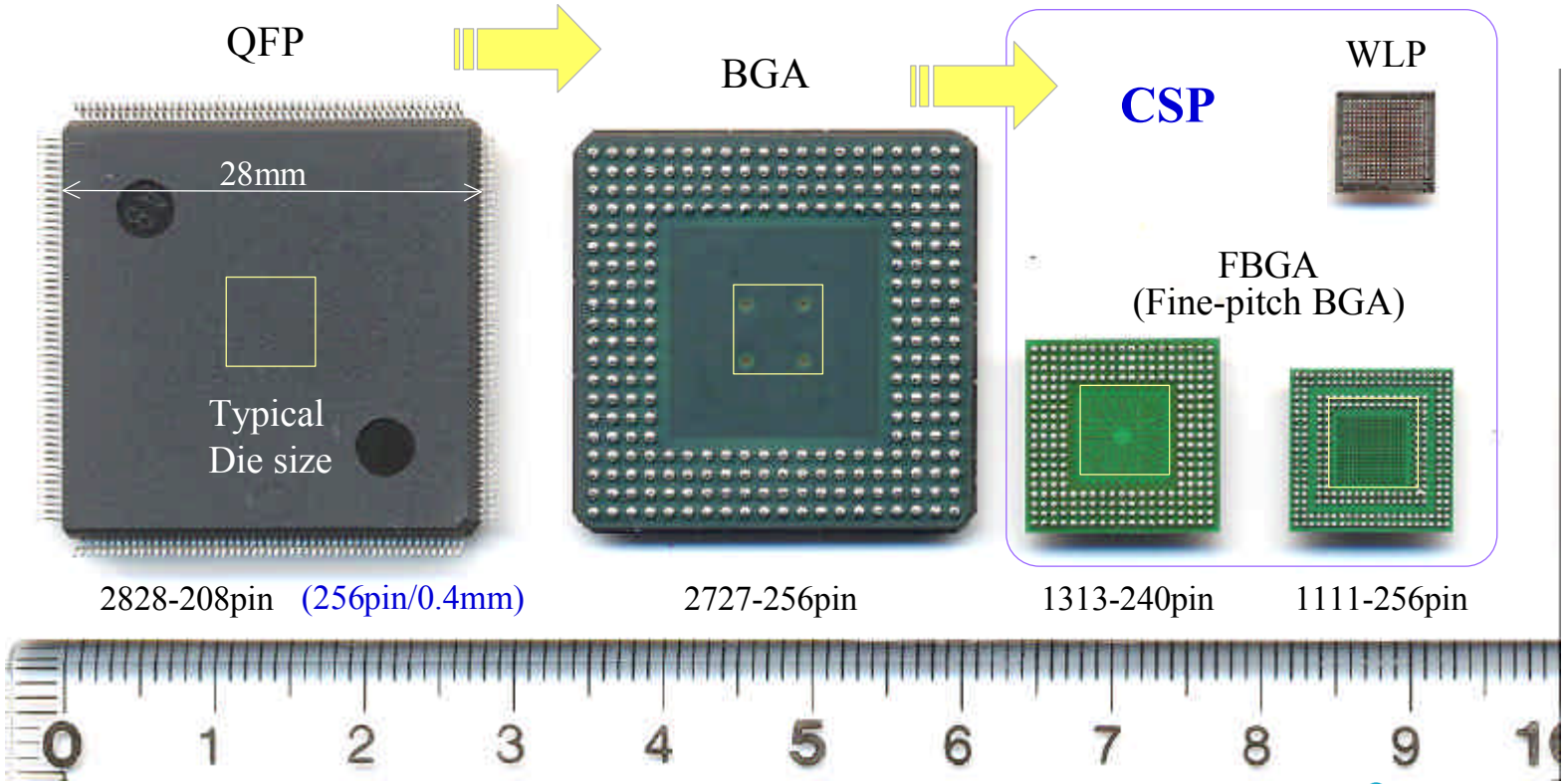
Package Miniaturization (QFP > BGA > CSP)

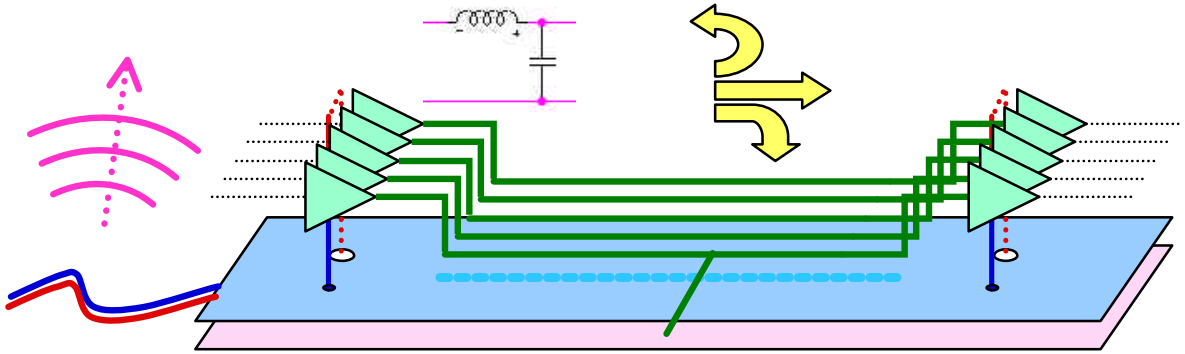
MPU for consumer products has been shaping up his body smaller and smaller

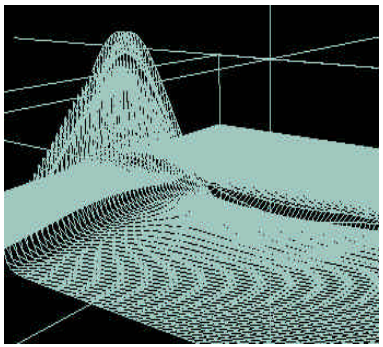


Bottleneck for High speed operation : *Interconnect Design*

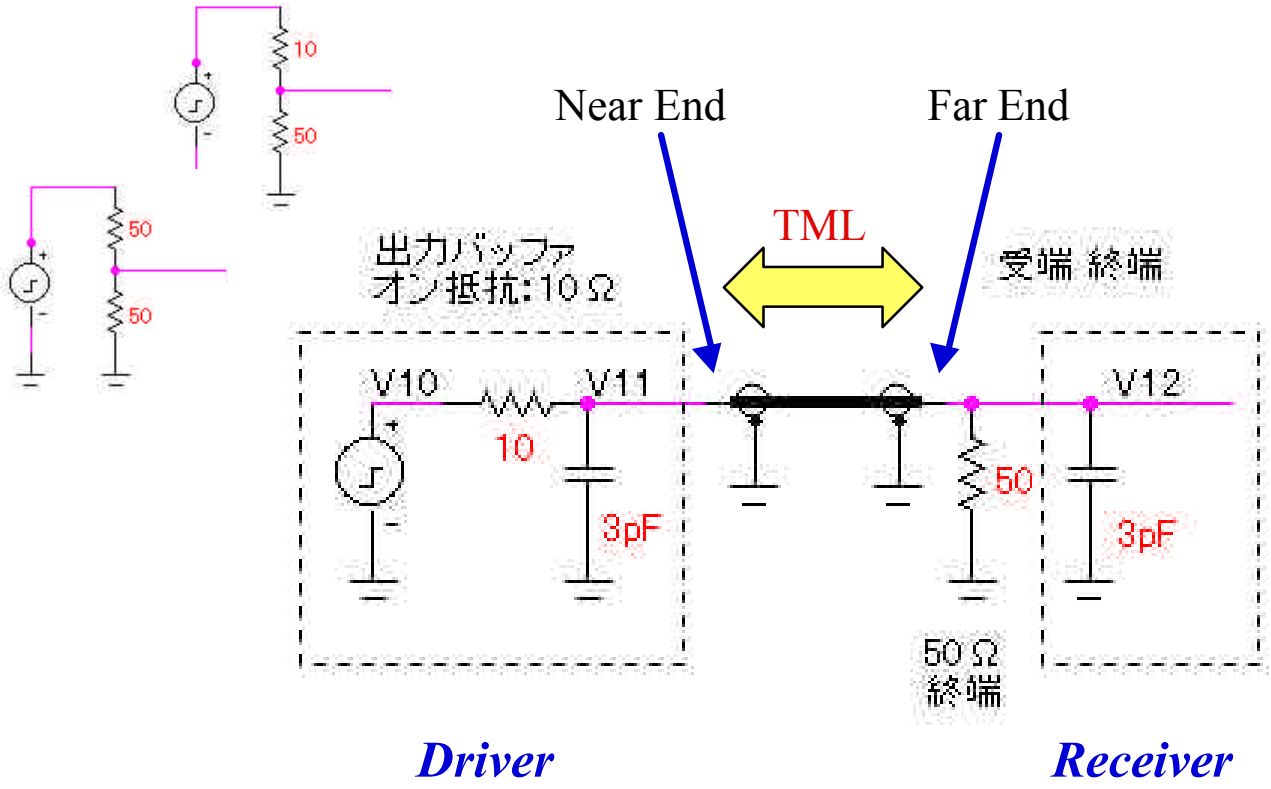
Higher Freq. Operation

- **SI (Signal Integrity)** — **Signal** [Reflection, Crosstalk, …..]
- **PI (Power Integrity)** — **Supply** [SSN]
- **EMI (Electromagnetic Interference)** — **Supply** [Emission]

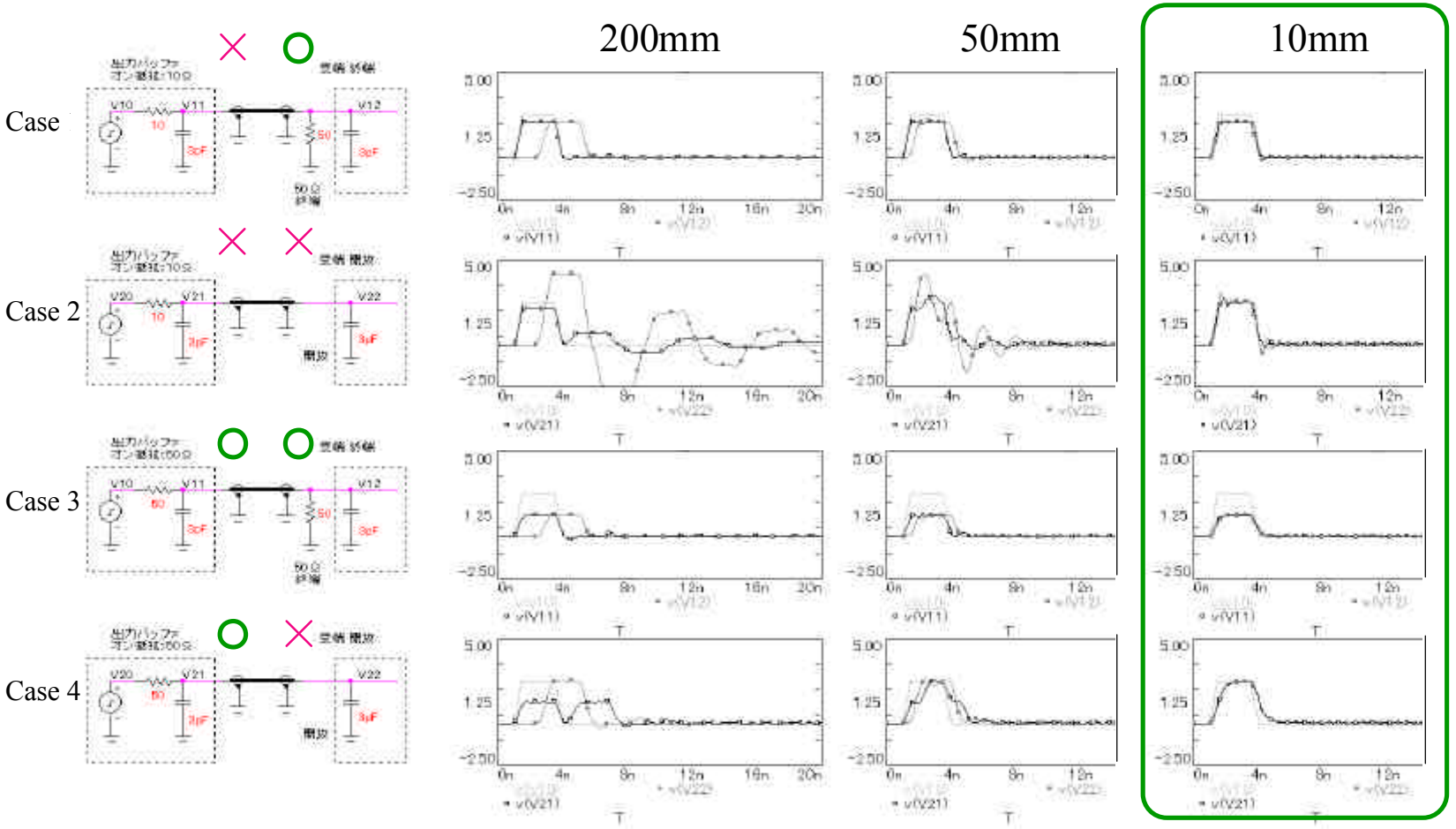




Impedance matching at Driver/TML and TML/Receiver

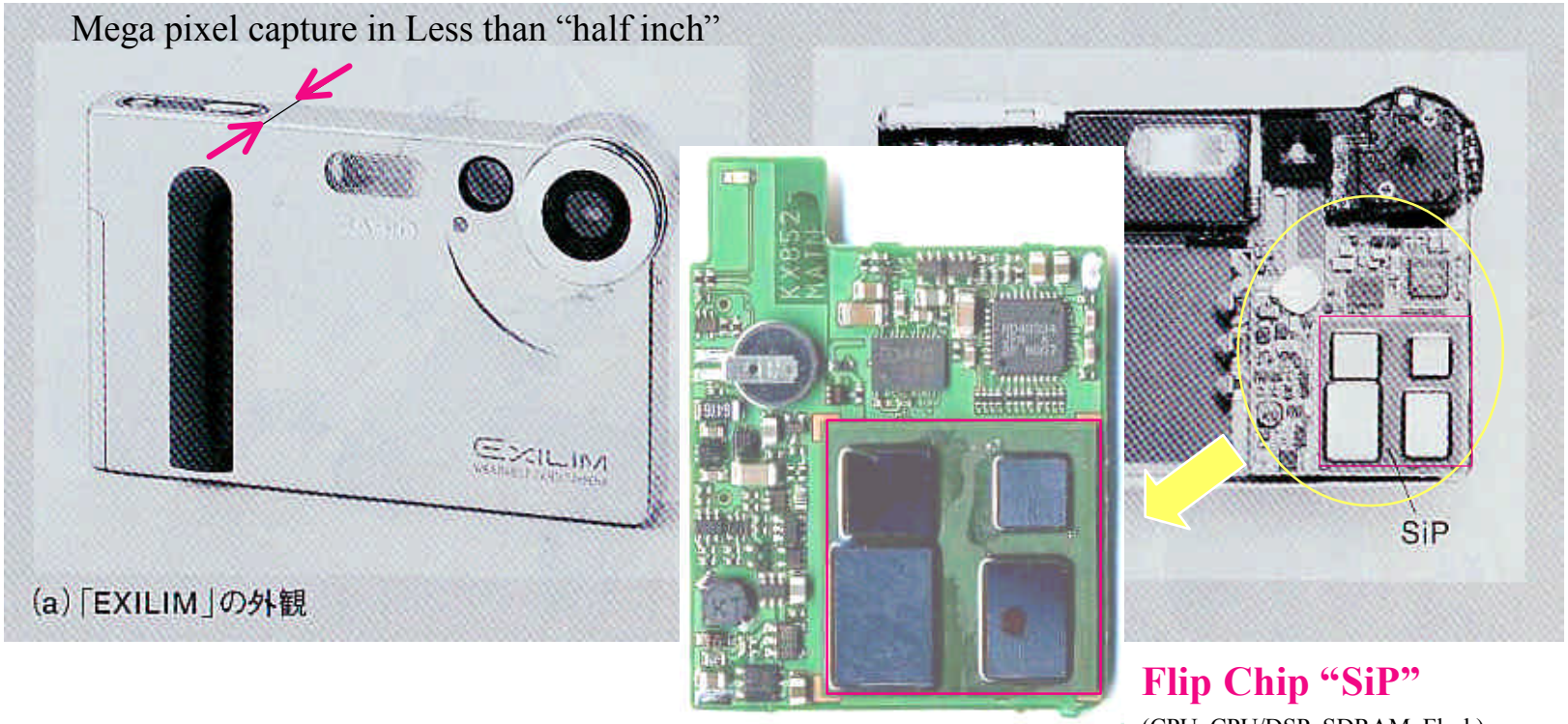


Waveform comparison on Termination, TML length



Miniaturization in Digital Consumer Products

Mega pixel capture in Less than “half inch”



Flip Chip “SiP”

(CPU, CPU/DSP, SDRAM, Flash)

“SiP vs SoC”, NIKKEI MICRODEVICES magazine, p65, No.208, Oct. 2002

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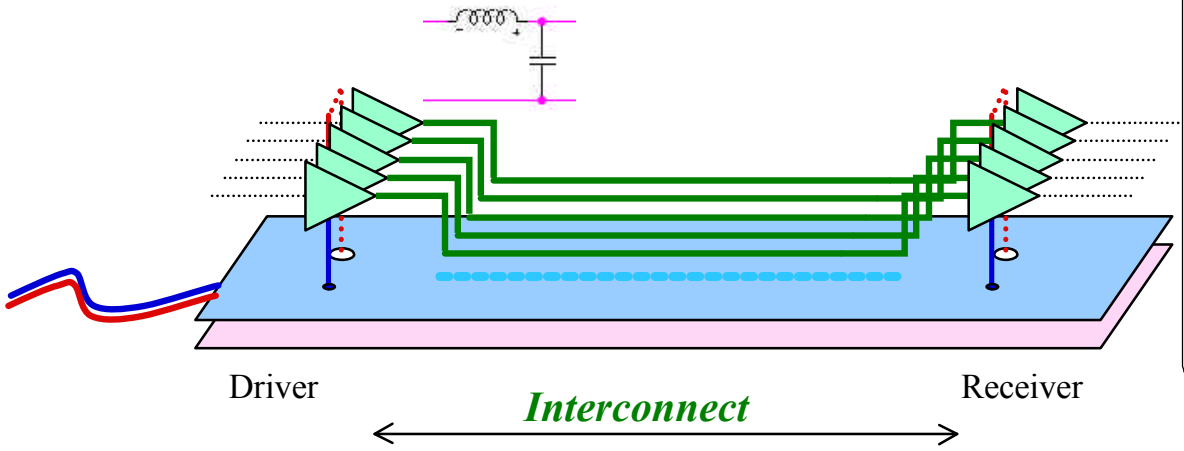
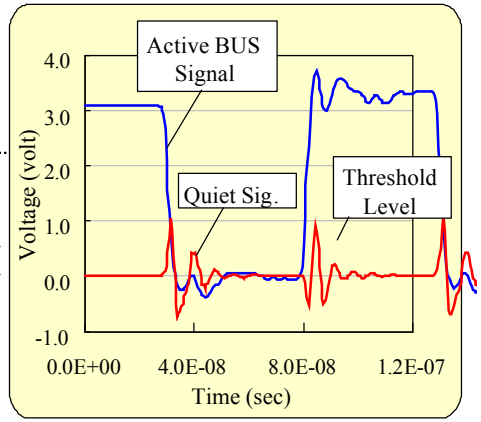
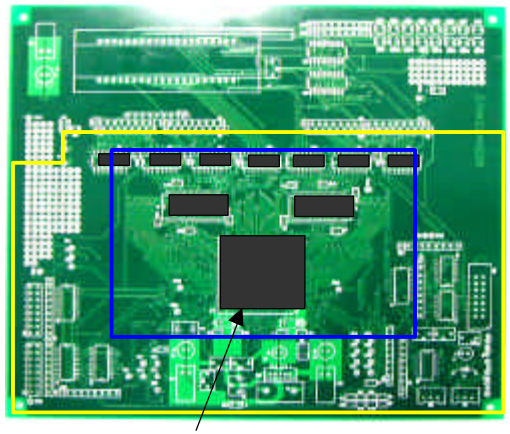




PCB Modeling for Power Integrity Analysis

LSI Package, BUS traces and V/G plane conductors in PCB should be analyzed in a single model for field solver.

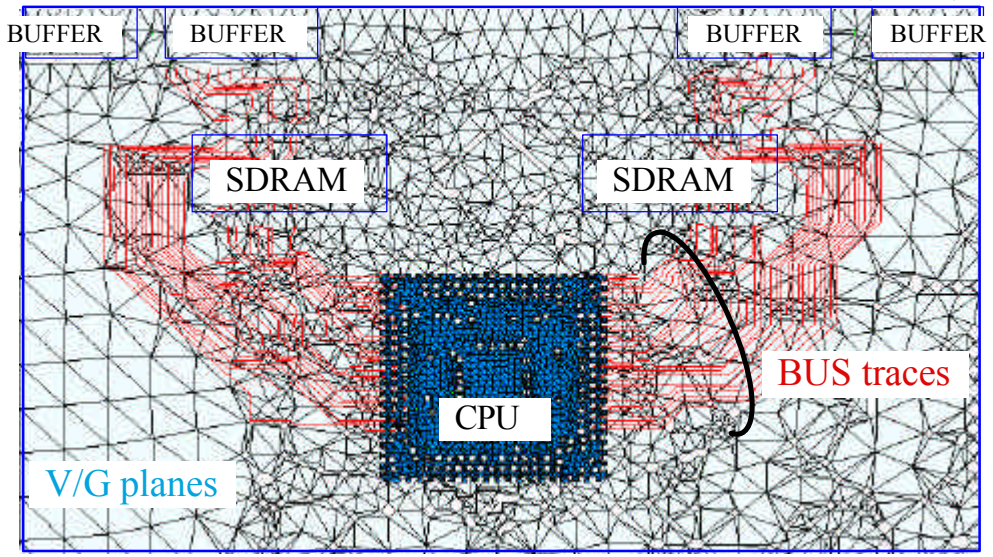
Analysis Vehicle



BGA package

PCB :	4 Layers
PKG (BGA):	2 Layers
Total	6 Layers

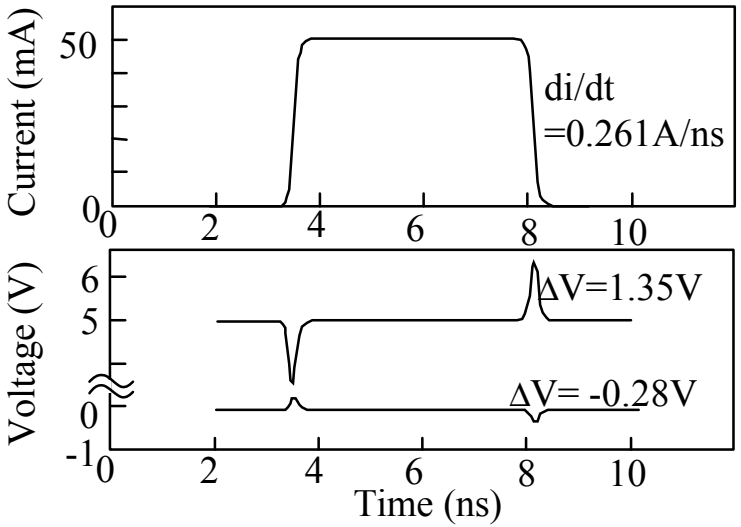
Evaluation board for SH4(BGA)

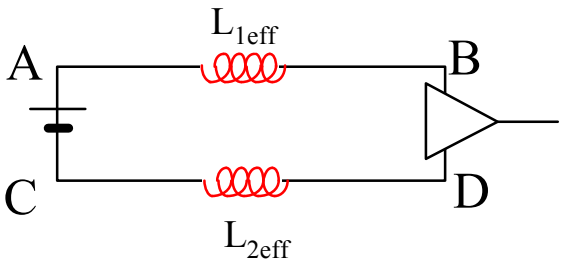


Analysis model (Traces, planes, and PKG)

"M" between trace and GND plane

(1) Estimation from measured waveform

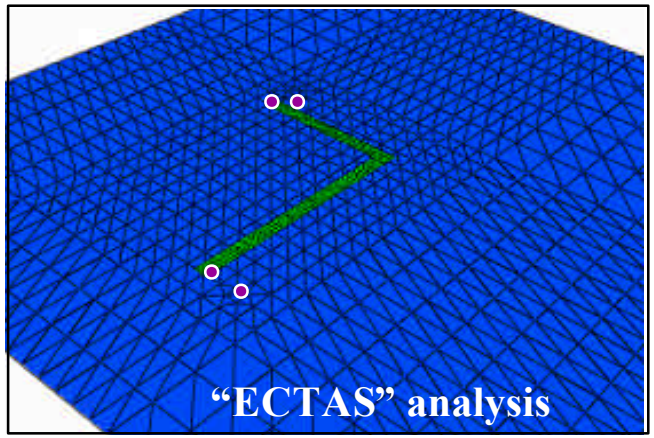


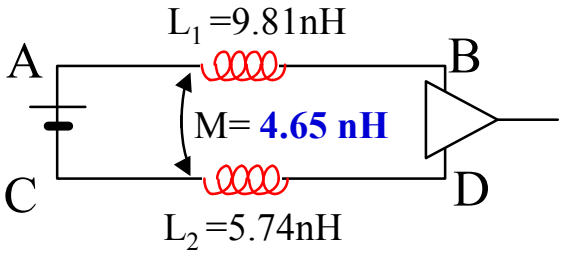


L_{1eff}=1.35/0.261= **5.17** nH

L_{2eff}=0.28/0.261= **1.07** nH

(2) EM analysis

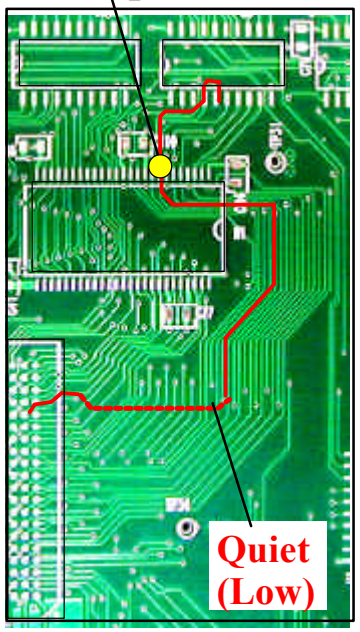




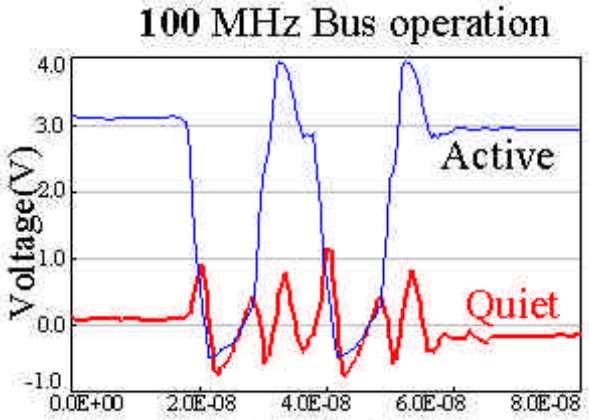
L_{1eff}= L_1 - M = **5.16** nH

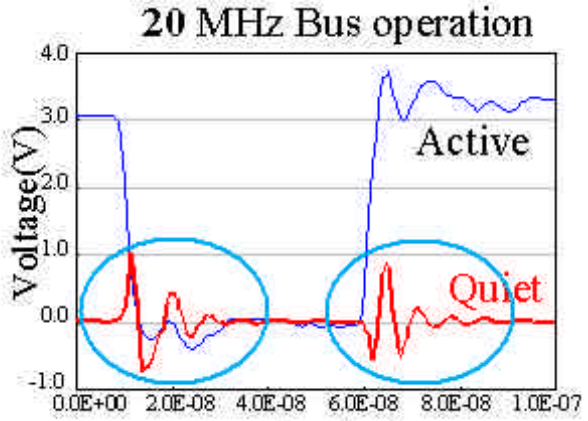
L_{2eff}= L_2 - M = **1.09** nH

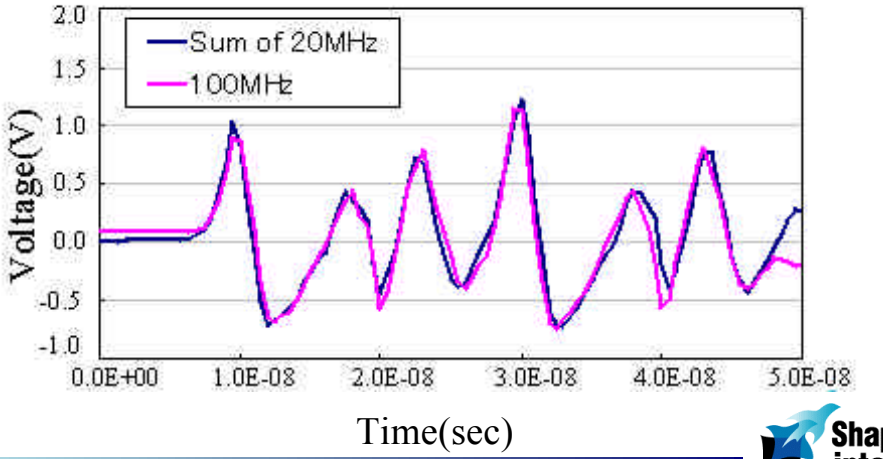
SSN waveform extraction at low frequency operation



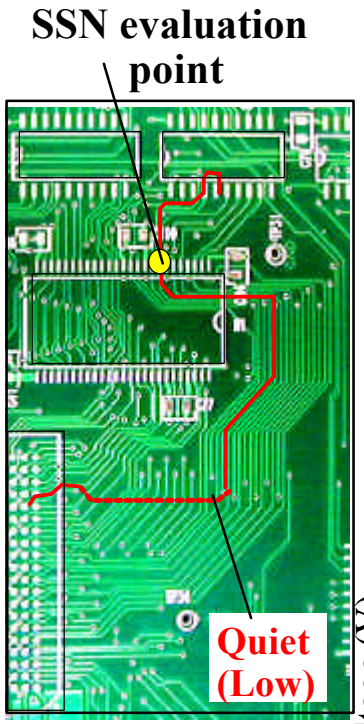
Switching 63 I/O traces simultaneously







Comparison between measured and simulated waveform



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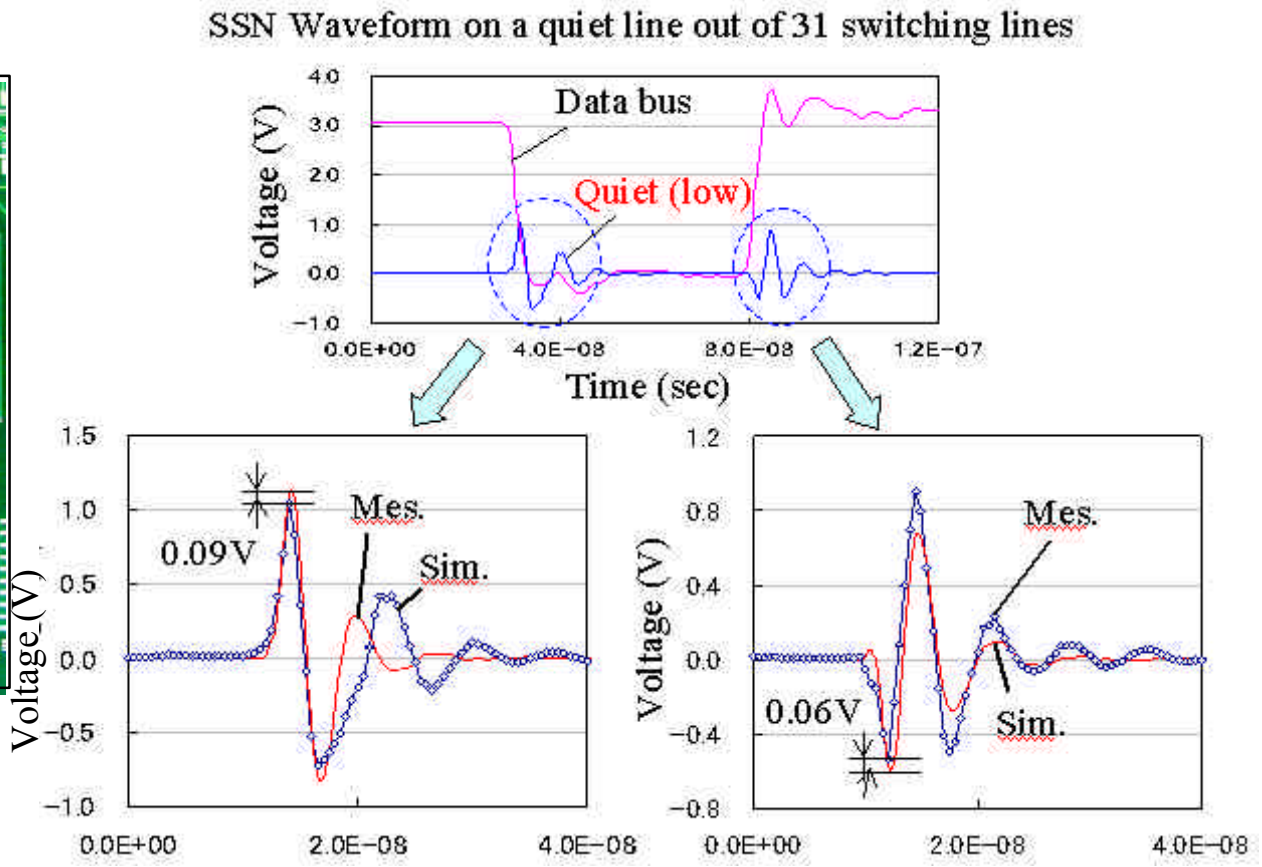
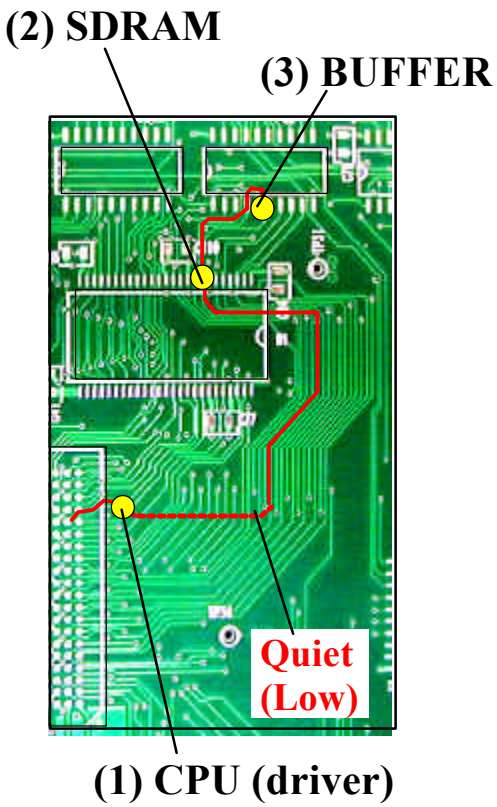
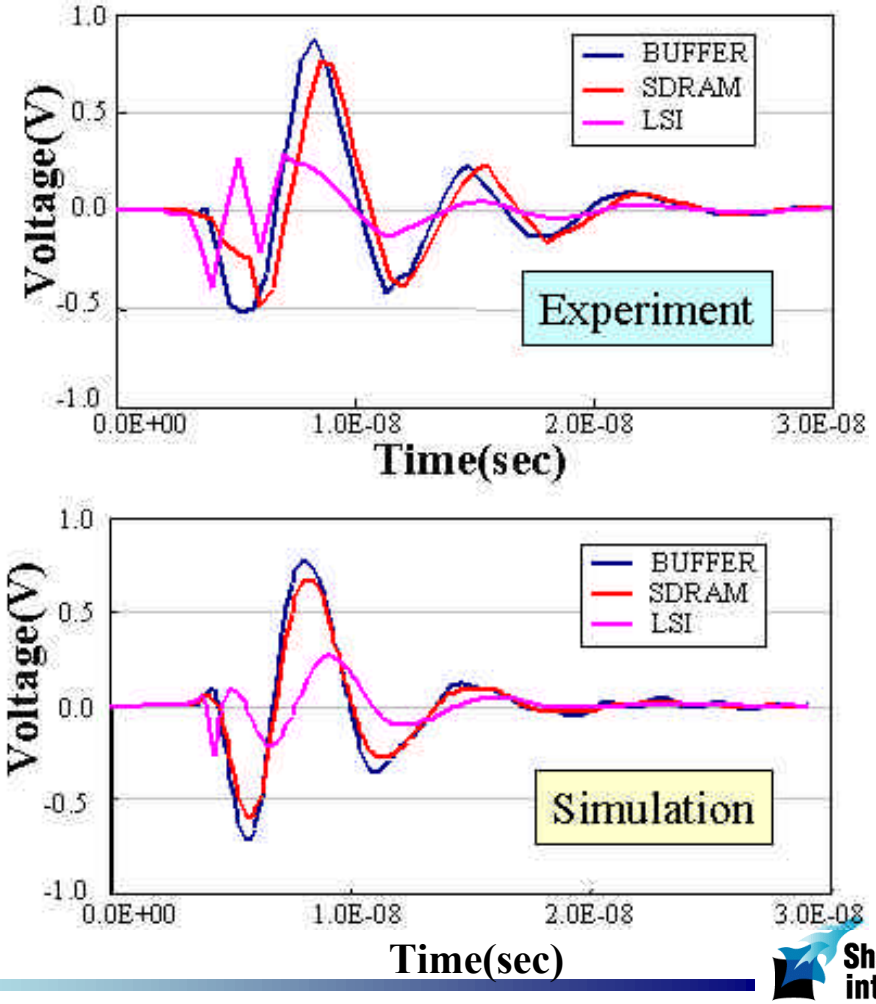
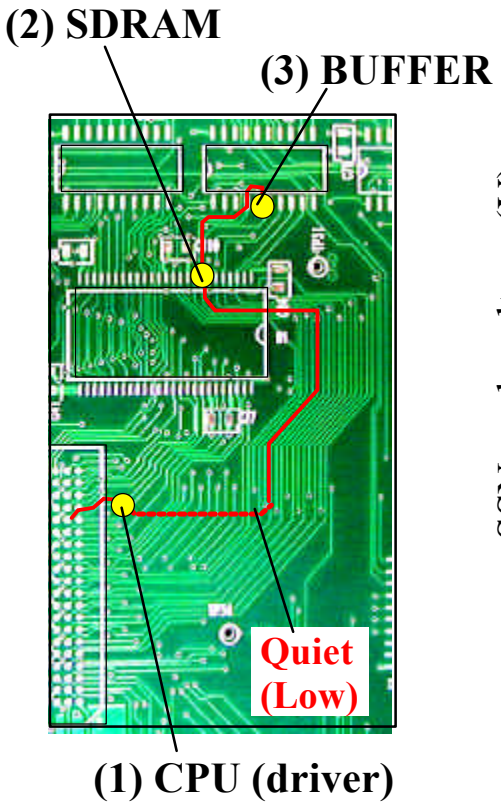


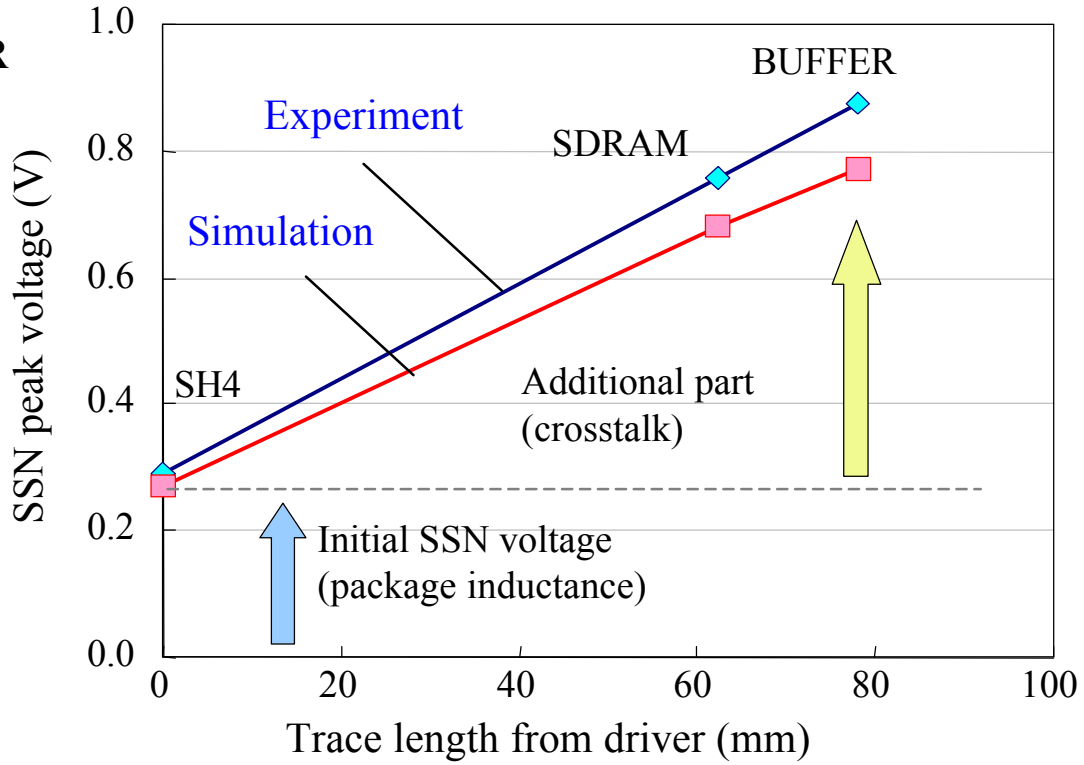
SSN waveform difference obtained at different point on the quiet trace





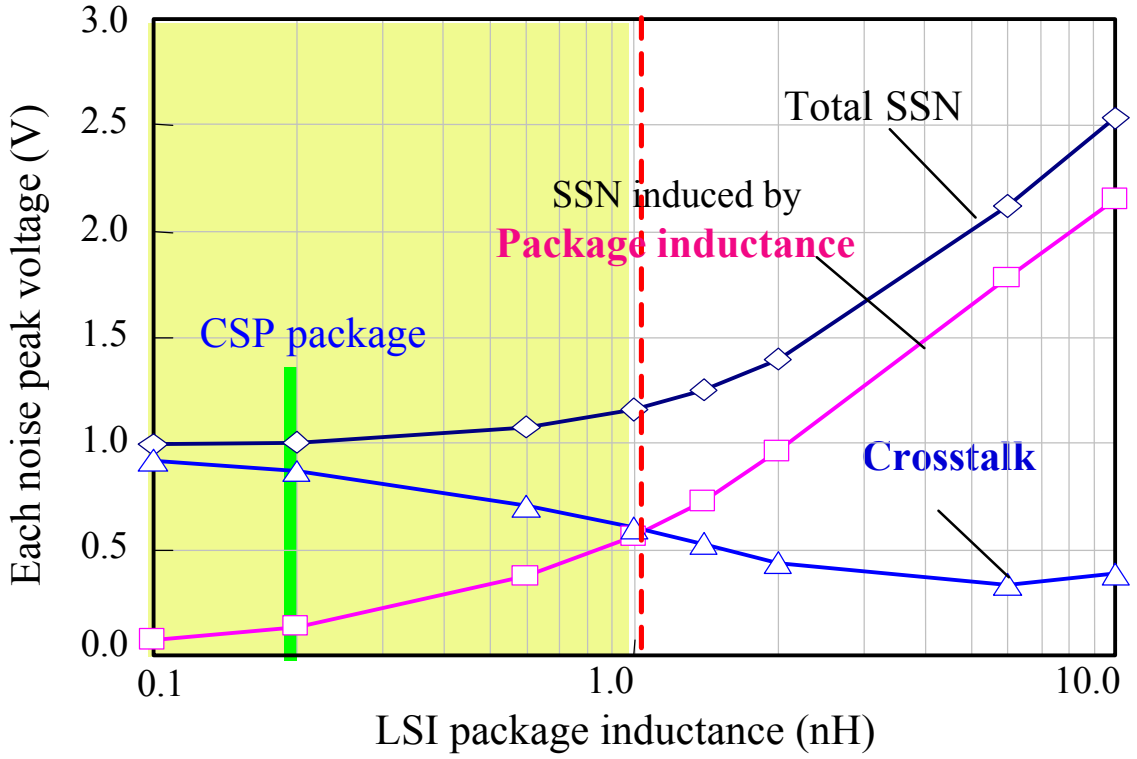
Peak voltage increase proportional to trace length





Package dominant and PCB dominant region

Cross talk part is dominant on BUS system using low inductance packages (Less than 1nH)



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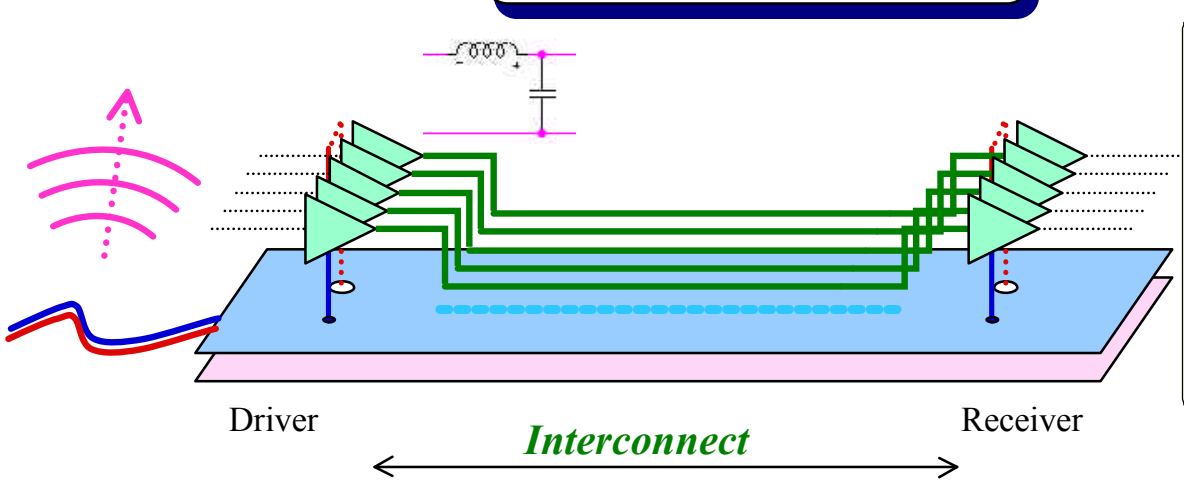
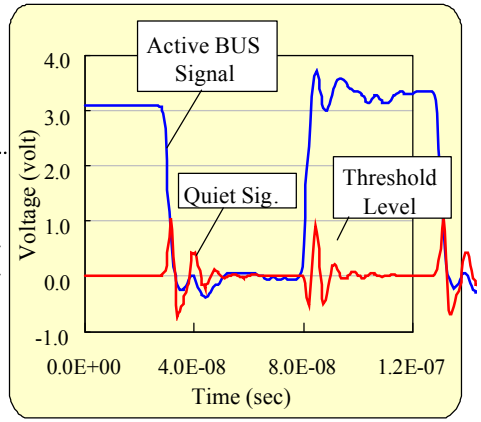
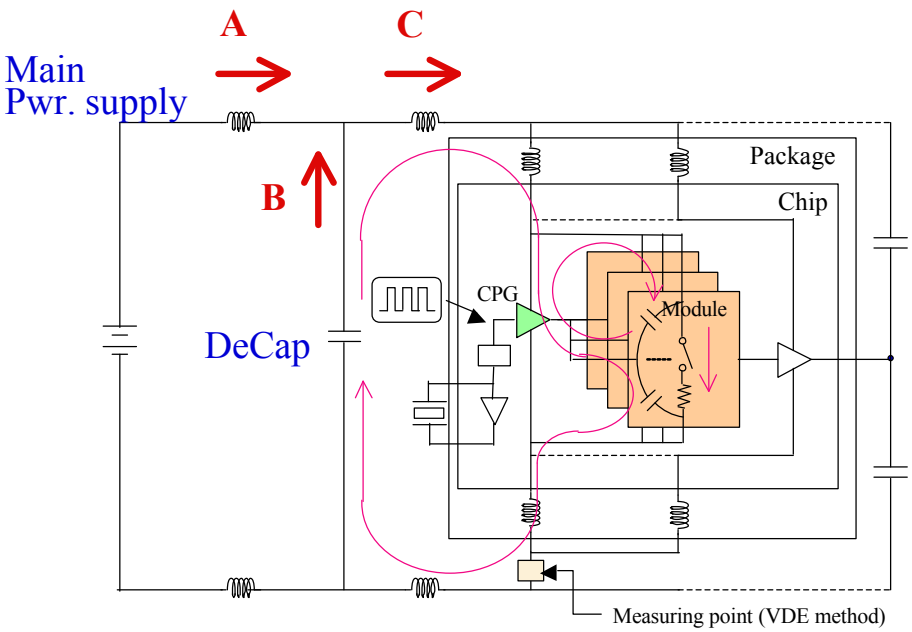
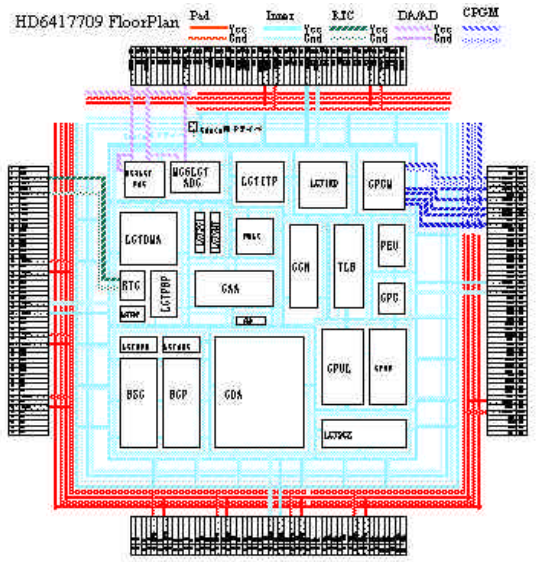




Low noise assembly Basics

- Minimize voltage fluctuation around CPU by Supply decoupling
- Increase current supply from DeCap (B) and decrease current from main Power supply (A)
- Current ratio A/C represents effectiveness of DeCaps

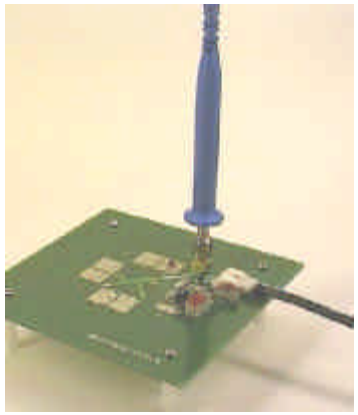




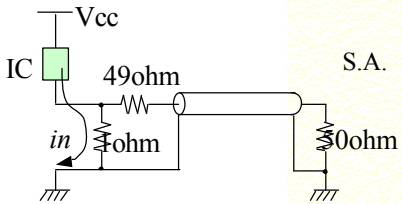
Example of multiple Vcc/Vss micro

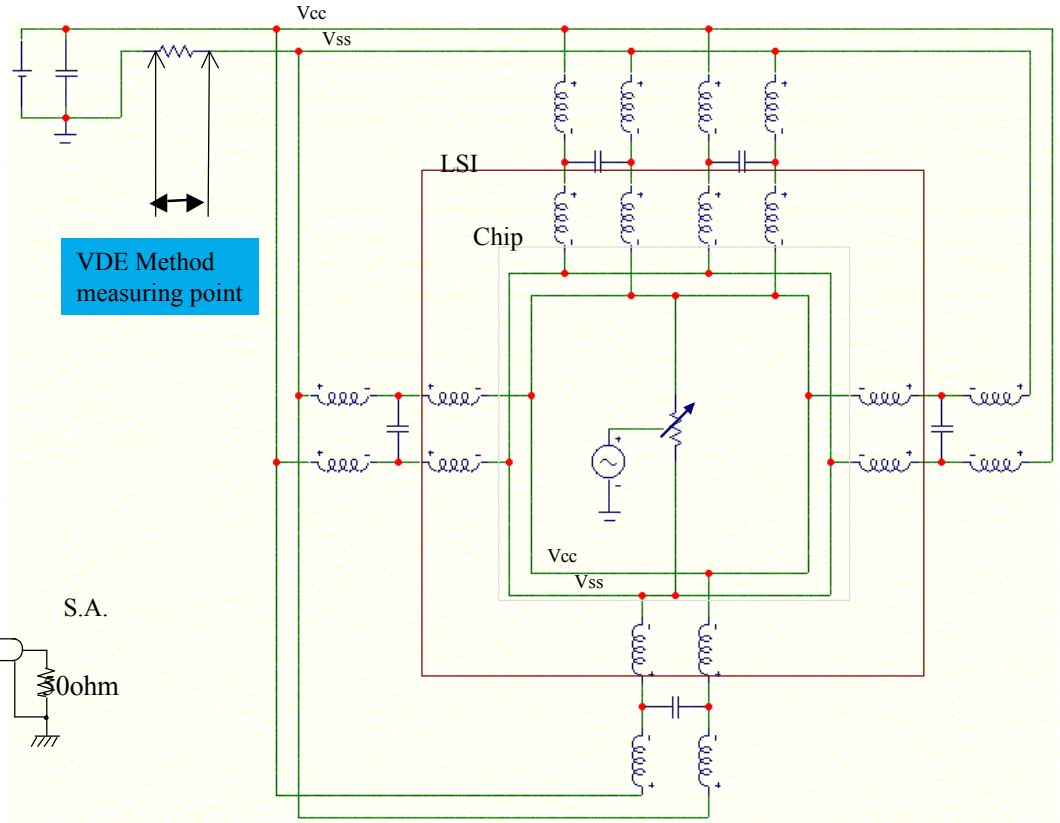
Noise current measurement

- Noise current can be measured by 1 ohm (VDE) probe
- Decoupling effect of Caps can be evaluated by w/ and w/o comparison



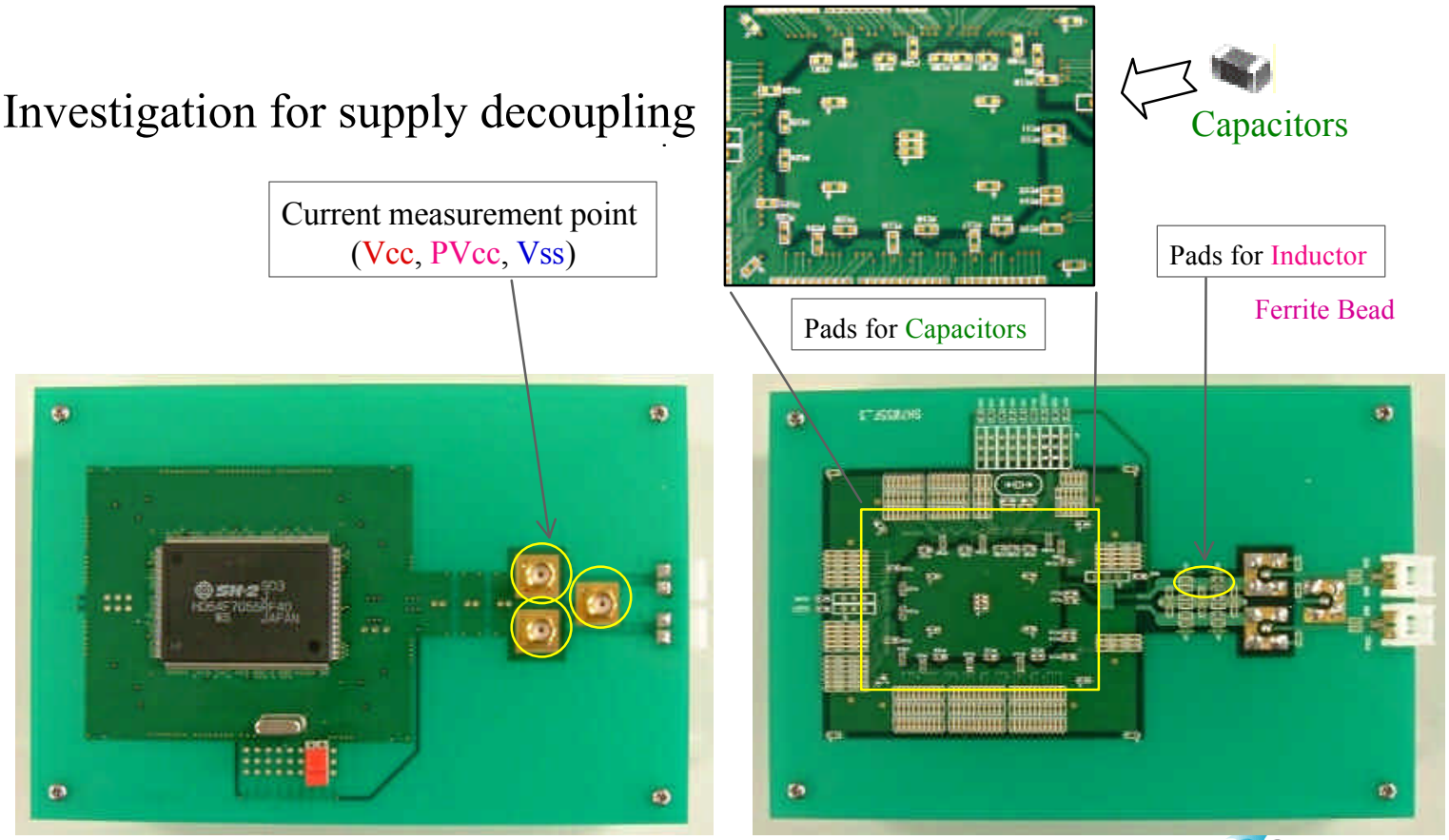
(1) VDE Method



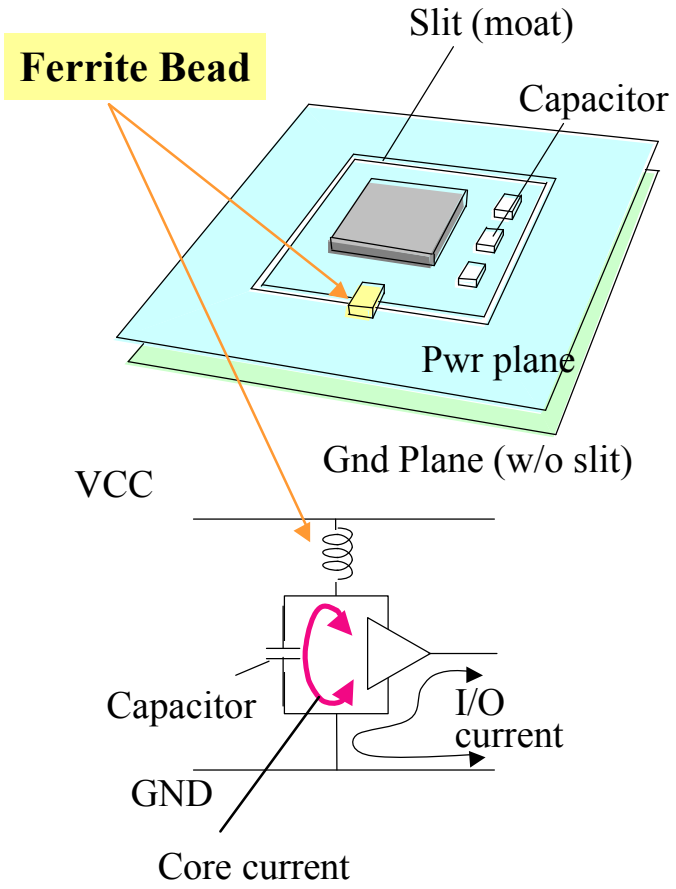


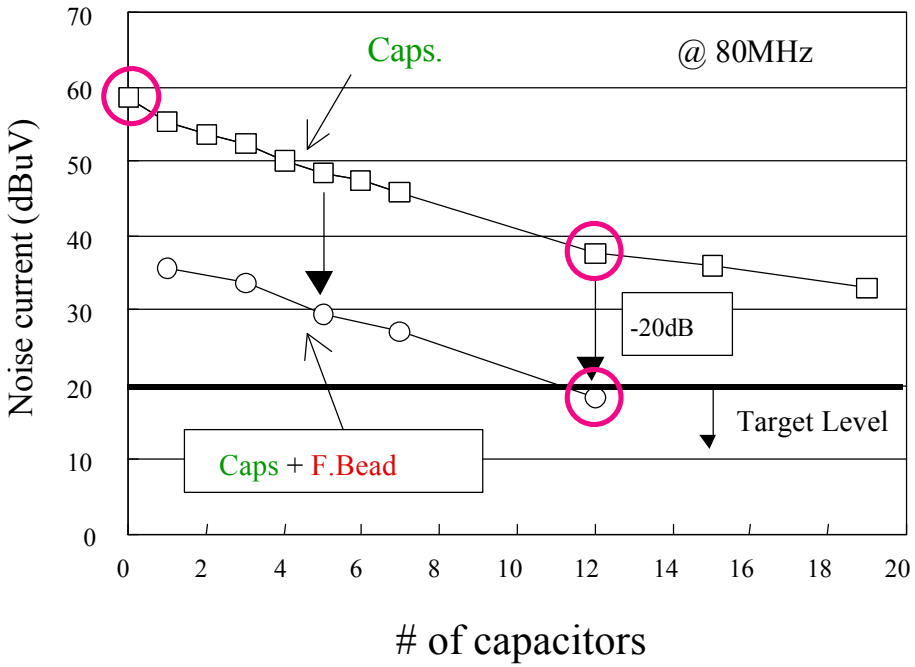
Decoupling evaluation board

- Investigation for supply decoupling



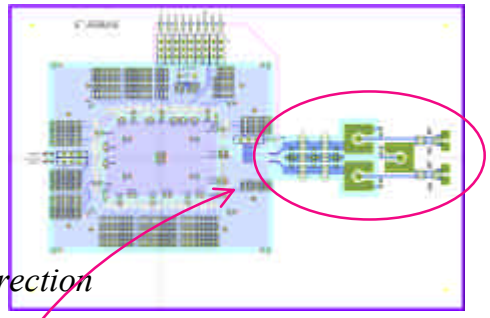
Supply Decoupling using Ferrite-Bead

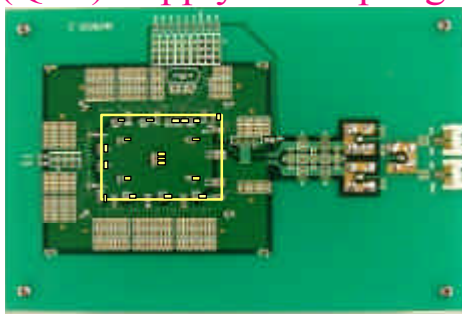




SH7055R(QFP) Supply Decoupling Evaluation

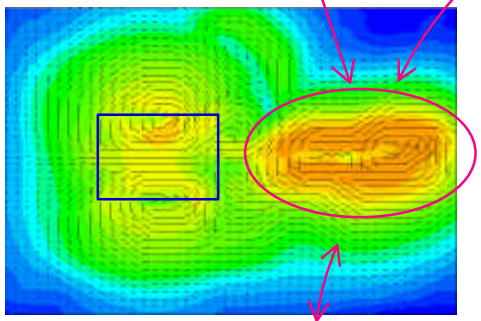
Compare the level of "RF current" in supply lines



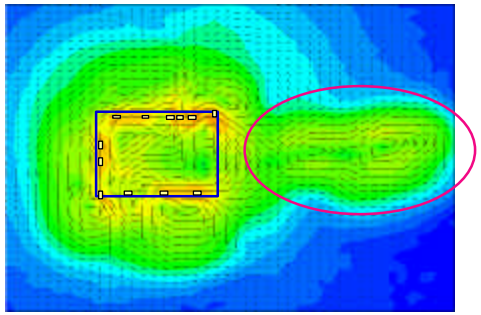


Black bars represent current direction

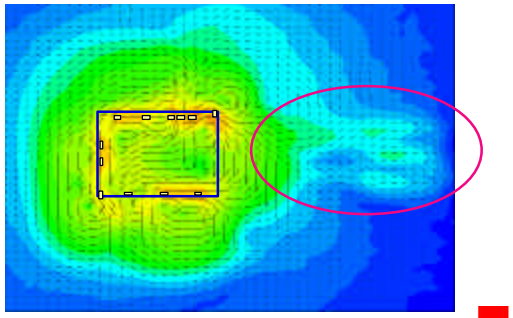
@ 80MHz



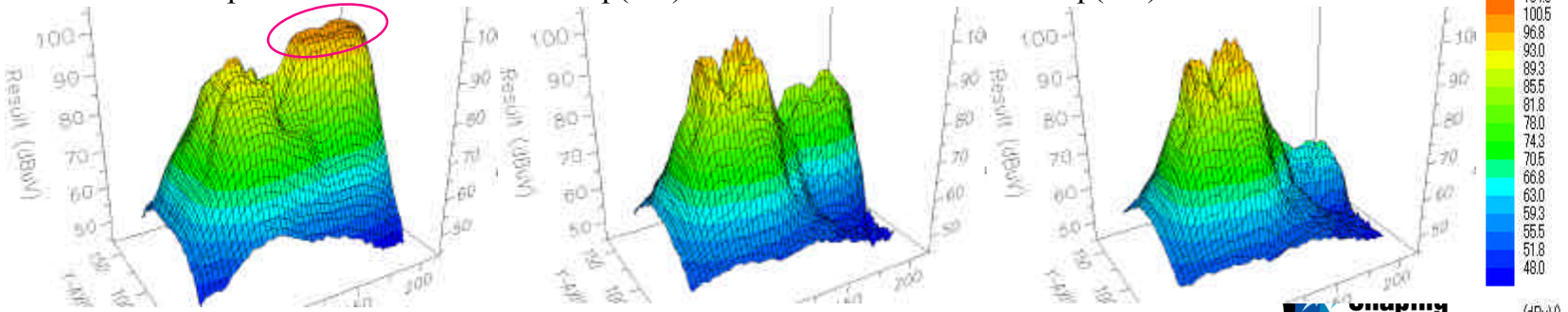
Ref : No Cap



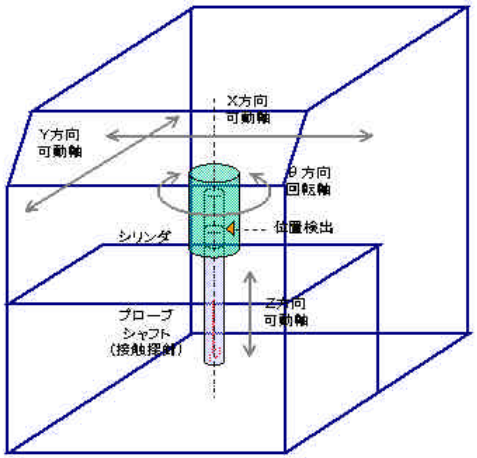
Cap(**t12**)

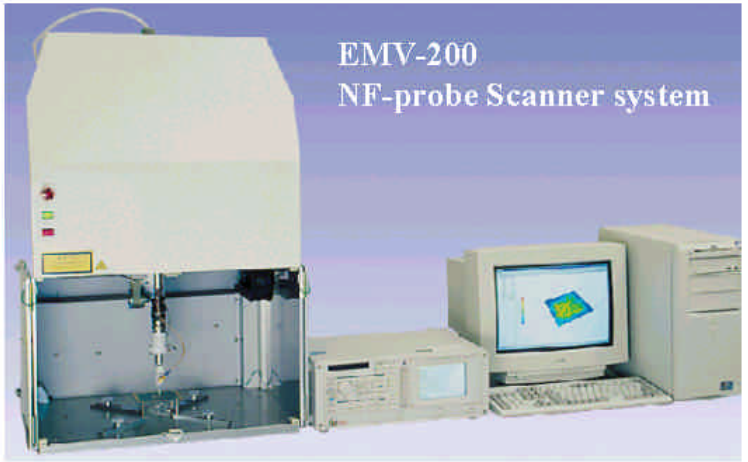


Cap(**t12**)+ **FB**

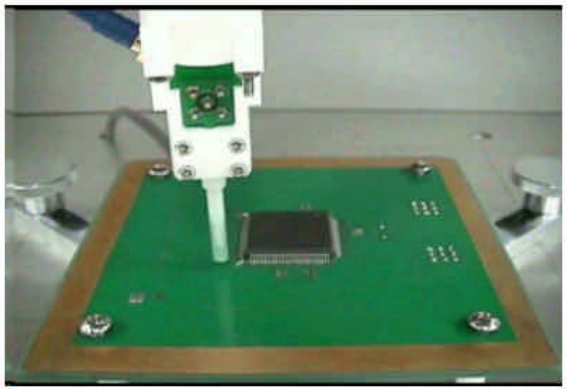


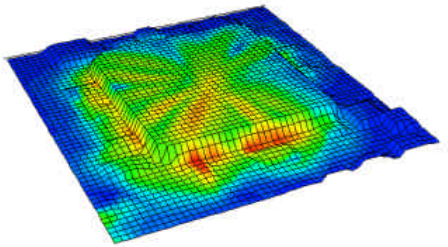
Four-axis Near Field Scanner





- Scan area : 300x300mm

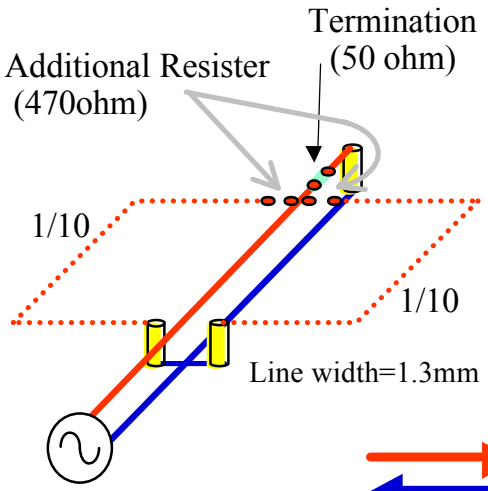


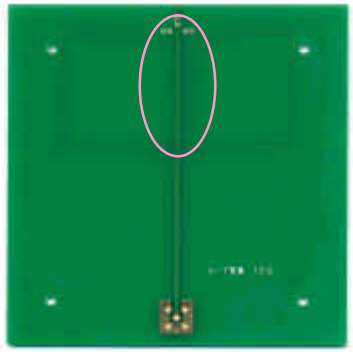


Example of "Surface scanning

http://www.hitachi.co.jp/HDEV/products/production/emi2/

NF-Probe evaluates Fwd/Bkd current balance in PCB

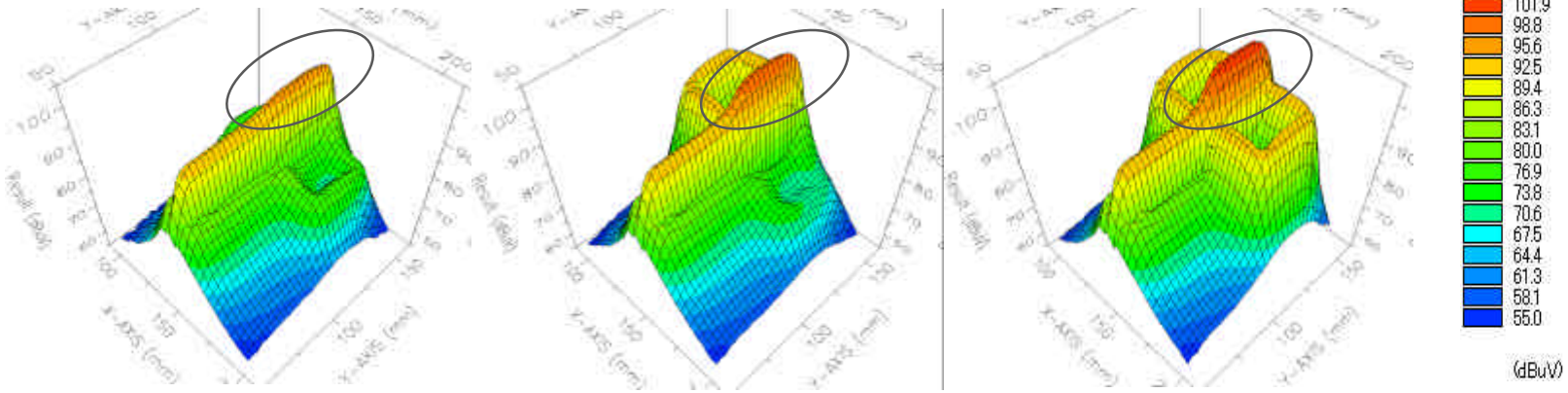




Far field field strength estimation

Point out the location generating Common mode current

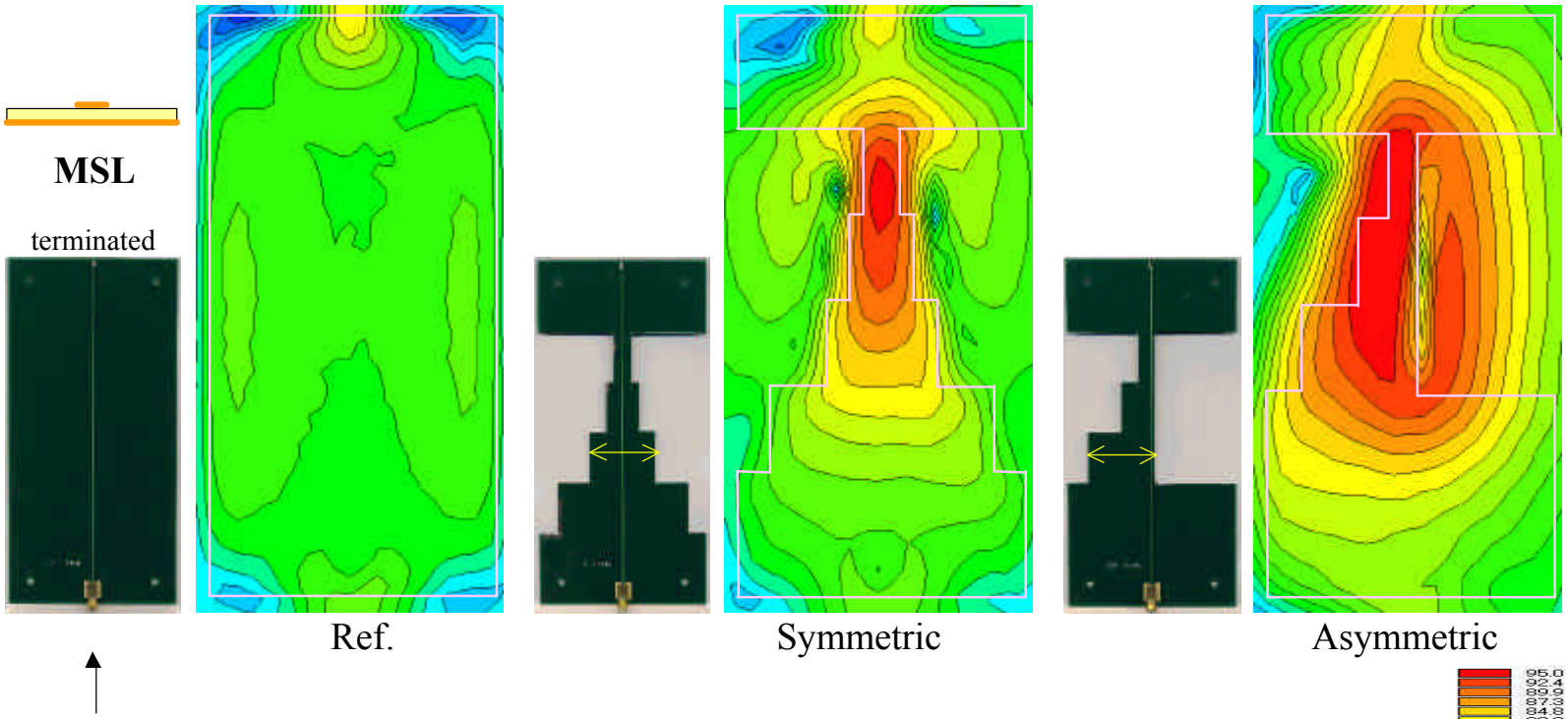
h=2.5mm



L op_R op | L 470_R op | L 470_R 470

Narrow & Asymmetric Ref. plane effect

pitch : 5mm Scan hight : 10mm
Scanned from bottom side (Ref. plane)



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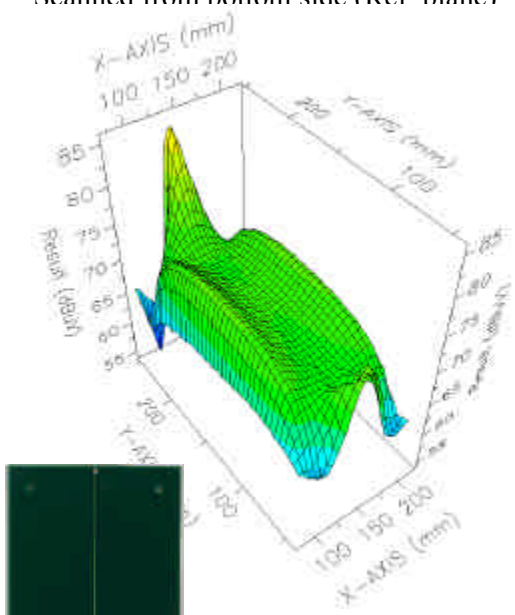

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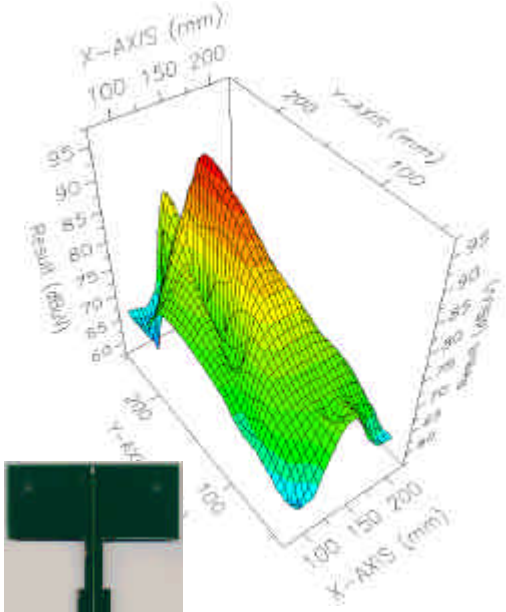
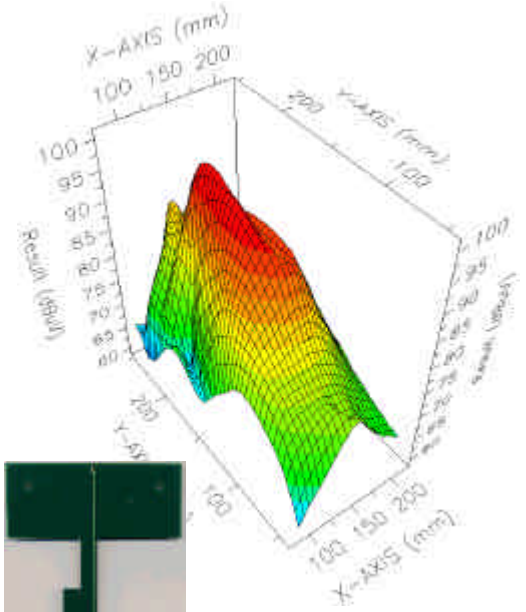


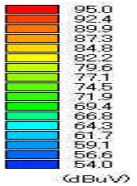
Symmetric



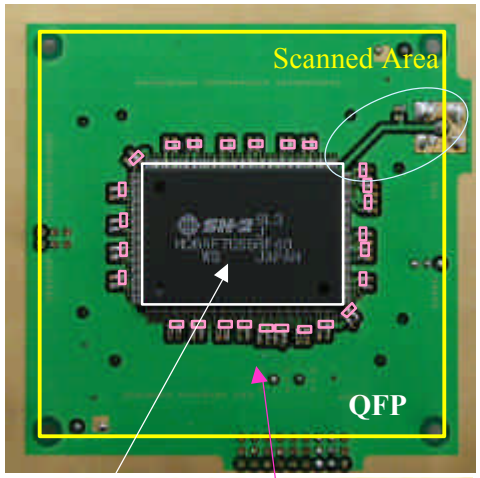
Asymmetric

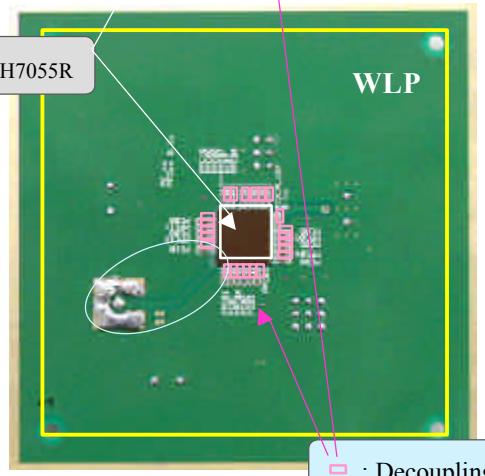
100MHz (Sinusoidal)
Vp-p:1.0 volt input applied

@100MHz



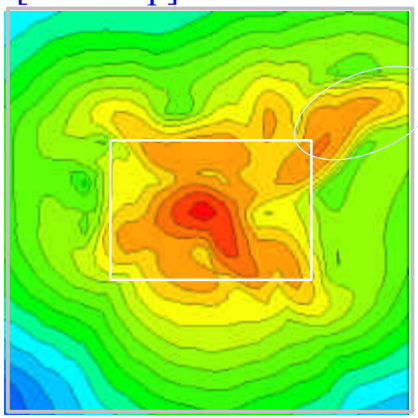
"QFP vs WLP" Current distribution [NF-probe scan]

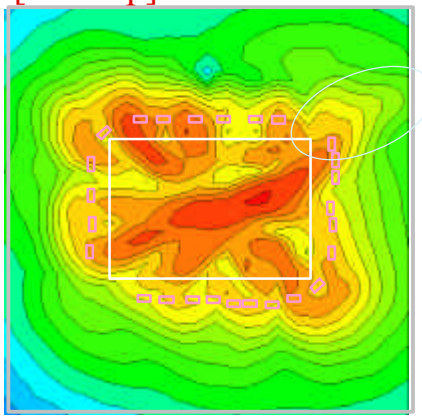


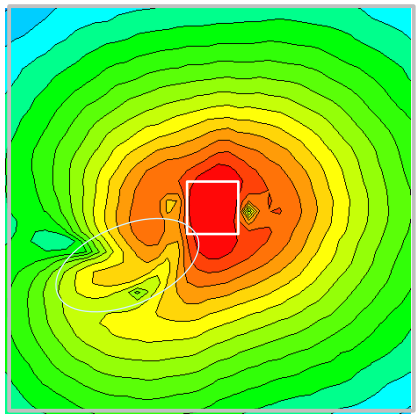


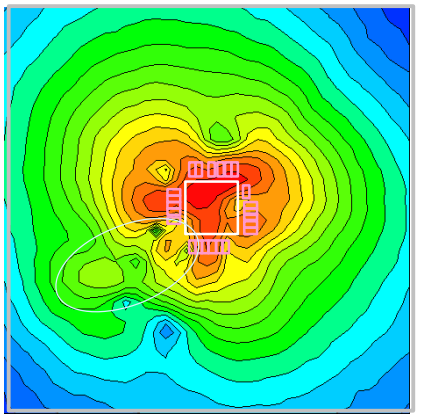
[w/o Cap]

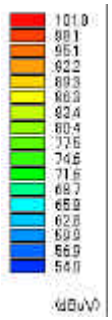
[w/ Cap]











@80MHz

Pitch : 2mm, Height : 5mm (above board)

Shaping intelligence
HITACHI SEMICONDUCTOR

SH7055R

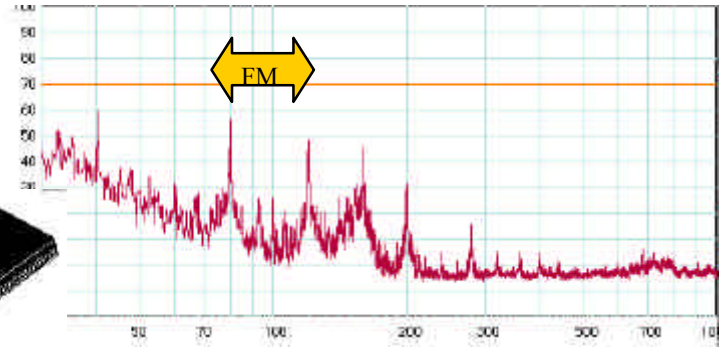
Conducted emission "QFP vs WLP" [VDE method]

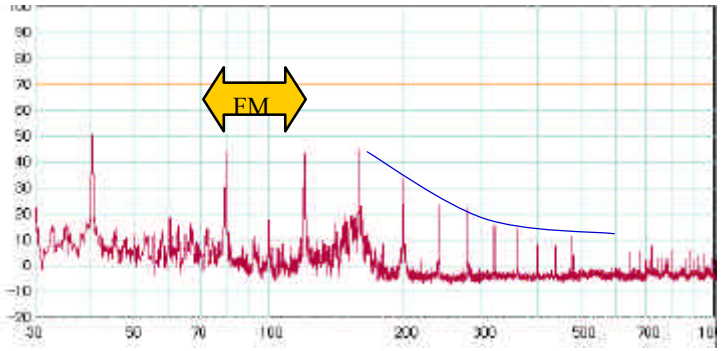
[w/o Cap]

[w/ Cap]

Vcc 12 Caps
PVcc 14 Caps

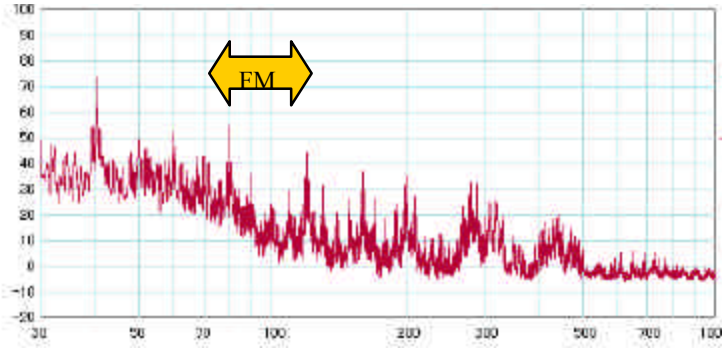
QFP

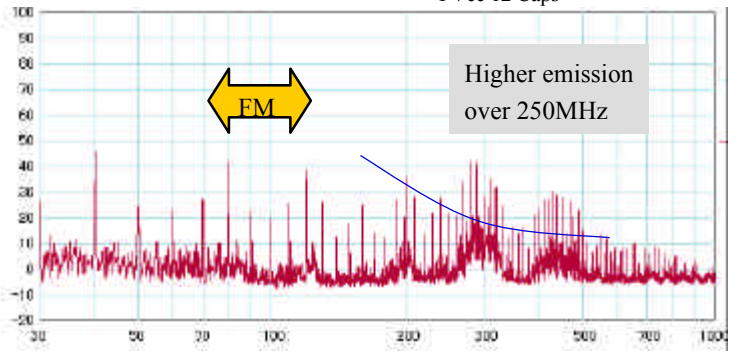




Vcc 11 Caps
PVcc 12 Caps

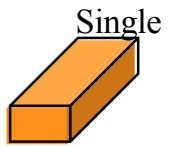
WLP



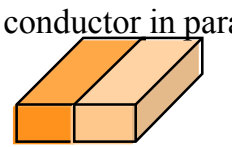


Higher emission
over 250MHz

Inductance comparison "QFP vs WLP"

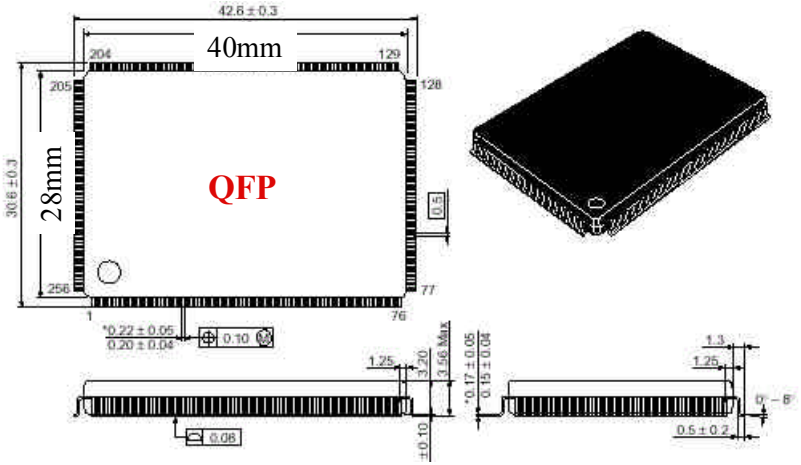


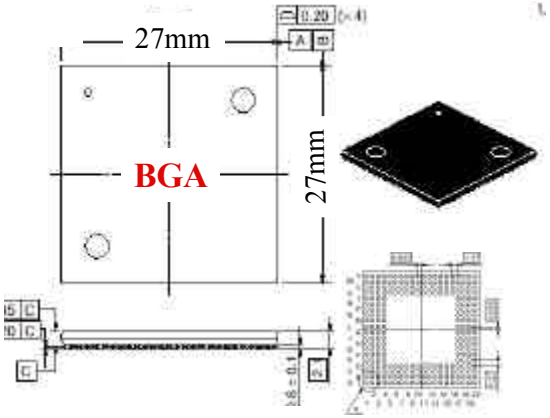
10nH

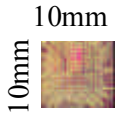


(10nH+8nH) x 1/2 = 9nH

Mutual inductance





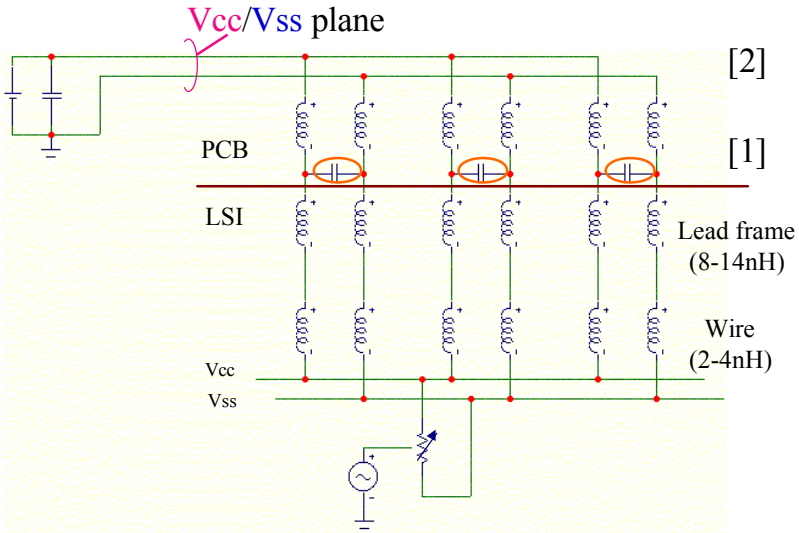


CSP

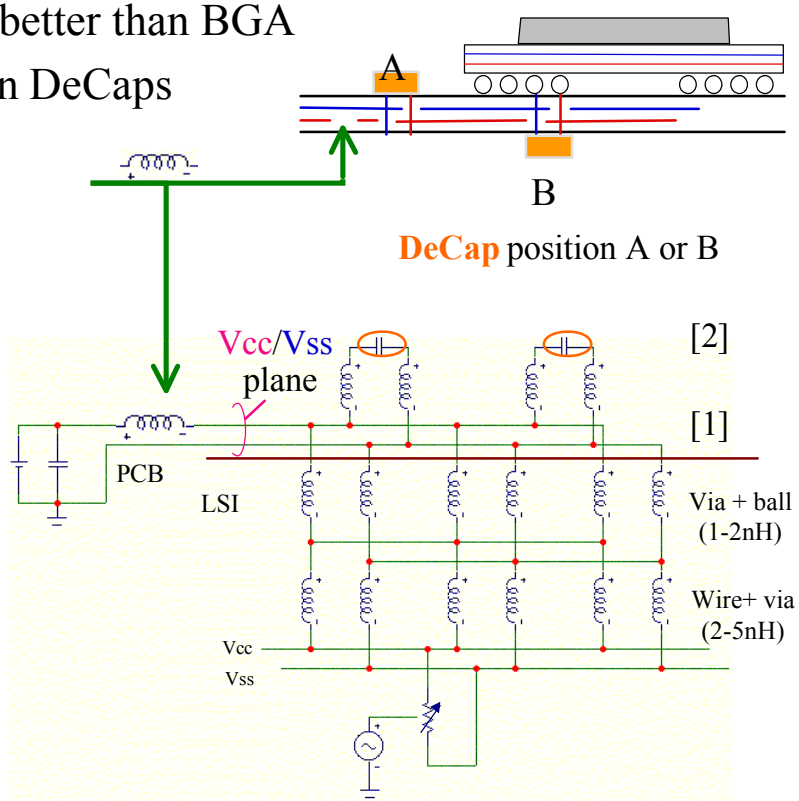
(Leff)	QFP	BGA	Pwr/Gnd	CSP
Wire part	2.0 - 3.0nH	2.0 - 3.0nH	(1.8 - 2.2nH)	-
Rest of wire part	5.0 - 8.5nH	2.0 - 3.5nH	(0.8 - 1.2nH)	0.7 - 2.5nH
Total	7.0 - 11.5nH	4.0 - 6.5nH	(2.6 - 3.4nH)	0.7 - 2.5nH

Decoupling Capacitor connection [QFP vs BGA]

- Typical DeCap connection for QFP is better than BGA
- V/G plane is closer to Vcc/Vss pin than DeCaps
  - Needs treatment to reduce current flow from V/G plane

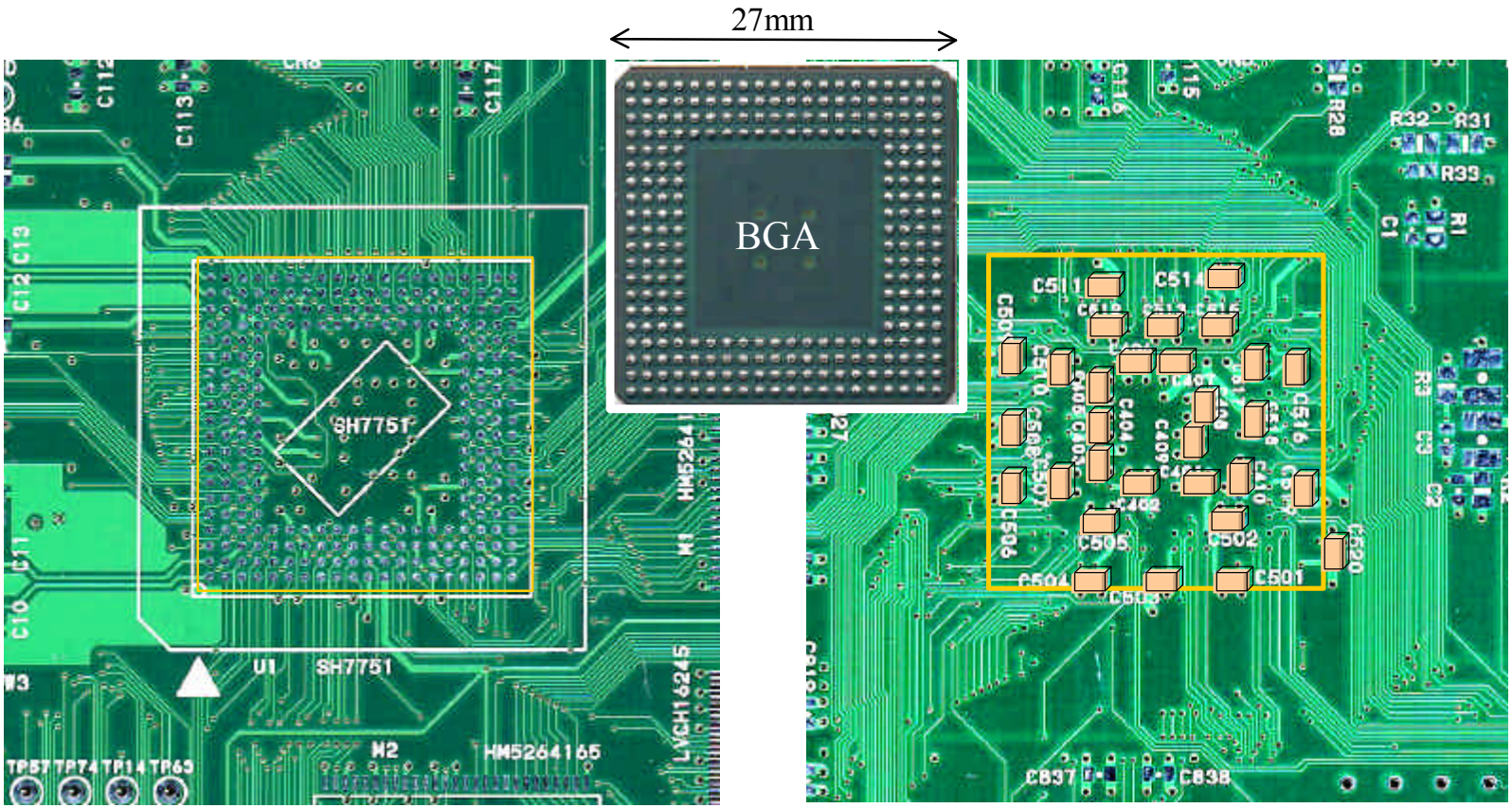


[QFP package + PCB]



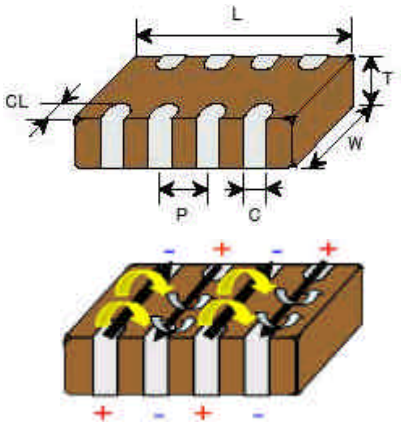
[BGA package + PCB]

Decoupling capacitors for BGA



Topside (BGA mount) Bottom side

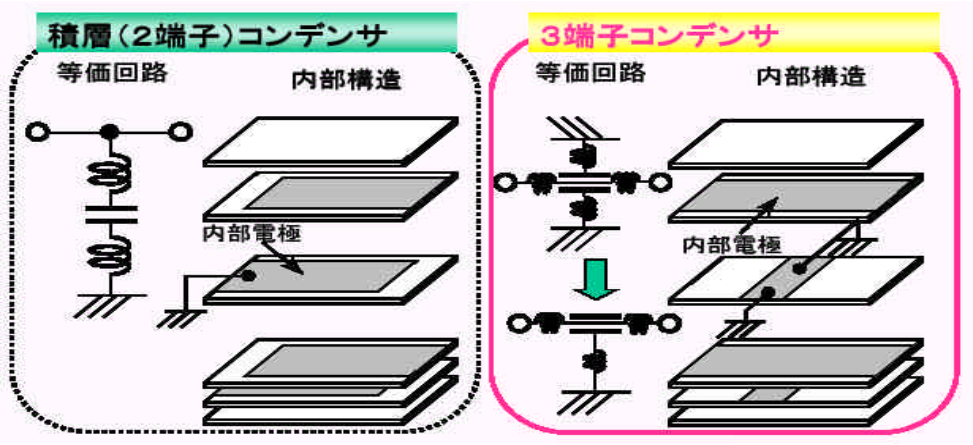
Cost effective Low ESL Capacitors



"IDC" type capacitor

(単位: mm)

	CLLD11 SERIES
L	2.00±0.15
W	1.25±0.15
T	0.85±0.10
C	0.30±0.10
CL	0.20±0.10
P	0.50±0.10

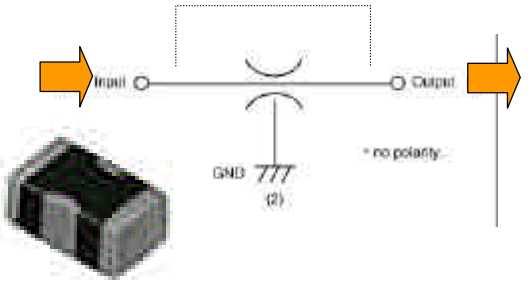


Conventional SMD

Feed through (Three terminal)

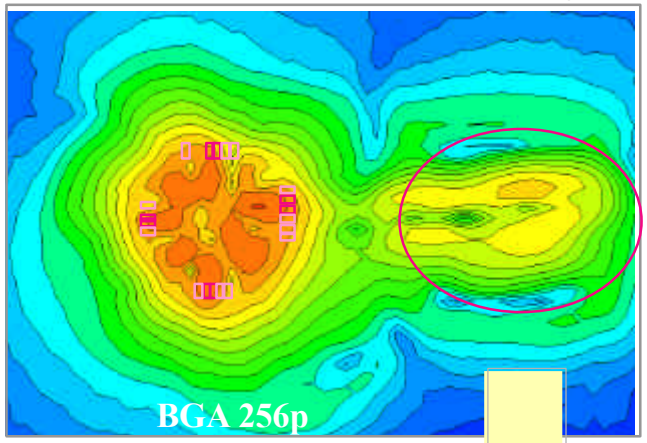
Capacitance	1.0μF
Lower Tolerance	-20%
Upper Tolerance	80%
Rated Current	2A
Rated Voltage	16Vdc
Insulation Resistance	500M ohm min.
Withstand Voltage	
Max. of DC resistance	0.03ohm
Min. of Operating Temp.	-40°C
Max. of Operating Temp.	85°C
Length	2.0mm
Width	1.25mm
Thickness	0.85mm

No extra Path!
100% supply must be fed through



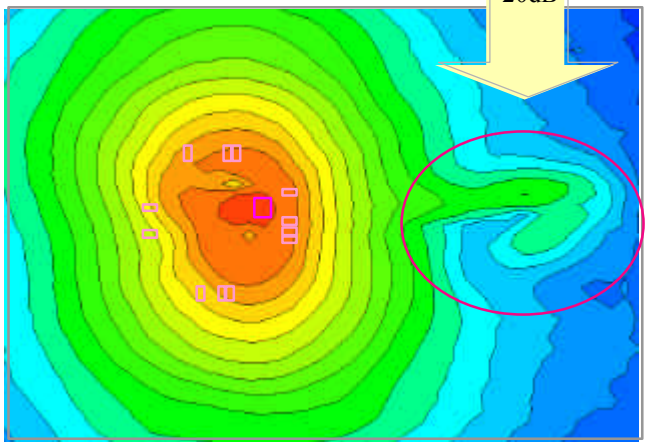
Feed through Capacitor (BGA)

Near Field Scan [Macro (Sensitive) probe] @80MHz

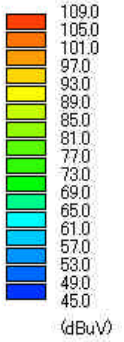


8 DeCaps
(0.1mF*8)

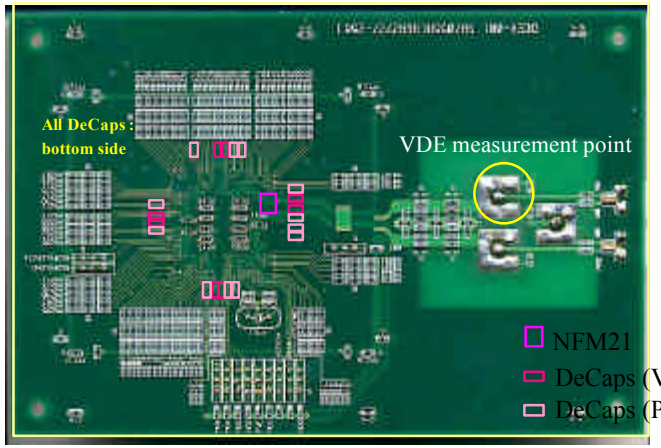
-20dB



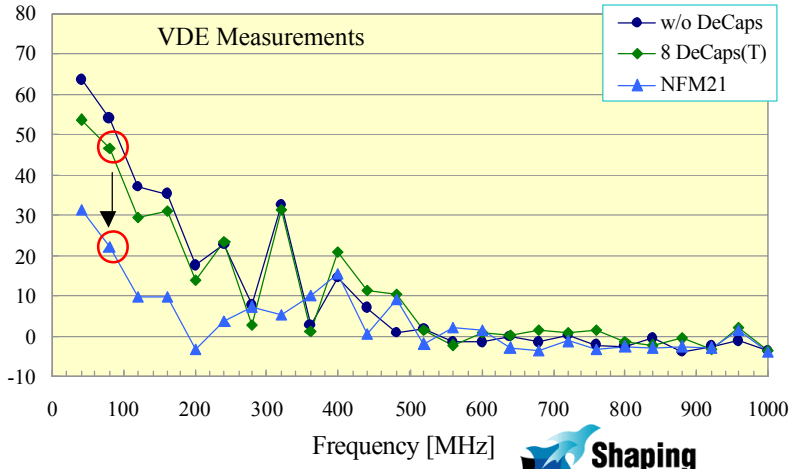
One
Feed Through
(1mF)



SH7055R (40MHz)



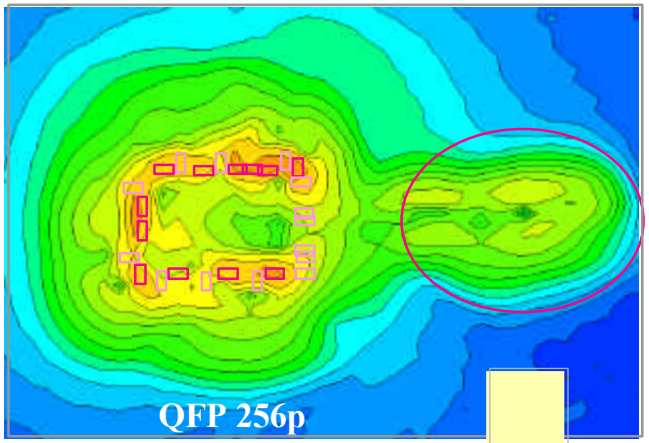
BGA



Shaping intelligence
HITACHI SEMICONDUCTOR

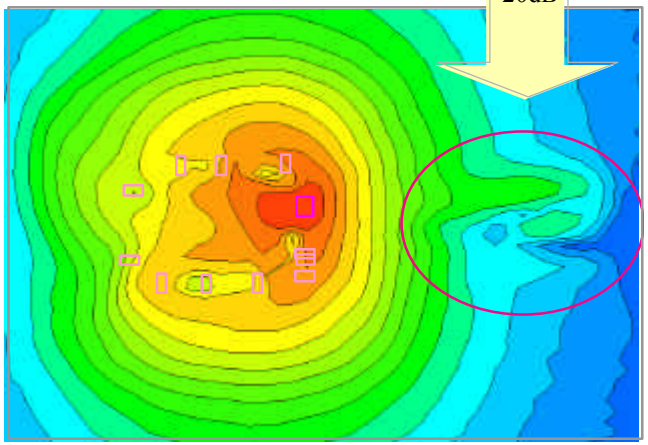
Feed through Capacitor (QFP)

Near Field Scan [Macro (Sensitive) probe] @80MHz

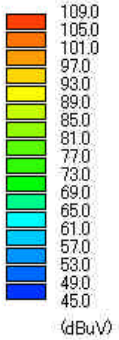


12 DeCaps
(0.1mF*12)

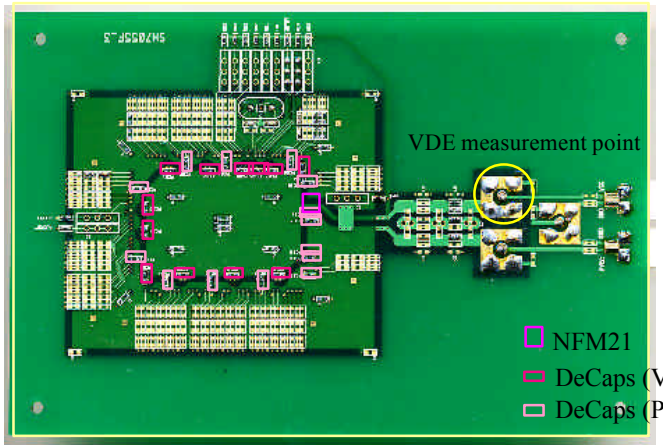
-20dB



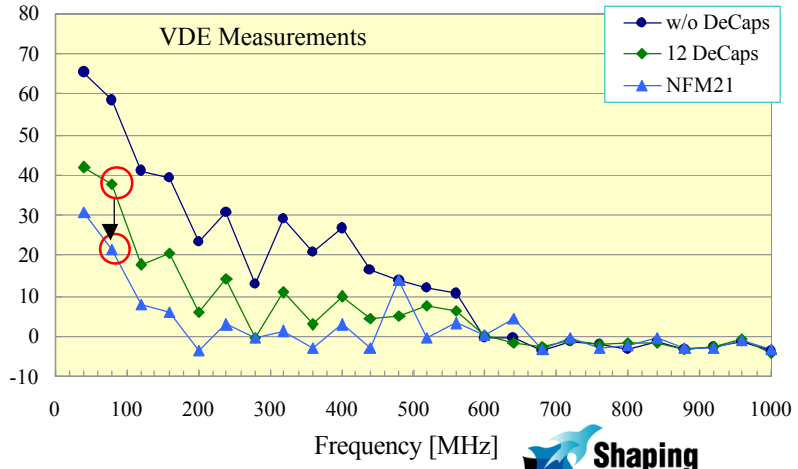
One
Feed Through
(1mF)



SH7055R (40MHz)

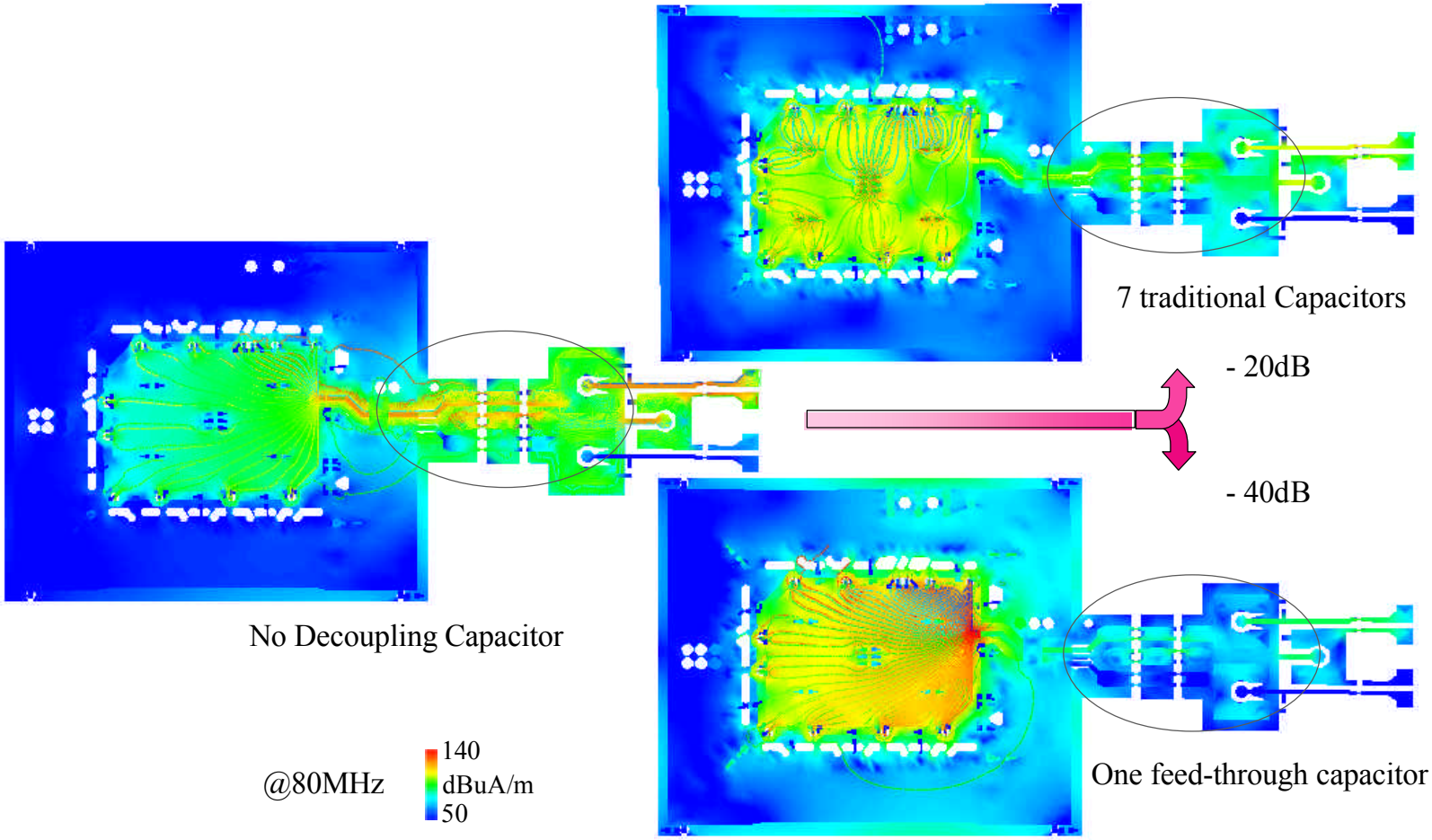


QFP

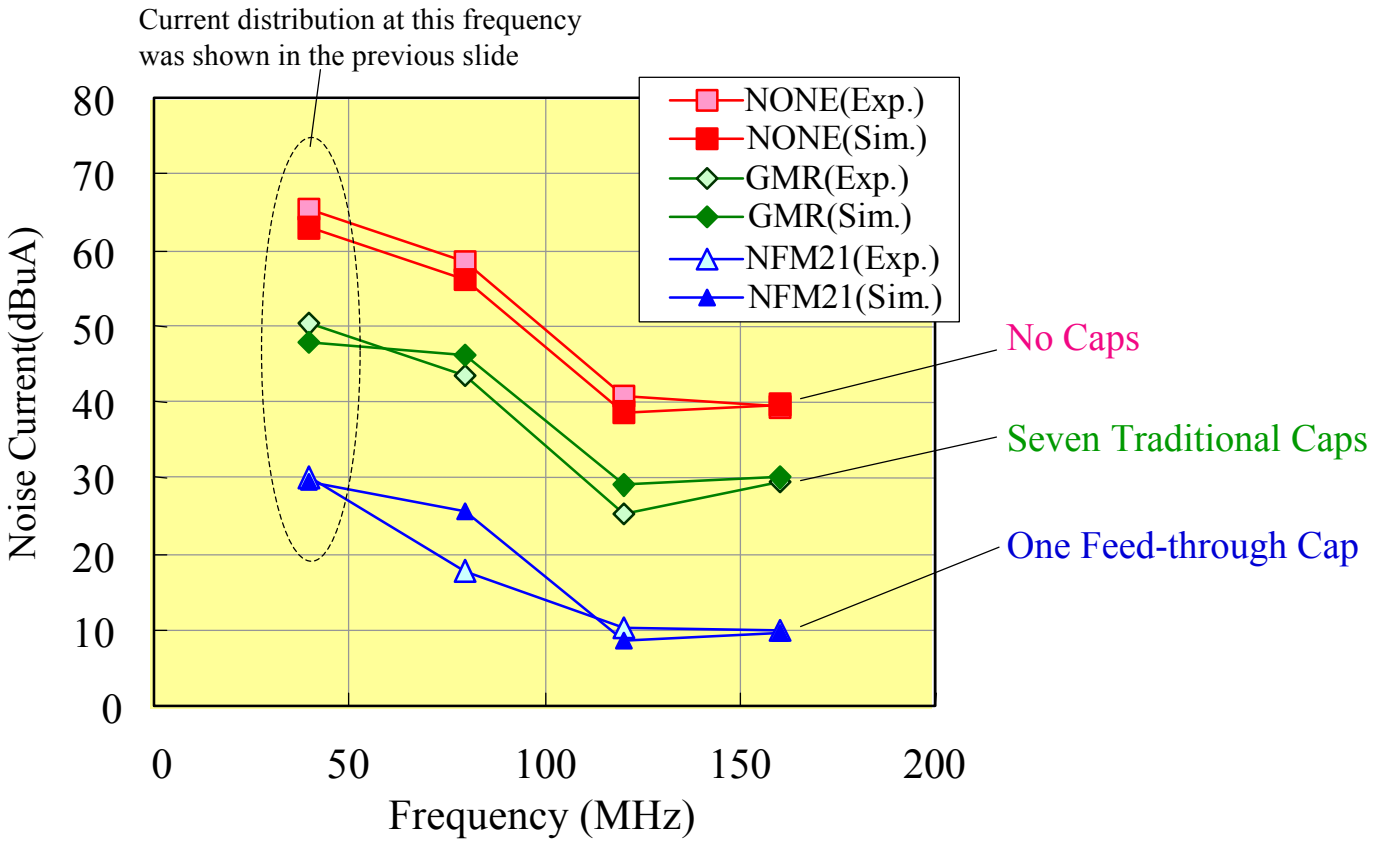


Shaping intelligence
HITACHI SEMICONDUCTOR

Current distribution [Simulation/ECTAS]



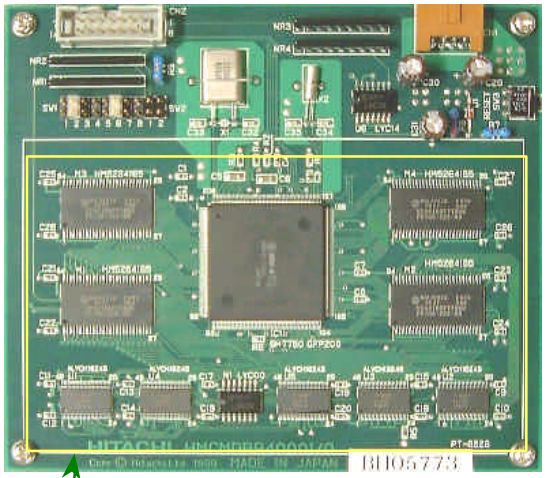
Effectiveness of Feed-through capacitor [Exp. vs Sim.]



Conducted emission reduction capability “Conventional” vs “Feed through”

Radiation from External BUS

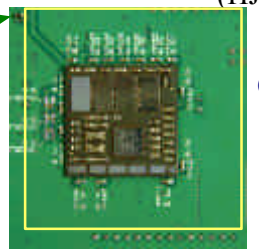
Area and Level of RF currents can be reduced by using SiP
--> Low radiation chance from PCB



MCM

[SH4+SDRAM] demo board(4L) (HJ940001BP) equivalent

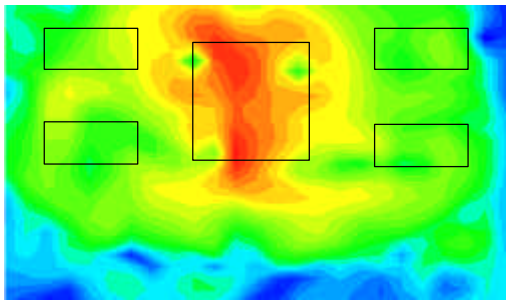
Scanned Are



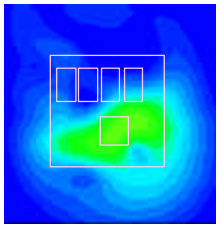
@ 81.0MHz (Ext BUS Freq)

Prog Exec (same prog for Demo board and MCM)

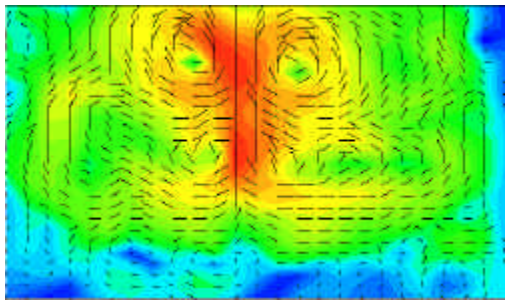
MCM (HJ940001BP)



Scanned plane : above 5mm from board surface

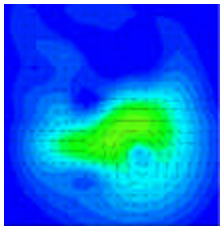


Scanned plane : above 5mm from chip surface

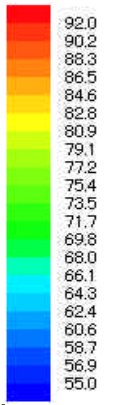


Current Direction Plot

Common Scale



Current Direction Plot



Summary

- Short trace interconnection (in SiP) solves most of the SI concern
- V/G plane analysis takes more important role for CSP age system
- Reduced EMI design is base on “Supply decoupling.” (for Single chip MPU)
- NF-Scanner shows us locations generating “Common mode” current
- Direct connection to V/G plane for CSP (BGA) is not recommended
- Feed-through Capacitor is a good solution for CSP’s decoupling
  saving space, great decoupling capability, making sense (cents)
- PCB design locating RF current trace adjacent to Gnd (return) path
  reduces emission. (ex. FC-SiP)