Full Chip Analysis

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Outlines

I. Introduction
II. Circuit Level Analysis
III. Logic Level Analysis
    I. Timing Analysis
    II. Functional Analysis
IV. Mixed Signal Analysis
V. Research Directions
VI. Conclusion

I. Introduction

1. Trends of On-Chip Technologies
2. Statistics About Design Flaws
3. Spectrum of Analysis

I.1 Trends of On-Chip Technologies

System:

Huge Numbers of Devices and Wires

Power/Ground Distribution:

Low Voltage, High Current

Wires: Lateral Coupling, Fragmented Parasitics

Devices: Modeling, Noise

Mixed Signal Design: RF+Analog+Digital

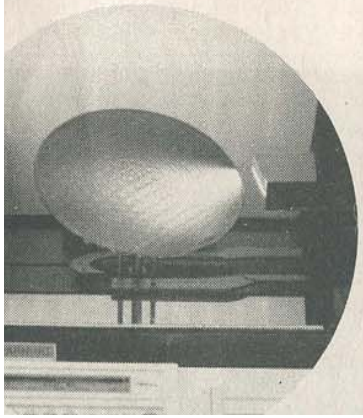
intel.com

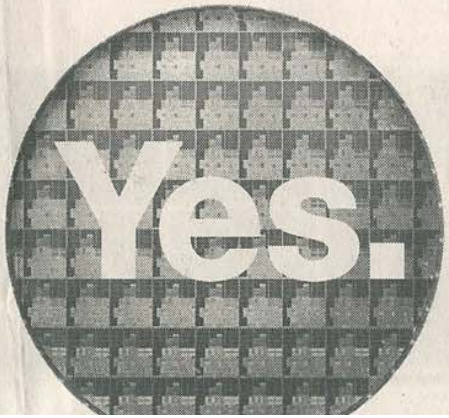
Will Moore's Law stand forever?

In 1965, Intel's Gordon Moore created a "law" that became shortha for the rapid, unprecedented growth of technology. He predicte that the number of transistors on a chip would grow exponentiall with each passing year

to fulfill Moore's Law, year after year, companies everywhere can do more at lower cost. And that's not just a good law.

It's very good business.





intel®

Power/Ground Distribution (ITRS)

Lower V margin: Higher I & Inductance x Freq.

	2002	2003	2004	2005
Supply Voltage(V)	1.5	1.5	1.2	1.2
Max Power	130	140	150	160
On-Chip Freq(MHz)	1,600	1,724	1,857	2,000
Off-Chip Freq(MHz)	885	932	982	1,035

Flip Chip Dynamic Effects

F:MHz	Vdd	Static	Dynamic		Dynamic Total	Static vs. Dynamic
		IR	*Ri(t)*	*Ldi/dt*		
250	1.8	9.9 mV	17.3 mV	1.2 mV	18.5 mV	0.5% 1.02%
500	1.5	16.2 mV	29.3 mV	12.3 mV	41.6 mV	1.08% 2.77%
750	1.2	19.3 mV	36 mV	28.5 mV	64.5 mV	1.6% 5.37%
1,000	1.0	22 mV	38.8 mV	41.6 mV	80.4 mV	2.2% 8.0%

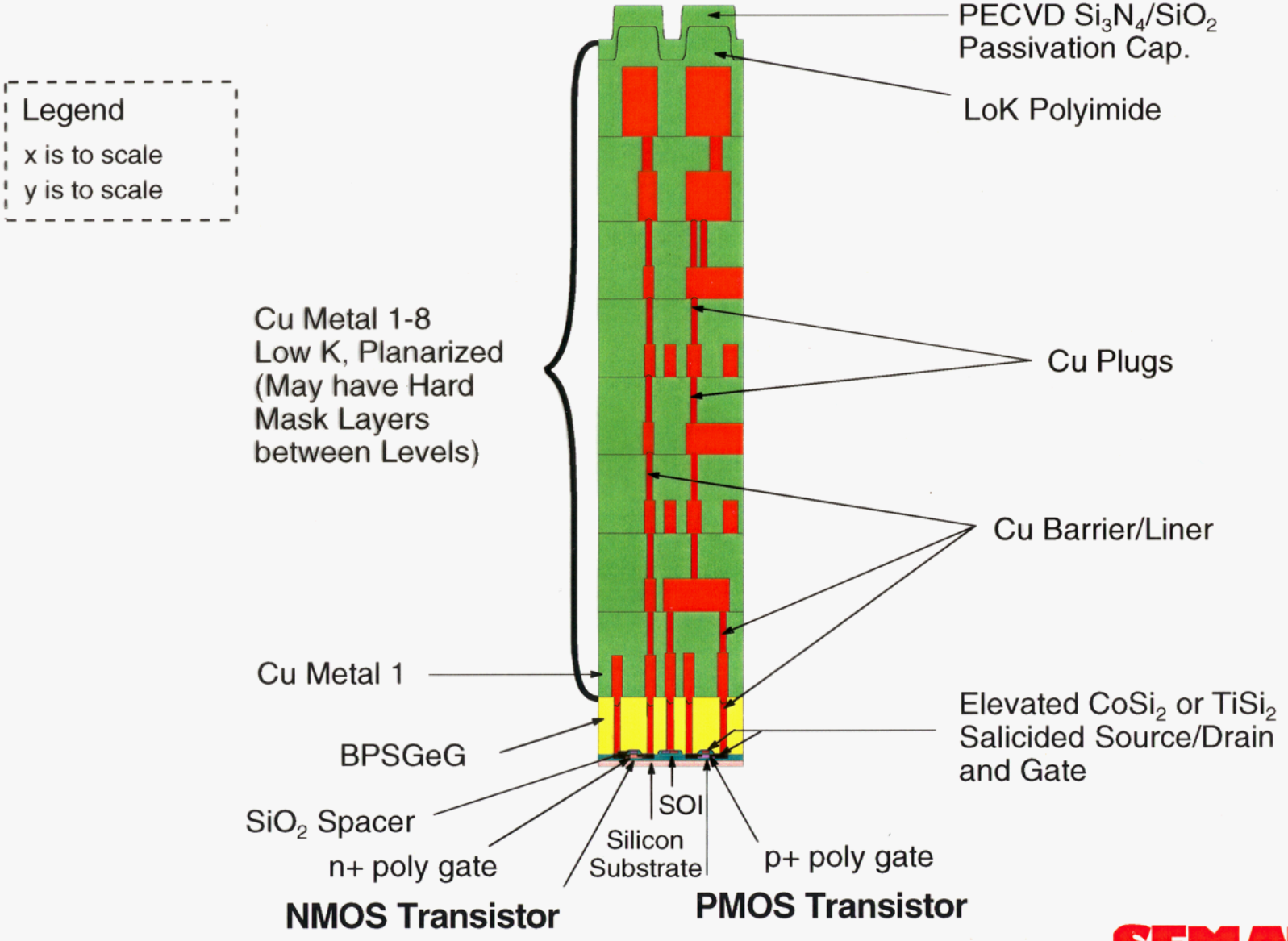
Courtesy of Apache

Wire-bond Dynamic Effects

F:MHz	Volt	Static	Dynamic		Dynamic Total	Static vs. Dynamic
		IR	*R i(t)*	*Ldi/dt*		
133	1.8	103 mV	147 mV	3 mV	150 mV	5.7% 8.3%
250	1.5	181 mV	275 mV	13 mV	288 mV	12% 19.2%
400	1.2	200 mV	276 mV	75 mV	351 mV	16.6% 29.2%

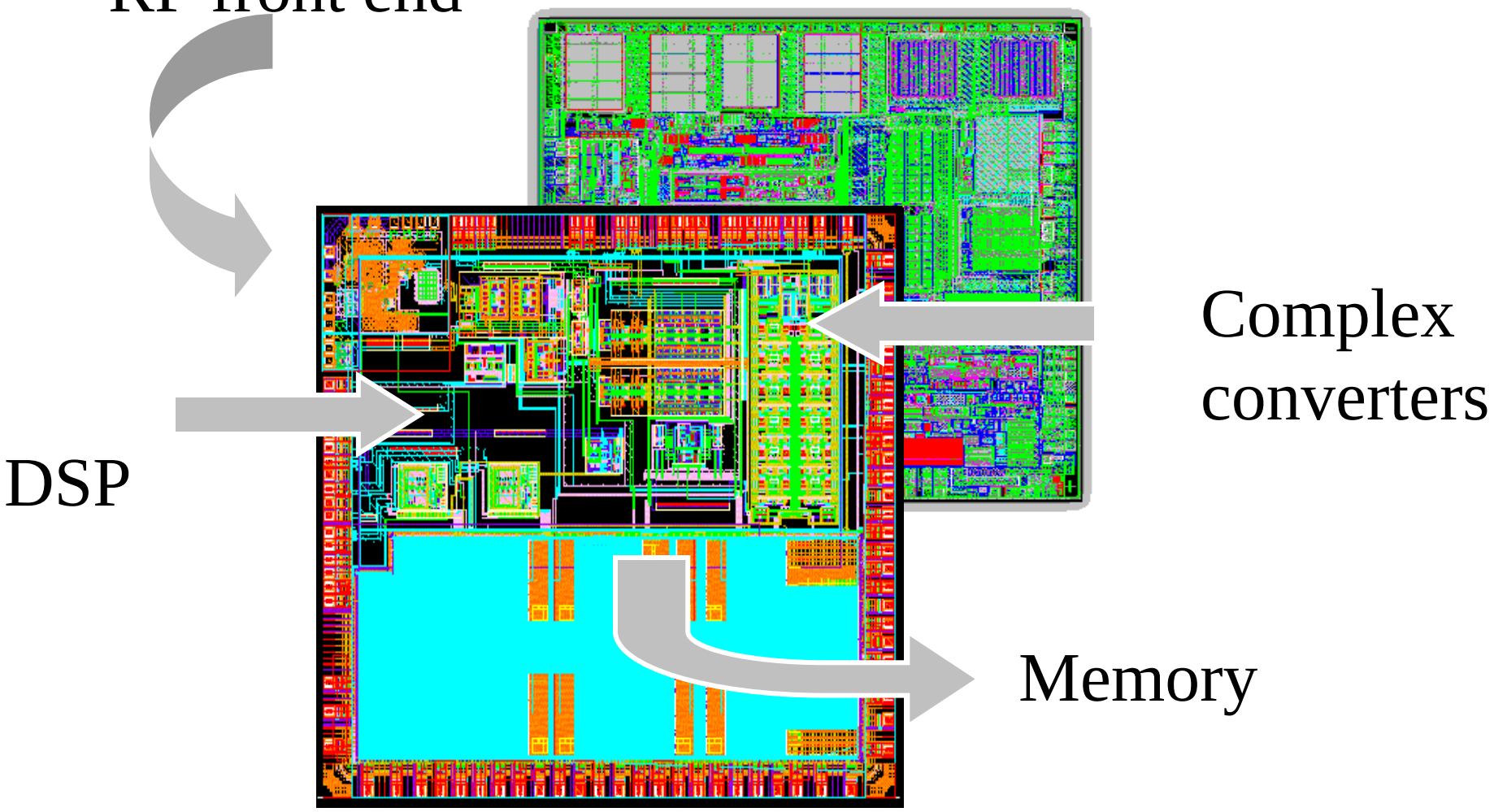
Courtesy of Apache

0.10µm CMOS Process Schematic
"High Performance" Logic



SEMATECH

Increasing System Complexity

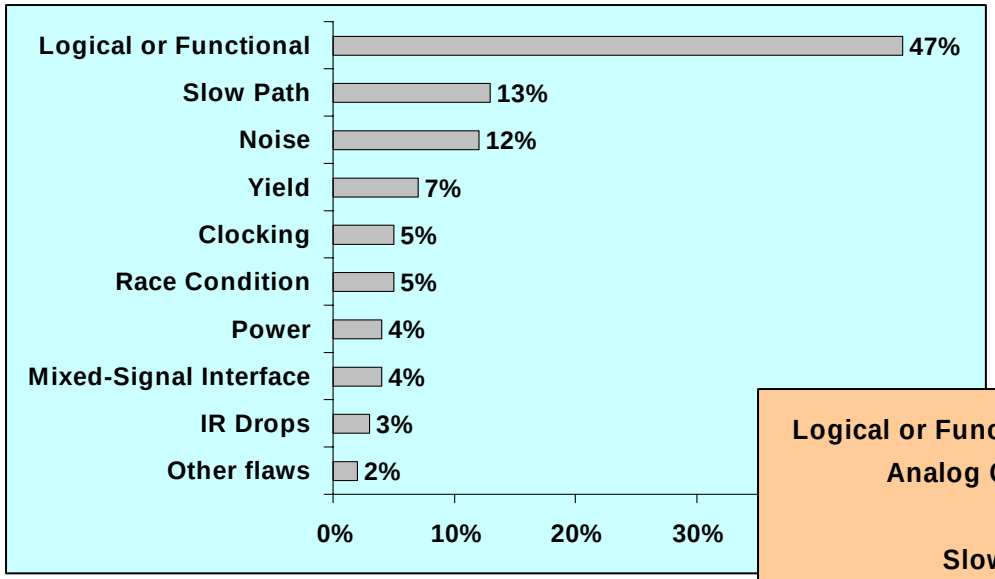


Courtesy of Mentor

I.2 Statistics about Design Flaws

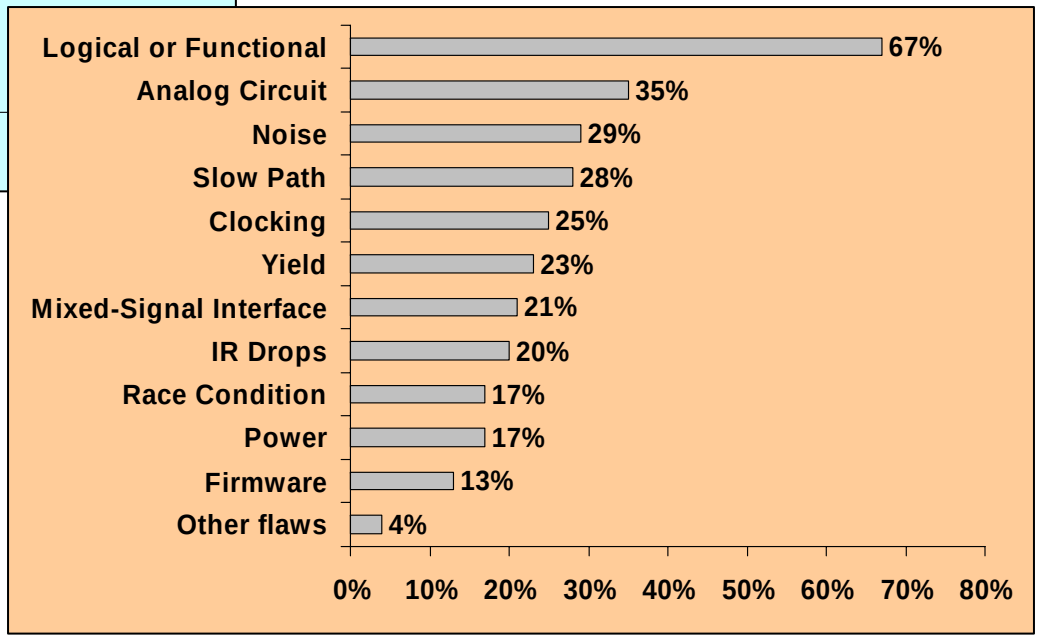
Percent of Total Flaws Fixed in IC/ASIC Designs Having Two or More Silicon Spins

Collett Intl. 2000 Survey



- Logical or Functional
- Slow Path
- Noise

- Logical or Functional
- Analog
- Noise
- Slow Path
- Mixed-signal interface
- Clock, Power/Ground
- Firmware



Collett Intl. 2001 Survey

I.3 Spectrum of Analysis

Device	Circuit		Logic				System
	Electrical	Behavior	Timing	Switches	Gate	RTL	

Physics

EE

Circuit theory

Complex, Real

Extraction

Precision

Math

CS

Engineering

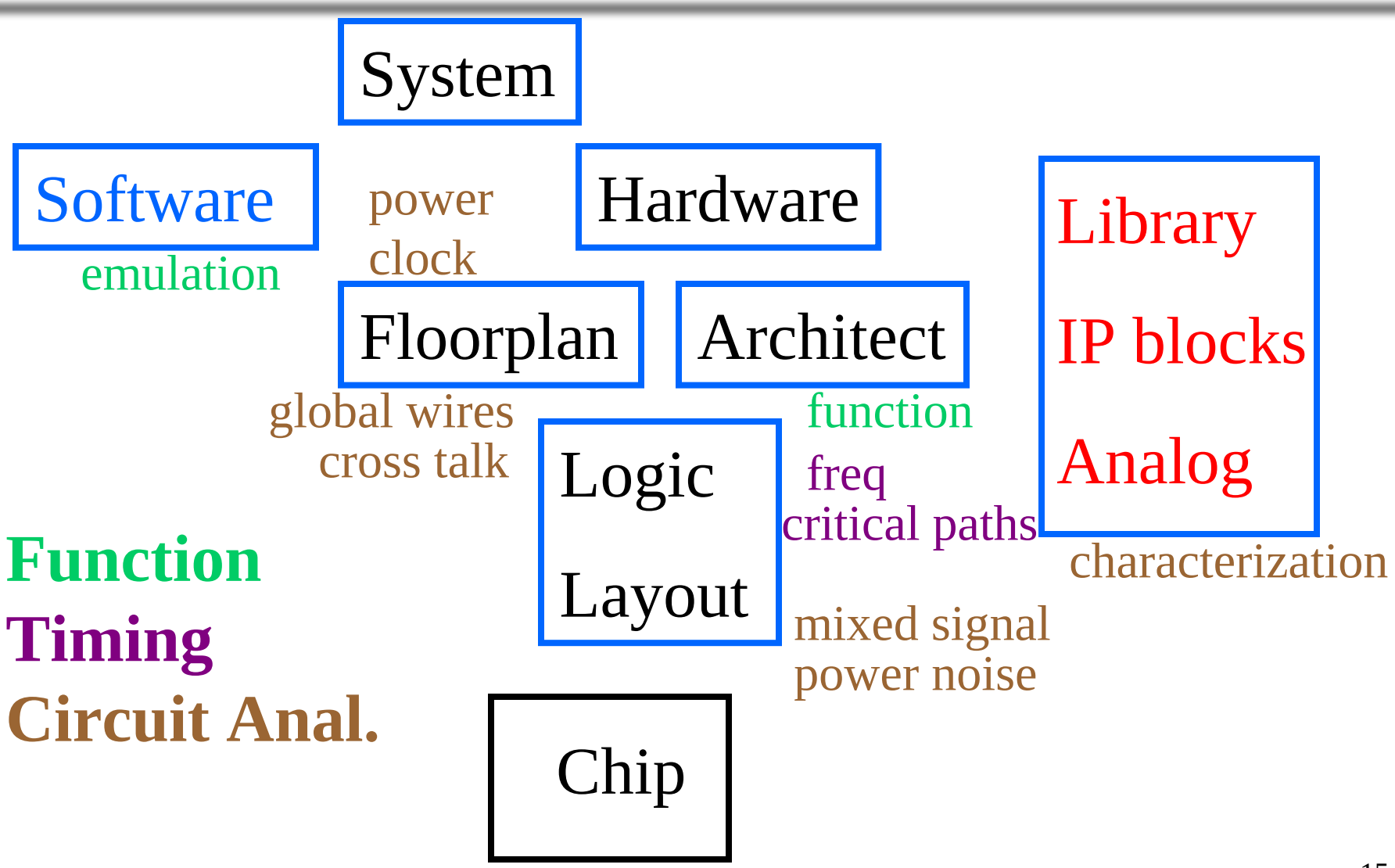
Algorithms

Database

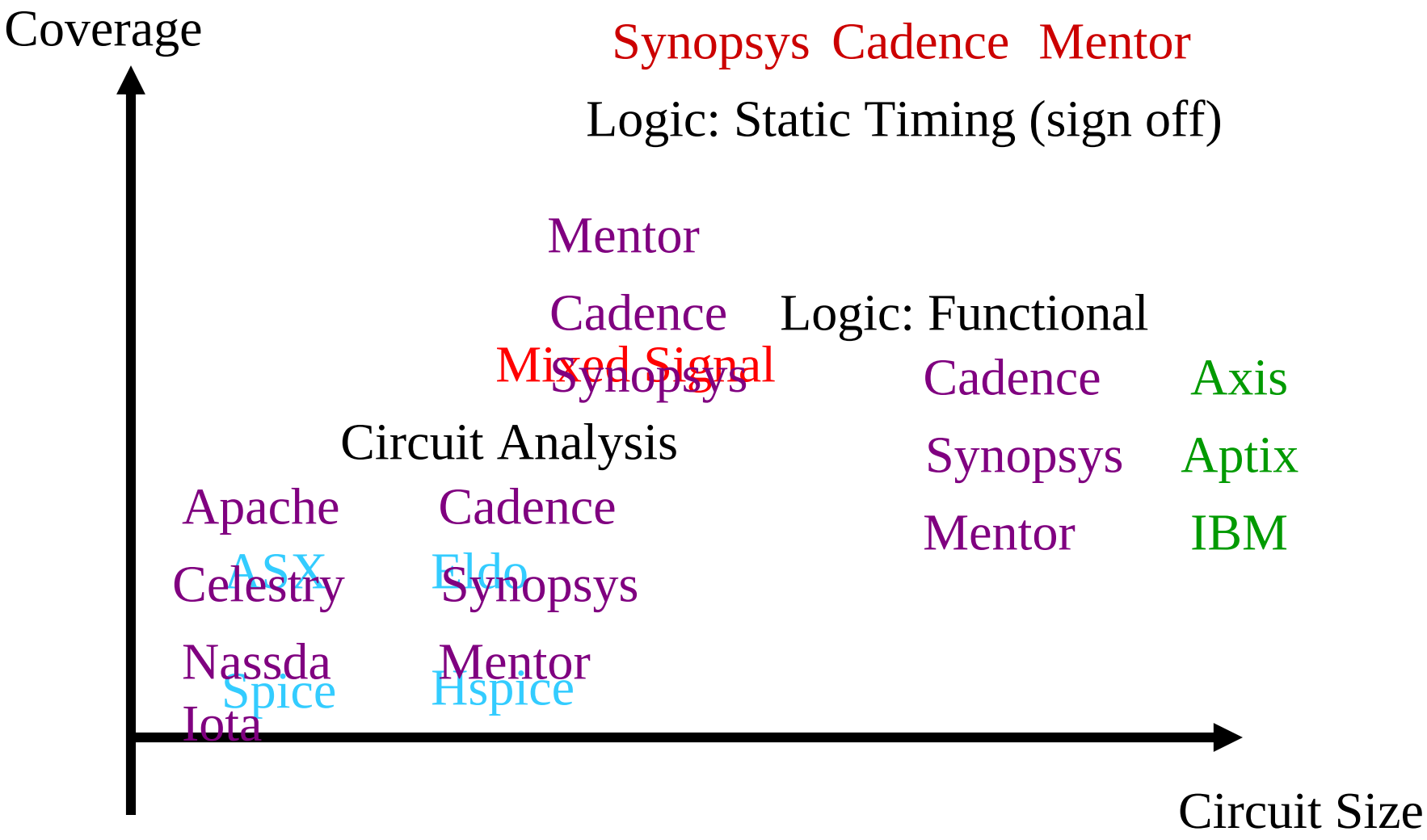
Programming

Discrete

I.3 Spectrum of Analysis(flow)



I.3 Spectrum of Analysis(coverage)



I.3 Spectrum of Analysis(trend)

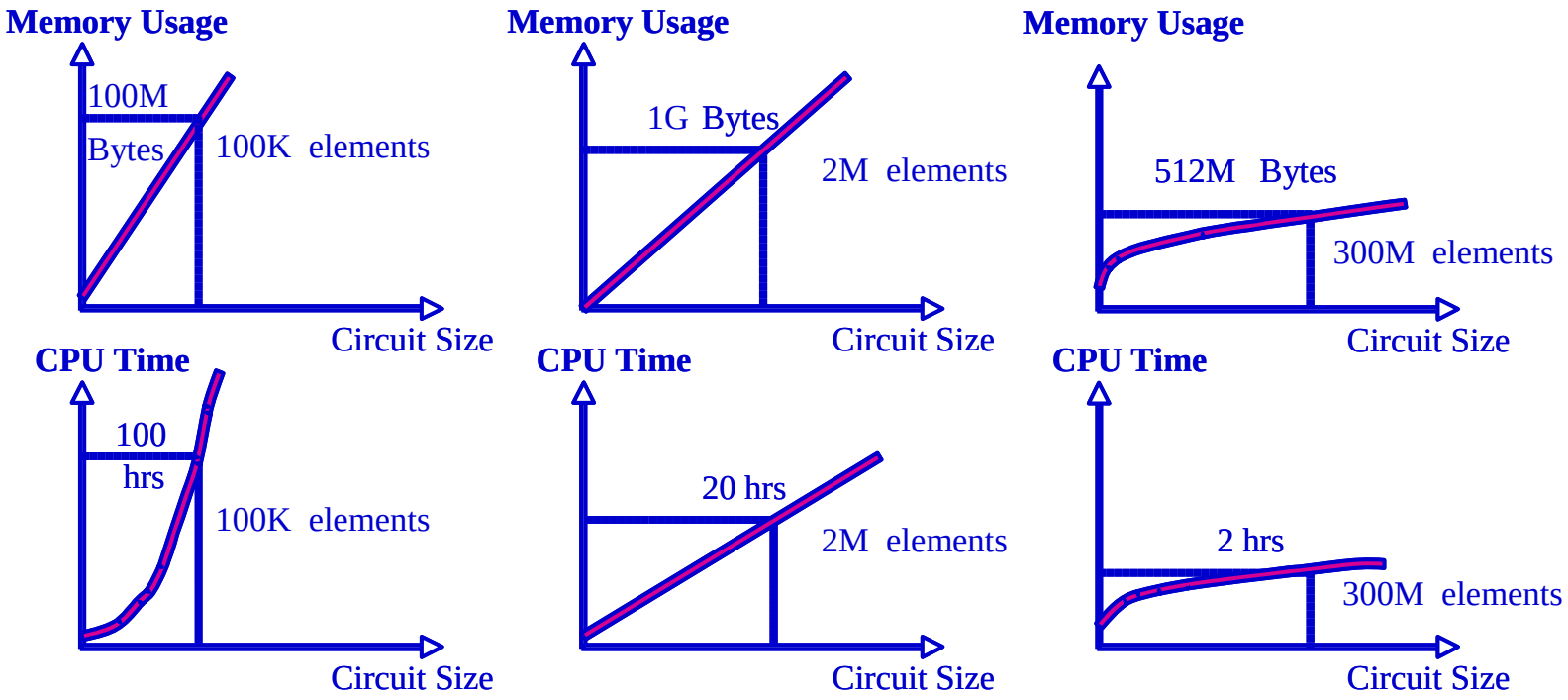
- Layout Dominated Analysis
  - Power/Ground, Clock
  - Wires
  - Pre-layout, Post-layout
- Layout Oriented Analysis
- EE + CS
  - EE=> CS High Complexity
  - CS=>EE Deep Submicron Effect
  - Accuracy and Efficiency

II. Circuit Level Analysis

1. Circuit Analysis Advancement
2. Circuit Analysis Techniques
3. Examples
4. Tasks

II.1 Circuit Analysis Advancement

1st Generation (SPICE) | 2nd Generation (Fast SPICE) | **Next Generation (HSIM)**



Courtesy of Nassda

II.2 Circuit Analysis Techniques

- Memory: Hierarchical Database
- Circuit Size: Parasitic Reduction
- Device Complexity: Table Model
- Simulation:
  - Backward Euler, Trapezoidal Integration
  - Hierarchical Flow
  - Event Driven (ignoring miller effect)
  - Mixed Rate, Multiple step sizes (partition)

II.3 Examples (HSIM)

Circuit Type (#MOS, #R,#C,#L)	Total Elements	Memory Usage	CPU Time (hrs)
Memory A (159M, 159M, 155M,0)	**473M**	**775MB**	**1.65**
Memory B (3.1M, 5.4M, 4.5M, 88)	**13M**	**195MB**	**0.69**
D/A (9K,65K,47K,0)	**121K**	**42MB**	**1.11**
PLL (2K, 8K, 23K, 0)	**51K**	**15MB**	**0.21**
Analog (119K, 175K, 232K,0)	**525K**	**111MB**	**0.37**

Courtesy of Nassda

II.4. Tasks

Device Mod. Convergence Input Patterns
Circuit Red. Event Driven Hierarchy Database
Matrix Solver Hierarchical Flow
Integration Partition

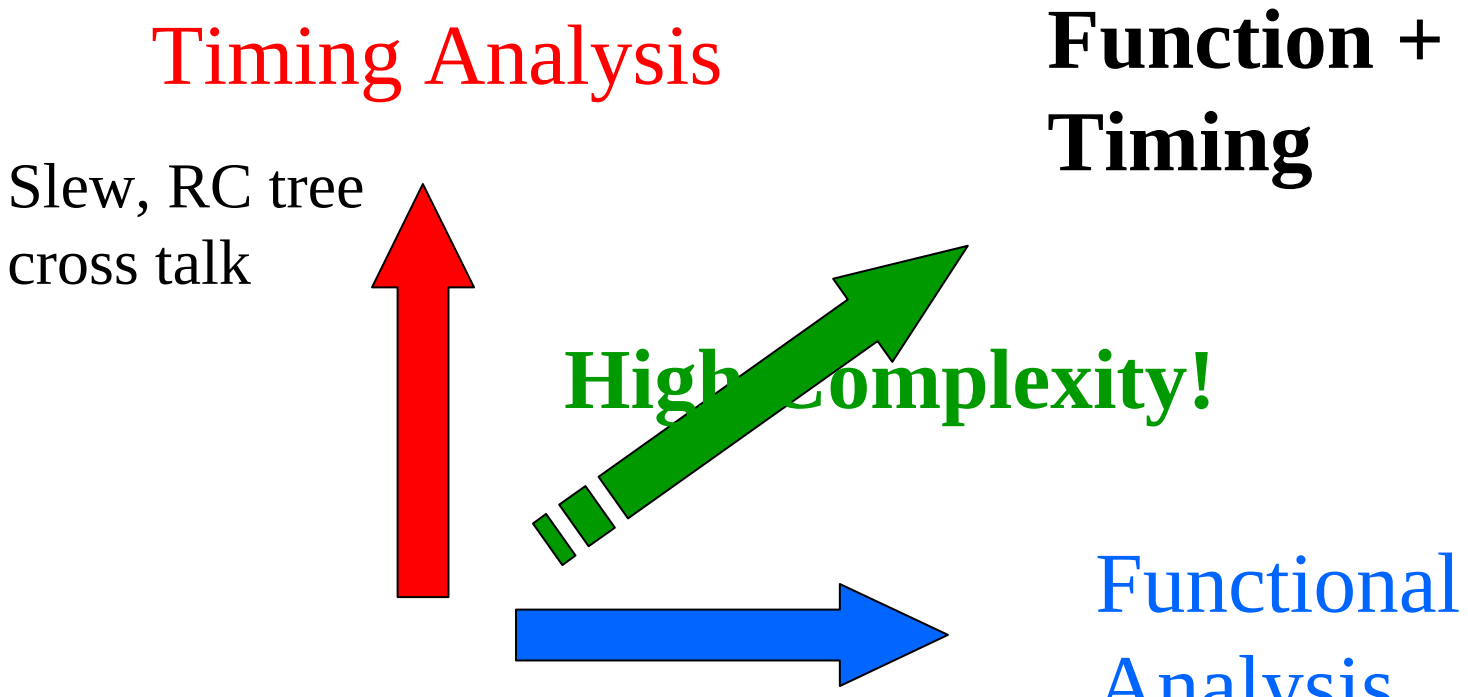
EE CS

Math

III. Logic Level Analysis

1. **Separation of Timing and Function**
2. **Static Timing Analysis**
   - **Algorithms, Gate Models, Path, Cross Talks**
3. **Functional Analysis**
   - Event Driven, Cycle Based
4. **Tasks**

III.1 Separation of Timing and Function



III.2 Static Timing Analysis

i. **Algor.: Shortest and Longest Paths Search**

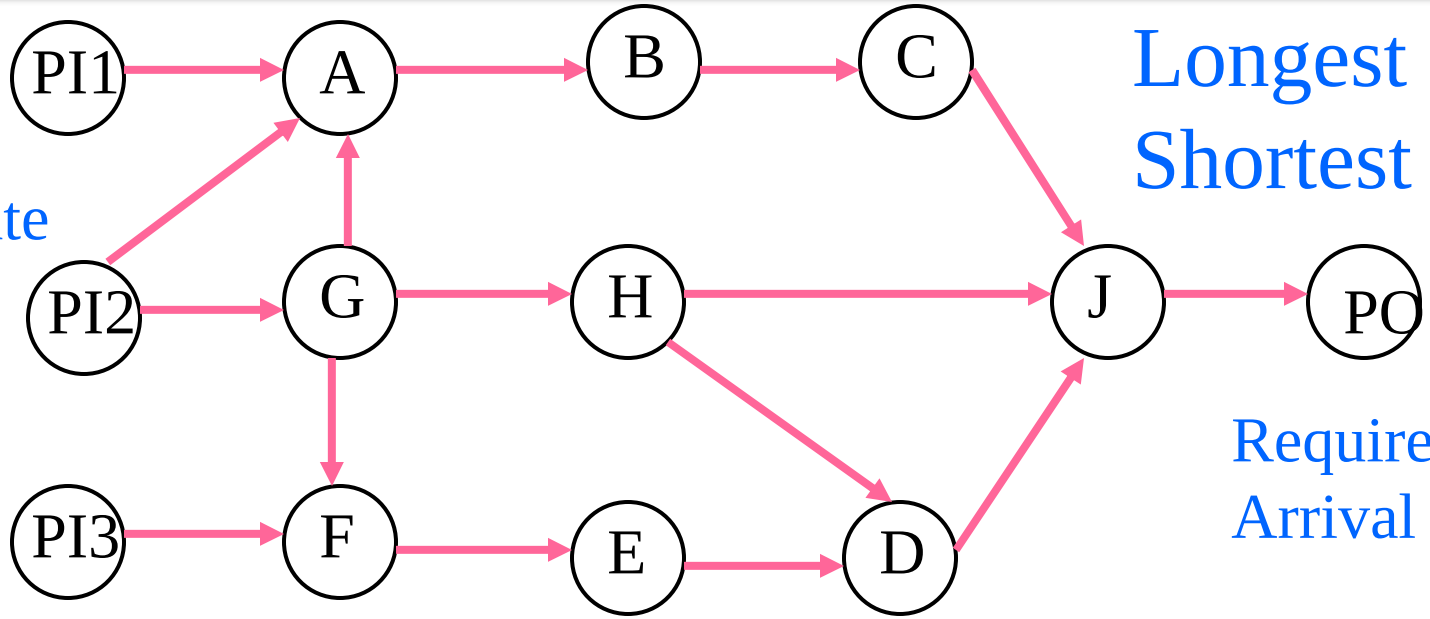
ii. **Gate Model:**
   - **Logic: Unate, Binate Signal Propagations**
   - **Timing: functions of Input Slope and Output Load**

iii. **Path Model:**
   - **Logic: False Path, Multiple Cycle Path, Cycles of Combinational Logic, Multiple Clock Frequencies**
   - **Timing: RC Tree**

iv. **Cross Talks: Timing Window, ATPG**

v. **Tasks**

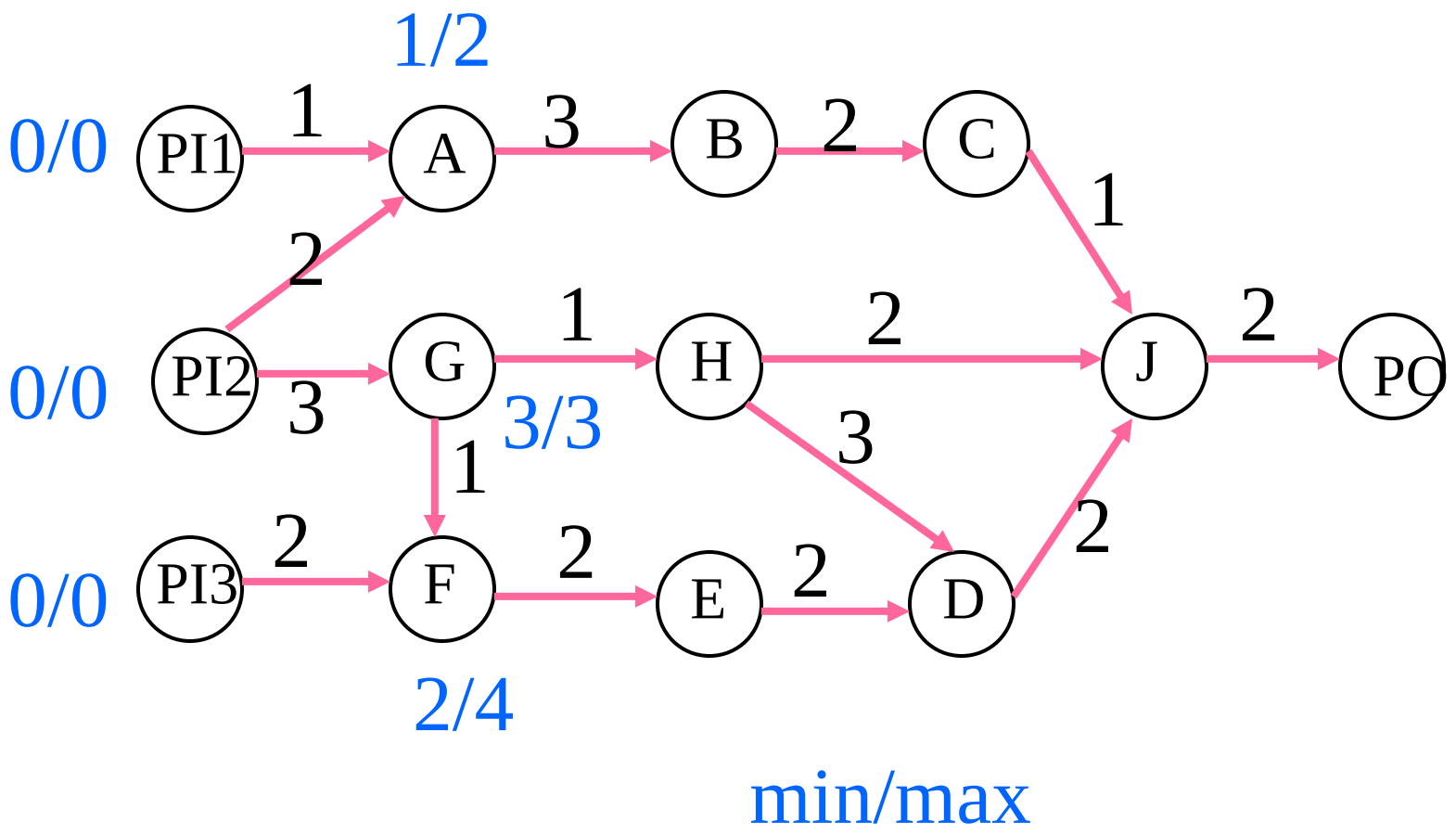
III.2.i Algor.: Path Search



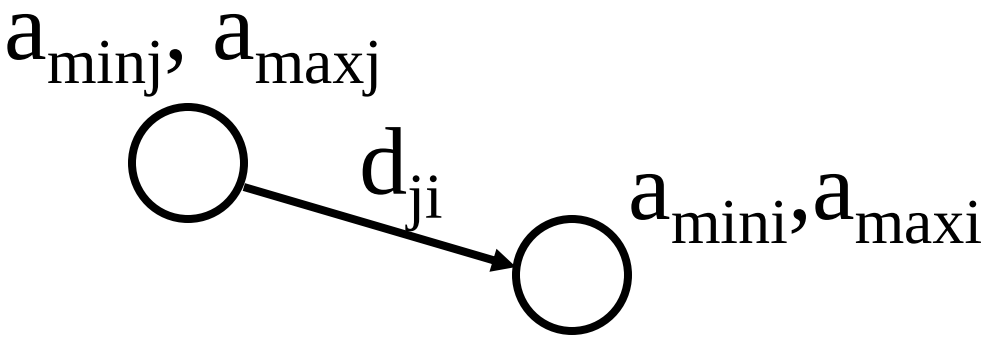
0->1 slew rate window 0->1 arrival time window
1->0 slew rate window 1->0 arrival time window

Static Timing Analysis: Worst Case Analysis, Independent of Input Patterns

III.2.I Algor: Path Search(cont)



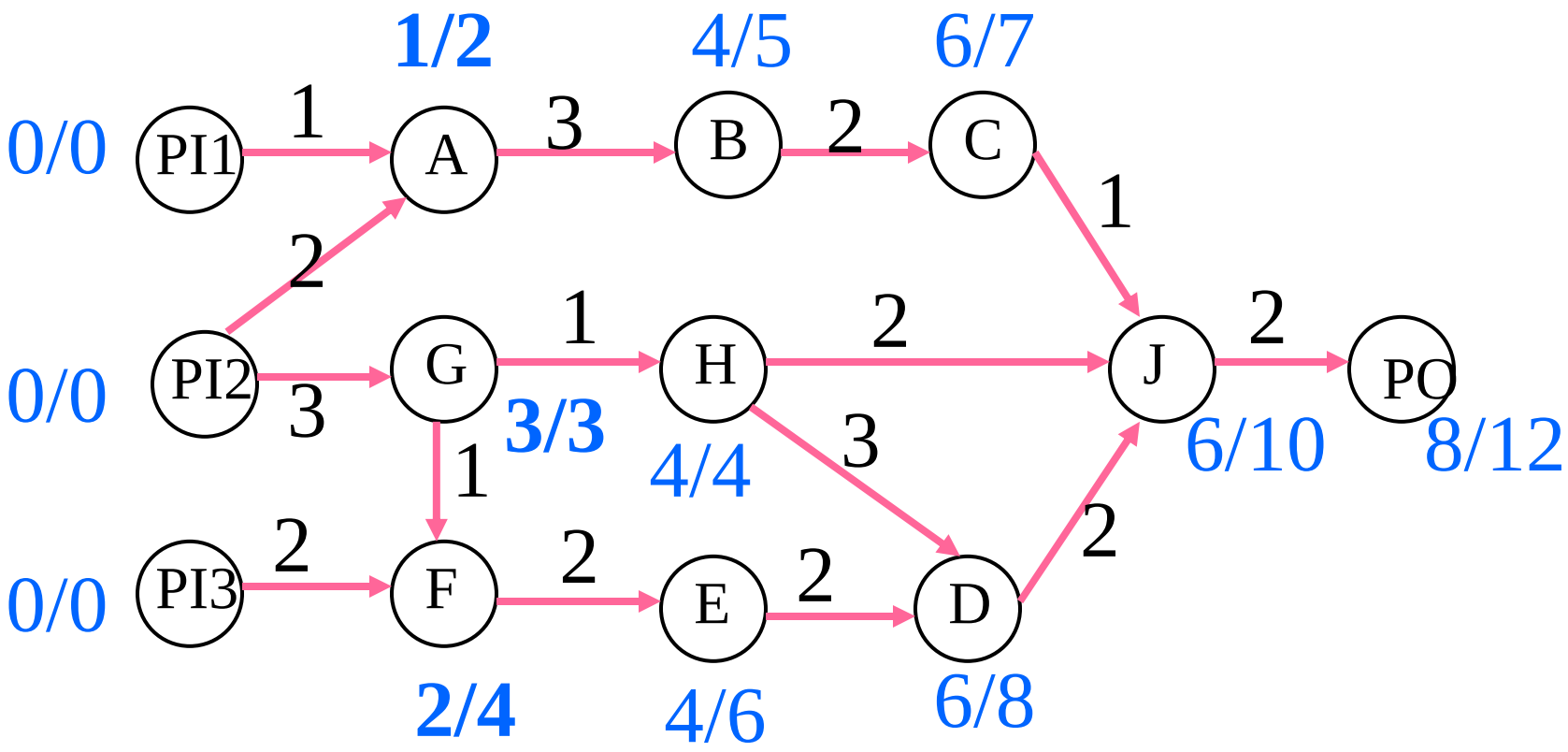
III.2.I Algor: Path Search(cont)



$$a_{mini} = \min_j a_{minj} + d_{ji}$$

$$a_{maxi} = \max_j a_{maxj} + d_{ji}$$

III.2i Algor.: Path Search

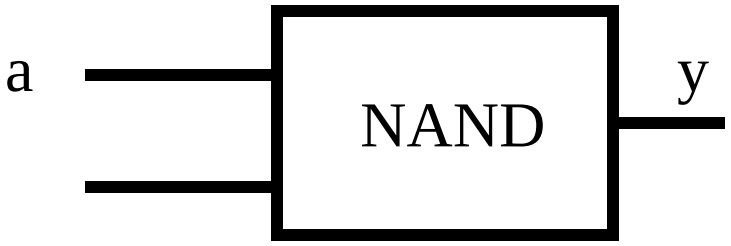


min/max

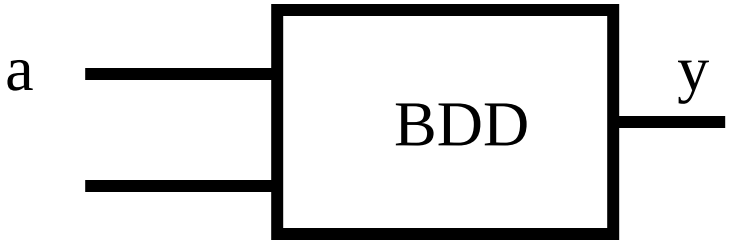
Longest: PI2,G,F,E,D,J,PO

Shortest: PI2,G,H,J,PO

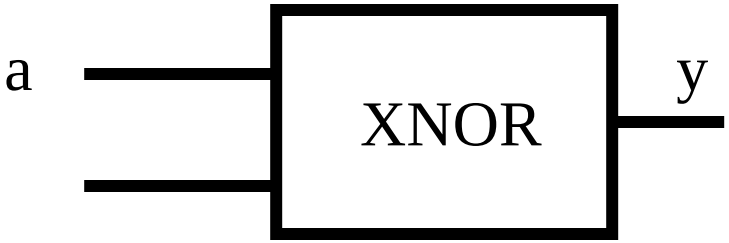
III.2.ii Gate Logic Model: Unate & Binate Signals



Unateness: a 0->1 => y 1->0

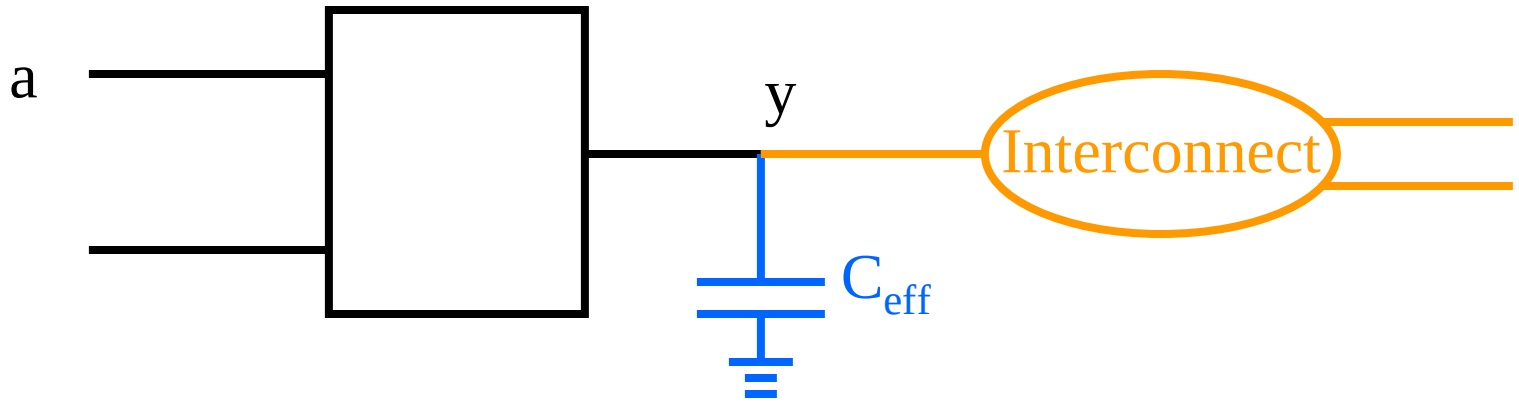


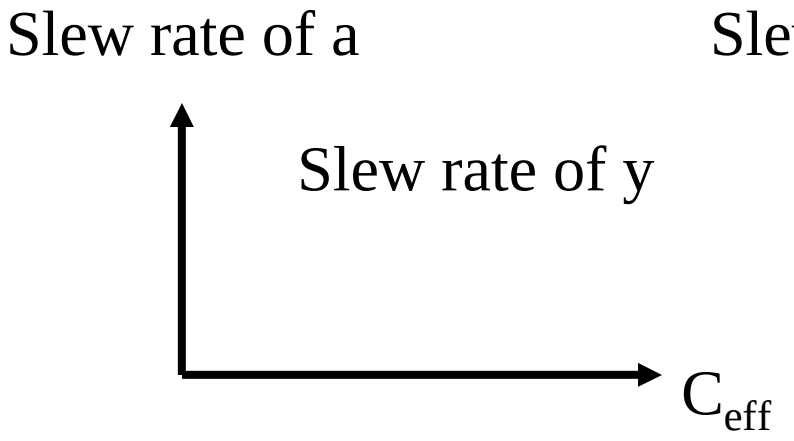
Check unateness based on BDD

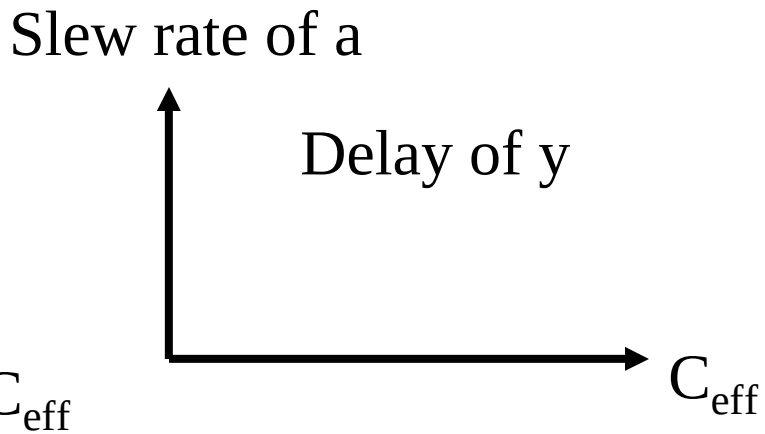


Binateness: a 0->1 => y 0->1 & 1->0

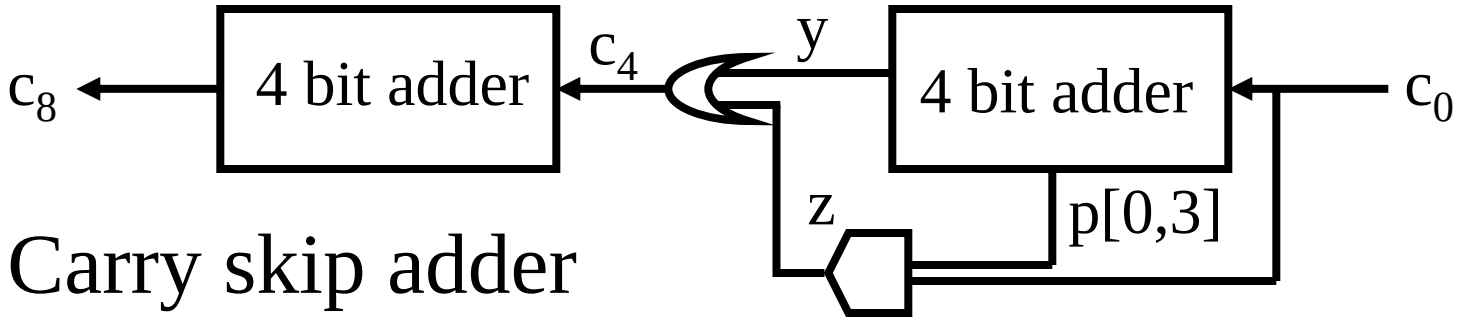
III.2.ii Gate Timing Model







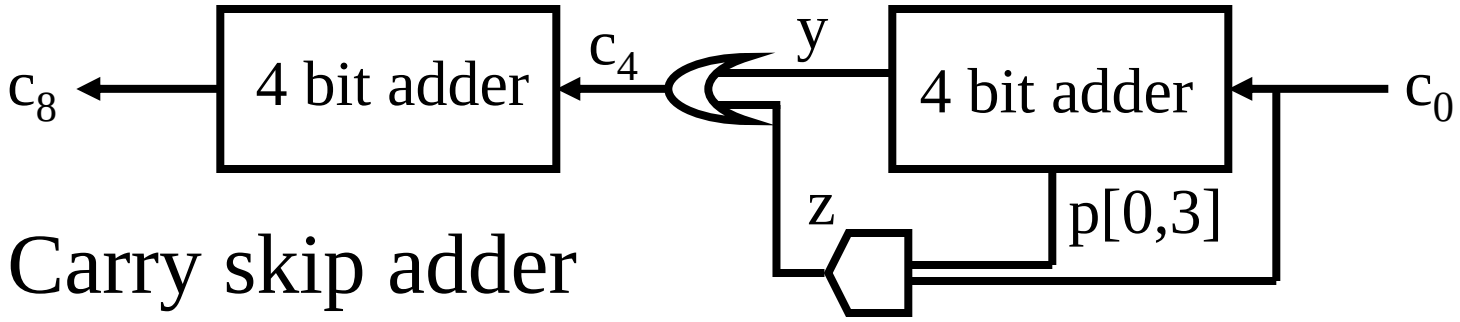
III.2.iii Path Logic Model: False Path



Carry skip adder

$$\begin{array}{rl} & 1 \quad C_0=1 \\ & 1011 \\ + & 0100 \\ \hline & 1111 \quad P[0:3]=1 \\ & 10000 \quad Z=1 \end{array}$$

III.2.iii Path Logic Model: False Path

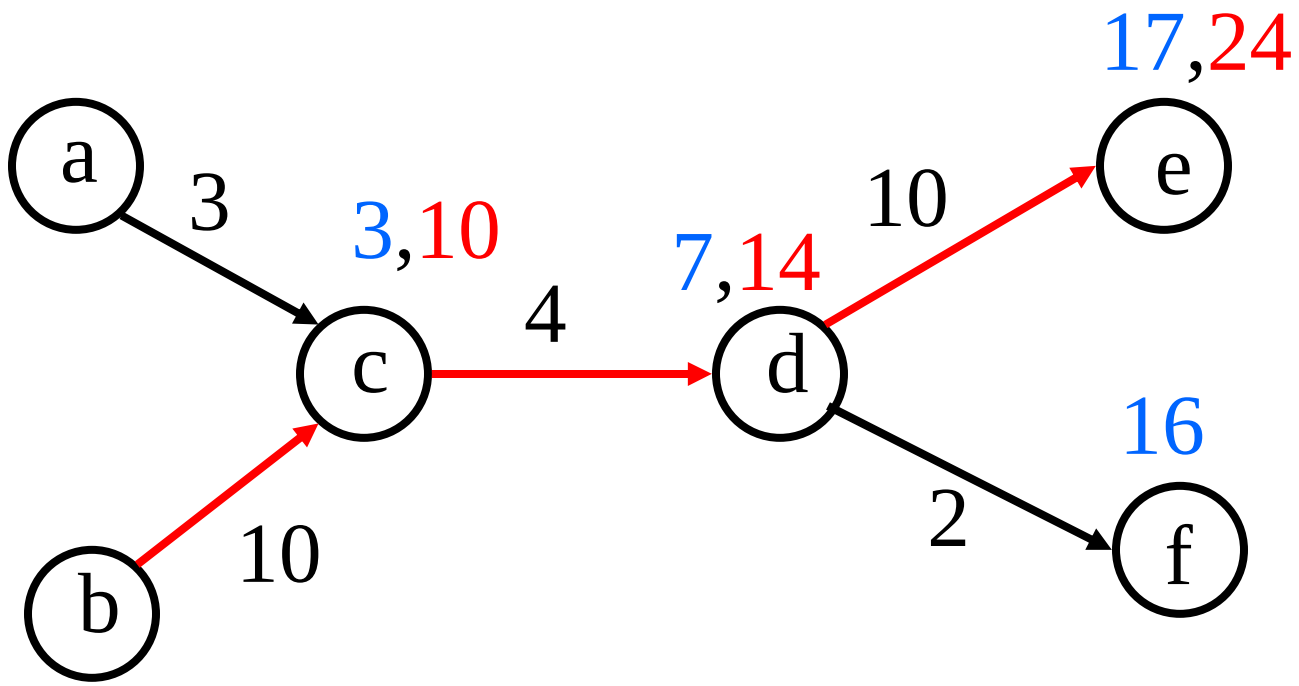


False path: c_0->y->c_4 ->c_8

Assumption: z->c_4 ->c_8 derives results faster

If we erase all false paths, we can identify the true critical paths and the corresponding input patterns

III.2.iii Path Logic Model: False Path

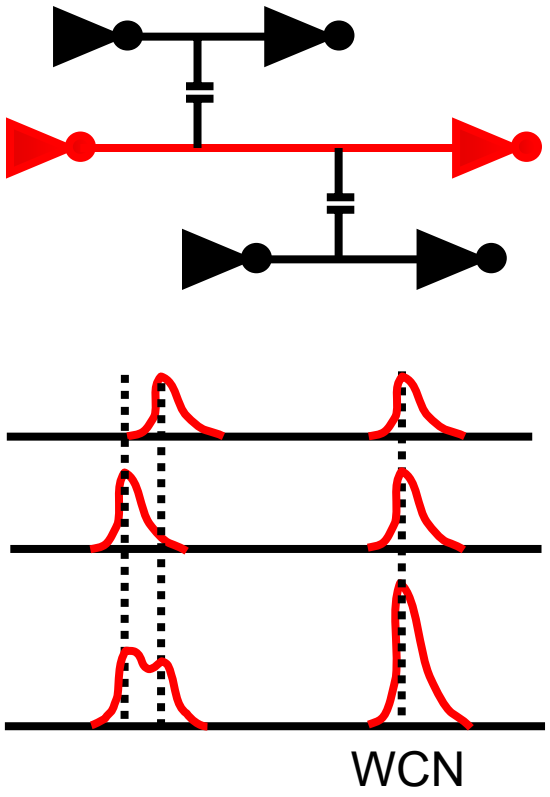


False path b->c->d->e

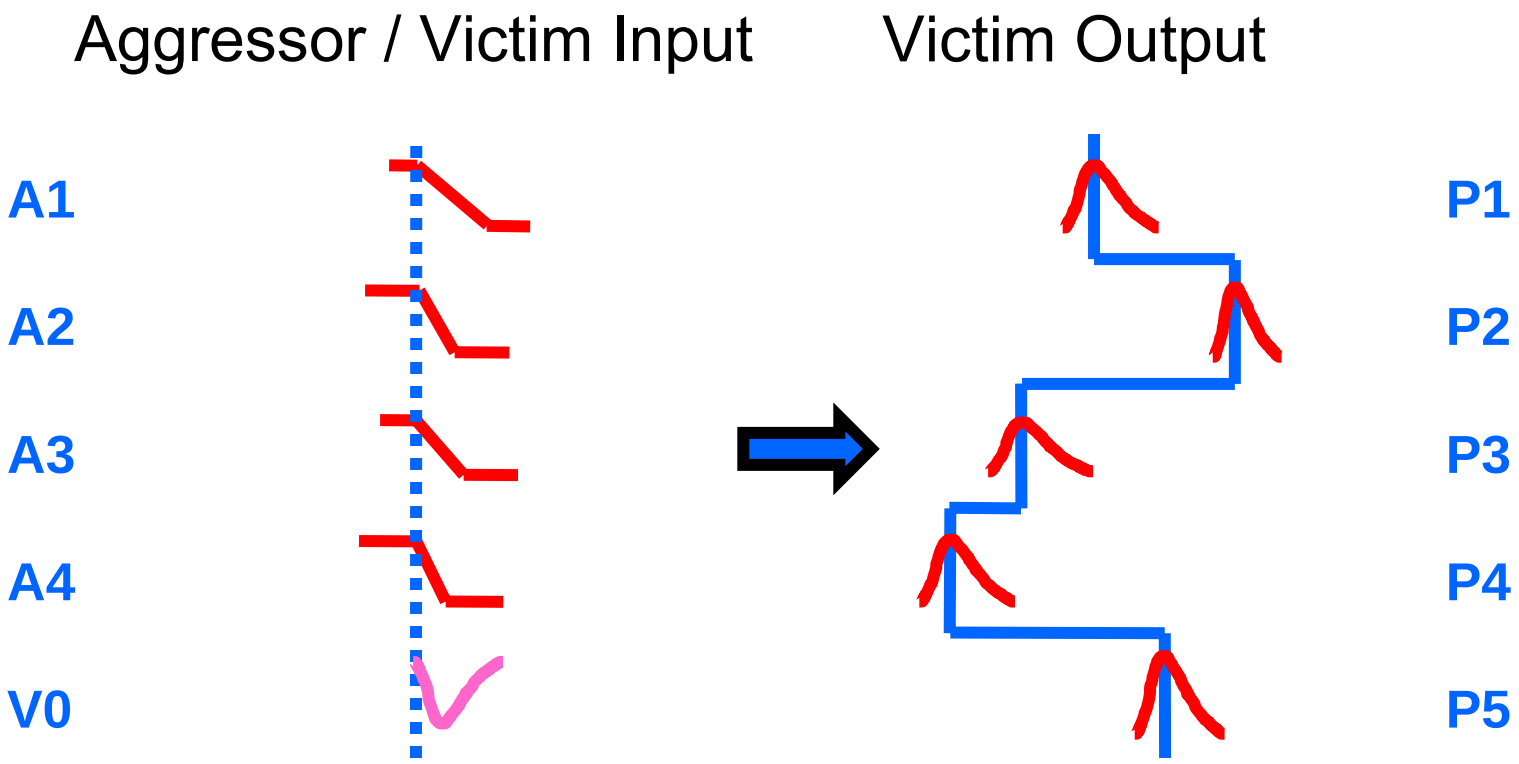
red+red=>red
red+blue=>blue
blue +blue=>blue

III.2.iv Cross Talk

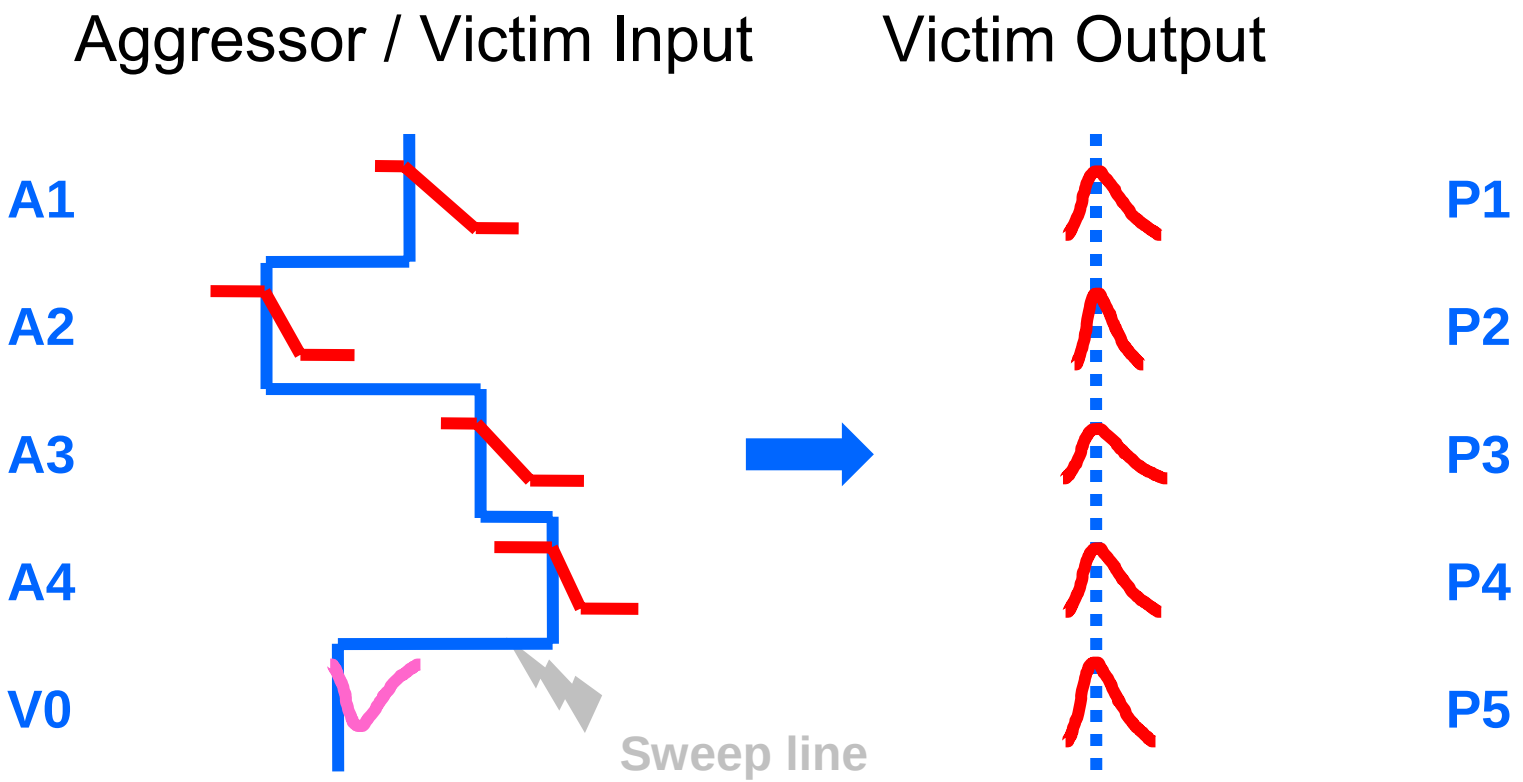
- WCN: worst-case noise: Delay & Glitch
  - Noise with maximum pulse height
    - Fixed circuit structure and parameters
    - Fixed transition time of input signals
    - Variable arrival time of input signals



III.2.iv Cross Talk: Timing Window

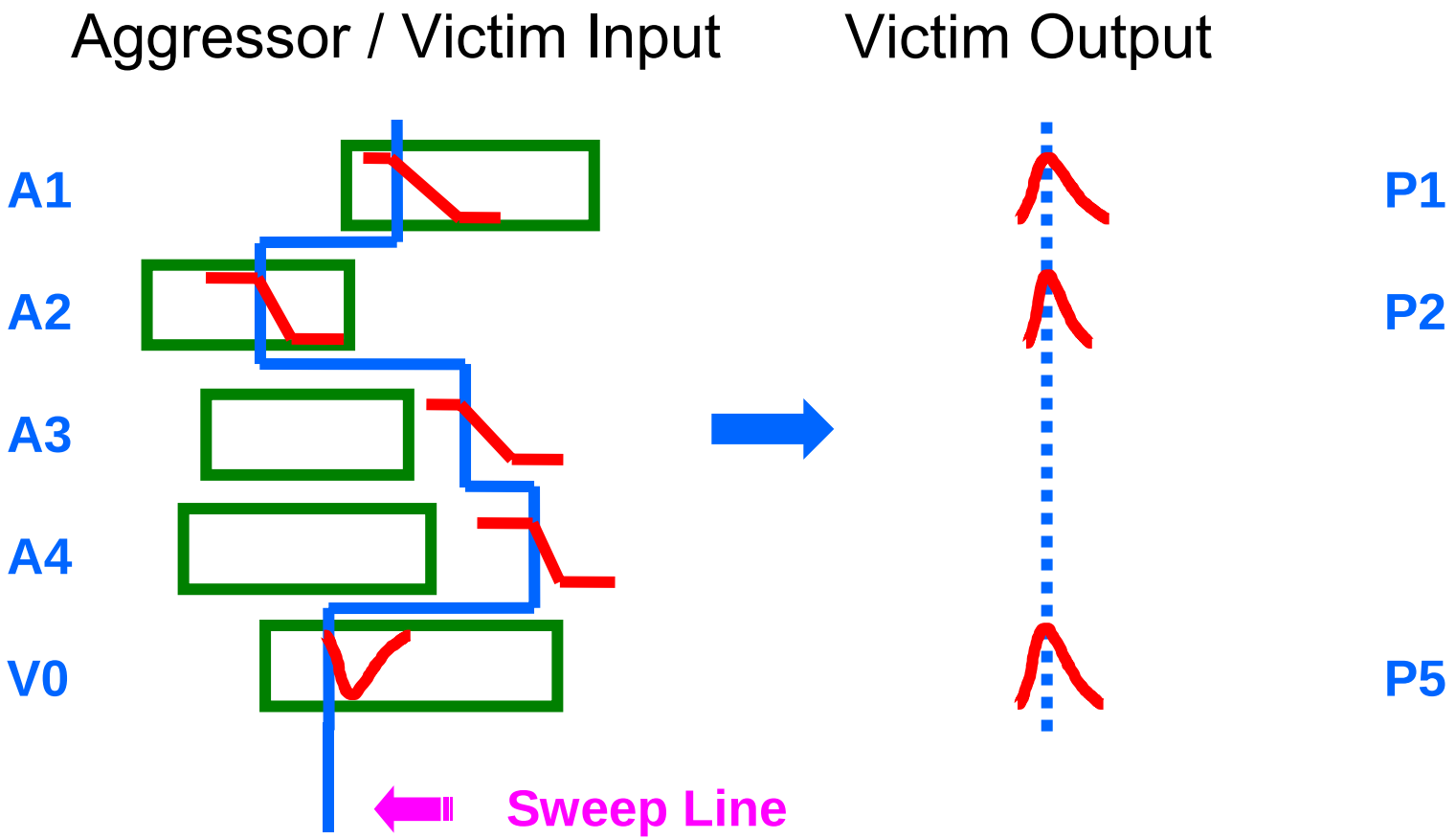


III.2.iv Cross Talk: Timing Window



Aggressor Alignment WITHOUT Timing Constraints

III.2.iv Cross Talk: Timing Window

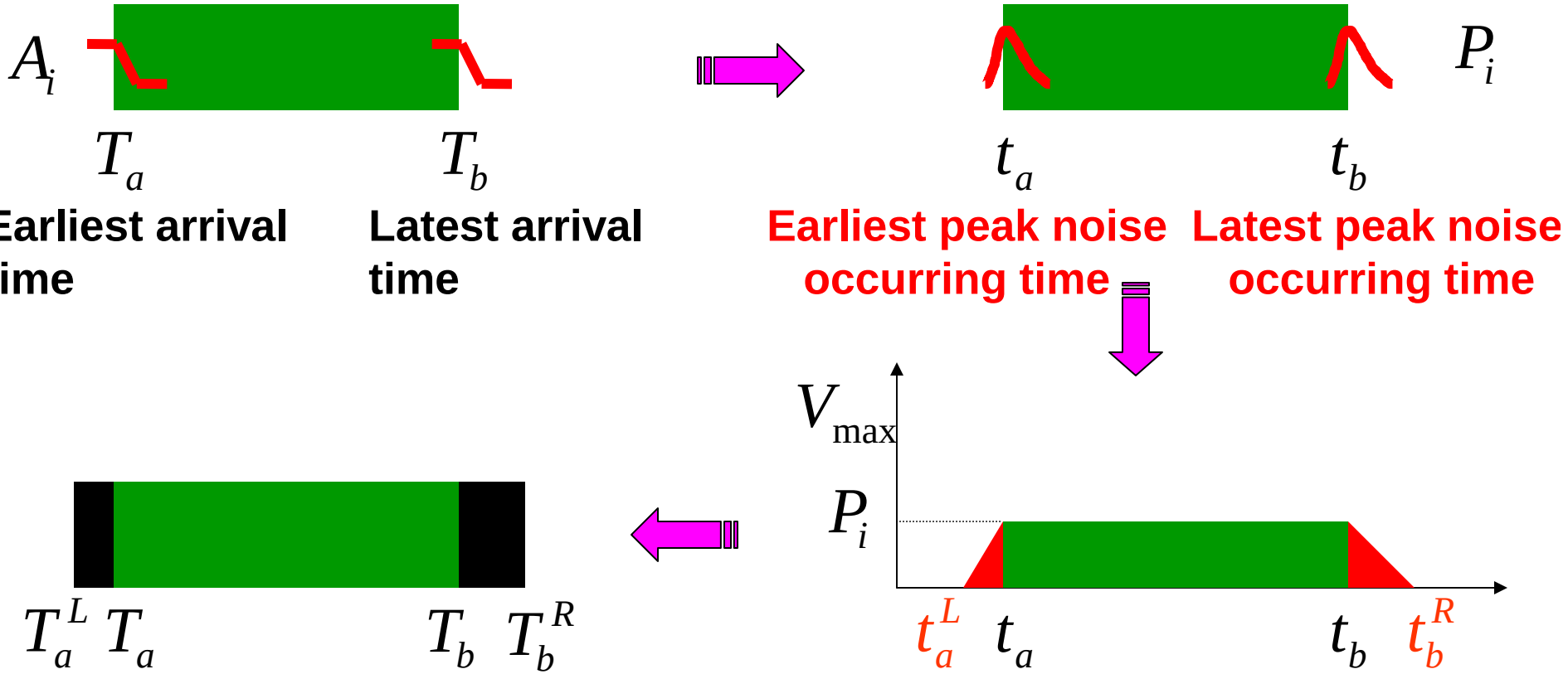


Aggressor Alignment WITH Timing Constraints

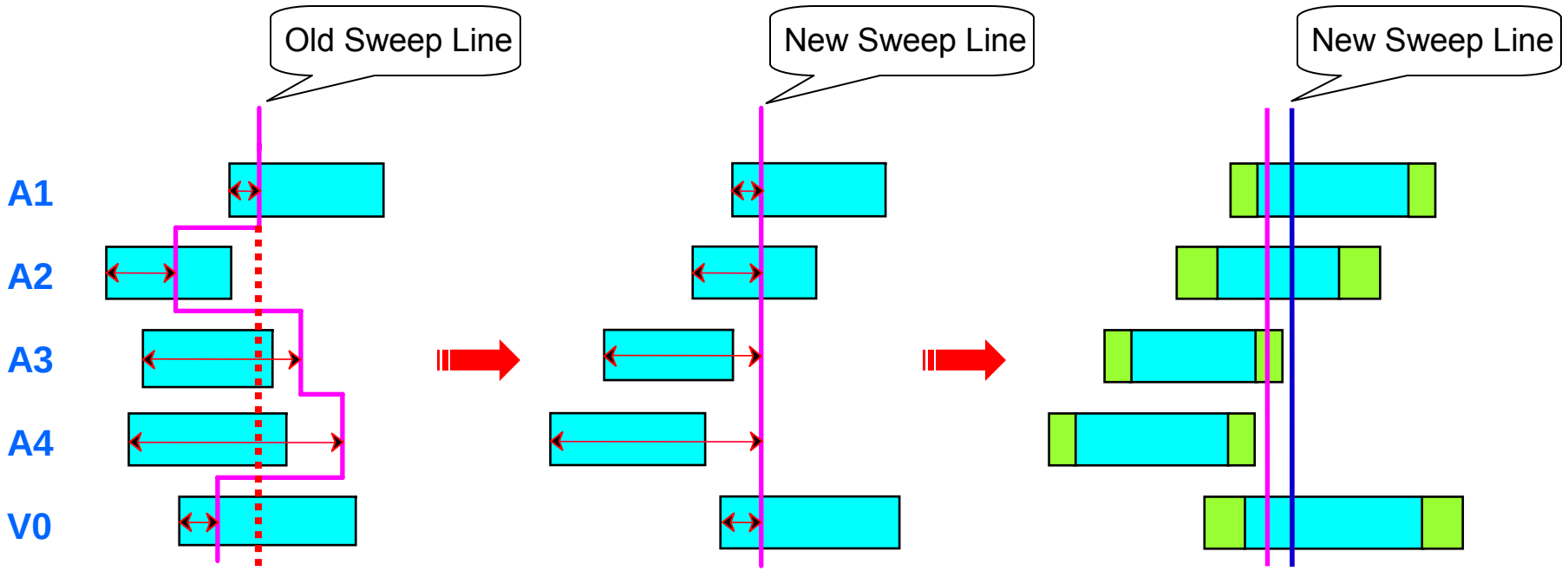
III.2.iv Cross Talk: Effective Timing Window

Timing window for aggressor input

Timing window for victim output



Aggressor Alignment with Timing Constraints -- Reformulation



(a) Original timing window (b) Shifted timing window (c) Expanded timing window

III.2.v Tasks

Gate model: power, noise

Path model: special cases

Path model: RCLK reduction

Path search in hierarchy

Cross talk

ATPG

Timing window+pattern

EE

Speed

Accuracy

CS

Math

III.3 Logic Level: Functional Analysis

i. **Functional Analysis Techniques**
ii. **Event Driven Analysis**
iii. **Cycle Based Analysis**
iv. **Tasks**

III.3.i Functional Analysis Techniques

- Event Driven Simulation
  - VCS, Verilog-XL, VSS, ModelSim
- Cycle Based Simulation
  - Frontline, Speedsim, Cyclone
- Domain Specific Simulation
  - SPW, COSSAP

III.3.ii Event Driven Analysis

- **Event Wheel**
  - **Maintains schedules of events**
  - **Enables sub-cycle timing**
- **Advantages**
  - **Timing accuracy**
  - **Good Debug Capability**
  - **Handles asynchronous**
- **Disadvantages**
  - **Performance**

III.3.iii Cycle Based Analysis

- RTL Description
- All gates evaluated every cycle
- Schedule is determined at compile time
- No timing
- No asynchronous feedback, latches
- Regression Phase
- High Performance
- High Capacity

III.3.iv Tasks

Dynamic timing model

Hardware acceleration

Pattern generation

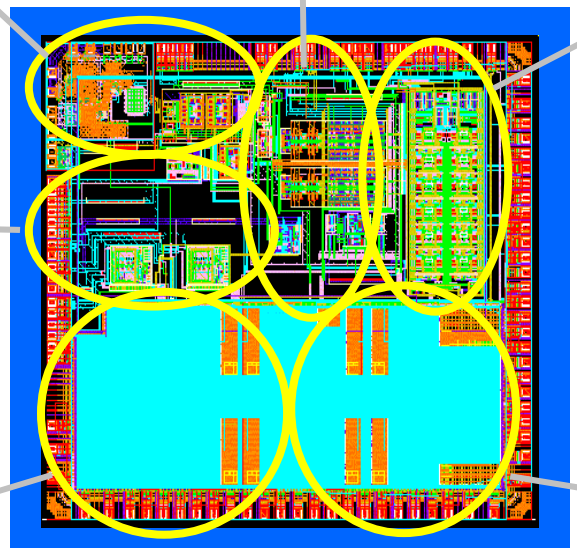
coverage

EE

CS

Math

IV. Mixed Signal Analysis



RF front-end

RF Simulator

Custom Logic & Mixed-Signal

Fast SPICE

Complex

Analog

Traditional

SPICE

Analog IP

VHDL-AMS

Verilog-AMS

DSP

HDL

VHDL/Verilog

Embedded

Memories

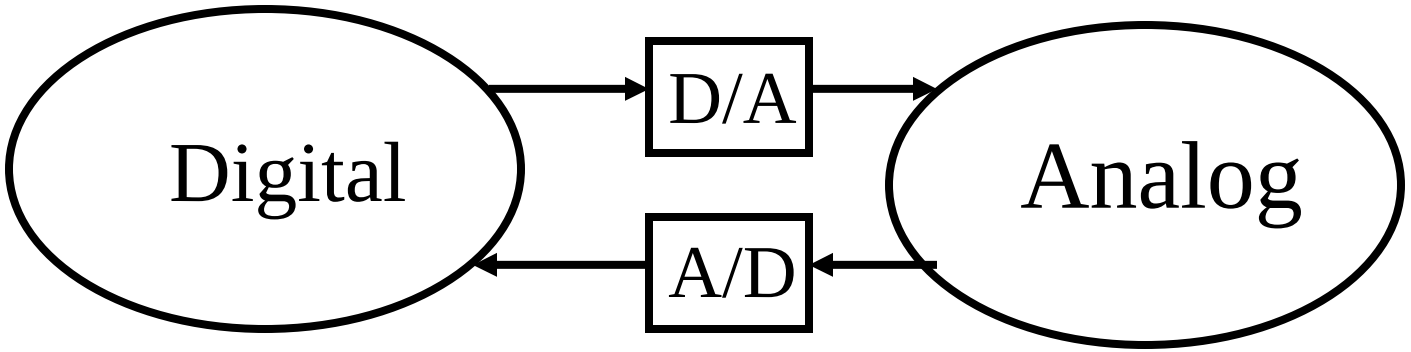
Hierarchical

Fast SPICE

Single-Kernel simulator for full-chip SoC Verification

Courtesy of Mentor

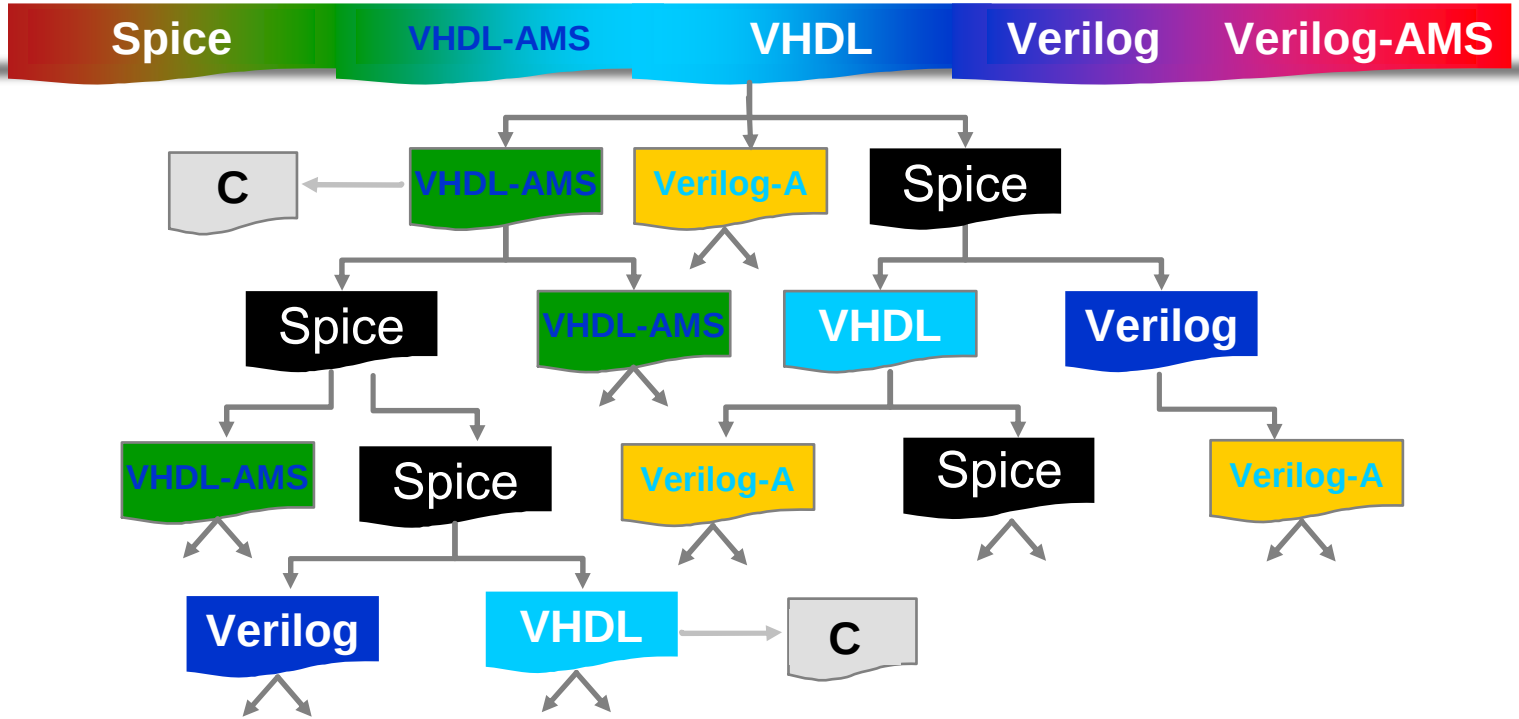
IV. Mixed Signal Analysis: Interface



Analog Signal — Threshold Detector — 0, 1, X

Rise, Fall Time
Rise, Fall Resistance

Mixed Signal: Mixed Languages



- **Single Kernel Architecture**
- **Single Netlist Hierarchy**
- **Automatic D/A and A/D converter insertion**

Courtesy of Mentor

IV. Tasks

RF, Analog,

Power, Noise,

Convergence

Interface

Partition

Language

Compiler

EE

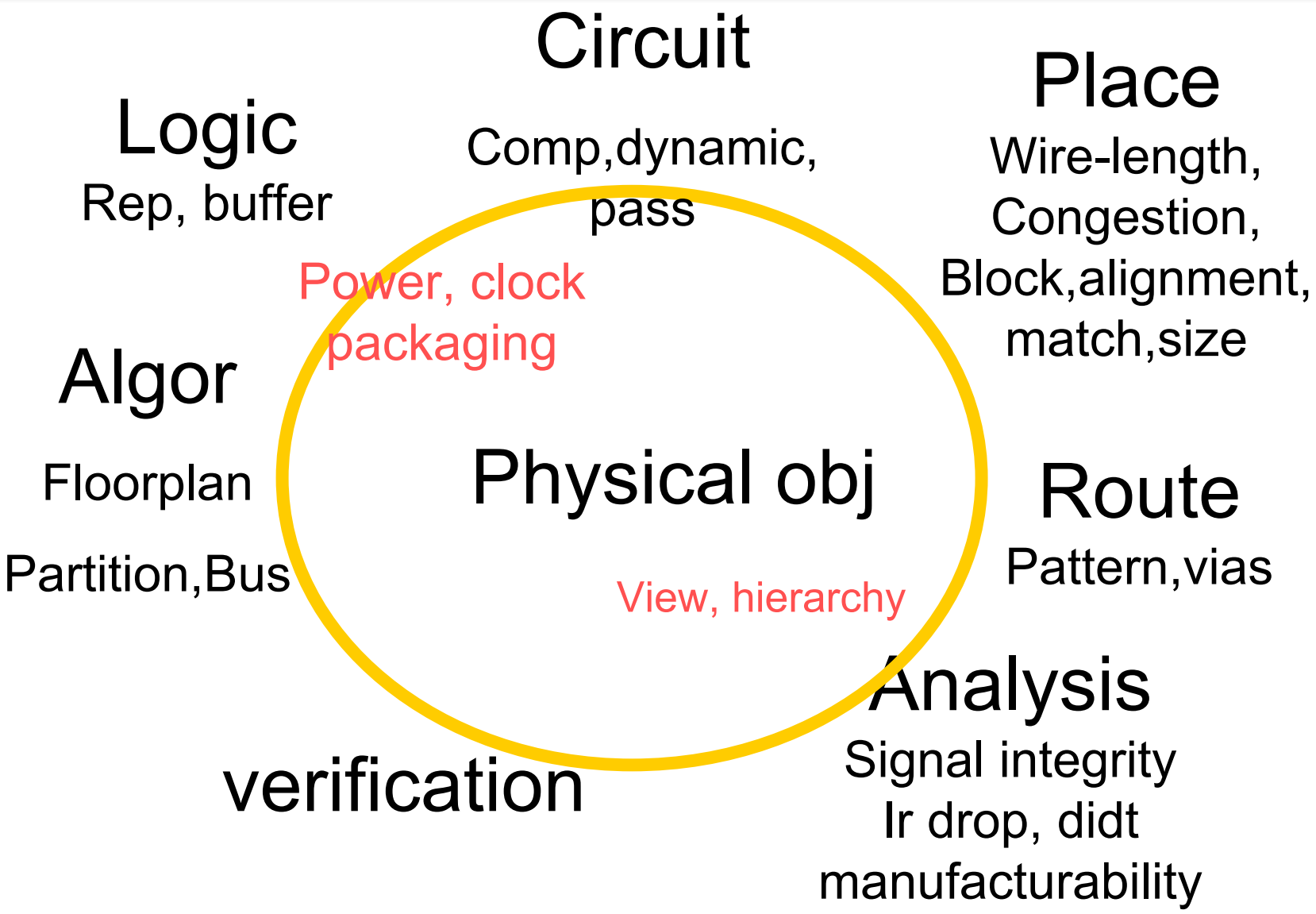
CS

Math

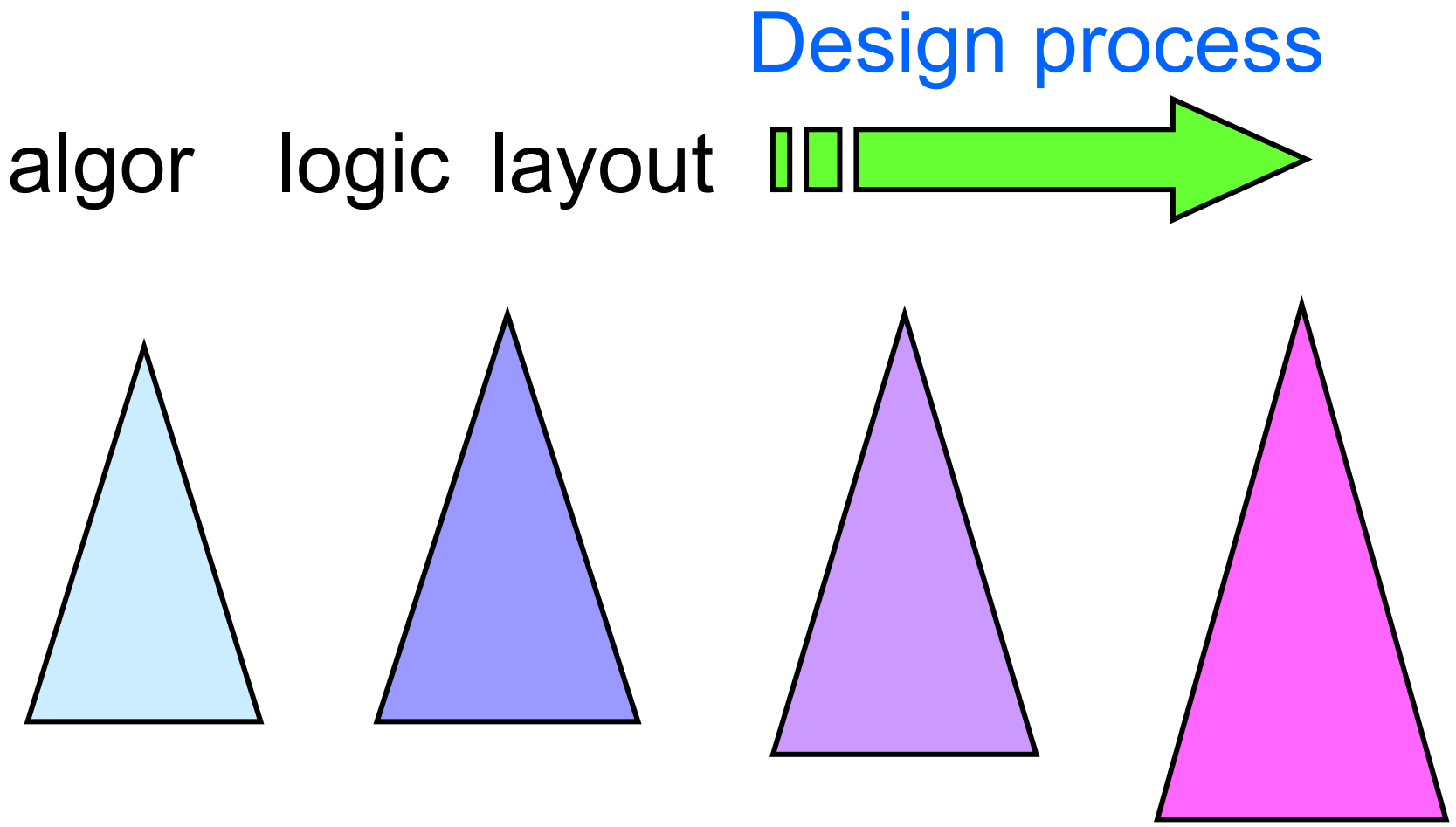
IV. Research Directions

- **Hierarchy Management**
- **Analysis + Optimization**
- **Layout Oriented Analysis**
- **Circuit Reduction**
- **Spice**

Hierarchy Management



Hierarchy management



Hierarchy Management (cont.)

- Hierarchy Tree Construction
- Hierarchy Tree Transformation
- Incremental Changes
- Graph Process on Tree Structure

Analysis and Optimization

i. Circuit Reduction
ii. Transient Analysis
iii. Optimization of
   - power/ground: pads, decoup caps, network
   - clock networks: topology, shield, decoup caps
   - Buses: shield, topology

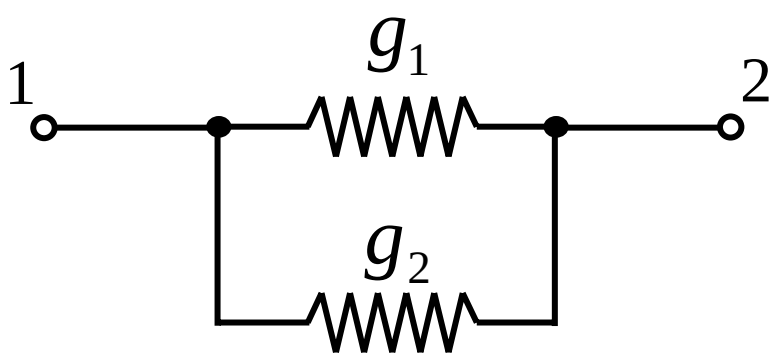
Layout Oriented Analysis

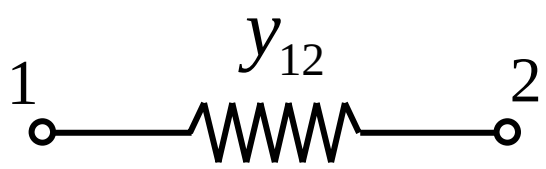
- Huge Circuitry
  - Millions of nodes
- Whole Chip Analysis
  - Power/Ground, Substrate, Analog
- Guaranteed Accuracy
  - Accuracy vs Execution Time
- Construction or Incremental Changes

Layout Based Signal Analysis

- Generalized Y-Delta Transformation
  - R,C,L,Coupling, Sources
- Natural Frequency
- Realizability
- Hierarchical Circuit Analysis

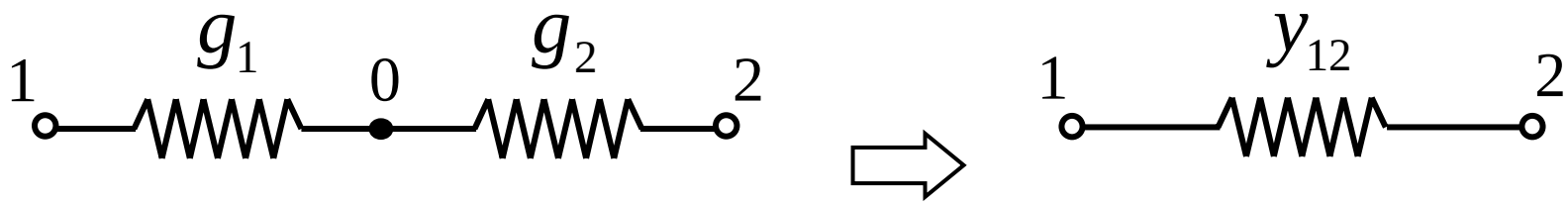
Conductance in parallel





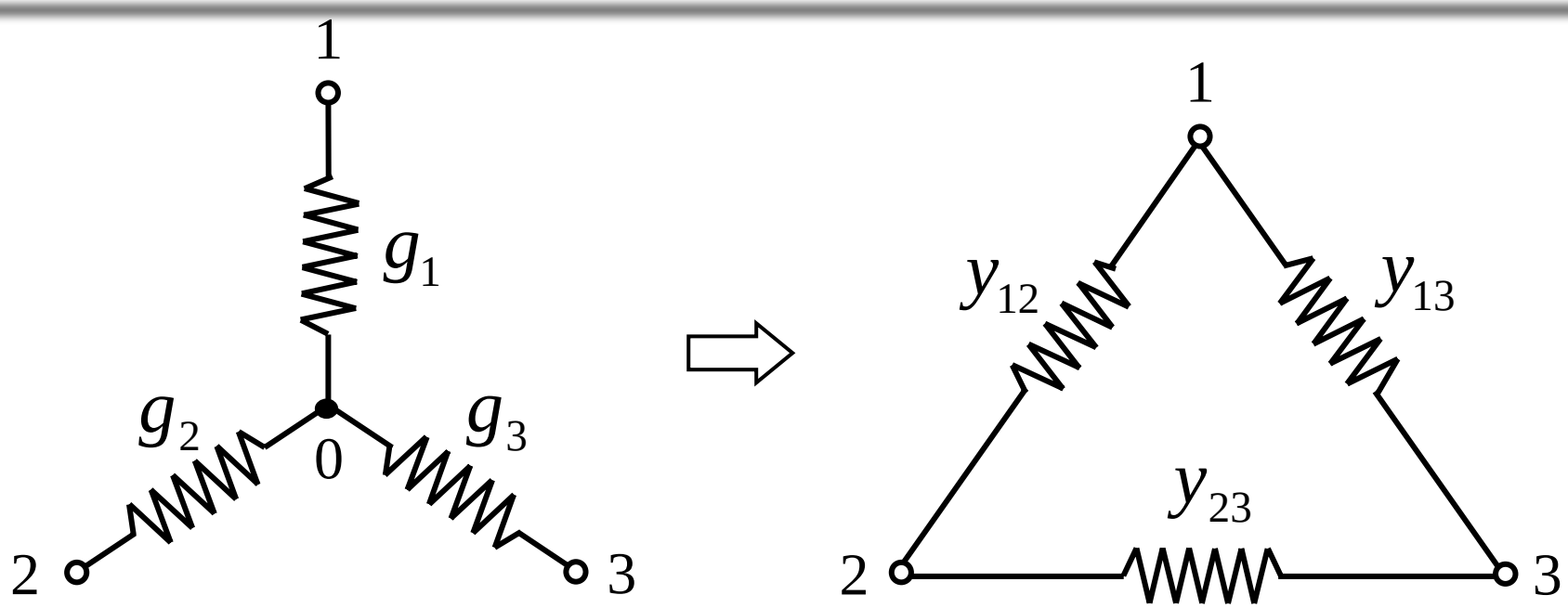
$$y_{12} = g_1 + g_2$$

Conductance in series



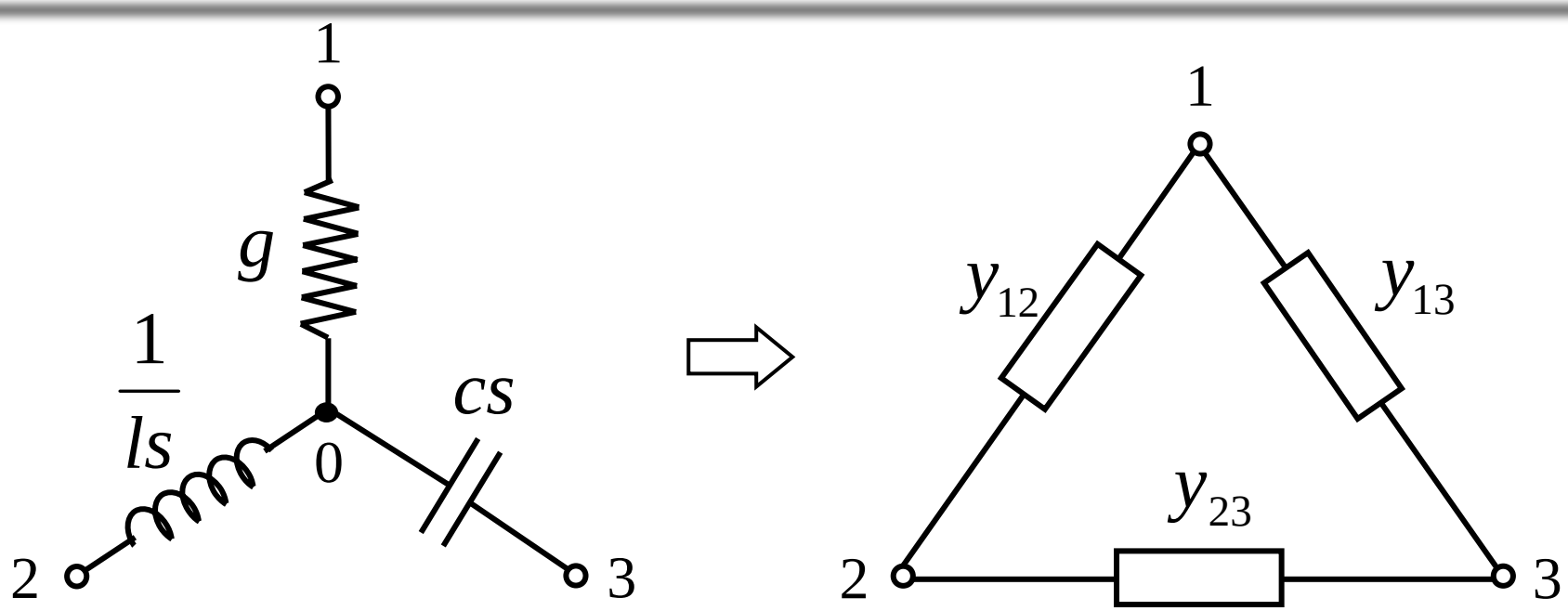
$$y_{12} = \frac{g_1 \cdot g_2}{g_1 + g_2}$$

Conductance in Y-structure



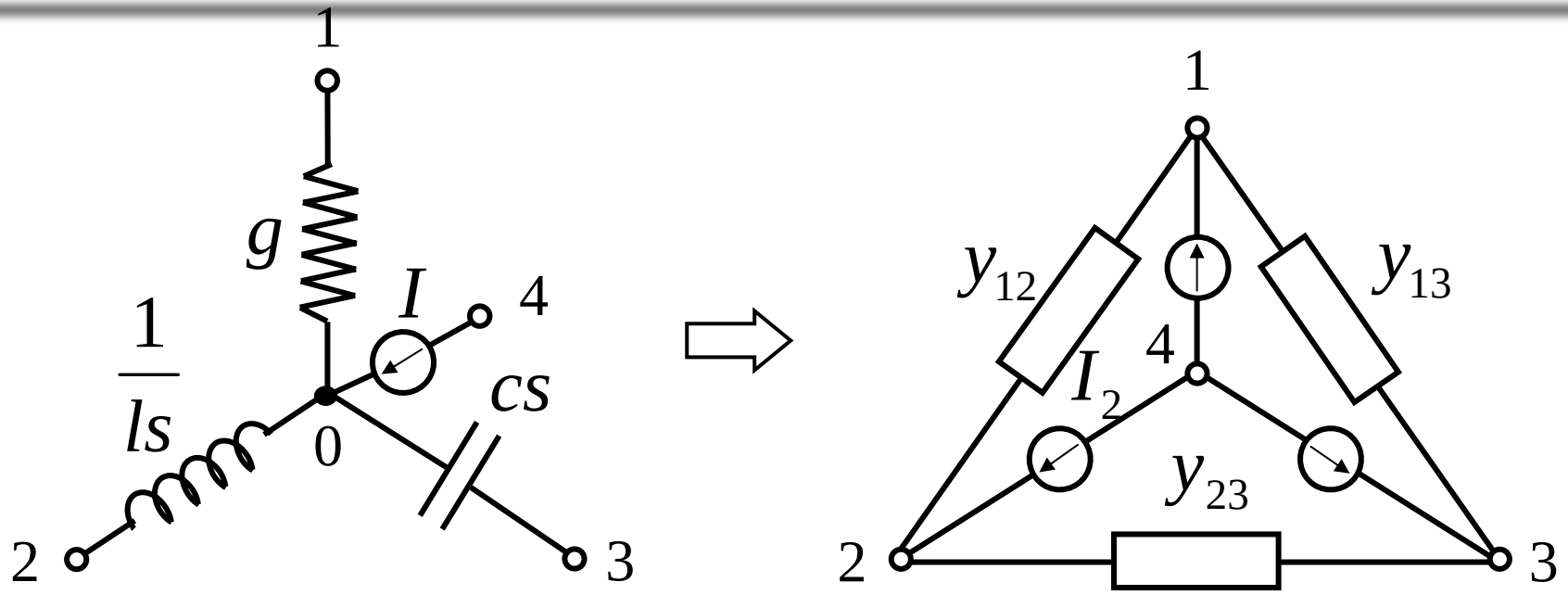
$$y_{ij} = \frac{g_i \cdot g_j}{g_1 + g_2 + g_3}$$

Admittance in Y-structure



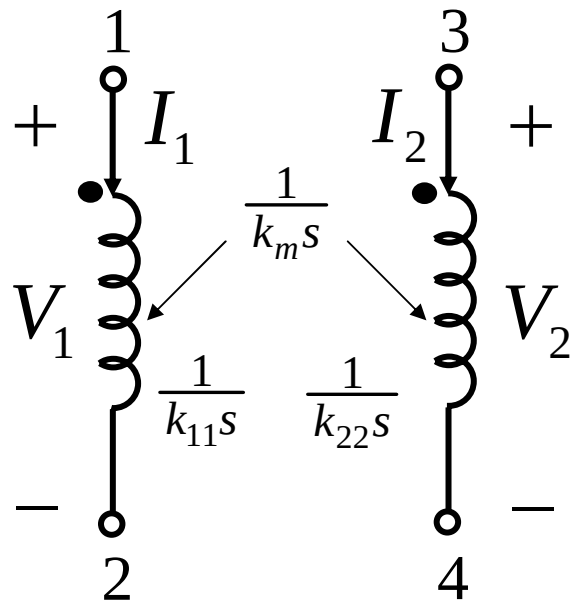
e.g. $$y_{12} = \frac{g \cdot \frac{1}{ls}}{g + \frac{1}{ls} + cs} = \frac{g}{1 + gls + cls^2}$$

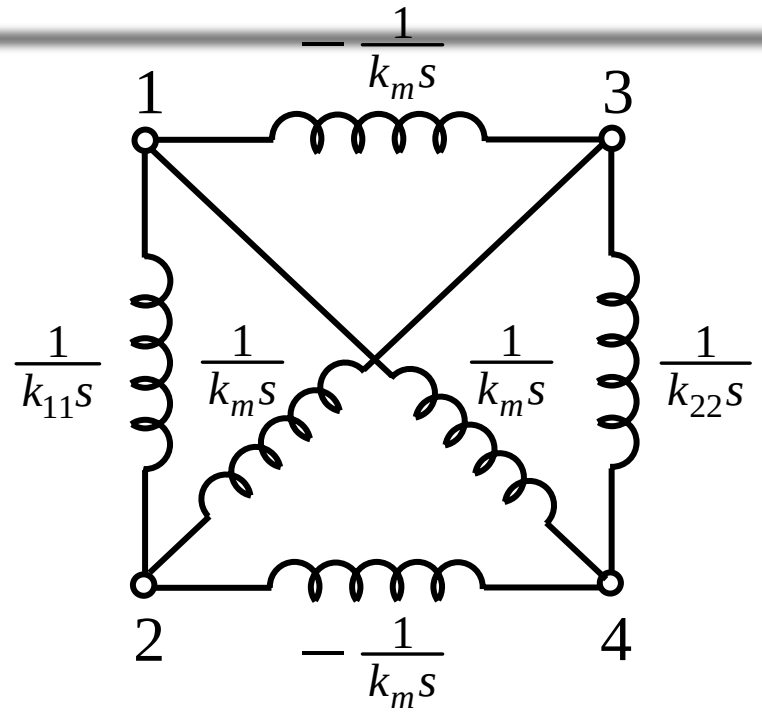
Admittance in Y-structure, with current source



y_{12} is the same , and $$I_2 = \frac{\frac{1}{ls} \cdot I}{g + \frac{1}{ls} + cs} = \frac{I}{1 + gls + cls^2}$$

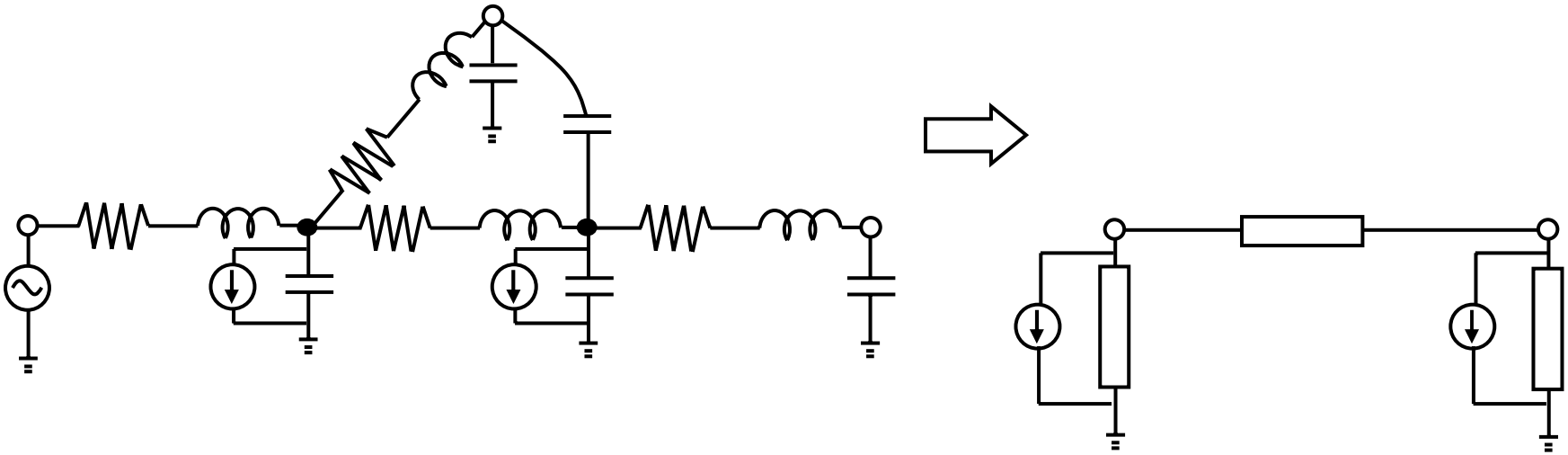
K-element



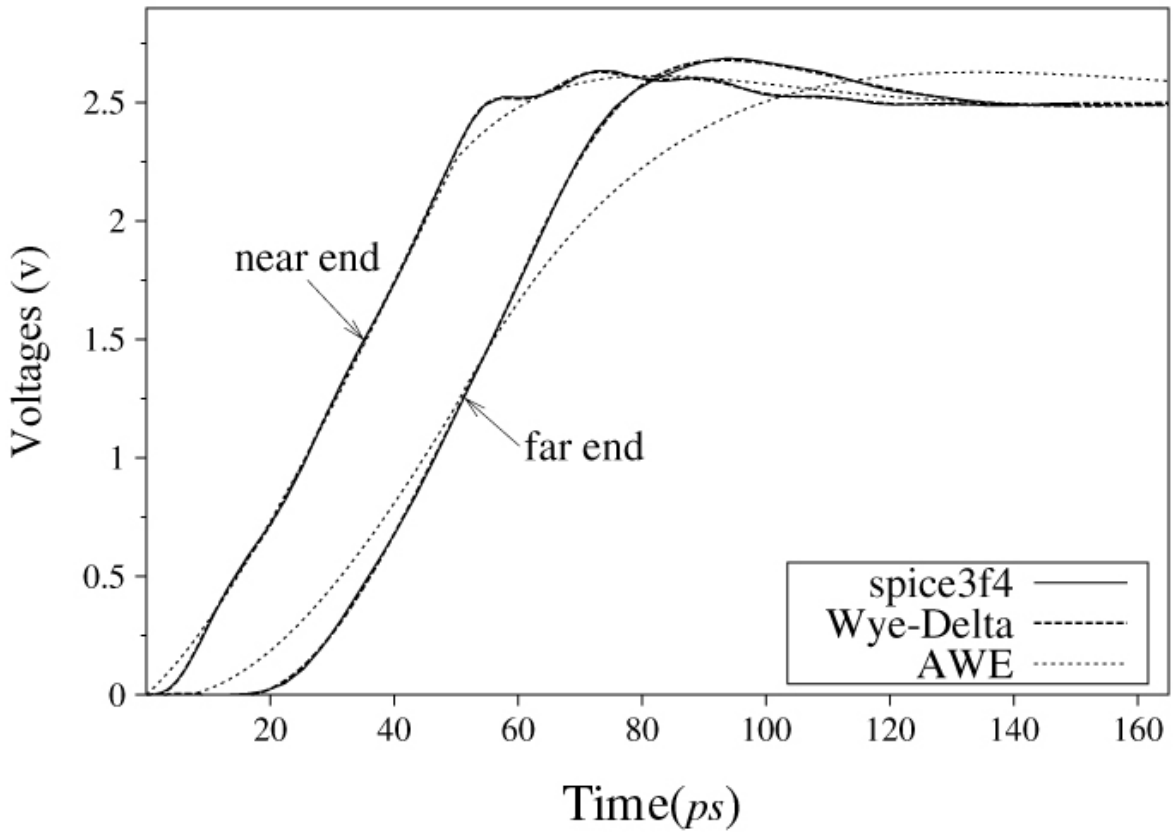


$$\begin{cases} \frac{1}{k_{11}s}V_1 + \frac{1}{k_m s}V_2 = I_1 \\ \frac{1}{k_m s}V_1 + \frac{1}{k_{22}s}V_2 = I_2 \end{cases}$$

Reduction example



Waveform Estimation

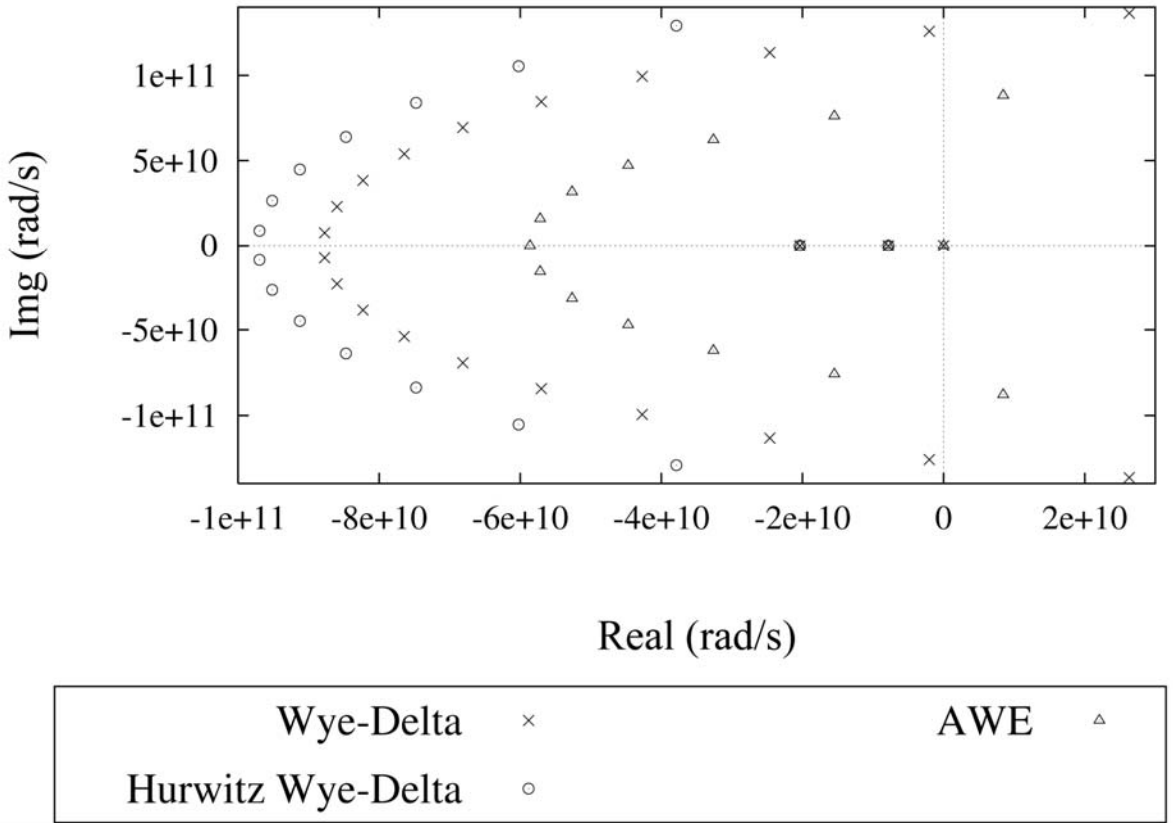


Transient response evaluated using Y-Δ transformation with Hurwitz polynomial approximation.

8th order stabilized Y-Δ models are used for near-end and far-end node waveform evaluation.

Only a 3rd order AWE model is obtained.

Pole Analysis



Both AWE and Y-Δ transformation have artificial *positive* poles;

High order AWE tends to collapse approximate poles, hiding other less dominant ones.

Y-Δ transformation with model stabilization yields no positive poles, and has broader band in pole estimation.

V. Conclusion

- Layout Oriented Analysis
- Unified tools combining EE and CS with Math as foundation
- New Methodologies
  - Larger Circuits, Shorter Product Turnaround

References

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