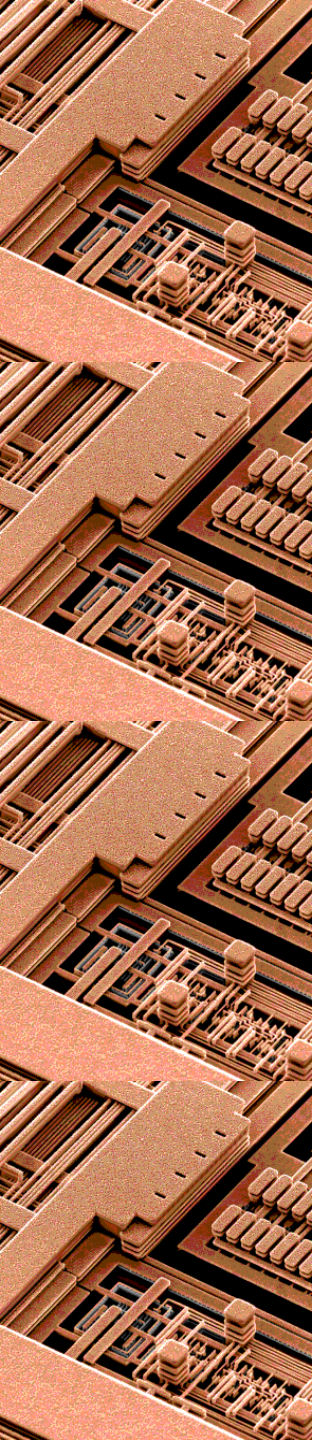

Toward Full-Chip Analysis with EM Accuracy:

Current State of the Art, Needs & Future Challenges

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CCEM

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ITRS 2001

PRODUCT YEAR	*2003*	*2005*	*2007*	*2010*	*2013*
TECHNOLOGY GENERATIONS (nm)	107	80	65	50	35
CHIP SIZE (mm^2)					
Hand-held	61	65	65	81	90
Performance	310	310	310	310	310
PACKAGE PIN COUNT					
Hand-held (max)	508	616	748	972	1264
Performance (max)	2057	2489	3012	4009	5335
PERFORMANCE (GHz)					
On-chip, Hand-held	0.5 - 3.2	0.6- 3.9	0.7- 4.7	0.9- 6.0	1.2 - 8.0
On-chip, Performance	3.09	5.17	6.74	12.0	19.0
Chip-to-board, fast buses	~2.0	~2.5	~3.0	~4.0	~5.4

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Forecasting the Challenge...

"With finer feature sizes and increasing signal speeds, the electrical interactions of integrated circuit interconnect, which is both local and global in nature, are the biggest integrated circuit design challenge of today and tomorrow. And hierarchy does not appear to be the answer.

The electric fields that couple integrated circuit interconnect cannot so easily partitioned and dealt with hierarchically as schematics and geometry. Hence, the call for post-layout performance verification which would entail the solution of Maxwell's equations across the entire chip.

Such a solution would be prohibitive expensive, even if possible.

(But that observation does not keep many who should know better from demanding it!)"

Ronald Rohrer, "A Brief History of the Future of Semiconductor Electronic Design Automation," CAD Plenary Talk, 1997 IEEE International Conference on Computer Design (ICCD '97)

Acknowledging the Need…

"Series-RL coupling through the power supply grid is a very troubling problem. It virtually never happened at 0.25-micron. Maybe we saw one or two instances at 0.18-micron. But now in 0.13-micron designs, it's not unusual to have tens or hundreds of nets impacted by this mechanism on a single design.

Growing use of clock and power supply gating techniques as part of aggressive power management strategies…[lead to] powerful transients on the supply grid all the way back to the package pins.

These powerful transients make accurate RLC modeling of the supply grid, lead frame and even the environment on the circuit board absolutely essential."

John Cohn (IBM): Session on "A to Z of SoCs," ICCAD 2002.

ITRS 2001 Modeling & Simulation Technology Requirements: Desired Capabilities

PRODUCT YEAR	*2003*	*2005*	*2007*	*2010*	*2013*
TECHNOLOGY GENERATIONS (nm)	107	80	65	50	35
CIRCUIT ELEMENT MODELING					
New circuit element mod.	Non-bulk CMOS compact models		2D quantum effects/non-quasi-static models	Circuit models for alternative devices	
Interconnect models	On-chip inductance effects, full-chip RLC				
PACKAGE MODELING					
Unified package and chip models	Unified RLC extraction		Full-wave analysis	Mixed electrical and optical	
Multi-physics models	Thermo-mechanical-electrical integrated models				

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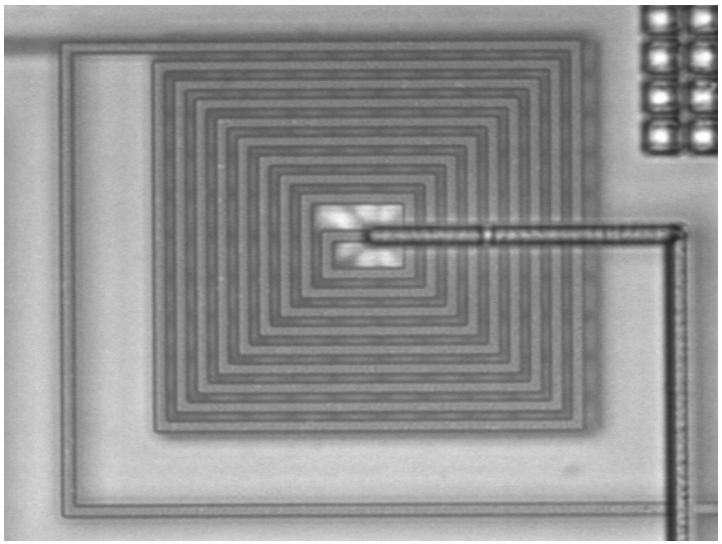
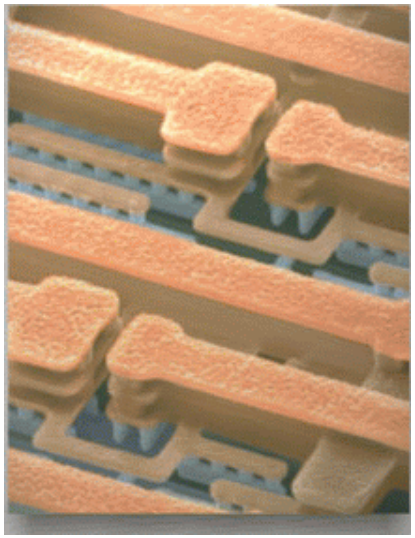
ITRS 2001 – Difficult Challenges (through 2007)

- **High-frequency modeling**
  - Efficient simulation of full-chip interconnect delay
    - 3D interconnect modeling
    - Interconnect inductance & transmission-line effects
  - High-frequency (electromagnetic) models
    - For interference coupling
    - For integrated passives
    - For substrate noise coupling
    - Power grid-induced noise and interference
  - Accurate broadband EM parameter extraction without RF/microwave measurements

The "Anatomy" of On-Chip Electromagnetic Modeling

- **Interconnect Geometry**
  - "Thick" wires of aspect ratio ~ O(1)
  - High-density 3D wiring in a highly non-uniform topography
- **Bandwidth of Interest**
  - Clock frequency → 10 GHz
  - Rise/fall time → ~ 10 ps
  - Effective bandwidth: 0 – 100 GHz
- **Interference Mechanisms**
  - Interconnect-induced crosstalk
  - Substrate coupling
  - Simultaneous Switching Noise
  - Supply grid-induced coupling





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The Uncertainty Factor

- Contrary to the predominantly deterministic nature of signal and power network layout and routing choices at the package and board level, their on-chip counterparts remain in a state of flux during a significant portion of the design flow.
  - **Unique requirements for on-chip SI-driven CAD**
    - **Statistical means of assessing electrical performance**
      - Stochastic modeling of EMI
      - "Homogenization" techniques for expedient estimation of noise generation and coupling
    - **"Hierarchical" modeling**
      - Tradeoff between accuracy and efficiency based on the objectives of the modeling/simulation exercise at the specific stage of design

ITRS 2001 Modeling & Simulation Technology Requirements: Accuracy & Speed

PRODUCT YEAR	*2003*	*2005*	*2007*
TECHNOLOGY GEN (nm)	107	80	65
CIRCUIT ELEMENT MODELING			
I-V Error compact model accuracy	5%	5%	3%
RLC delay accuracy (% of (max chip frequency)$^{-1}$)	5%	5%	3%
PACKAGE MODELING			
Package delay accuracy (% of (max chip frequency)$^{-1}$)	1%	1%	1%
NUMERICAL METHODS			
Linear solvers (equations per minute)	600k	700k	800k
Parallel speed-up	4x	8x	16x
MFLOPS required	4000	6500	10000

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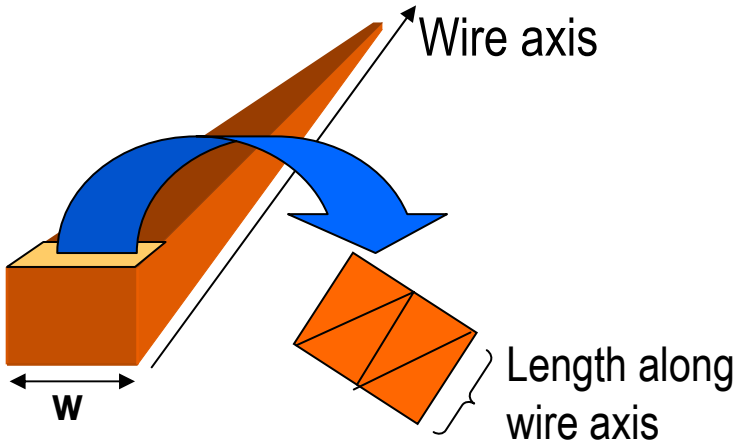
The Solvers of Choice: Fast Integral Equation Solvers

- Electrodynamic extensions of **FastCap** & **FastHenry** aiming at O(NlogN) memory and CPU-time complexity
  - Fast Multipole Methods
  - Pre-corrected FFT/Adaptive Integral Method
  - **IES3**
- **Time-domain versions** enable transient non-linear analysis of hybrid interconnect-circuit networks
- Parallel implementations enhance modeling capacity

Estimating complexity

- # of cells per wire cross section: 16 (minimum)
- Cell size along wire axis: variable {w to 5w}
- Example: 32-wire bus, 6 mm in length, of w = 1 μm
  - # of crossing wires (above and below): 100/mm
  - Length of crossing wires: 600 μm
- Total # of cells: ~ 1.35 M



"Outsmarting" Interconnect Complexity

"A better approach is a new design methodology that focuses on the interconnect. That is, the dense array of integrated circuit interconnect must be thoroughly understood and carefully characterized to preclude the need for its post-layout analysis."

Ronald Rohrer, "A Brief History of the Future of Semiconductor Electronic Design Automation," CAD Plenary Talk, 1997 IEEE International Conference on Computer Design (ICCD '97)

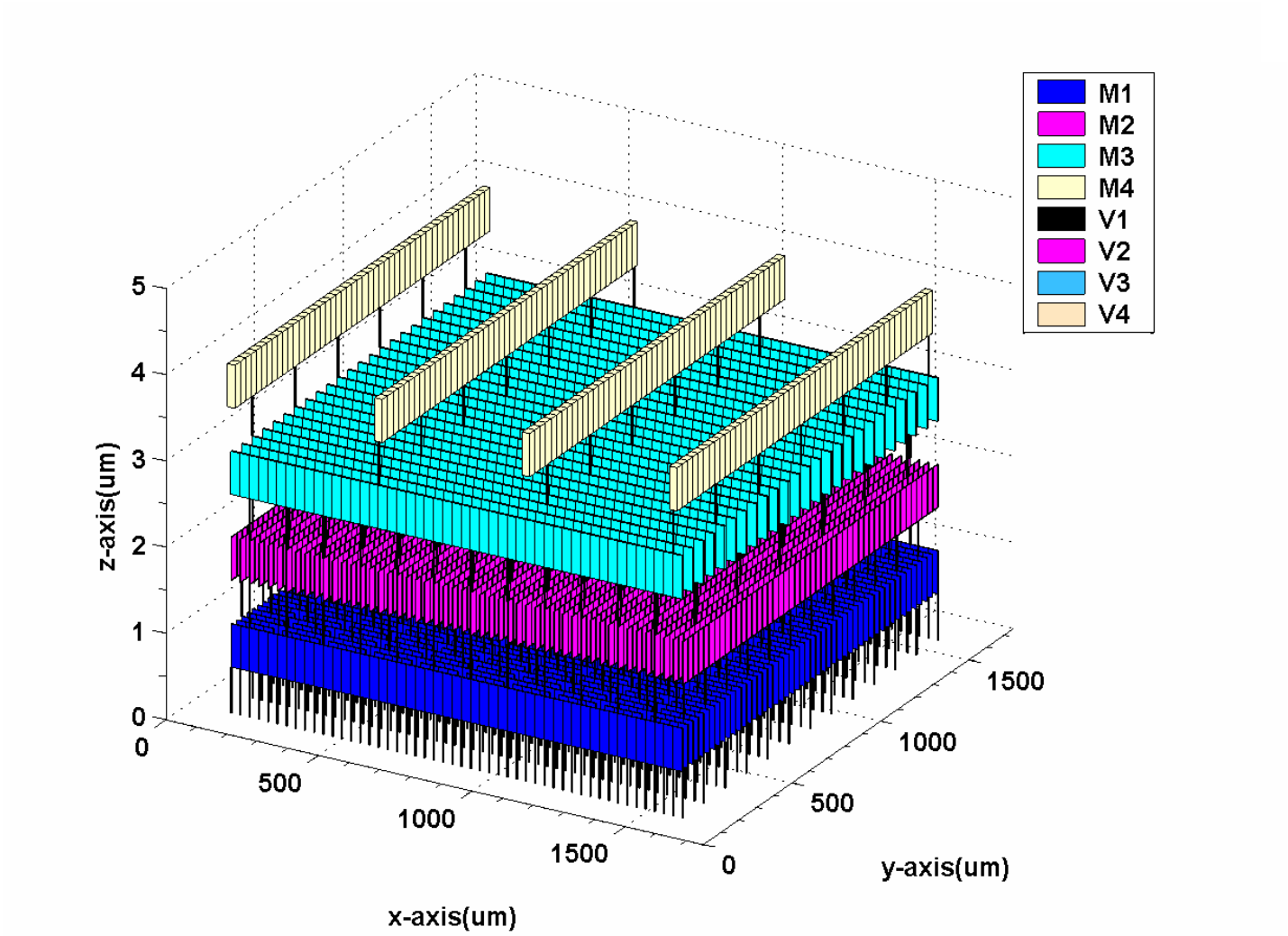
On-Chip Power Grid Modeling

- "INDUCTIVE EFFECTS" important for accurate on-chip power grid simulation for < 130 nm technology
- Current approaches tend to be [R][L]-driven
  - Need to extract [L] first
- Drawbacks of a-priori [L] extraction
  - Computationally expensive
  - Return current path-dependent
  - Displacement current impact significant at pico-second switching speeds
    - RL-only analysis inaccurate!
- [R][L][C] modeling of the electromagnetic analysis is cumbersome and leads to very dense and huge SPICE netlists

The Electromagnetic Alternative

- **Maxwell equation's-based modeling of the power grid**
- **Key Attributes**
  - Model developed directly from physical structure
  - Cumbersome and error-prone extraction of [L] and [C] avoided
  - Rigorous modeling of electromagnetic effects
  - In addition to power switching noise analysis it enables prediction of power grid-induced EMI between different blocks on the chip

The Issue of Complexity



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Modeling Methodology

Finite-volume discretization of Maxwell's equations

$$\oint_{C_F} \vec{E} \cdot d\vec{l} = -\frac{d}{dt} \iint_{S_F} \mu \vec{H} \cdot d\vec{S}$$

$$\oint_{C_A} \vec{H} \cdot d\vec{l} = \frac{d}{dt} \iint_{S_A} \varepsilon \vec{E} \cdot d\vec{S} + \iint_{S_A} \sigma \vec{E} \cdot d\vec{S}$$

- Micron-size cross-sectional dimensions of grid exploited to contain model complexity
  - Grid size of the order of grid feature size
  - Uniform distribution of current over wire cross section

Accommodating the circuit models of the devices

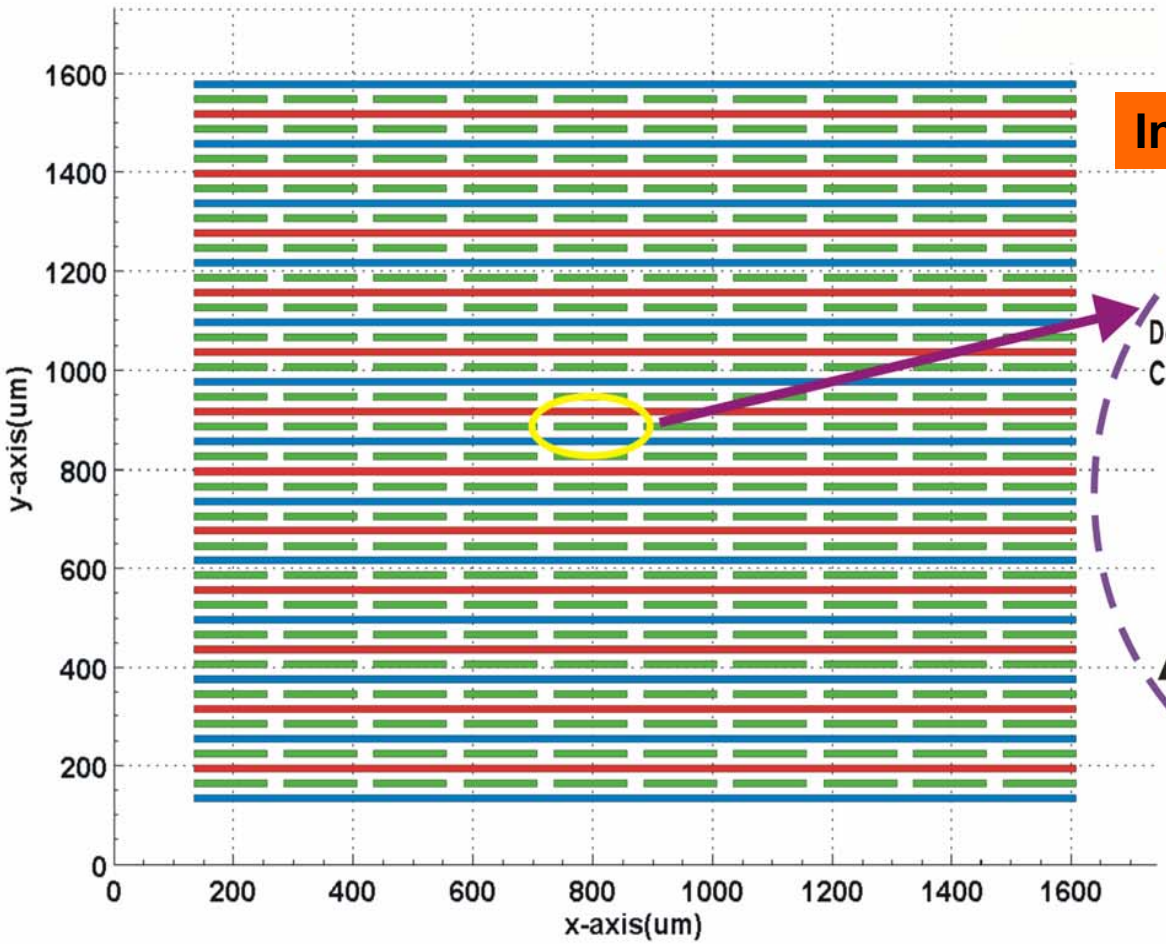
The state-space form of the discrete model,

$$\begin{bmatrix} \mathbf{G} & \mathbf{D}_h \\ \mathbf{D}_e & \mathbf{R} \end{bmatrix} \begin{bmatrix} \mathbf{e} \\ \mathbf{h} \end{bmatrix} + \begin{bmatrix} \mathbf{C} & \mathbf{0} \\ \mathbf{0} & \mathbf{L} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \mathbf{e} \\ \mathbf{h} \end{bmatrix} = \begin{bmatrix} \mathbf{i}_S \\ \mathbf{v}_S \end{bmatrix}$$

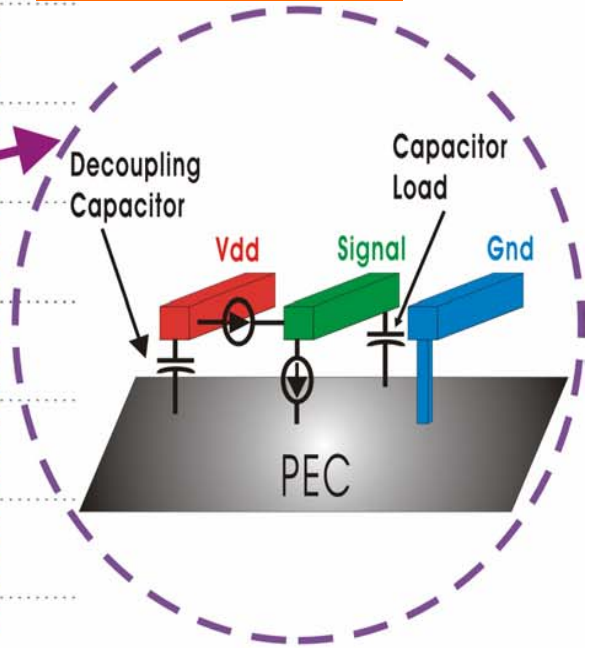
facilitates direct incorporation of lumped circuits and behavioral models for drivers and receivers

- e , h : the discrete unknown fields
- G, R, L, C, D_h, D_e : sparse matrices (dependent on material and geometric properties of the structure)
- i_S, v_S : voltage & current sources connected to the grid

Top view of Metal-1 Layer



Inverter Model



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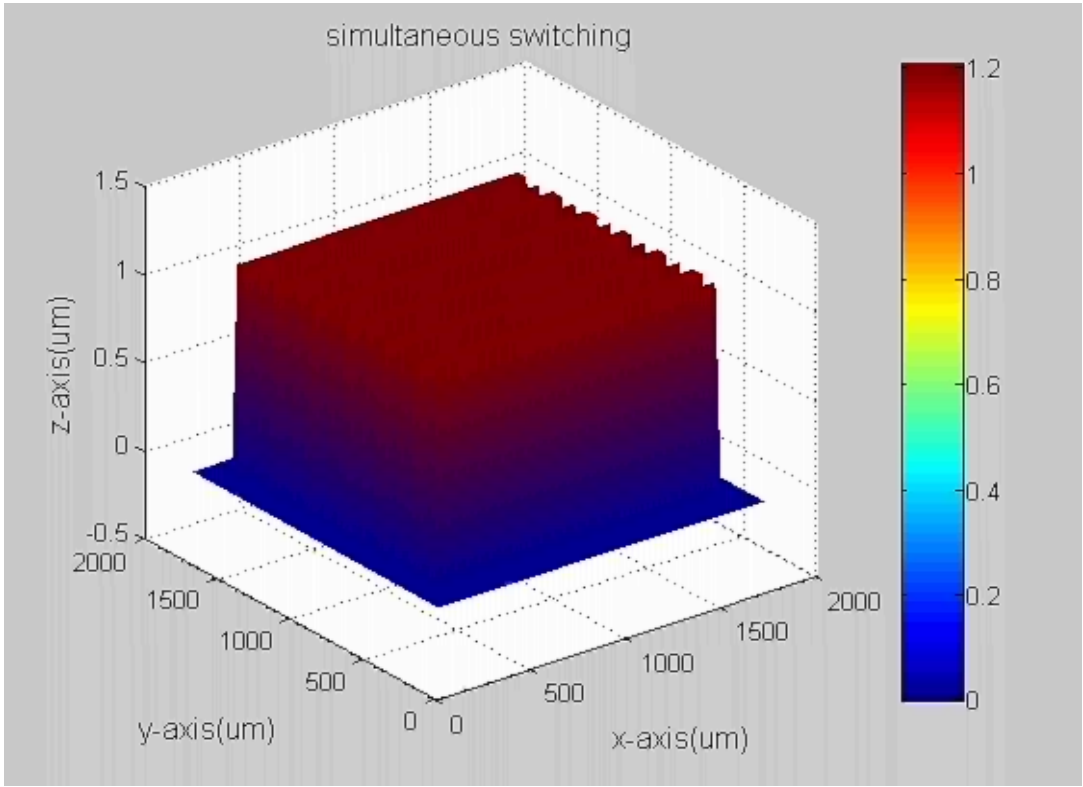
Transient EM Modeling of Simultaneous Switching

Simultaneous switching at all nodes



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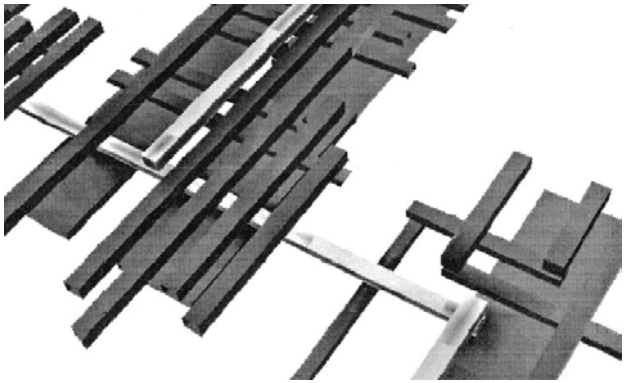
Chip-package power grid co-design through reduced-order macro-modeling

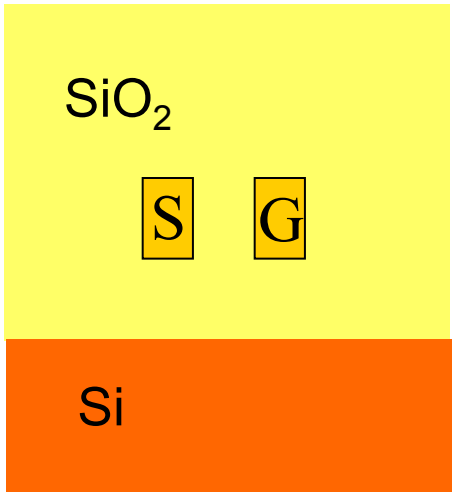
- **Electromagnetic modeling of the package**
  - Generation of broadband multi-port macro-model
- **N-port package macro-model captures:**
  - Distributed decoupling and resonances due to package power & ground planes
  - The distributed effect of the combination of various on-chip decaps
  - The impact of on-chip non-uniform switching
- **Power grid-induced noise is modeled correctly**
  - **Essential for mixed-signal designs!**

EM Modeling of the Interconnect

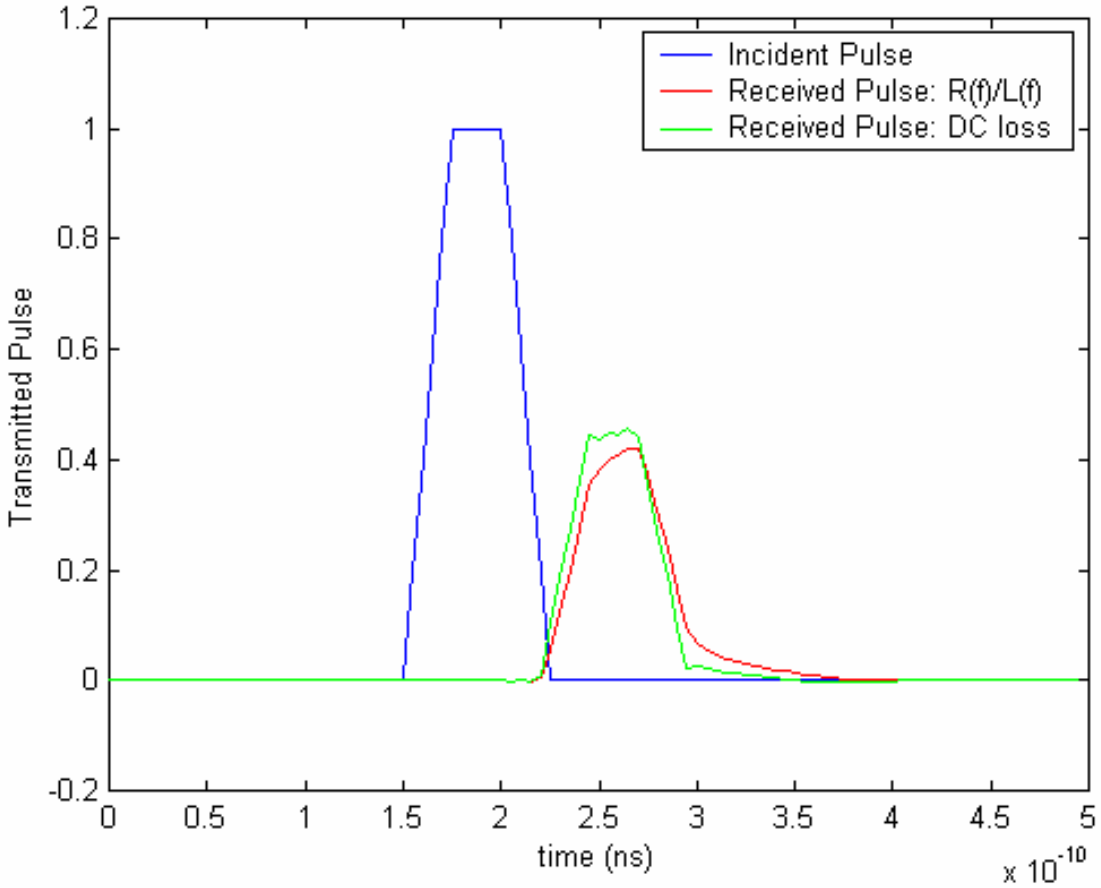
- Need to tackle 3D complexity:
  - Crossing wires
  - Skin effect
  - Frequency-dependent return path
- Noise-aware design relaxes complexity
  - Dedicated return path for critical nets
  - Transmission line-based modeling may be applicable
    - Dependent on both bandwidth of interest and geometry
    - Use of 2D extractors (frequency-dependent per-unit-length parasitics) whenever possible
- 3D EM solvers needed where 2D models fail
  - Broadband interconnect characterization (from dc to multi-GHz)
  - Multi-port description
  - Synthesis of SPICE-compatible equivalent circuit models



Despite sub-micron cross-sectional dimensions skin effect is still an issue



width = 1.0 μm
thickness = 1.5 μm
pitch = 2.0 μm
Copper metallization



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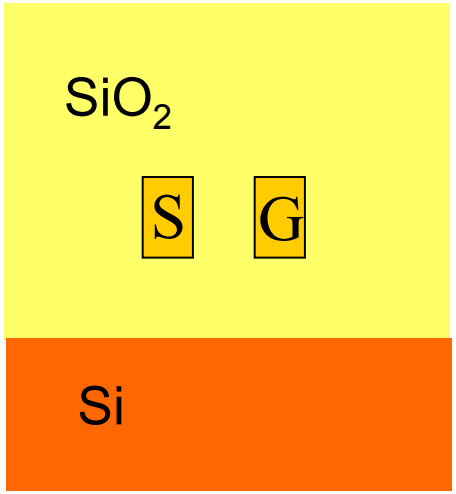
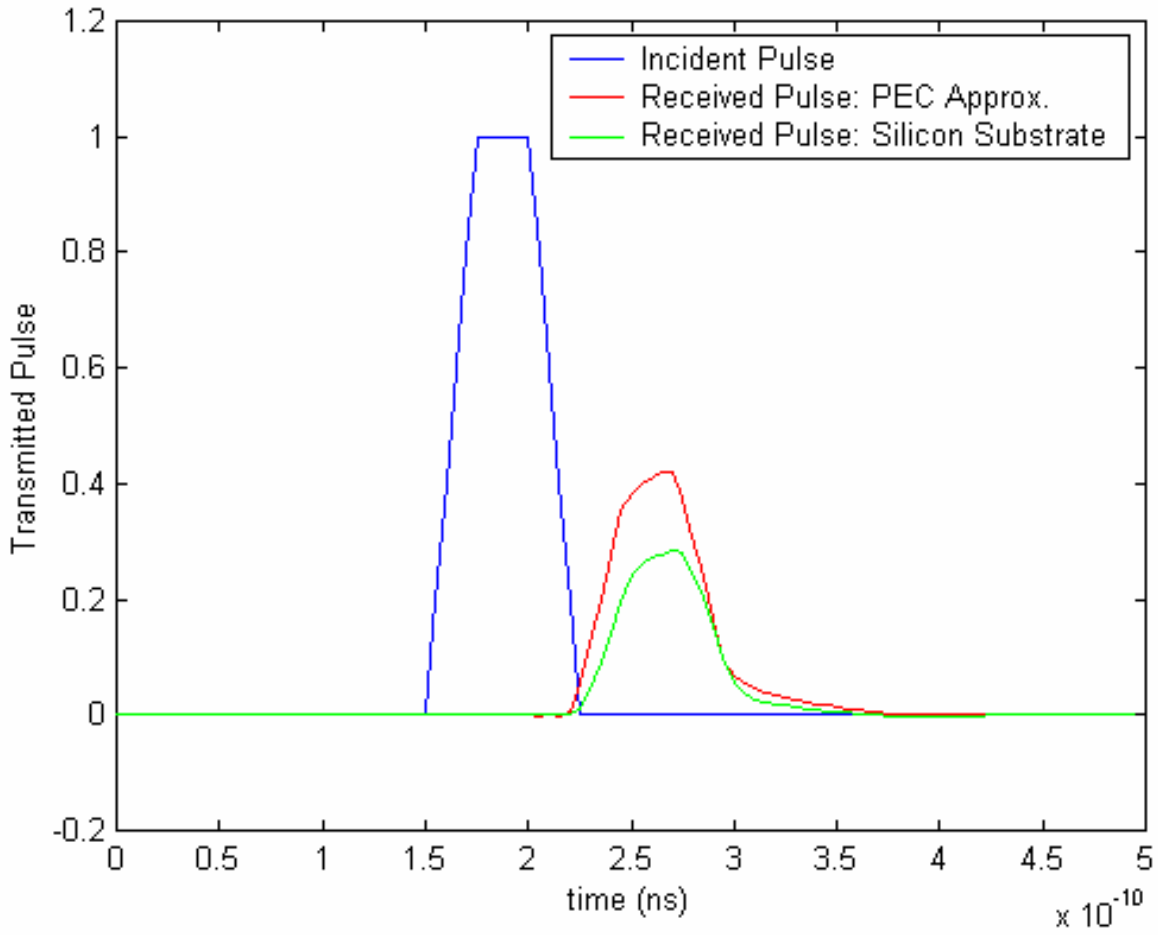
Silicon substrate loss a factor of concern at high speeds…



width = 1.0 μm
thickness = 1.5 μm
pitch = 2.0 μm
Copper metallization
ρ_{Si} = 0.1 Ohm·cm



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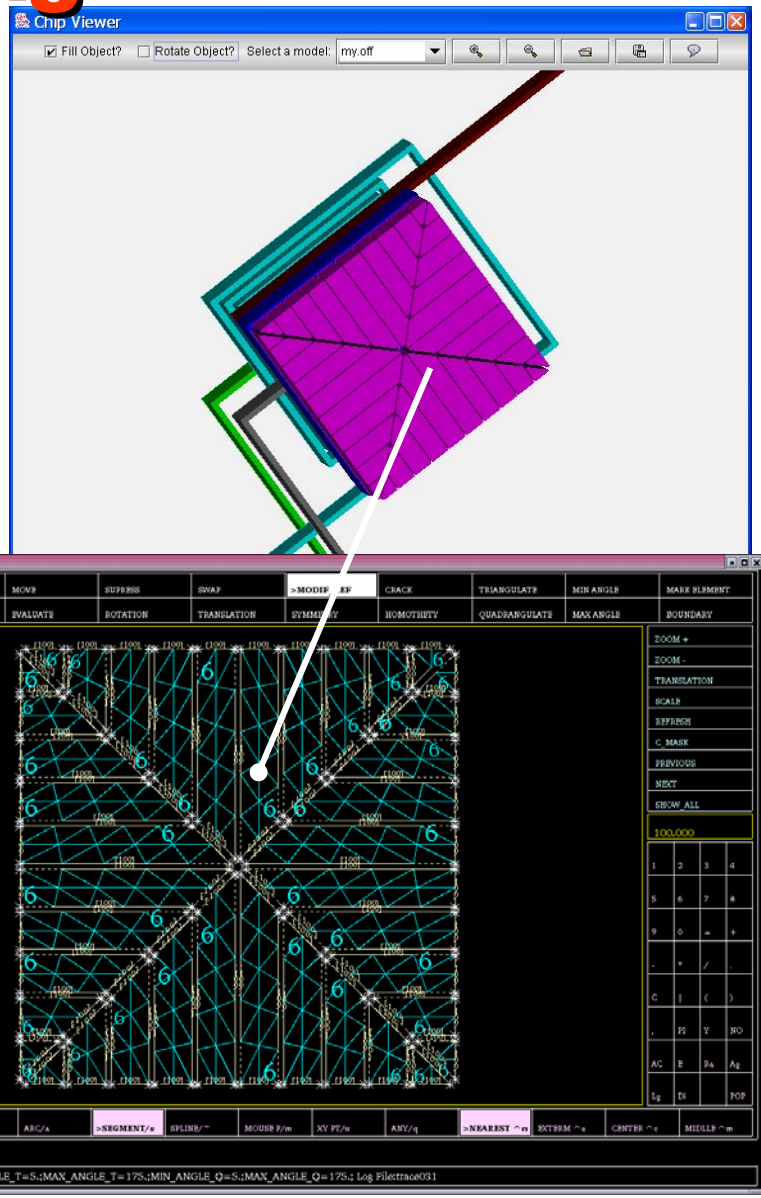
EM Field Solver streamlined for interconnect modeling

- Generalization of the Partial Element Equivalent Circuit (PEEC) approximation of Maxwell's equations through the use of:
  - **Frequency- and position-dependent surface impedance on wire cross section to capture frequency-dependent skin effect**
  - **Layered media Green's function for efficient modeling of the impact of layered, lossy substrates**
  - **Use of triangular elements for geometry discretization**
  - **Replace MNA-based formulation with Mesh (Loop)-based formulation to ensure numerical stability as ω→0**



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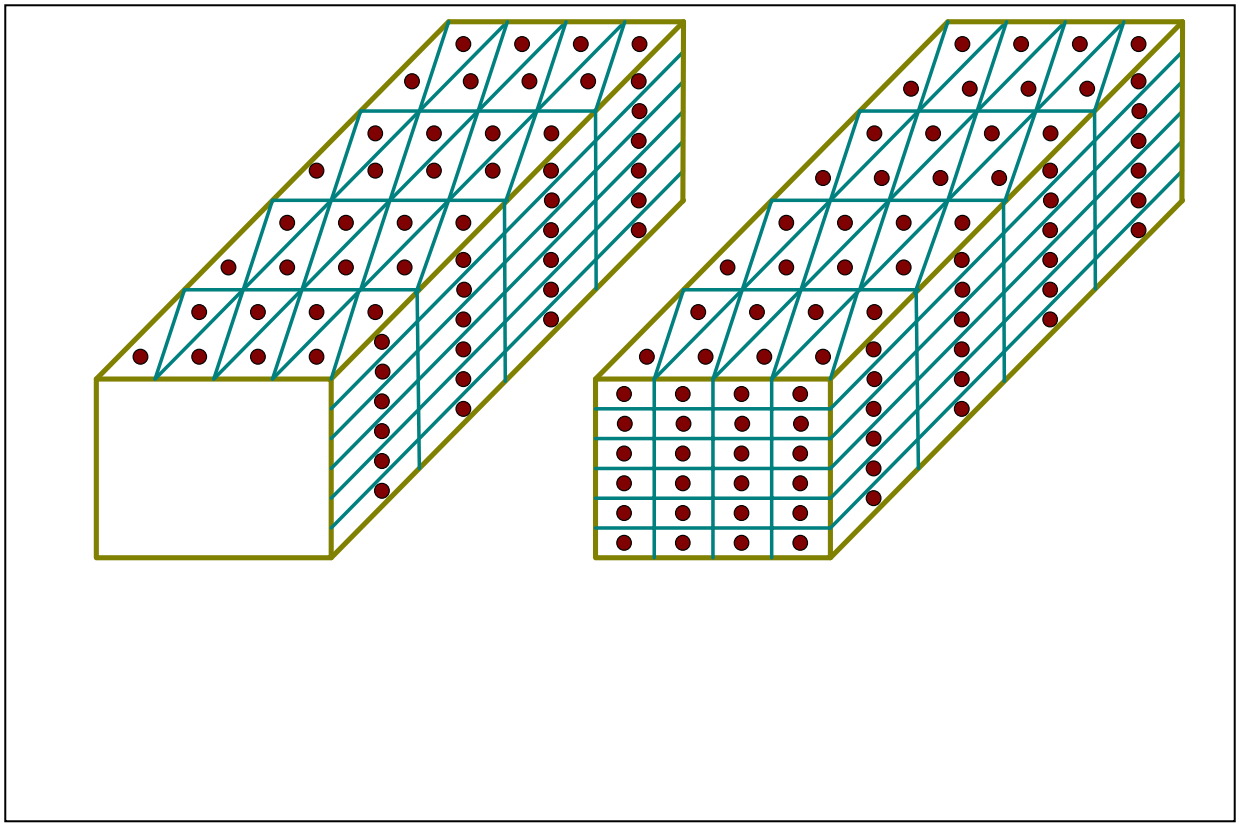
Skin-effect loss modeling requires accurate modeling of wire interior



Surface formulation helps contain the # of unknowns in the discrete problem

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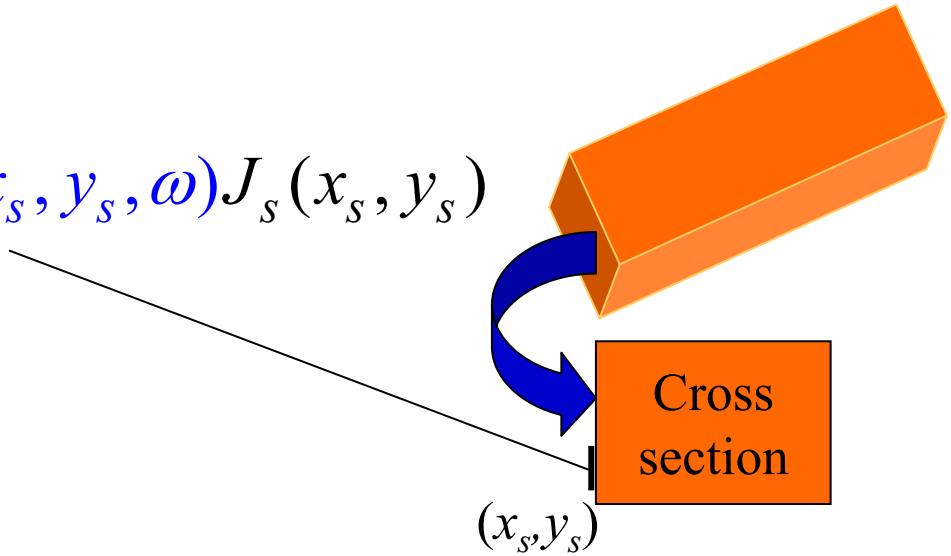
Efficient handling of skin effect via a position-dependent surface impedance

Assuming longitudinal only current flow in the interior, a position- and frequency-depended **effective** surface impedance can be obtained from the solution of an interior 2D boundary value problem

$$E_s(x_s, y_s) = Z_s^{eff}(x_s, y_s, \omega) J_s(x_s, y_s)$$



Interpreting the Physics through the PEEC Model

For time-harmonic fields (angular frequency ω):

$$\vec{E}(\vec{r},\omega) = \underbrace{-j\omega\left(\int_{S_C} G(\vec{r},\vec{r}';\omega)\vec{J}(\vec{r}',\omega)ds\right)}_{\text{"Inductive" Contribution}} \underbrace{-\nabla\left(\int_{S_C} G(\vec{r},\vec{r}';\omega)\rho(\vec{r}',\omega)ds\right)}_{\text{"Capacitive" Contribution}}$$

- Layered media built-in in $G(\vec{r},\vec{r}';\omega)$
- Solve for electric currents and charges
- Equation is enforced on conductor surface through:

  a) use of effective surface impedance condition:

  $$Z_{eff}(\vec{r},\omega)\vec{J}(\vec{r},\omega) = \vec{E}(\vec{r},\omega)$$

  b) and the calculation of a "weighted voltage drop" along each current patch:

  $$\int_{\text{current patch}} Z_{eff}(\vec{r},\omega)\vec{J}(\vec{r},\omega)\cdot\vec{w}(\vec{r})ds$$

Low-frequency Numerical Instability

$$\left.\begin{aligned} \left|(j\omega\mathbf{L})_{km}\right| &\propto \omega h_{cell} \propto \frac{h_{cell}}{\lambda} \\ \left|\left(\frac{1}{j\omega}\mathbf{P}\right)_{km}\right| &\propto \frac{1}{\omega h_{cell}} \propto \frac{\lambda}{h_{cell}} \end{aligned}\right\} \Rightarrow \left|\left(\frac{1}{j\omega}\mathbf{P}\right)_{km}\right| \gg \left|(j\omega\mathbf{L})_{km}\right| \text{ as } \omega \to 0$$

- "Capacitive term" dominant as $\omega \to 0$
- "Inductive term" saturated by numerical noise
  - Capturing inductive behavior of interconnect circuits as $\omega \to 0$ becomes problematic
- MNA matrix (numerically) singular as $\omega \to 0$
  - Iterative solution of the MNA matrix unreliable as $\omega \to 0$

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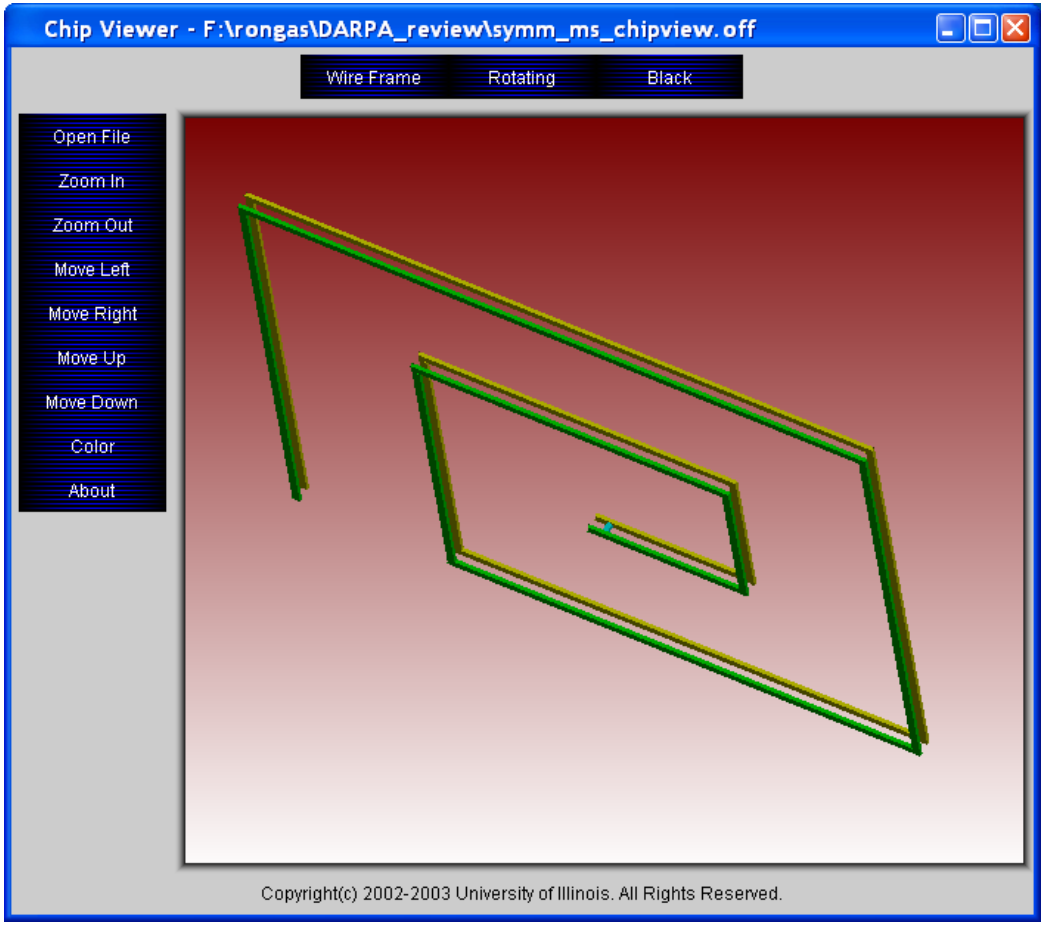
Remedying Low-frequency instability via "Mesh" Formulation



Short-circuited two-wire strip loop

Parameters

Width: 12 microns

Thickness: 4 microns

Gap: 12 microns

Via: 8x8 microns

Length: 4.75 mm

Conductivity: 28.5 s/micron

Insulating substrate: 4.1

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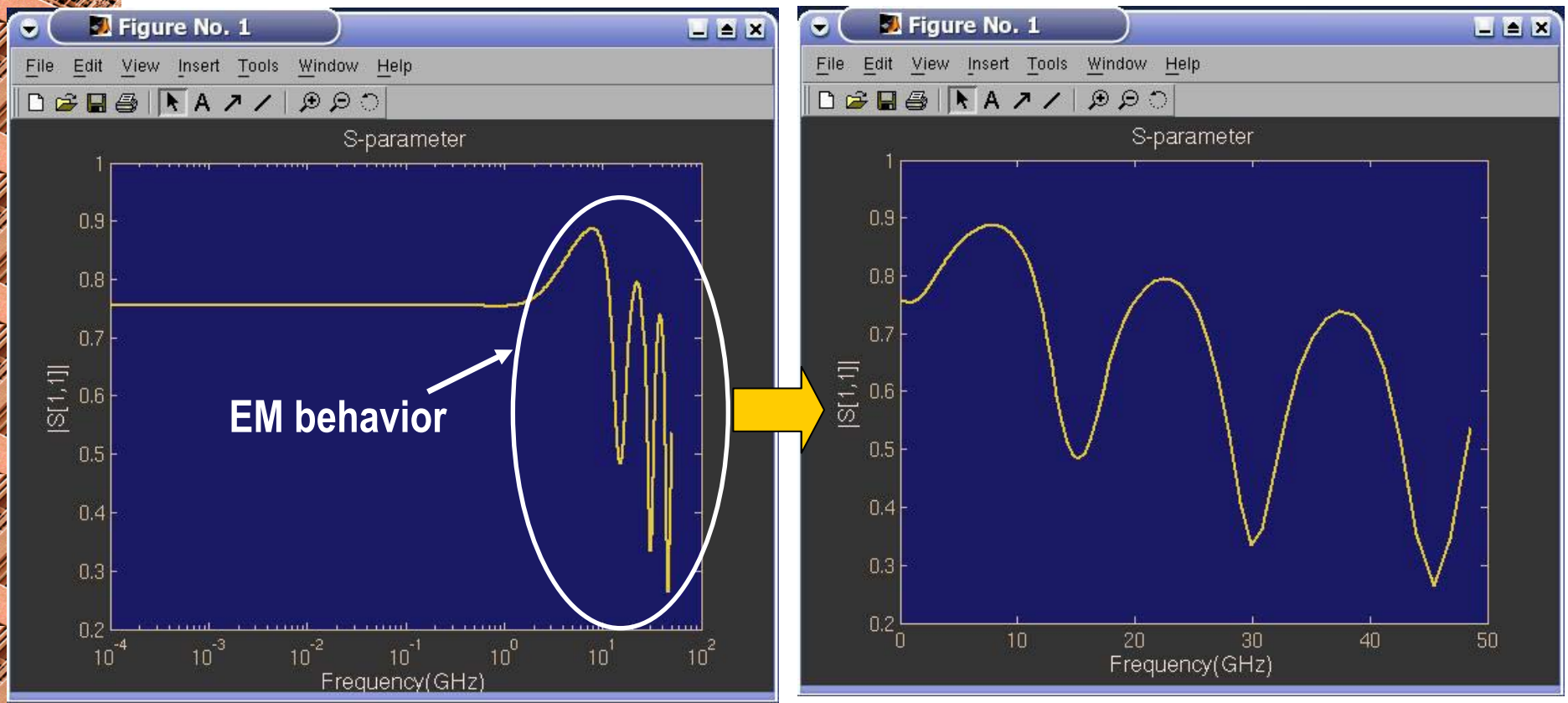
Stable modeling from dc to 50 GHz



Calculated reflection coefficient at input of short-circuited loop

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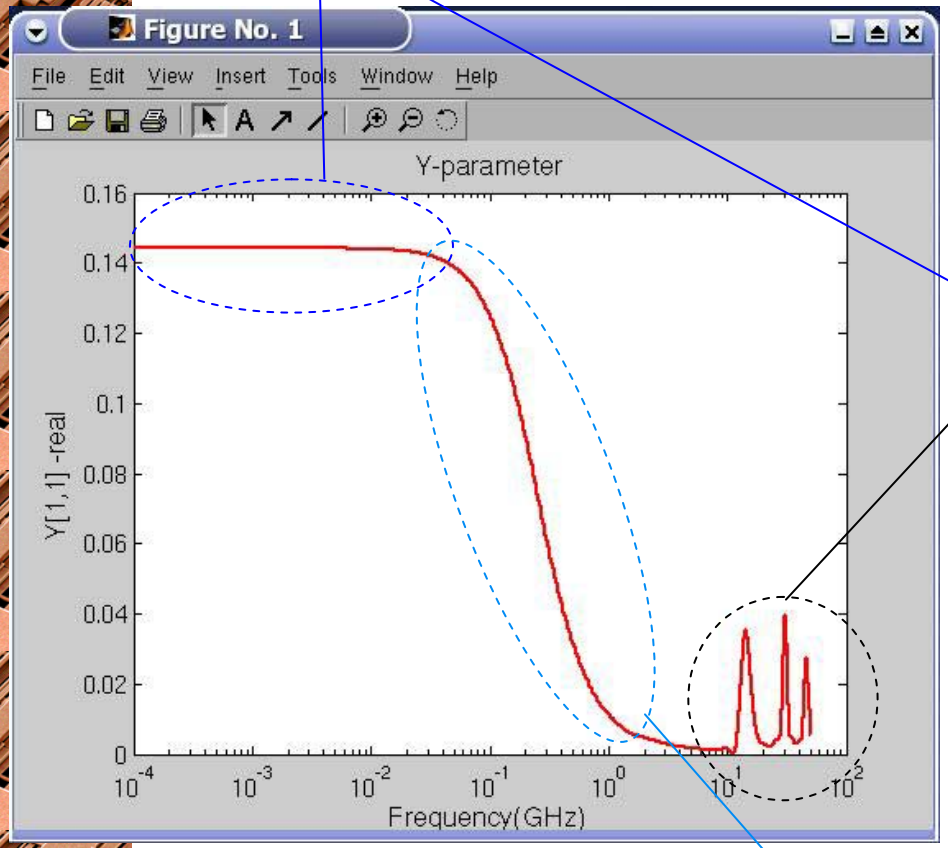
Accurate multi-GHz bandwidth response using a single solver

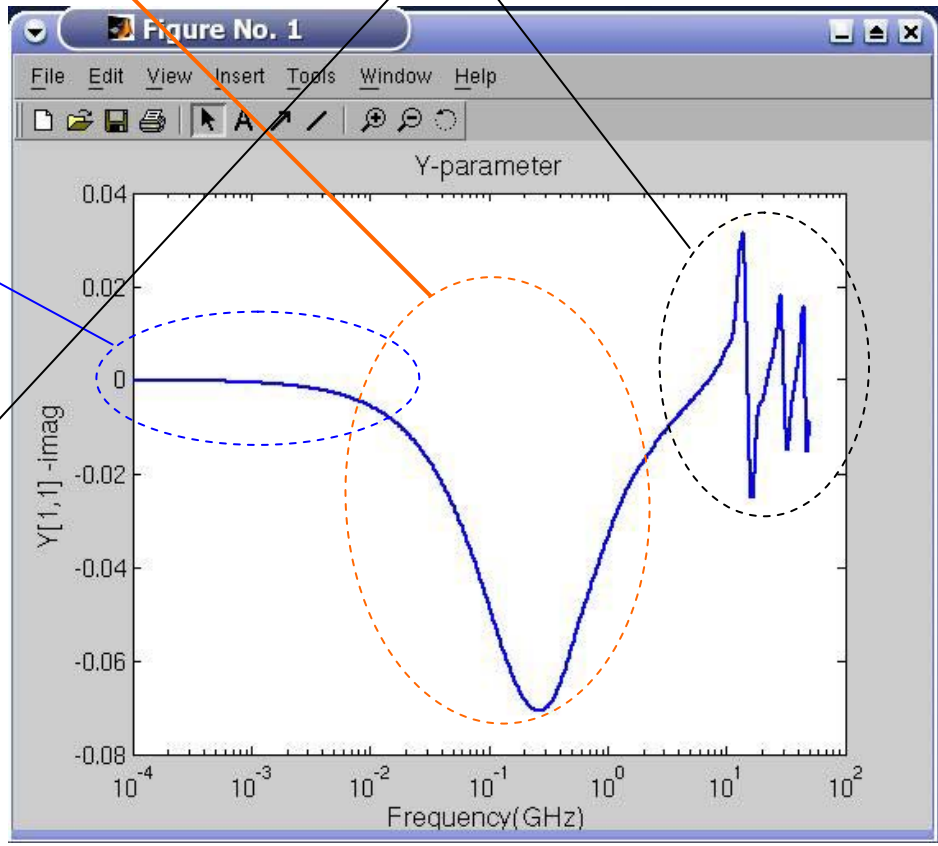
Resistive behavior

Inductive behavior

Antenna behavior



(a) Real part



(b) Imaginary part

Skin effect

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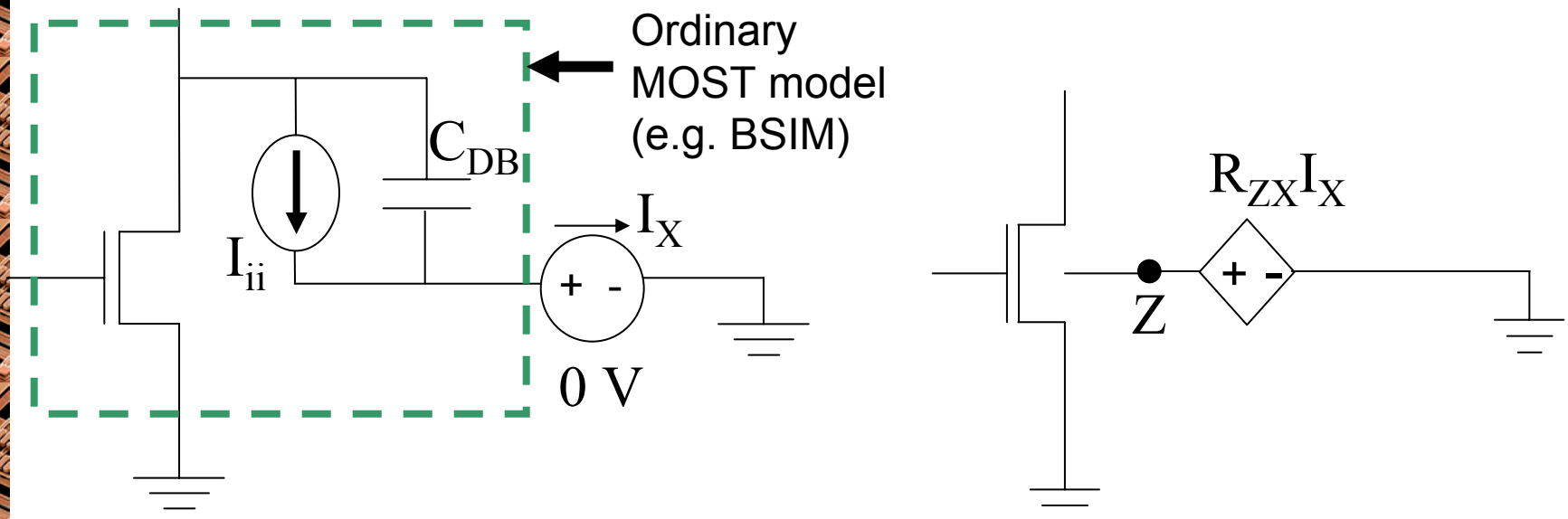
Modeling of Semiconductor Substrate Noise Coupling

- Semiconductor substrate modeling particularly important for single-chip mixed-signal designs
  - Also relevant on interconnect and on-chip passives electrical performance prediction
- SPICE-compatible modeling of substrate-induced coupling effected through the extraction of a multi-port conductance matrix
  - Capacitive behavior of the substrate can be incorporated also
  - Modeling to date based on quasi-static assumptions
    - Semiconductor substrate dealt with separately from the interconnect grid
    - Interconnect-to-substrate coupling grossly modeled through ad-hoc procedures

Modeling of Noise Injection to/from NMOSTs

- Substrate current captured by adding current monitors to netlist
- R_{ZX} is the transfer resistance, which models the substrate coupling between node X and node Z

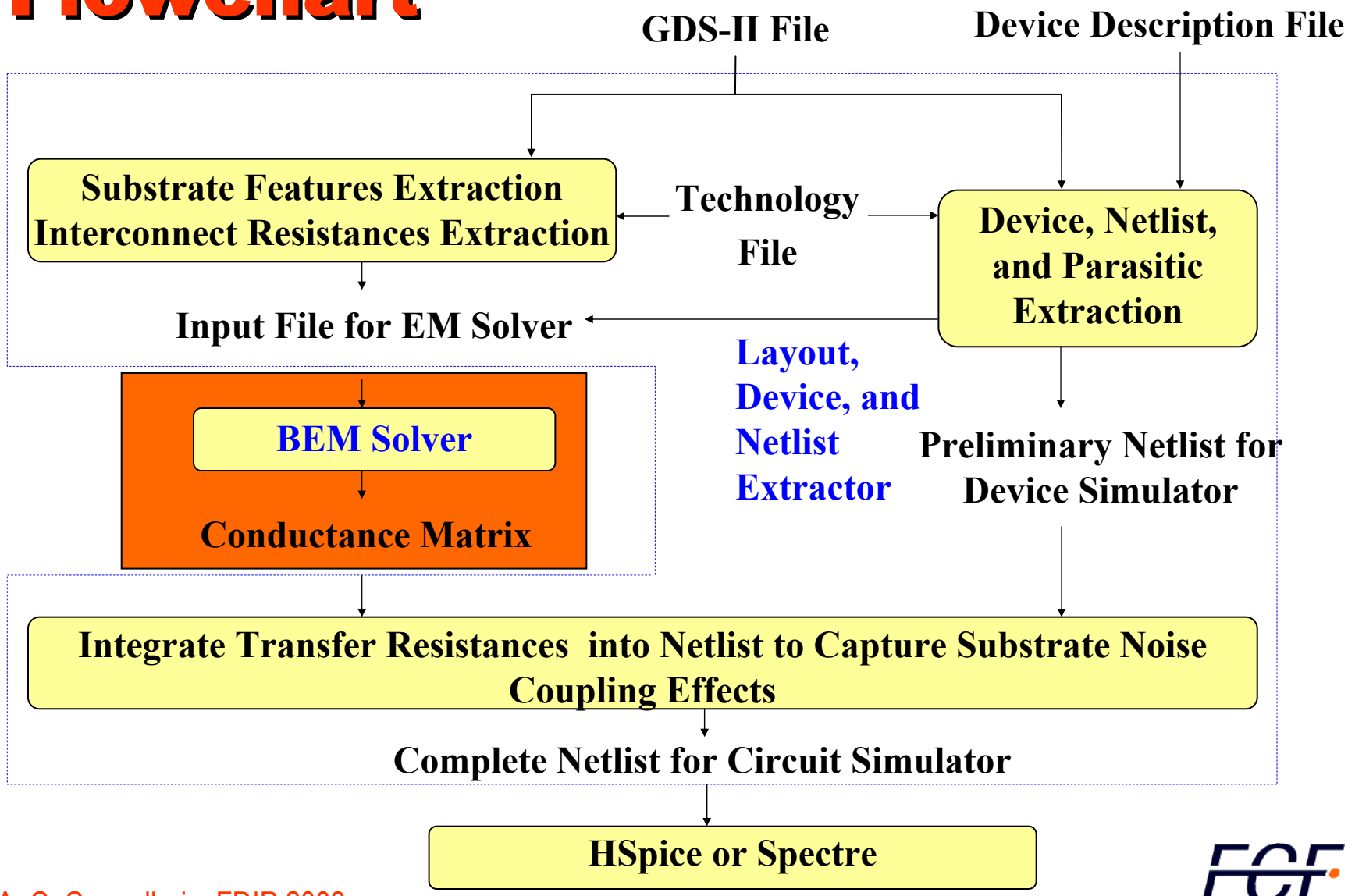


- I_{ii} is impact ionization current (i.e., dc substrate current)

Modeling of Noise Sources (cont.)

- Such a model is impractical to use SPICE for large circuits
- May need to simulate digital blocks (noise sources) and analog blocks (noise sensors) separately
- Macromodeling allowed
  - User can pre-characterize noise waveforms injected by specific circuit blocks
  - Substrate solver treats such circuit blocks as either point noise sources or distributed noise sources
- "Distributed noise coupling" from interconnect difficult to capture

Substrate Noise Analysis Flowchart



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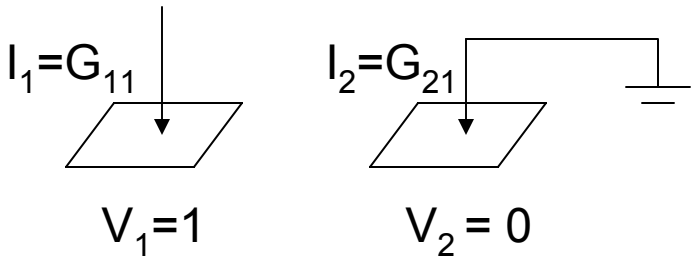
Boundary-Element Method Solvers

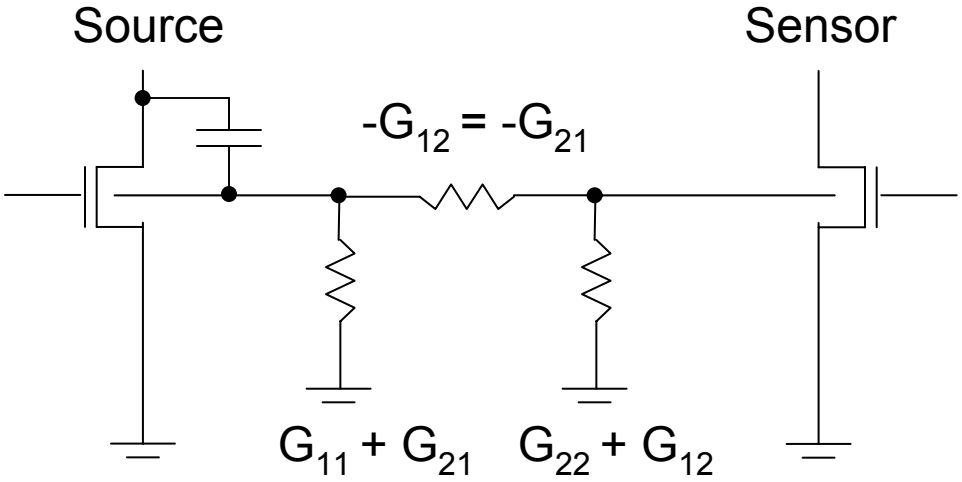
- **Integral equation solvers with static or quasi-static Green's function kernels**
  - Sophisticated versions include:
    - Layered media Green's function capability
    - Hybrid FEM-BEM formalism to handle non-uniformly doped volumes of finite extent
  - Fast solution capability
    - Pre-corrected FFT solver

Substrate Conductance Matrix Calculation

- To calculate *G*, BEM equation is again solved by setting one of the ports to 1V, and the other at 0V.



- Equivalent circuit with conductance matrix:



G-matrix abstraction of substrate coupling

- **Fifty-two contacts example.**
  - Substrate height h=400 μ m, one layer with ρ =15 Ω -cm, backside contact.
  - R matrix is defined as an element-by-element inverse of the conductance matrix.
  - Figure taken from [1]
  - [1] N. Masoumi, M. I. Elmasry, et al, *Proc. IEEE Int. Workshop on Electronic Design, Test and Applications*, p. 355, Jan 2002.

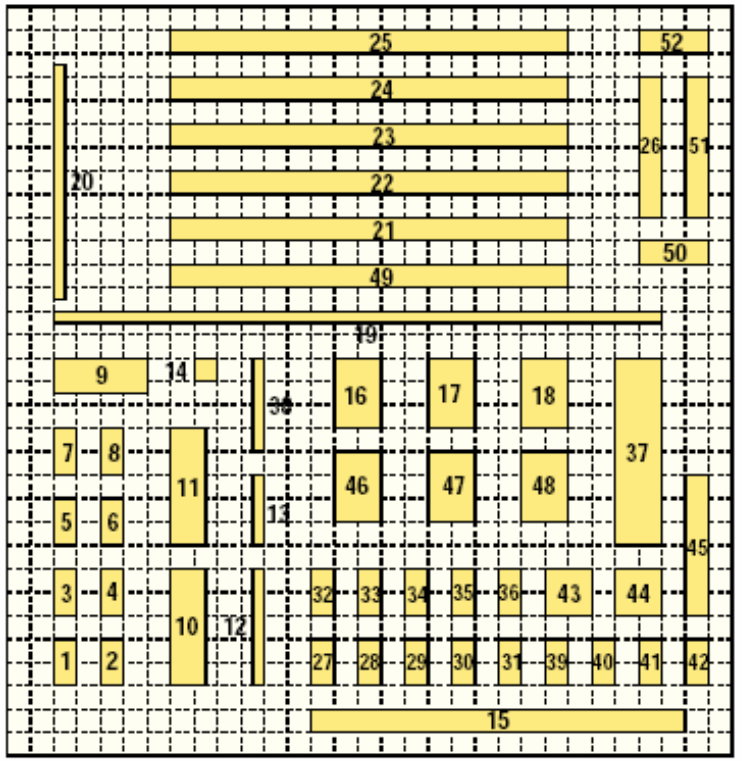
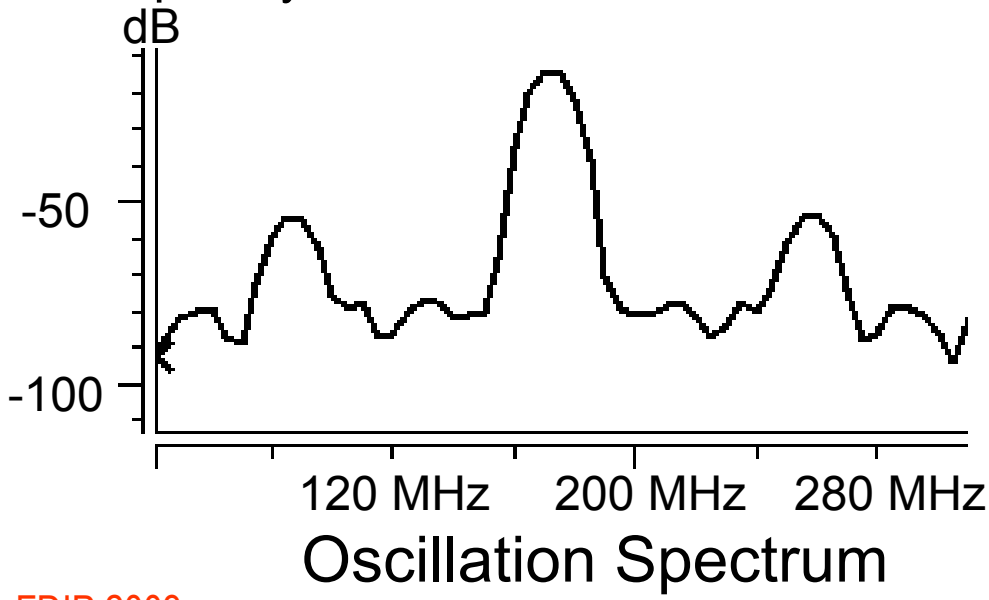


Figure 7. The substrate contact layout of the 52-contact problem.

	R(3,4)	R(10,19)	R(25,50)	R(33,34)	R(48,50)
R[1](KΩ)	60.35	353.55	437.77	61.92	1,005.64
R (KΩ)	59.30	378.98	460.63	60.85	1,056.20
Diff.	1.75%	7.19%	5.22%	1.73%	5.03%

Study the Effect of Substrate Noise on a Ring Oscillator

- Single-ended ring oscillator, operating frequency of about 172MHz.
- Noise injector is large inverter operating at 72MHz.
- Turning on the noise source does not affect the oscillation frequency but does introduce side lobes approximately 80MHz from the frequency of oscillation.



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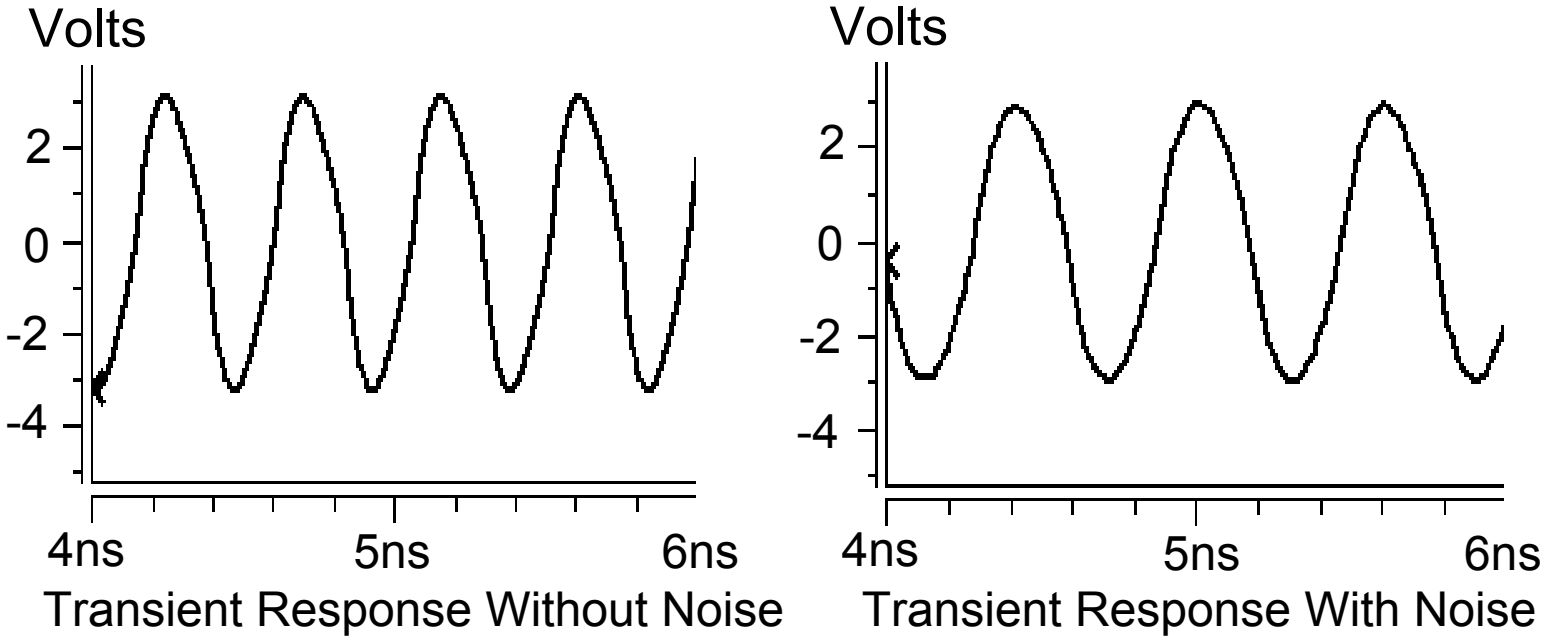
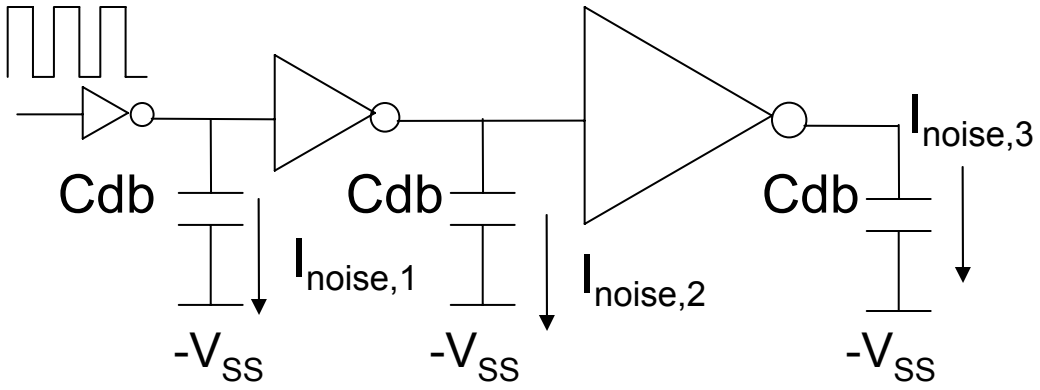
Effect of Substrate Noise Coupling on Voltage Controlled Oscillator

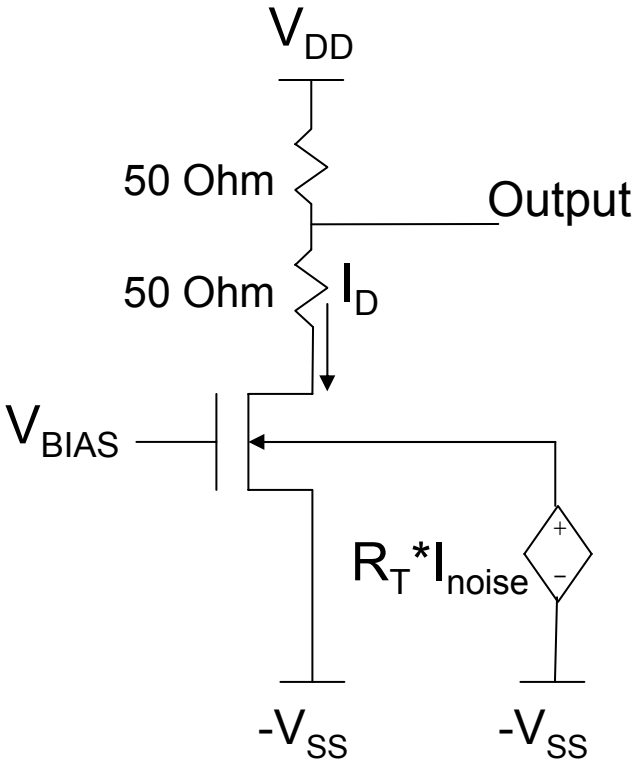


- VCO with operating frequency of 2.19 GHz and peak voltage values of -3.21 V and 3.11 V.
- Noise injector is a large inverter operating at 1.25 GHz.
- Noise lowers operating frequency to 1.695 GHz and reduces peak voltage to -2.95 V and 2.90 V.

Test Chip: Noise Injecting and Sensing Circuits



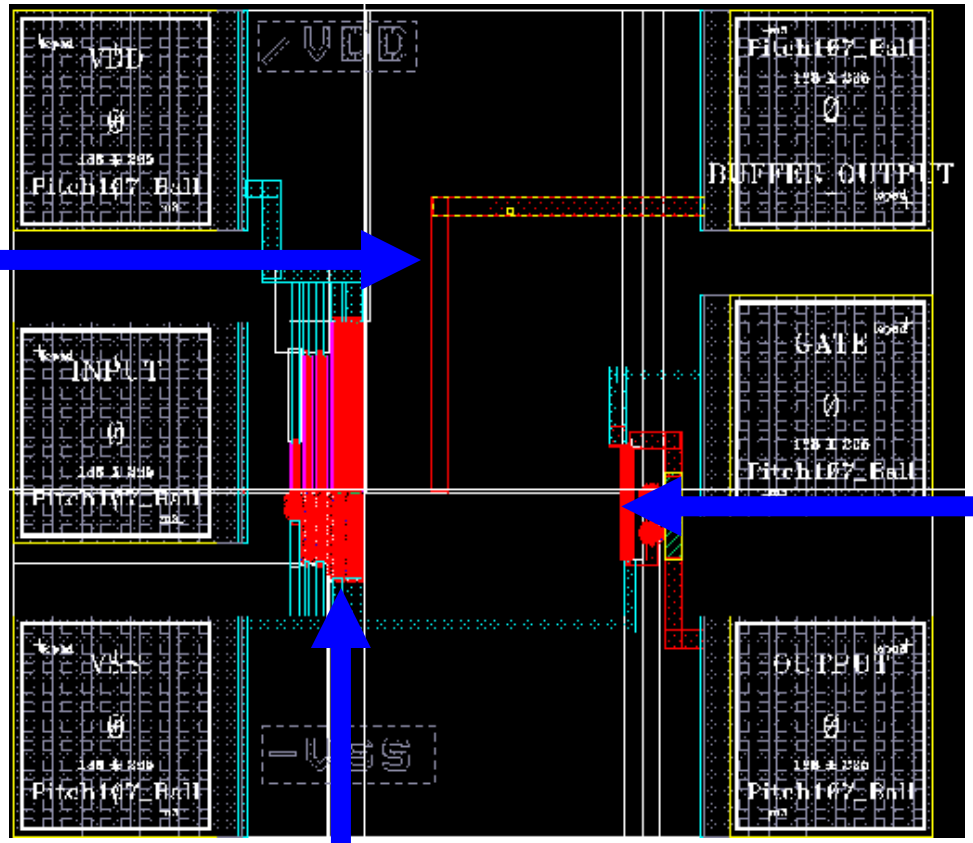
Injector: output buffer



Sensor: Common-source amplifier

Test Circuit Layout

Long interconnect from buffer output to pad



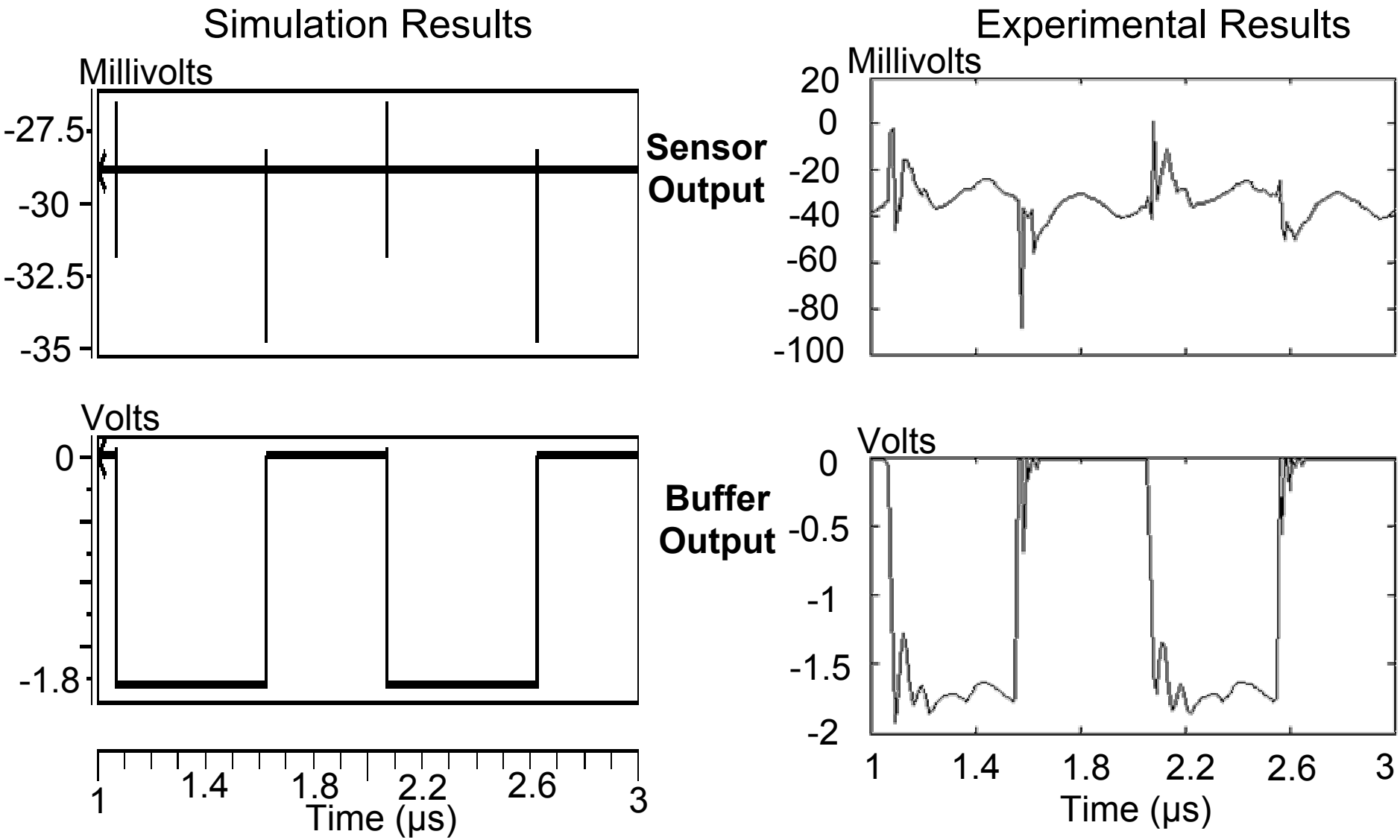
Sensor NMOST

Output Buffer (injector)

Experimental Notes

- **HSPICE circuit simulator was used.**
  - Level 49 MOS model (BSIM) was used.
- **In the experimental setup, V_{dd} = 0V and V_{ss} = -1.8V.**
  - Sensor output node directly connected to oscilloscope (50Ω input).
- **Negative going spikes in the sensor output waveform correspond to increasing drain current.**
  - This would be the result of threshold voltage reduction by positive substrate voltage fluctuations ($V_B > -V_{SS}$).

Experiment vs Simulation



Apparent shortcomings of the model

- Measured ΔV at sensor was larger than simulated values (approximately 50mV in worst case)
  - **This, most likely, is due to additional substrate coupling from the interconnect and pads.**
    - The buffer output is connected to a long interconnect (see layout) and pad in proximity to the sensor. Displacement current injected from these structures will add to that injected by the inverters.
    - Pads are 100 μm X 100 μm in metal 3.

Interconnect Coupling to Substrate

- Including coupling from interconnect to state-of-the-art substrate-coupling models is non-trivial.
  - Example: How many RC segments should the interconnect be partitioned into, so that computations will be quick but accurate?
- What is needed, instead:
  - A rigorous model, where semiconductor substrate and the appropriate portion of the interconnect at Metal 1 are modeled concurrently, overcomes the modeling shortcomings of current substrate-coupling modeling tools
    - Such a model should employ electro-dynamic kernels
    - Noise coupling quantified in terms of multi-port transfer matrices

"Management" Challenges

- **Management of knowledge, understanding and data generated by the field-centric characterization of the EM behavior of the interconnect**
  - If we cannot "hide the physics" from the designer, we then need to abstract its implications through the development of design-relevant noise-aware rules and guidelines
  - EM CAD tool developers are not the ones to decide the needed abstraction
  - Major EDA tool vendors are critical players in the development and implementation of such interconnect-centric design philosophy; yet they seem reluctant to assume the role of the playmaker
- **New start-ups?**
- **Open-access EDA?**

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