CAD Tool Requirements for Next Generation On-Chip Signal Integrity Issues

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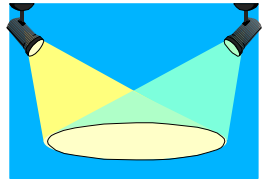
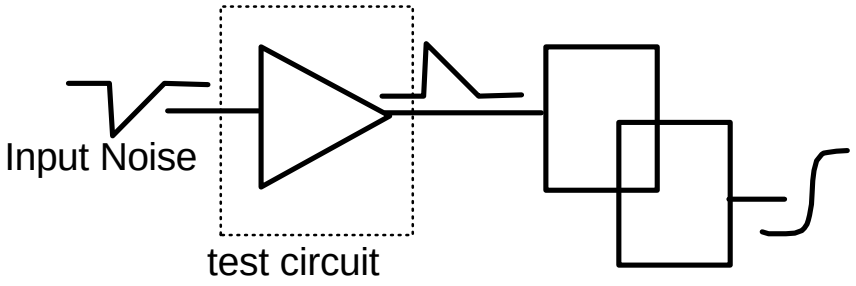


Agenda

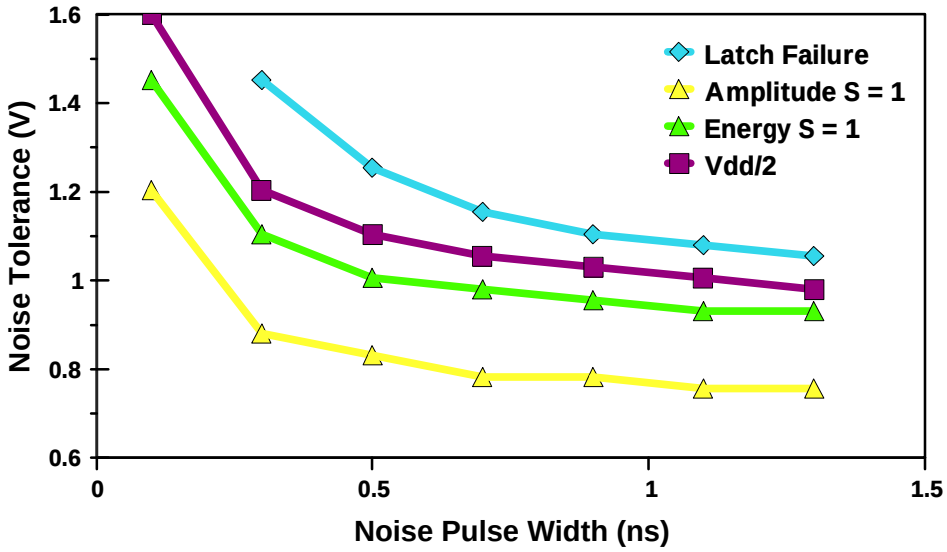
- Circuit failure criteria
  - functional
  - timing
- Noise sources and evaluation techniques
  - coupling
  - common mode
  - differential power supply
  - charge sharing
  - leakage
- Noise summation process
- Future tool needs

Circuit Noise Failure Criteria(functional)

- Data corruption at storage node
  - non-recovering circuits
    - dynamic nodes
    - latches
  - exceed circuit noise margin
- Noise margin definitions
  - AC noise margins
    - set/reset latch
    - sensitivity criteria
      - $\Delta\Phi out(t)/\Delta\Phi in(t)$
        - amplitude
        - energy
        - etc.



Latch



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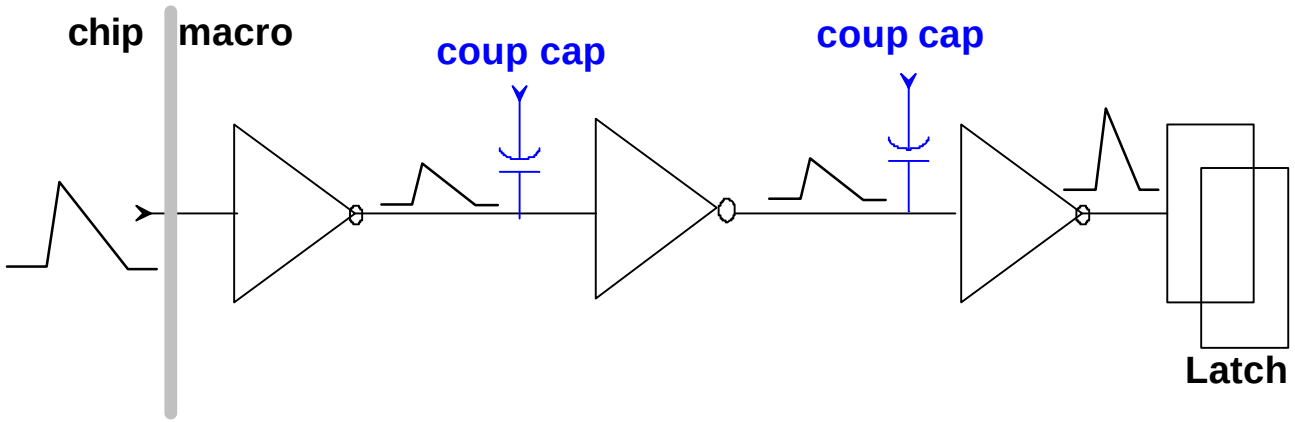
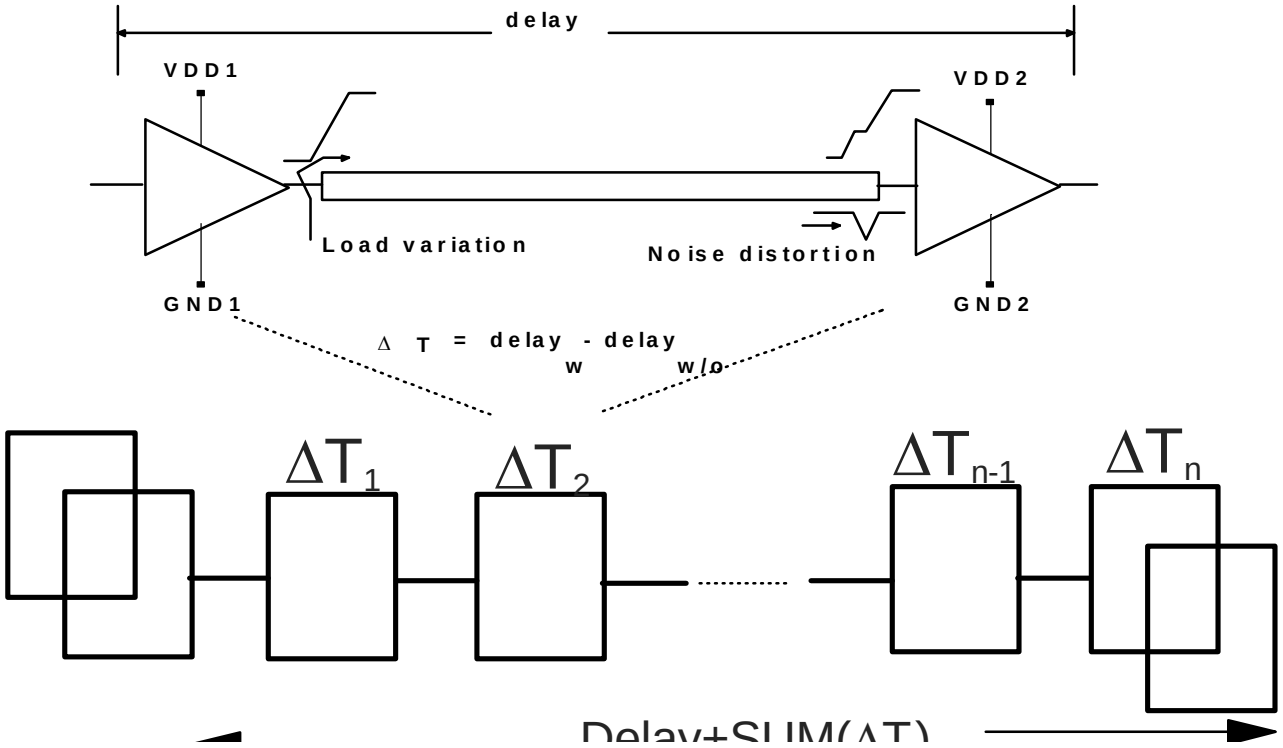
Circuit Noise Failure Criteria(functional)

- Path evaluation
  - stage to stage noise propagation
    - circuit based noise margins conservative
    - "static" noise verification technique
      - noise injection @ circuit input
        - summation of noise sources
      - noise propagation @ circuit output
  - transistor based simulations
  - tools: IBMmlsa(IBM internal), CADMOS



Circuit Noise Failure Criteria(Performance)

- Net based noise jitter effects
  - delay variations(ΔT) due to net coupling and/or power supply noise
    - rise time distortion at receiving circuit
    - load variation at driving circuit
    - wire delay variations
- Noise Jitter accumulates through logic stages in a path



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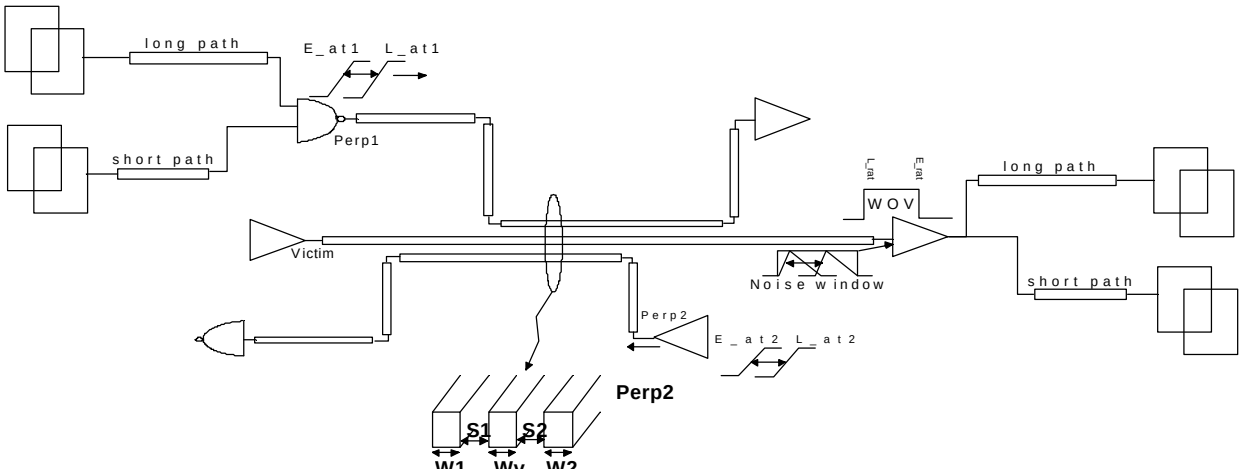
Coupling Noise

- RC coupling
  - high wire resistance
  - 90% of net population
- RLC coupling
  - RC model error > 20%
    - R*L / 2*Zo <~ 1.5
    - Z_{drv}*Ct < 3*R*C*L^2/2
  - frequency dependent RLC
    - proximity effects
  - time and noise critical nets
- Multiple coupling interactions
  - horizontal and vertical
- Timing dependency
  - noise source alignment
  - quiet net susceptibility window(WOV)



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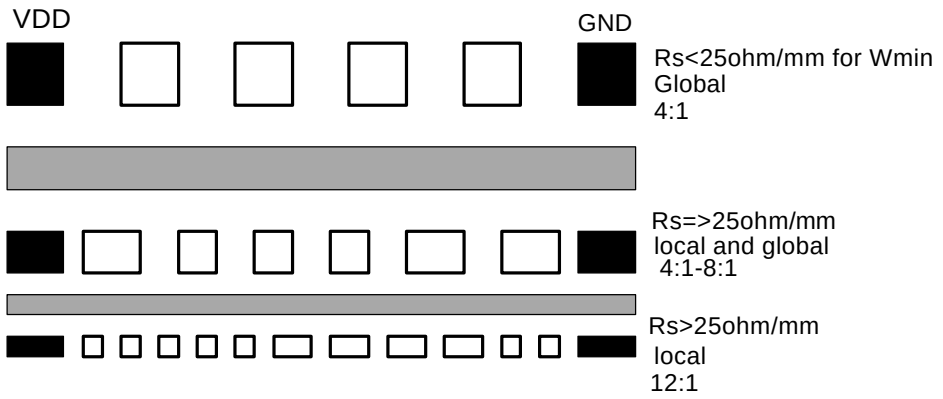
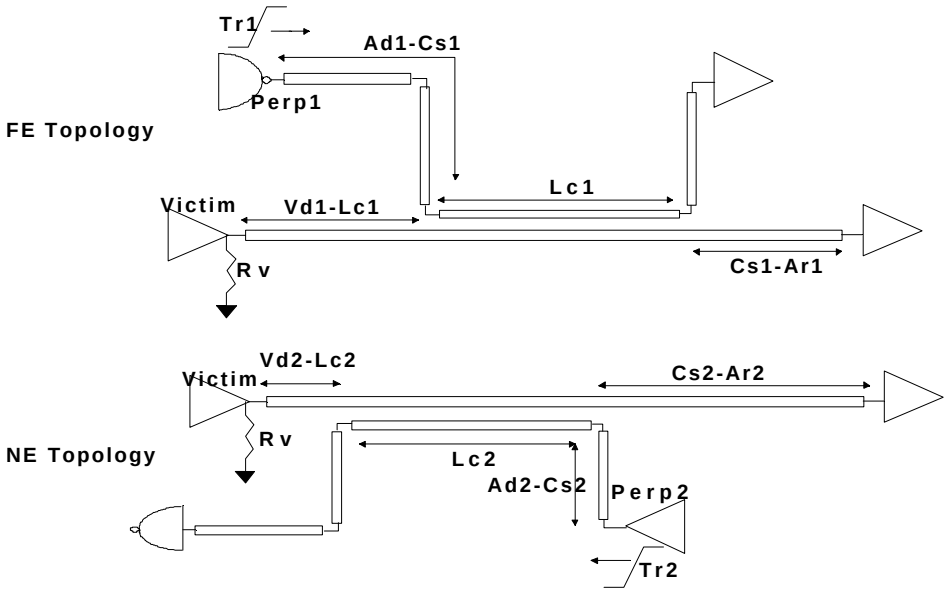
Coupling Noise Evaluation Dependencies

- Geometric
  - BEOL
  - power distribution
    - signal to power ratio
  - signal wiring patterns
- Coupling length
- Coupling location
- Net topology
  - signal direction
  - 1-drop, 2-drop, etc
    - capacitive loading
- Drive Strength
  - victim drv res
  - perp rise time
- 10-20x variation in noise level for a given coupled length





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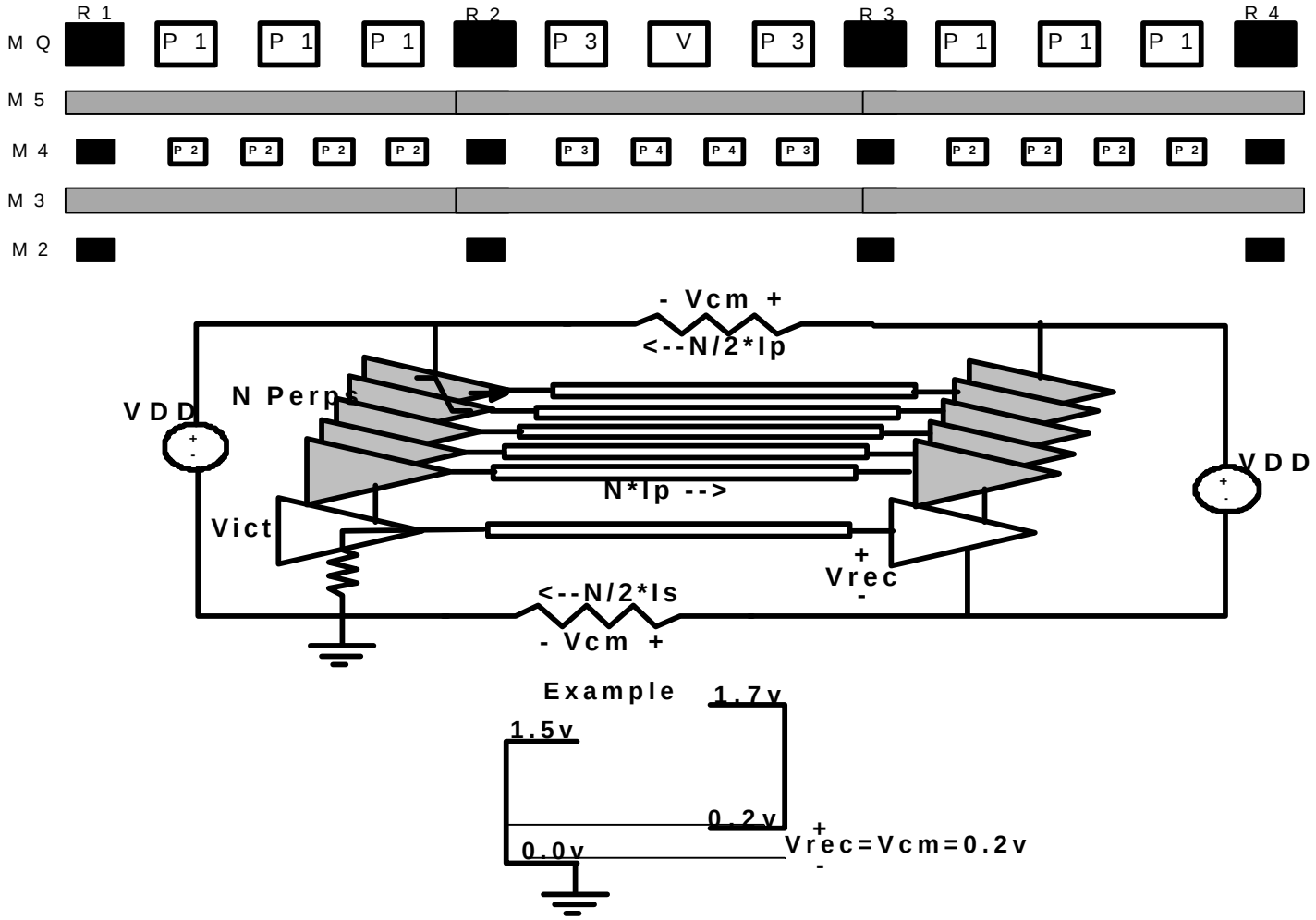
Common Mode Noise

- Drv to receiver voltage offset
  - Induced and displaced currents through resistive return path, $R_{ij}(f)$



Coupling and Common Mode Noise Evaluation Techniques

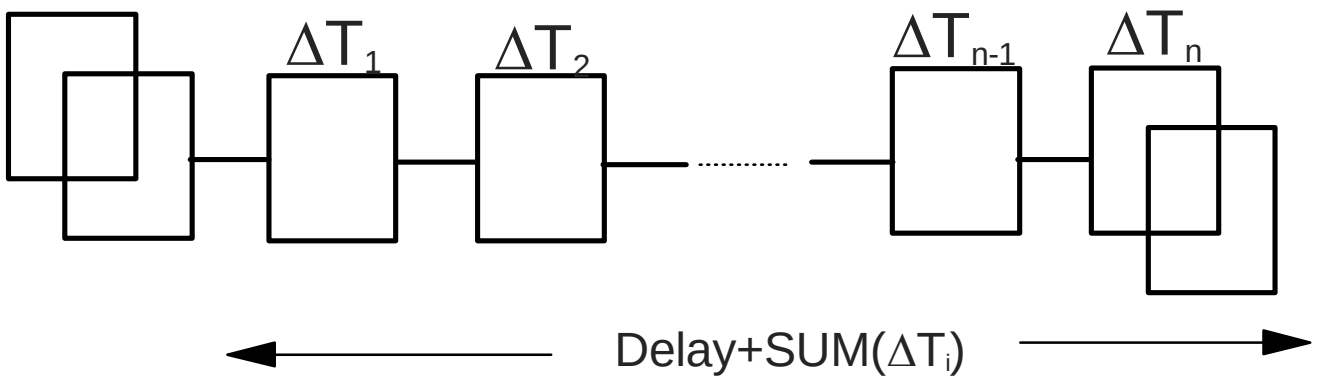
- Global level extraction (+200k nets)
  - RLC based
    - 3D capacitance
      - equations or table based
        - 10-15% error w.r.t. field solver solutions
        - Dynamic cap table build via field solvers(Rapheal, C2D)
    - 2D-R(*f*)L(*f*)
      - Extraction radius
        - narrow local coupling
        - wide for CMN? --> data volume issue
      - field solver or equations, i.e. Grover
        - PEEC, filament element
      - MOR or circuit synthesis for time domain simulations
  - Turn around time(TAT)
    - Production level performance
      - <8hrs
    - parallel processing techniques
  - Tools: 3DX(IBM internal), Columbus

Coupled and Common Mode Noise Evaluation Technique

- Coupling topology netlister
  - complete network representation of victim and aggressor nets
  - RLC circuit simulations using linear circuit solvers
    - parasitic data
    - pin capacitances
    - drv impedance/slews
      - linear model representation
  - peak noise @ receivers
    - superposition of noise sources based on timing overlap
  - functional fail criteria for a net
    - peak noise > noise limit within WOV
  - Tools: 3DNoise(RLC chip level, IBM internal), IBMmlsa(RC macro level, IBM internal), CADMOS

Coupled and Common Mode Noise Evaluation Technique

- Path based noise jitter effects accounted for in static timing
  - Static RC coupling approach
    - Uplift C_{total} by $K*C_{ij}$
    - adjust windows
    - iterate
      - chicken and egg issue
  - RLC solutions ??
  - Tools: Einistimer(IBM internal)



Differential Power Supply Noise

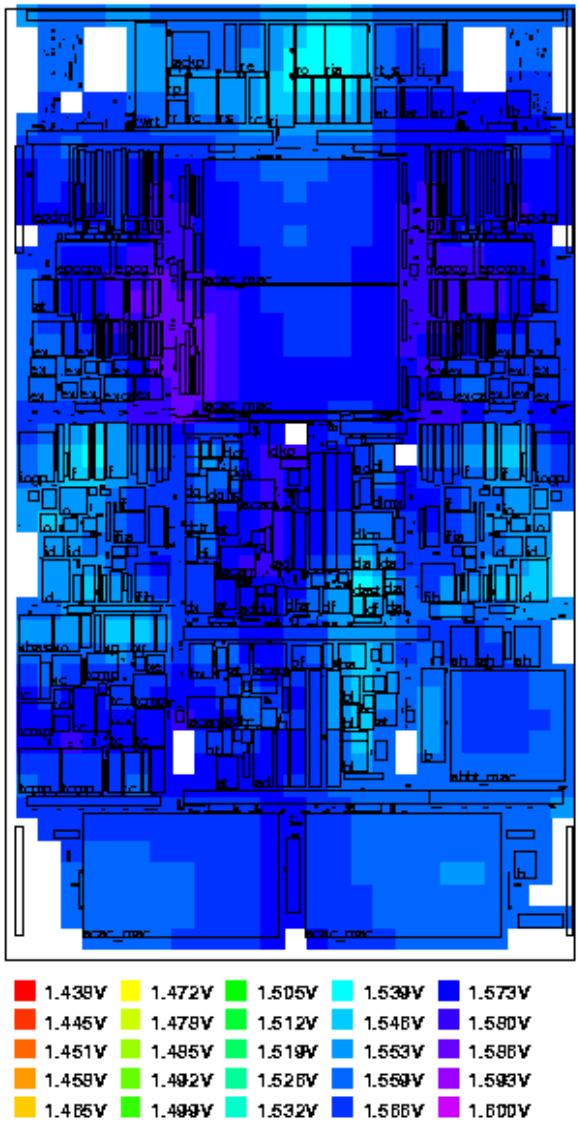
- Local and global power supply disturbance
  - IR drops
    - resistive power grid model
    - avg power assumption @ macro level
  - high frequency response
    - RL power grid model, on-chip capacitance
    - macro level transient load currents
  - load variations through resonant structures
- Resonance response
  - factored against DC operating condition
  - chip/package interface ~ 100 mhz
    - package inductance, on-chip capacitance
  - 1st/2nd level pkg design ~ 1-50mhz
  - Regulator Feedback --> 1khz - 1mhz
- High frequency response
  - circuit noise margin penalty
    - noise budget component

Differential PS Noise Evaluation Technique

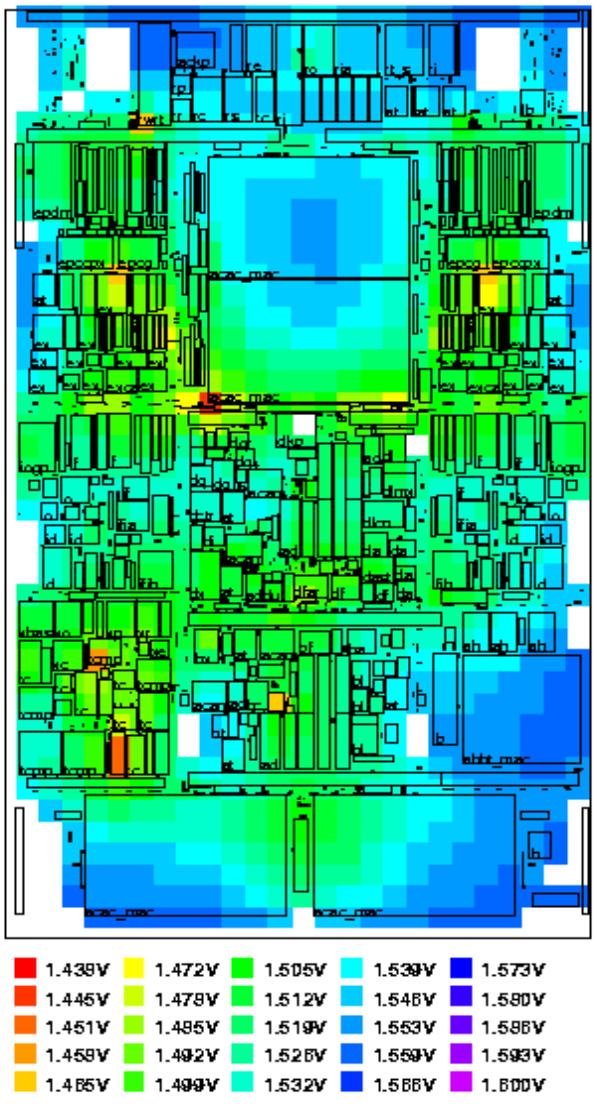
- Full chip evaluation process
  - RL segment models of chip power grid
    - coalesce power grid shapes to reduce model size
    - independent calculation of loop inductance via field solvers
  - VDD-GND current sources to represent circuit Loads
    - vector based power calculator for each macro/circuit
      - fast circuit simulations using piece wise linear device models
  - intrinsic capacitance(gate, nwell, wire) estimation from layouts
    - area/perimeter calculations
  - added decaps projected into model from chip floorplan
  - evaluation performed using fast linear simulator techniques
- Evaluation yields
  - VDD-GND collapse
    - chip/pkg resonance (when pkg model included)
    - high frequency noise
  - decap effectiveness
- Tools: NOVA, RAPID and ALSIM(IBM internal), Simplex, etc.

Differential PS Contour Map

On-Chip Vdd Distribution (T = T0 + 13.30 ns)



On-Chip Vdd Distribution (T = T0 + 13.70 ns)



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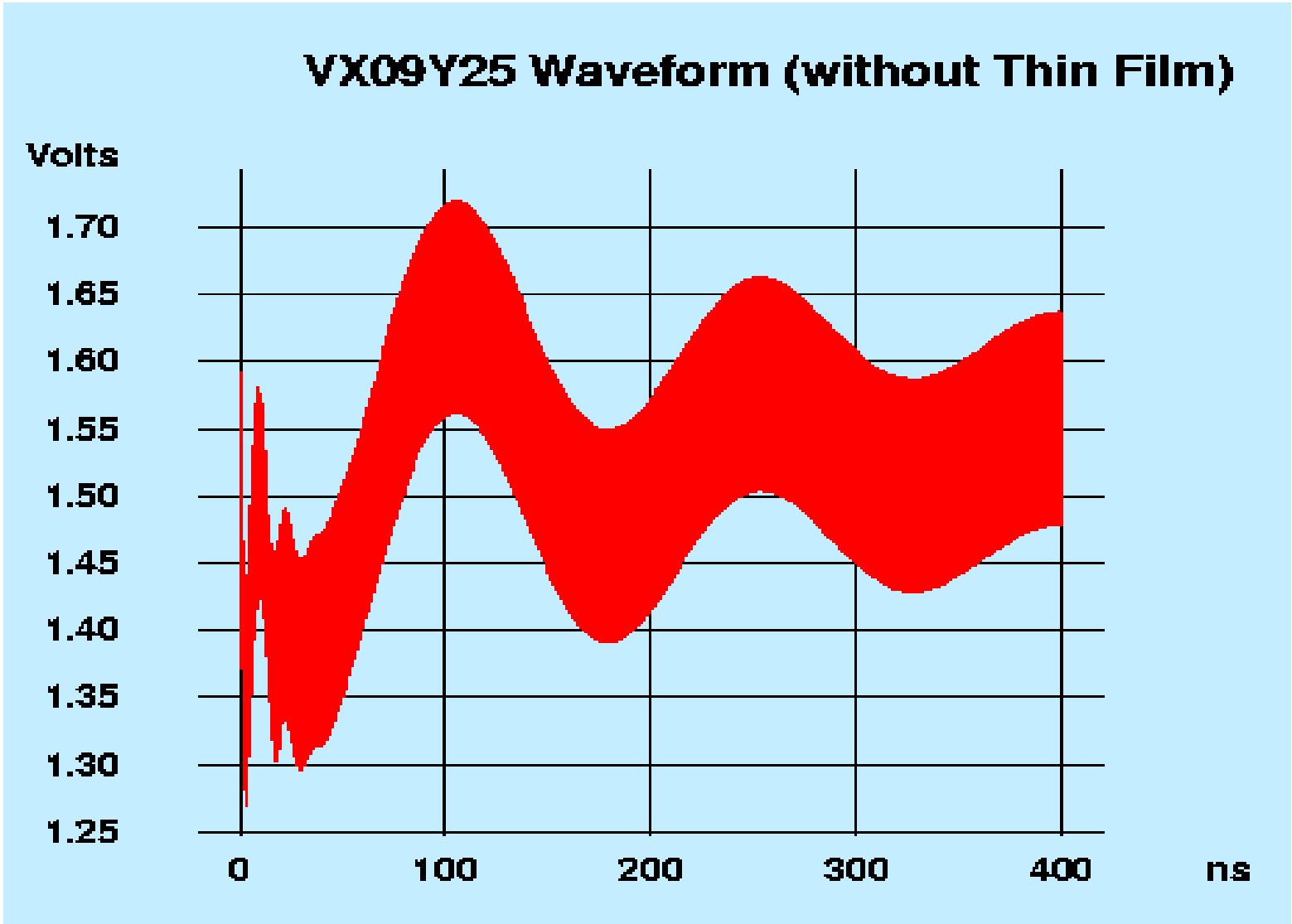
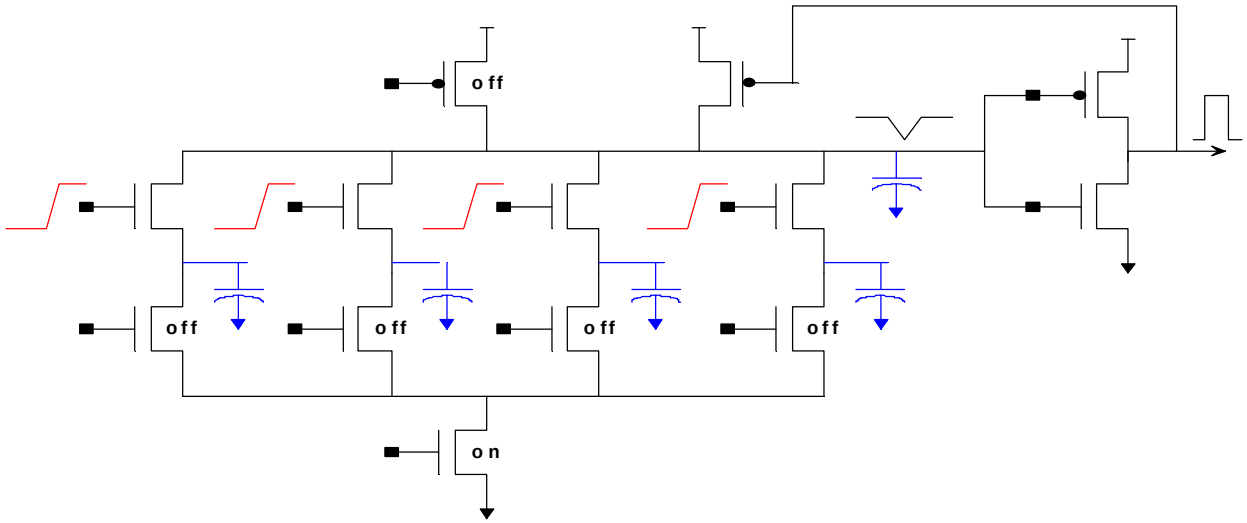

VX09Y25 Waveform (without Thin Film)
Volts
1.70
1.65
1.60
1.55
1.50
1.45
1.40
1.35
1.30
1.25
0
100
200
300
400
ns

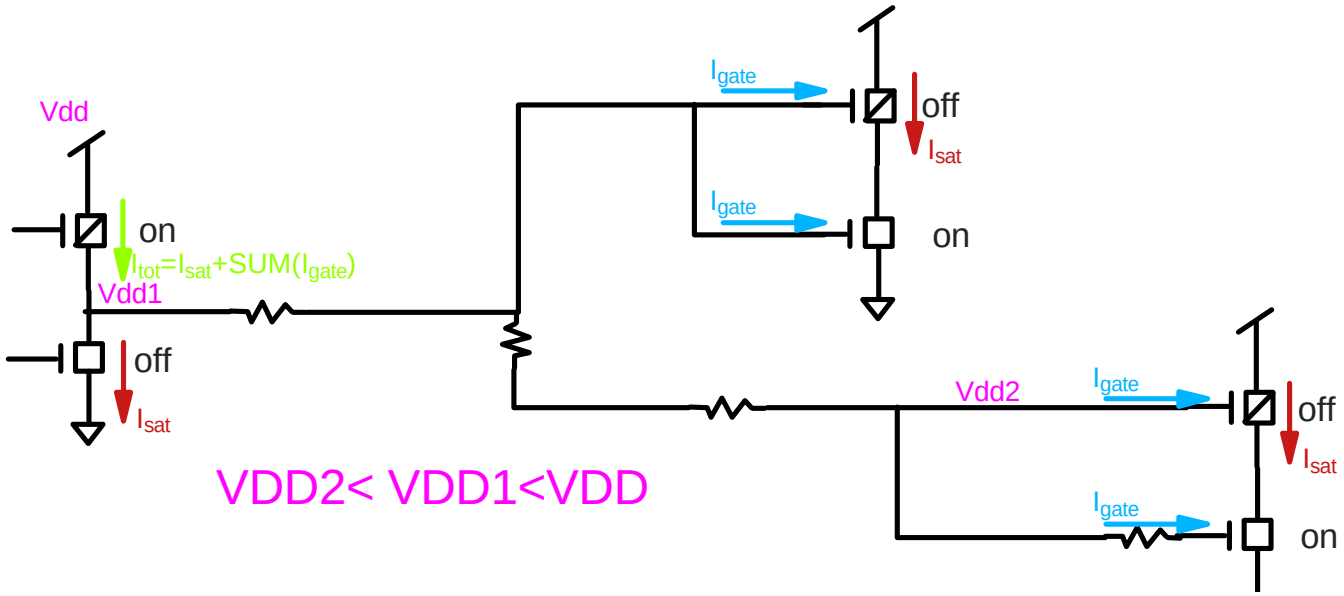
Charge Sharing

- Charge redistribution within internal circuit nodes
  - circuit design dependent
    - dynamic or weak static node
    - stacked devices
- Transistor level simulations
  - piece wise linear device models to decrease evaluation time
  - circuit topology recognition
    - input pattern dependency
  - Tools: IBMmlsa(IBM internal), CADMOS



Circuit Leakage

- Device Leakage due to deep sub-micron scaling
  - Lower subthreshold voltage increasing I_{sat}
    - inverse temp dependency, manufacturing variations
  - Thinning gate oxide --> "tunneling effects" increasing I_{gate}
- Leakage biasing of circuit levels reduces circuit noise margins
- Transistor Level simulations
  - accurate device modeling in subthreshold region??
  - Resistance extraction of signal wires
- Tools: IBMmlsa(IBM internal), CADMOS?



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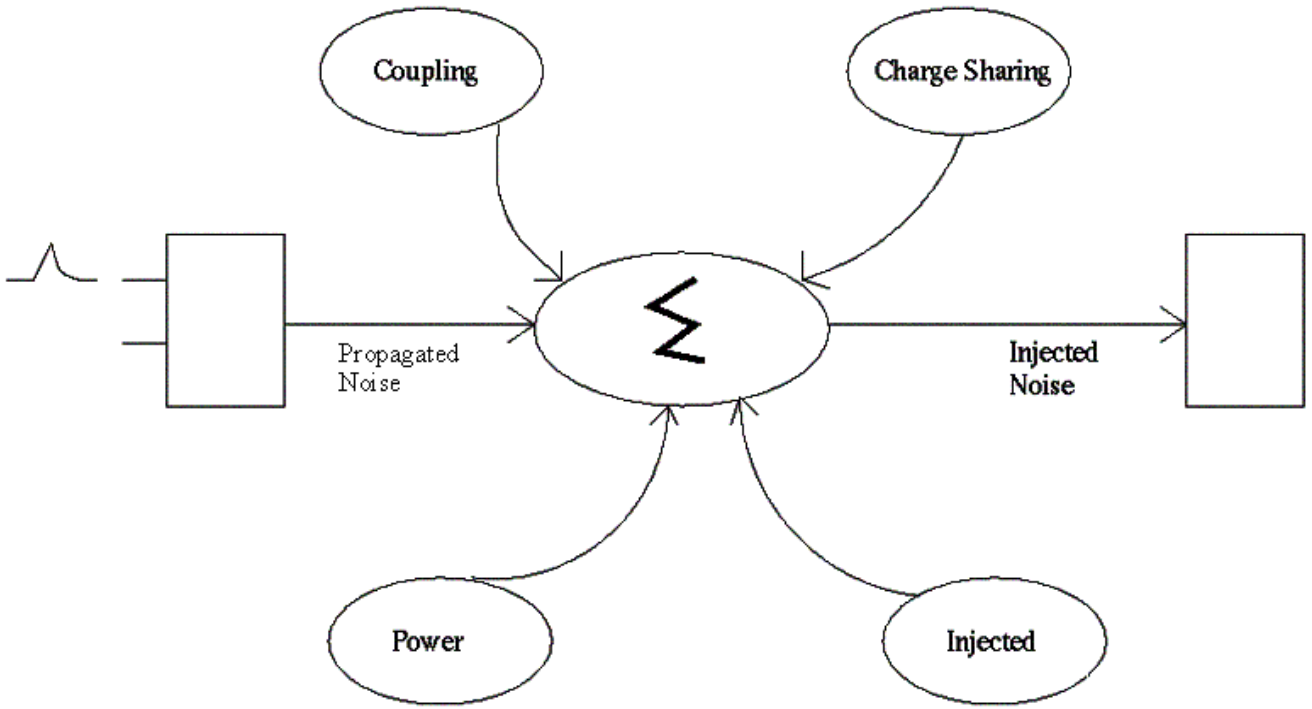
Summation of Noise Sources in Digital Circuits (Noise Budget)



- Summation of quasi independent calculation processes

Future Tool Needs

- Full-chip R(*f*)L(*f*)C extraction process for comprehensive evaluation of coupling/common mode noise
  - efficient wide radius techniques
    - TAT
    - netlisting into simulator
      - MOR
- Combined noise and timing calculators
  - in-core timing information
  - common netlisting procedure
    - timing, functional noise, noise effects on timing
  - transistor and rules based approaches
    - Complete Interlock to account for all noise sources
  - fast non-linear simulation techniques

Future Tool Needs

- Combined evaluation of CN/CMN/PS interactions
  - current loop assumptions inconsistent at circuit ports
    - zero VDD-GND impedance for CN/CMN
      - introduction of multiple power rails
        - discontinuous current return loops possible
    - VDD-GND current loop for PS
      - VDD or GND to Signal
  - Comprehensive R(*f*)L(*f*)C extraction and device level simulation of combined interconnect/PS problem " The Holy Grail ! "
    - full chip evaluation ??
      - device and parasitic extraction process
      - very fast circuit simulation capabilities
      - circuit switching statistics an issue
        - dynamic simulations
        - pattern dependency and switching times uncertainties
  - LEXSIM from Nassada satisfies some of the above requirements
      - Macro based
      - RC netlist reduction
      - fast circuit simulation