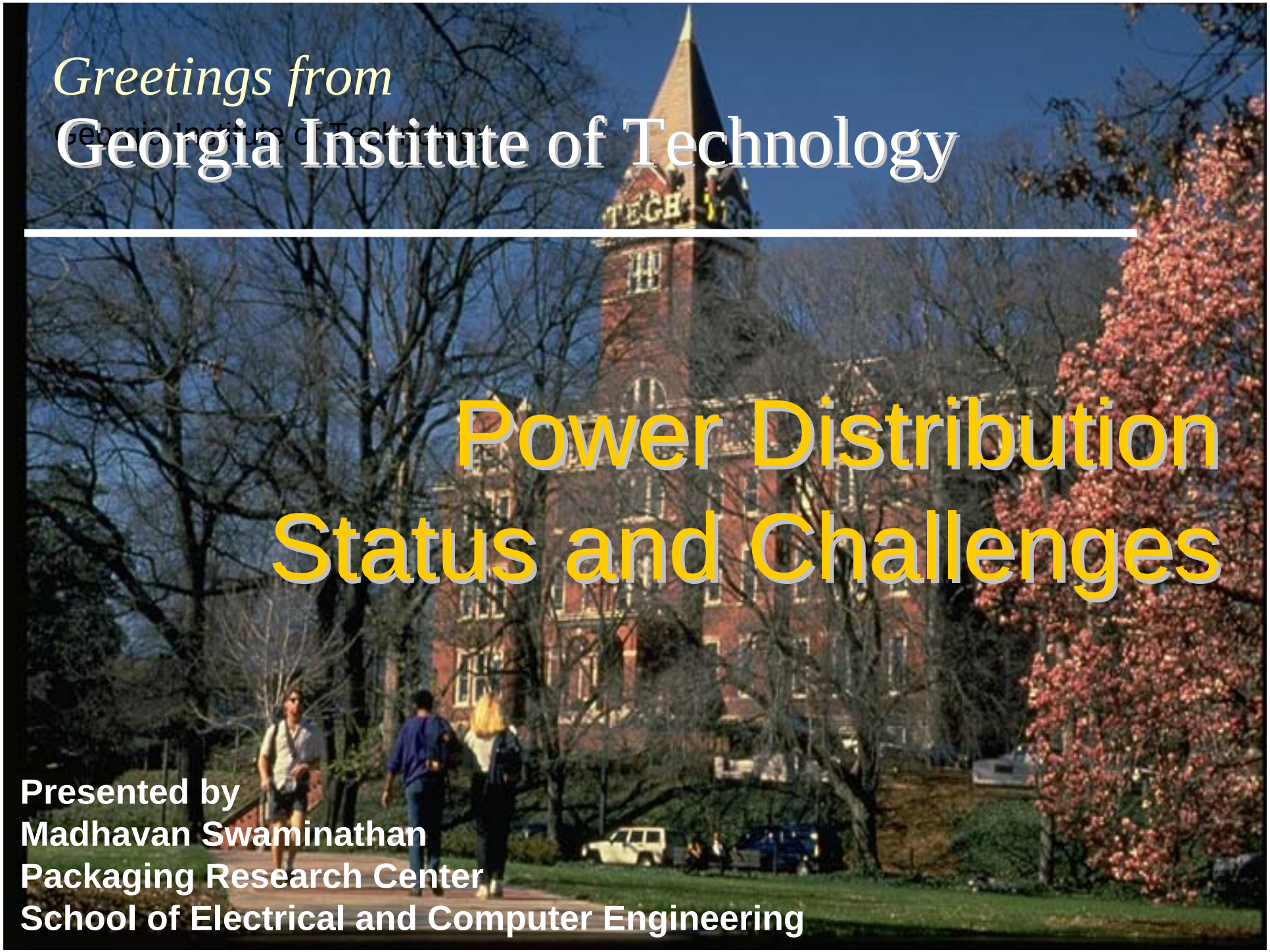

Greetings from
Georgia Institute of Technology
Power Distribution
Status and Challenges
Presented by
Madhavan Swaminathan
Packaging Research Center
School of Electrical and Computer Engineering

Acknowledgement

- Prof. Joungho Kim – KAIST, S. Korea
- Dr. Istvan Novak – SUN, USA
- Mr. James Libous – IBM, USA

Outline

- Introduction

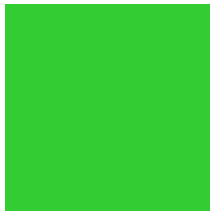
- Digital Systems
  - On-Chip
  - Package and Board
  - New Technologies

- Modeling
  - On-Chip
  - Package and Board

- Mixed Signal Systems
  - RF and Digital Integration

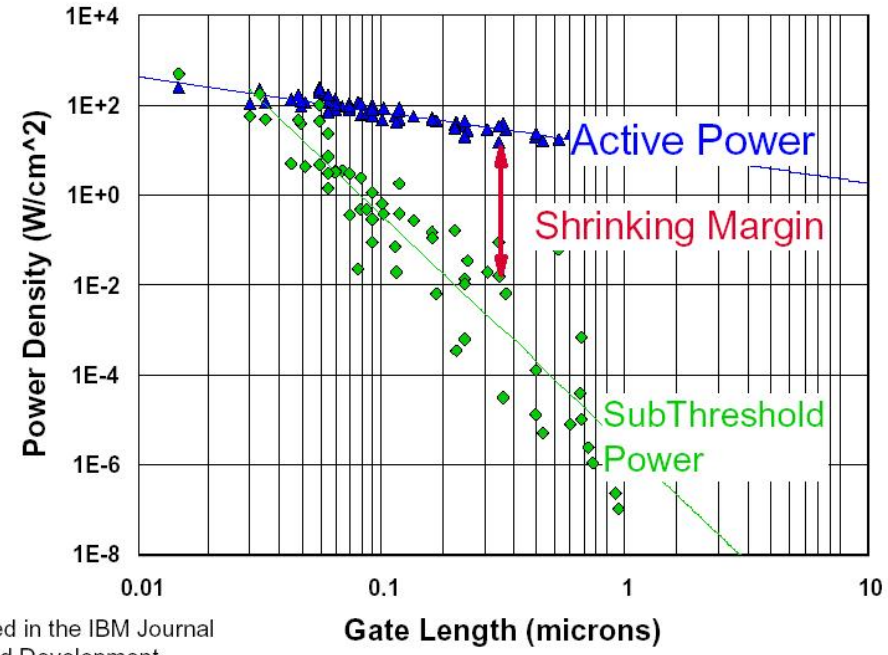
- Summary

Microprocessor Projections



μP 140 mm²

Device Leakage Power Density Increasing



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- In the past, CMOS **active power** was main concern with power delivery

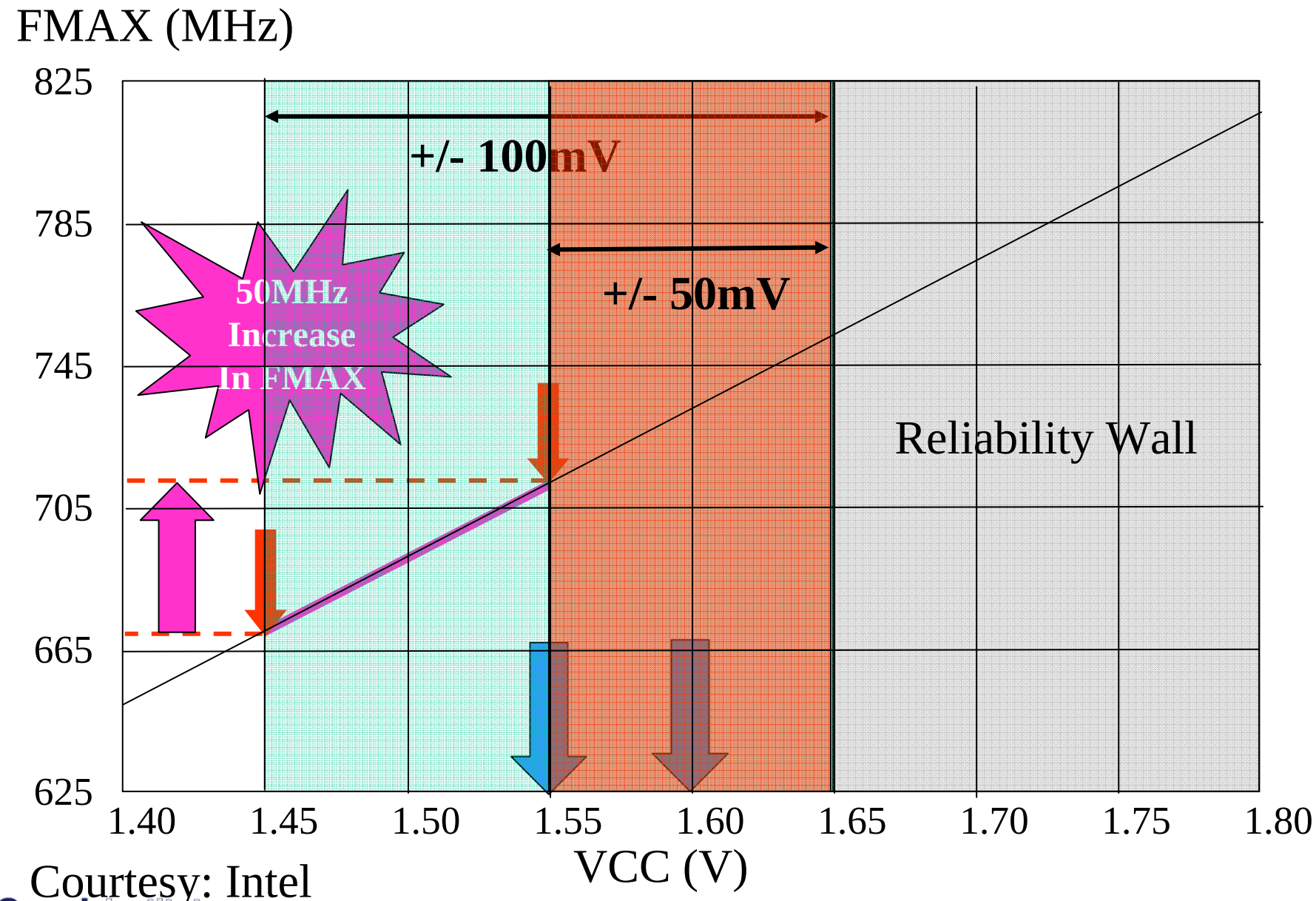
- As CMOS scales to below 90nm, process related device leakage current contributes a significant **passive power component**

-Leakage current can be reduced by using **high-k dielectric** materials as replacement for silicon dioxide as the gate dielectric

-**Passive power** puts a further strain on the on-chip power distribution system as it erodes the dc IR drop noise budget and compounds the EM problem

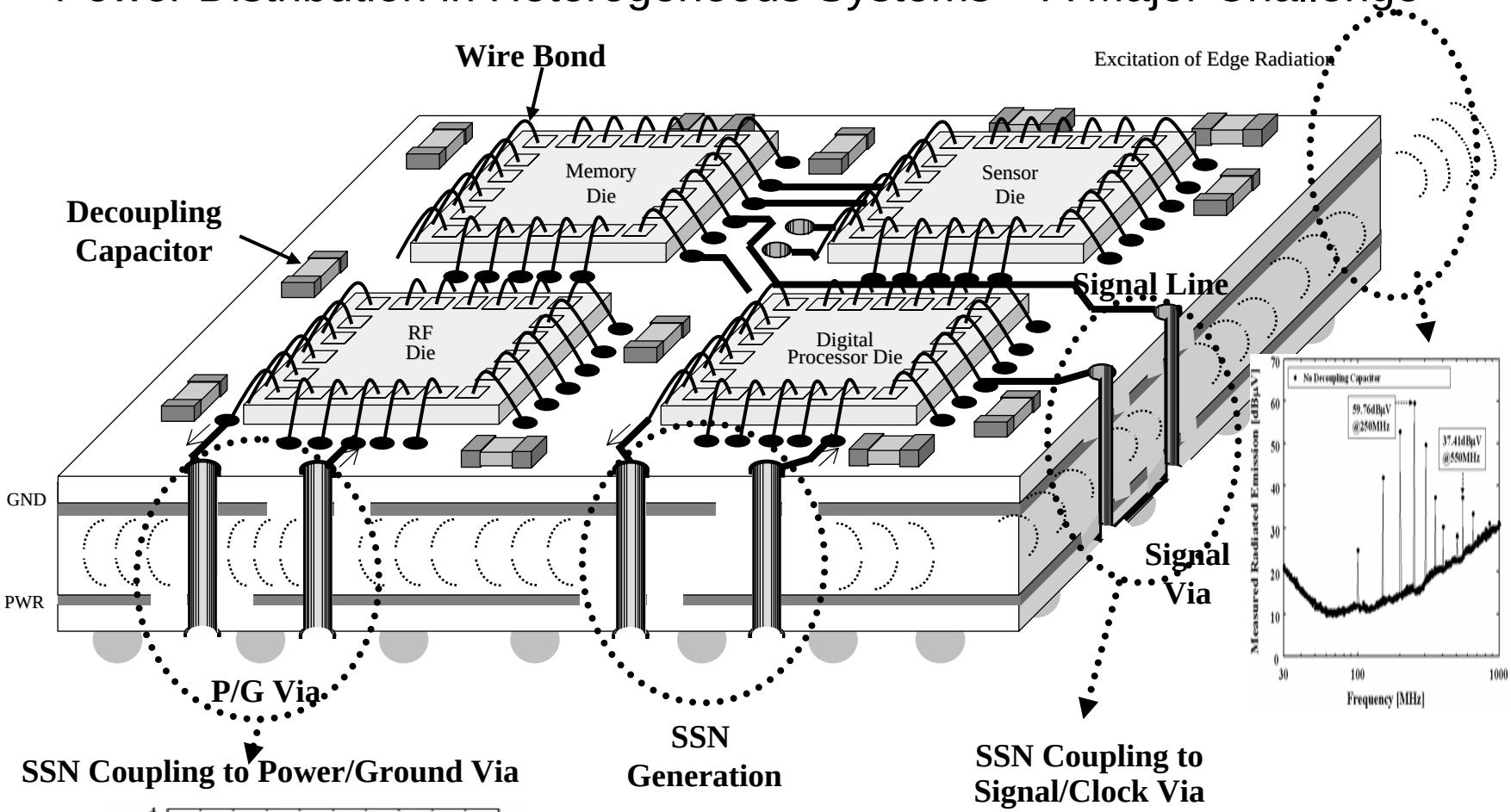
Courtesy: J. Libous, IBM

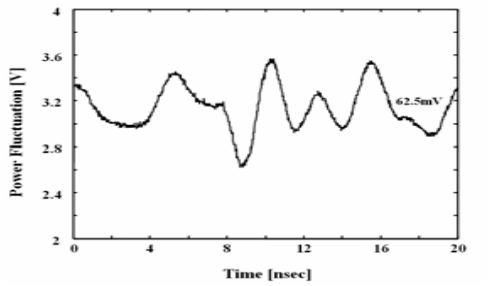
Importance of Power Distribution

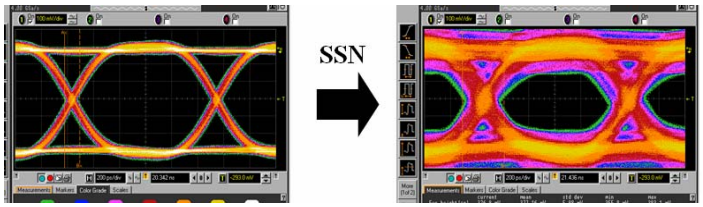


Courtesy: Intel

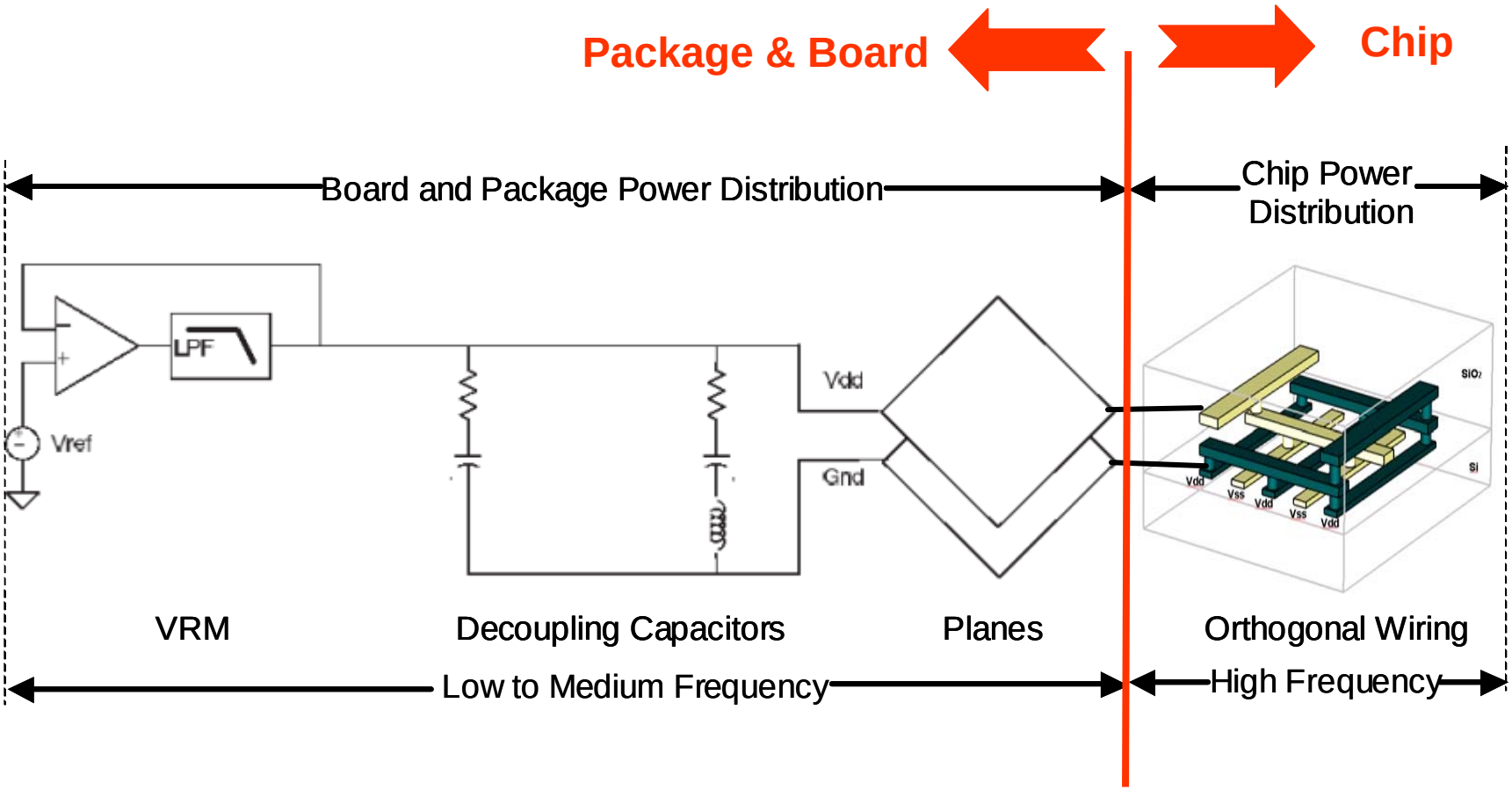
Power Distribution in Heterogeneous Systems – A Major Challenge







Power Distribution – DC to Daylight Problem



Chip – Package Co-design of Power Distribution is a necessity for Future Systems

Digital Systems

Power Supply Sensitivity

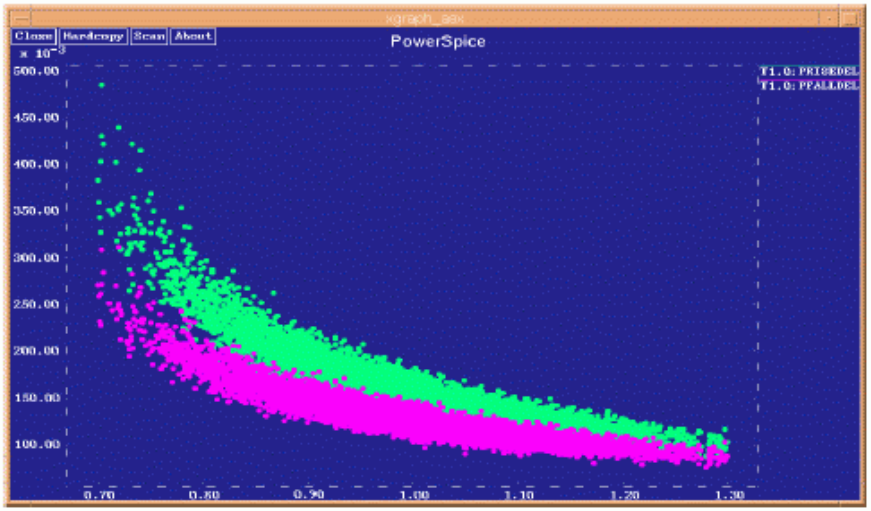
- Scaling reduces Vdd headroom (operating on a steeper part of the delay versus Vdd curve)

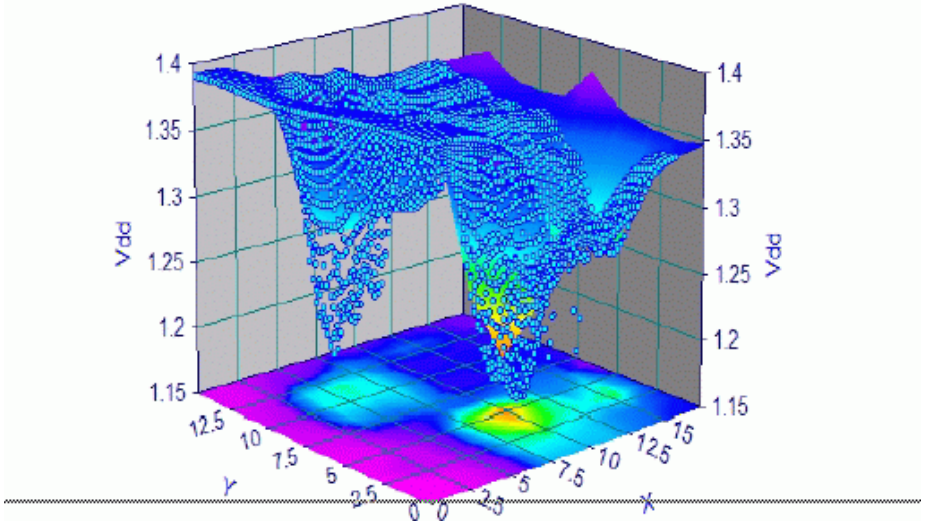
-As Vdd values drop and power densities increase, IR drop becomes more of an issue

-Instantaneous voltage drop and spatial variation must be analyzed and controlled

-On-chip decoupling capacitors used as local power source to handle instantaneous current demands

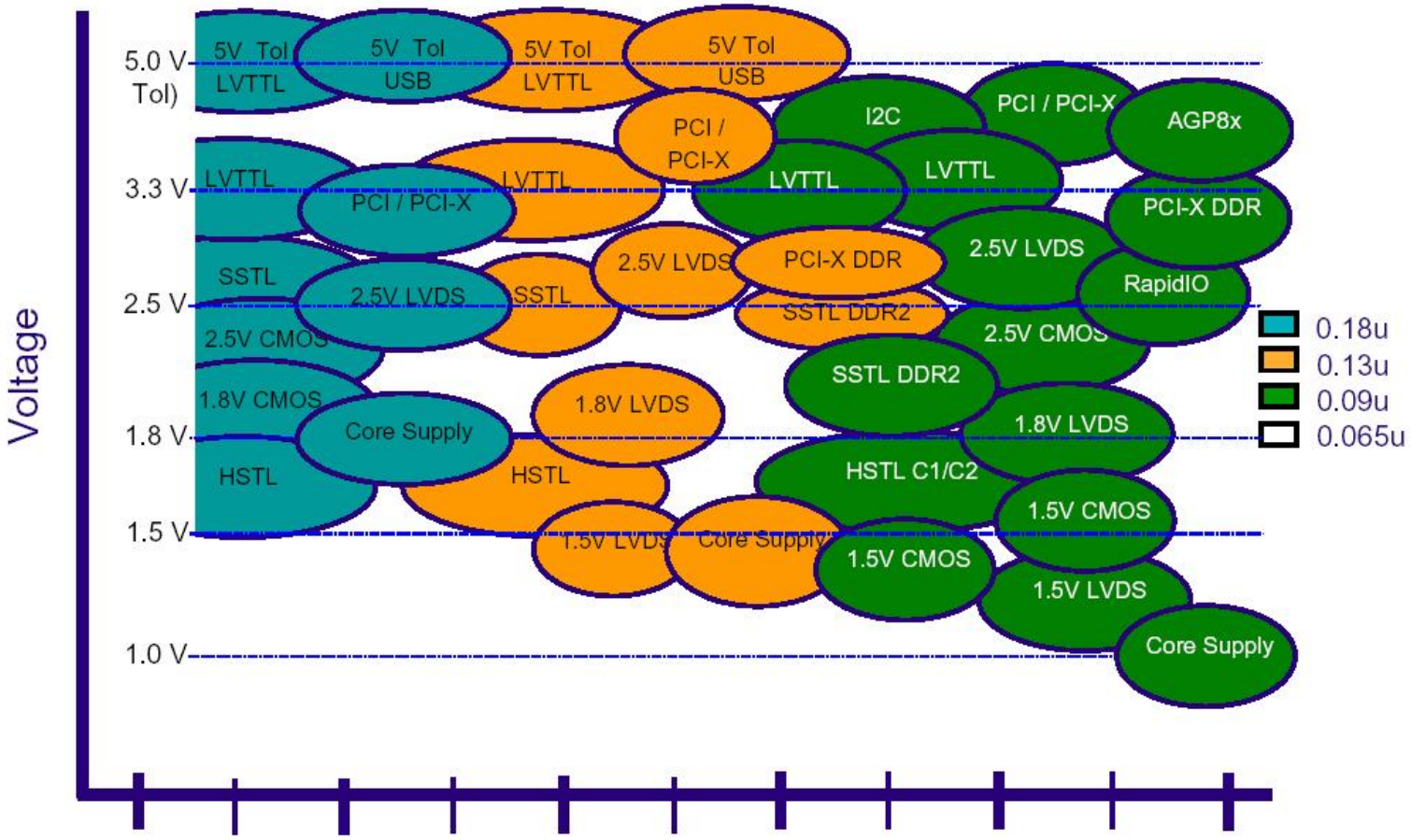
-Dcaps must be placed where needed and requires a thorough understanding of chip current demand prior to chip physical design





Courtesy: J. Libous, IBM

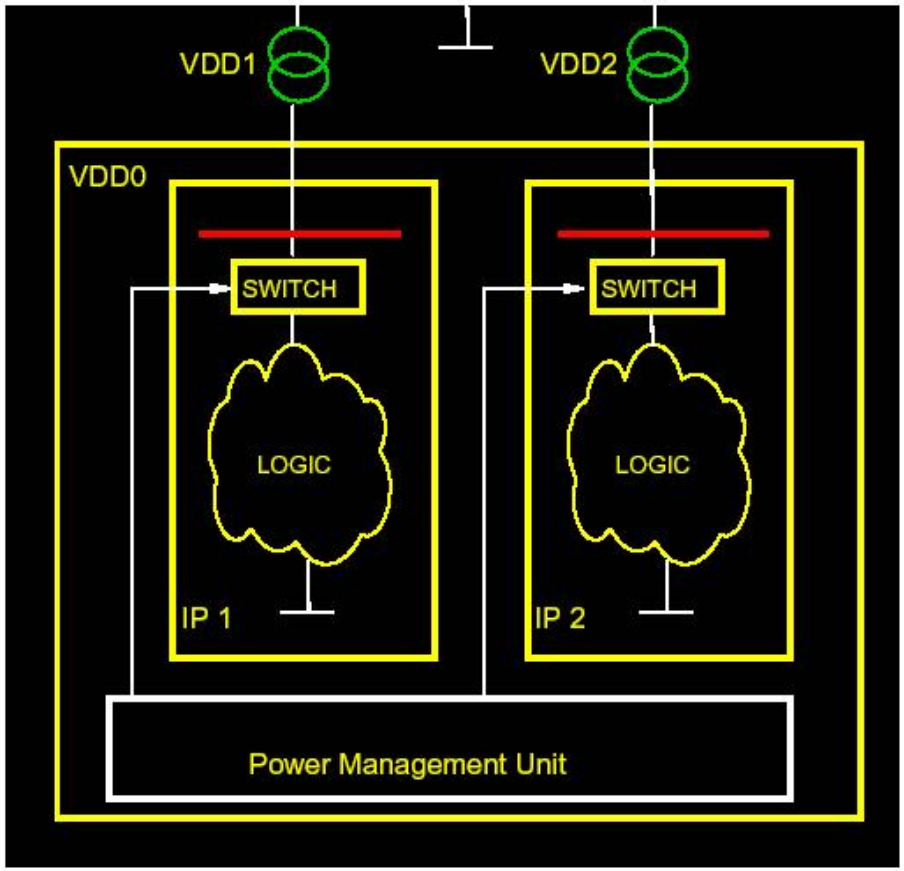
Legacy I/O Voltages Must Be Distributed along with Core Voltages



Courtesy: J. Libous, IBM

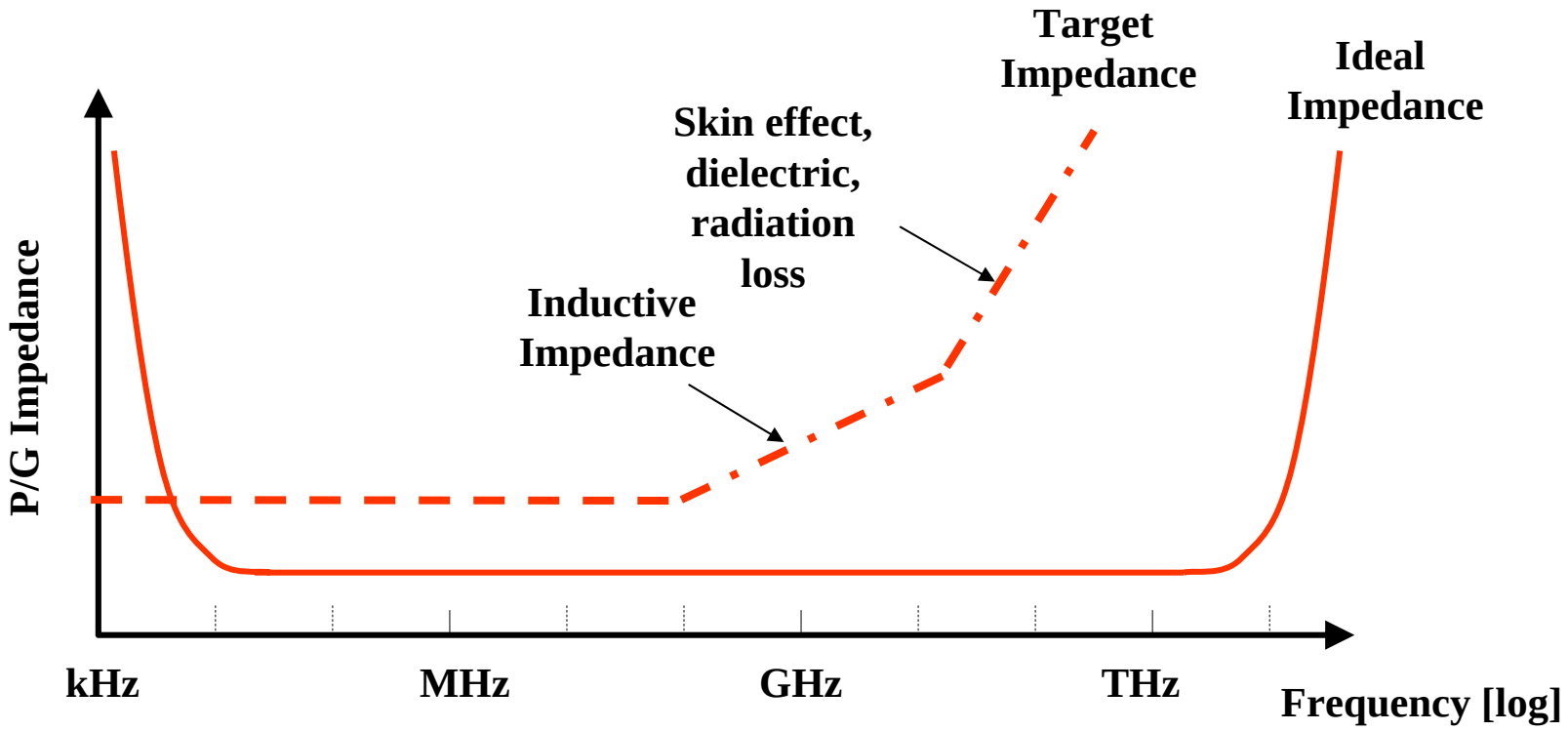
Voltage Islands and Power Domains

- Design approach to manage the active and passive power problem
- **Voltage Islands -** Areas on chip supplied through separate, dedicated power feed
- **Power Domains –** Areas within an island fed by same Vdd source but independently controlled via intra-island header switches
- **Distribution Challenges** – dcap isolation, transients due to activation & deactivation of islands, multiple supplies
- **Simple Concepts….. Complex methodology and design tools**



Courtesy: J. Libous, IBM

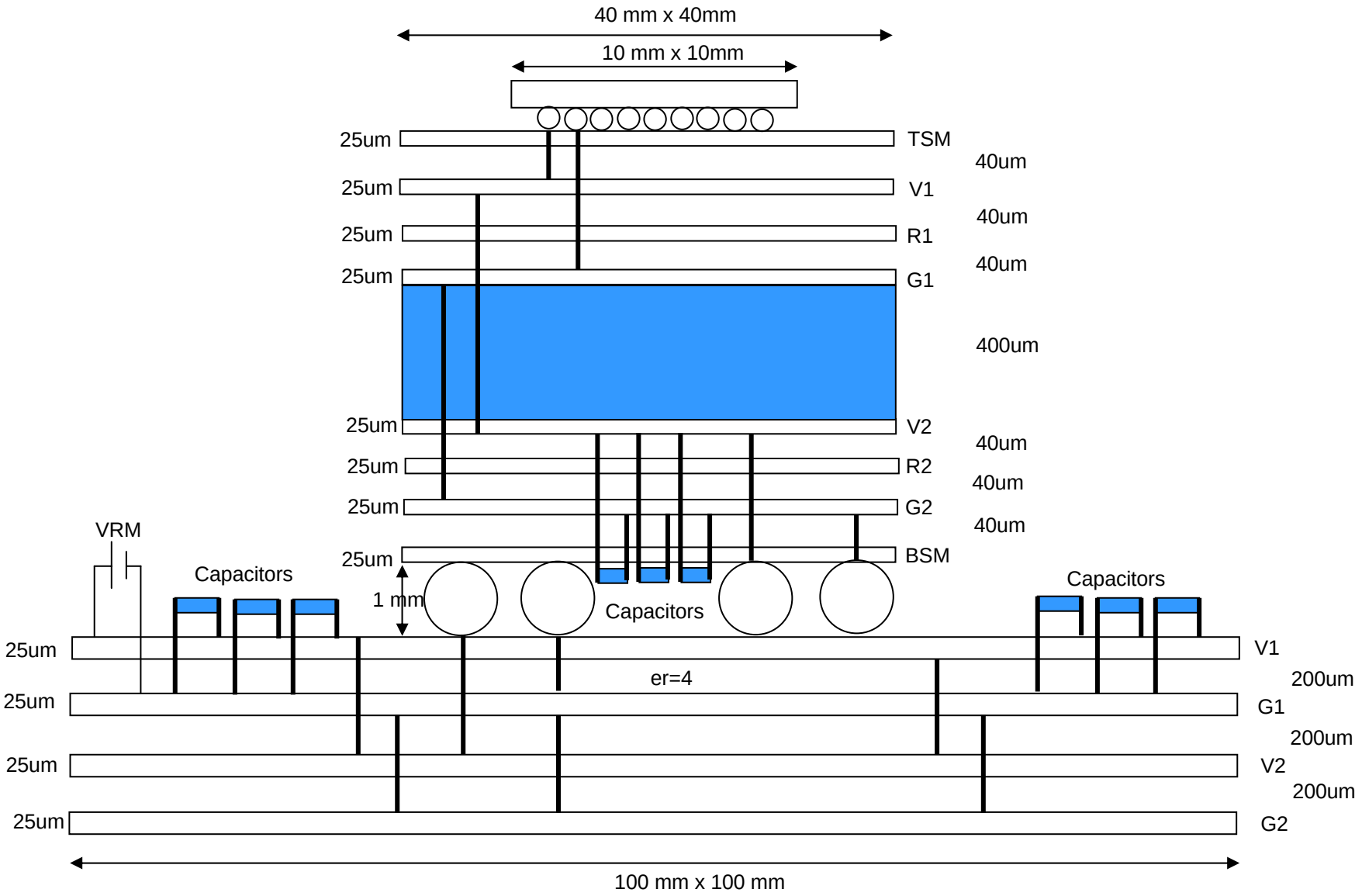
Target Impedance of Power Distribution Network



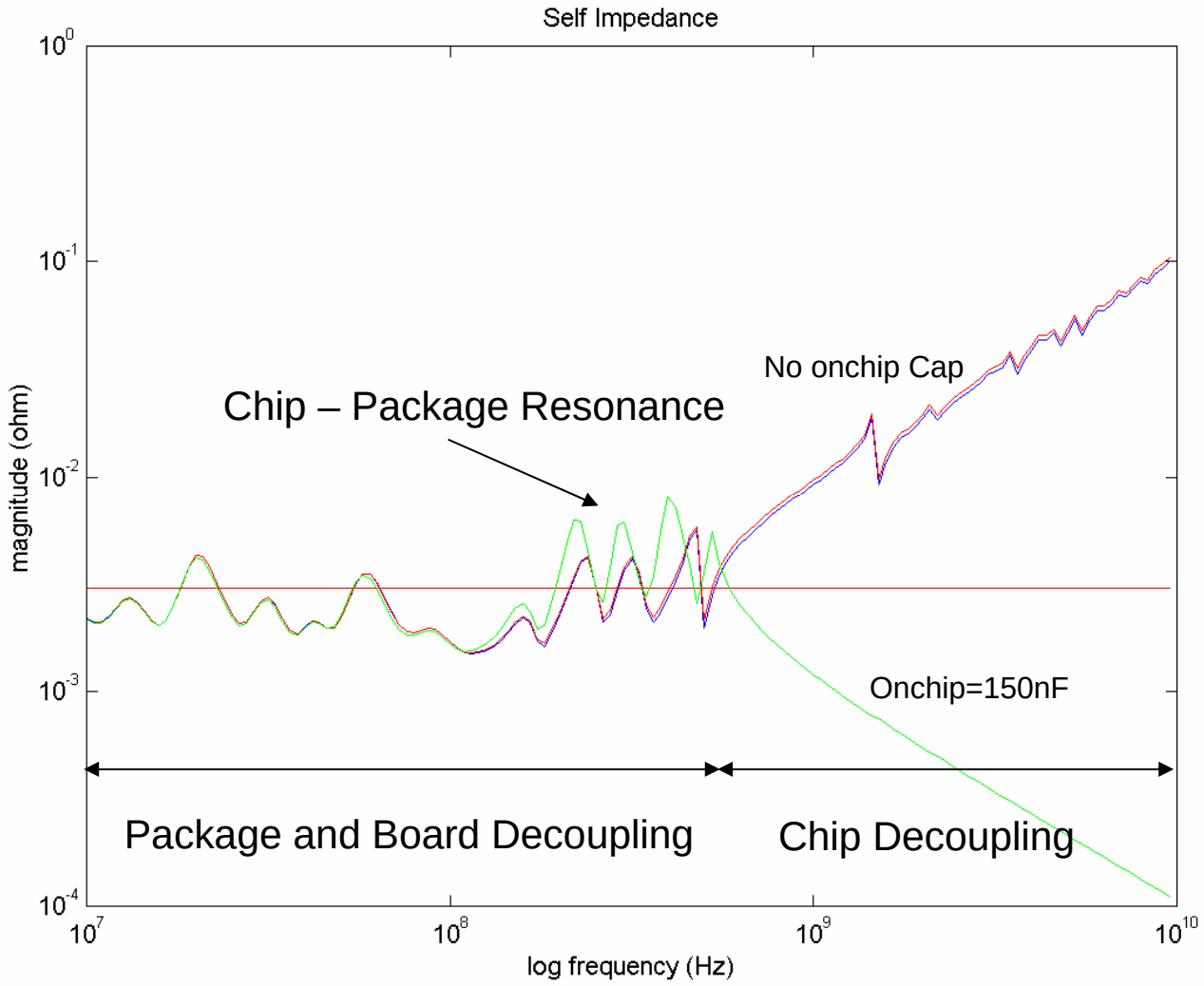
A concept becoming popular in the packaging community

Courtesy: J. Kim, KAIST

Package on Board

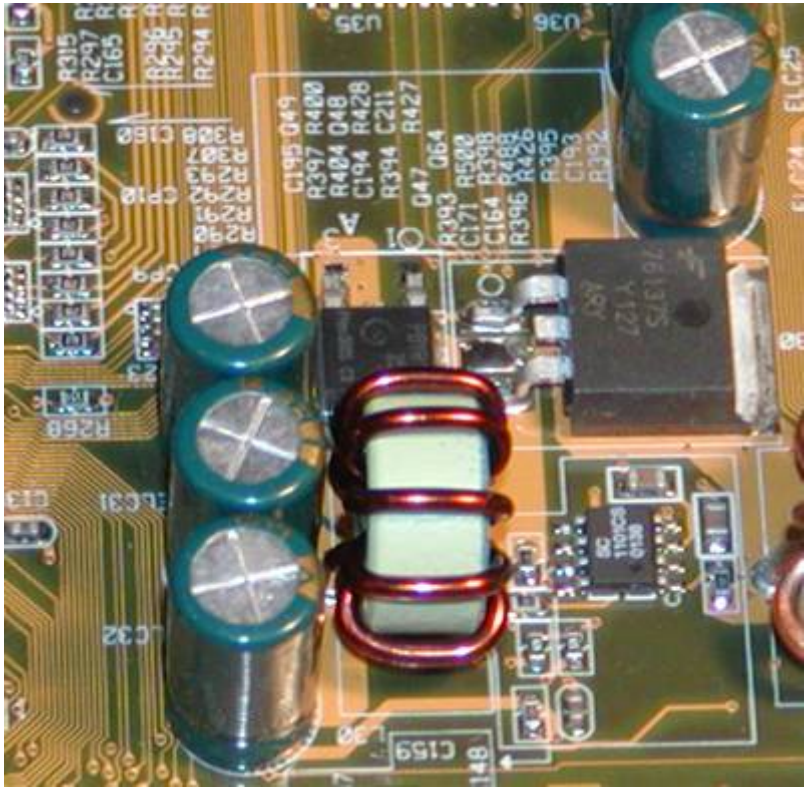


Impedance seen by Chip on Package With Capacitors



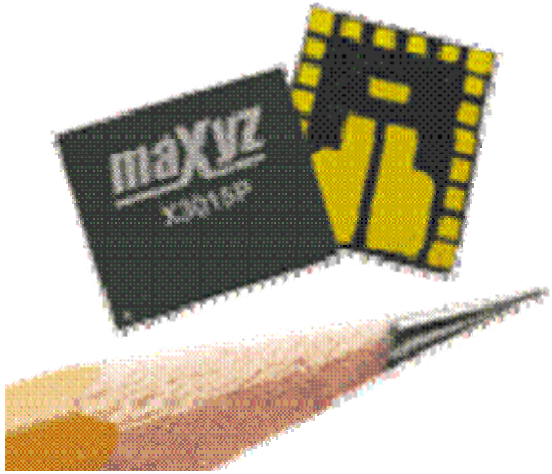
Modeling Results

DC-DC Converters
State of the Art



POL converter in PC

Courtesy: I. Novak. SUN



12x10mm 15A POL converter.
Source: www.power-one.com

SI parameters:

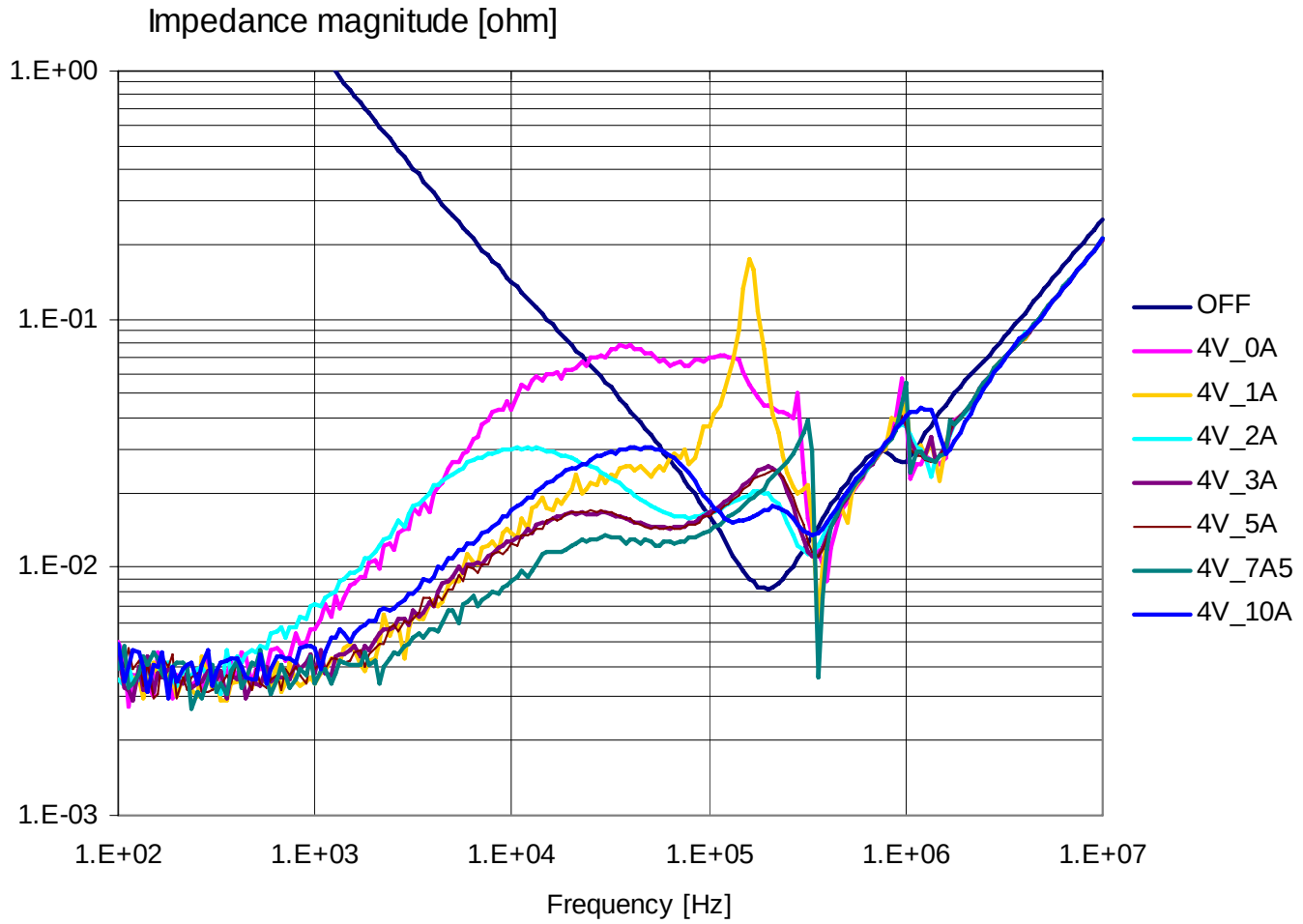
Z_{out}, Z_{in}, V_{out}/V_{in}

Output ripple

Loop stability

Large-signal response

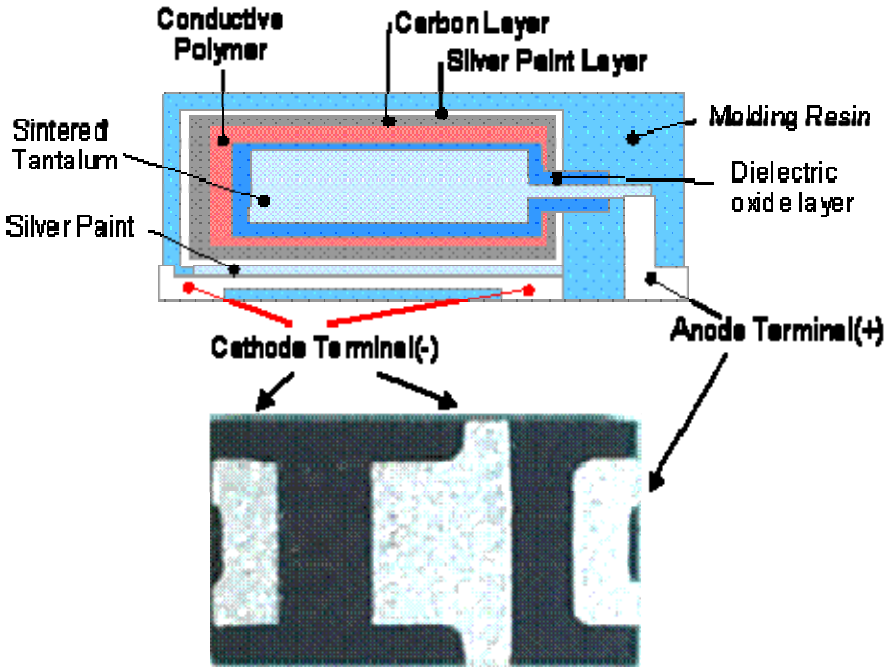
Potential Low-Frequency Problem:
Peaky/Changing Output Impedance

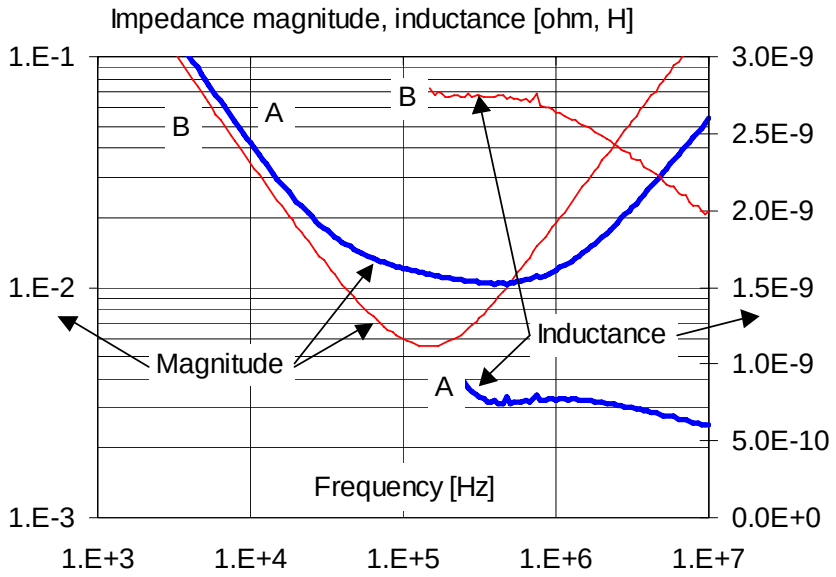


Courtesy: I. Novak. SUN

Bypass Capacitors
State of the Art, Bulk Capacitors

Face-down, low-inductance, low-ESR, low-profile, D-size polymer tantalum capacitor (curves A on the impedance plot)



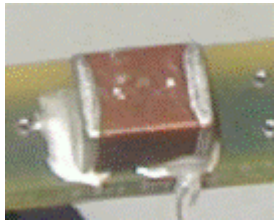


"Overview of Some Options to Create Low-Q Controlled-ESR Bypass Capacitors," Proceedings of EPEP2004, October 25-27, 2004, Portland, OR

Courtesy: I. Novak. SUN

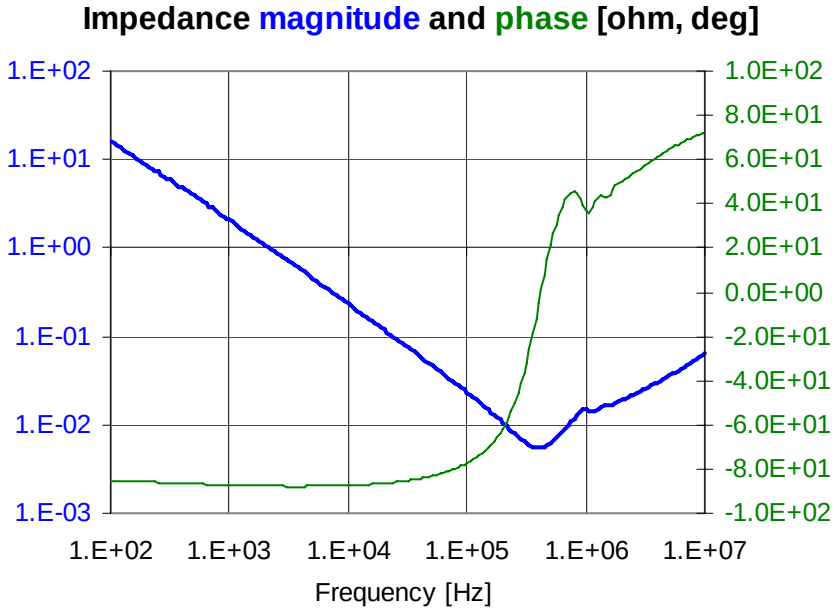
Bypass Capacitors

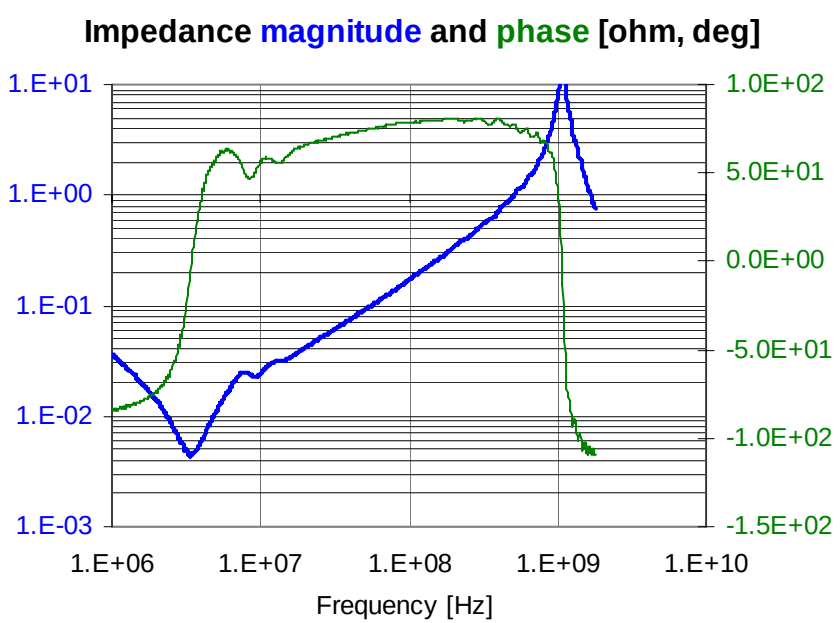
State of the Art, Two-terminal Ceramic Capacitors



1210 100uF

0508 4.7uF
reverse geometry

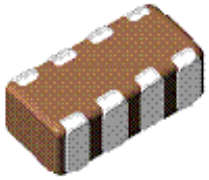




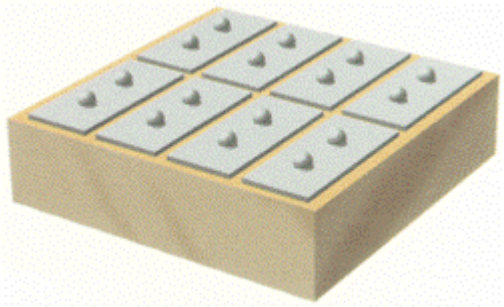
Courtesy: I. Novak. SUN

Bypass Capacitors
Multi-terminal Ceramic and Film Capacitors

Multi-terminal capacitor

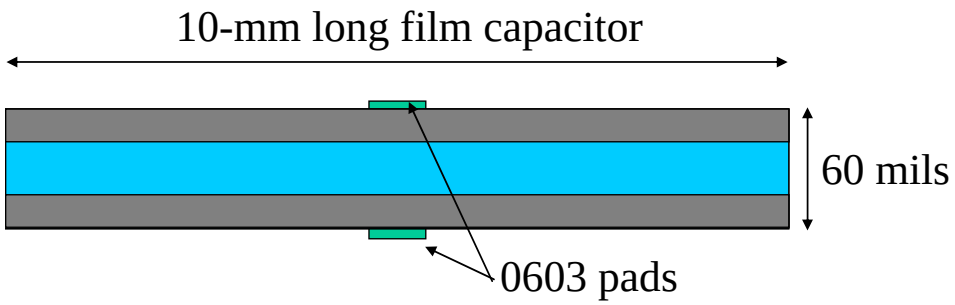


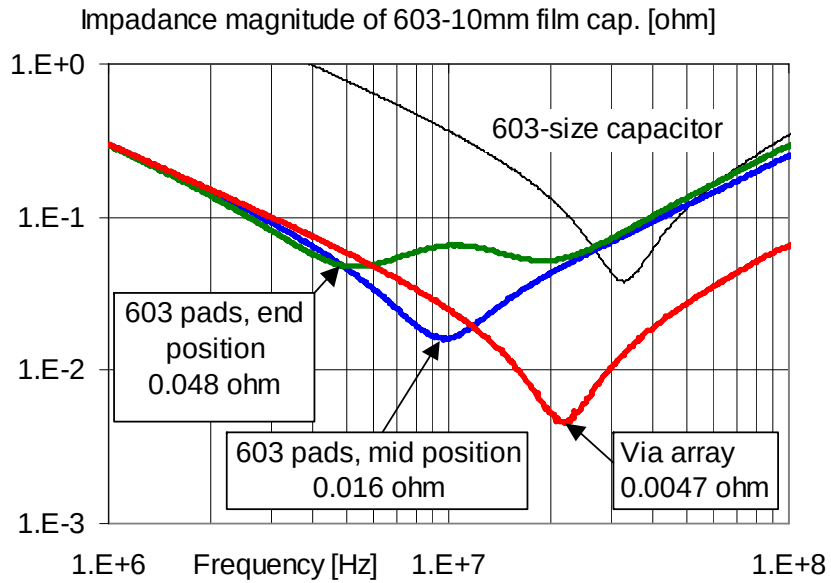
BGA capacitor



Source: AVX Corporation: Low Inductance Capacitors, S-LICC5M396-C brochure

Film capacitor

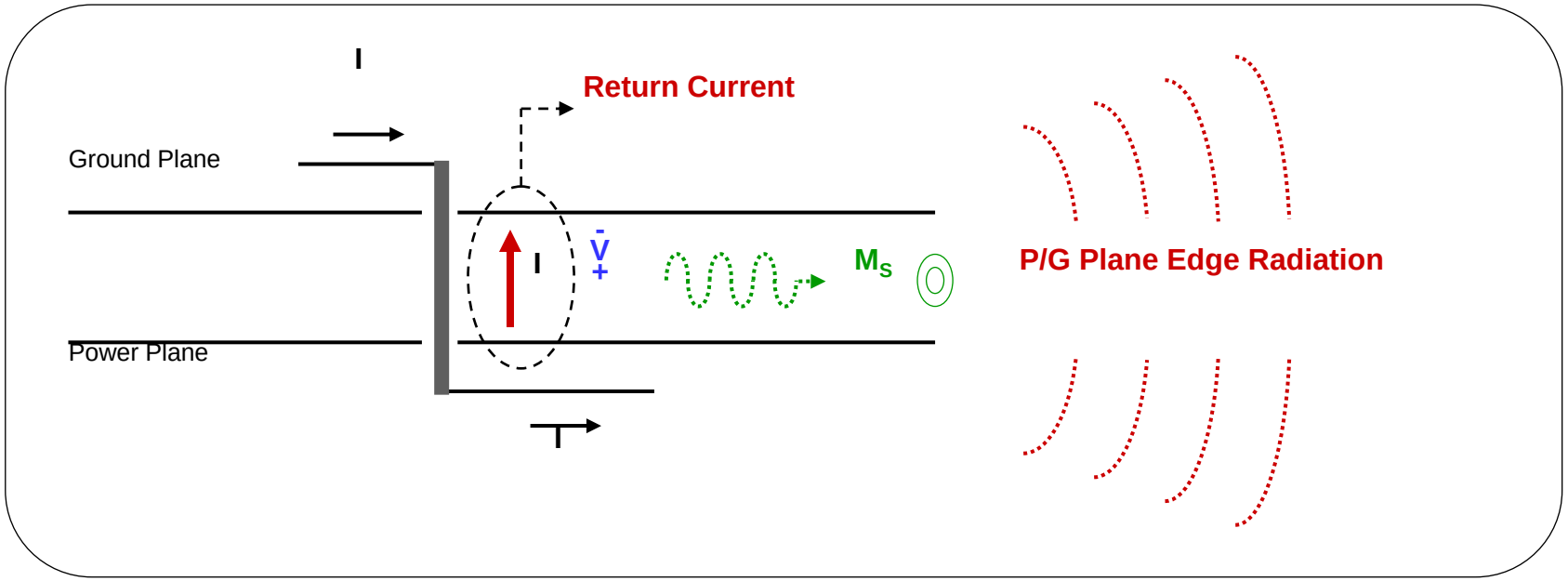




Courtesy: I. Novak. SUN

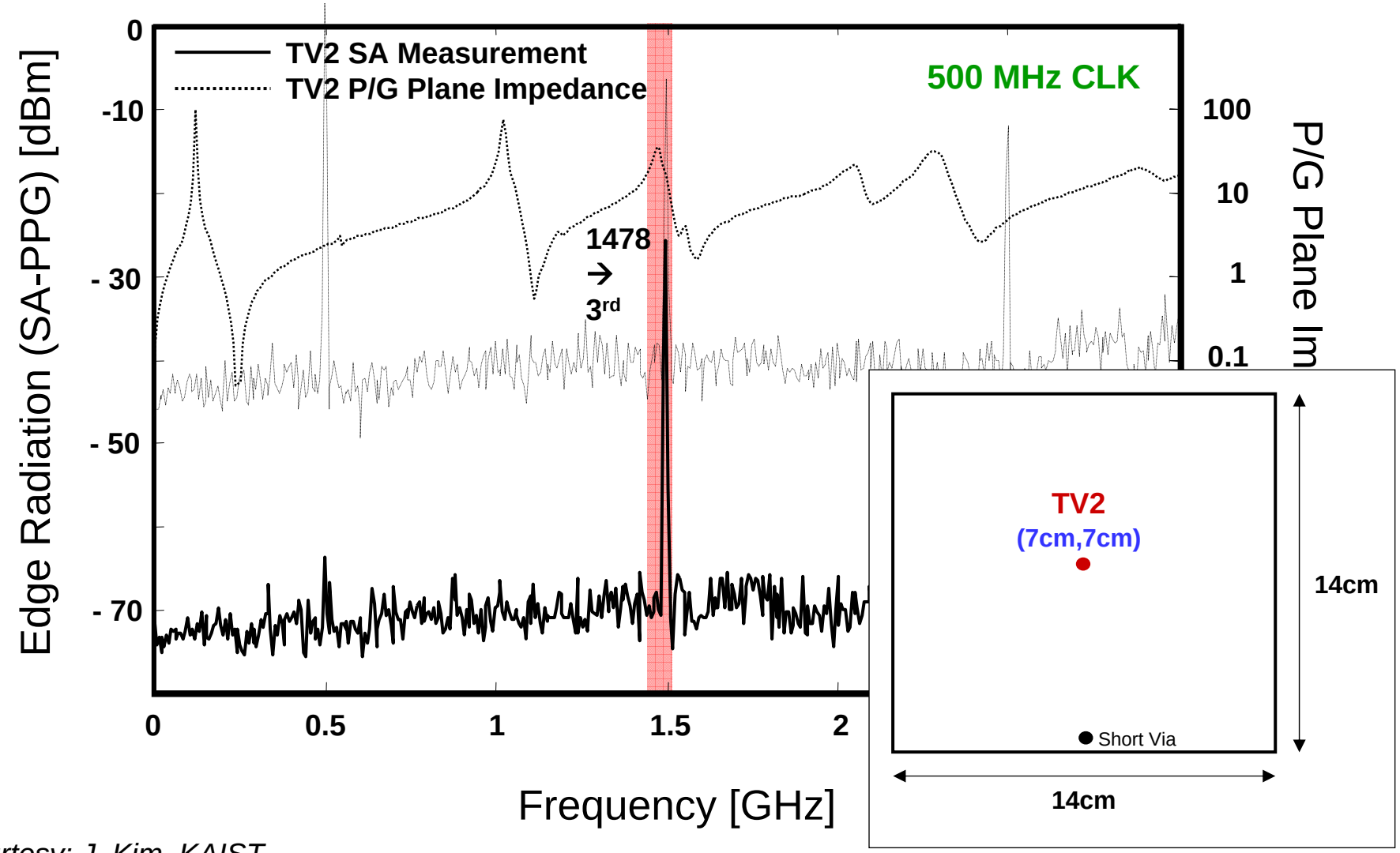
New Technologies

Plane Resonance and Edge Radiation



Courtesy: J. Kim, KAIST

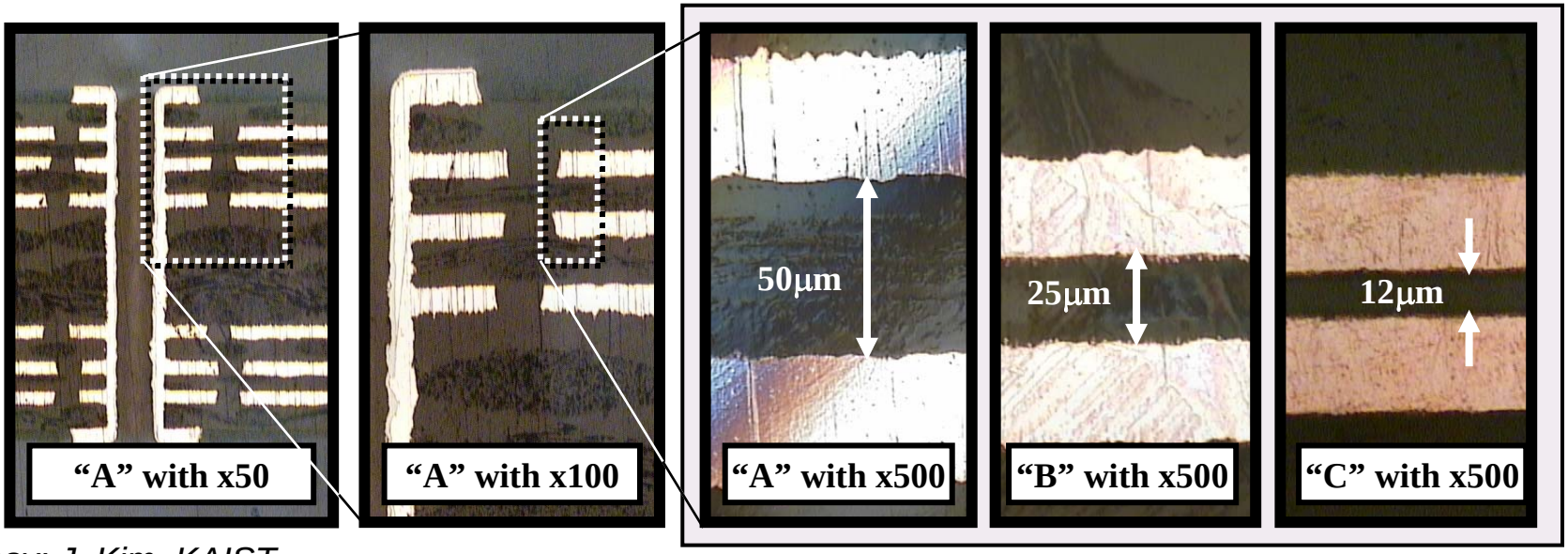
PCB Edge Radiation excited by 500 MHz Clock



Courtesy: J. Kim, KAIST

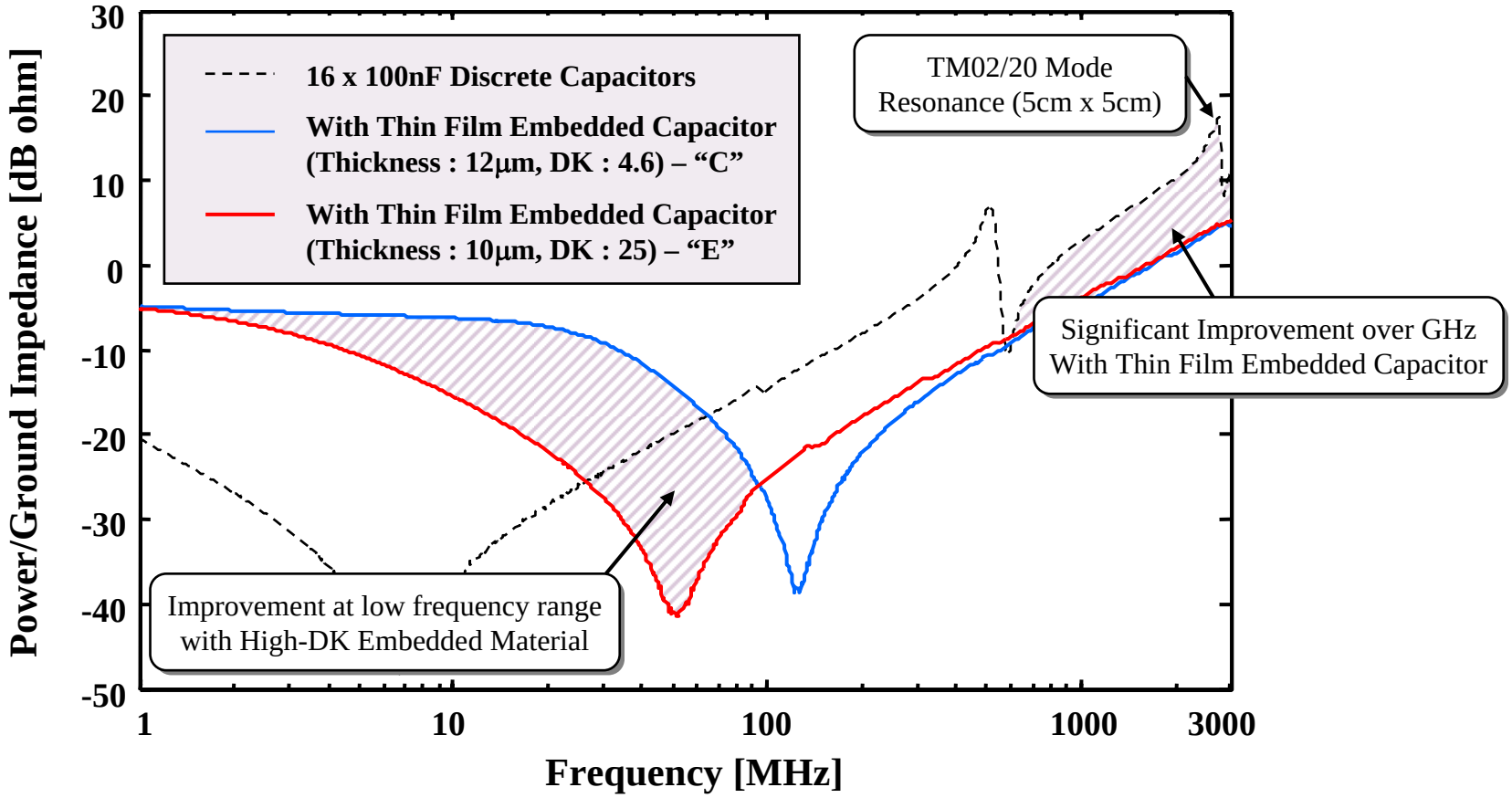
Thin Film Embedded Capacitor

Vehicle Code	Dielectric Thickness	Dielectric Constant (DK)	Capacitance/cm^2	Total Capacitance (5cm x 5cm with 2 pairs)
A	50 μm	4.6	81.46 pF	4.07 nF
B	25 μm	4.6	162.91 pF	8.15 nF
C	12 μm	4.6	339.40 pF	16.97 nF
D	10 μm	16	1416.64 pF	70.83 nF
E	10 μm	25	2213.50 pF	110.68 nF



Courtesy: J. Kim, KAIST

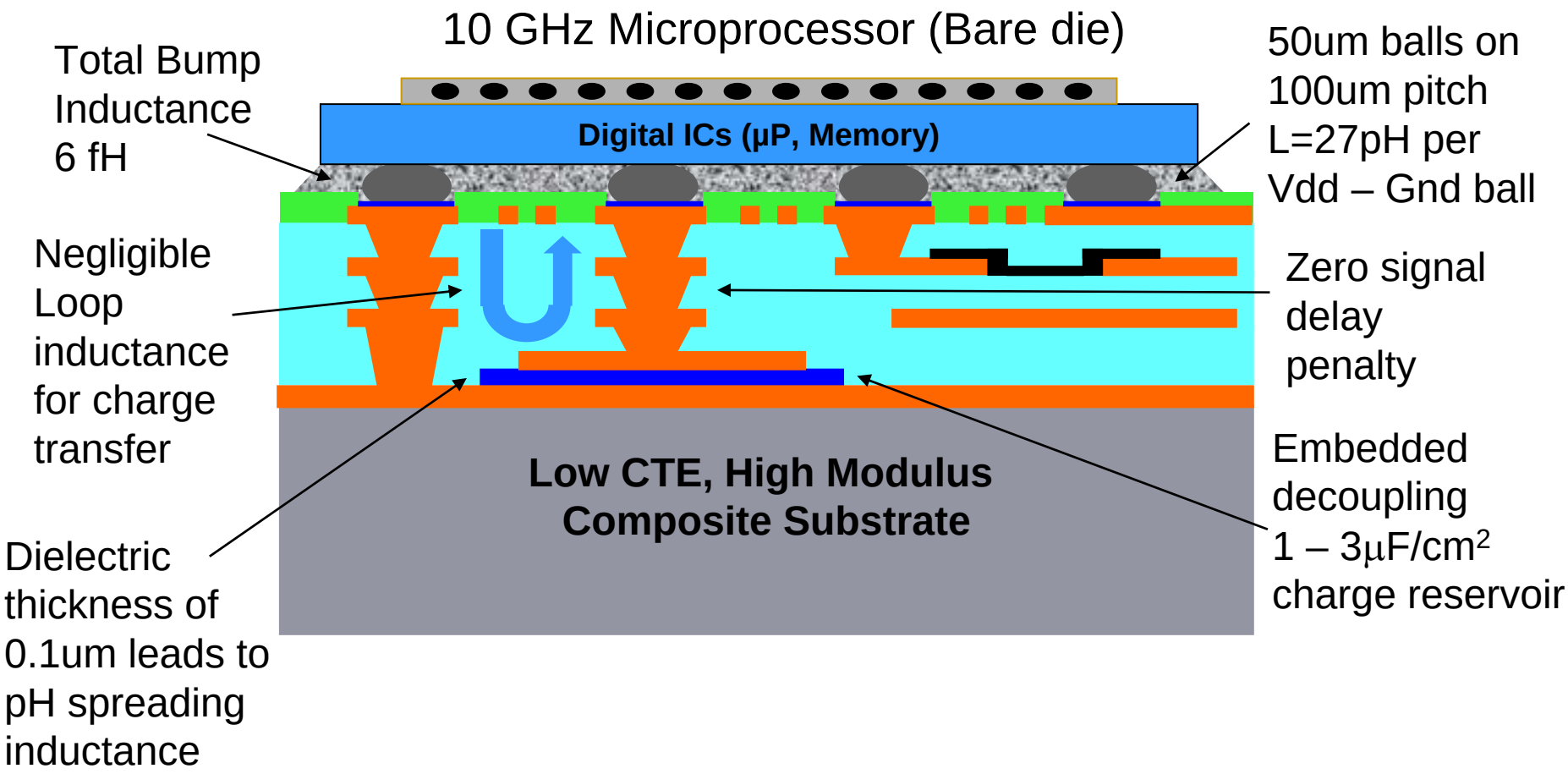
Measured PDN Impedance Curve



- Significant improvement over GHz with Thin Film Embedded Capacitor (**Very low ESL of Embedded Capacitor**)
- More improvement at low frequency range with high-DK embedded capacitor (**More Capacitance**)

Courtesy: J. Kim, KAIST

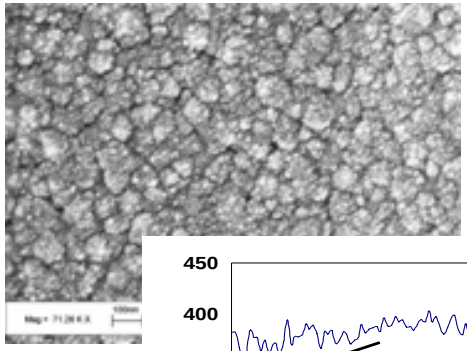
Low ESL Embedded Decoupling Capacitors in the Package

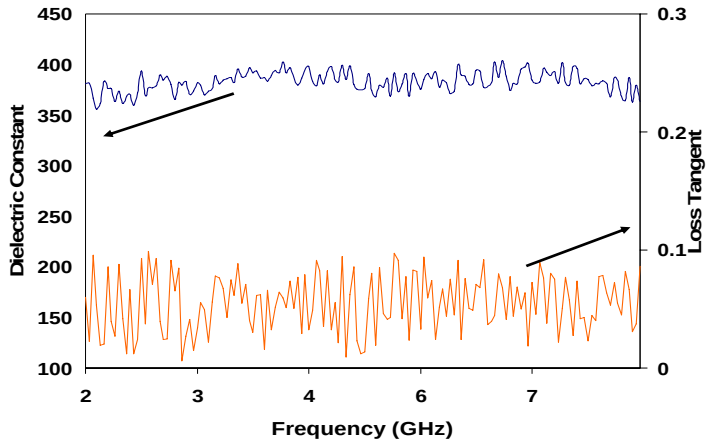


Technical Innovation in Embedded Capacitors

Low temperature hydrothermal synthesis of $BaTiO_3$

- <100°C Process Temperature
- 100-500nm Thick Film
- *Capacitance Density > 1μF/cm² Achieved*
- Loss Tangent ~ 0.05

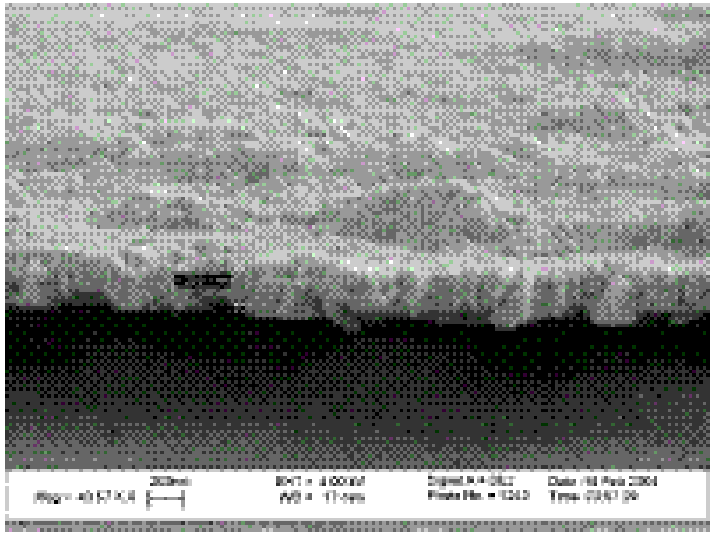




High frequency measurement

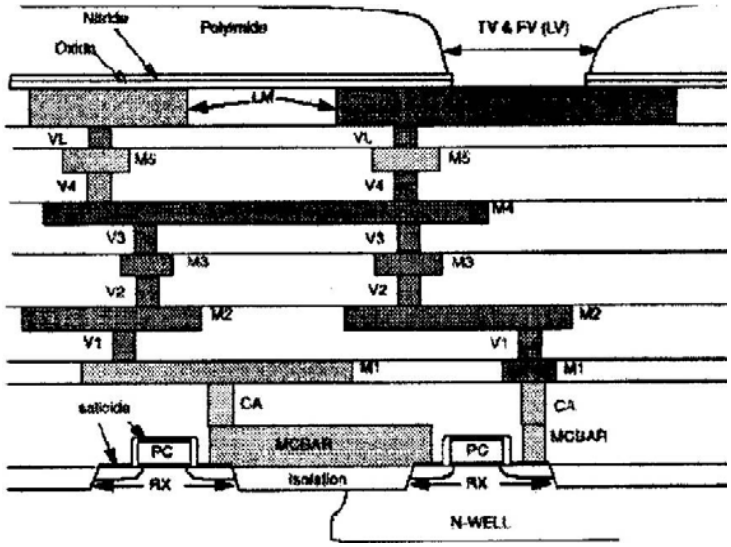
Sol-gel synthesis of $BaTiO_3$, $SrTiO_3$

- High Temperature Process (~600°C)
- Rapid Thermal Process Developed (3 min)
- 200-900nm Films Processed on Ni/Ti Foils
- Lamination Process for Integration
- *Capacitance Density ~500nF/cm²*
- Loss Tangent ~0.005

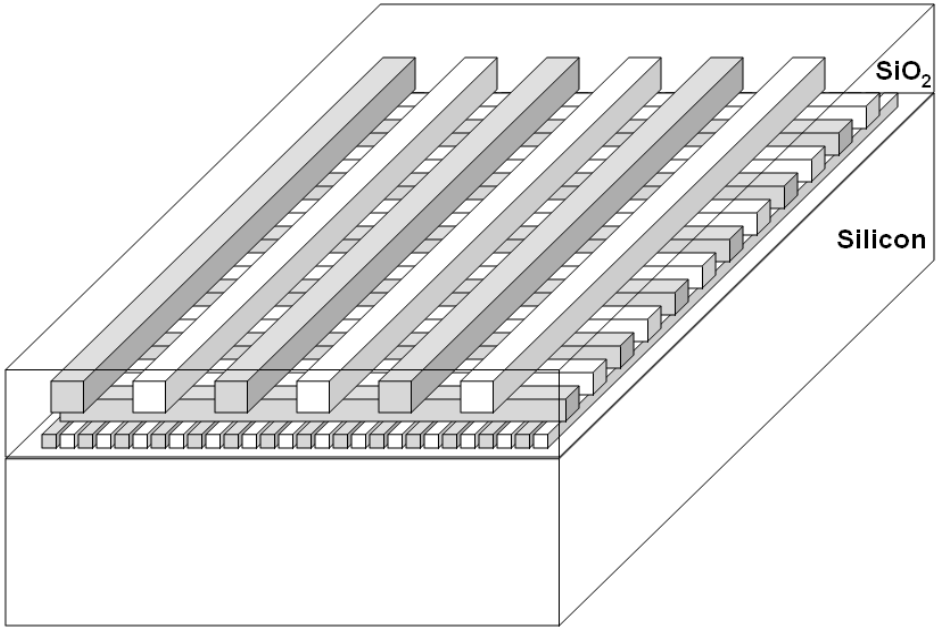


Modeling

On-chip Power Distribution Network

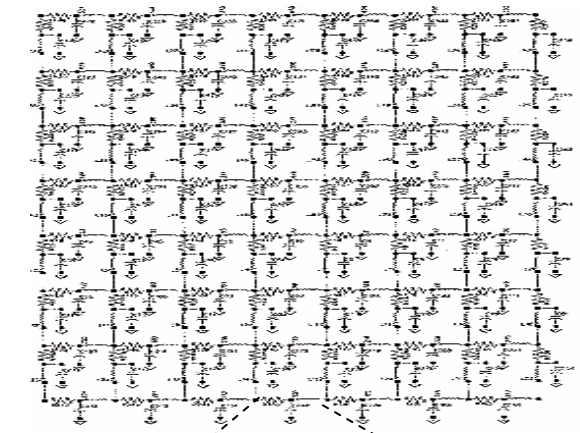


Cross section of ASIC power distribution*



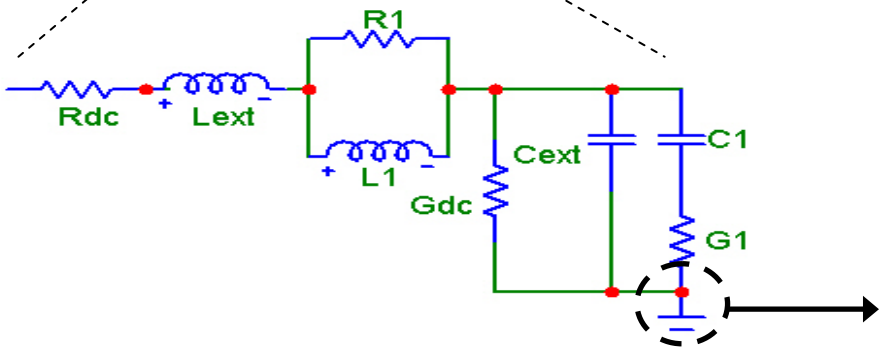
3D view of on-chip power grid

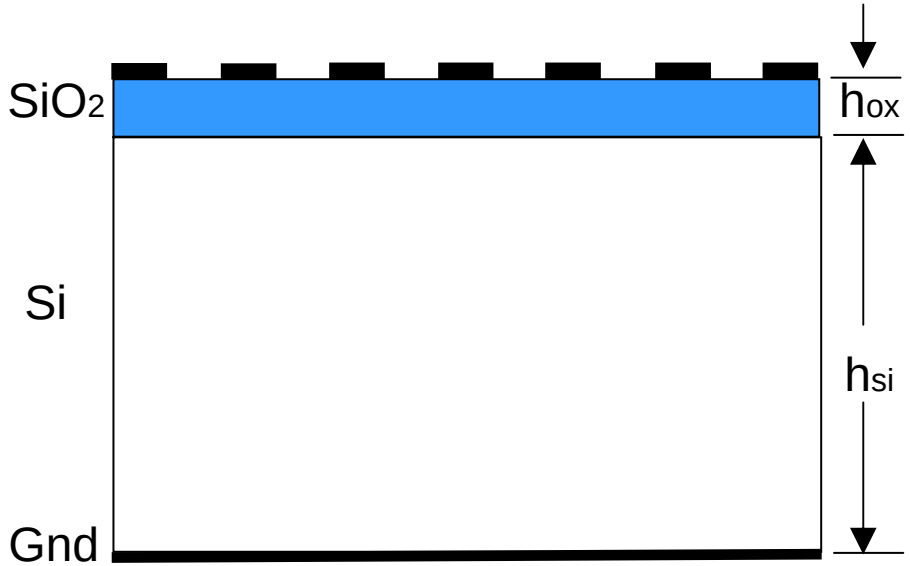
Finite Difference Time Domain Method



$$Z = R_{dc} + j\omega L_{ext} + \frac{j\omega L_1}{1 + j\omega L_1 / R_1},$$

$$Y = G_{dc} + j\omega C_{ext} + \frac{j\omega C_1}{1 + j\omega C_1 / G_1}$$

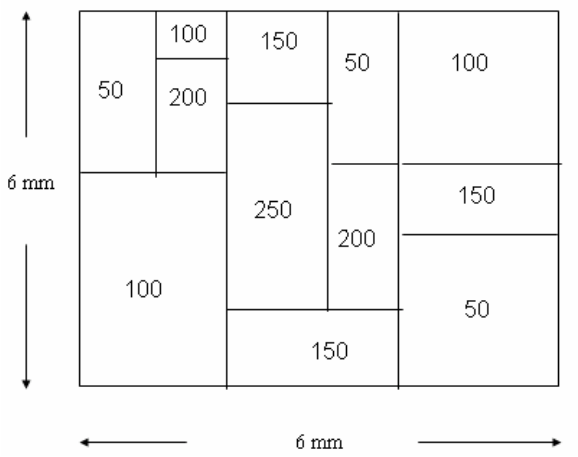




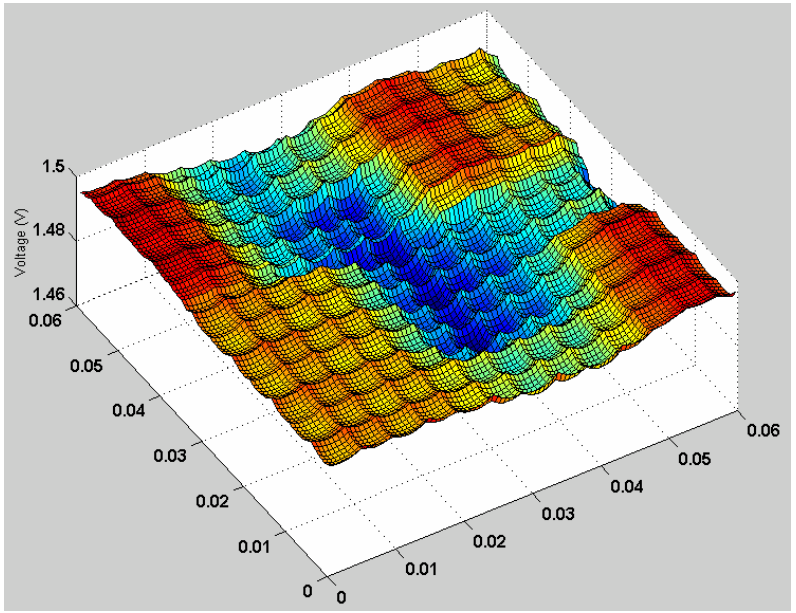
First order Debye equivalent circuit

Cross section of on-chip power grid

Simulation of Power Supply Noise using FDTD



Chip composed of blocks with different power densities (unit=mw/mm^2)



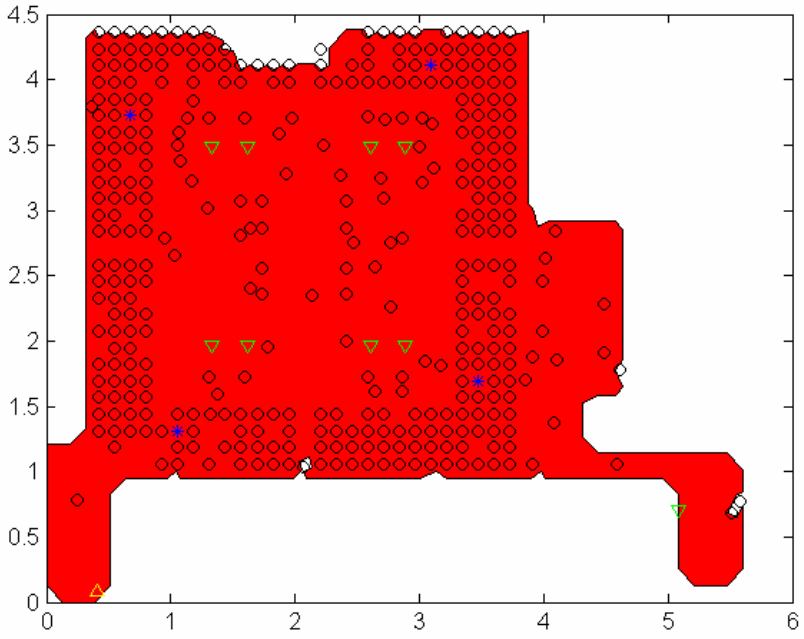
Size(mm×mm)	6×6
Metal Layers	6 (M1…M6)
Nodes	5,661,354
Element (RLGC)	22,645,380

Modeling of Core Power Distribution in Package and Board

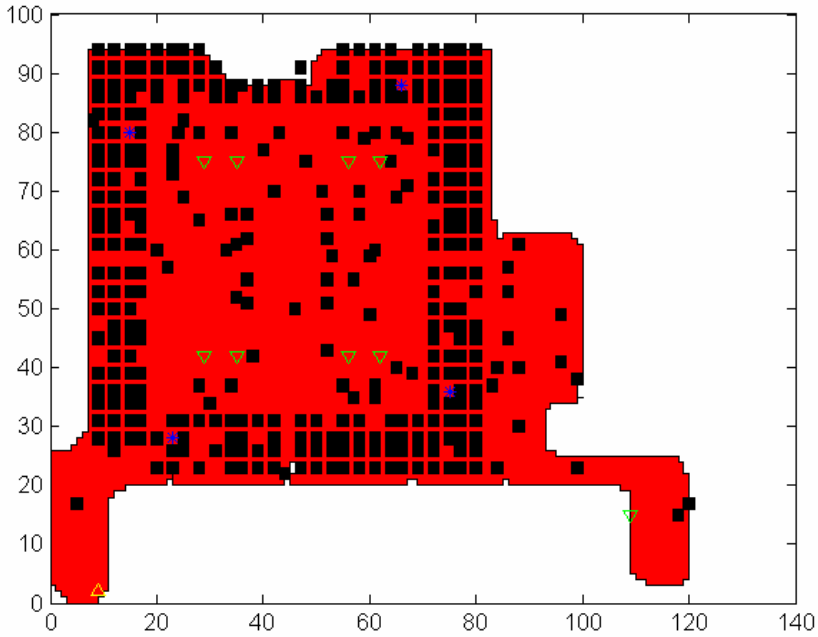
Unit cell size: 0.093 X 0.093 cm

* Port 1: (0.677, 3.7268)
Port 2: (1.058, 1.3138)
Port 3: (3.471, 1.6948)
Port 4: (3.09, 4.1078) cm

∇ Decaps
Δ Ferrite + C25



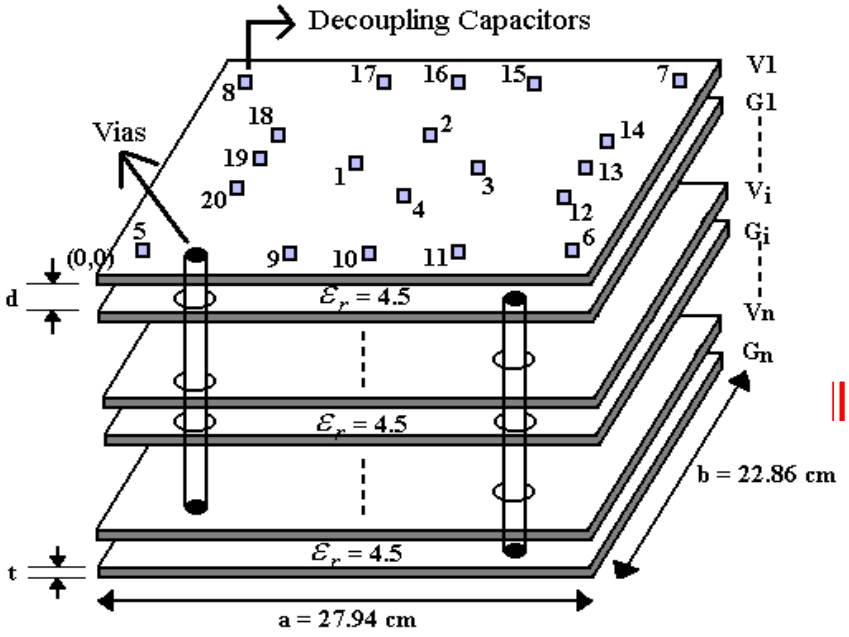
Original Plane



Grid

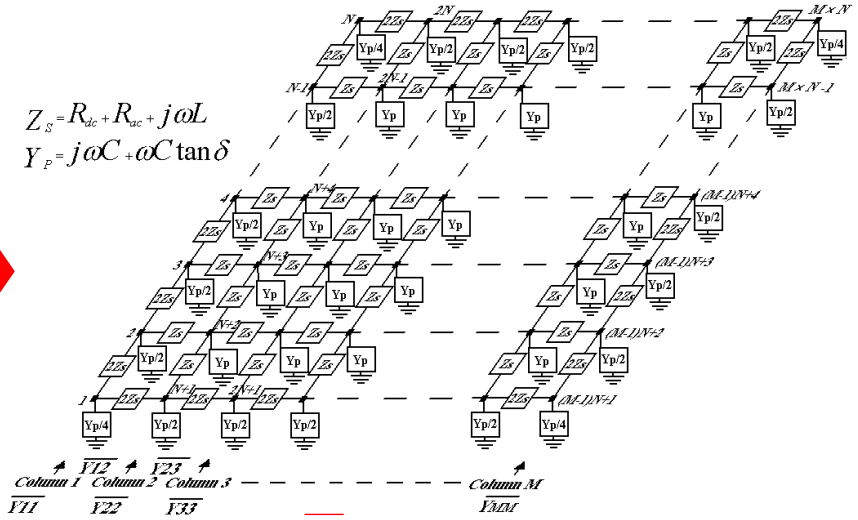
Courtesy: Kodak

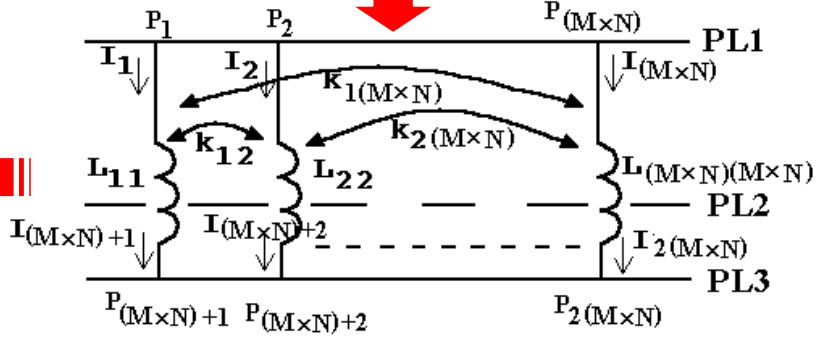
Modeling of Multi-layered Planes in Packages and Boards using Transmission Matrix Method



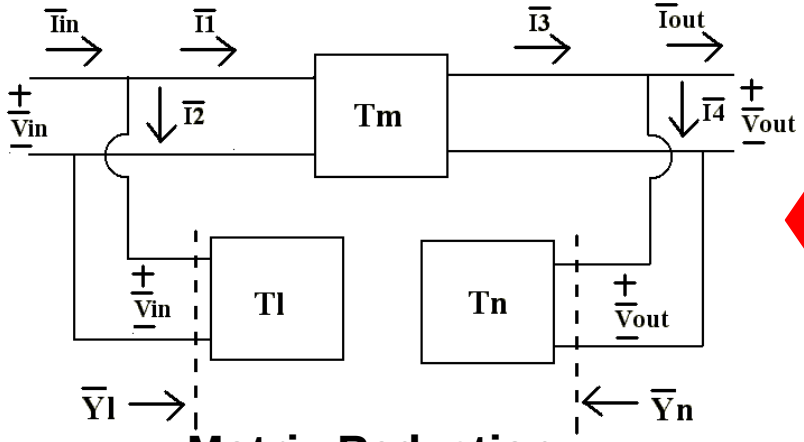
Horizontal plane pair approximated using discretized RLGC parameters

$$Z_S = R_{dc} + R_{ac} + j\omega L$$
$$Y_P = j\omega C + \omega C \tan\delta$$





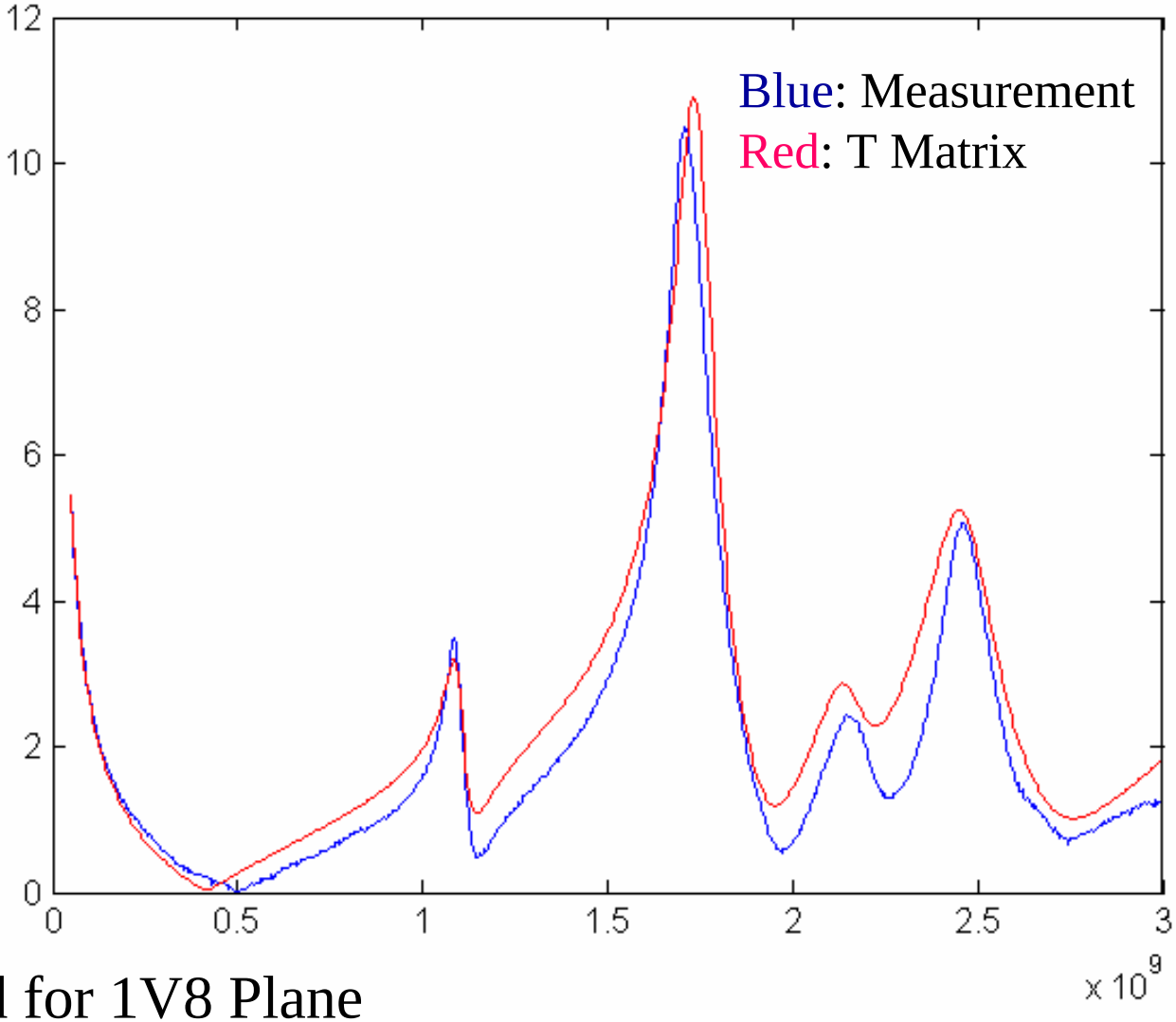
Planes connected using via inductance



Matrix Reduction

Model to Hardware Correlation

Z11

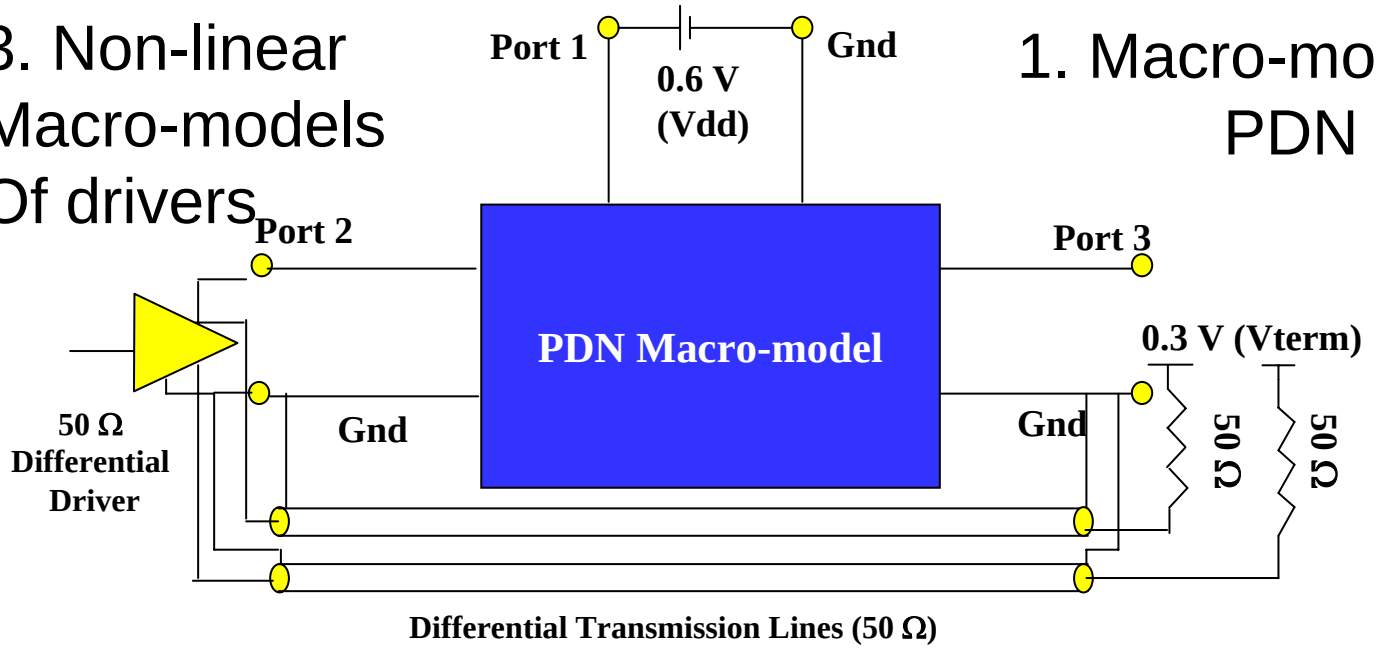


Bare Board for 1V8 Plane

Modeling of I/O Power Distribution

3. Non-linear Macro-models Of drivers

1. Macro-models of PDN



2. RLGC Models or Macro-models of Transmission Lines

Coupled Signal and Power Distribution Simulation using TMM

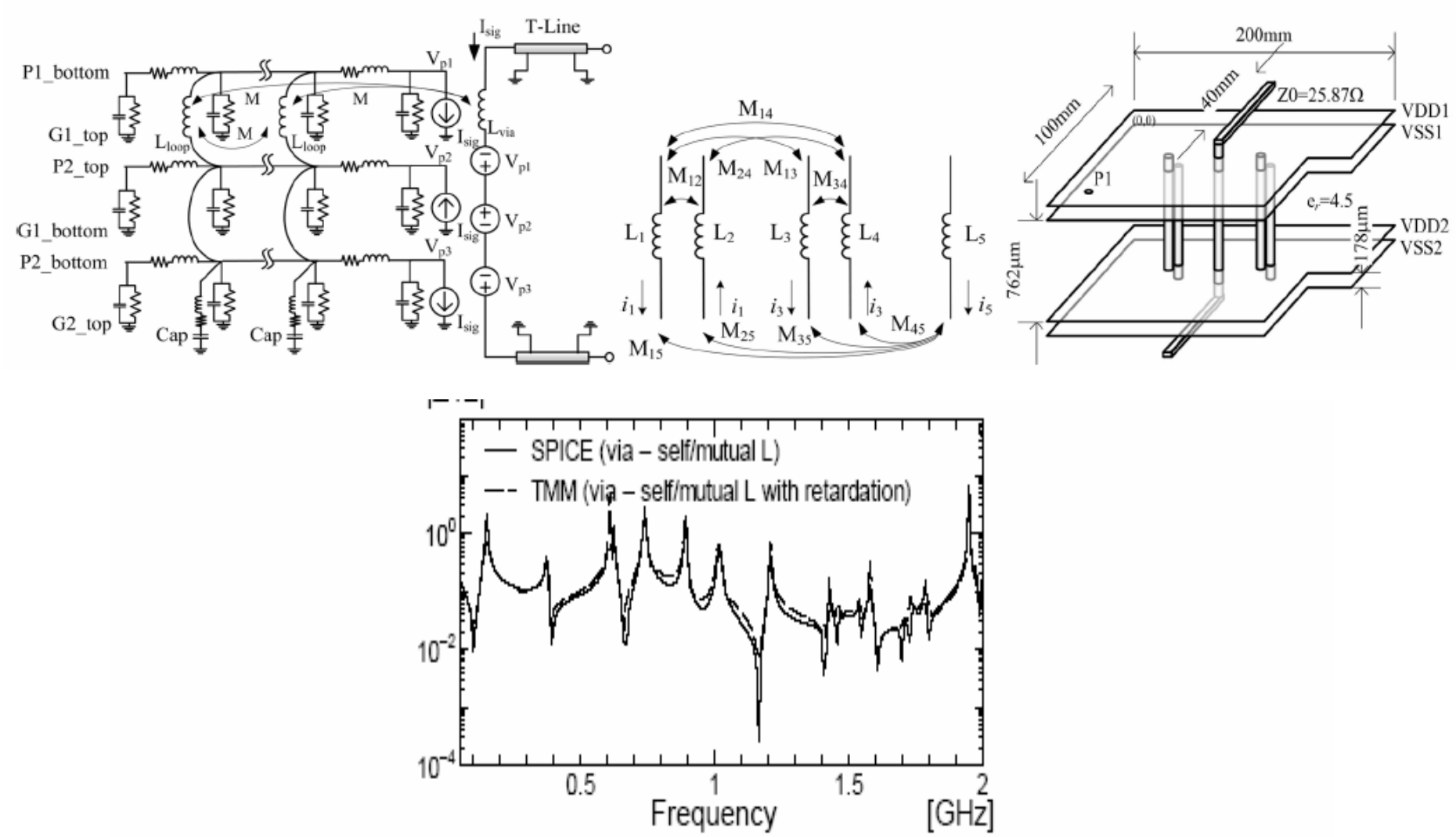
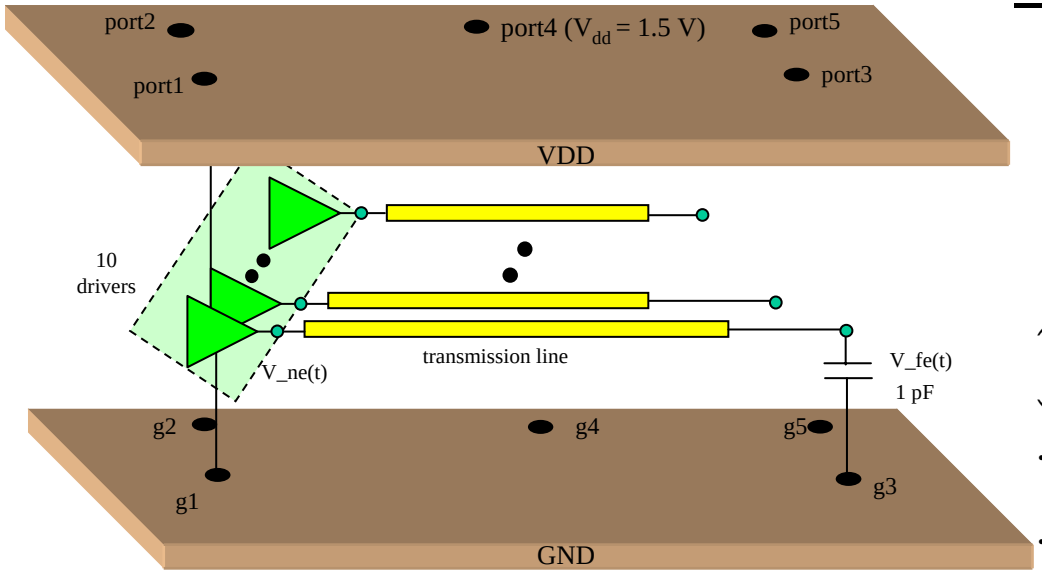
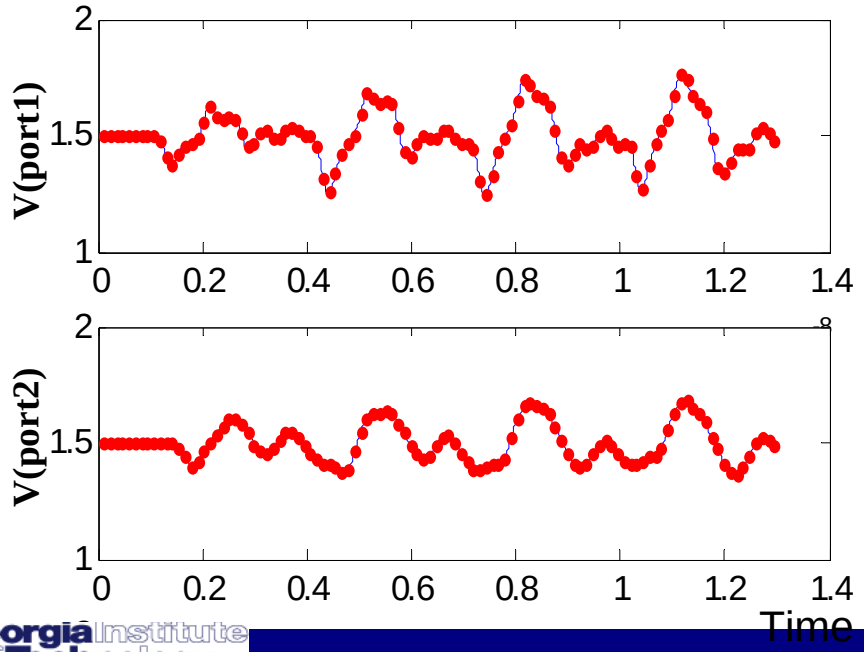
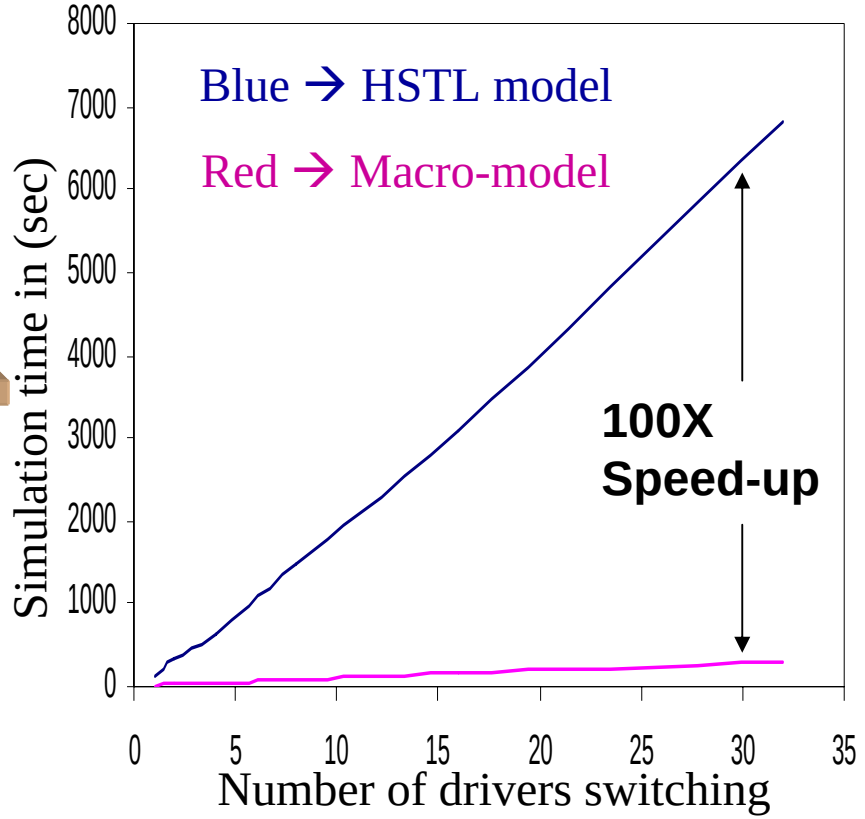


Fig. 10: Transfer impedance spectra between the near-end of T-Line and the port P1.

Test Case: IBM HSTL_B 350MHz Driver



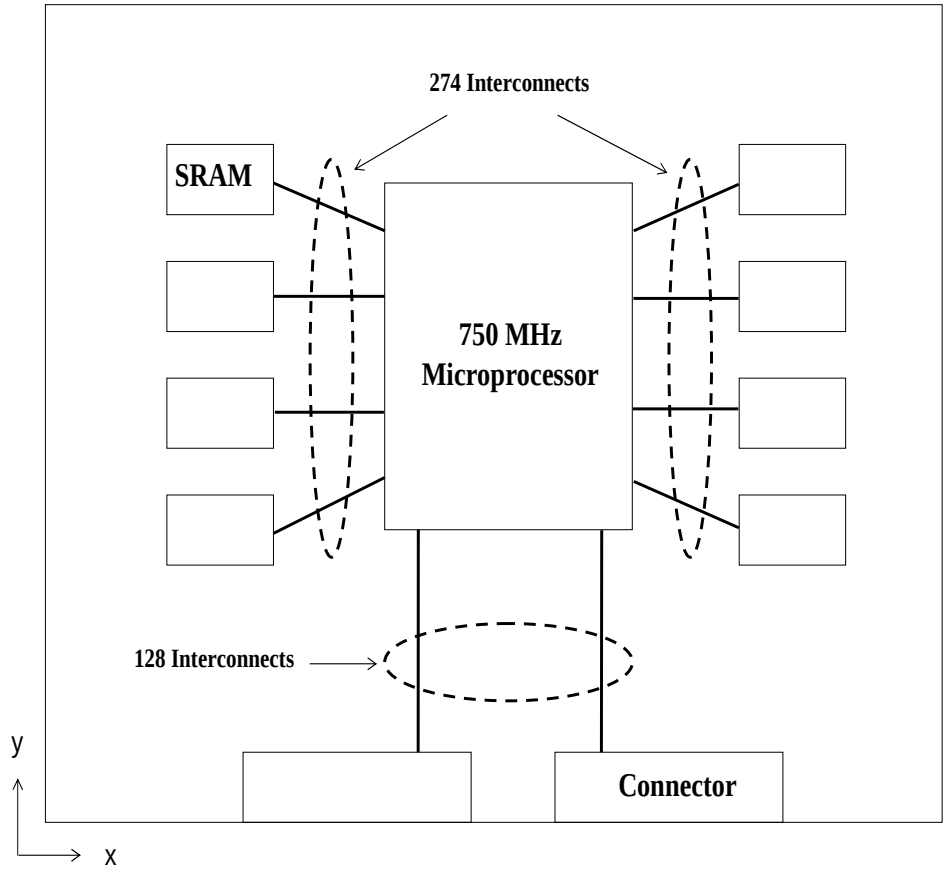




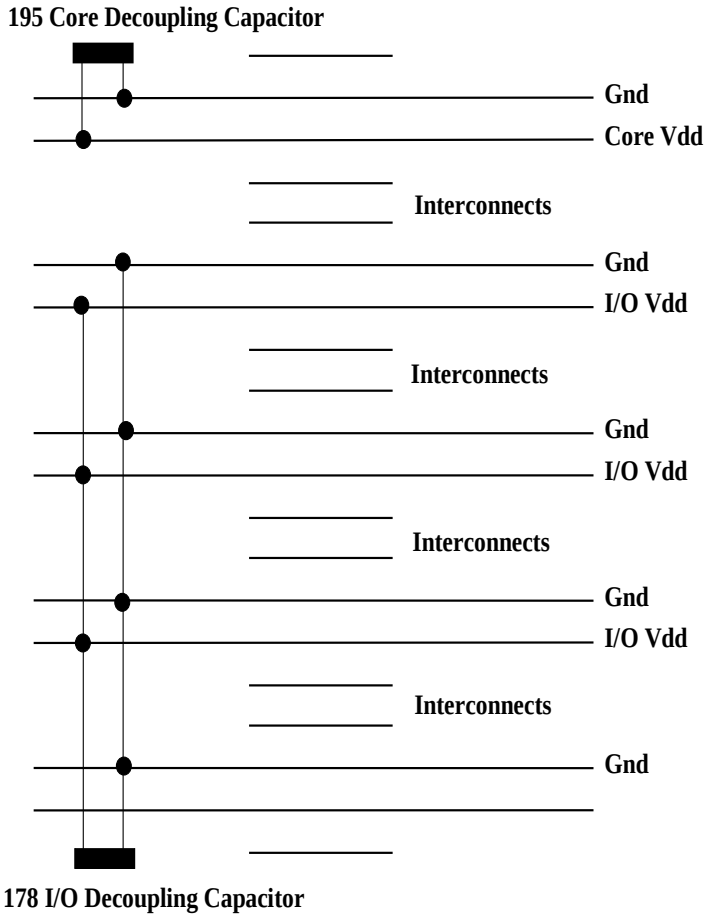
Time (s)

Example from SUN

[Top View]

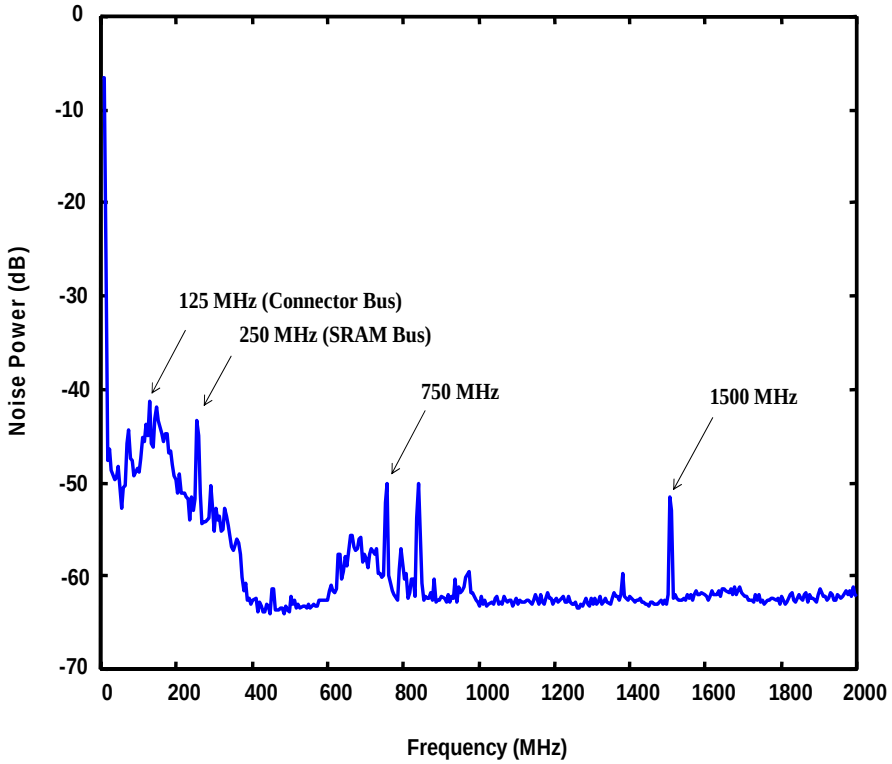


[Cross Section]

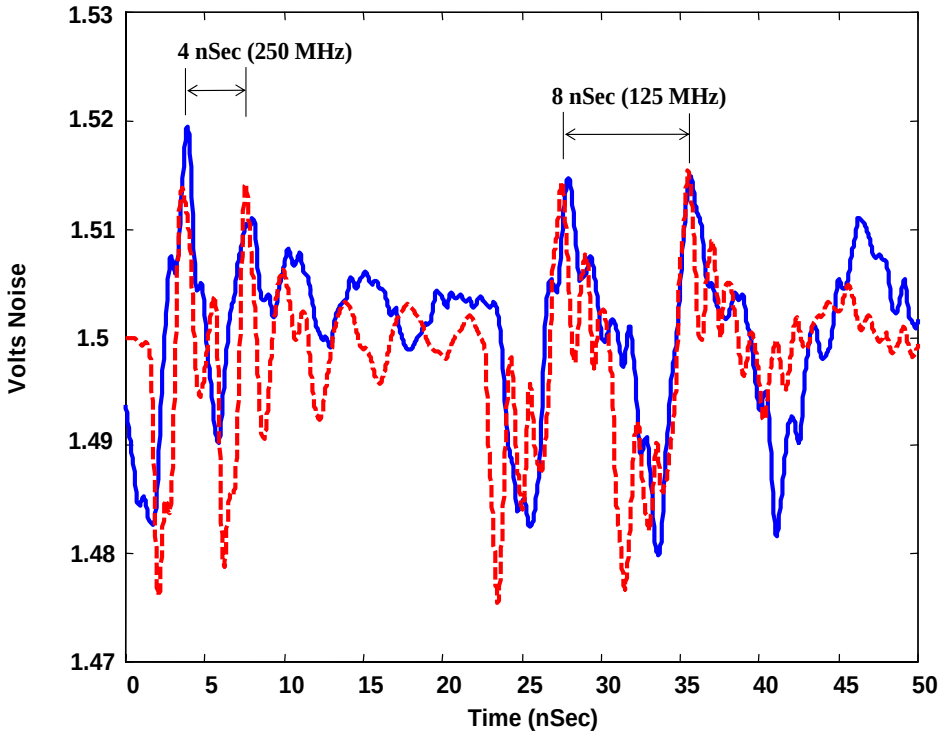


I/O PDS Noise

[Frequency Domain]



[Time Domain]



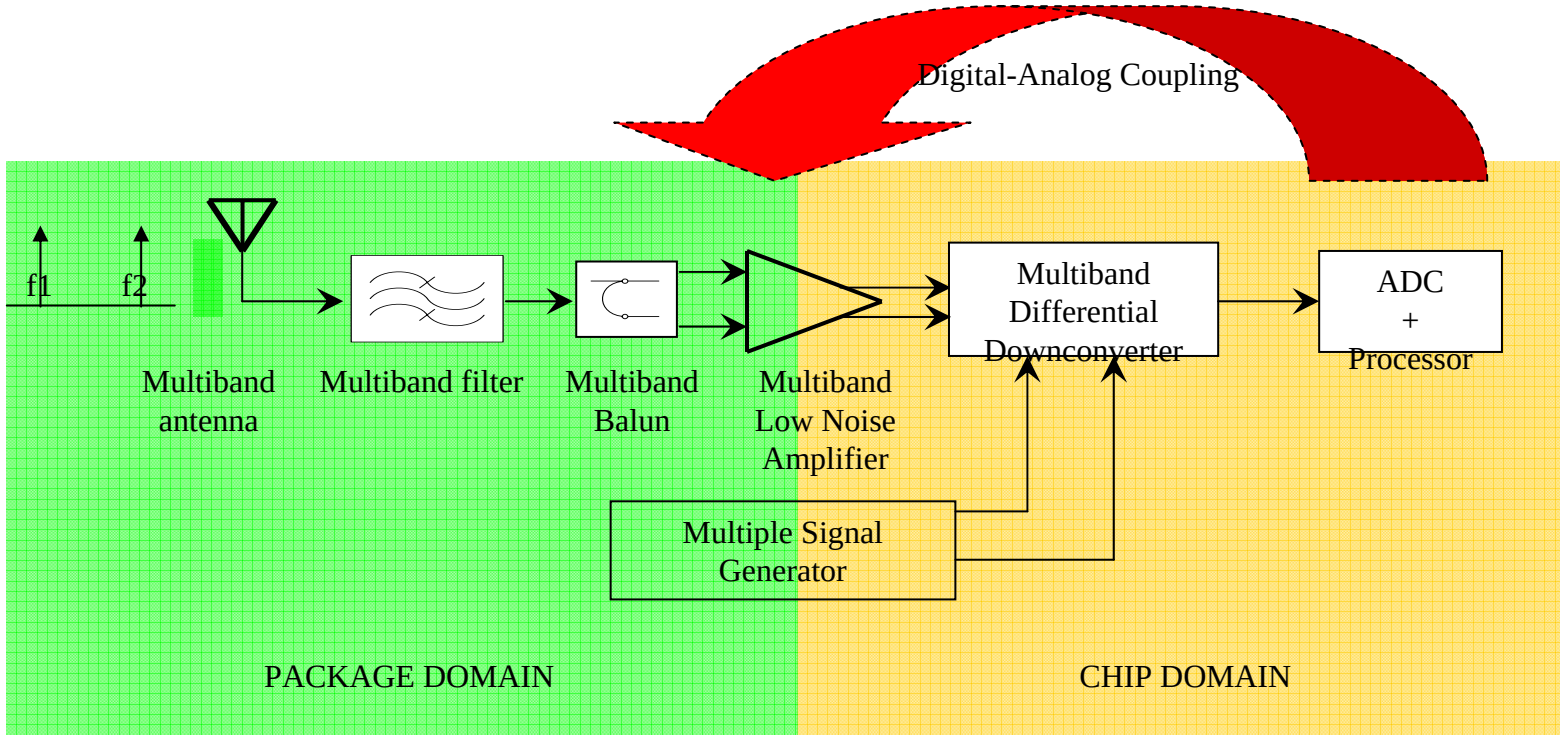
Simulation Time: 124 Seconds with 20 ps time step

Blue: Measurements, Red: Modeling

I/O switching noise is caused by the return current flowing on the I/O vdd/gnd planes.

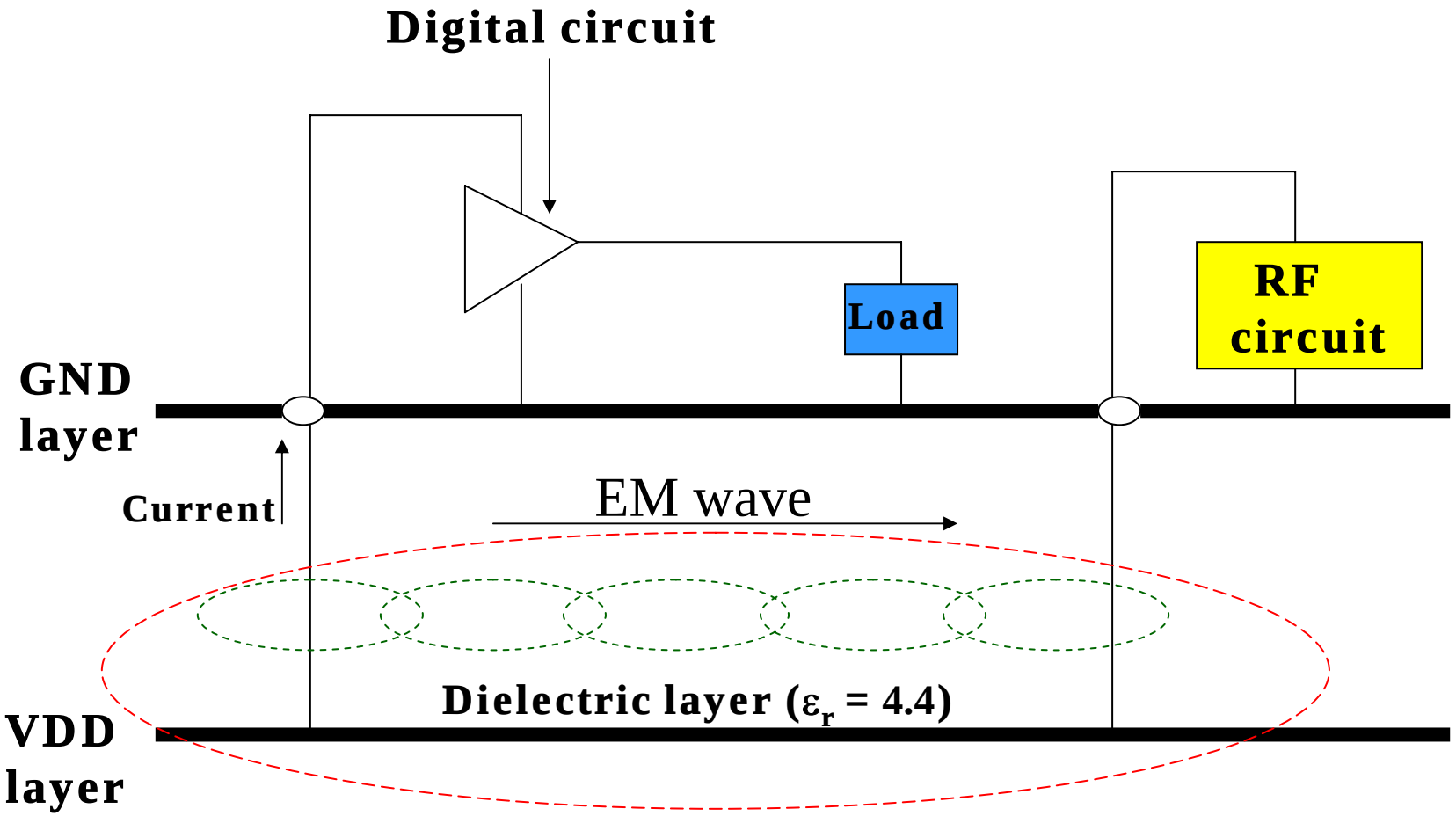
Heterogeneous Systems

Heterogeneous Integration



Example: 802.11 a/b/g; WiMaX; UWB; Handset

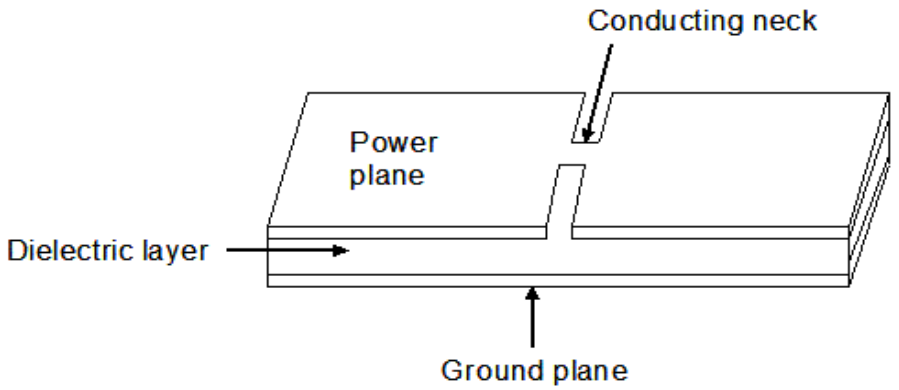
Electromagnetic Coupling in Mixed-Signal Systems



EM coupling

Isolation Methods Available

- **Split planes & Ferrite bead**
  - ferrite bead is placed between split planes for DC connection
  - require a single power supply
  - still poor isolation at high frequencies due to EM coupling through a gap
- **Power-plane Segmentation**
  - conducting neck is placed between split planes for DC connection
  - requires a single power supply
  - poor isolation except narrow frequency range

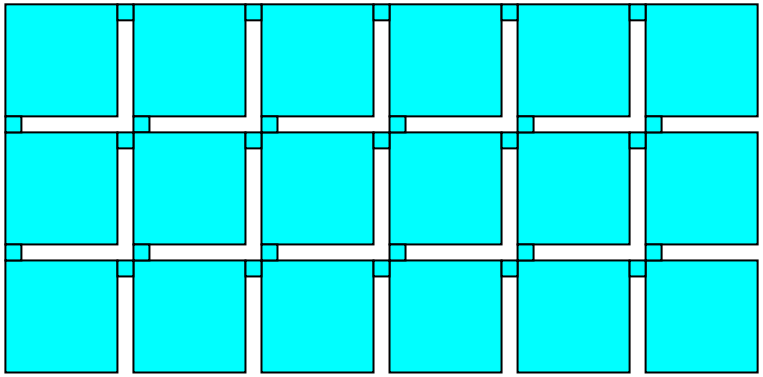


⇒ ***Better isolation technique is needed for mixed-signal system applications***

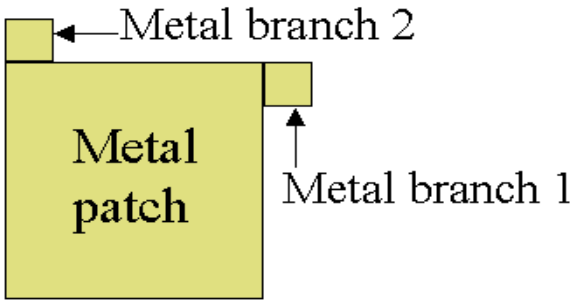
EBG Structure

- Two-dimensional (2-D) square lattice with each element consisting of a metal patch with two connecting metal branches.
- Metal branches introduce additional inductance and capacitance is mainly formed by metal patches and corresponding parts of other plane.

  $\Rightarrow$ **Distributed LC network**.



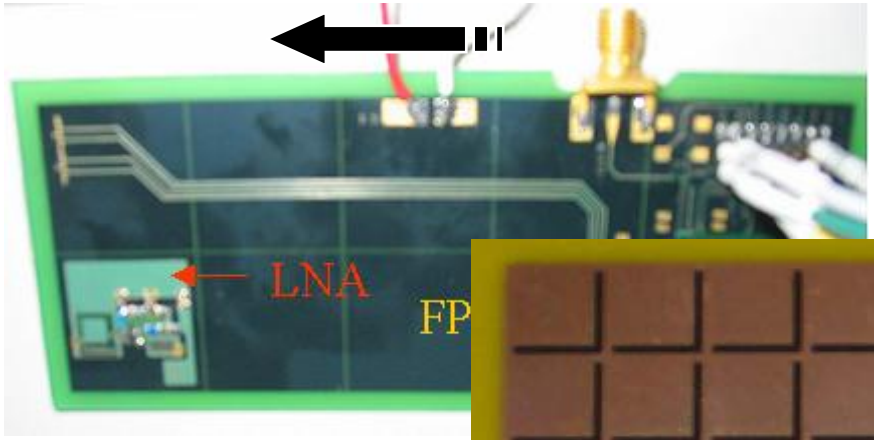
Schematic of Novel EBG Structure in GND plane



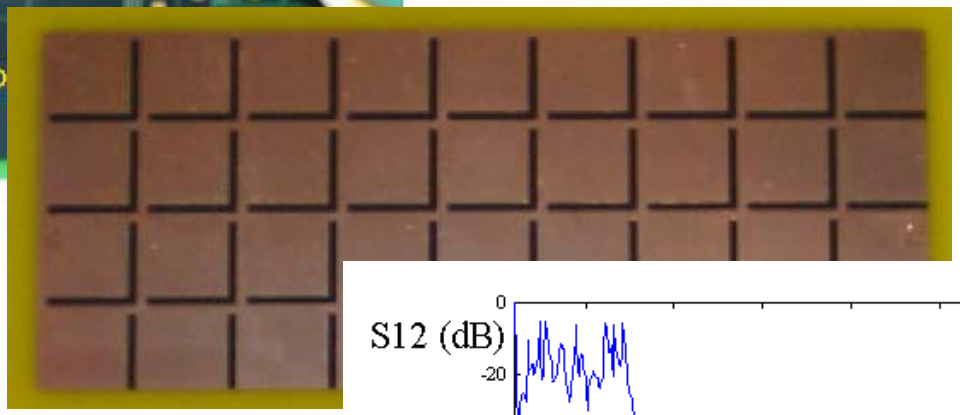
Unit Cell of Novel EBG Structure

Noise Isolation using Electronic Bandgap Structures

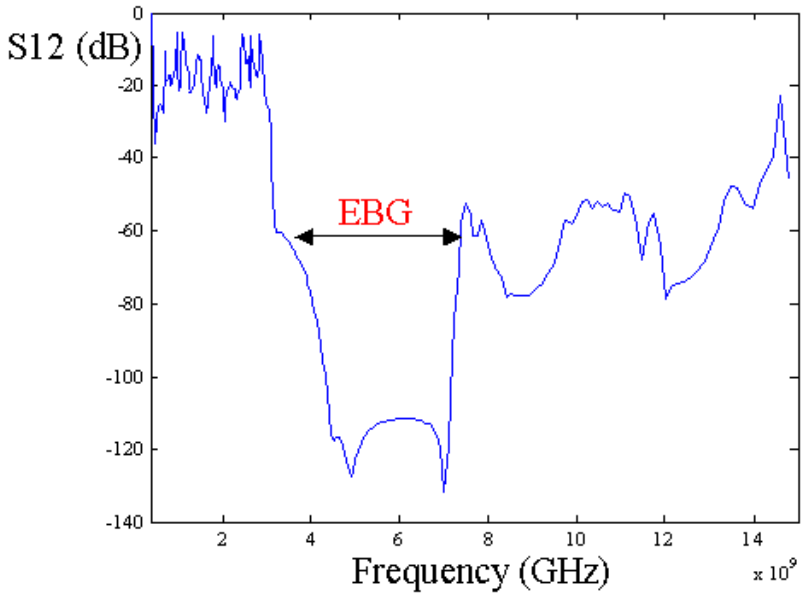
Substrate Coupling



300MHz FPGA with 2.13GHz LNA

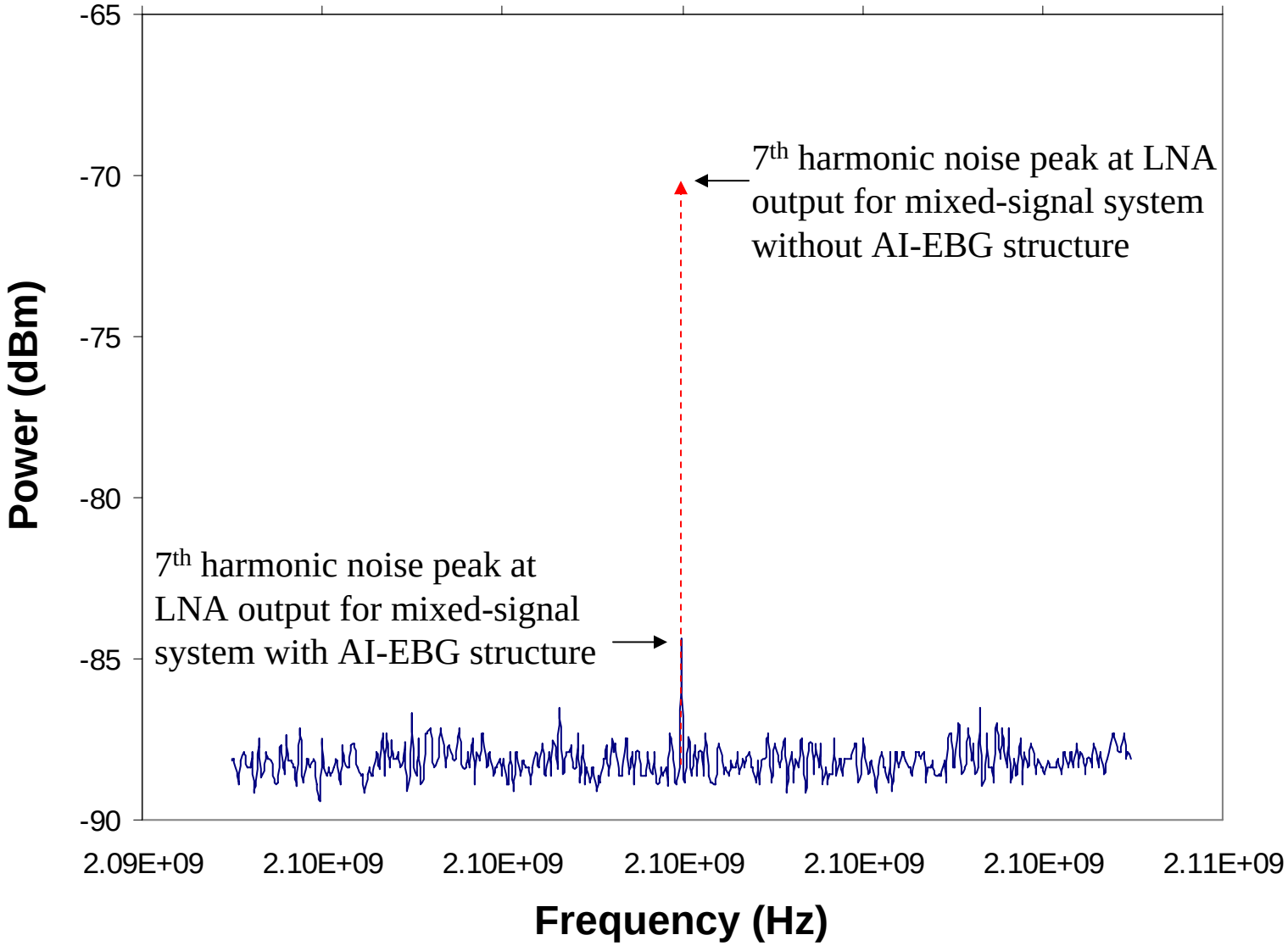


Patterned Ground Plane



EBG Response

Noise Reduction with EBG Structure



Summary

- Digital Systems

  Increasing chip power and technology scaling placing challenges on IR drop, EM, leakage and active power

  Voltage islands on-chip and multiple I/O voltages making the design complex

  Decoupling capacitors on package running out of steam

  Embedding decoupling increasing design complexity

- Modeling

  On-chip Modeling: Still very complex due to the feature sizes,

  irregular layouts and uncertainty in the return current path

  Chip – Package Interface: Integrated modeling of chip and

  package still doesn't exist

  Estimation of current signature a big challenge

  Modeling of isolation in mixed signal systems with low noise floors

- Heterogeneous Integration

  Achieving -85dBm over broad frequency a challenge

  3D Integration is making it worse

Reference

M. Swaminathan, J. Kim, I. Novak and J. Libous,
"Power Distribution Networks for System on a Package: Status And Challenges", IEEE Trans. On Advanced Packaging, pp. 286 – 300, Vol. 27, No. 2, May 2004