Emerging Trends in High-Speed Interconnects and Packaging Engineering

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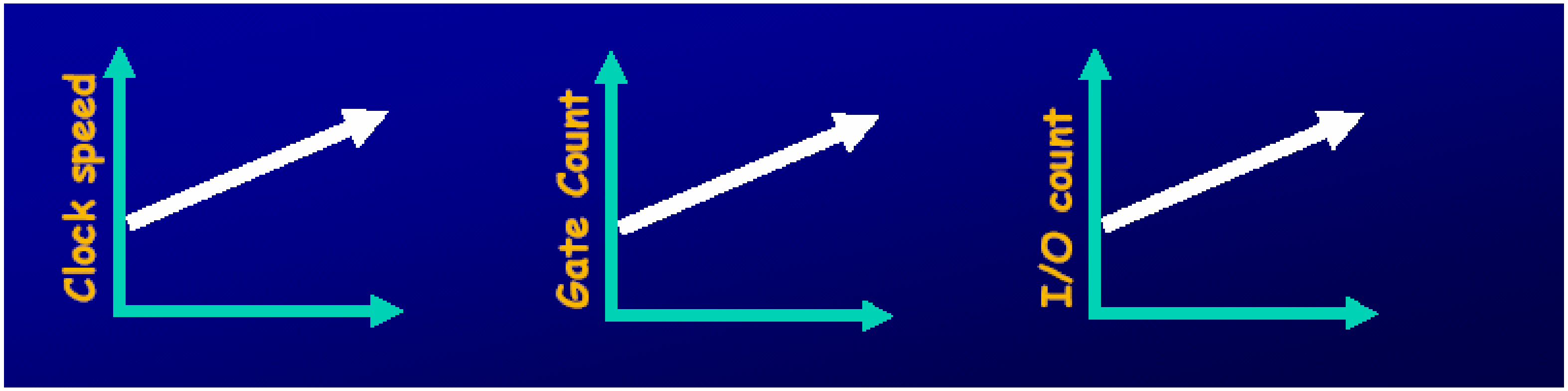
Drivers
Trends
Silicon challenges
Packaging challenges
PCB evolution
Silicon, packages, boards Trends
Considerations
Testability
Ultra High-Speed Interconnects
Conclusions

Drivers

- CUSTOMERS' expectations
- Mission critical applications

drive

- Overall architecture, complexity
- Performance and Density

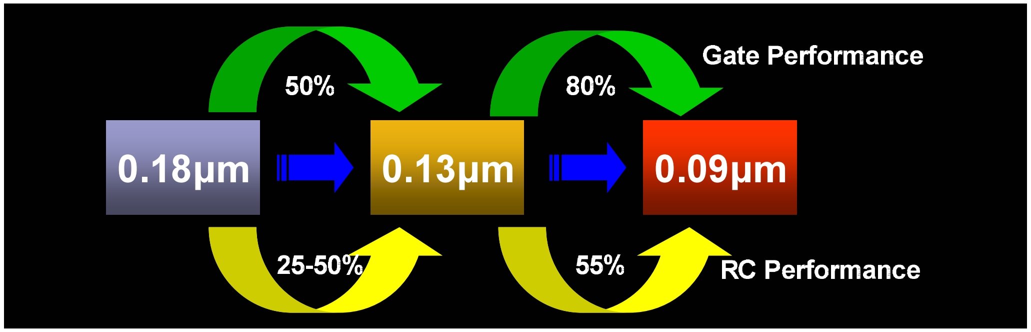


Trends

- Migration to newer *Nodes* is necessary
  - ➢ Higher integration
  - ➢ Higher performance
  - ➢ Lower power per gate
- Is it attractive?
  - ➢ More complexity, less predictability
  - ➢ Longer design cycles
  - ➢ Higher expenses
  - ➢ More resources
  - ➢ Higher risks

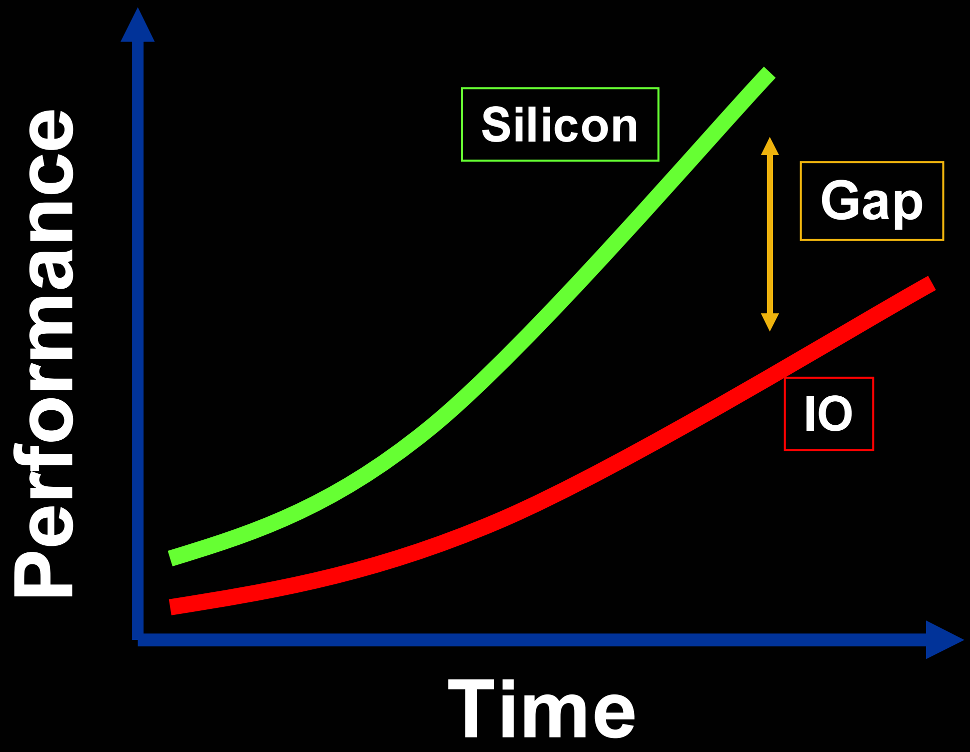
Silicon Challenges

- 90nm and below
  - ➢ NRE costs are huge
  - ➢ Schedules are longer
  - ➢ ASIC re-spins have severe impact on TTM and … …customers' perception
  - ➢ Gate performance higher than wiring performance



- ➢ Growing *on-chip* Signal / Power / Timing Integrity demands

Silicon Vs Packaging: an emerging GAP!



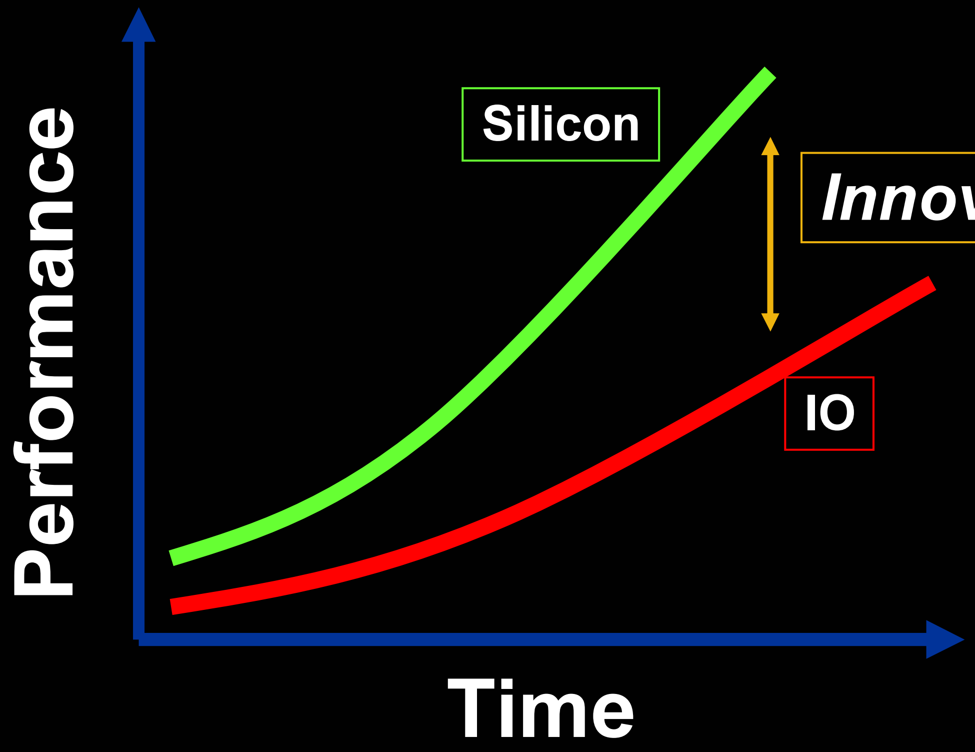
Packaging Challenges

- Signal and Power distribution
- Multi - GHz Signaling speeds
- Low voltage swing interfaces
- Supply voltage 1V, or less
- Higher power to feed
- Higher data rates, lower noise margins
- Increasing usage of hi-speed I/O

Packaging Challenges

- Higher power to dissipate!
- Increasing I/O number
- Increasing number of pwr/gnd terminals
- Larger package size
- Reduced access and observability

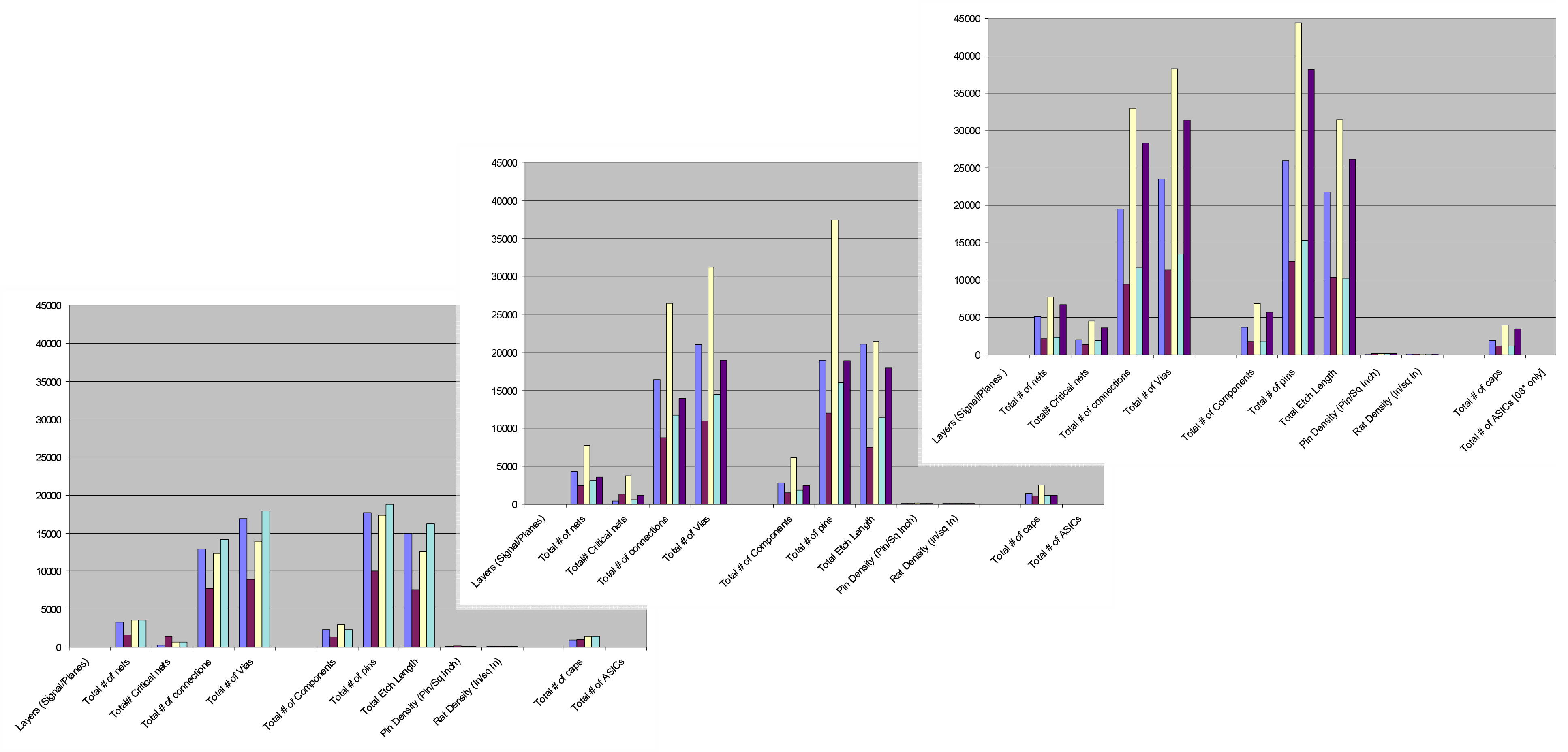
An opportunity for innovation!



Innovate to close this gap !

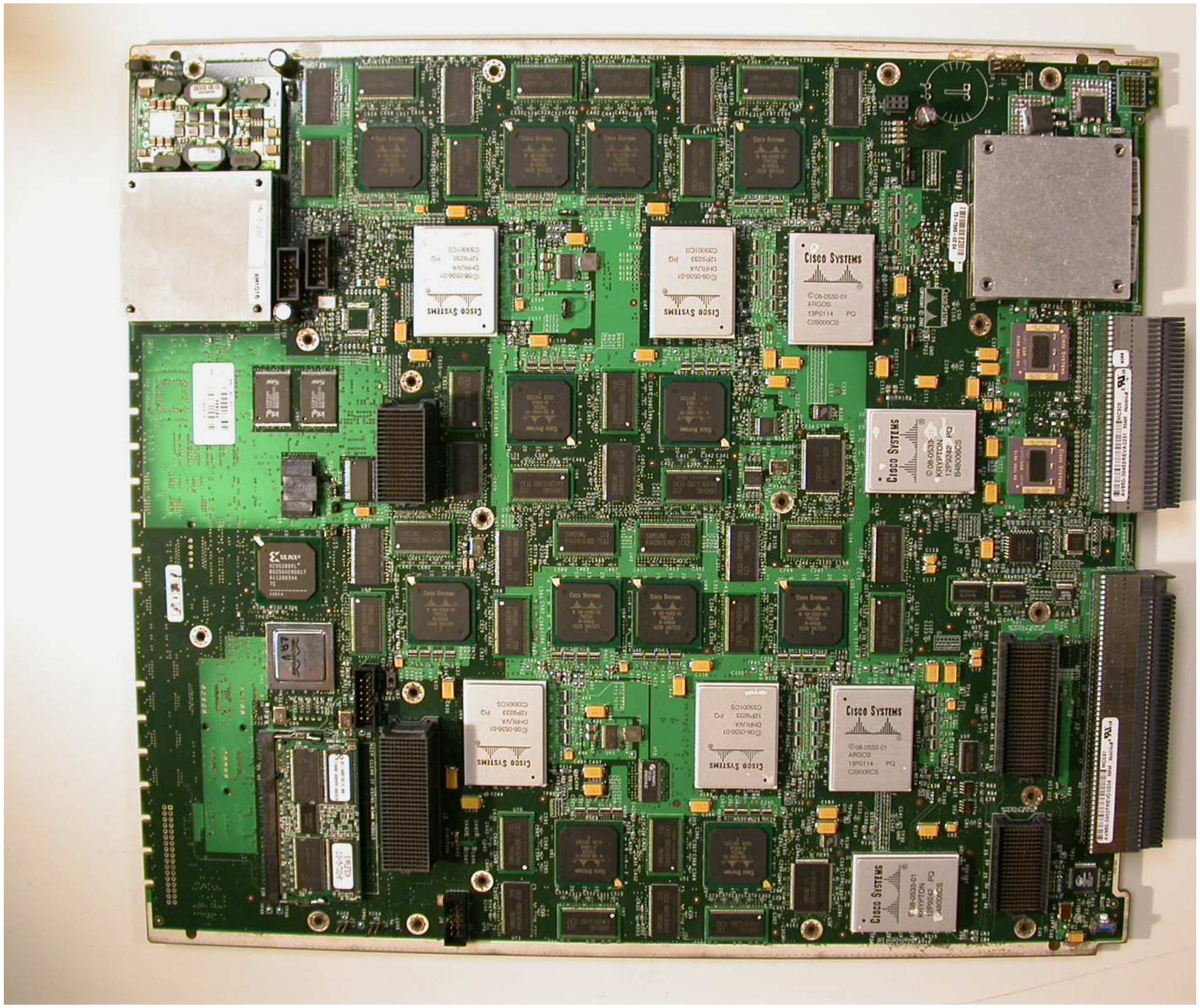
PCB Evolution from 1999 to Present Date

(modular switching platform example)



PCB Example: Test Line Card

circa year 2002

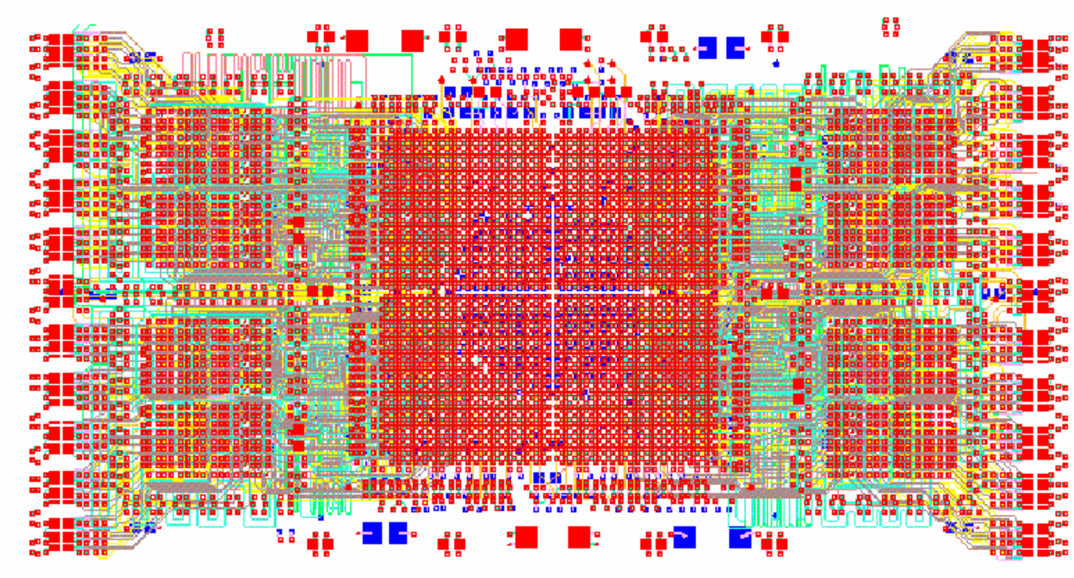


PCB Example: Functional Island

circa year 2003

Nets	534
Connections	998
Vias	3972
Signal layers	8
Plane layers	10

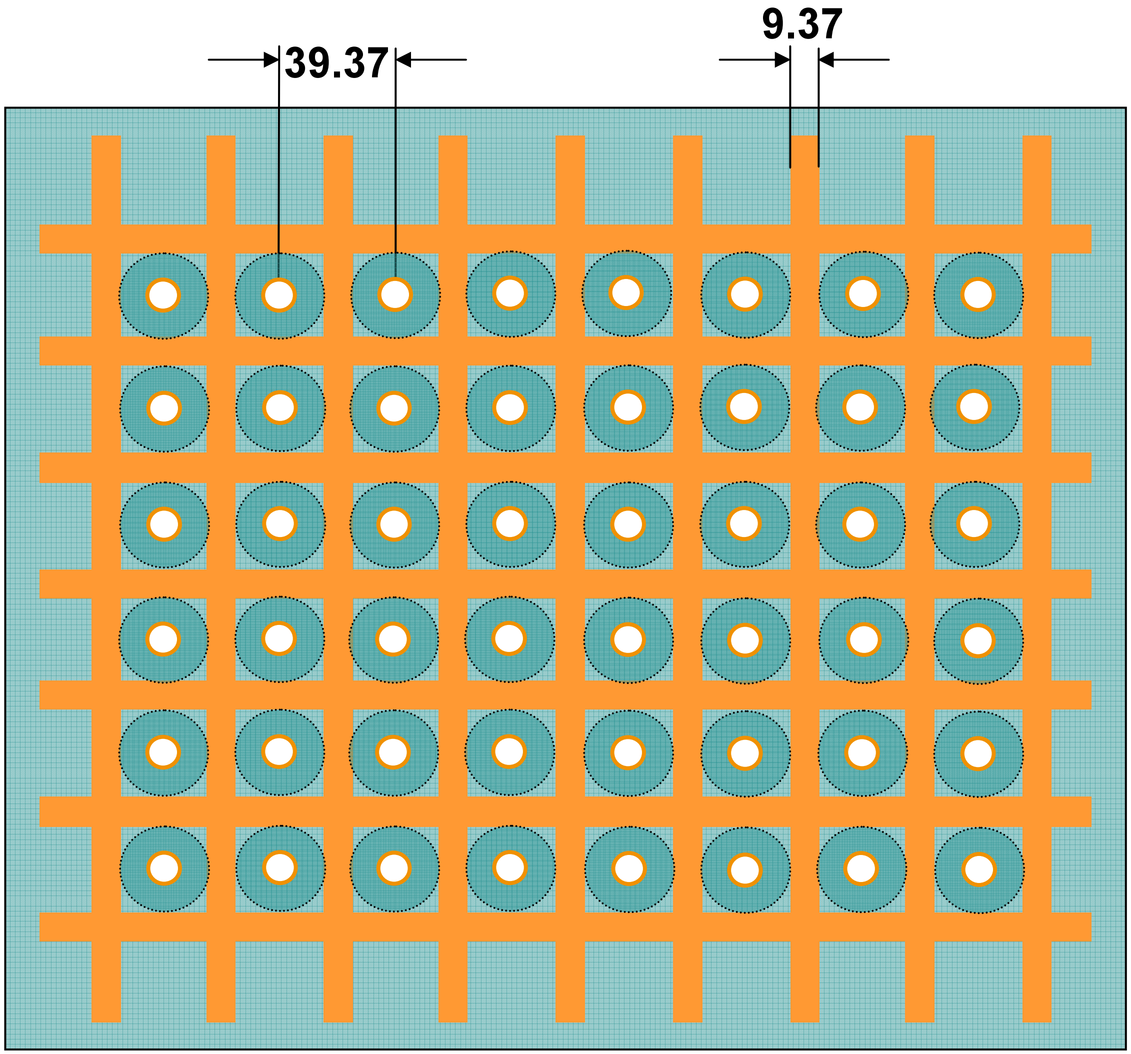
Board area: 3.8” x 2.64” x2 (top and bottom)



ASIC	1
Memories	8
Total components	974
Pins	5193
Total etch length	1222”

Why so many *planes* ?

…because planes are *grids*



The planes under a typical 1mm BGA ASIC show a high degree of perforation.

Only about 25% of the area has copper, while the rest is voided to provide the *anti-pad* clearance. This is done in order to avoid shorting the via barrel with the grid shown.

The so called *plane* is a low density *grid.* This fact carries significant electrical and thermal implications.

Silicon, Boards, Packages Trends

Silicon Integration:	90nm and below
Boards:	higher data rates and 1V cores accelerate the transition from today PCB technology to High Density Interconnects (HDI) substrates with µ-vias, to mitigate noise.
Multi package SiPs:	bare die ASIC + CSP1 memories to alleviate the burden placed on the Plated Thru Hole (PTH) based PCBs

Note 1: Chip Scale Package (CSP)

Considerations

- *Architectures* need to be physically implementable
    - Mitigate ASIC SSO noise with hi-speed differential I/Os
    - Lessen the demands on the Power Distribution Network
    - Chip_to_chip serial I/Os
- Holistic Chip / Pkg / Board co-design *methodology*
    - optimize timing, noise, complexity, cost
    - *Smart* ASIC I/O buffers, adaptive, self-timed, de-skewed
- Seek more effective *trade-offs*
    - innovative packaging solutions (SiP, MCP, 3D-stacking) to complement the advances in silicon integration

Testability, Accessibility

- ASICs, Modules, Functional Islands ought to include advanced *self diagnostic* capabilities
  - Higher signaling speeds and smaller features (µ-vias) will greatly limit intrusive probing (e.g. test points)
  - Board and Module quest for density and the deployment of µ-vias will greatly limit oscilloscope and LA access
  - *Life in the lab* will likely change substantially!

Interconnect Challenges at Ultra High-Speed

Ultra High Speed Signaling demands new elements such as digital communications theory, coding and semiconductor physics, as performance enablers

With UHS Systems, manufacturing processes and environmental conditions (temp., humidity) determine the “real-life” characteristics of the materials (e.g. copper and dielectric)

Noise, and more specifically Power-bus noise and its effects on jitter, is one new salient performance limiter!

This is yet another Paradigm Shift!

Interconnects and Packaging Engineering

for Ultra High Speed Systems

ULTRA HIGH-SPEED INTERCONNECTS REQUIRE THE APPLICATION OF ADVANCED PACKAGING DESIGN PRINCIPLES TO THE PHYSICAL REALIZATION OF GUIDED WAVE STRUCTURES FOR DIGITAL DATA COMMUNICATION CHANNELS[1] WITHIN SYSTEMS.

CIRCUIT THEORY, ELECTROMAGNETIC FIELD ANALYSIS, MATHEMATICAL MODELING, NUMERICAL SIMULATION

ALL CONVERGE,

AND ARE USED TO DRIVE THE MULTIDISCIPLINARY DESIGN OF MANUFACTURABLE AND RELIABLE SYSTEM INTERCONNECT[2] STRUCTURES[3]

(1) A *Channel* is defined as the Silicon-to-Silicon path

(2) The physical and electrical connection of a signal, its associated return paths and its Power Distribution Network

(3) Transmitter, substrate, balls, PWB traces / vias / pad-stacks, connectors, backplane, all the way up to the receiver

UHS Interconnects Engineers
…the SI engineers’ evolution

FREQUENCY – DOMAIN ANALYSIS

S – PARAMETERS, SMITH CHARTS

LAPLACE and FOURIER TRANSFORMS

EMBEDDING, DE-EMBEDDING

CONVOLUTION

COMMUNICATION THEORY, CODING

STATISTICS

UHS Design Elements

- **Statistical design**
  - ➢ **Realistic worst-case conditions (probability of occurrence)**
  - ➢ **Up-front analysis of parameter sensitivity**
  - ➢ **Knowledge of parameters distribution (mean, skew, variance) w.r.t. manufacturing process and environmental conditions**
- **Simulation**
  - ➢ **Vary input parameters over user - defined distributions**
  - ➢ **Sensitivity analysis to find variables interaction, dependence**
  - ➢ **Monte Carlo analysis to realistically estimate system limits**

Access to process parameters distribution requires strong teamwork and collaboration with different organizations, ecosystem

UHS Design Elements

- Data sorting
  - Find simulation output trends vs. system parameters variation
- Design optimization
  - Determine the optimal centering of the design, to
  - Obtain maximum margin

Monte Carlo analysis with real parameters distributions produces timing and noise margin distributions that reflect the real system performance

Outcome:
a better understanding of the design

The resulting distributions can be used to predict the likelihood of producing a defective system.

Within reason this defect level guarantees performance, to a certain point, depending on the desired *confidence*.

Hence, this outcome can be used as an indicator of Quality

Models Evolution

- I/O models
  - Matlab (equalization, DFE, …)
  - IBIS v4.1 (VHDL-AMS, Verilog-AMS)
  - ICM v1.0 (more for connectors, cables, PCB, etc.)
  - several emerging formats (mostly proprietary thus far)
- Interconnect models
  - Rapid change from behavioral to structural
  - Vias, interconnects modeled as microwave structures; the same applies to other transitions, ASIC packages, solder balls, etc.
  - Structural Models inclusive of materials electrical and thermo-mech properties, manufacturing process and environmental variations
  - Surface finishing deserves much greater attention than in the past!

This shall originate new model libraries for simulation as well as a new generation of CAD symbols

Methodology Evolution

from *measurement-based* to *predictive*

- **Measurement based**
  - ➢ 1 backplane, 1 man/month, 1 lab *…for 1 data point!*

- **Predictive Channel Analysis**
  - ➢ Simulation based Channel Analysis
  - ➢ Simulate millions of bits / hour
  - ➢ Integrated with layout: read / write CAD board files
  - ➢ Simulate complex driver, receivers, equalizat., process + environm.
  - ➢ Determine optimal tap setting

  - ➢ **Test Vehicles:** complement simulation with *ad-hoc* heuristics
    - Materials analysis: assembly process development, early statistics / distributions
    - Performance analysis: traces, vias, CB-vias, connectors

Conclusion: a *holistic* approach

Solutions to future High - Speed Interconnects and Packaging Engineering challenges will result from a multidisciplinary effort based upon proven Science and the concurrent electrical, physical, and thermo-mechanical design-space definition of the interconnects and dielectric materials, from transmitter to receiver, across the connectors and backplane, with the related processes and conditions.

(This statement is based upon our measured results and observations)

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