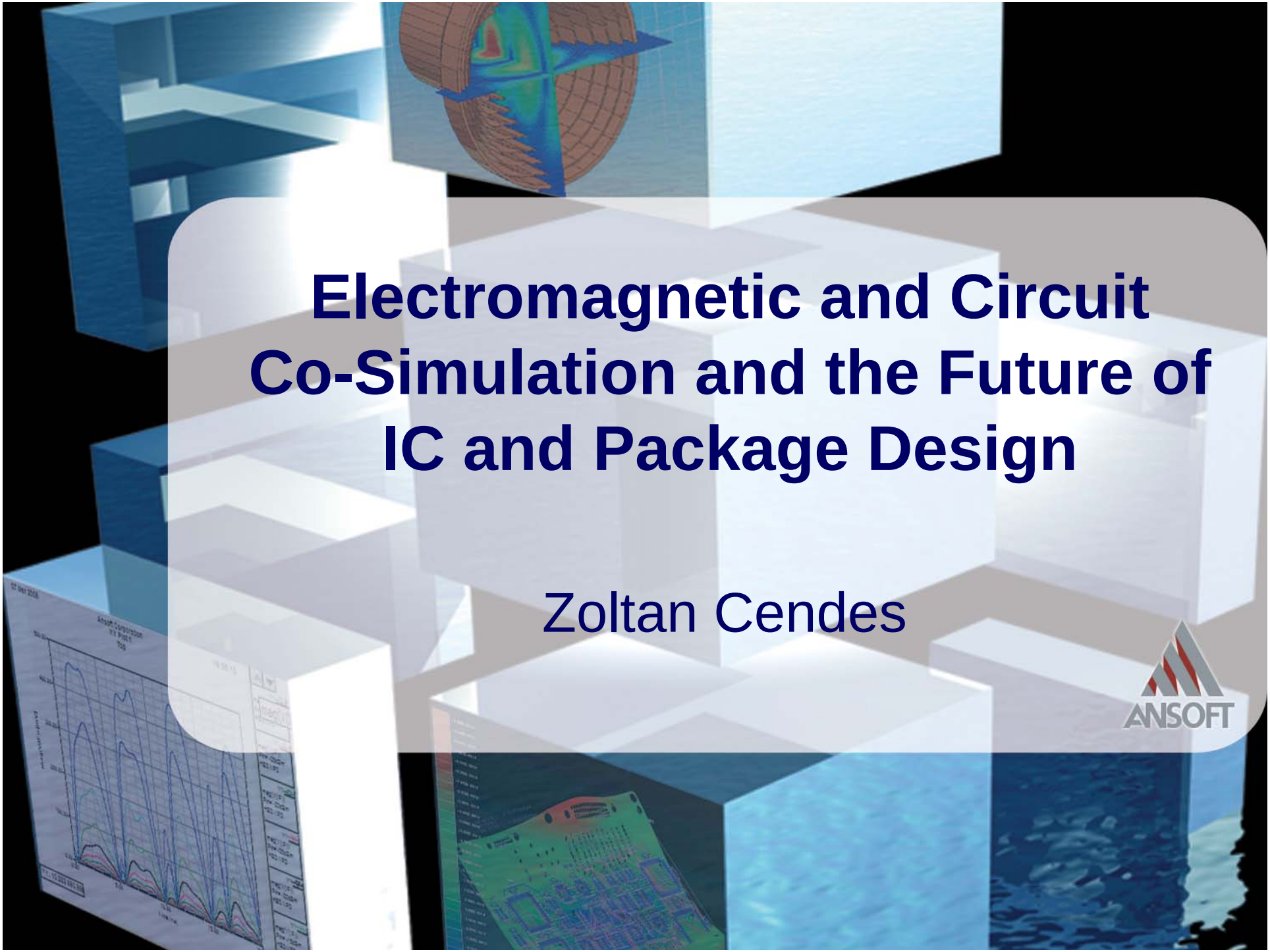
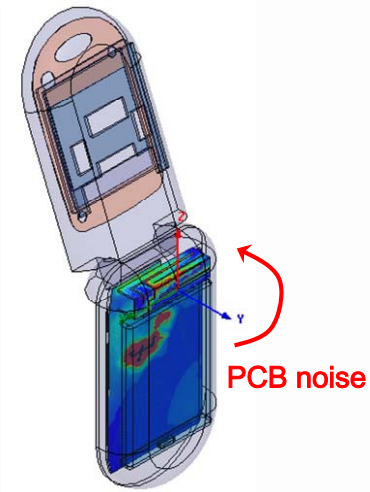


Electromagnetic and Circuit Co-Simulation and the Future of IC and Package Design

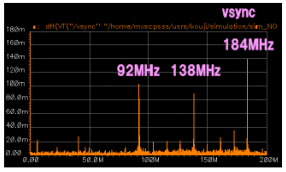
Zoltan Cendes

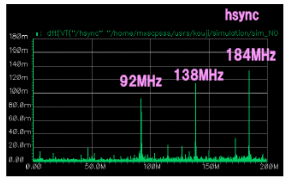
ANSOFT

Wireless Consumer Devices



System SI Predicts Receiver Desensitization





System EMI Predicts Display Anomaly

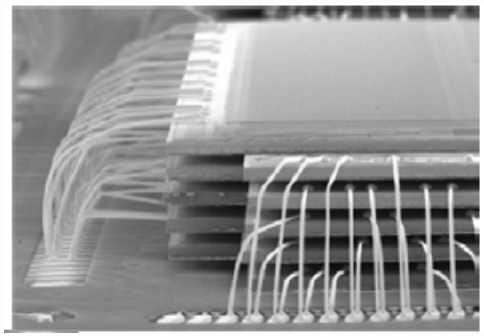
2006 model
SCH-B570

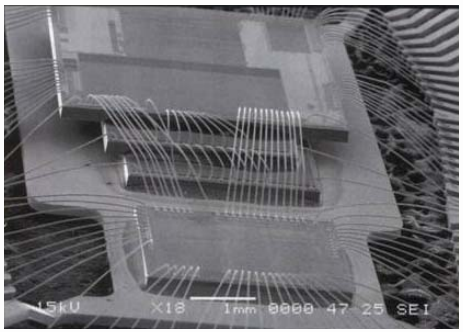
8 GB HD (16 movies)
2 Mp camera
GPS
MP3 (1600 files)
Picture in picture

New devices integrate RF/Analog/Digital with Memory, Graphics, Storage, GSM radio, Bluetooth/802.11x radio, Antenna, LCD, camera, MP3, and broadcast FM

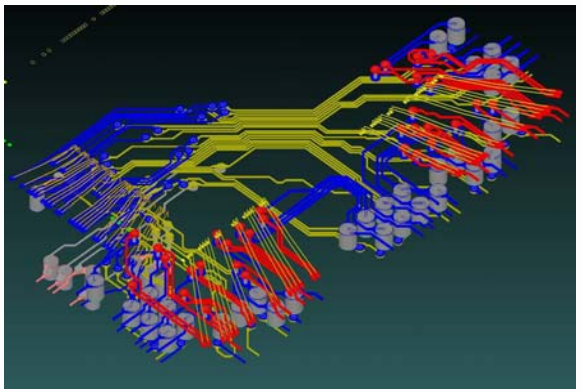
***Trend*: High performance consumer electronics dominates/drives semiconductor market**

System in Package (SiP)

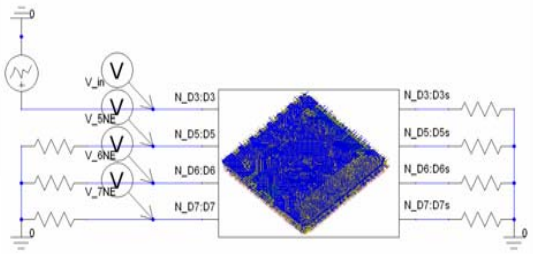


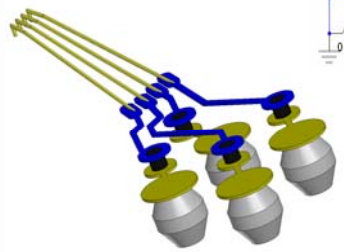


3D SiP SEM Images courtesy of ST Microelectronics



Package on Package (PoP)
courtesy Philips Semiconductor



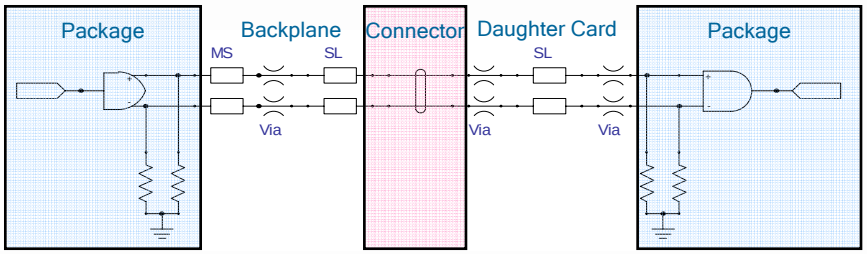


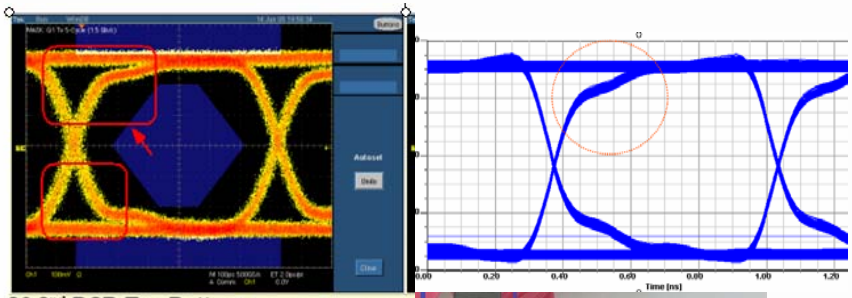
Parameterization of critical interconnect

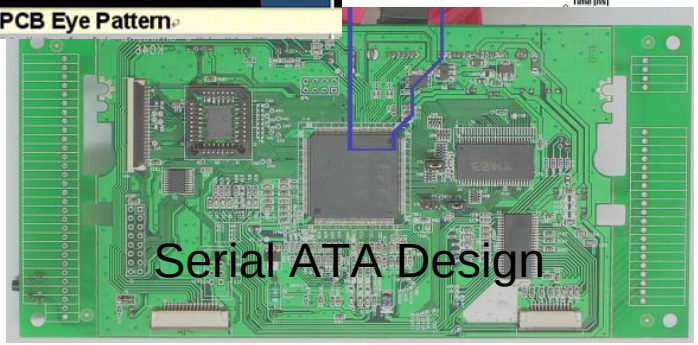
***Trend*: Pervasive communications leads to greater integration driving stacked die, package on package (PoP) 3D packaging solutions**

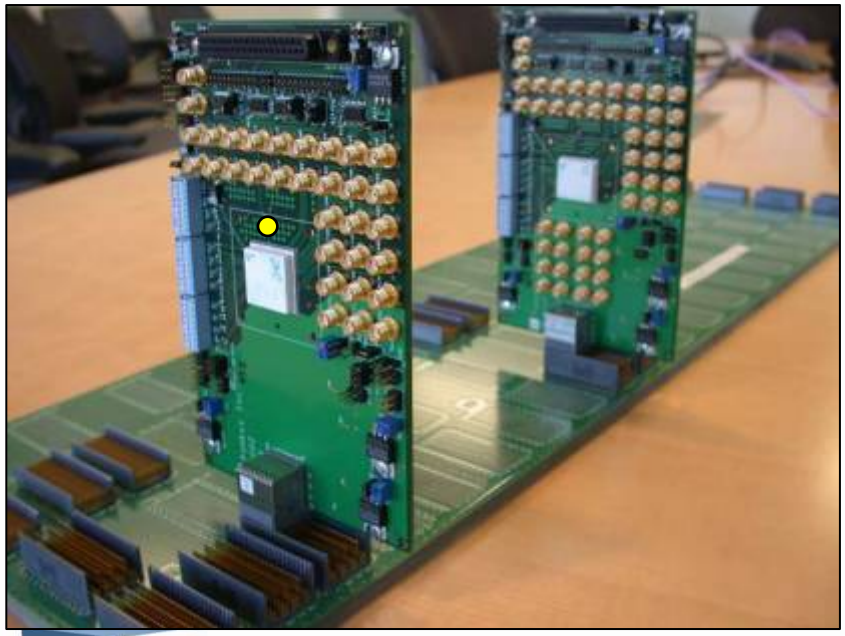
Chip/Package/Board Co-Design

Signal Integrity









***Trend*: Cost/performance targets drive the integration of IC's, SoCs and SiPs onto low cost printed circuit boards. Chip/Package/Board Co-design is required**

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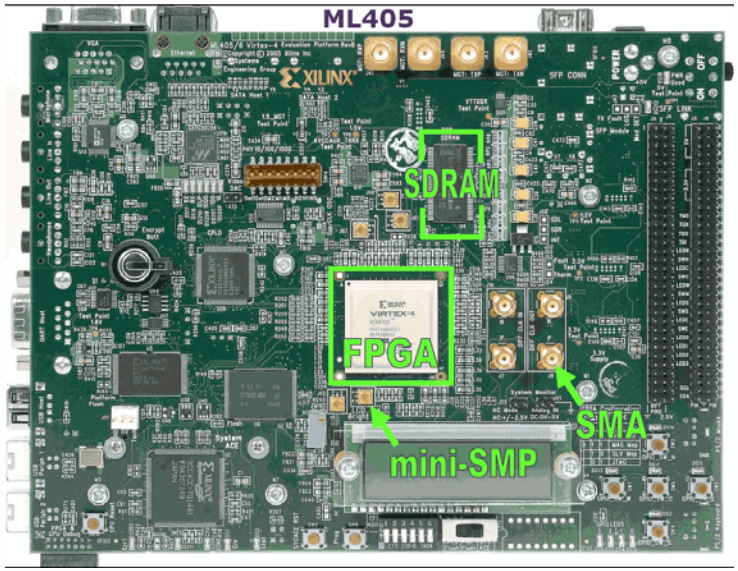
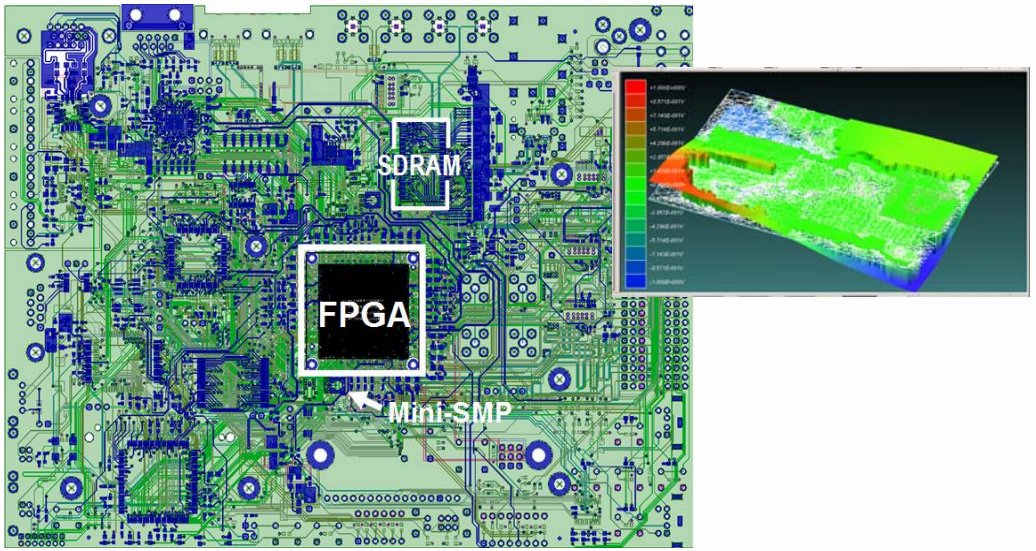
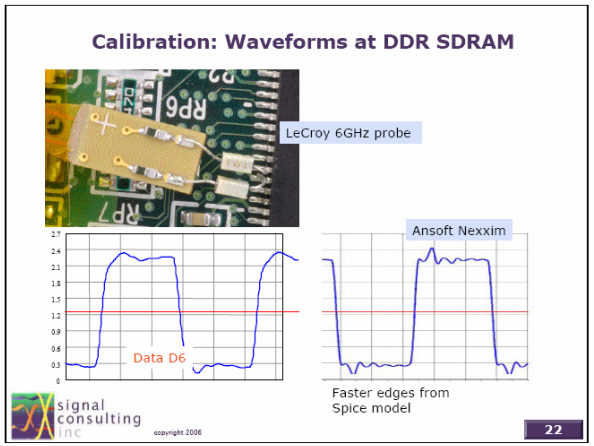
Chip/Package/Board Co-Design

Power Integrity



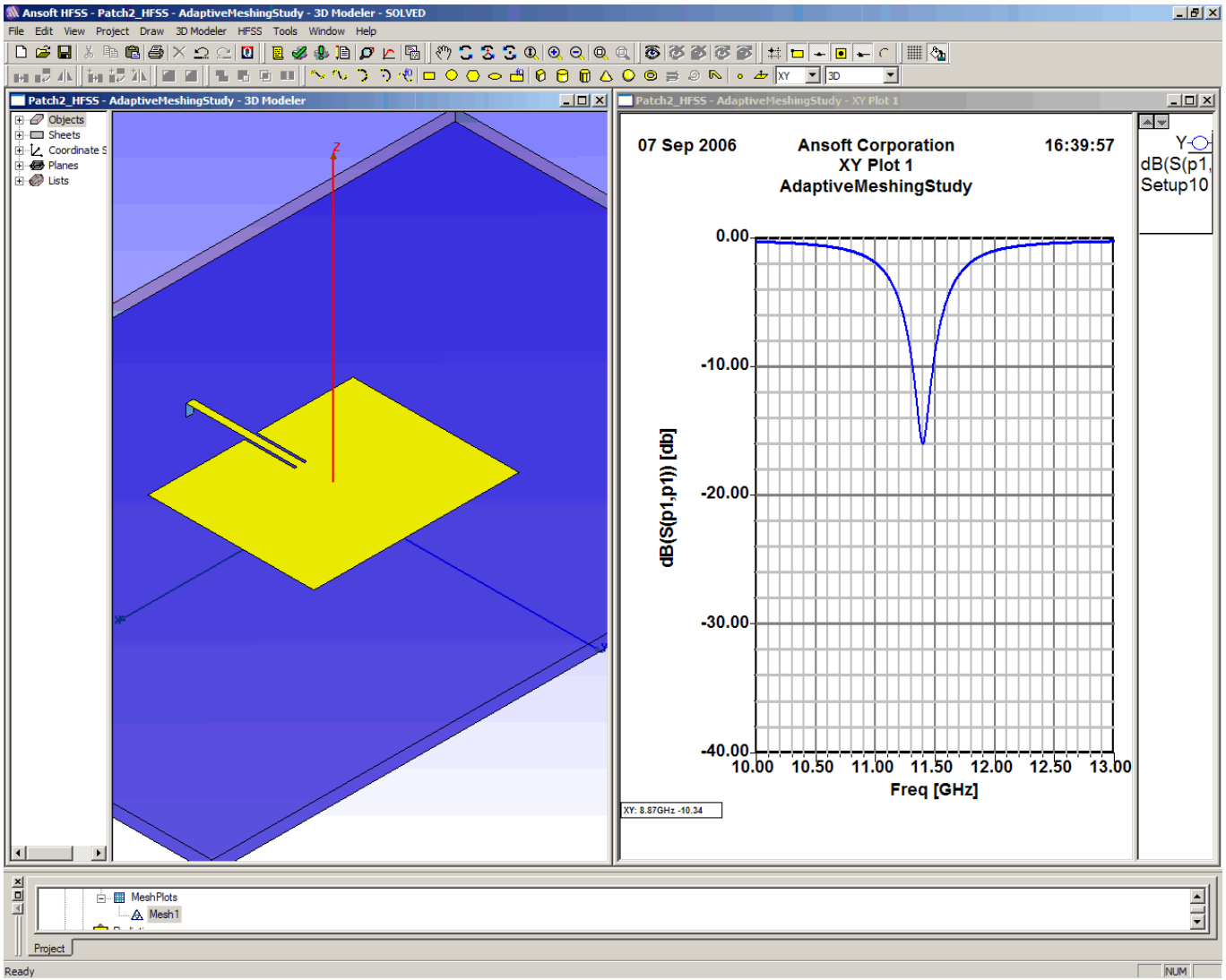




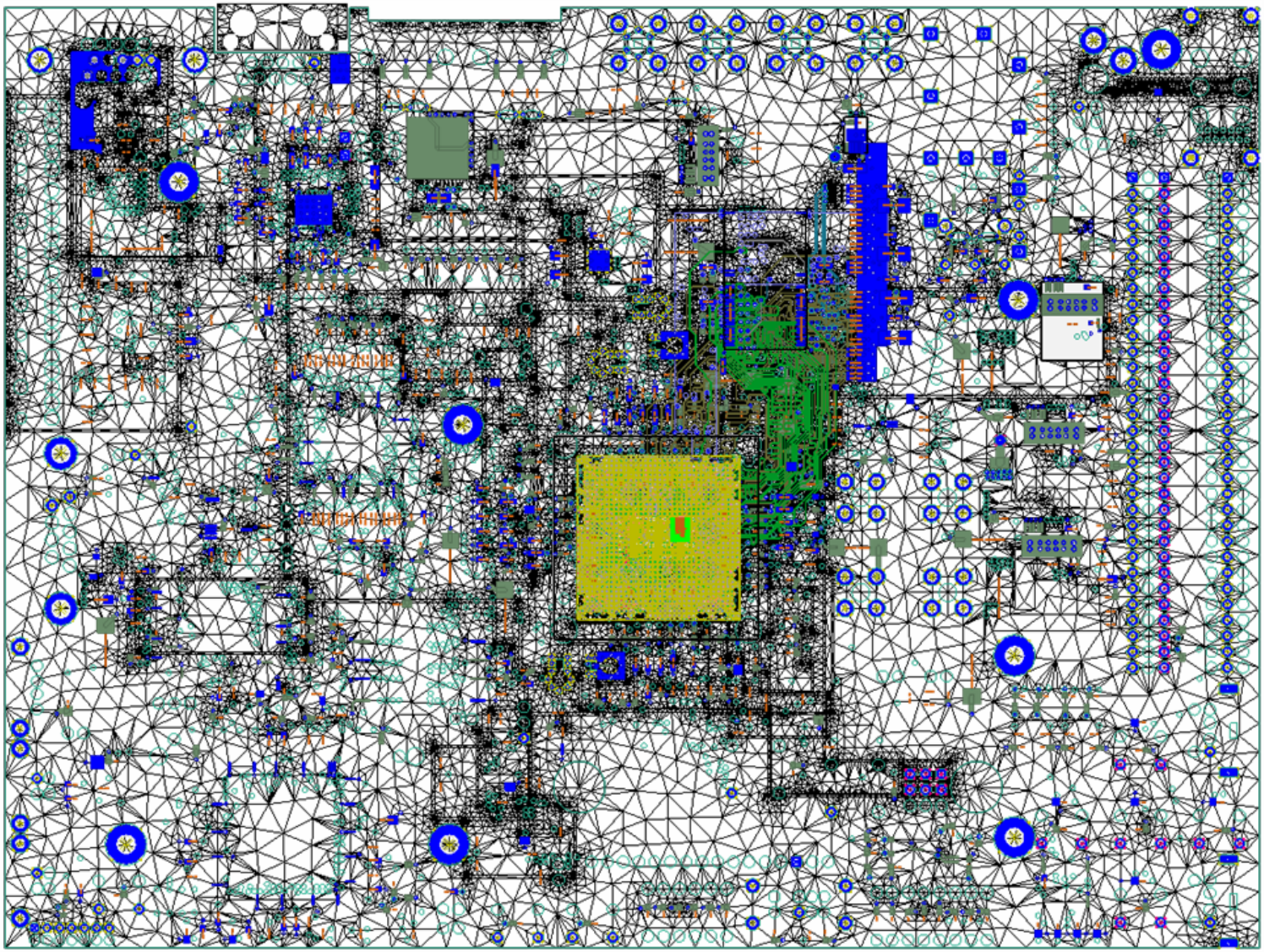
Courtesy of Xilinx Inc. and Dr. Howard Johnson
"Virtex™-4 Power System Performance"

***Trend*: Cost/performance targets drive the integration of IC's, SoCs and SiPs onto low cost printed circuit boards**

“Adaptive” Mesh Refinement



Adaptive Mesh – Package on PCB

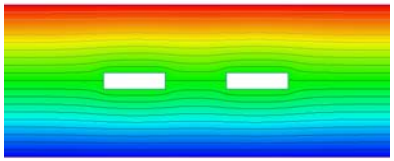


Ultra-Fast Finite Element Simulation of Planar Electromagnetic Structures

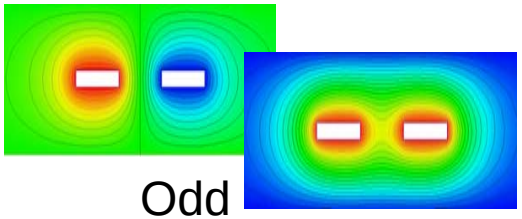
SIwave

- Complex, multi-layer PCB's and packages are predominantly planar structures
- Planar modes and transmission line modes are orthogonal and may be treated separately

Parallel Plate Modes



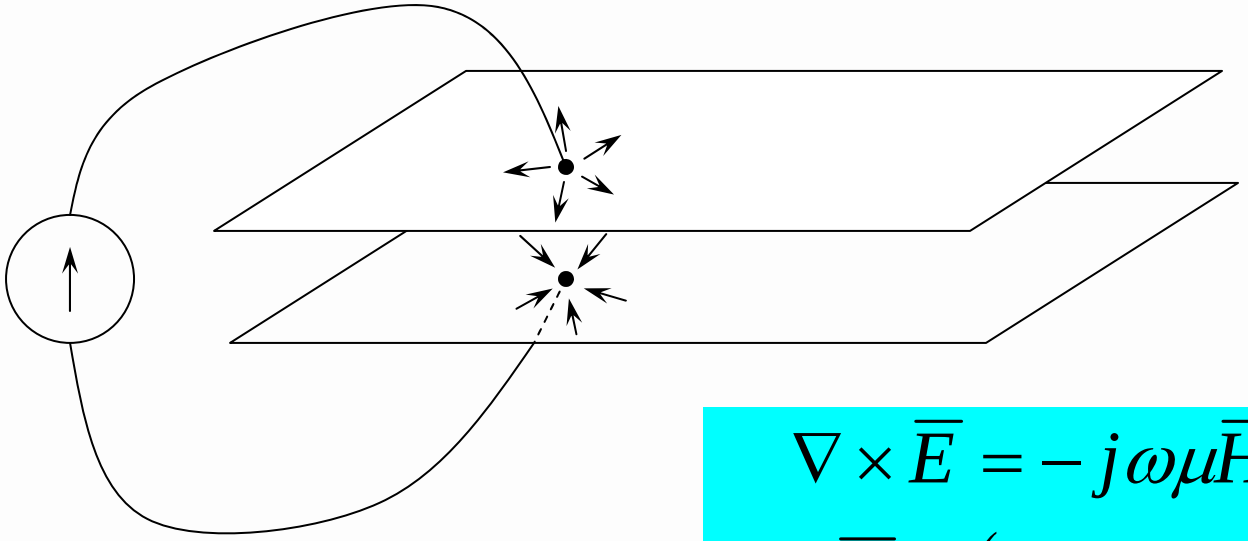
Transmission Line Modes



Odd

Even

2D for Planes – 3D for Vias



Power and Ground planes

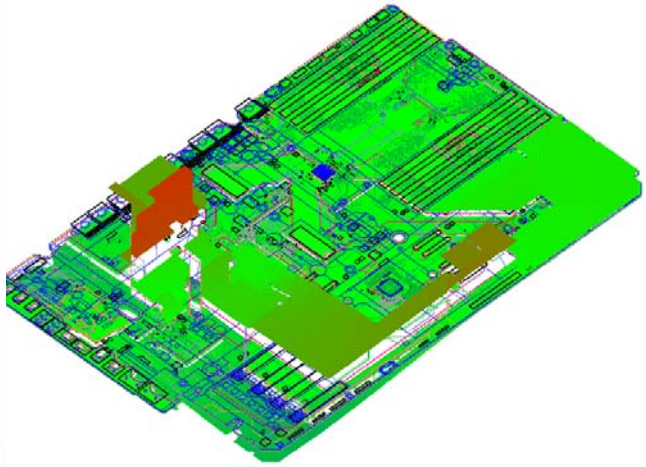
$$\nabla \times \bar{E} = -j\omega\mu\bar{H}$$
$$\nabla \times \bar{H} = \left(j\omega\varepsilon + \sigma_d\right)\bar{E}$$

Voltage drop between planes

$$V = E_z d$$

$$\bar{J} = \hat{z} \times \bar{H}$$

Current on bottom plane



SIwave – FEM Formulation

$$\frac{1}{(R+j\omega L)}\nabla^2 V-(G+j\omega C)V=I_s$$

Applying Galerkin's method

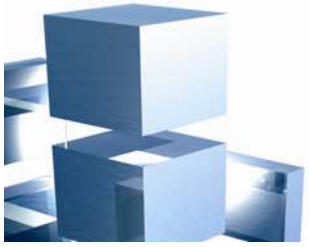
$$\left[\frac{1}{(R+j\omega L)}S-(G+j\omega C)T\right][V]=[I_s]$$

$$G(\omega)=\frac{k_0\varepsilon_r\tan(\delta)}{d\eta_0}$$

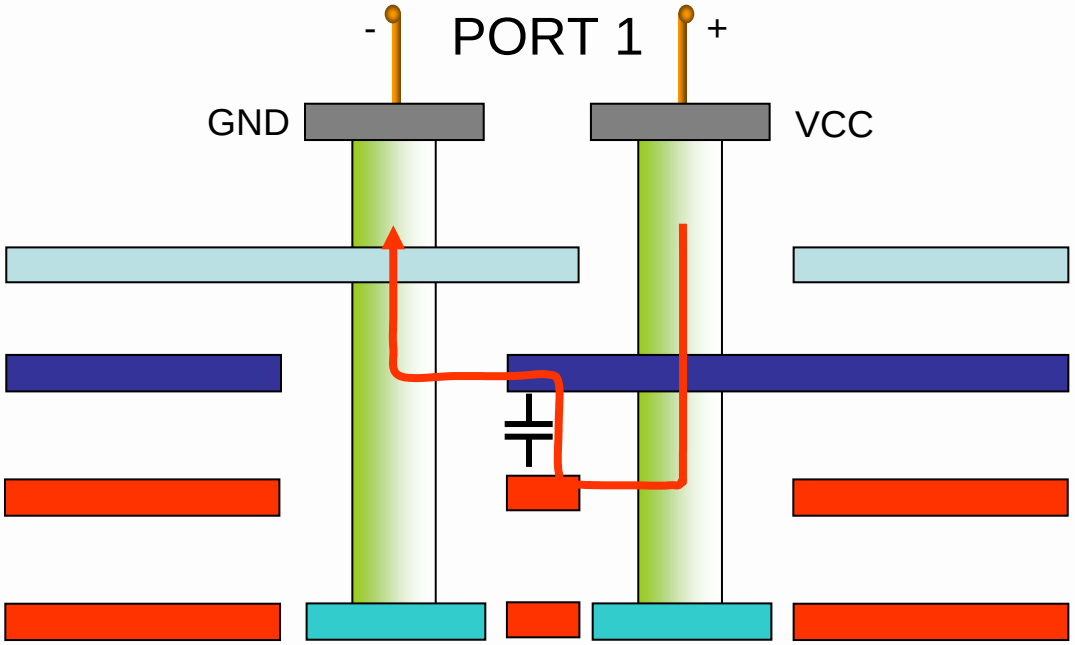
$$R(\omega)=\sqrt{\frac{\eta_0\mu_r k_0}{2\sigma_m}}$$

$$L=\mu d$$

$$C=\frac{\varepsilon}{d}$$



Vias

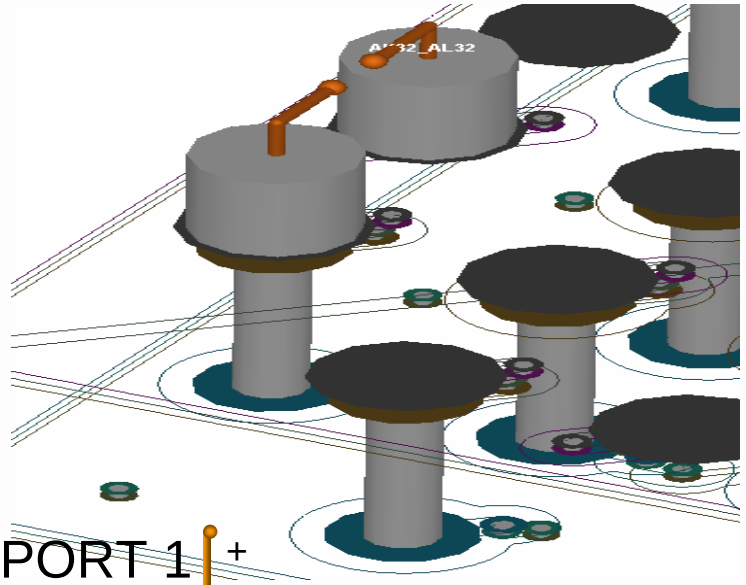


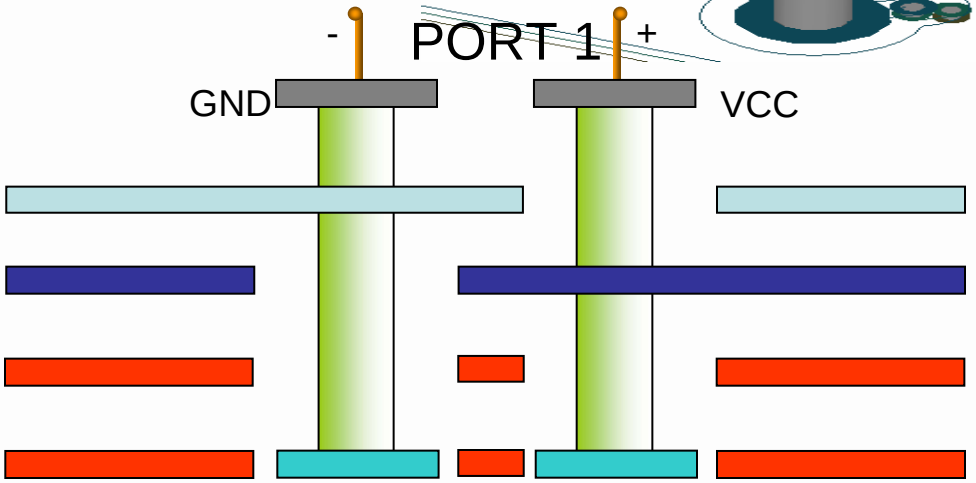
Example Stackup

- Solved parametrically using HFSS
- Inductance based on 3D solution

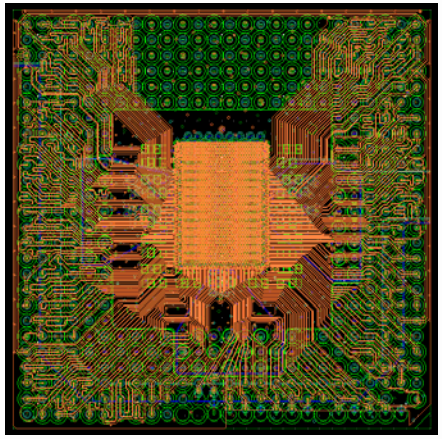
Key Physical Features

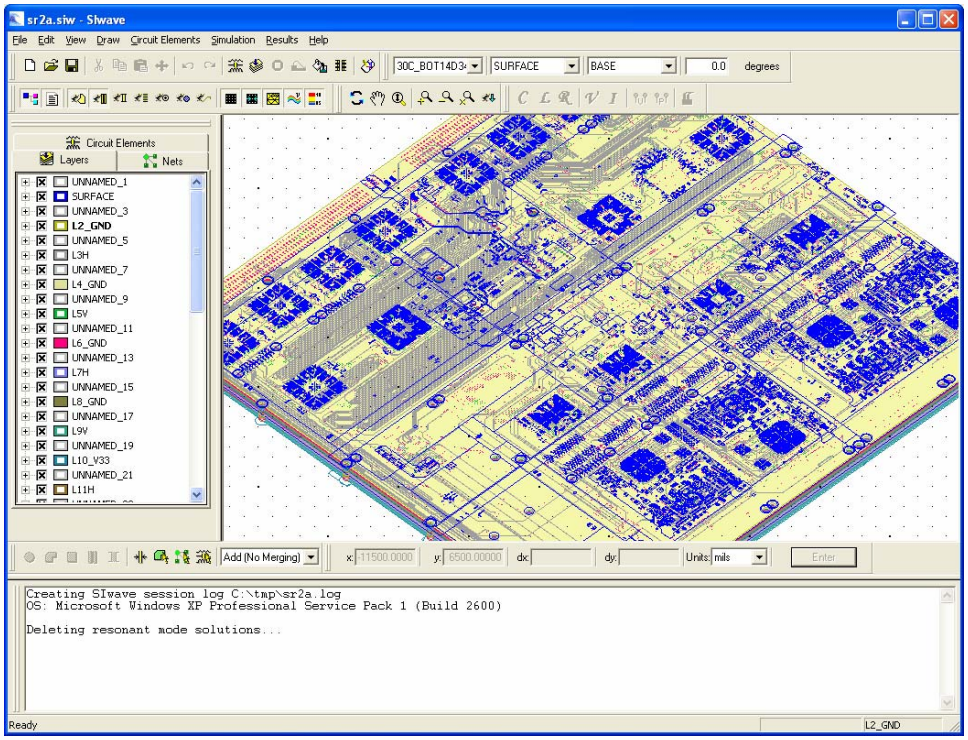
- Some 3D features
  - Solderballs and Solderbumps
- Interconnects
  - Transmission lines
  - Vias
  - Circuit elements
- Coupling
  - Trace-to-trace
  - Trace-to-plane
  - Via-to-plane
  - Via-to-via





Example: Package on Board





- 30 cm by 40 cm board
- 26 metallization layers
- 6500 nets, 210 decoupling capacitors
- Courtesy of EMC Corporation

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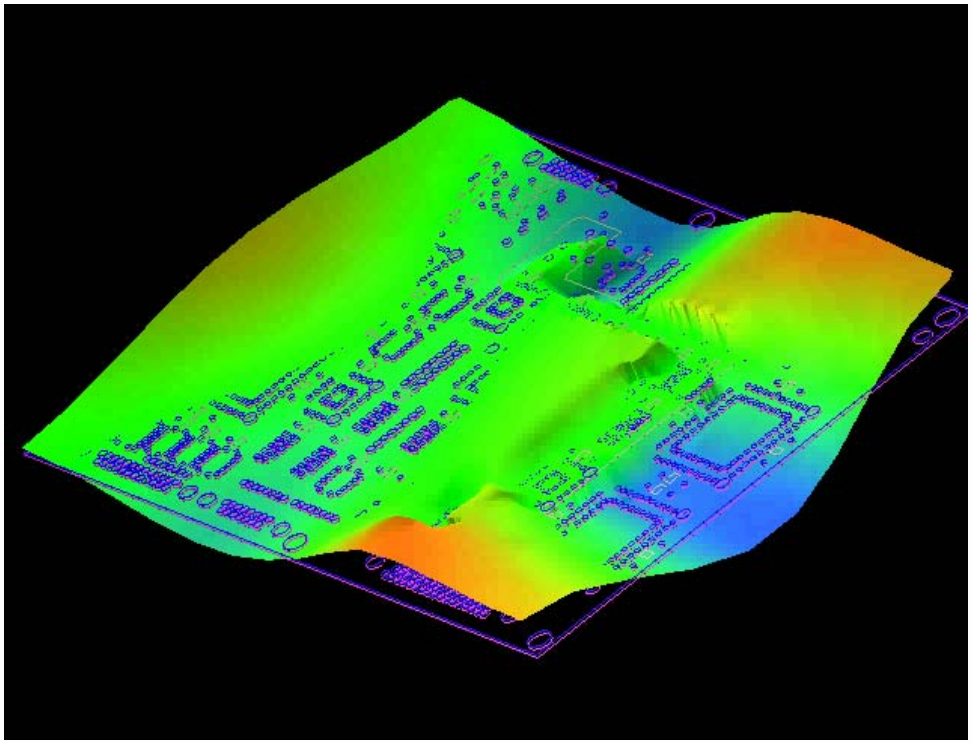
EMC² where information lives

Example: Package on Board



- 30 cm by 40 cm board
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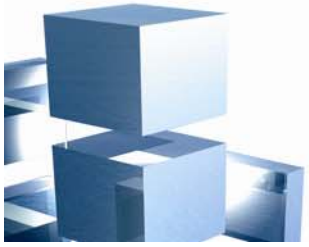
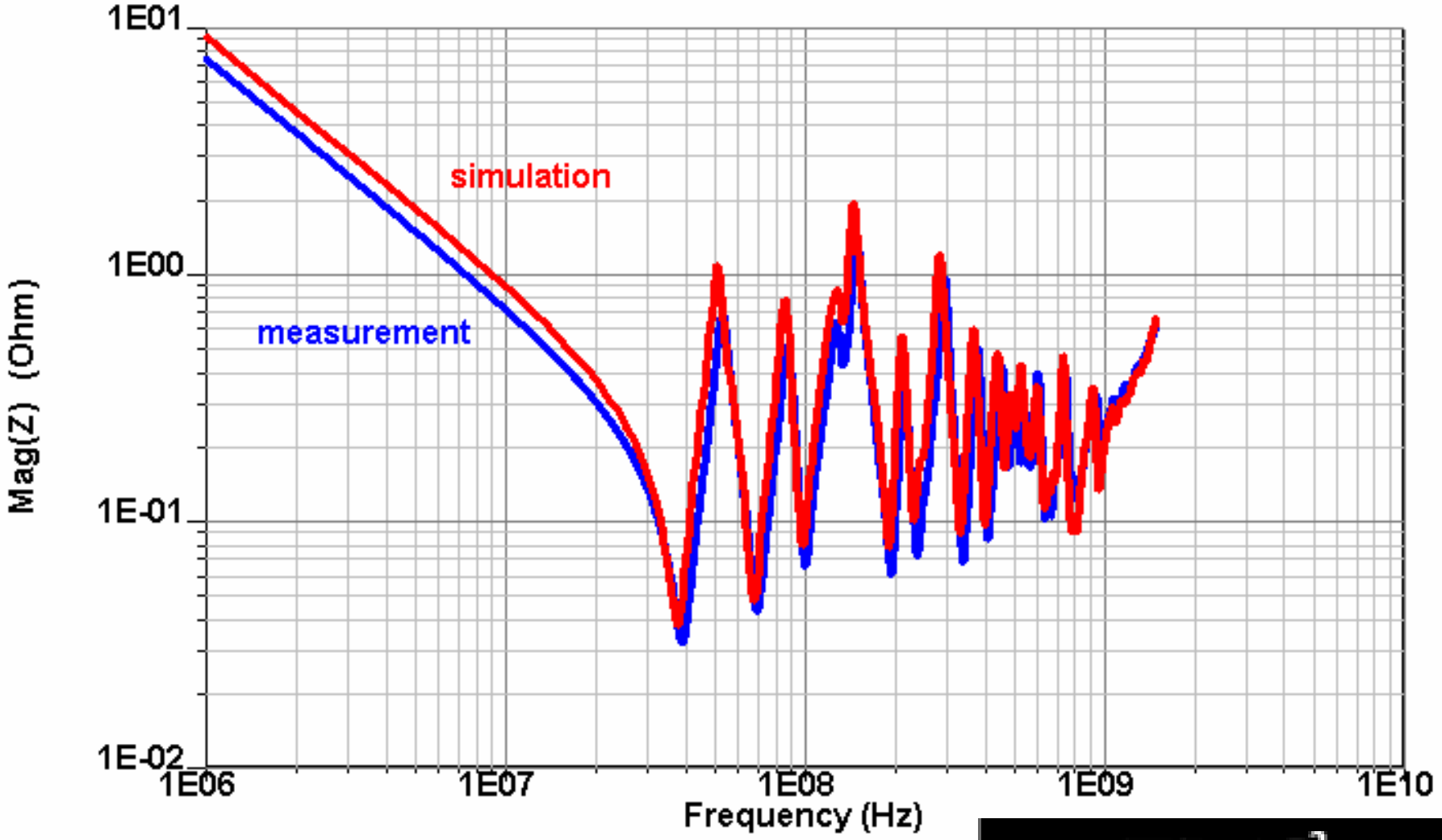


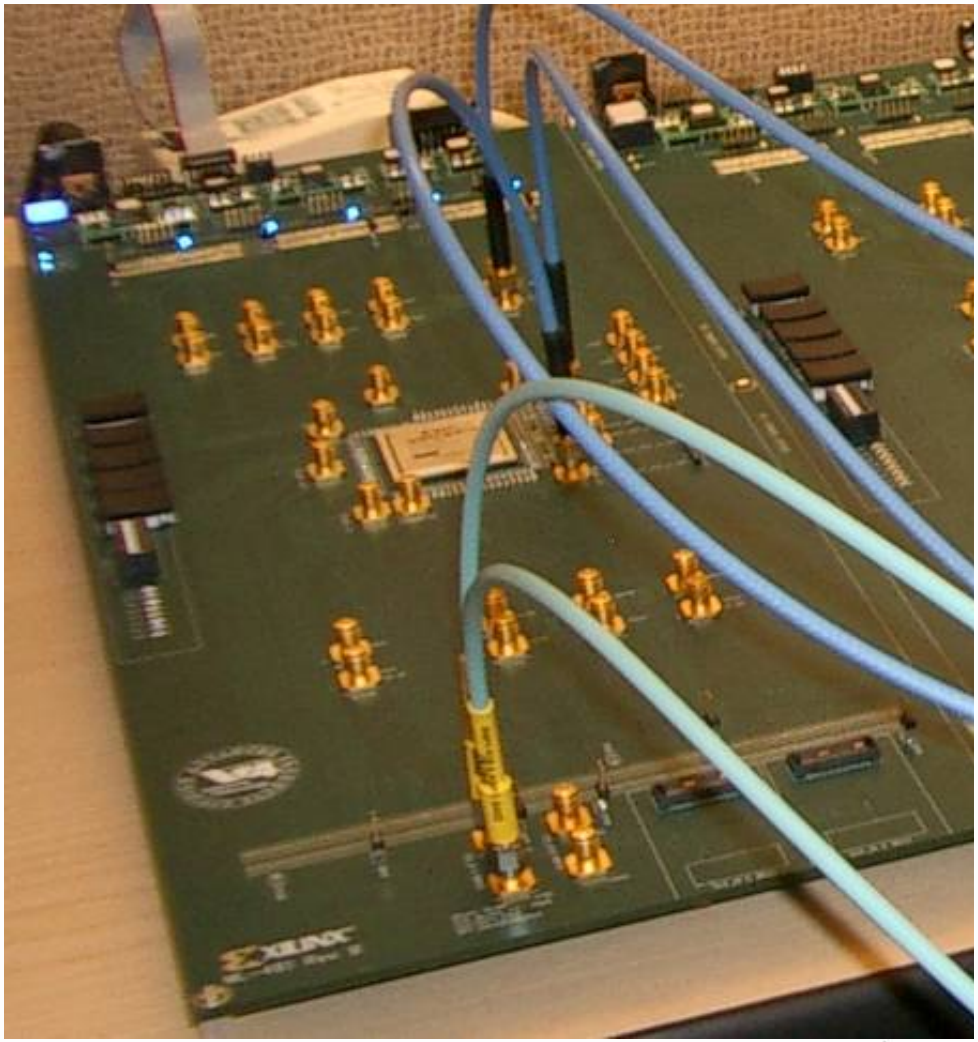
Impedance versus Frequency

Z without decoupling capacitors



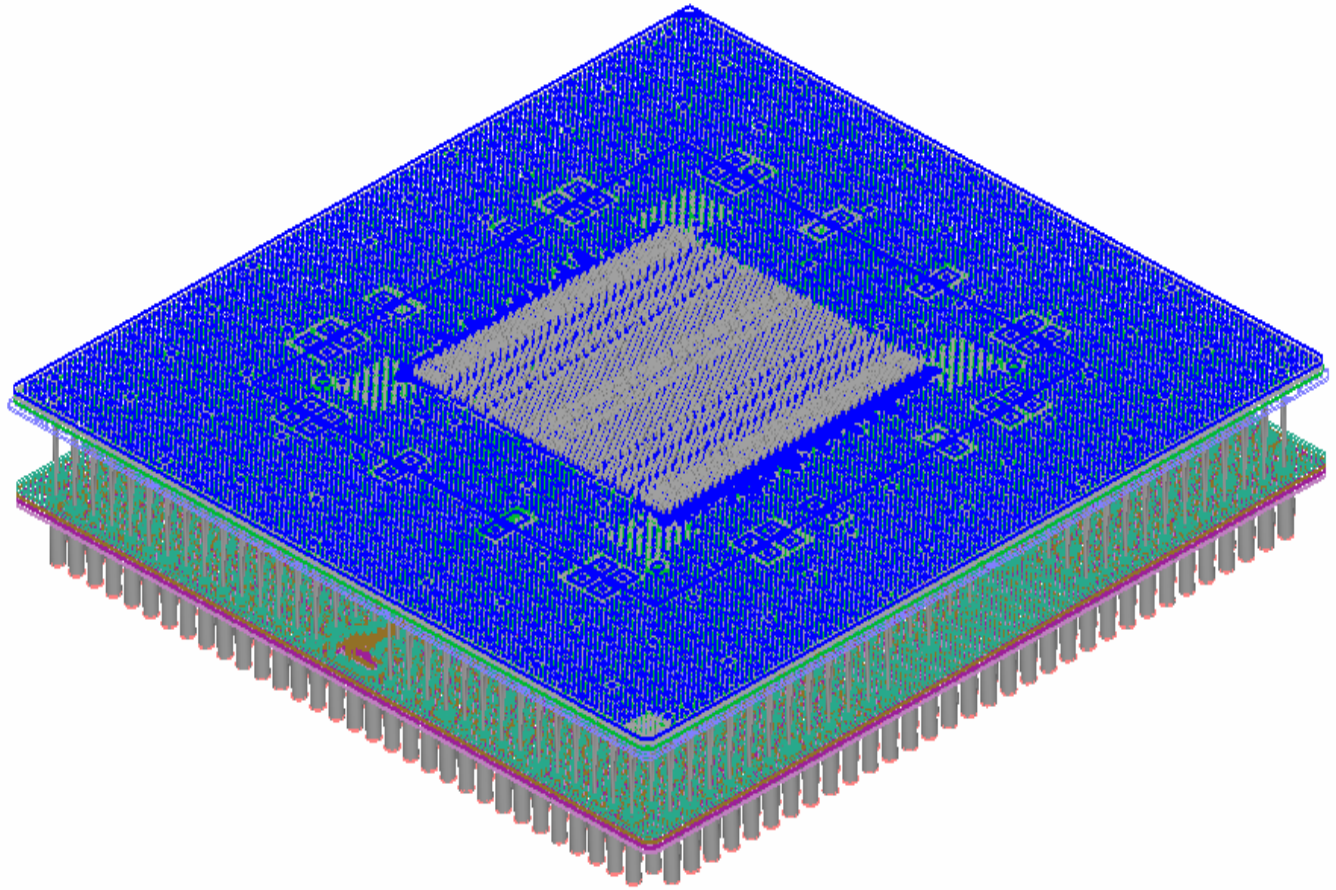
Xilinx ML481 Test Board

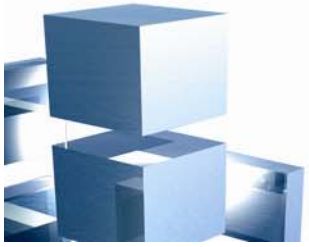
- 8-layer package on 24 layer test board
- Test points are at SMA connectors (Spyholes)
- Lab Measurement by Xilinx and Dr. Howard Johnson, Sigcon



Xilinx FPGA: Virtex-4 LX60 FF1148 Package

- 8-layer flip-chip BGA package
- Single Core
- 34 x 34 mm
- 1148 Balls





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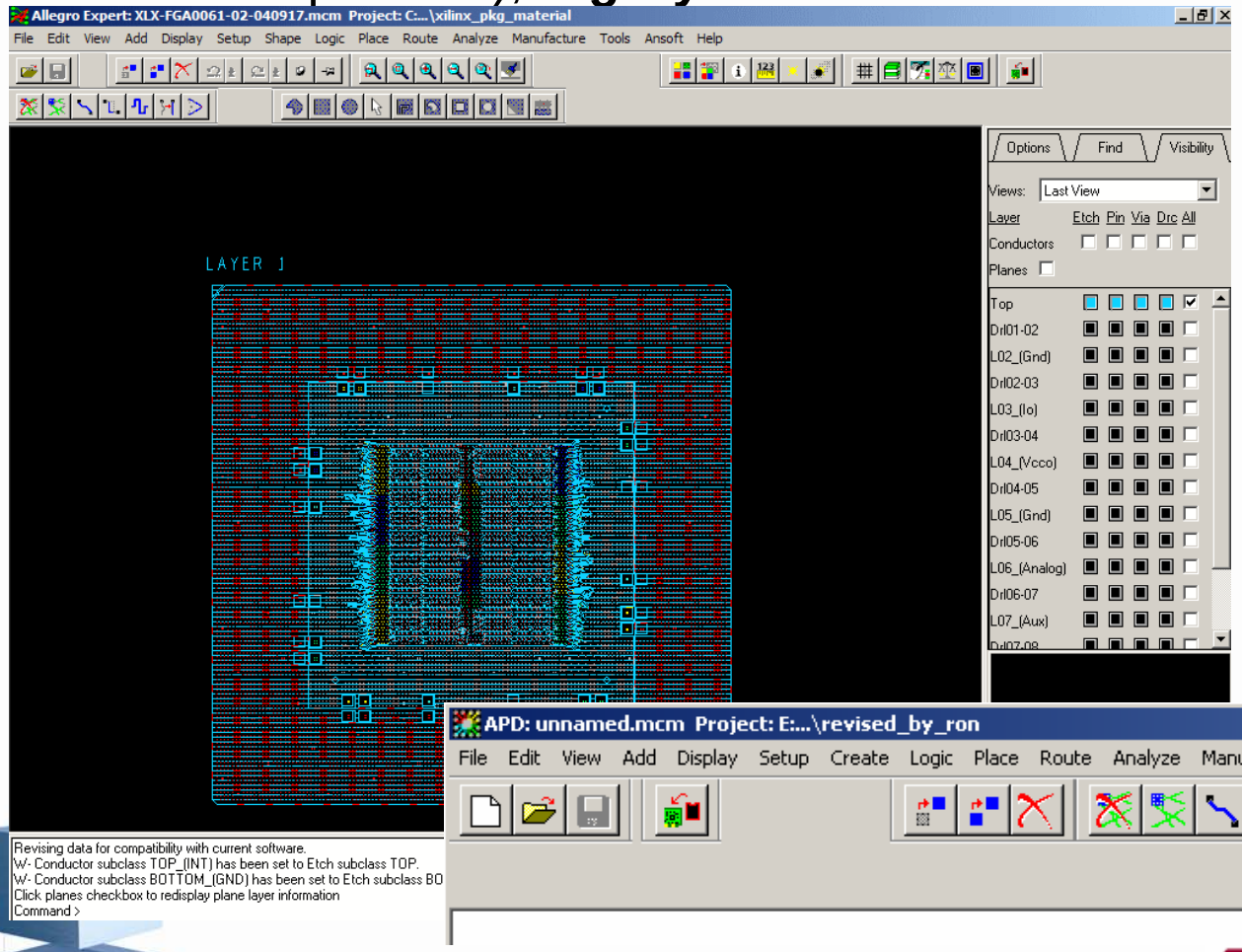
Xilinx Virtex-4® FPGA

➢ AnsoftLinks

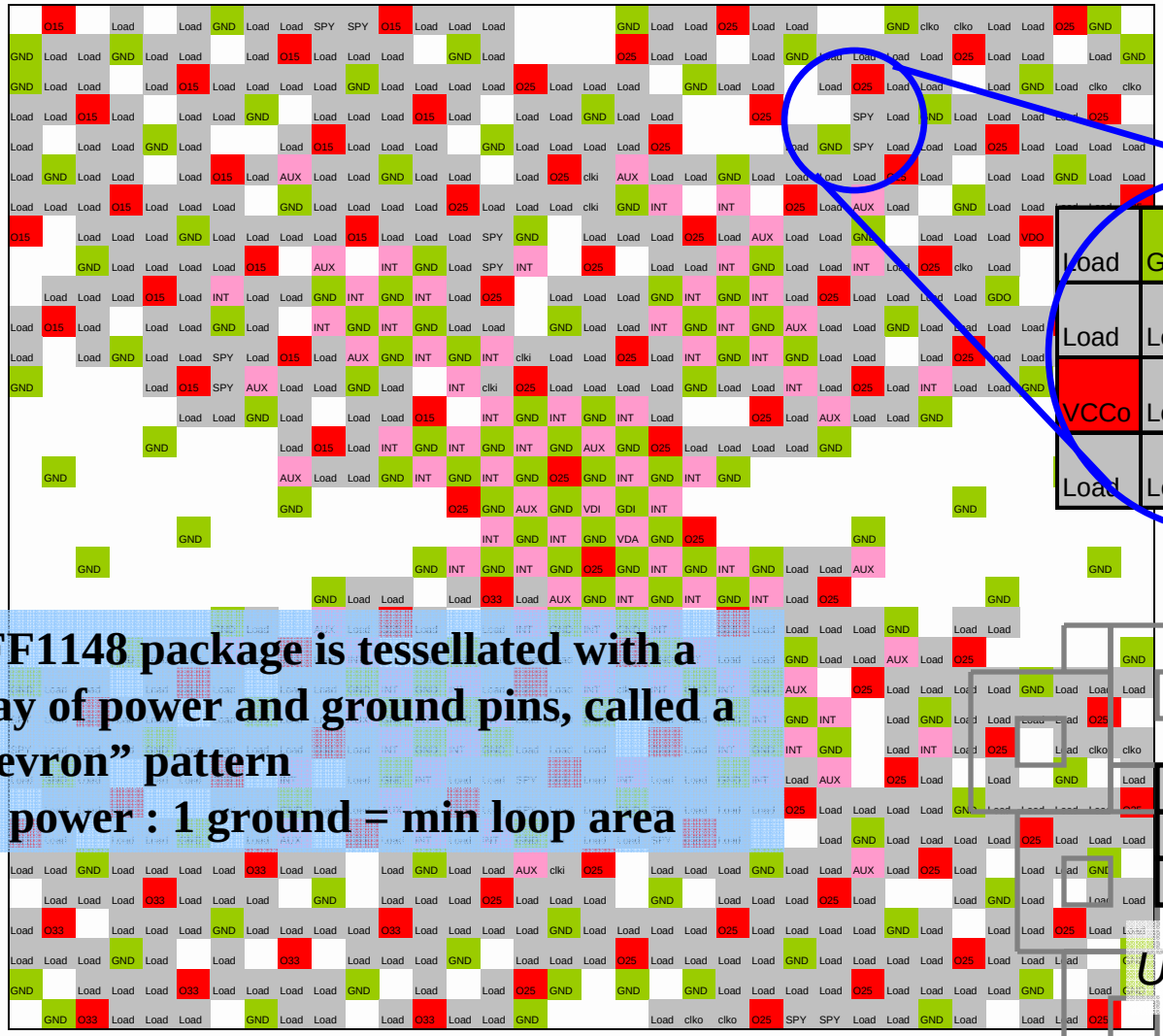
- ➢ **Cadence** (APD, Allegro), **Mentor** (Boardstation, PowerPCB, Expedition), **Sigrity** Encore and **Zuken** CR5000

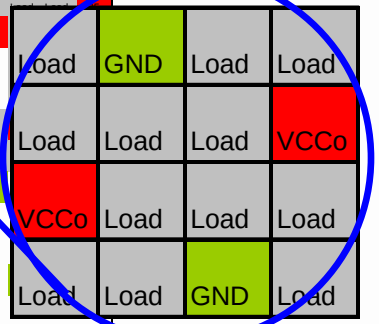


Cadence Advanced Package Designer (APD)

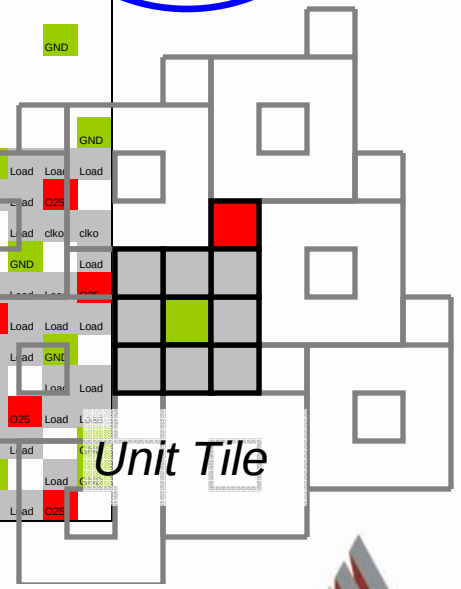
Access directly from APD

Package Pinout





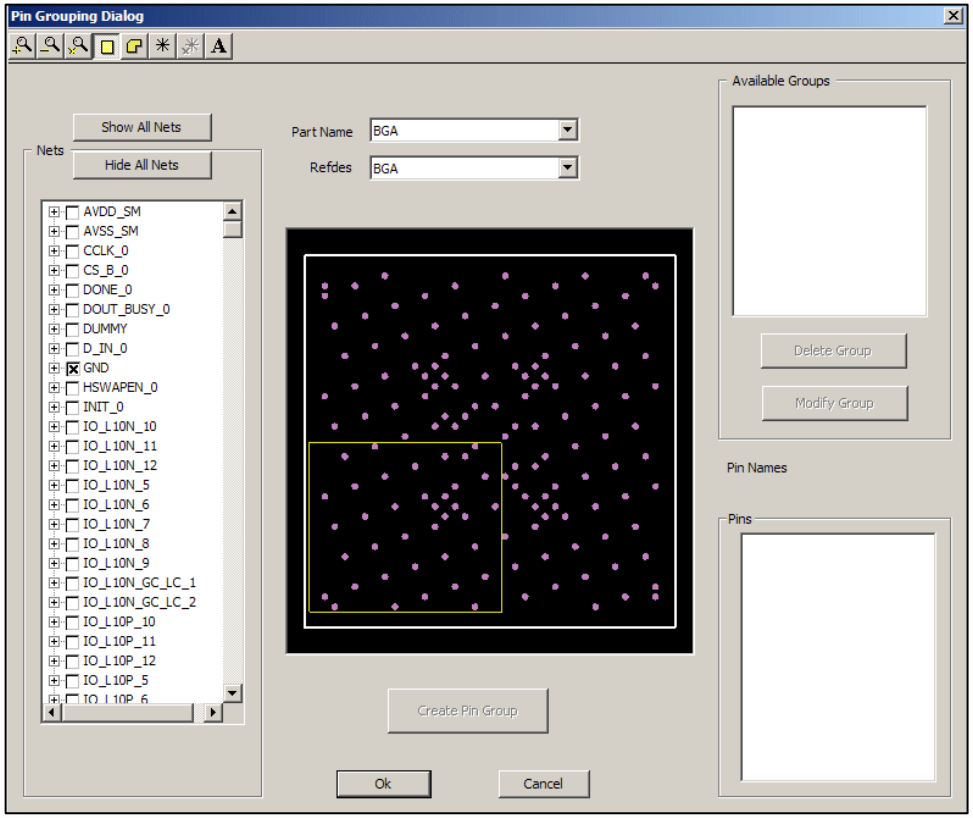
The LX60 FF1148 package is tessellated with a regular array of power and ground pins, called a "Sparse Chevron" pattern
8 signals : 1 power : 1 ground = min loop area



Ref: BGA Crosstalk by Howard Johnson, March 1, 2005

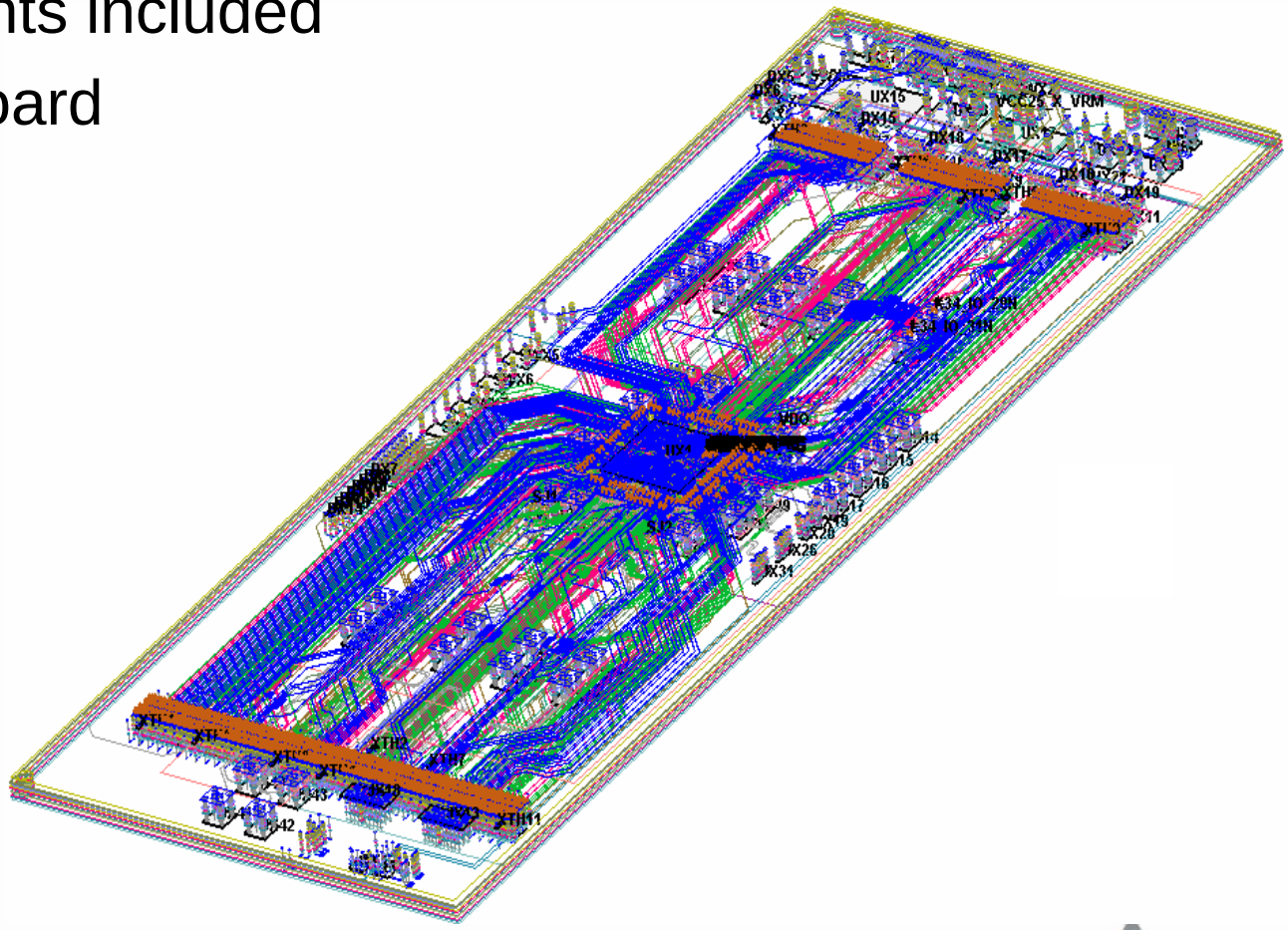
Automated Grouped Nodes

- Automated Pin Grouping: pins shorted for easy analysis
- Parts, Pin and Net names preserved
- User can define region for grouping



Xilinx ML481 Test Board

- Virtex-4 FPGA test board
- Board components included
- 24 layer, FR4 Board
- 7.5 in x 20 in



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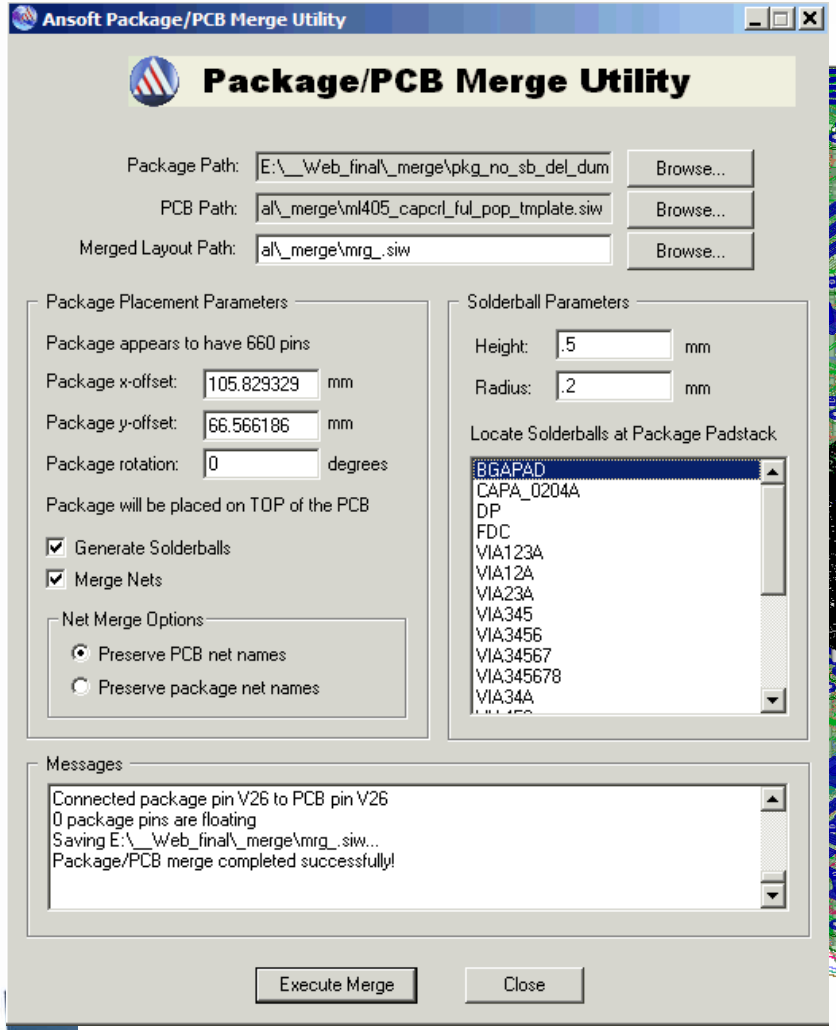
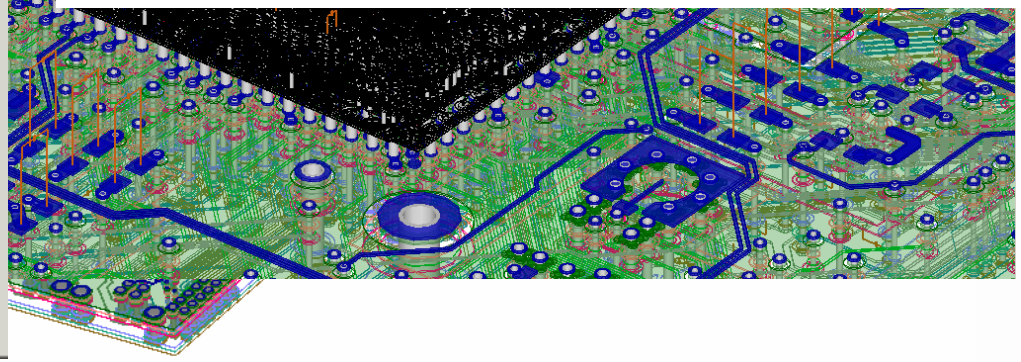
SIwave: Merge Package and PCB

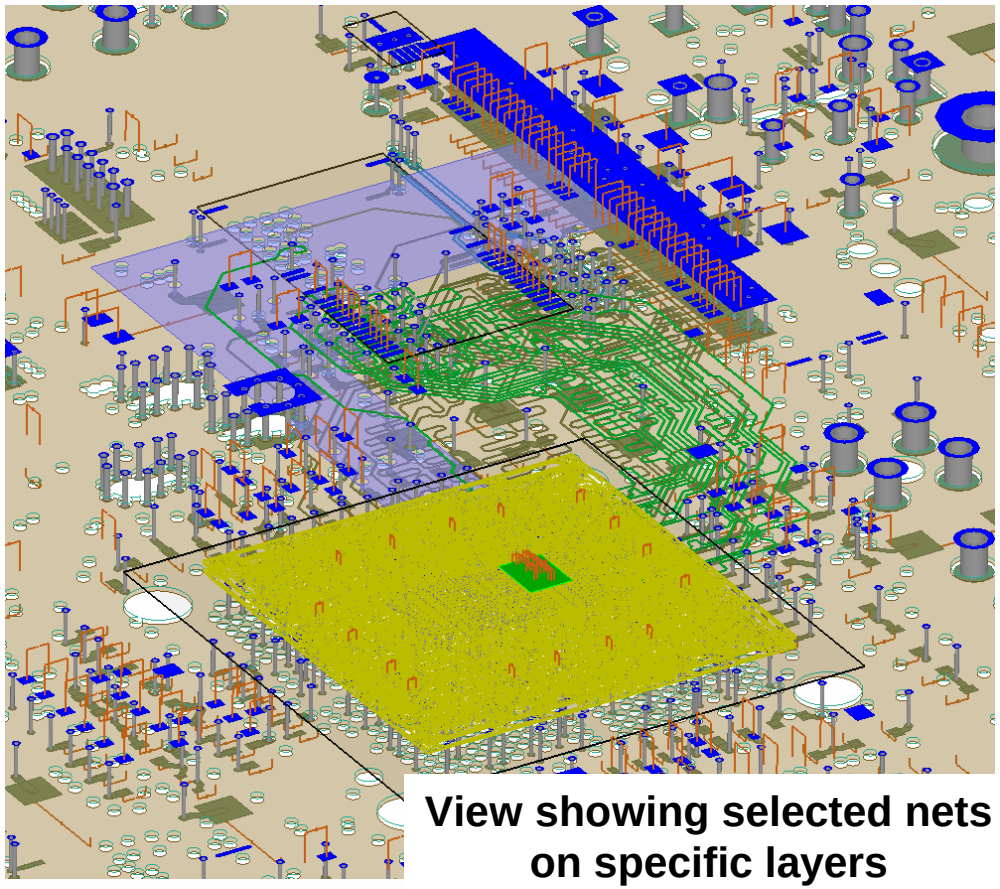


- Cadence APD Package
- Mentor PADS PCB
- Merge .siw files to preserve:
  - All R, L, C Components
  - All IO, IC Discrete Device Footprint and Pin Information

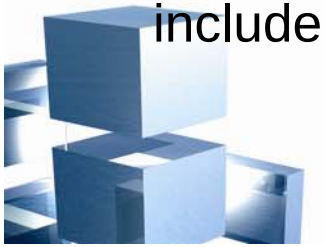


Virtex-4 Package on ML580 Board

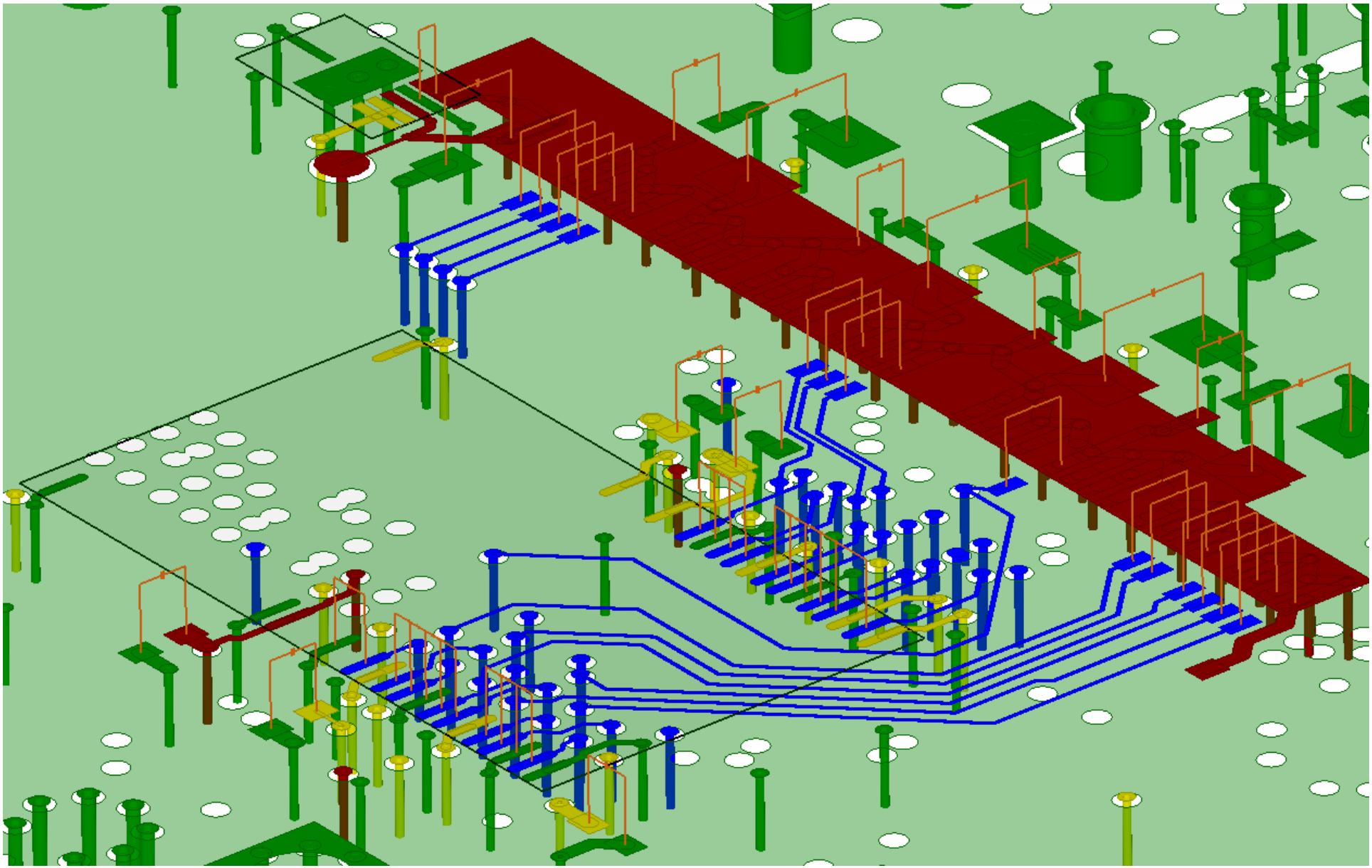
- 32 SDRAM I/O
  - 32 I/O ports at pkg bumps
  - 32 I/O ports at SDRAM
    - 16 at top part, 16 at bottom part
- VRM ports
  - 1 for 2.5V supply
  - 1 for VTT supply
- Die power port
  - 1 at 2.5V bumps
- Total: 67 port extraction
- Discrete decoupling capacitors included (package and PCB)
- I/O pull-up resistors to VTT included



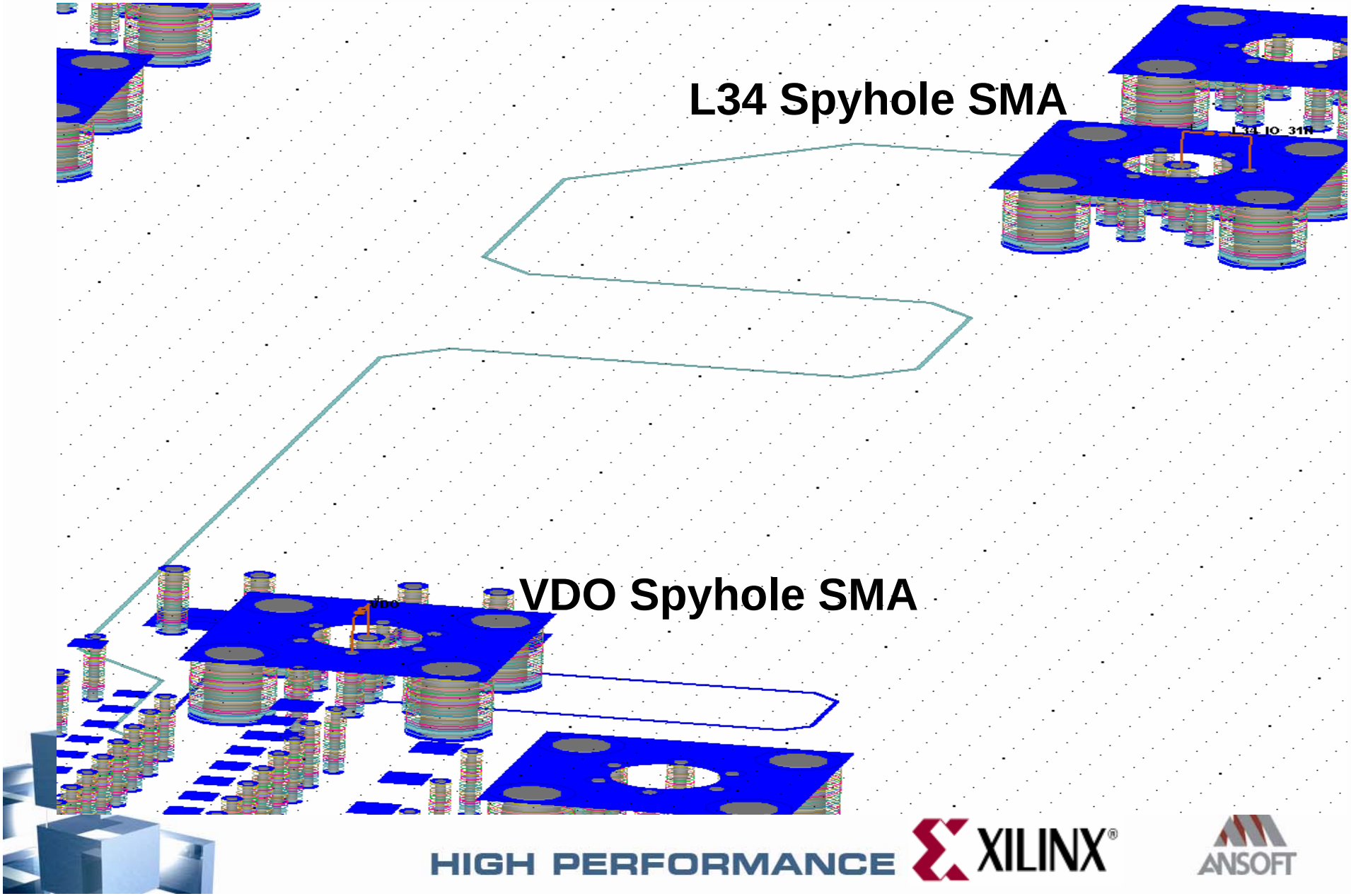
View showing selected nets on specific layers



Virtex-4 Package on ML580 Board



Board “Spyhole” IO’s



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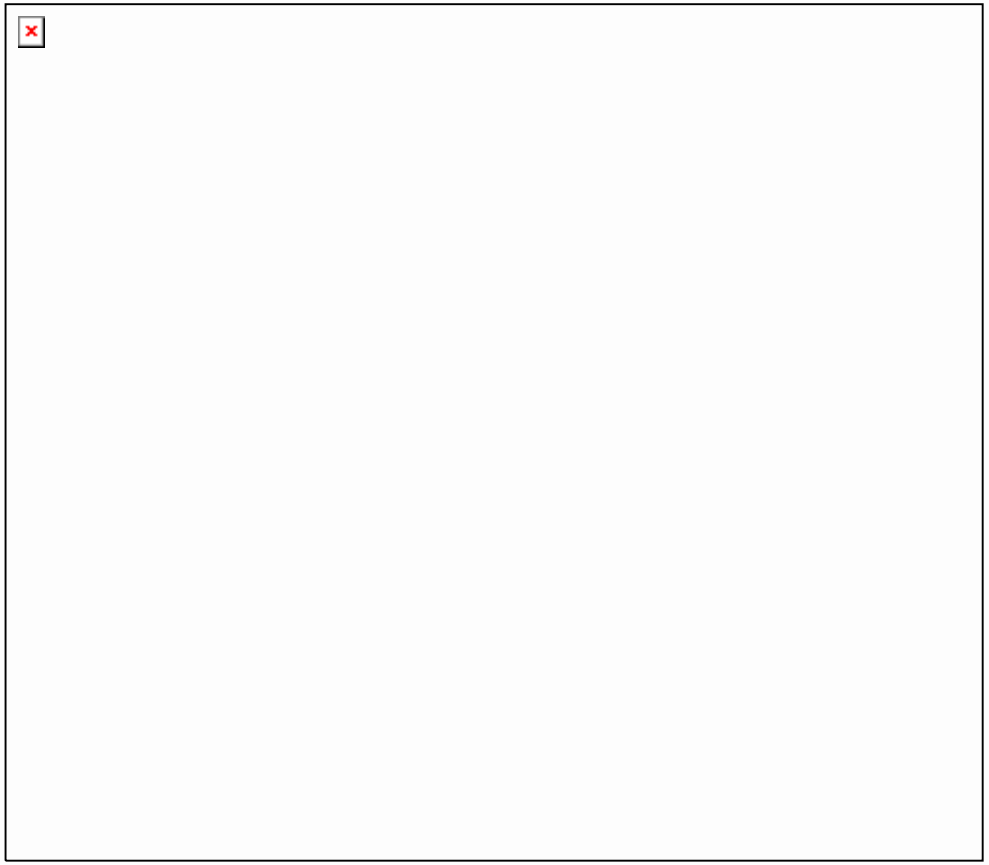
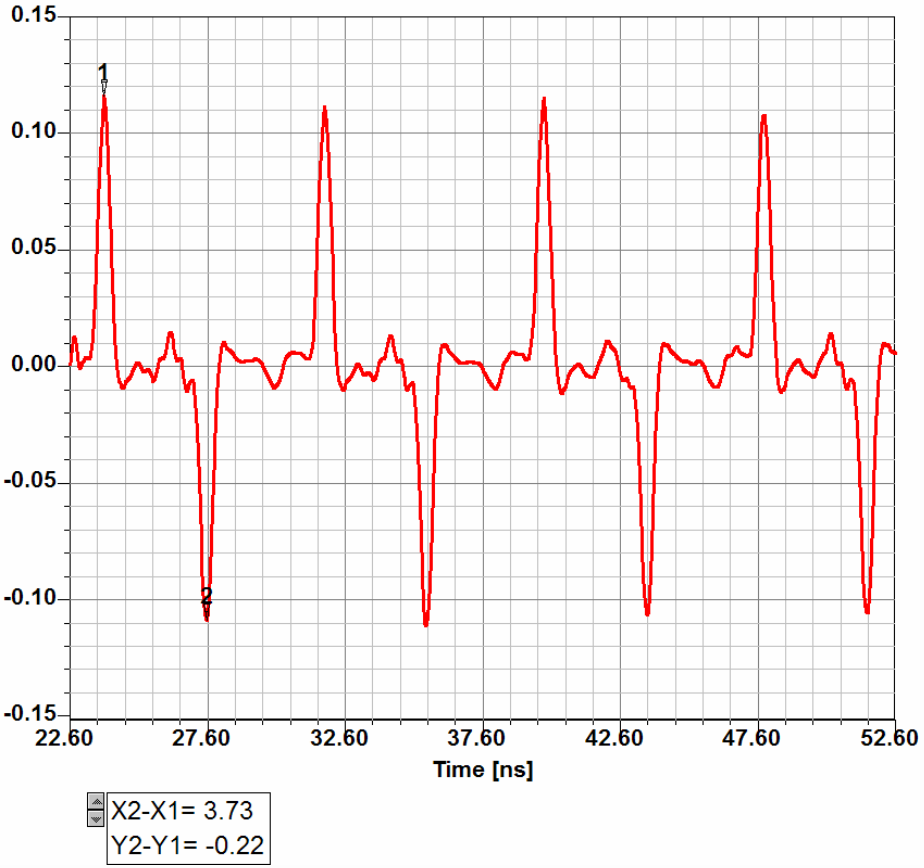
SSO Measured versus Simulated

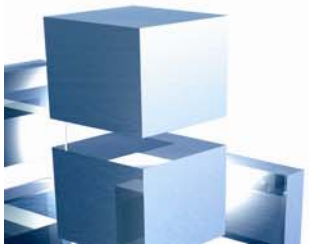
Measured

SIwave + Nexxim





- 125 MHz Clock, 400 ps edge
- SSO Measured at L34 Spyhole



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