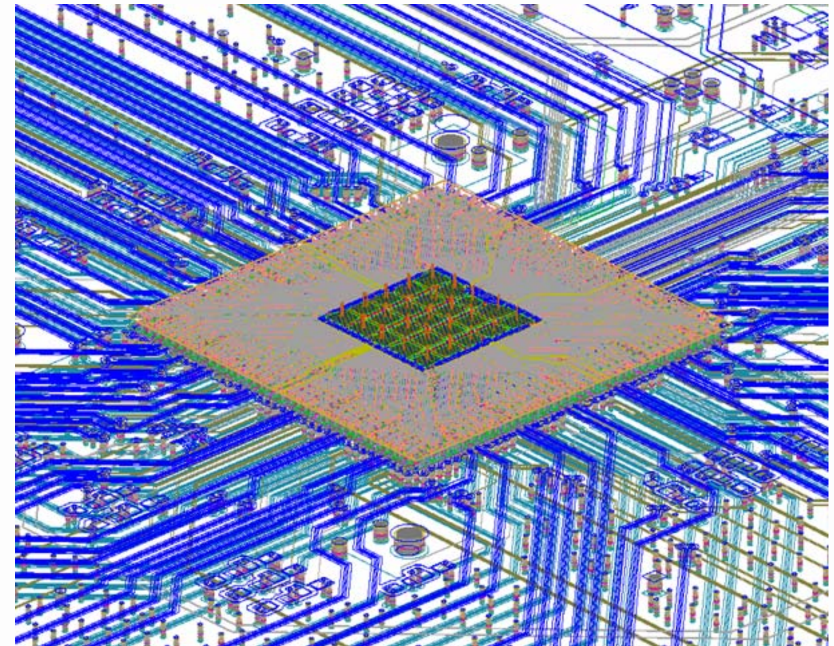
Solving the challenges posed by Chip/Package/Board Co-Design

Identify and locate sources of unwanted coupling

Simulation ***link to EM***:

Critical Interconnect, Vias, Discontinuities, Embedded Passives, etc



Solving the challenges posed by Chip/Package/Board Co-Design

1. Electromagnetic effects must be captured as passive and causal Spice circuit models
2. Adding IC, Package, and PCB physical layout effects create increasingly larger and more complex circuits

Model Order Reduction (MOR)

- A linear system can be described by a transfer function
  - Time Domain $$y(t) = \int_0^{\infty} x(\tau) h(t-\tau) dt$$

    or

  - Frequency Domain $$Y(s) = X(s) H(s)$$

  which are related to each other through the Laplace Transform

$$Y(s) = \int_0^{\infty} y(t) e^{-st} dt$$

Transfer Function

- The transfer function *H(s)* can be represented by a rational function

$$H(s) = \frac{b_{q-1}(s - z_{q-1})(s - z_{q-2})\dots(s - z_1)}{a_q(s - p_q)(s - p_{q-1})\dots(s - p_1)}$$

where (z_i, p_i) are the zeros and the poles of the system

J. E. Bracken, D. K. Sun and Z. J. Cendes, “S-domain methods for simultaneous time and frequency characterization of electromagnetic devices”, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 9, pp. 1277-1290, September 1998

S-Parameters from FWS

Field solver
S-parameters

(Usually passive)

Full-wave Spice
(Rational Function
Fitting)

$$S_{11}(j\omega) \approx \sum_{n} \frac{k_n}{j\omega - p_n}$$

Spice Subcircuit

Spice model
S-parameters

(May not be passive!)

Passivity

- A circuit is called passive if it cannot generate energy
- Conditions for a passive 1-port:
  - $\mathrm{Re}(Z_{11}) \geq 0$, or
  - $|S_{11}| \leq 1$
  - (for all frequencies from DC to infinity)
- It's a bit more complex for an N-port:

$$\max(\mathrm{SVD}(\mathbf{S}(f))) \leq 1 \quad \text{for} \quad 0 \leq f \leq \infty$$

SVD = singular value decomposition

Passivity Enforcement

- Given: a rational function model that may not be passive

$$S_{11}(j\omega) \approx \sum_n \frac{k_n}{j\omega - p_n}$$

Optimize these (→ k_n)

- Keep the poles fixed and optimize the residues so the passivity constraint is met

Causality

FR4, 10 cm line, far end

* test causality of new mom2d rl model

Voltages (lin): 0, 100m, 200m, 300m, 400m, 500m, 600m, 700m, 800m, 900m, 1000m, 1.1

Time (lin) (TIME): 0, 500p, 1n, 1.5n, 2n, 2.5n

Constant tan δ

Djordjevic model

New model

HIGH PERFORMANCE EDA

ANSOFT

Zoomed-In View

* test causality of new mom2d rl model

Constant tan δ

Djordjevic model

New model

100m

0

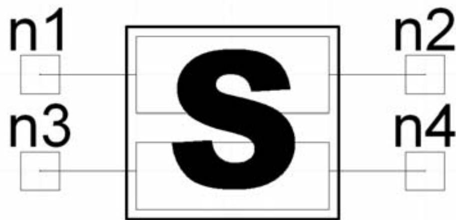
Voltages (lin)

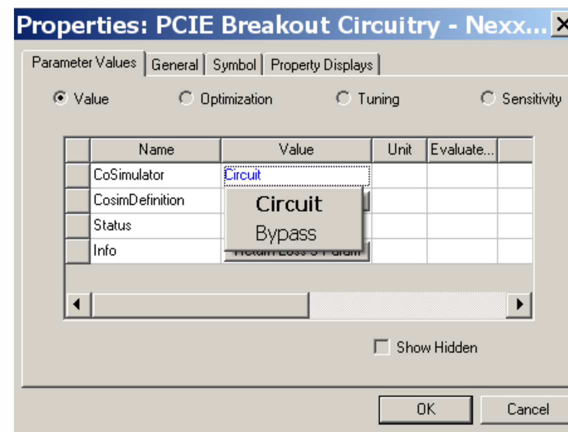
0 50p 100p 150p 200p 250p 300p 350p 400p 450p 500p 550p 600p

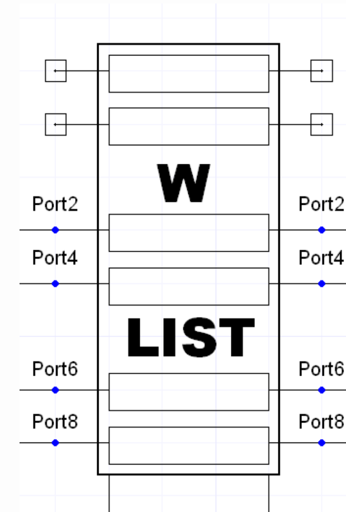
Time (lin) (TIME)

S-Parameters and W-Elements

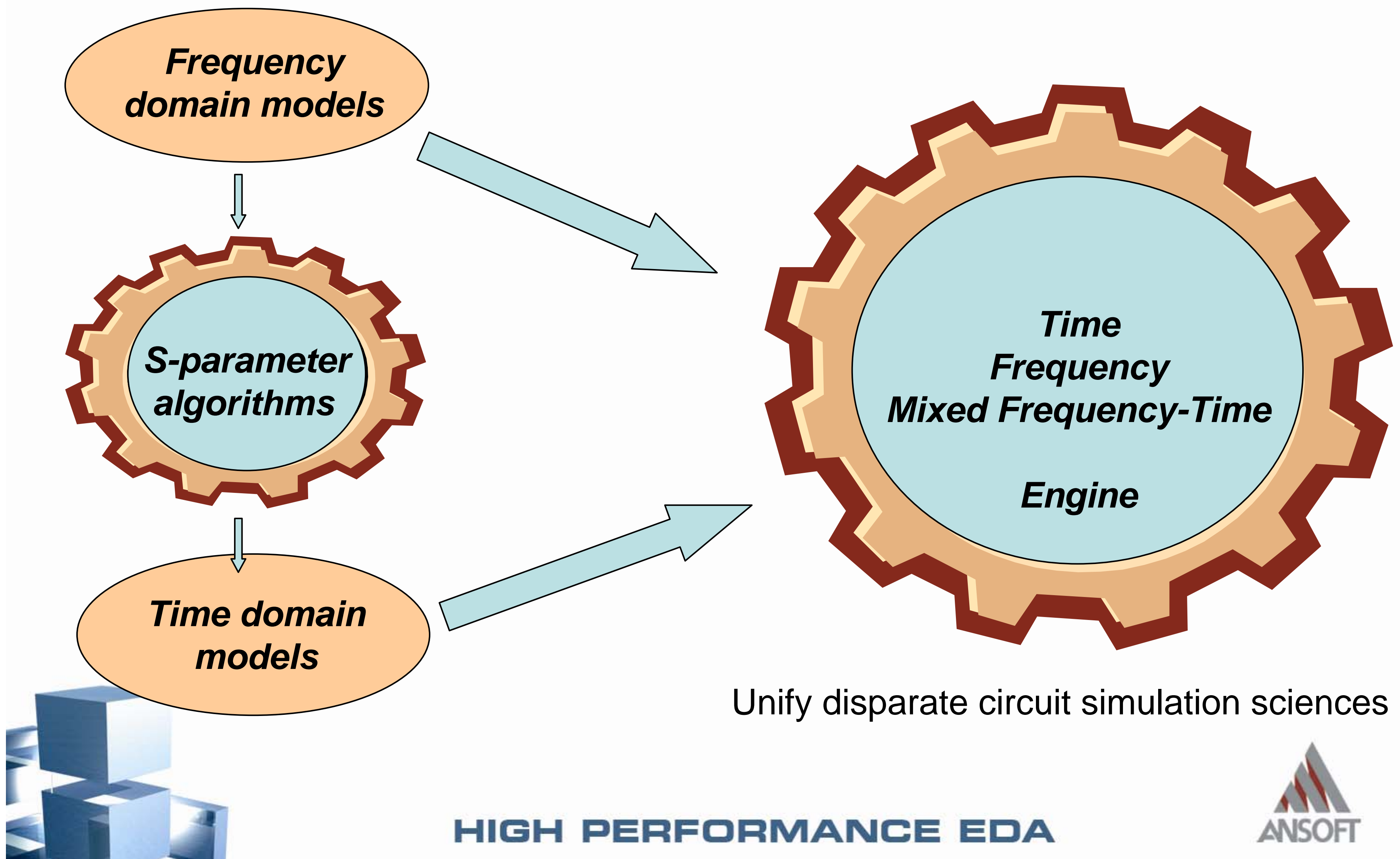
- Import any s-parameter file
- Superior s-parameter handling
  - State-space models
  - Verification & enforcement of Causality & Passivity (user choice)
- Parameterizable through NMF



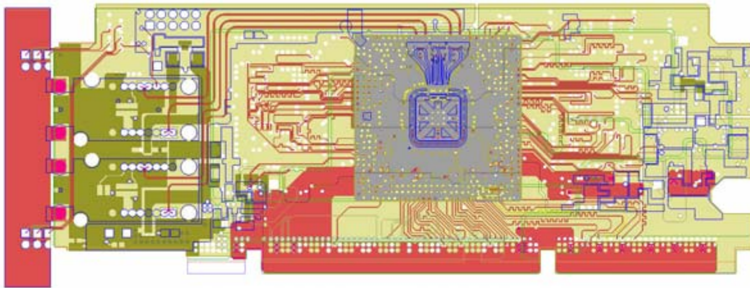


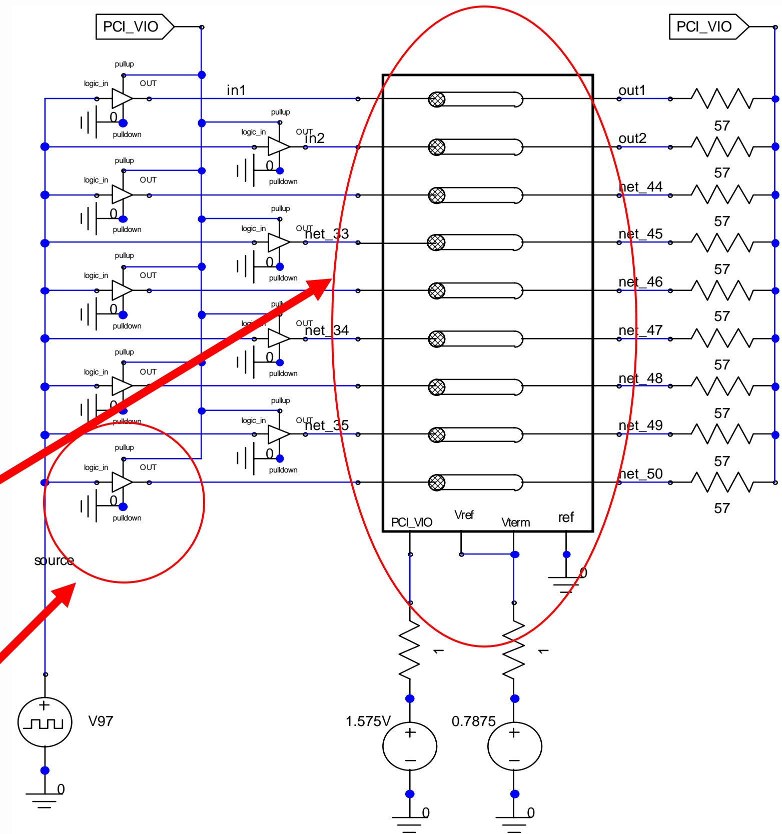


What does this mean for circuit simulation?



Example: Power Integrity

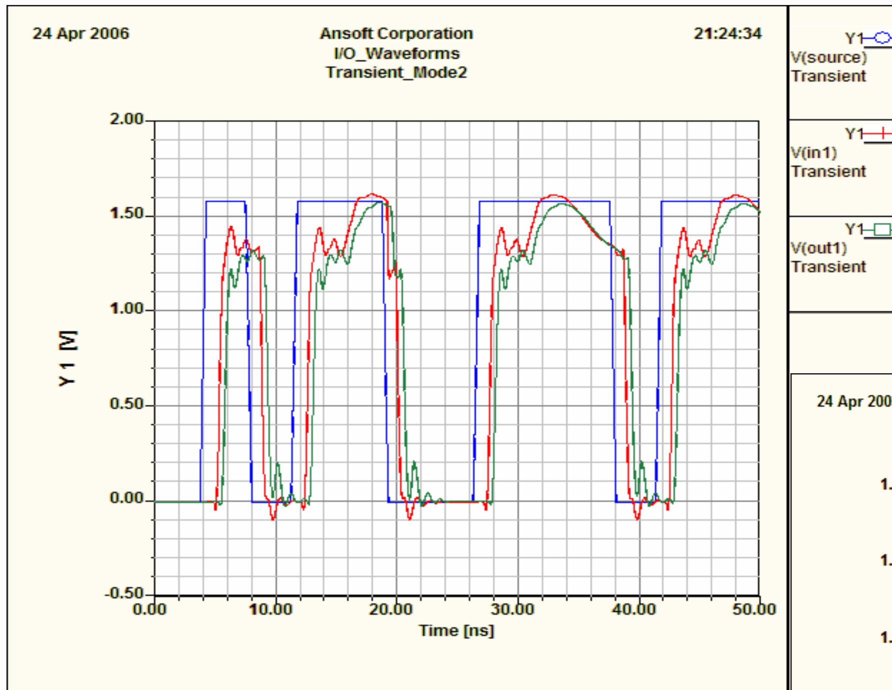




57 Port S-parameter block
DC to 5GHz

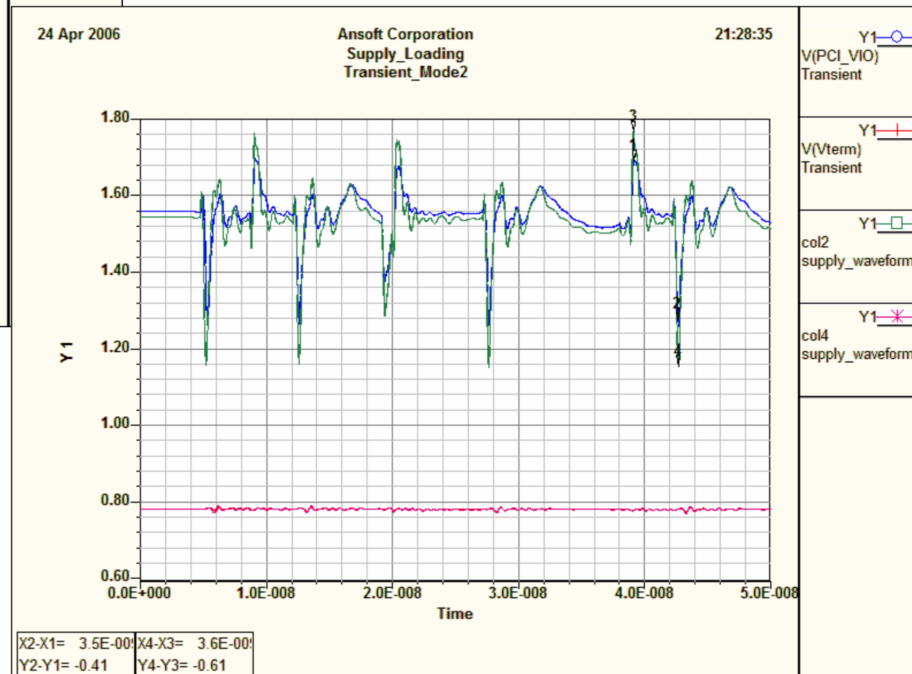
IBIS Drivers

Transient Analysis using Nexxim



18 IBIS Drivers
57 Port S-parameter model

Transient simulation time: 366s



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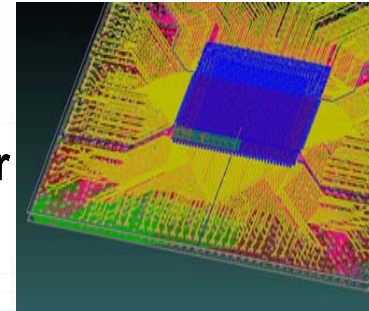
Chip and Package Design

Circuit simulation in DesignerSI



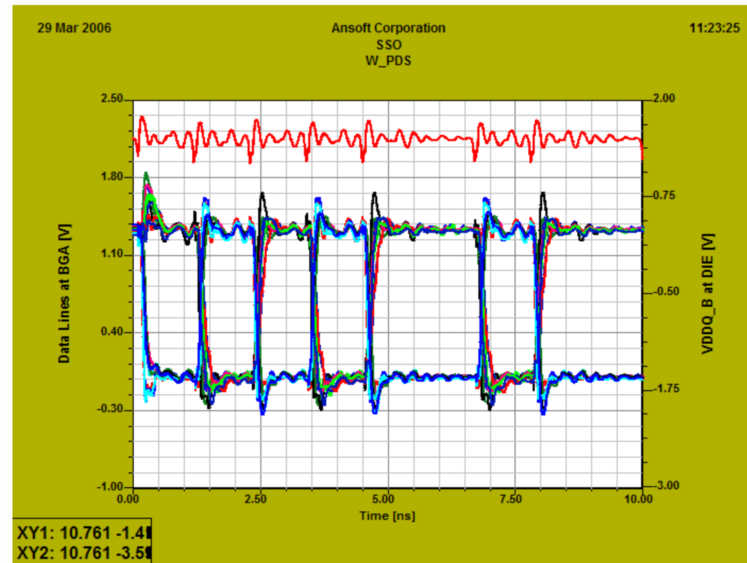
44-port S-parameter
From SIwave

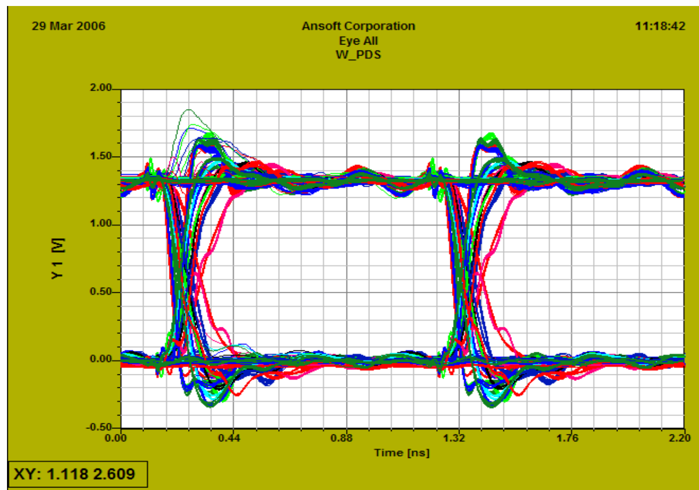
Silicon Driver Models
More accurate than IBIS
Also more complex

Chip and Package Design

64-bit Nexxim

44 port S-parameter model
148,000 MOSFETs
1.7 Million Capacitors
500,000 Resistors





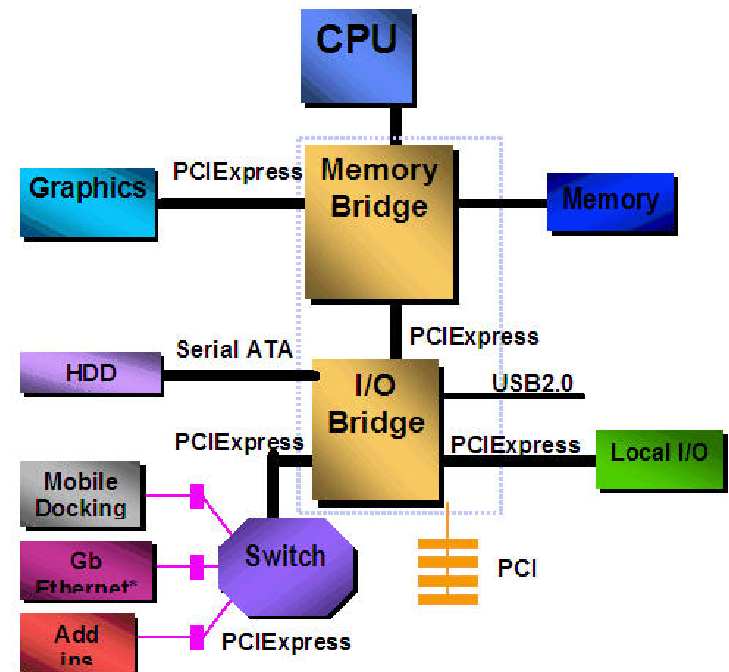
Other simulators cannot solve this problem!

Nexxim solution time: 36 hrs

PCI Express

- Originally developed by PCISIG
  - Intel® was a major contributor
  - 1st specification released at Q2, 2002
  - Movement towards communication industry technology
- Why serial and not parallel bus ?
  - Parallel I/O interconnects limited
  - Serial bus architecture
    - *More bandwidth per pin*
    - *Scales easier to higher bandwidth*
  - Enables network point to point links
    - *Instead of multi-drops*

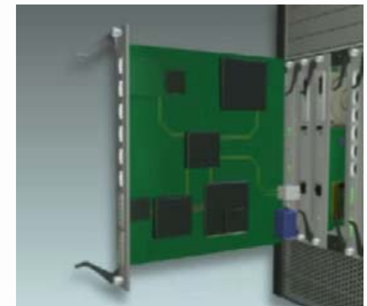
Flexible, scalable, high-speed serial point to point hot pluggable & swappable interconnect

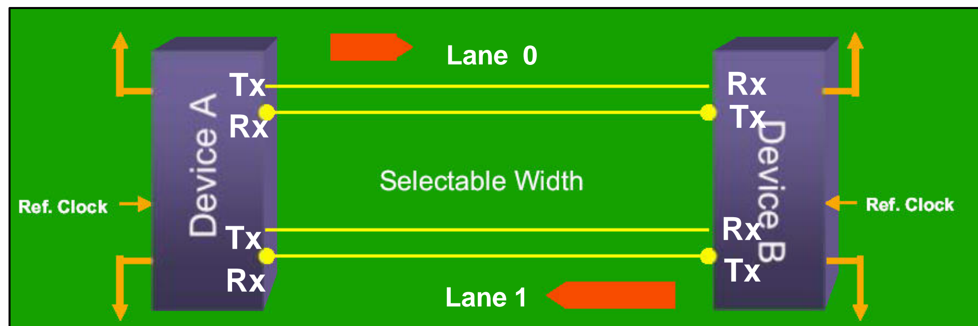


Courtesy of Intel Corporation

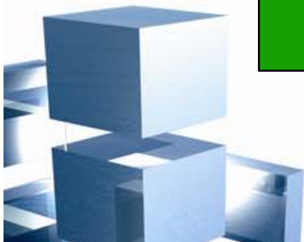
PCI Express Electrical Specifications

- Each PCI Express lane has two CML Tx/Rx pairs
  - 2.5 Gb/s per lane
  - Current Mode Logic
- Each data lane uses 8B/10B encoding
- 8 bit byte is translated to 10 bit character
  - Equalizes numbers of 1's and 0's
- Selectable multiple line widths
  - 1, 2, 4, 8, 16 or 32 lanes
  - Accommodates higher bandwidths

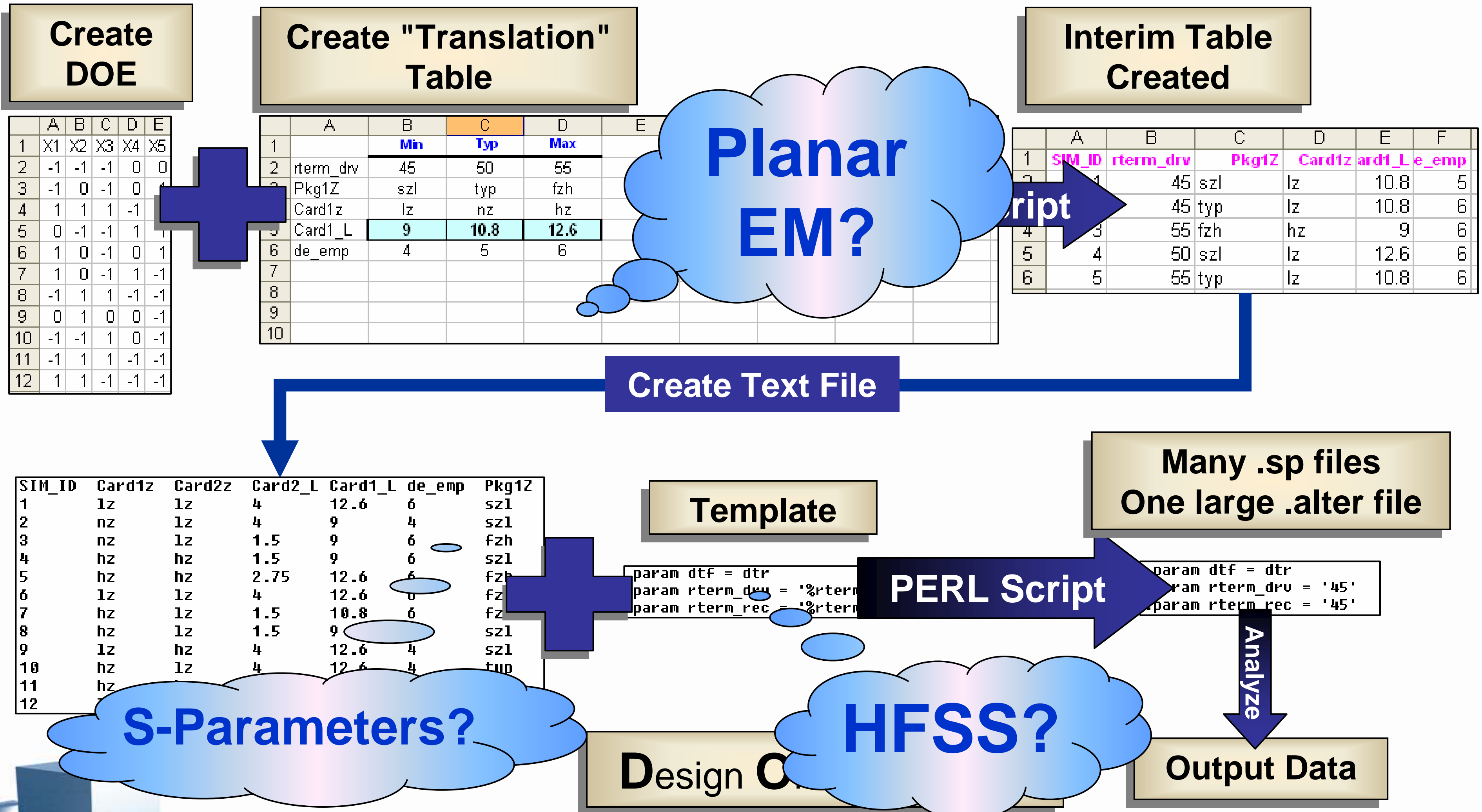




Specification is focused on "card" type connections, as opposed to cable connections

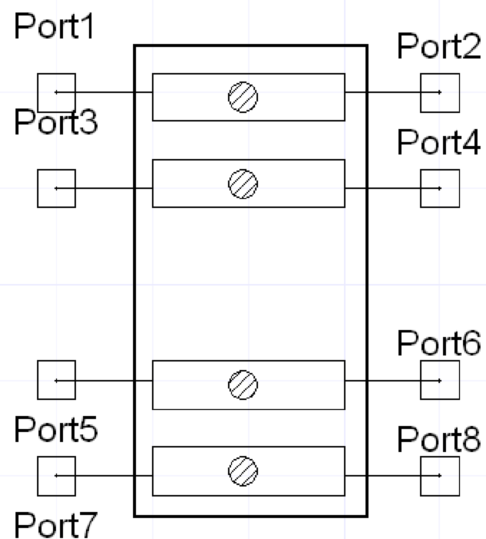


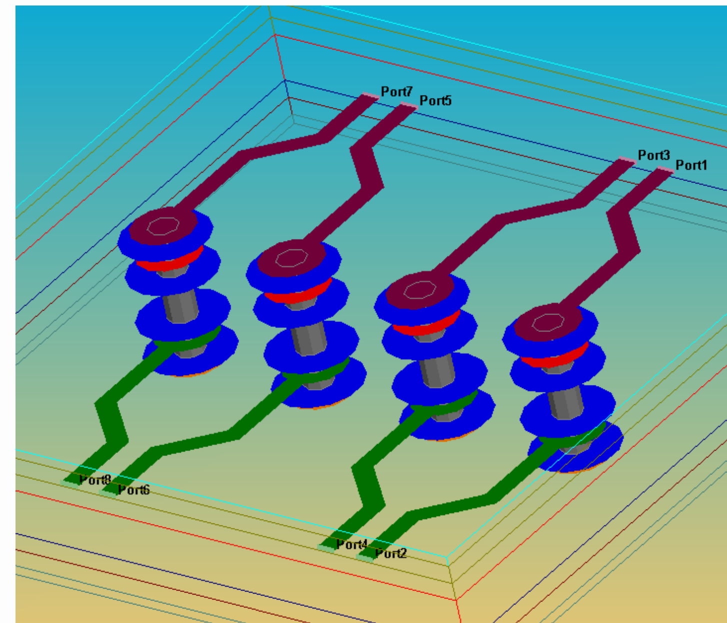
Existing Intel "DOE" Design Flow



Integrated Planar EM

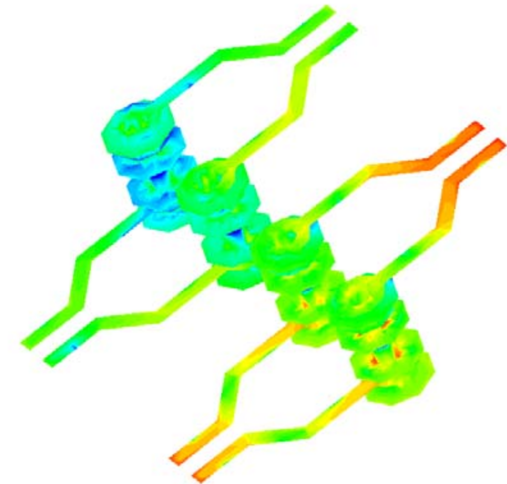
- Fully integrated
  - Any geometry
- Variable stackups, dielectric constants



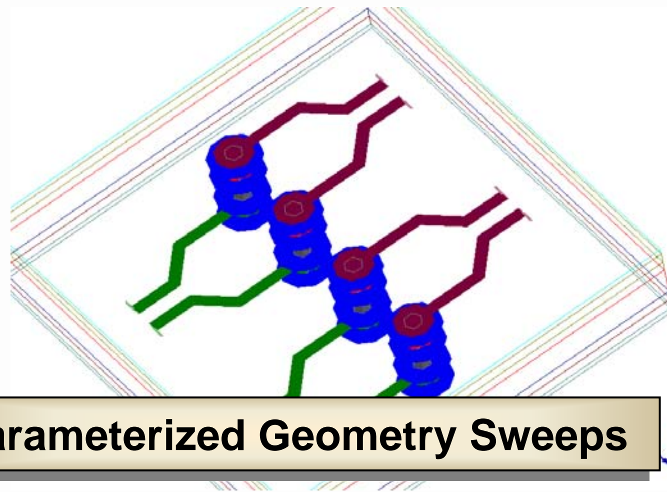


Planar EM Simulations

- Simulate within circuit or separate
  - Same project
- Fields & currents
  - Observe crosstalk & ground current
- Fully integrated
  - No re-solving on changing parameters
  - Auto-interpolation



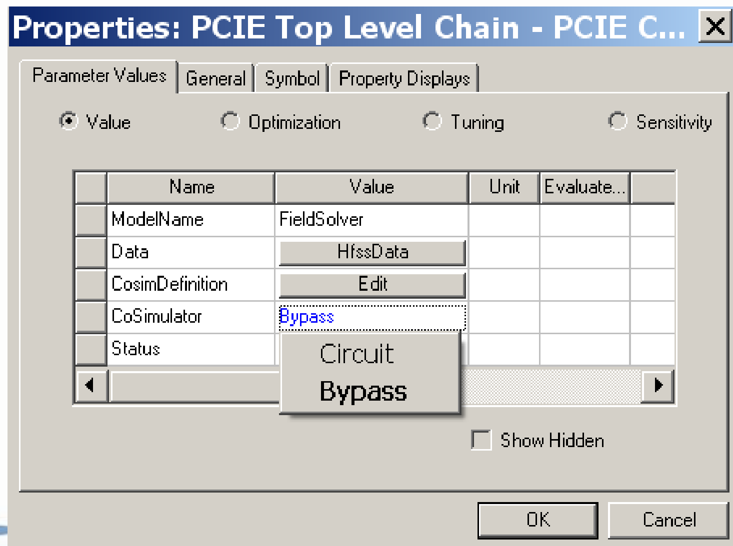
View Surface Currents



Parameterized Geometry Sweeps

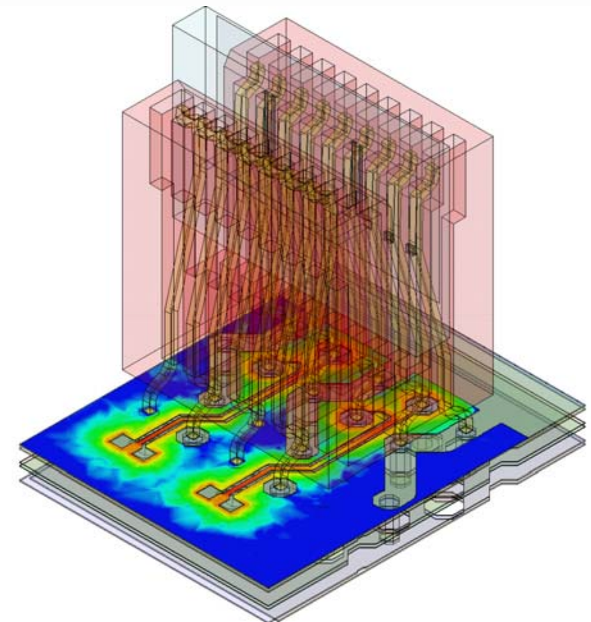
Integrated HFSS Simulations

- Fully integrated
- Any geometry
- Fully parameterizable

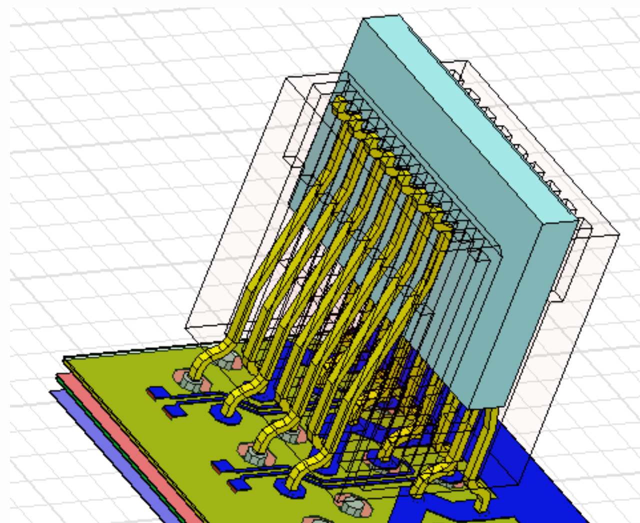


HFSS Full 3D Simulations

- Cosimulation separate or within circuit
  - View fields or surface currents
- Dynamically linked
  - No re-solving on changing parameters
  - Auto-interpolation

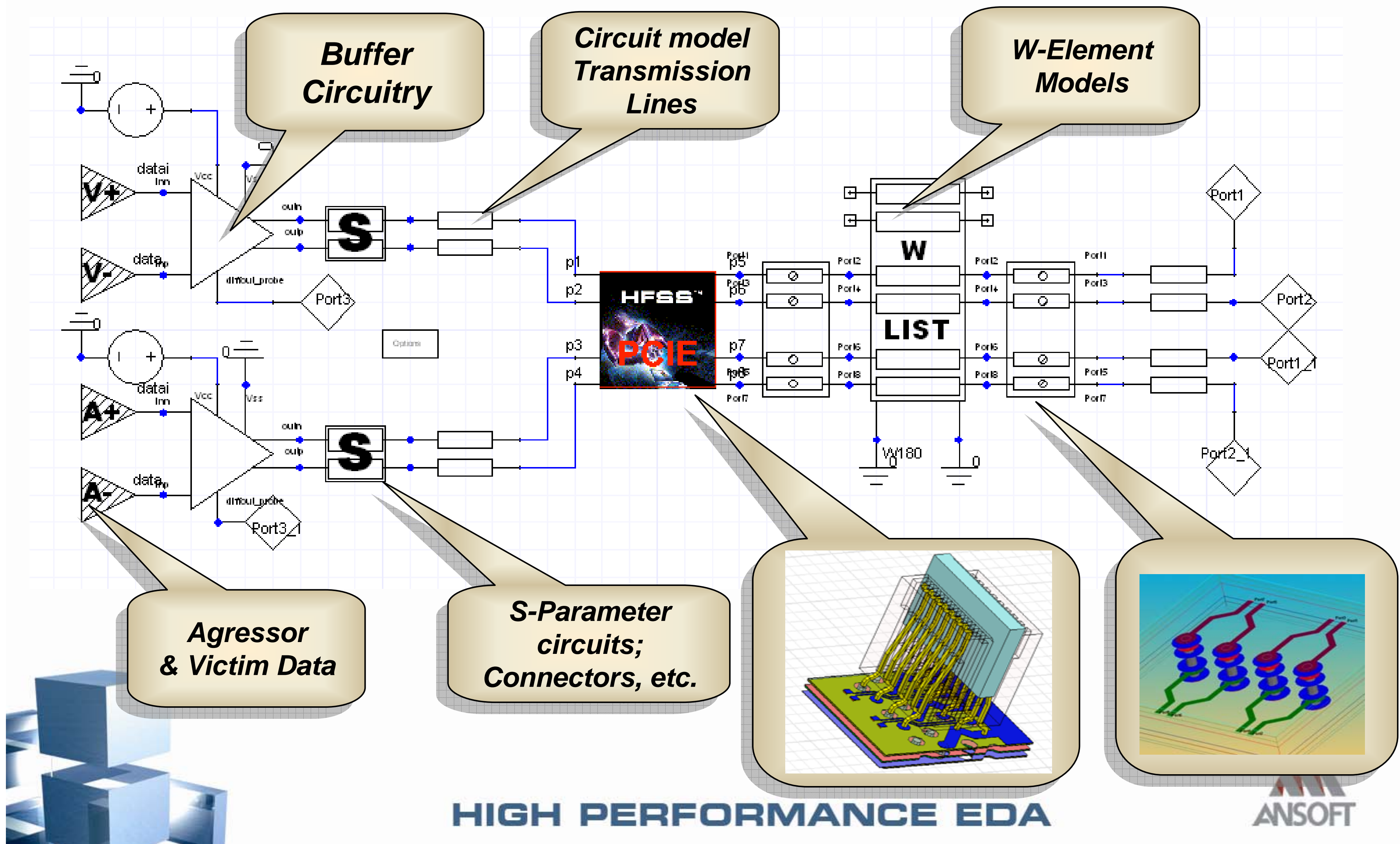


View Surface Currents, fields, EMI, etc.



Parameterized Geometry Sweeps

Block Diagram of Gigabit Serial Channel



Intel's New Design Flow

	A	B	C	D	E
1	X1	X2	X3	X4	X5
2	-1	-1	-1	0	0
3	-1	0	-1	0	1
4	1	1	1	-1	1
5	0	-1	-1	1	1
6	1	0	-1	0	1
7	1	0	-1	1	-1
8	-1	1	1	-1	-1
9	0	1	0	0	-1
10	-1	-1	1	0	-1
11	-1	1	1	-1	-1
12	1	1	-1	-1	-1

DOE and "Translation" file files can be text format

	A	B	C	D	E	F	G	H	I
1		Min	Typ	Max		Min	Typ	Max	
2	rterm_drv	45	50	55					
3	Pkg1Z	szl	typ	fzh		80	91	101	
4	Card1z	lz	nz	hz		80	91	100	
5	Card1_L	9	10.8	12.6					
6	de_emp	4	5	6					
7									
8									
9									
10									

Output Data files Or Process Data in GUI

"Single Button Click" Solution

Designer:

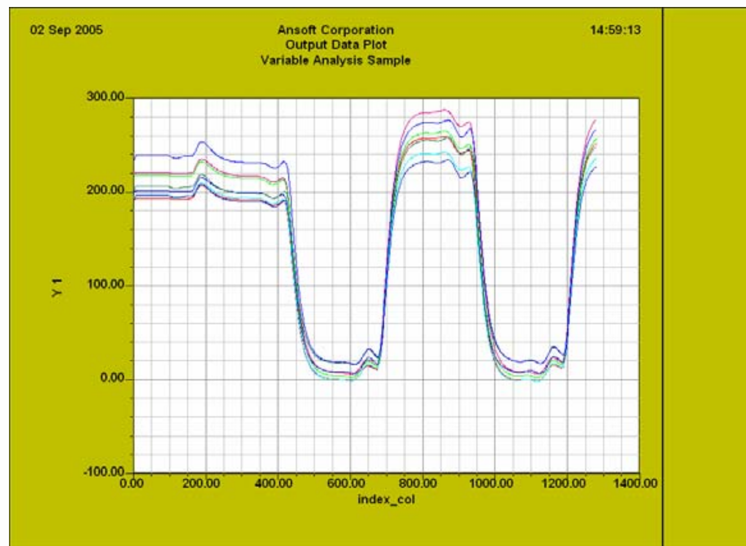
- **Reads DOE file**
- **Reads "Translation" files**
- **Processes Information**
- **Performs simulations**
- **Outputs/ Post processes data**

Important!

Parameterized HFSS circuits
parameterized Planar EM circuits
"Variable" S-Parameters
Can now be *included* in DOE analyses!

Design Flow DOE Example

- Choose project, Design, etc.
- Press "Start DOE"
- Designer *Automatically* Runs
- Saves each iteration in a Data file
  - Post process in Designer or aftermarket tool



Data

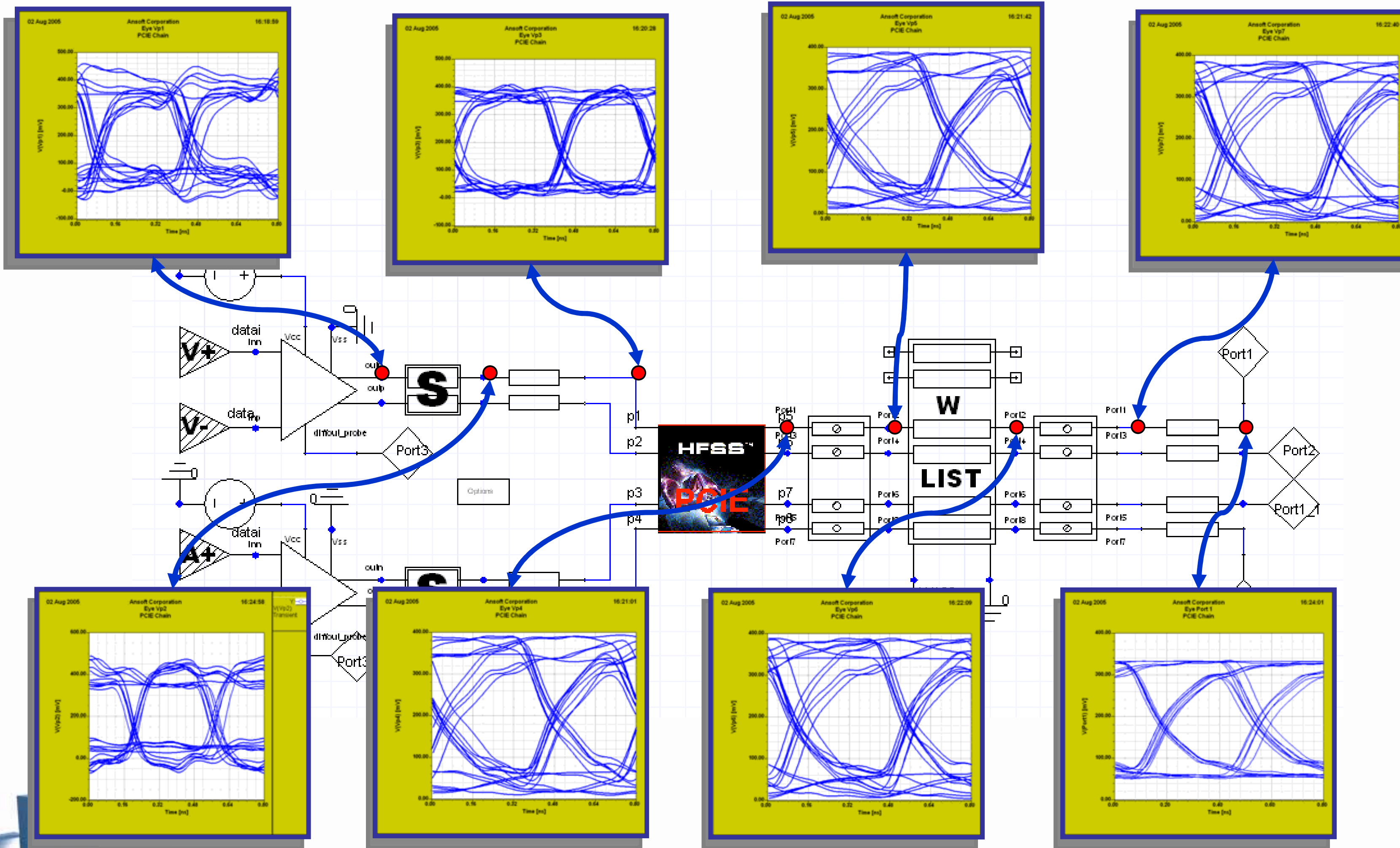
File Edit View Favorites Tools Help

Back Search Folders

Address C:\Designer\Rebuild Of General Project Go

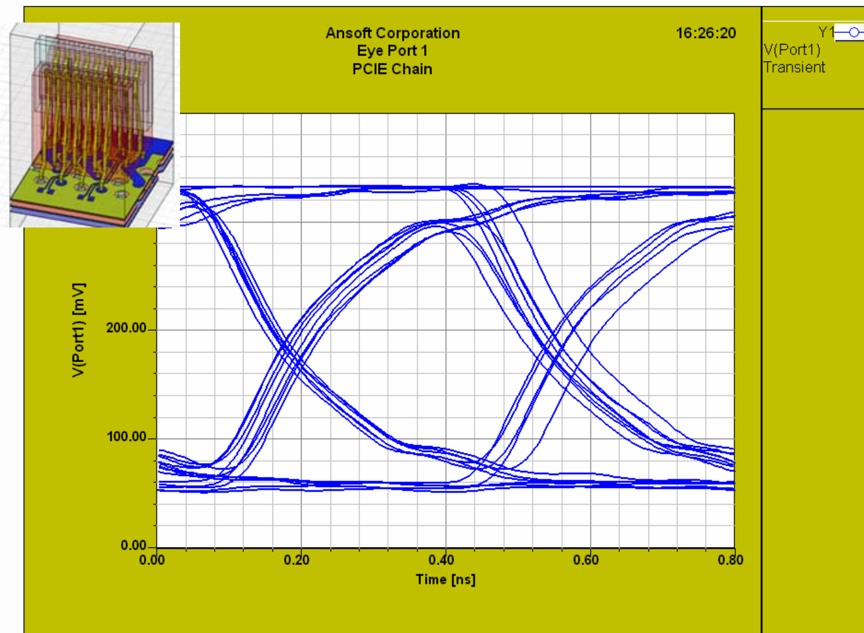
Name	Size	Type	Date Mo
OutputFile0.tab	49 KB	TAB File	8/15/20
OutputFile1.tab	49 KB	TAB File	8/15/20
OutputFile2.tab	49 KB	TAB File	8/15/20
OutputFile3.tab	49 KB	TAB File	8/15/20
OutputFile4.tab	49 KB	TAB File	8/15/20
OutputFile5.tab	52 KB	TAB File	8/15/20
OutputFile6.tab	49 KB	TAB File	8/15/20
OutputFile7.tab	49 KB	TAB File	8/15/20
OutputFile8.tab	49 KB	TAB File	8/15/20
OutputFile9.tab	49 KB	TAB File	8/15/20
OutputFile10.tab	49 KB	TAB File	8/15/20
OutputFile11.tab	52 KB	TAB File	8/15/20

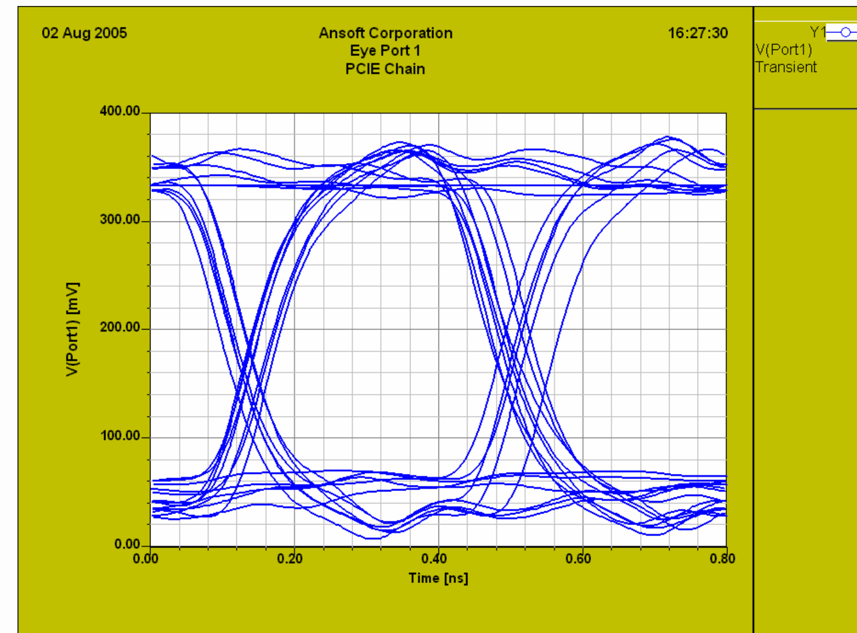
Allows Rapid "What if" Analyses



All components "Active"

Allows Rapid “What if” Analyses



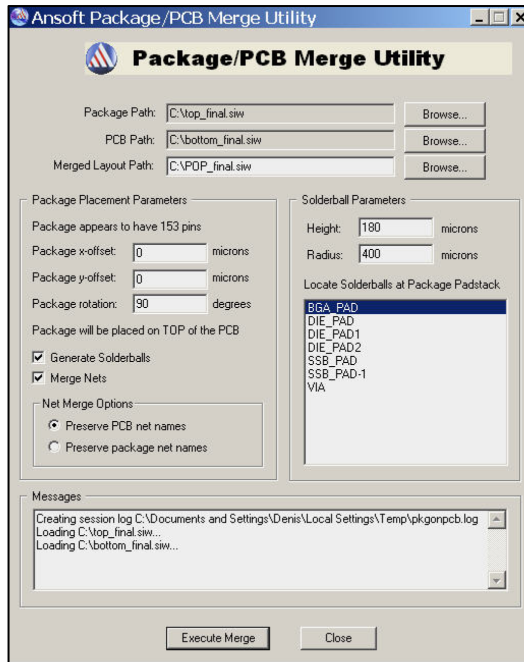


Connector In Circuit

Connector "Bypassed"

The connector has the largest effect on closing the eye

Package/Package Merge Utility

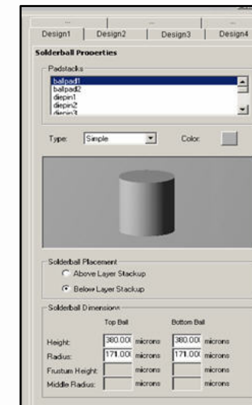


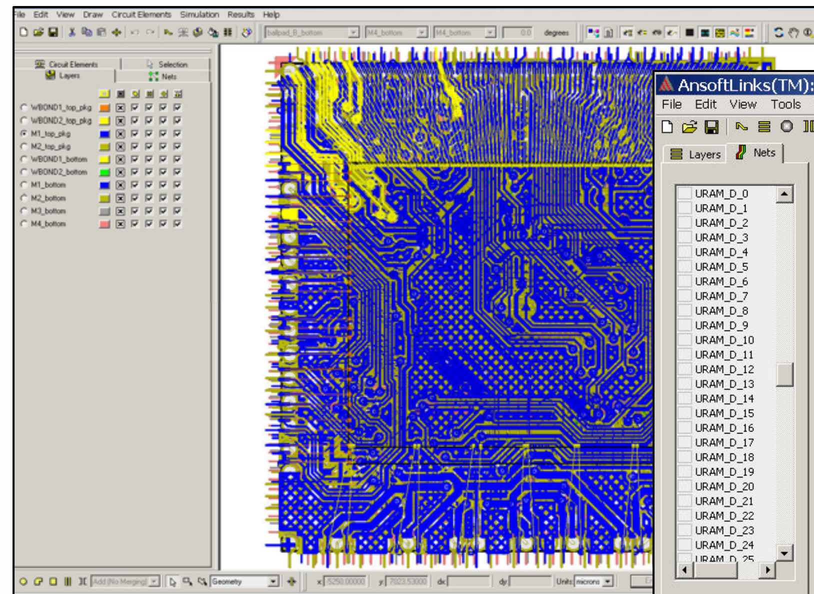
Layer Stack-up Editor

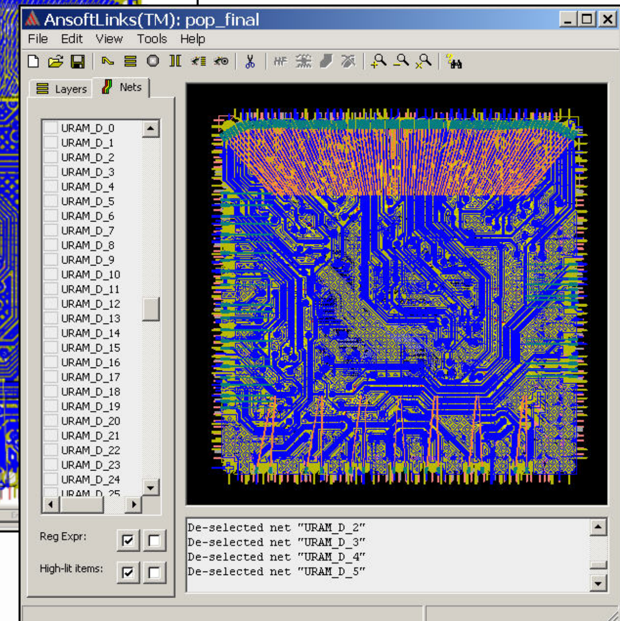
Name	Type	Film	Material	Thickness (mic...	Elevation (microns)
Top Dielectric_pkg	DIELECTRIC		air	350	796
WBOND1_top	WIREBOND		gold	0	796
WBOND2_top	WIREBOND		gold	0	796
M1_top	METAL	POSITIVE	copper	20	776
UNNAMED_5_pkg	DIELECTRIC		FR4_epoxy	100	676
M2_top	METAL	POSITIVE	copper	20	656
pkg_pcb_air	DIELECTRIC		FR4_epoxy	400	256
WBOND1_bottom	WIREBOND		gold	0	256
WBOND2_bottom	WIREBOND		gold	0	256
M1_bottom	METAL	POSITIVE	copper	20	236
dielectric3_B	DIELECTRIC		FR4_epoxy	40	196
M2_bottom	METAL	POSITIVE	copper	18	178
dielectric4_B	DIELECTRIC		FR4_epoxy	100	78
M3_bottom	METAL	POSITIVE	copper	18	60
dielectric5_B	DIELECTRIC		FR4_epoxy	40	20
M4_bottom	METAL	POSITIVE	copper	20	0

Add New Metal Layer

Above Selected Layer | Below Selected Layer | Edit Layer Properties... | Delete Selected Layers | OK | Cancel







Package on Package/View

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