Modeling and Analysis Challenges for Complex Digital Systems-in-Package Designs

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Note

- The content of this presentation is the collected effort of the entire SiP team in SPB division at Cadence.

Topics

- SiP Overview
  - What is SiP?
  - Why is SiP Important?
  - SiP applications
- SiP Design Challenges
- Requirements of EDA tools for SiP design and analysis
  - Co-Design methodologies
  - Design management
  - SI and PI analysis
- Summary

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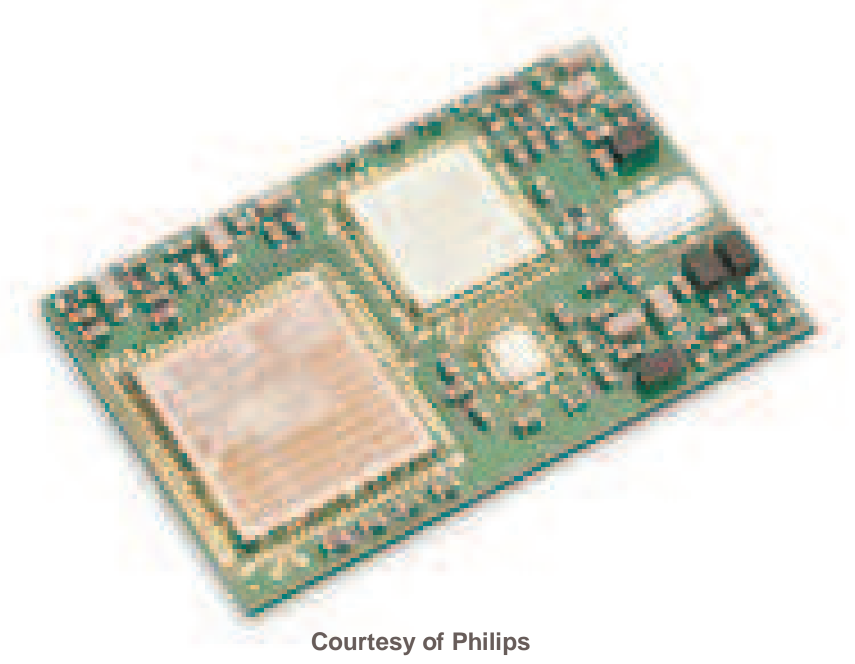
What is SiP?

- SiP (System-in-Package)
  - Single package that combines all of the electronic components (digital ICs, analog ICs, RF ICs, passive components or other elements) needed to provide a system or sub-system.
- Applications
  - Cellular
  - Bluetooth
  - 802.11 WLAN
  - CMOS Sensors



Courtesy of Philips

Why is SiP important?

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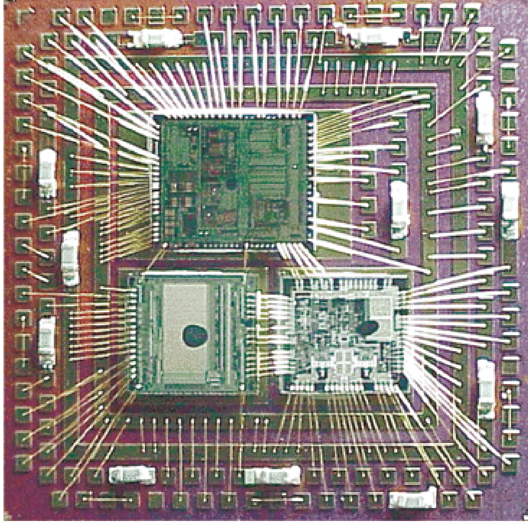
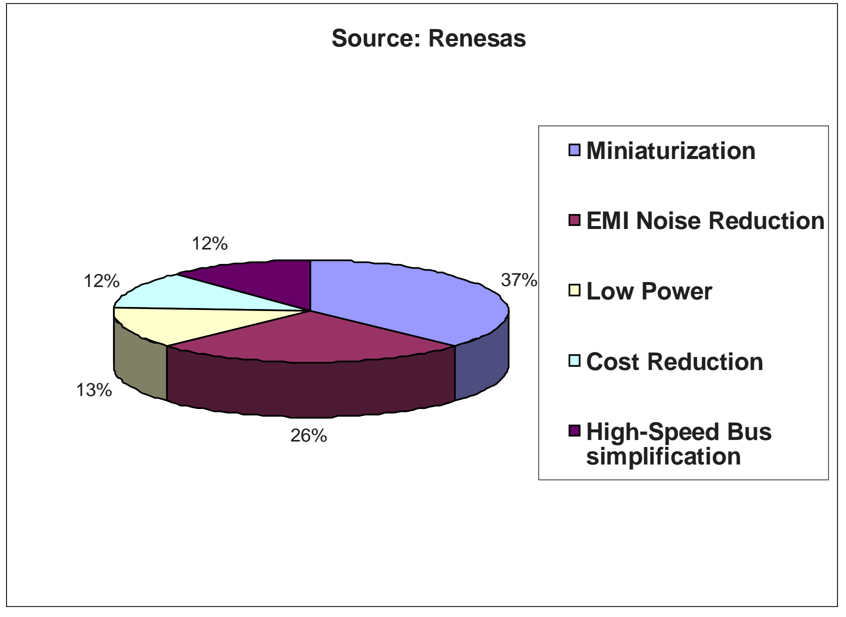
- Increased functional density
  - Miniaturization due to fewer packages and 3D stacked die
  - Multiple technologies in a SiP
- Reduced time-to-new product concepts
  - Faster design cycles (over SoC)
  - Reduce system board complexity and layer count
- Performance through interconnect elimination
  - Low power
  - High speed
- **Optimization of complexity, cost, and time to market**



Courtesy of ASAT



SiP applications in wireless devices

SiP Functions

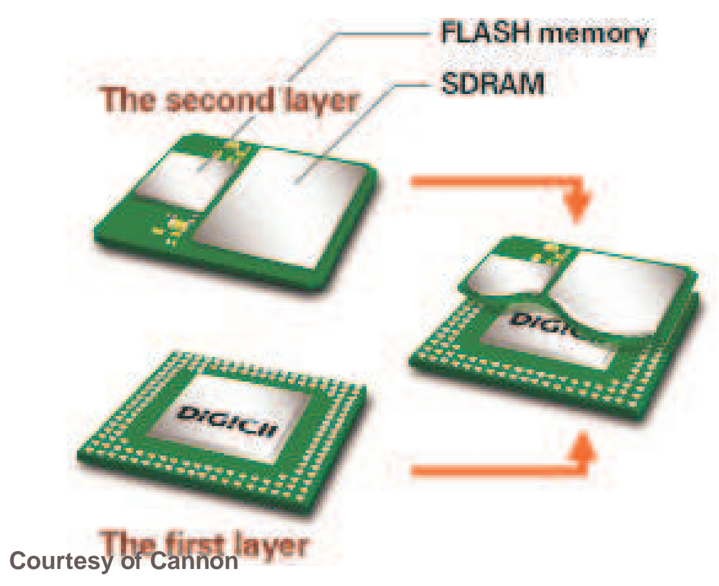
RF/IF
(WLAN, Bluetooth, GPS)

Camera
(A-FEP,DSP,VDr)

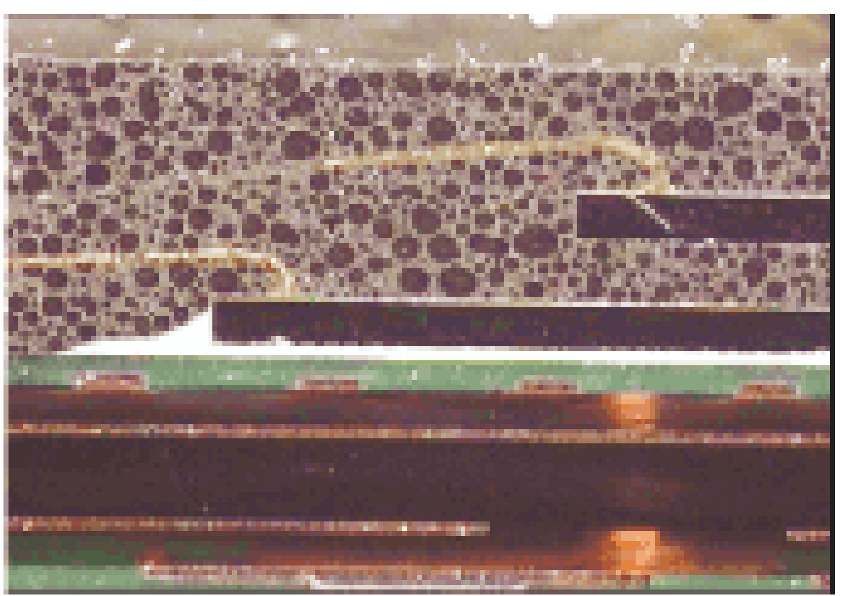
Baseband
(DSP,memory)

Application
(GPU,CPU,memory)

Multi-Die package forecast



Courtesy of Cannon



Courtesy of ASAT

SiP and Stacked-package designs increase 21% yearly

Designs move from experts to majority of designers

(Source: Electronic Trend Publications)

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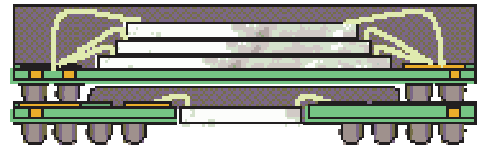
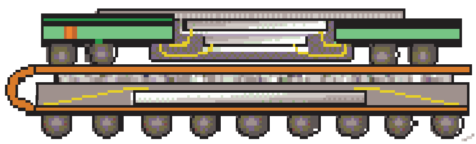
Multiple die connections

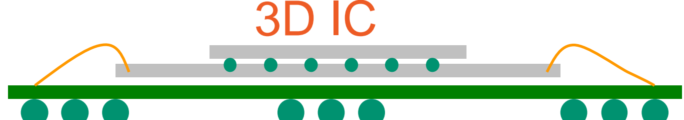
Die stacking



Package-on-package



3D IC



RF module

Flip Chip
RFIC
L, R, C
SRAM
FLASH
Embedded Passives

Complex die stack design

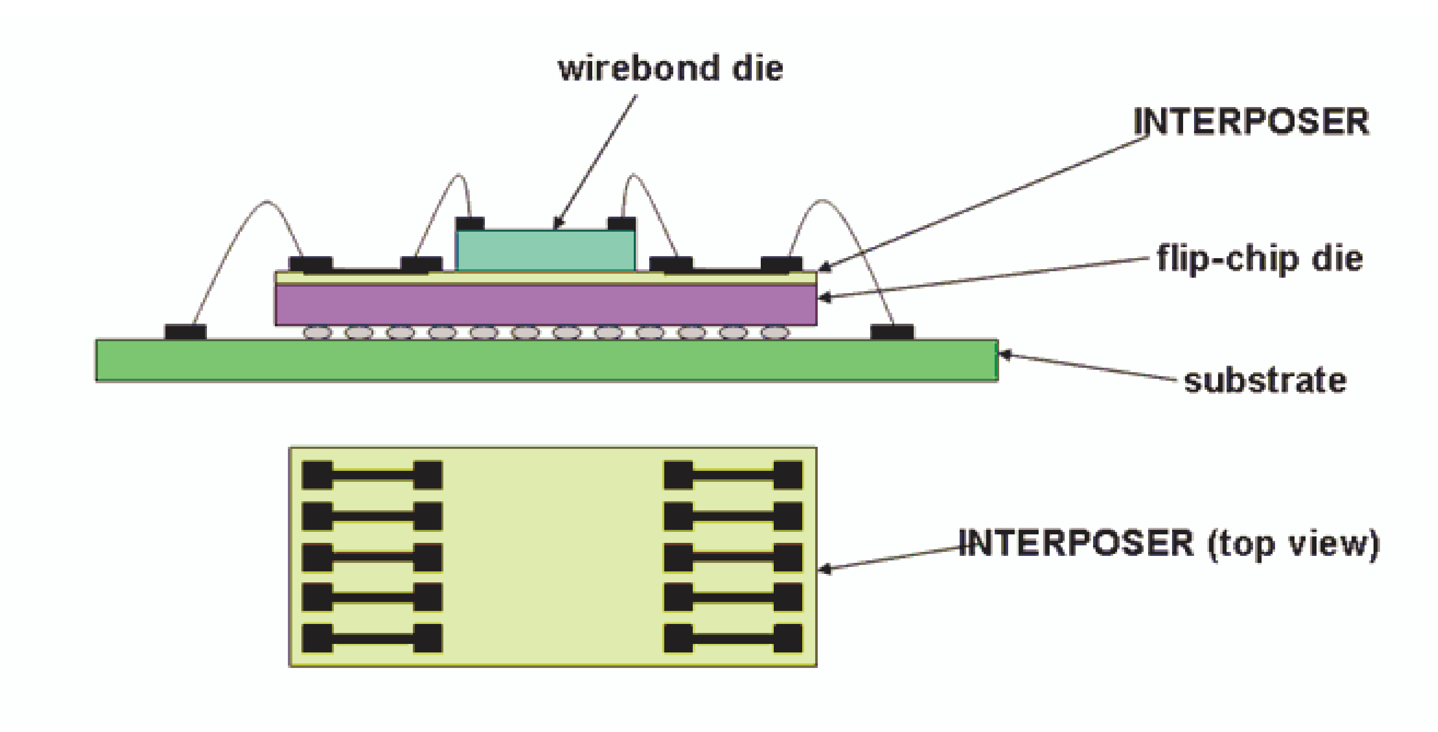
Actual Stack Design

3D Stack Viewer

3D Stack Design

Complex die stack design

- Interposer



Systems interconnect

Driving I/O buffer on chip

C4 Bump

Pin on chip package

PCB to PCB

Receiving I/O buffer on chip

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  - Co-Design environment
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Modeling and analysis challenges

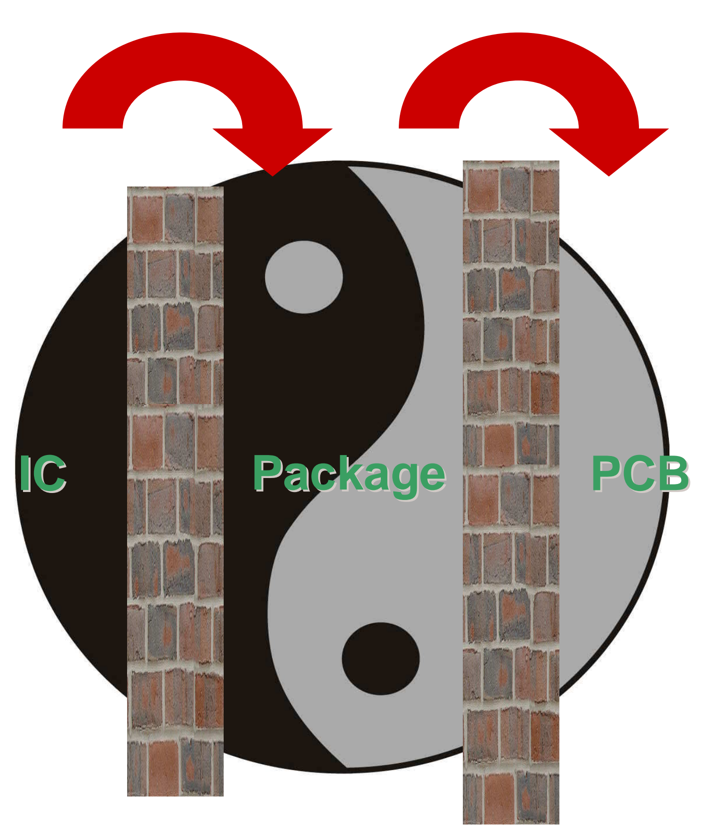
- Optimization requires design automation
- Recongnicing the differences between SiP design and classic single package and PCB designs
- Issues
  - Multiple stacked dies are placed vertically or horizontally
  - Connection between multiple dies are realized by wirebonding, interposer, interconnect, or flip-chip technology
  - IC design needs to consider package design, while package design needs to consider IC requirements
    - How to make die information available to package designers, and how to pass package models back to IO designers to simulate entire signal path
      - Data passing and property mapping

Modeling and analysis challenges

- Fundamental requirements for SiP tools
  - An environment with IC/package/board co-design and co-simulation capabilities
  - To provide engineers with Signal Integrity (SI) and Power Integrity (PI) solutions
    - Concurrent pre-route analysis and post-route verification

Current methodologies must change

- Isolated IC, Package, and PCB design tools increases costs and design cycle times
  - Many problems not discovered until integration (costly iterations)
- New methodology requires full system interconnect planning
  - IC package interconnect and its influence must be fully understood and modeled
  - Must arbitrate connection scheme across chip, package and board
- Timing, signal integrity and power delivery intertwined
  - Full analysis of system interconnect from buffer to buffer required
- Constraints have to be established based on accurate pre-route analysis



Opening Up the Solution Space

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IC Design Space

Package Design Space

Board Design Space

I/O Pad ⇔ Bump Array Placement and Optimization

RDL Routing

I/O Pad to Bump Delays

System Level I/O Buffer Characterization

I/O Pad to Package Pin Physical Design and Modeling

Package Footprint Creation

Schematic Symbol Creation

I/O Pad to Package Pin Delays

Package Pin Optimization

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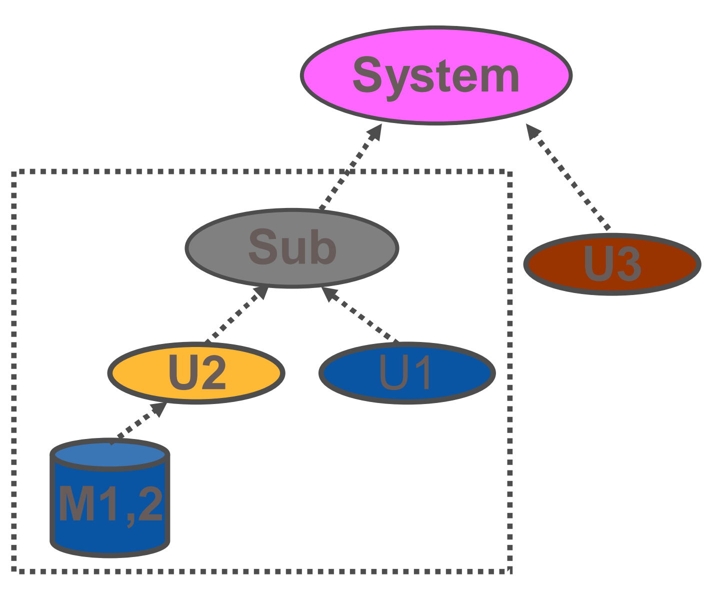
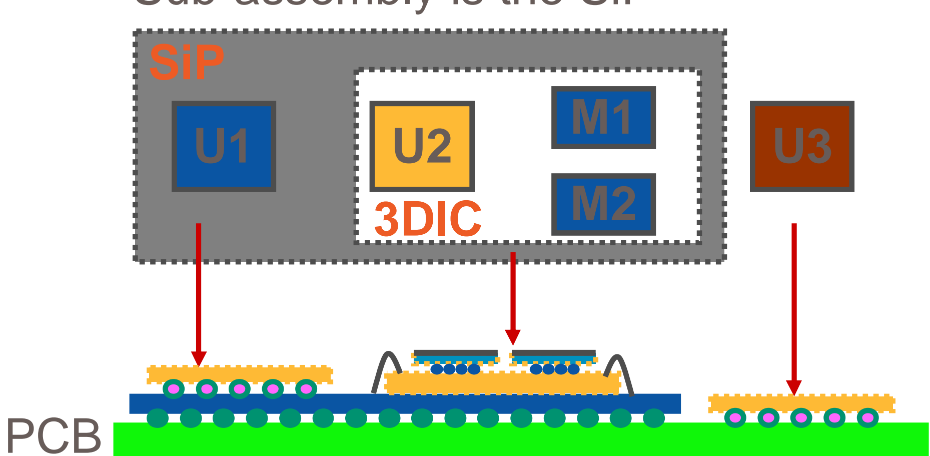
SiP digital design flow



System Design Hierarchy

- Concurrent designs & independent teams
- Unique IC processes
- Design chain geographically diverse



Resulting SiP

Complex 3D Structures & Technologies

- U1: flip chip, 90nm digital
- 3DIC:
  - U2: wire bond 130nm
  - M1 & M2: wire bond 90nm memory
- U3: fixed die, flip chip 130nm digital

SiP digital design methodology

Co-design Environment

VSIC Model

System Arch

Partition into Components

Architect

Concept Planning

Feasibility & Analysis

Layout

Multi-domain Multi-technology Implementation

SI/PI

System Integration & Verification

Manufacturing

Design Planning

Interconnect Planning

Test Concept

Manufacturability

Modeling & Verification

Digital SiP connectivity hierarchy

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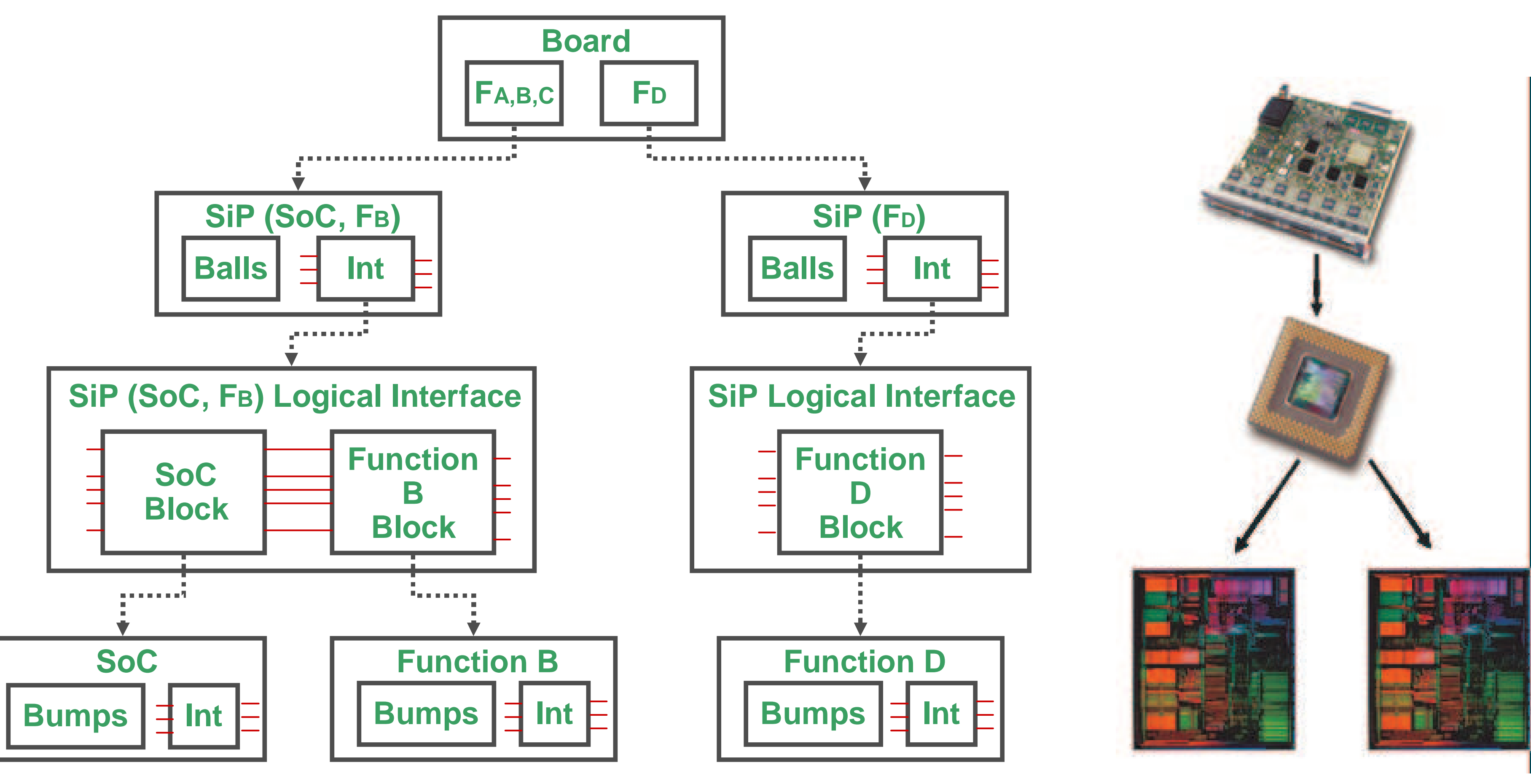

Co-design dies

- IC tool based die abstract editor
- Co-design die are hierarchical design elements on substrate
- Die abstracts management
- Data Import/Export

Concurrent design to enable optimization of DIE abstracts

SIP IO Planner
Co-design DIE

Flip chip with drivers, RDL and Bumps

SiP Substrate Editor

Wire bond chip (standard)

Flip chip (standard)

Route feasibility analysis: IC-RDL and SiP substrate

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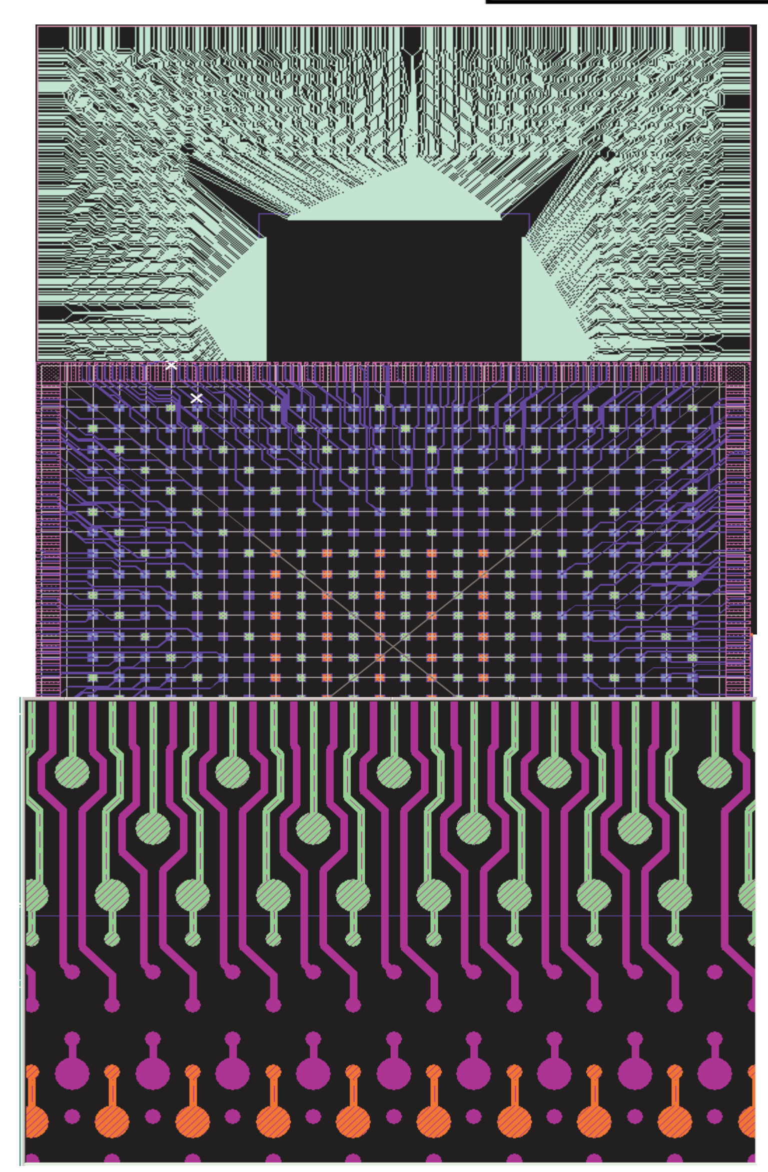
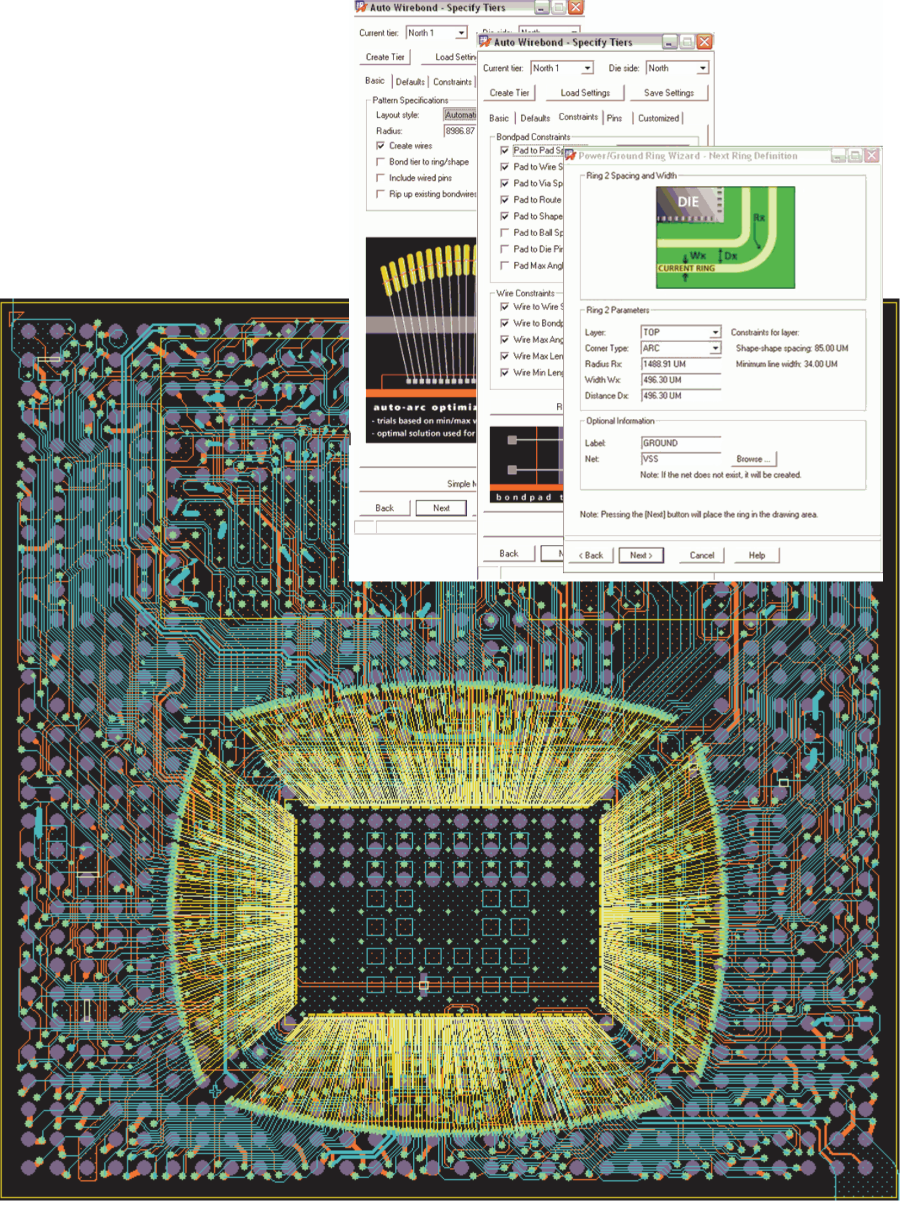
- Flip Chip or Wirebond Attachment
  - Automatic optimization strategies via node swapping
- Based on Package Pin Assignment
- Flip Chip Escape Patterns
- Feasibility Routing for RDL
  - IOP mask ready RDL routing
  - I/O Buffer to Bump/Die Pad in IOP
- IC-Pkg routability analysis
  - All angle, Orthogonal, Diagonal
  - Support for Differential Signaling
  - Materials and Standard Package trade-offs
  - Full mask ready substrate routing



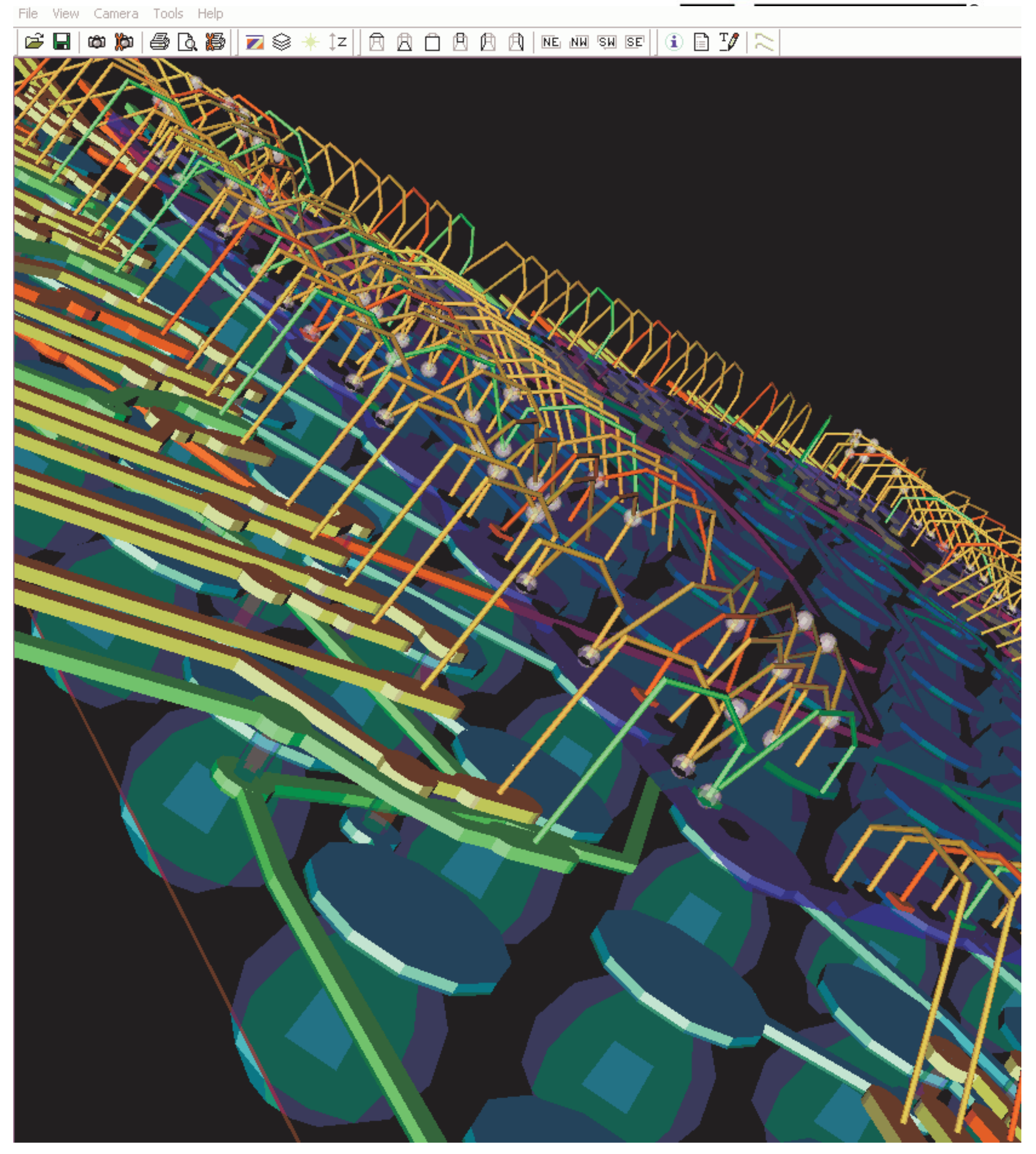
Package Physical Layout

- Automatic Bond Shell Creation
- Net assignment based on Routability of Package
- All angle auto-routing
- Unique routers for wire-bond and flip-chip routing styles
  - DRC correct
  - Electrical constraints and Physical rules



3D Visualization

- Support for Die Stacks
- Bond Wire Clearance Checking
  - Reverse Bonding
- Micro-Via Checking



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Co-design methodologies in high-speed design

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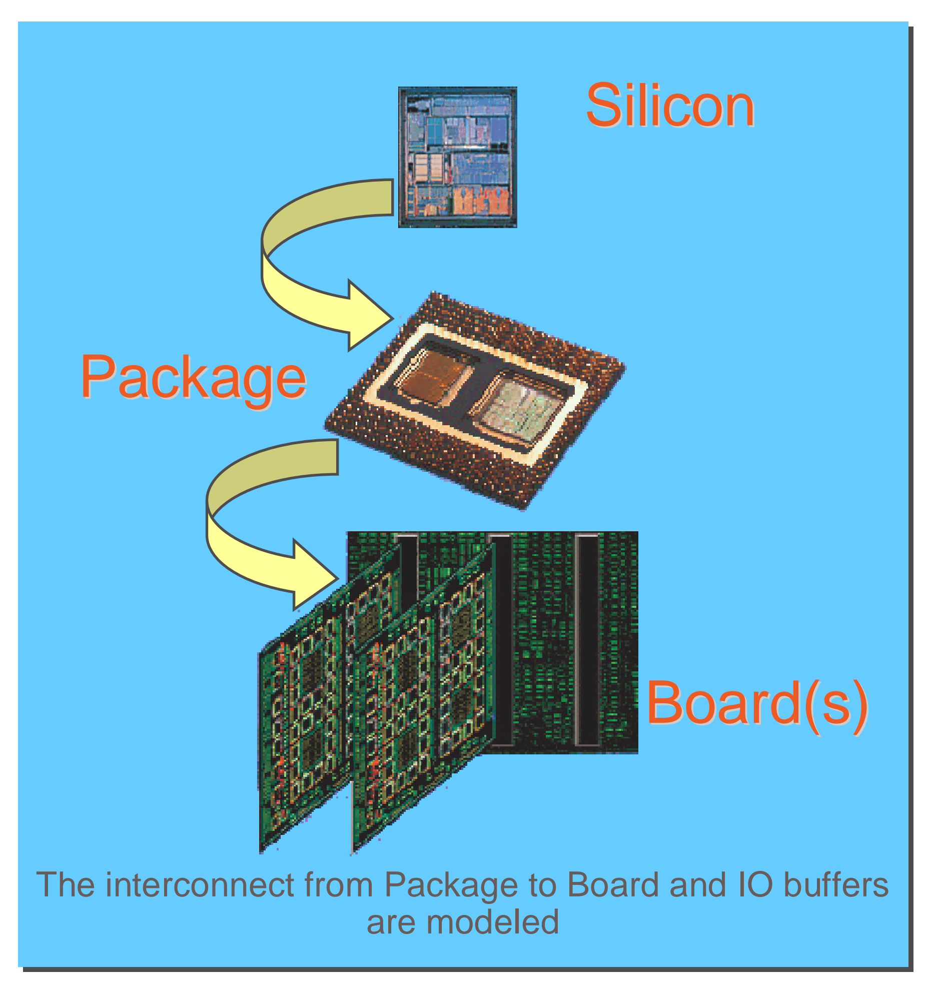
- Problem1: Signal path from silicon to board through package
  - Reflections, xtalk, timing



Co-design methodologies in high-speed design (cont’)

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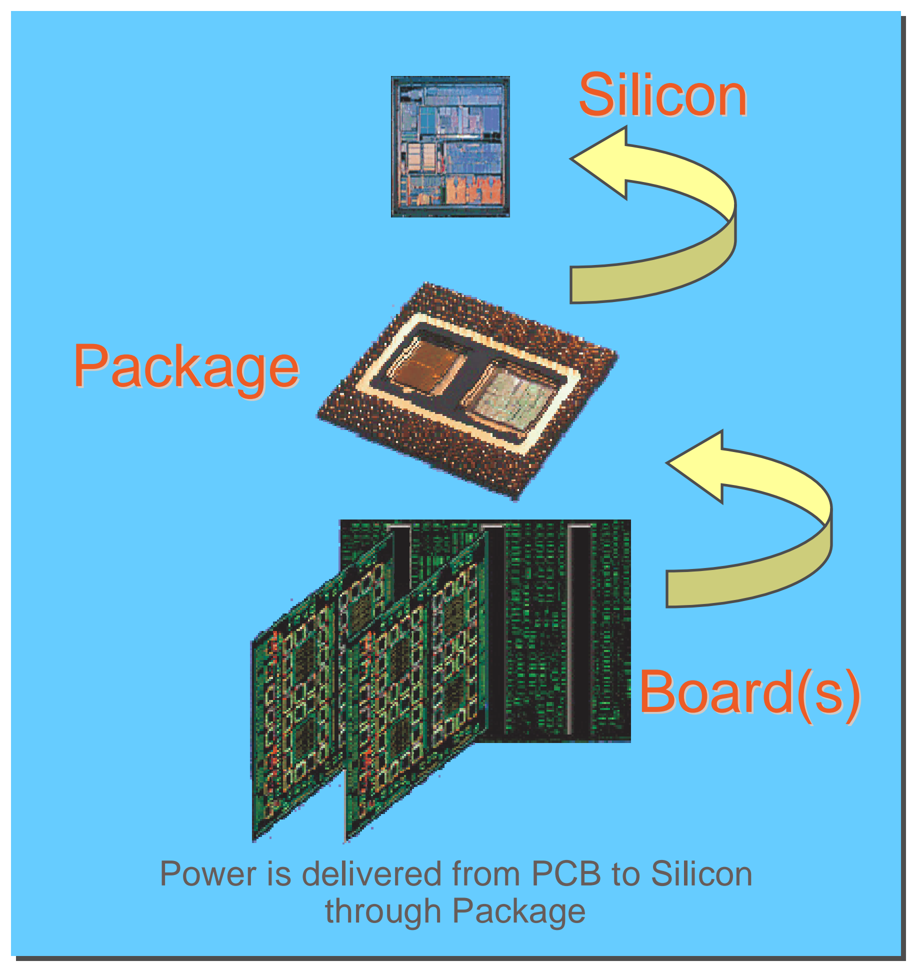
- Problem 2: Power delivery path from board to silicon through package



Co-design methodologies in high-speed design (cont')

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- Problem 3: Effects between signal and power supply

Problem 3: Interference of signal and power

Problem 1: signal

Silicon

Package

Board

Problem 2: power

Signal analysis: Establishing constraints

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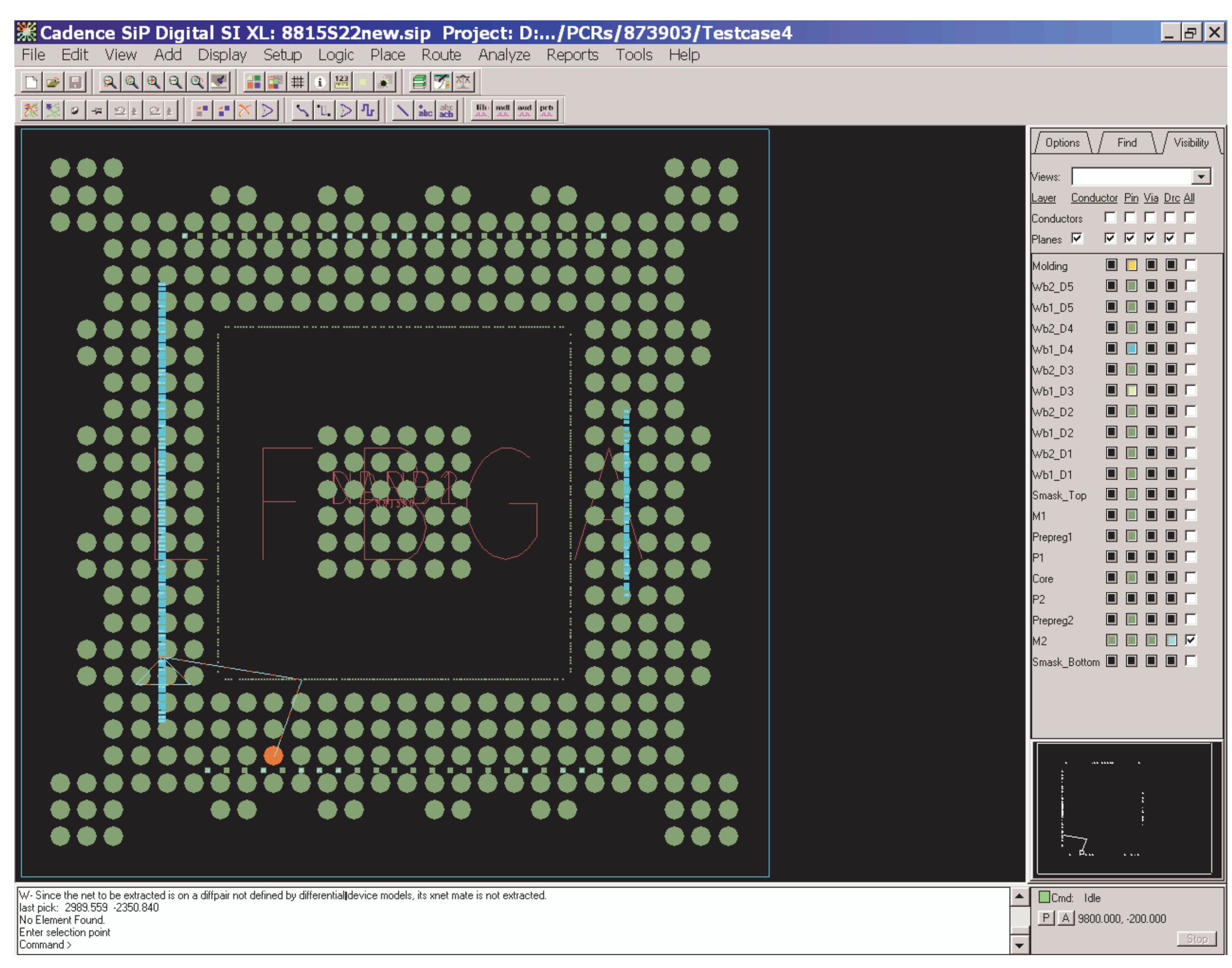
- Early exploration on multi-die connection



Signal analysis: Establishing constraints

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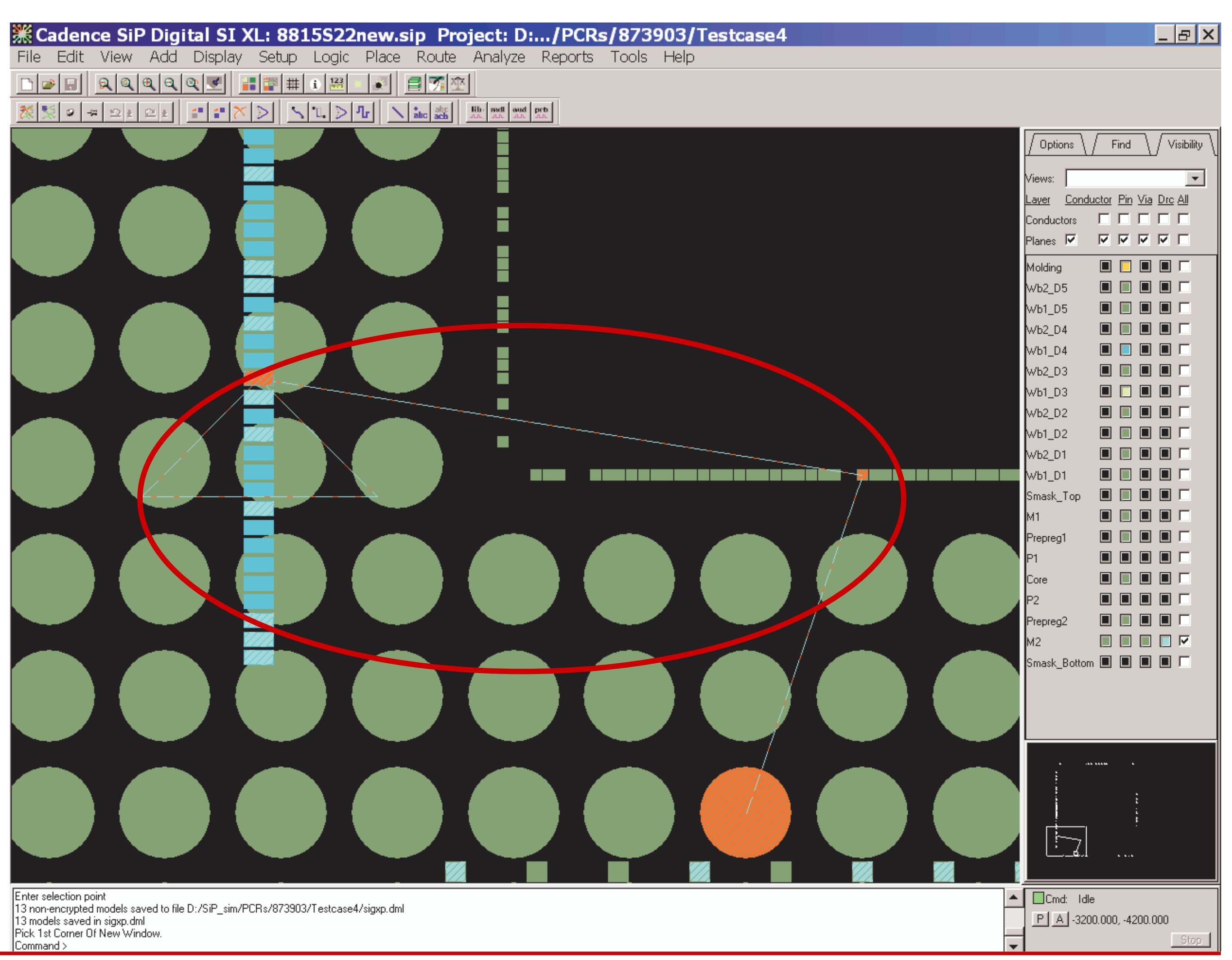
- Early exploration on multi-die connection



Signal analysis: Establishing constraints

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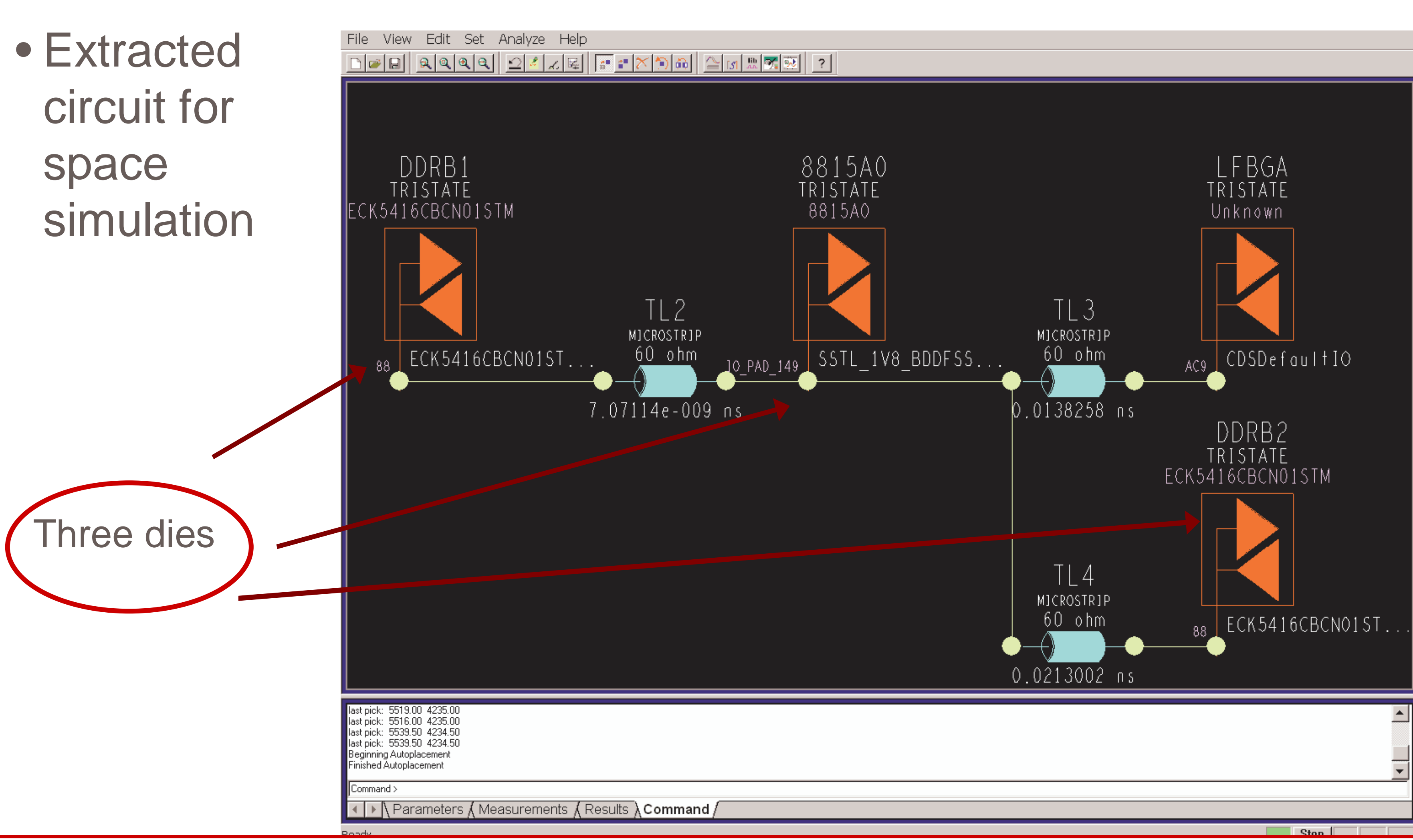
- Extracted circuit for space simulation

Three dies



Signal analysis: interconnect modeling

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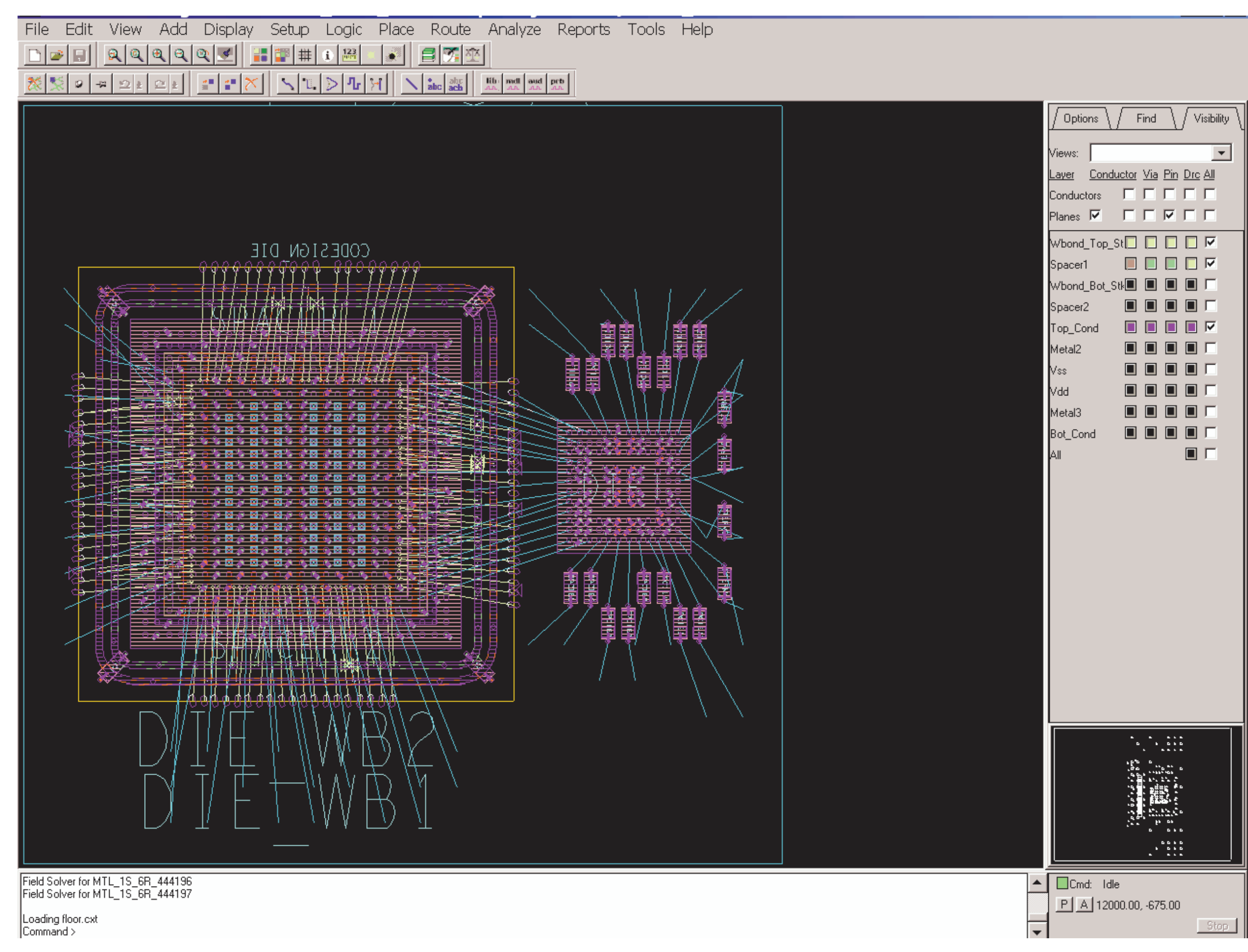
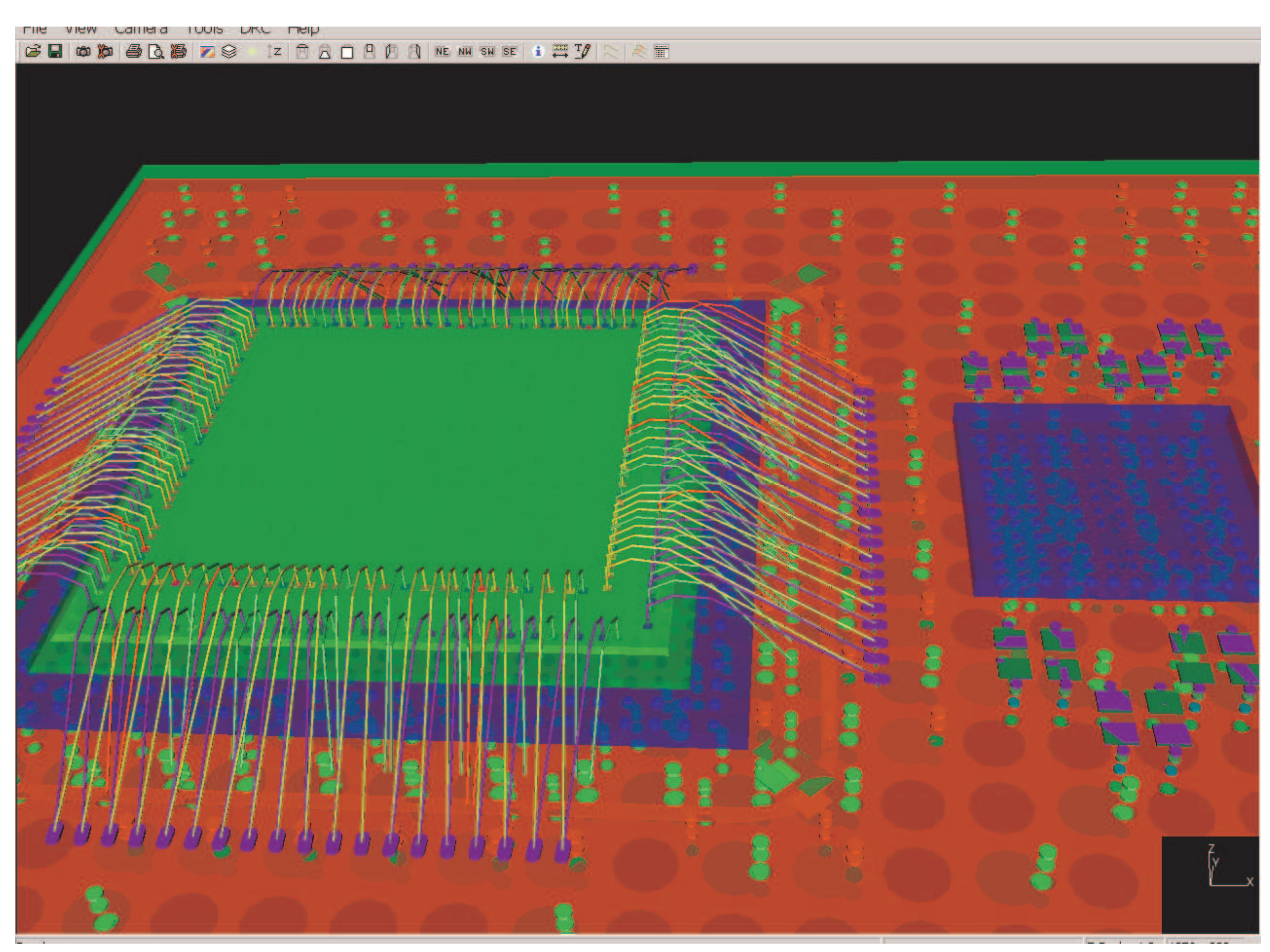
- Detailed interconnect modeling



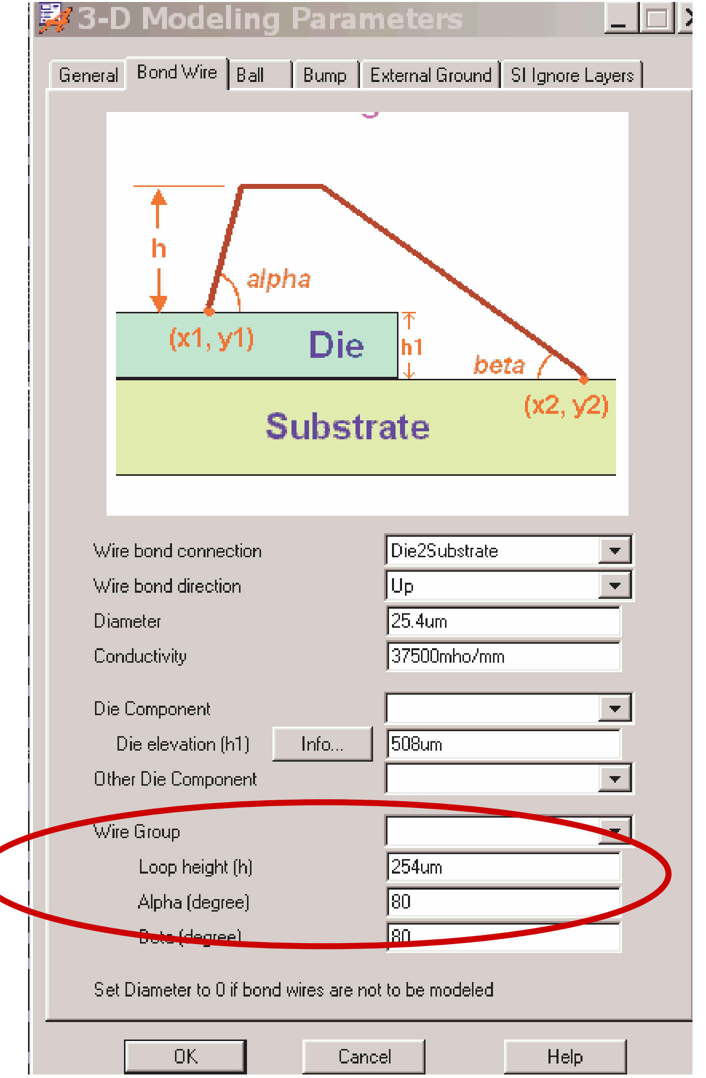
Signal analysis: assistant to analysis

- 3D view



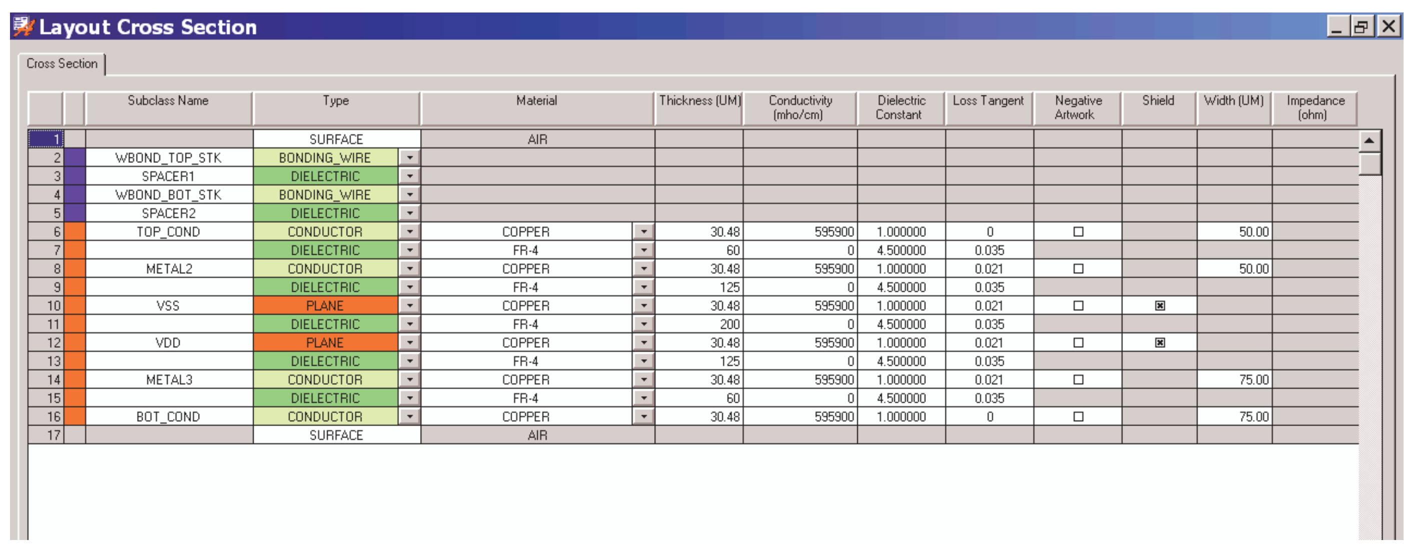
Signal analysis: wirebond constraints

- Perform what/if analysis by changing wirebond profiles
  - Work with existing design and/or start new design
  - Edit the parameters
  - Update (or extract) constraints



Signal analysis: stackup design

- Crossection details



Layout Cross Section

Cross Section

	Subclass Name	Type	Material	Thickness (UM)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (UM)	Impedance (ohm)
1		SURFACE	AIR								
2	WBOND_TOP_STK	BONDING_WIRE									
3	SPACER1	DIELECTRIC									
4	WBOND_BOT_STK	BONDING_WIRE									
5	SPACER2	DIELECTRIC									
6	TOP_COND	CONDUCTOR	COPPER	30.48	595900	1.000000	0	☐		50.00	
7		DIELECTRIC	FR-4	60	0	4.500000	0.035				
8	METAL2	CONDUCTOR	COPPER	30.48	595900	1.000000	0.021	☐		50.00	
9		DIELECTRIC	FR-4	125	0	4.500000	0.035				
10	VSS	PLANE	COPPER	30.48	595900	1.000000	0.021	☐	☒		
11		DIELECTRIC	FR-4	200	0	4.500000	0.035				
12	VDD	PLANE	COPPER	30.48	595900	1.000000	0.021	☐	☒		
13		DIELECTRIC	FR-4	125	0	4.500000	0.035				
14	METAL3	CONDUCTOR	COPPER	30.48	595900	1.000000	0.021	☐		75.00	
15		DIELECTRIC	FR-4	60	0	4.500000	0.035				
16	BOT_COND	CONDUCTOR	COPPER	30.48	595900	1.000000	0	☐		75.00	
17		SURFACE	AIR								

Signal analysis: wirebond modeling

- Interested wirebonds

Signal analysis: wirebond model re-use

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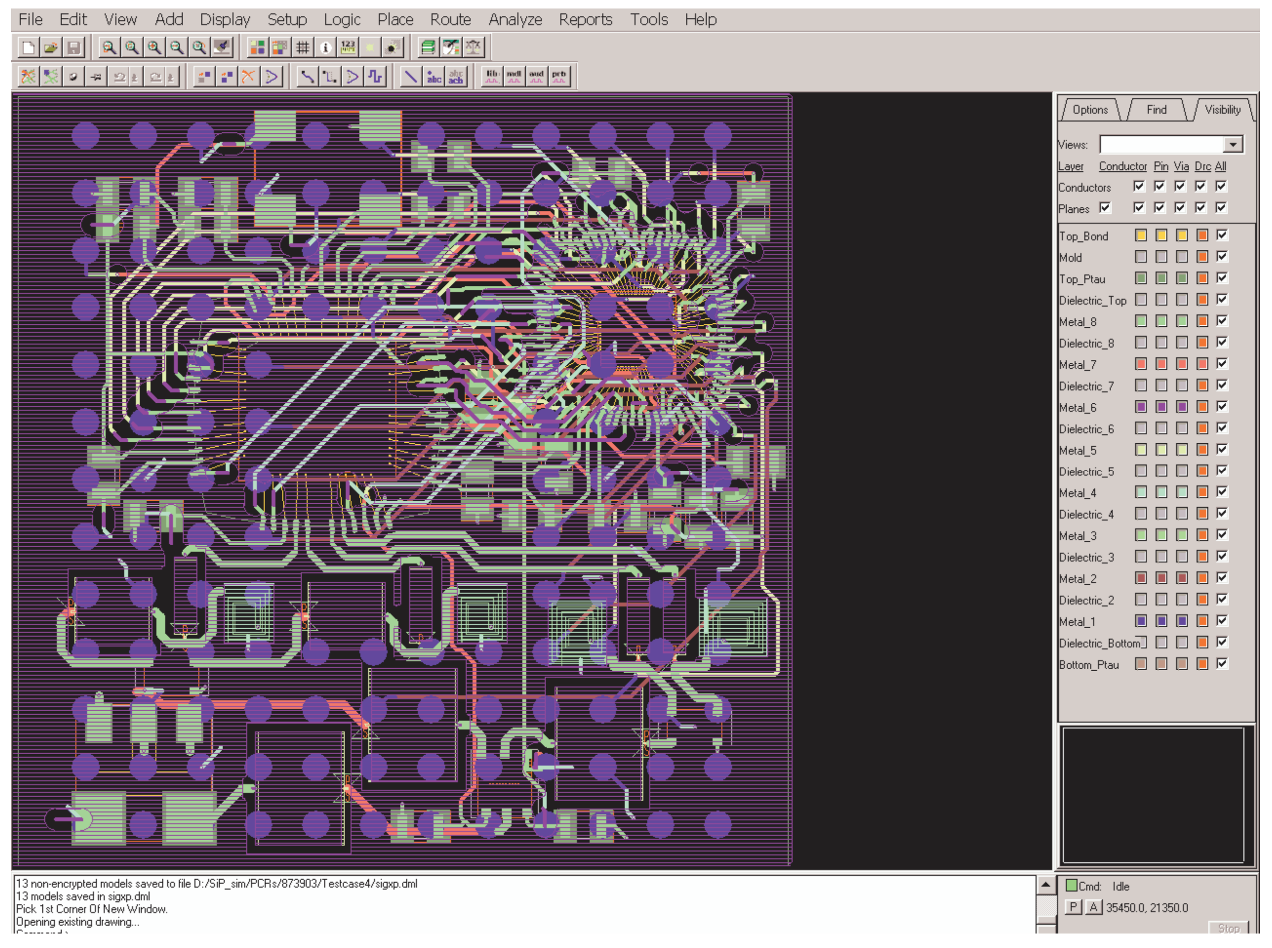
- Extracting models from existing design



Signal analysis: wirebond model re-use

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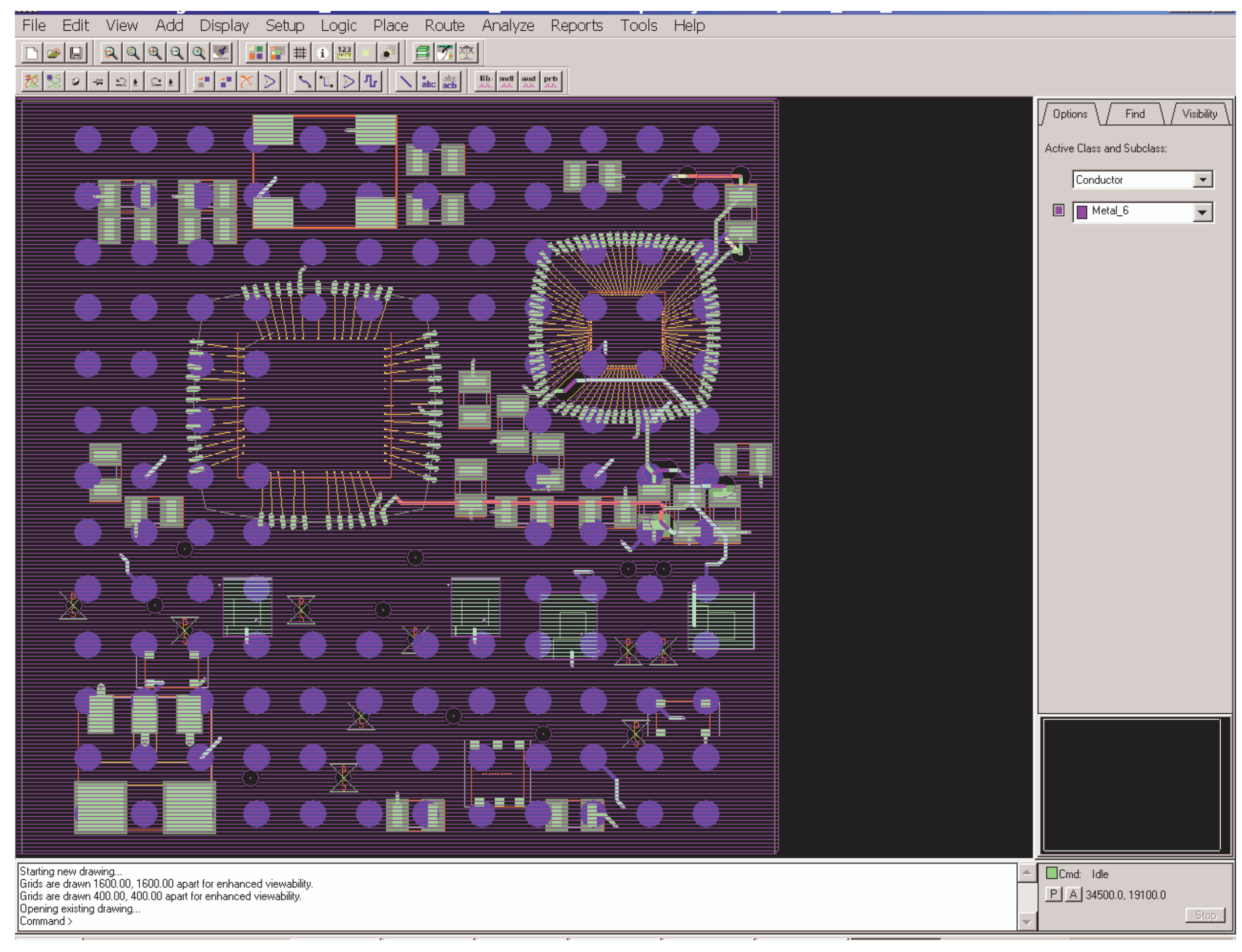
- The corresponding design with only wirebonds



Signal analysis: wirebond model re-use

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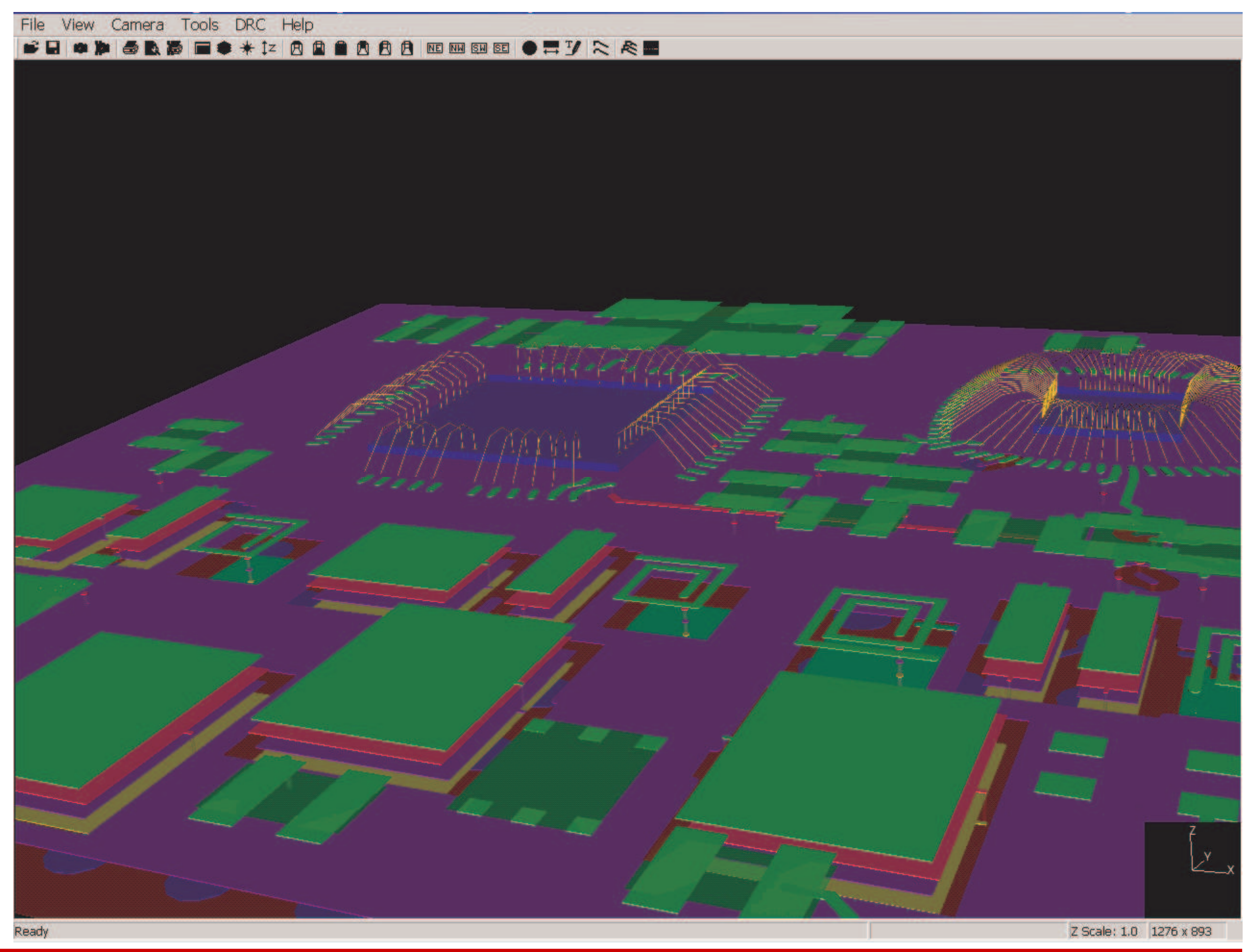
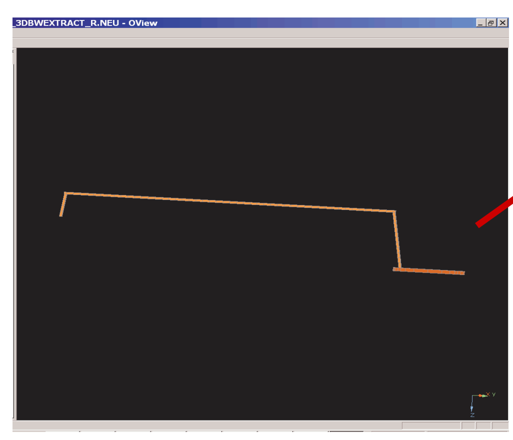
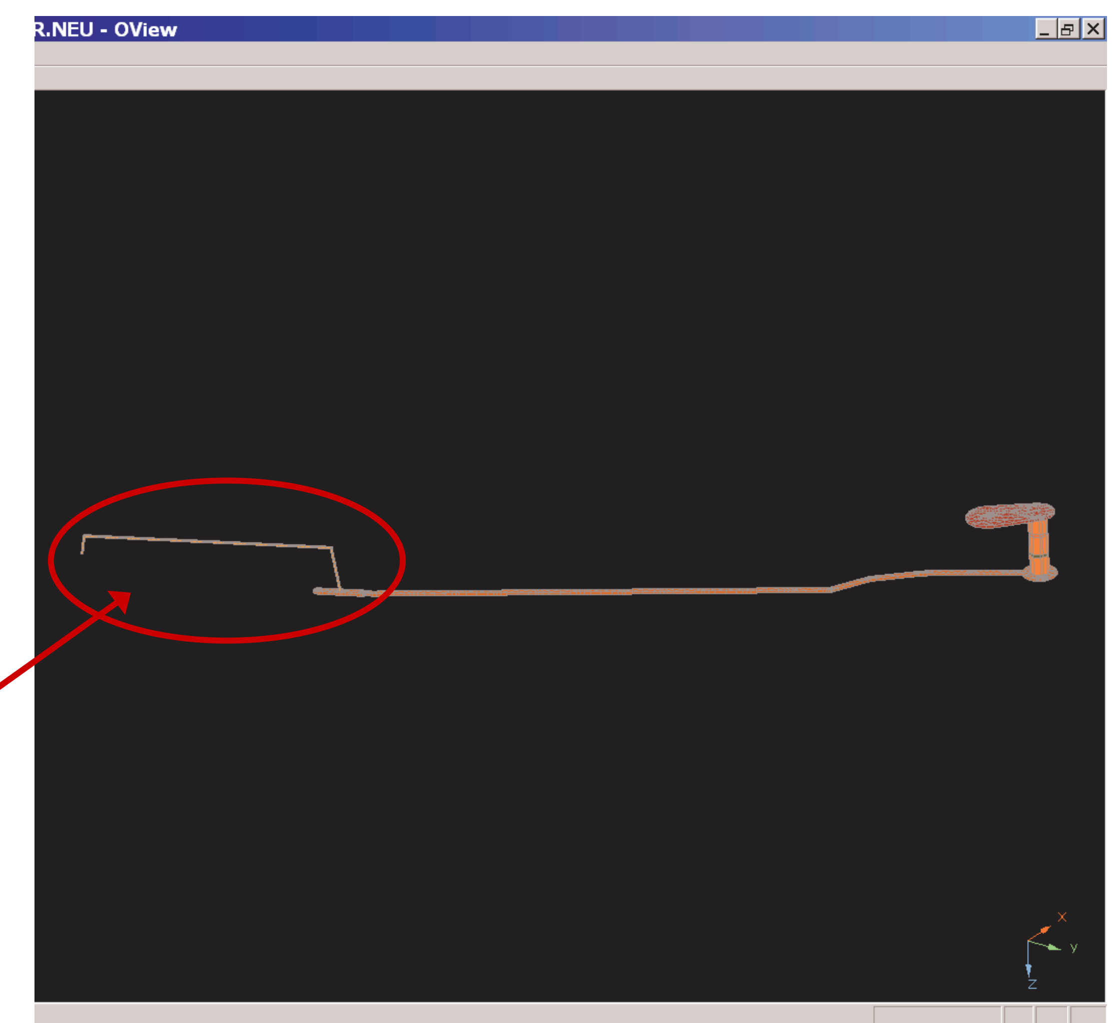
- 3D view of the multi-die design



Signal analysis: wirebond model reuse

- View geometry mesh
  - Original net (in full)





Signal analysis: reflections, crosstalks, timing

- Building simulation circuits
  - 3D modeling

Signal analysis: reflections, crosstalks, timing

- Simulation circuit

Two dies

Power analysis: power delivery

- Power delivery to multiple dies

File Edit View Add Display Setup Logic Place Route Analyze Reports Tools Help

Pick 1st Corner Of New Window.
Enter selection point
last pick: 25466.6 17862.1
Enter selection point

Power analysis: power delivery

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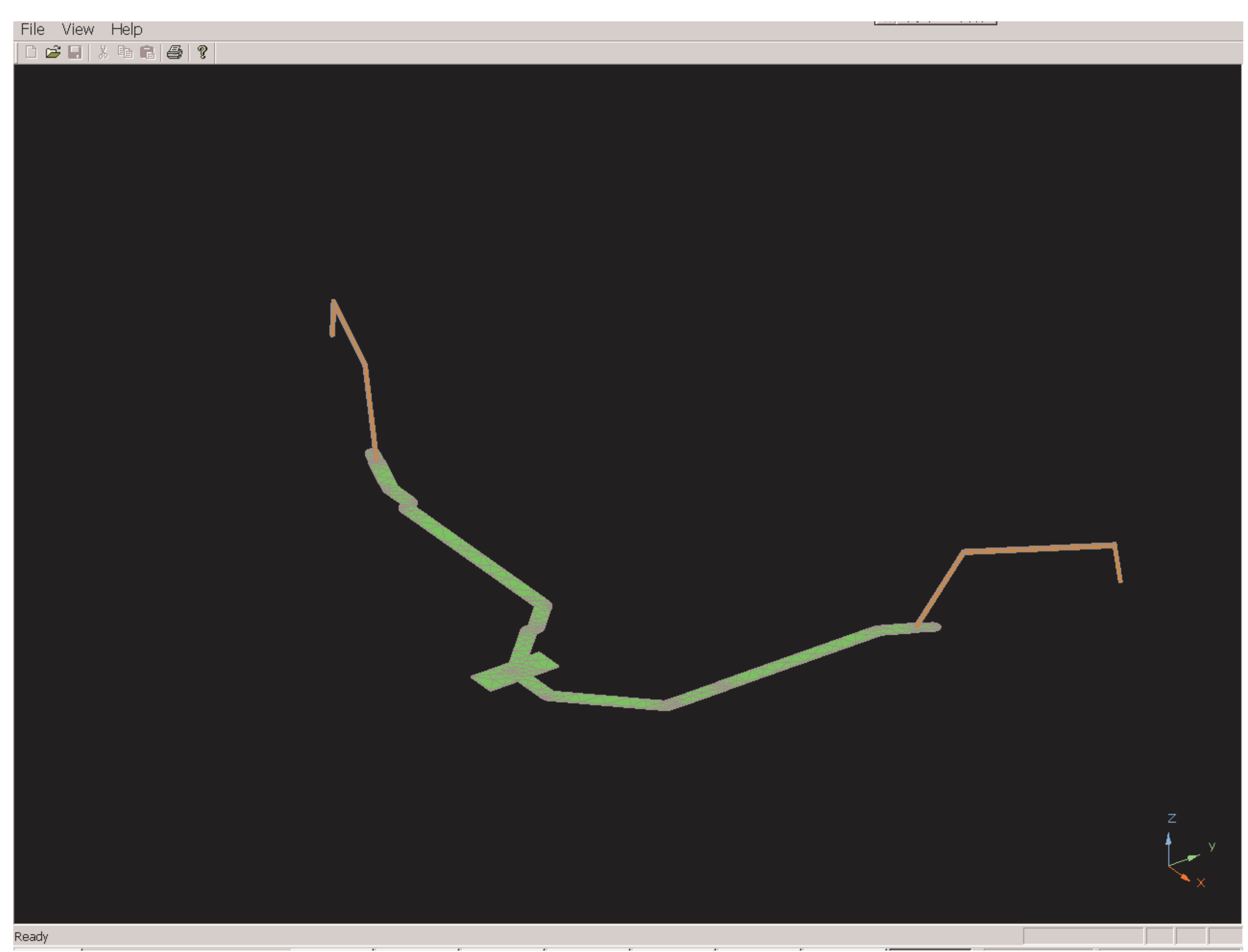
- Power delivery to multiple dies



Power analysis: power delivery

- Power delivery to multiple dies
  - Decoupling capacitor selection and placement

Power analysis: IR-Drop analysis at IC level with package effects included (cont')

- Voltagestorm output using multi-port DC net model of package

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Vstorm B6.1.2c
show
ON METAL_8
ON VIA_7
ON METAL_7
ON VIA_6
ON METAL_6
ON VIA_5
ON METAL_5
ON VIA_4
ON METAL_4
ON VIA_3
ON METAL_3
ON VIA_2
ON METAL_2
ON VIA_1
ON METAL_1

Plot : IR

0%	0.922 - 0.950 V
0%	0.950 - 0.990 V
0%	0.990 - 1.020 V
0%	1.020 - 1.050 V
0%	1.050 - 1.080 V
0%	1.080 - 1.120 V
7%	1.120 - 1.160 V
92%	1.160 - 1.200 V

Design: data/routed1_5.5via.def.gz | Library: ./work/lib_merged | ir_nopkg.gif | Wed Aug 23 17:12:03 2006

cadence
Vstorm B6.1.2c
show
ON METAL_8
ON VIA_7
ON METAL_7
ON VIA_6
ON METAL_6
ON VIA_5
ON METAL_5
ON VIA_4
ON METAL_4
ON VIA_3
ON METAL_3
ON VIA_2
ON METAL_2
ON VIA_1
ON METAL_1

Plot : IR

0%	0.922 - 0.950 V
0%	0.950 - 0.990 V
1%	0.990 - 1.020 V
21%	1.020 - 1.050 V
78%	1.050 - 1.080 V
0%	1.080 - 1.120 V
0%	1.120 - 1.160 V
0%	1.160 - 1.200 V

Design: data/routed1_5.5via.def.gz | Library: ./work/lib_merged | ir_nport.gif | Wed Aug 23 17:06:10 2006

Without package effects

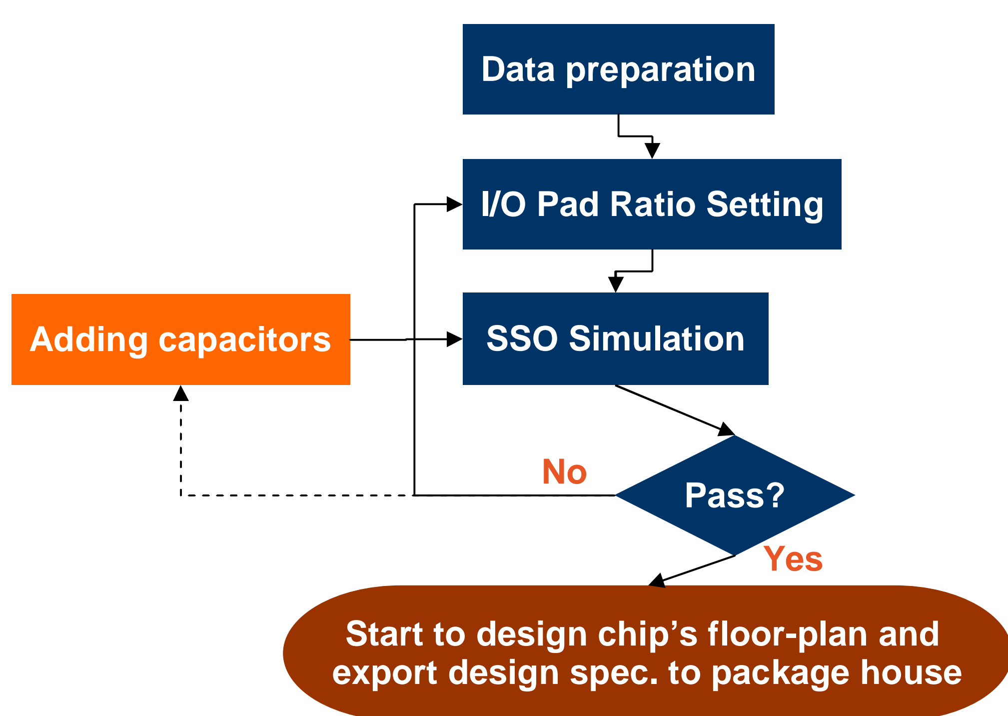
Worst IR-drop : 155mV

With N-port DC net model in package

Worst IR-drop : 253mV

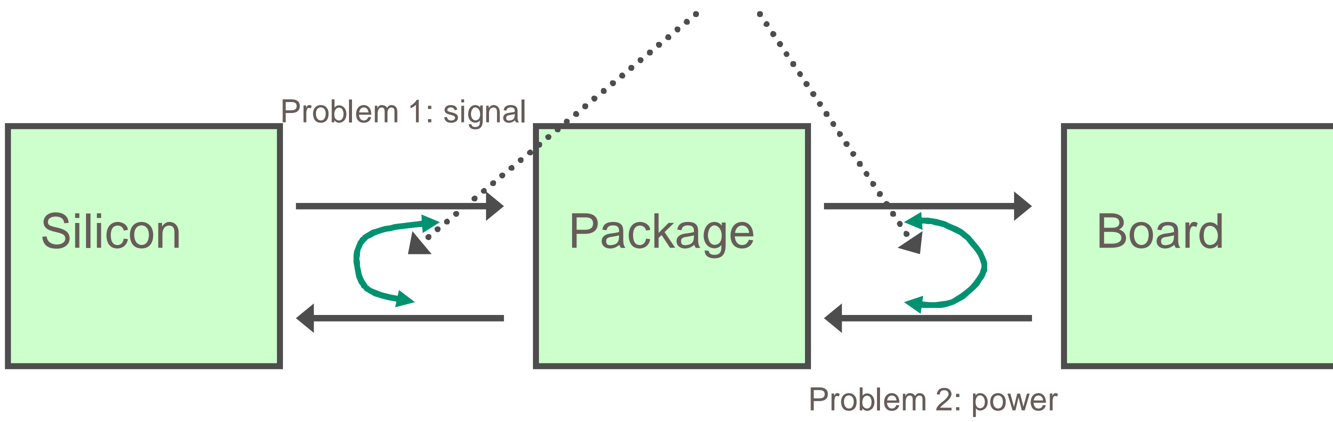
Power analysis: stability study

- Estimate SSO/SSN impacts at early design stage
  - This methodology helps decide the ratio of signal I/O pads to power & ground pads before starting chip design



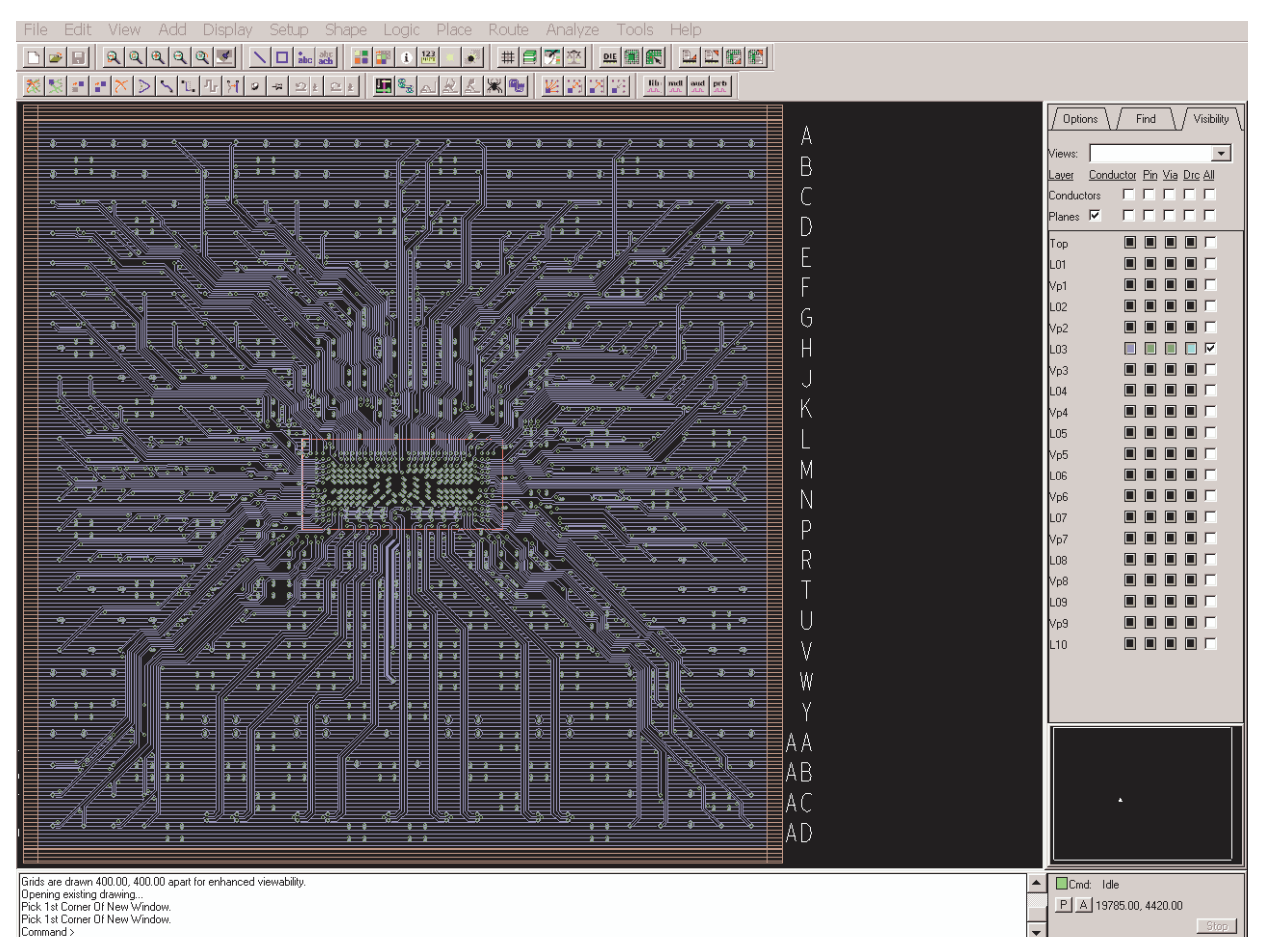
Co-simulation in SiP: final verification

- Final verification for solutions 1-3
  - Consider entire signal path
    - Silicon to board through package
    - Examine signal quality and timing budget
  - Consider power stability
  - Key is SSN analysis



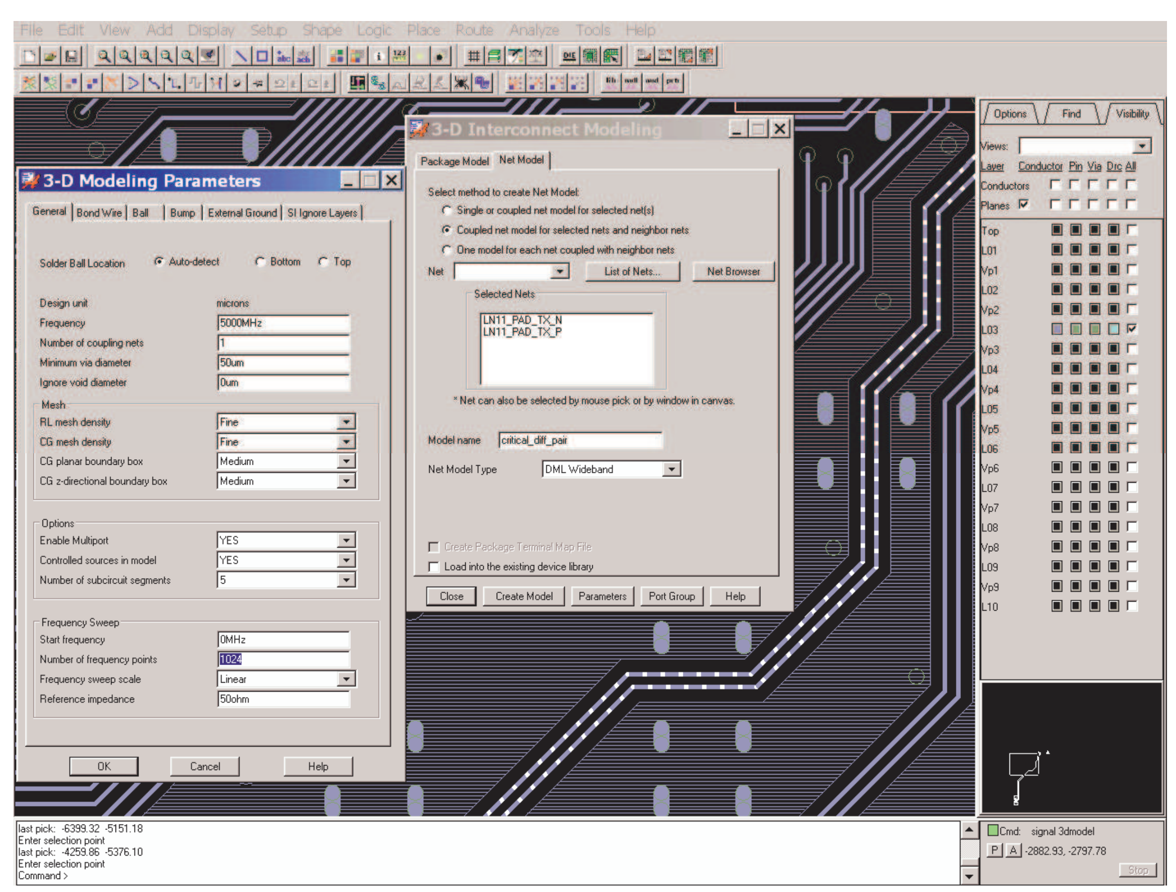
Co-simulation in SiP: final verification

- Design example: finished package design
  - Many diff. pairs
  - Multi-GHz signaling



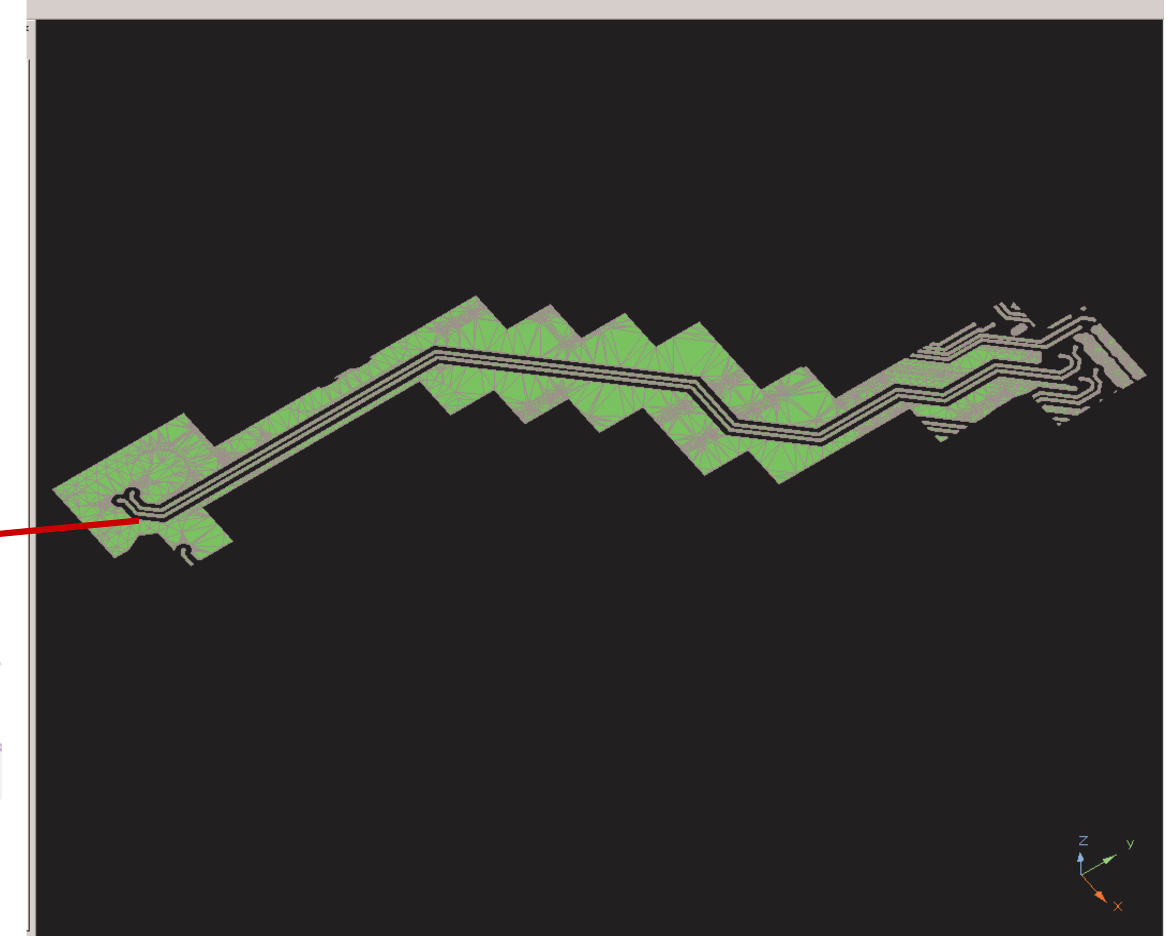
Co-simulation in SiP: final verification

- Design example
  - Finished package design
    - Wideband model extraction



Co-simulation in SiP: final verification

- Design example
  - Mesh view of a pair of critical differential signals



Co-simulation in SiP: final verification

- Design example
  - Driver/receiver model
    - Transistor level model wrapped in Spectre format
    - Macromodel
  - Long trace representing board
  - Run Spectre directly in SiP environment

File View Edit Set Analyze Help

Analysis Preferences

Simulation Modes | Measurement Modes | EMI

Pulse Stimulus | Simulation Parameters

Fixed Duration: 25ns

Waveform Resolution: 0.02ns

Cutoff Frequency: 10GHz

Buffer Delays: From Library

Save Sweep Cases

Simulator Spectre | Set Simulator Preferences...

Fast/Typical/Slow Definitions...

OK | Cancel | Help

last pick: 5456.50 4225.00
last pick: 5593.00 4206.00
last pick: 5609.50 4218.50

Command >

Parameters | Measurements | Results | Command

Co-simulation in SiP: final verification

- Large package model

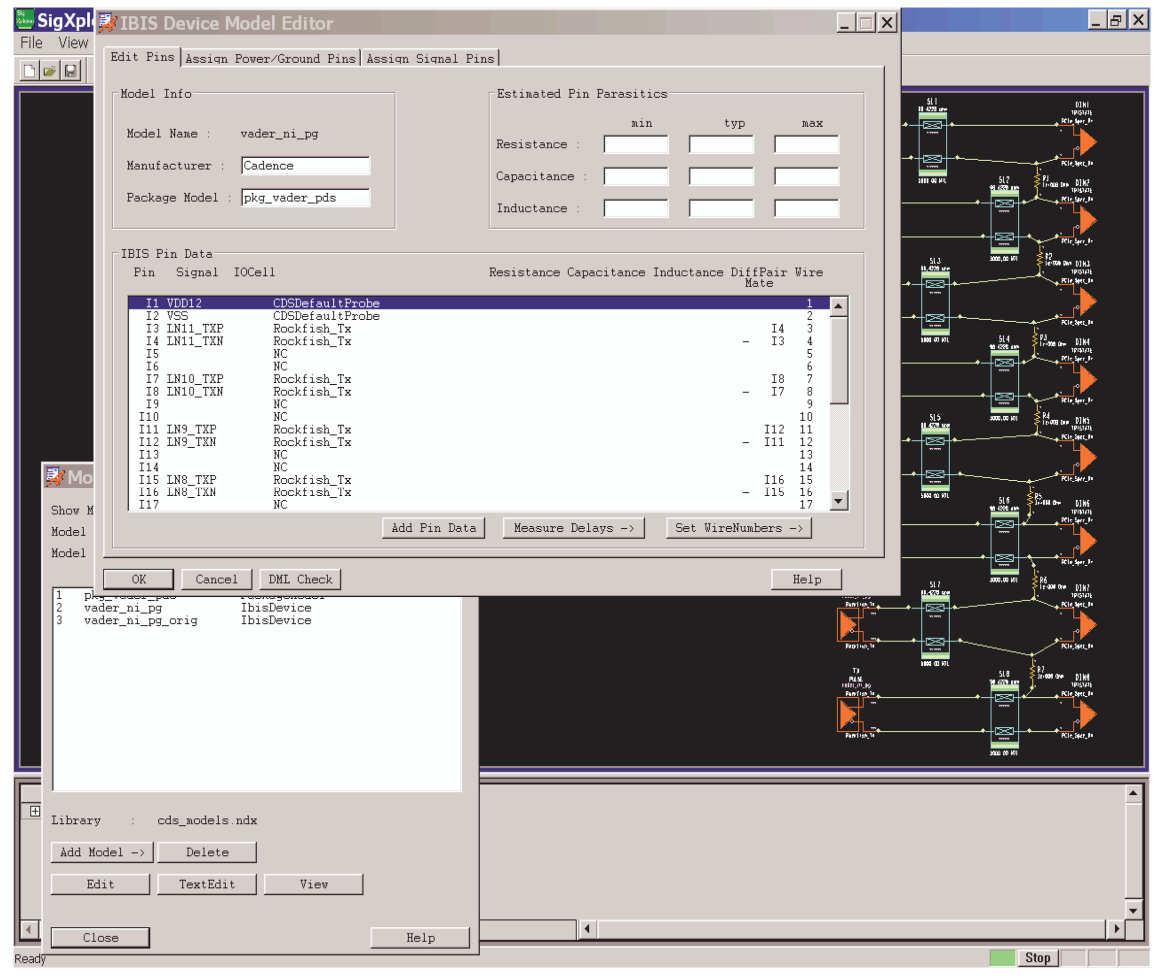
File Edit View Insert Format Help

```
("pkg_vader_pds"
     ("CircuitModels"
       ("SingleLineCircuits"
           ("1-34"
             ("SubCircuitName" "pkg_single")
           )
       )
       ("CoupledLineCircuits"
           ("1-4, 7-8, 11-12, 15-16, 21-22, 25-26, 29-30, 33-34"
             ("Terminals" "1.in" "1.out" "2.in" "2.out"
                 "3.in" "3.out" "4.in" "4.out" "7.in"
                 "7.out" "8.in" "8.out" "11.in" "11.out"
                 "12.in" "12.out" "15.in" "15.out" "16.in"
                 "16.out" "21.in" "21.out" "22.in" "22.out"
                 "25.in" "25.out" "26.in" "26.out" "29.in"
                 "29.out" "30.in" "30.out" "33.in" "33.out"
                 "34.in" "34.out"
             )
             ("SubCircuitName" "vader_pds")
           )
       )
       ("SubCircuits"
"

.subckt pkg_single in out
* This is a simple single-line circuit.
r1 in 1 2m
t1 1 0 2 0 z0=50 td=75n
r2 2 [illegible] 2m
.ends pkg_single

.subckt vader_pds I1 O1 I2 O2 I3 O3 I4 O4 I7 O7 I8 O8
+ I11 O11 I12 O12 I15 O15 I16 O16
+ I21 O21 I22 O22 I25 O25 I26 O26 I29 O29 I30 O30
+ I33 O33 I34 O34
*
* Convergence aids
[illegible]converge1 I1 I2 100p
Cconverge[illegible] 100p
RconvergeI3 I3 0 100meg
RconvergeI4 I4 0 100meg
RconvergeI7 I7 0 100meg
RconvergeI8 I8 0 100meg
RconvergeI11 I11 0 100meg
RconvergeI12 I12 0 100meg
RconvergeI15 I15 0 100meg
RconvergeI16 I16 0 100meg
RconvergeI21 I21 0 100meg
RconvergeI22 I22 0 100meg
RconvergeI25 I25 0 100meg
RconvergeI26 I26 0 100meg
RconvergeI29 I29 0 100meg
RconvergeI30 I30 0 100meg
RconvergeI33 I33 0 100meg
RconvergeI34 I34 0 100meg
```

For Help, press F1

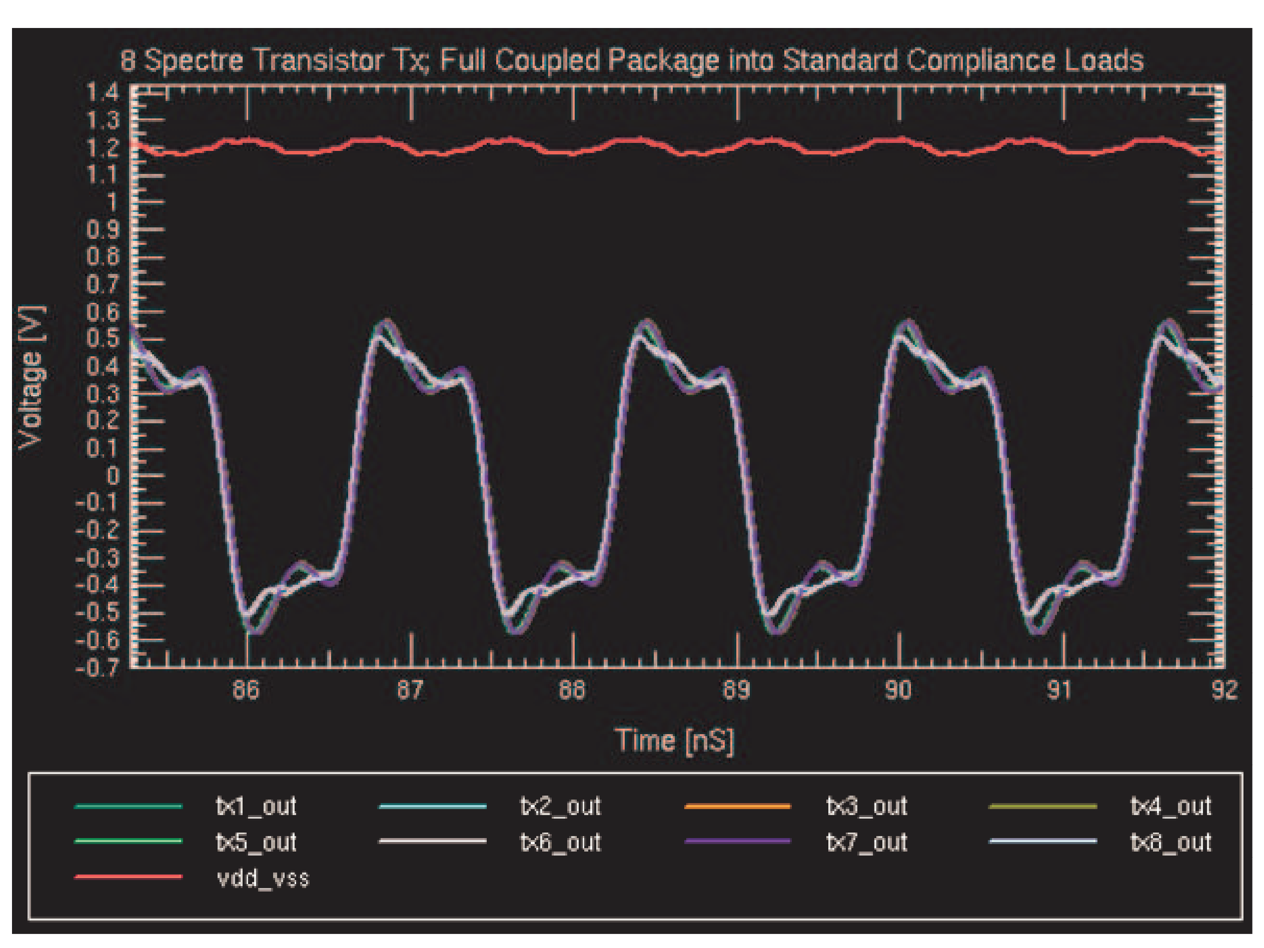
Co-simulation in SiP: final verification

- Assign package model and power/ground buses



Co-simulation in SiP: final verification

- Results of detailed Spectre simulation
  - 8 Lane SSO analysis results



Summary

- System-in-Package is the right integration solution for wireless and consumer products
  - It posts great challenges to designs and analyses (differences between single package and PCB designs)
- Design tools are evolving to meet the needs of designers
  - IC-Package-Board co-design and co-simulation enable designs to be optimized to meet design requirements
- SiP Digital tool
  - Providing a co-design environment for SiP interconnect including embedded ICs and the target printed circuit board
  - Including integrated signal integrity, parasitic extraction/modeling and substrate interconnect editing, power delivery, and signal/power interference analyses

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Thank you