Future Directions in IC and Package Design Workshop

Signal Bandwidth for High-Performance Computing

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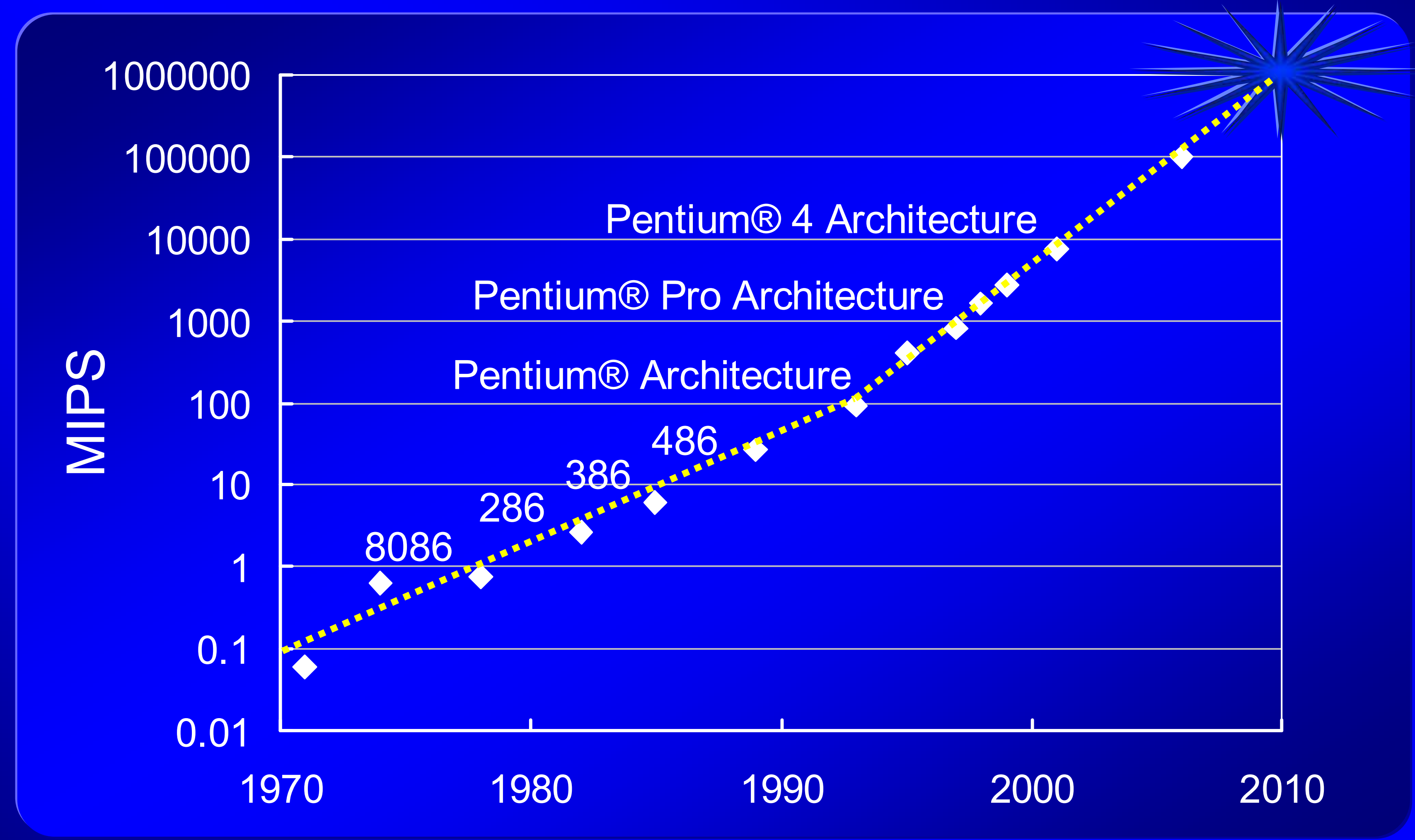
October, 2007

Packaging solutions to system performance growth

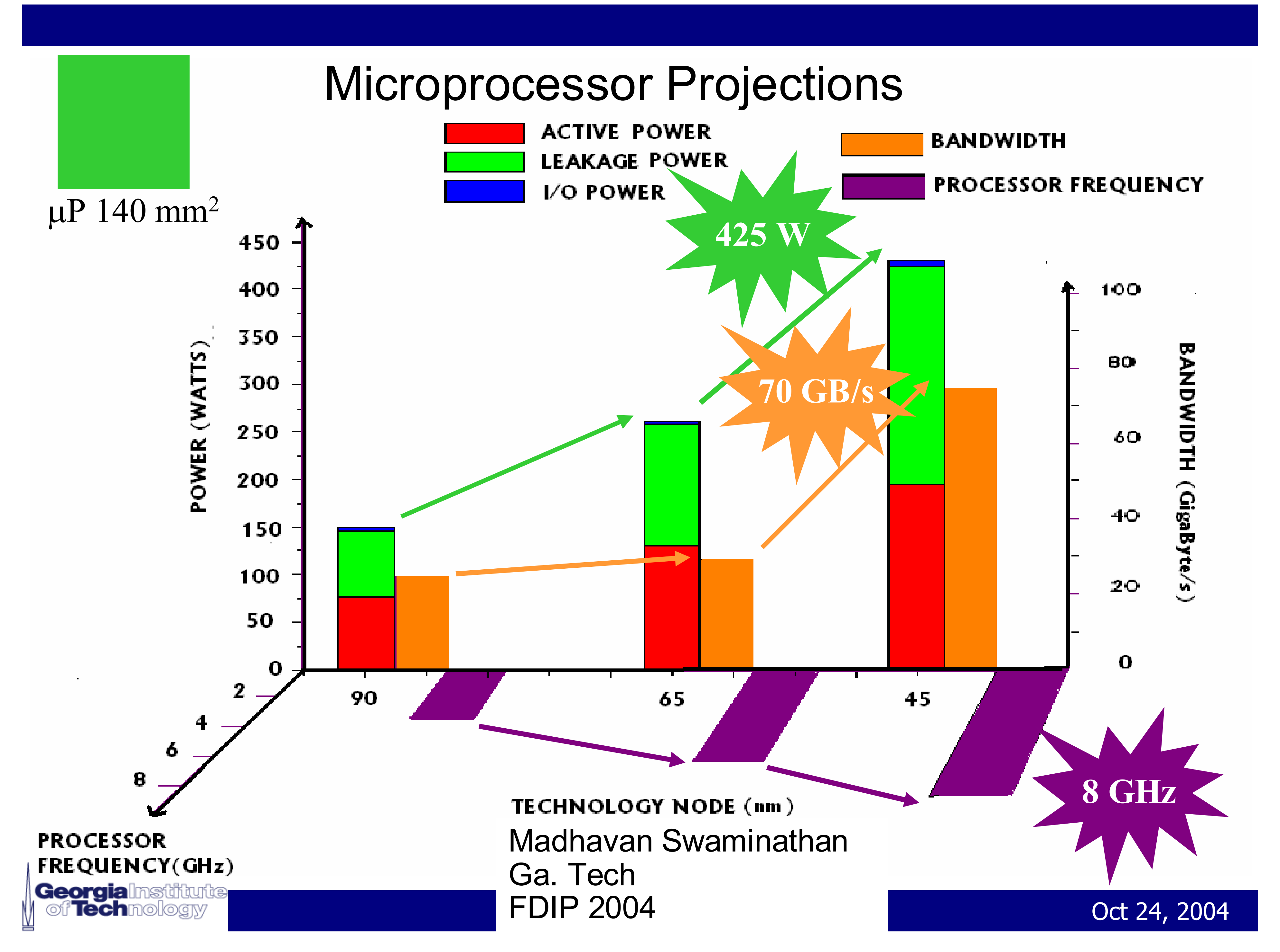
- **Industry targets through the eyes of the IEEE FDIP Workshop.**
  - Future Directions in IC and Package Design Workshop
- **Observations that impact server packaging technology**
- **System and package electrical design considerations**
- **What does this bandwidth cost?**

Goal: 1TIPS by 2010

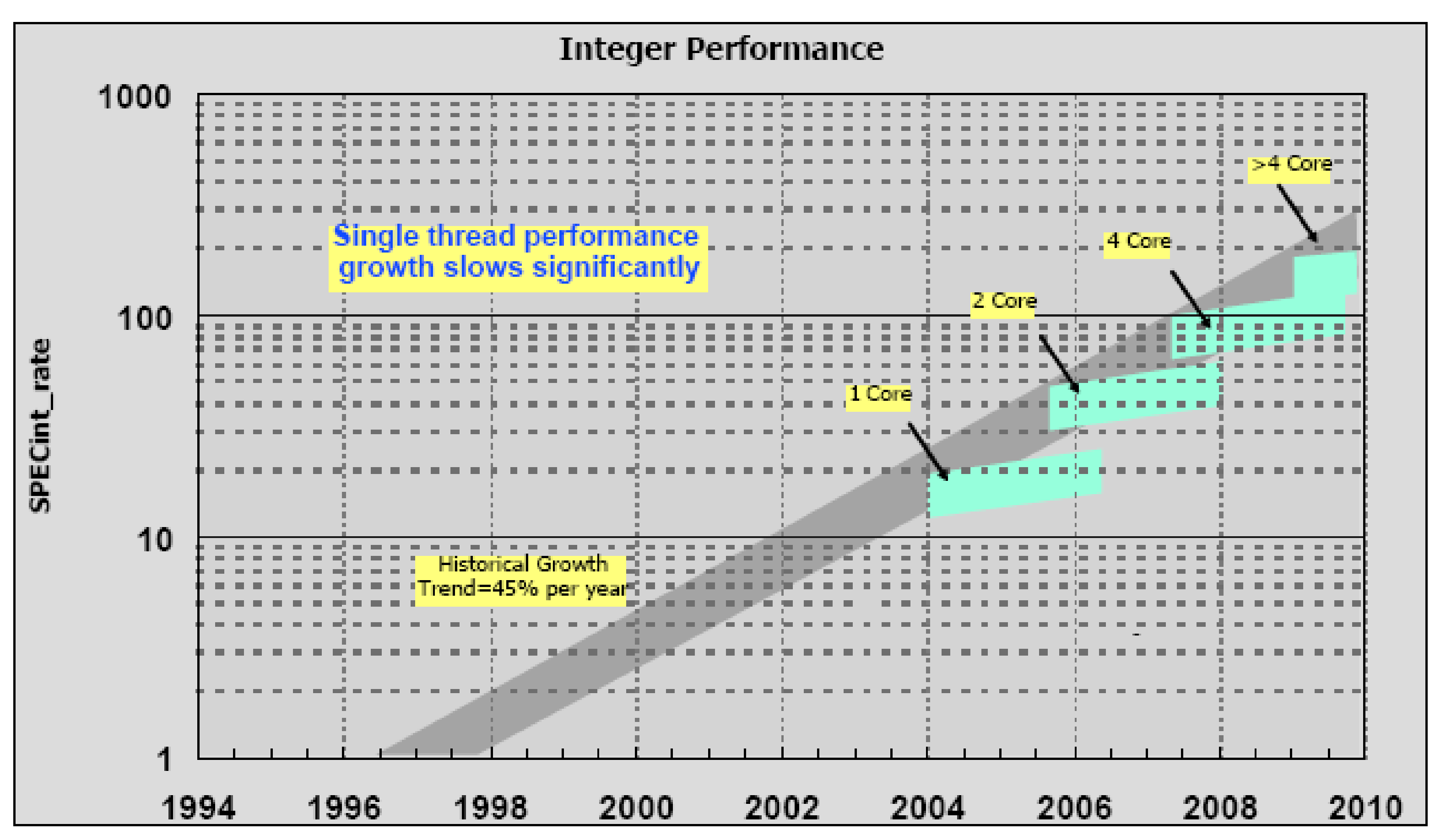


How do you get there?

Shekhar Borkar
Circuit Research, Intel Labs
FDIP … October 24, 2004


Microprocessor Projections
μP 140 mm2
ACTIVE POWER
LEAKAGE POWER
I/O POWER
BANDWIDTH
PROCESSOR FREQUENCY
425 W
70 GB/s
8 GHz
POWER (WATTS)
450
400
350
300
250
200
150
100
50
0
BANDWIDTH (GigaByte/s)
100
80
60
40
20
0
90
65
45
2
4
6
8
TECHNOLOGY NODE (nm)
PROCESSOR FREQUENCY(GHz)
Madhavan Swaminathan
Ga. Tech
FDIP 2004
Georgia Institute of Technology
Oct 24, 2004

Chip Performance Trends

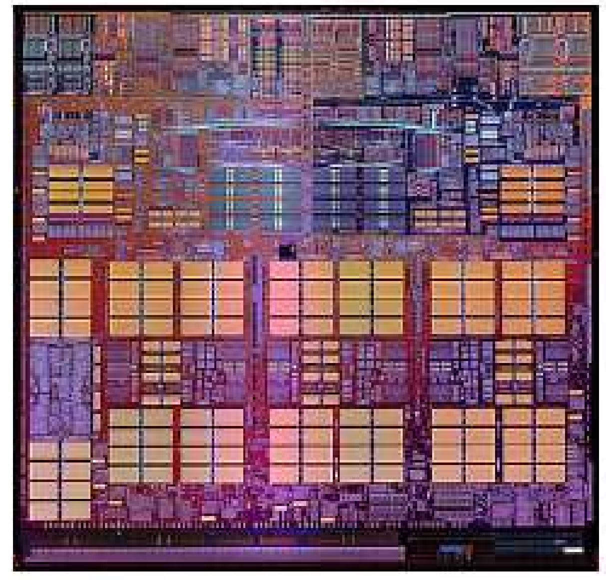


Carl Anderson
IBM
FDIP – Oct. 2005

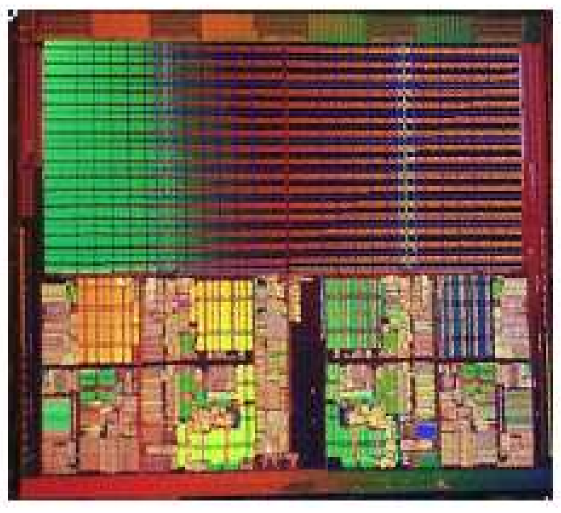
Carl Anderson
IBM

Multi Cores

- 2-4 Cores per Socket Available Now
  - 8+ Cores By 2010



Power 4
1st Dual Core 2001



Dual Core Opteron
1st Desktop Dual Core

Power 5
Quad Core per Socket

The CEC bandwidth component and requirements

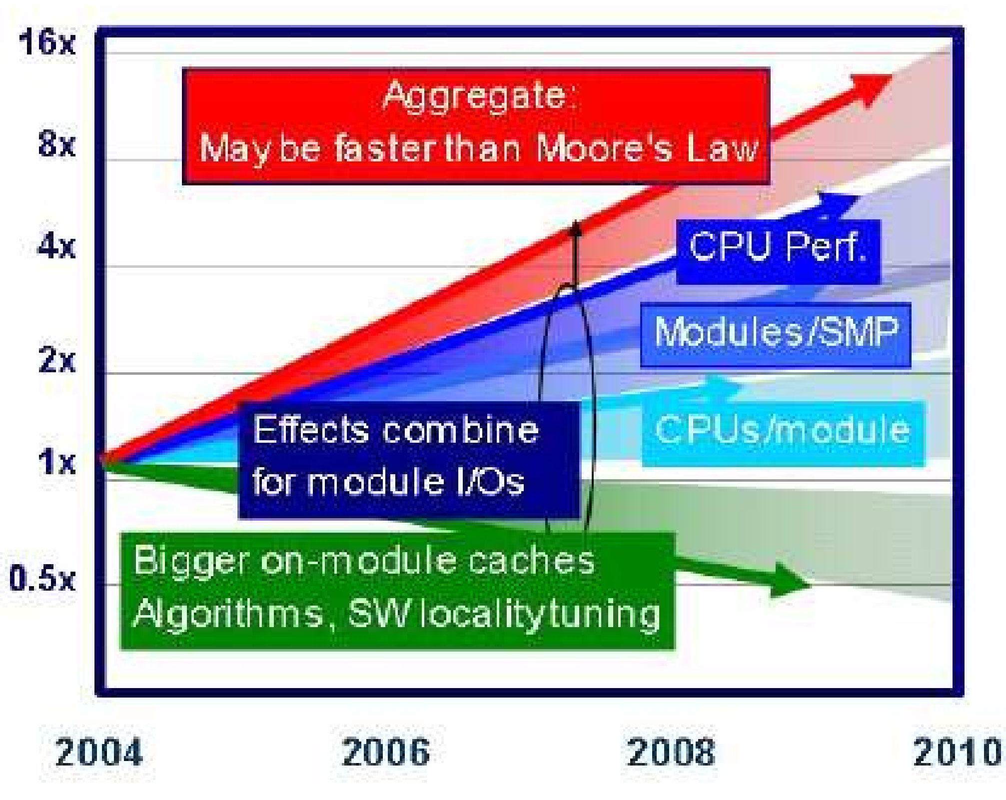


Figure 1: MCM signal I/O requirement trends

TWO ways to do it

More pins
and/or
higher frequency of interconnect

George Katopis
IBM
FDIP – Oct. 2005

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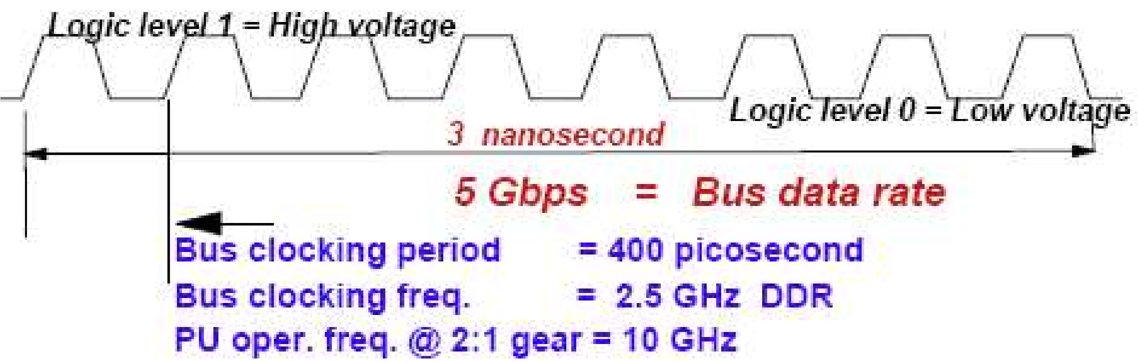
The EM modeling challenge



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Eq. PU Freq. of Oper.. GHz	Time	Data rate for 2:1 bus gear Single Ended	Data rate for 1:1 bus gear Differential	Bus freq. in GHz	Interc. Model freq. GHz
2	Now	1 Gbps	2 Gbps	0.5-1	5-10
5	Next Gen.	2.5 Gbps	5 Gbps	1.25-2.5	12.5-25
10	2010	5 Gbps	10 Gbps	2.5-5	25-50

The tools and verification measurements must be acurate for up to 50GHz in 2 years

G. A. Katopis © 2005 IBM Corporation

Personal View of Processor Designs

Voltage

5.00
4.75
4.50
4.25
4.00
3.75
3.50
3.25
3.00
2.75
2.50
2.25
2.00
1.75
1.50
1.25
1.00

150
140
130
120
110
100
90
80
70
60
50
40
30
20
10

84 86 87 88 90 91 93 94 95 97 98 99 01 02 04 05

Year

Inmos Transputer

Ultrasparc

Niagara

Chip Multithreading Effect

Voltage
Power

David Greenhill
Sun
FDIP – Oct. 2006

System Performance Stack

Customer Perceived System Performance $\approx \dfrac{(N \times Frequency)}{(CPI \times PathLength)}$

Application		
S/W Development Tools	Middleware	
	Operating System	Hypervisor
SMP System Structure Fabric, switches, busses, memory system, protocols, …		
Compilers		
Microprocessor Core Microacrchitecture, logic circuits, design methodology	Cache Cache levels, granularity, latency, throughput	Interconnect
		I/O
Package Buses, Memory Bandwidth, Memory Size & Latency, Cooling		
Semiconductors Device, process, interconnect		

Number of Computing Elements

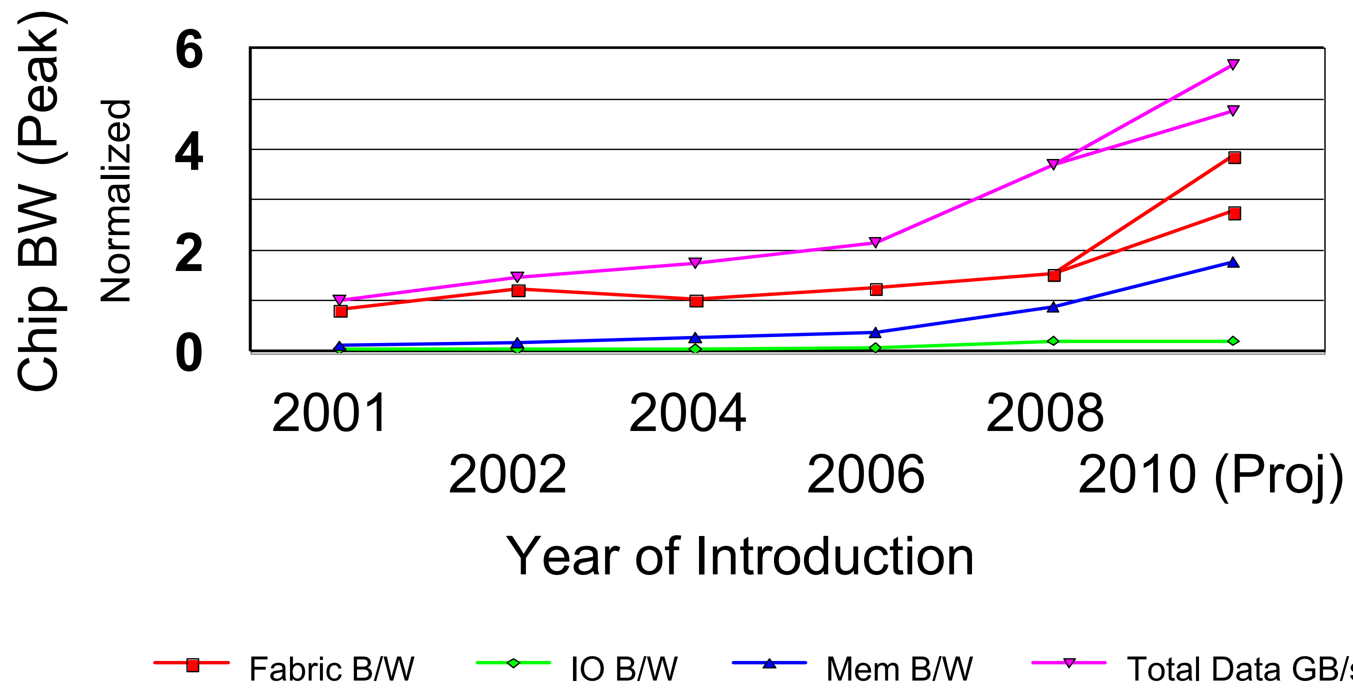
Pathlength

Cycles / Instruction

Frequency

Robert Guernsey
IBM
ESPW– Jan. 2007

"Peak bandwidth" – My experience



Trend of package I/O bandwidth density.

Architecture 1

GB/sec per cm^2

20
15
10
5
0

2003 2005 2008 2010 (proj)

System Year

Architecture 2

GB/sec per cm^2

20
15
10
5
0

2003 2004 2006 2008 2010 (proj)

System Year

Key Observations for Server Systems

- **System performance growth rate is maintained for the foreseeable future**
- **Innovative ways to maintain growth rate while minimizing growth in power and thermal**
- **Processor frequency growth rate is leveling off to help reduce power growth**
- **Off-processor signal frequency is increasing rapidly to maintain performance growth**
- **Memory bandwidth is a key part of maintaining performance.**
- **Also note that ASIC (Bridge chip) frequencies are increasing to keep up with off-chip bandwidth**

System Packaging Design Key Challenges

- **Manage Processor Power Growth**
  - Multiple voltage domains with similar voltage levels
    - Tune voltage levels to logic frequency sort points
    - Enable more aggressive power saving modes
  - Multiple cores
    - More cores per system
- **Enable High-Bandwidth Signaling**
  - High number of connections
  - Low-loss interconnections
  - Minimize jitter
    - Clocks, Switching Noise, Crosstalk, Reflections
- **Tends to lead to more on-chip integration of function**

Electrical Considerations

- **Low Loss Signal Traces**
  - Minimize stubs and boards with low resistance and low tan δ
- **Low Noise Interfaces**
  - Low crosstalk in connectors
- **Reference Current Returns**
  - Splits induced by connector vias
- **Power Distribution**
  - DC analysis becomes more system level
    - Number of chip pins impacted by electromigration limits
    - Number of package pins impacted by thermal limits
  - Decoupling is challenged by multiple voltage domains

SI - A historical perspective

Year	Bit Rate	Evolving Constraints	Evolving Design Verification at tape-out
1996	0.166 Gb/s	Bound Timing Limits AC Noise Budget	Spreadsheet timing SSN determine VDDmin
1998	0.250 Gb/s	ISI In Noise Budget	Multi-pkg level Crosstalk Core Noise included in SSN
2000	0.450 Gb/s	Clock-Data Timing	Noise feedback to timing Spatial Vdd variance spec'ed
2003	0.650 Gb/s	Freq. Dependent Loss	Fast simulation of each Net IR Analysis Required
2005	1.9 Gb/s on-MCM	Transmitter Equalization	Timing and Noise Combined SSN induced jitter
2007	2.5 Gb/s off-MCM	Tx and Rx Equalization	Scattering Parameters/BER Statistical Random Jitter
2010	6.4-10 Gb/s Differential	Include Physical Layer	Channel Analysis Full System Considerations

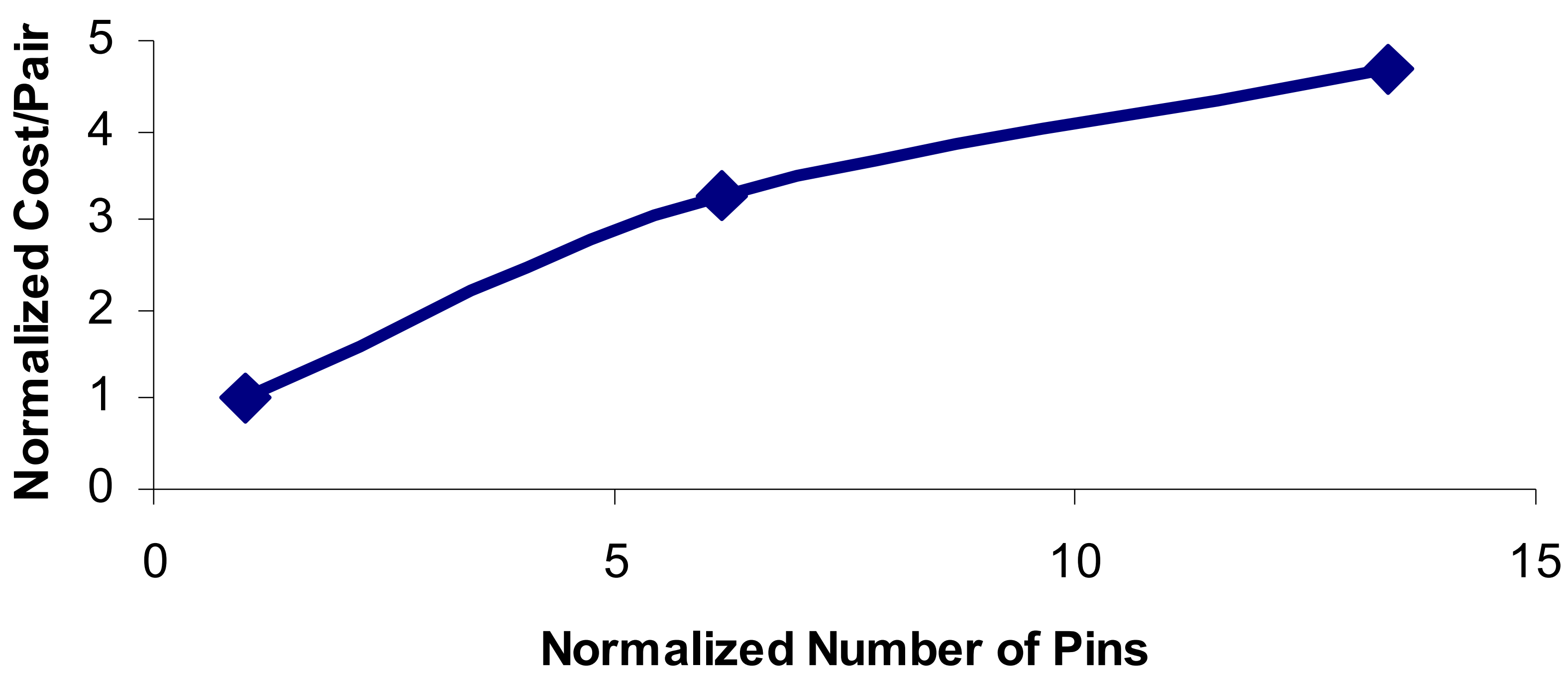
What does this mean for electrical design tools?

- **Extraction – 3D Full-wave tools**
  - High-frequency operation
  - Fully 3D effects of via stubs and discontinuous return paths
    - The discontinuous return paths are a big challenge
- **Power Distribution Analysis**
  - Electromigration limits
  - Impact of switching noise on signal interfaces
- **Signal Distribution Analysis**
  - Frequency-Domain Analysis
  - Consortium defined interfaces and meeting compliance
- **Increasing use of commercial tools**
  - Tools are maturing
  - Standardize design process when sharing design work among design teams
  - Manage tool development cost

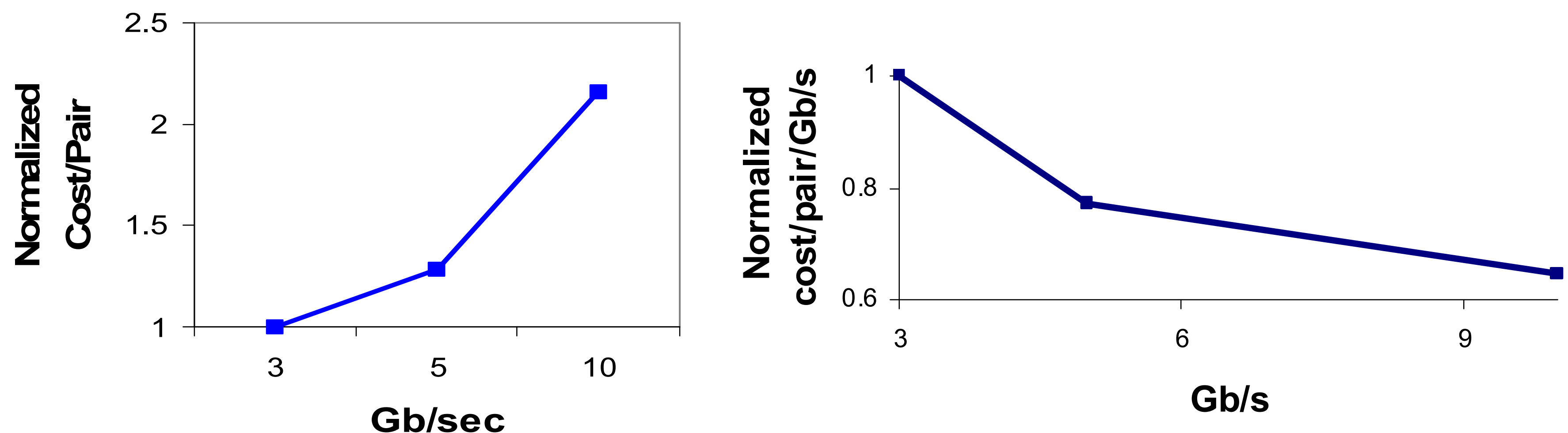
Bandwidth Cost Pressures

- **Need to either increase number of pins or frequency to meet bandwidth growth**
- **Frequency increase requires more expensive technology**
  - High Frequency Connectors
  - Removing Via Stubs
  - Low Loss Laminates
- **More pins … cost is not linearly proportional to number**
  - More expensive connectors
  - More card real estate for wiring and connector
  - More card area is committed to provide proper plane and via signal shielding.

The cost of dense interconnection – Server comparisons



Cost Requirements for high-performance
Assuming maintaining the same system structure



My Assumptions assuming high number of pins, 1 meter connection, 2 connectors

3 Gb/s … 1x PCB, 1x connector cost

5 Gb/s … 1.4x PCB, 2x connector cost

10 Gb/s … 3x PCB, 4x connector cost

Higher frequencies create significant design and characterization effort.

Higher frequencies also significantly increase chip area and power for I/O circuits.

Conclusions

- **Multi-core sockets are needed to maintain performance growth.**
  - Meet 2010 targets for system performance
- **This trend stresses packaging**
  - Packaging larger chips or multiple processor chips in a socket.
  - More cores demand more signal bandwidth, memory bandwidth
- **Electrical package design needs development**
  - Power distribution network impact on signal distribution
  - Chip – Package co-design … system level design tools
  - Cost optimization to meet competitive pressures