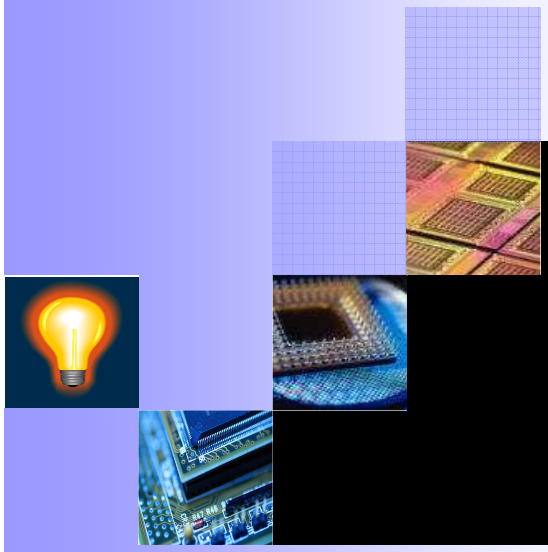

# *Power Delivery System Design Challenges and Explorations on How to Overcome Them*

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# Overview

- The importance of power integrity has been recognized for well over a decade
- Power delivery system (PDS) has been a hot topic ever since the first EPEP in 1992
- A number of commercial tools for PDS analysis and simulation have been developed and brought to market since late 1990s by several software vendors
- More than 100 companies worldwide have acquired commercial software tools for PDS design and analysis

## Questions:

- **What are the main remaining design challenges for PDN?**
- **Are software tools adequate to help engineers overcome such challenges?**

# Observation

- A very small number of companies are able to put a large amount of dedicated resources to do extensive pre- and post-layout design and analysis using software tools for power delivery systems
- Many companies use software tools to do power analysis only when they encounter problems or suspect to have problems related to PDS
- Most of the companies use *trial-and-error* instead of software tools in placing decoupling capacitors on the board. Such practice often leads to many iterations or grossly over designs.

# What Seems Lacking in PDS Designs

- Design specifications
  - Quite often there is no PDS design specifications, or
  - The design specifications are not specific enough
- Effective design flow to meet design specifications
  - No streamlined procedure to implement, optimize, and sign-off PDS designs

# What Are the Proper Design Specifications for PDS

- Voltage noise magnitude in terms of mV?
  - Under what stimulus or stimuli?

    Can chip vendors provide them?

    Can system people measure and extract them?

- Power-ground impedance Z(f) over a certain range of frequency?
  - How to determine them?
  - Who provide them?  By chip vendors?
  - How can system people measure and extract them?

# What Are the Proper Design Specifications for PDS (Cont.)

- Power-ground loop inductance L (particularly for packages)?
  - How to determine them?
  - Who determine them?  By chip vendors?
  - Can package designer extract them?

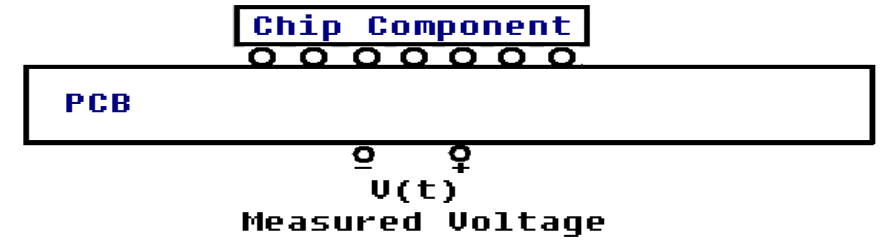
- In terms of signal quality?
  - Jitter?
  - Eye-diagram characteristics?

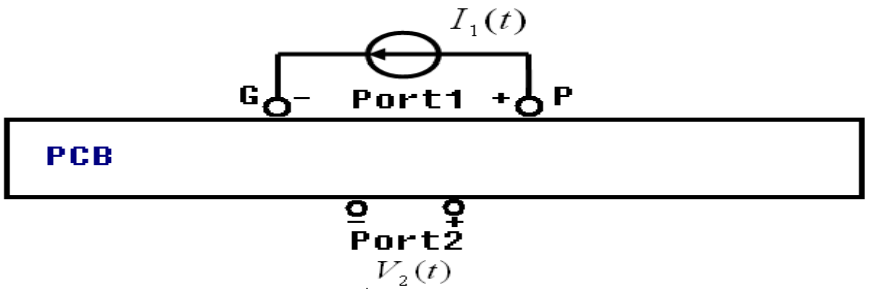
# Who and How to Determine PDS Design Specifications

- By chip vendors with EDA tools
  - Chip vendors use EDA tools to generate chip power models with time-domain stimuli as well as the requirement of maximum magnitude of power net voltage noise
  - Chip vendors use EDA tools to obtain the PDS impedance profiles Z(f) of packages and reference boards, and provide the PDS impedance profiles as design specifications for board and package designers.

# Who and How to Determine PDS Design Specifications (Cont.)

- Extract chip current by measurement
  - Measure the voltage noise waveform and extract chip current waveform




$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 = 0 \end{bmatrix}$$

$$V_2 = Z_{21} I_1, \text{ Or}$$

$$I_1 = V_2 / Z_{21}$$

## Who and How to Determine PDS Design Specifications (Cont.)

- Build PDS characteristics and performance database library by board and package vendors

  The database includes the PDS performances of the components successfully used in previous applications

  - **Computed PDS impedance profiles (or effective power-ground loop inductances)**
  - **Any lab assessment on actual PDS performance in system operation**
  - **Required (or recommended) design specifications (e.g., impedance profiles) of the components for similar application**

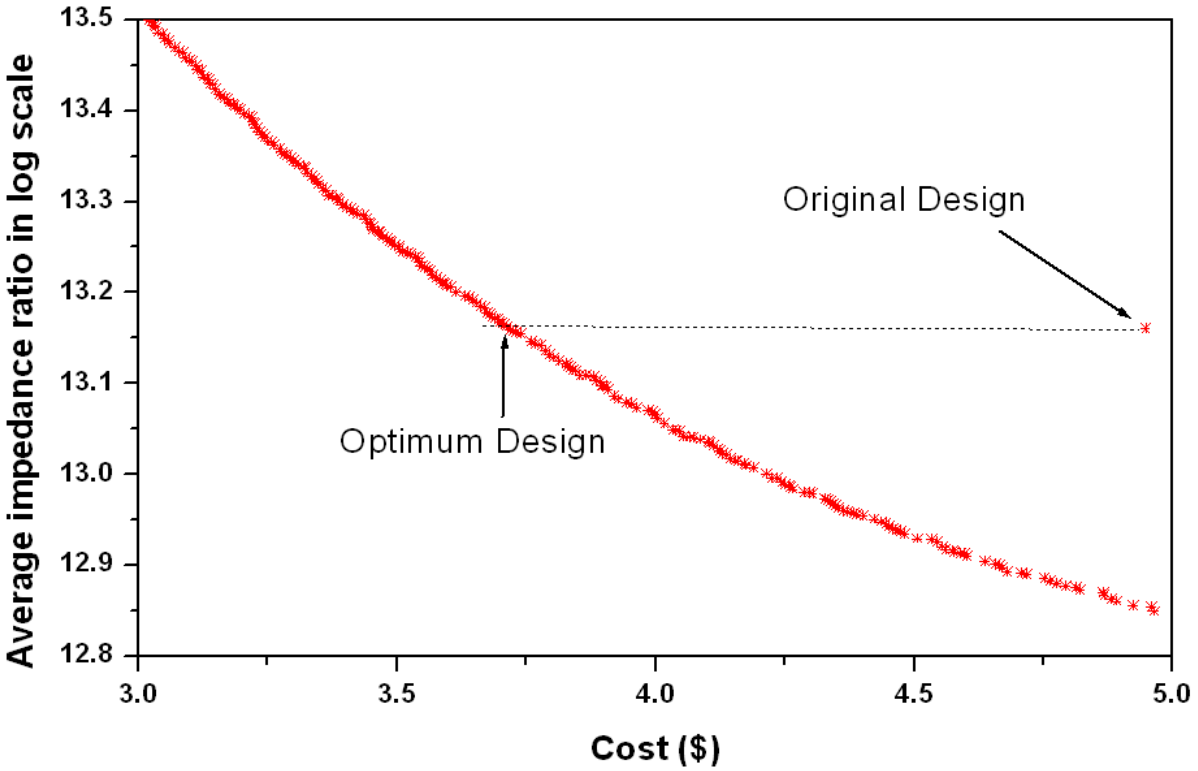
## Who and How to Determine PDS Design Specifications (Cont.)

- Benefits of the database library
  - Important reference on the characteristics and actual performance of PDS in previous products
  - Generate PDS design specifications for the components to be used in new systems for similar applications
  - Help to generate PDS design specifications (through certain extrapolation) for the components to be used in new systems for different applications
  - Help to generate PDS design specifications (through certain extrapolation) for new components

# Decoupling Capacitor Placement and Selection

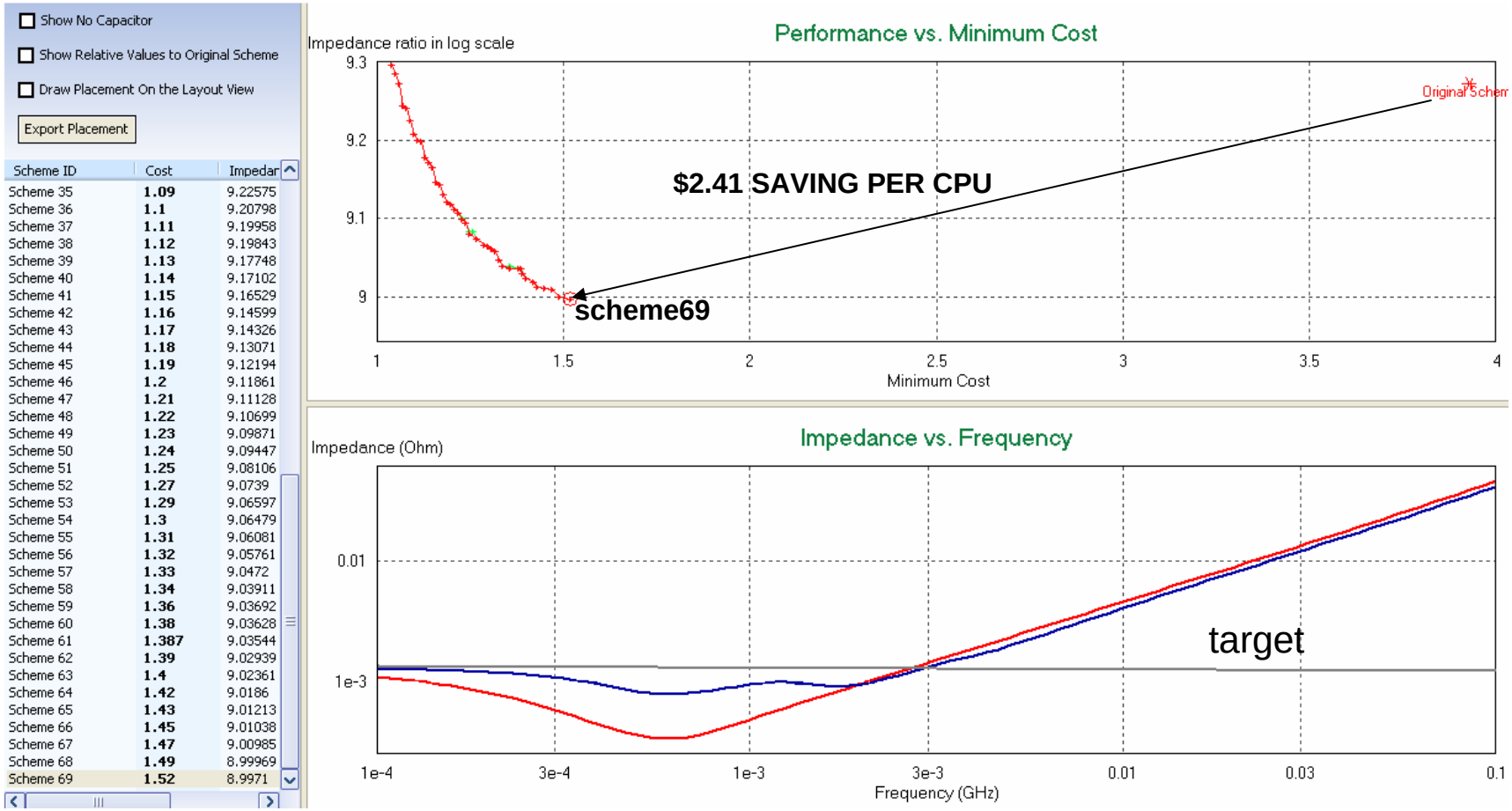
- With a given target PDS performance (or design specification), there are numerous options in the selection of decoupling capacitors
  - Where to put
  - How many needed
  - Which capacitor to choose from at each location
  - What are the cost constrains
  - What are the space constrains
  - What are the impacts if certain capacitors do not function

# Case Study – Cost reduced by more than 25% without sacrificing performance



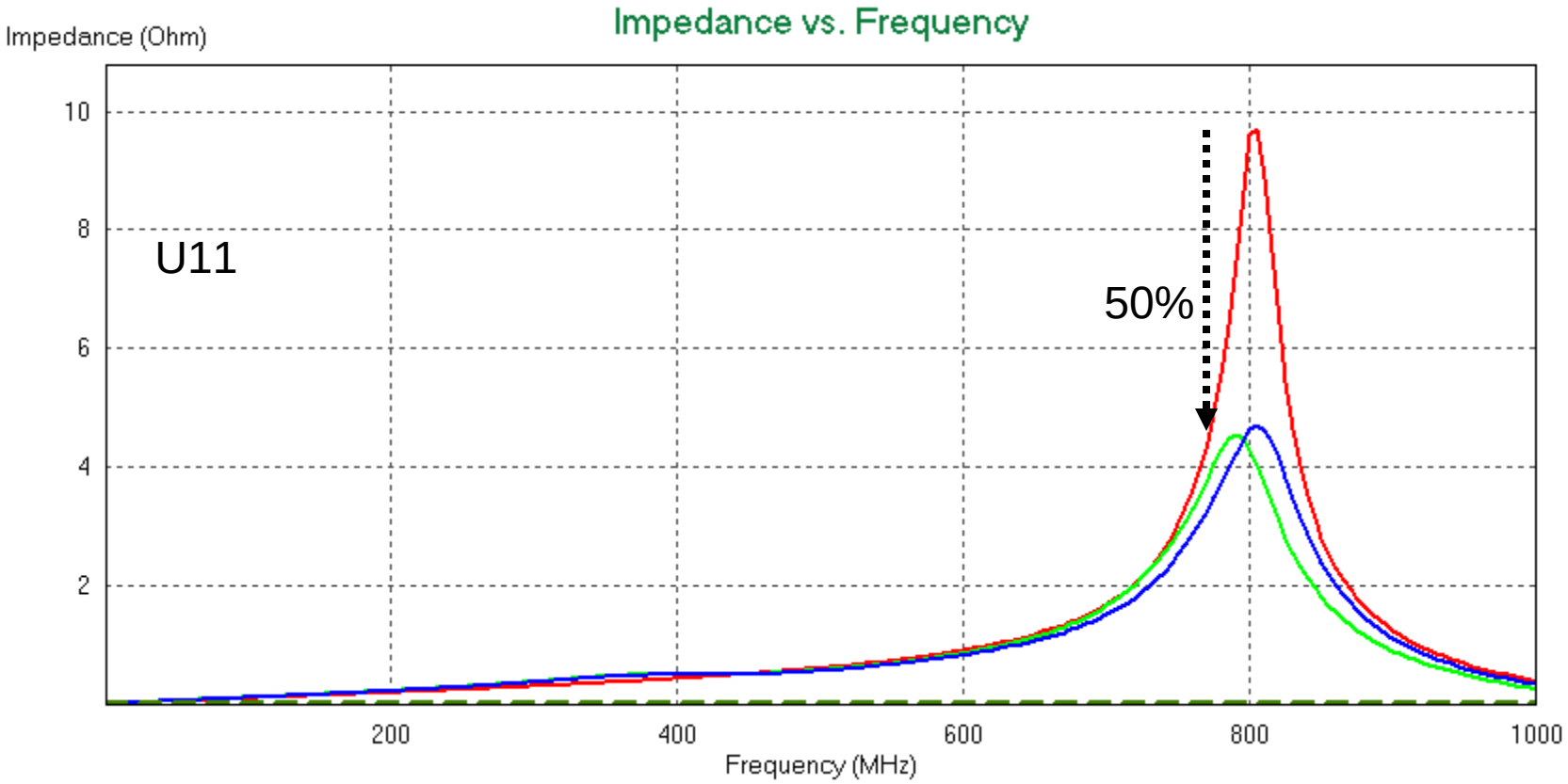

| | Average impedance ratio | Cost($) |
|---|---|---|
| Original design | 13.1600 | 4.95 |
| Optimum design | 13.1594 | 3.72 |

# Case Study - Eliminate over design and get $4.82 cost saving on a two CPU motherboard



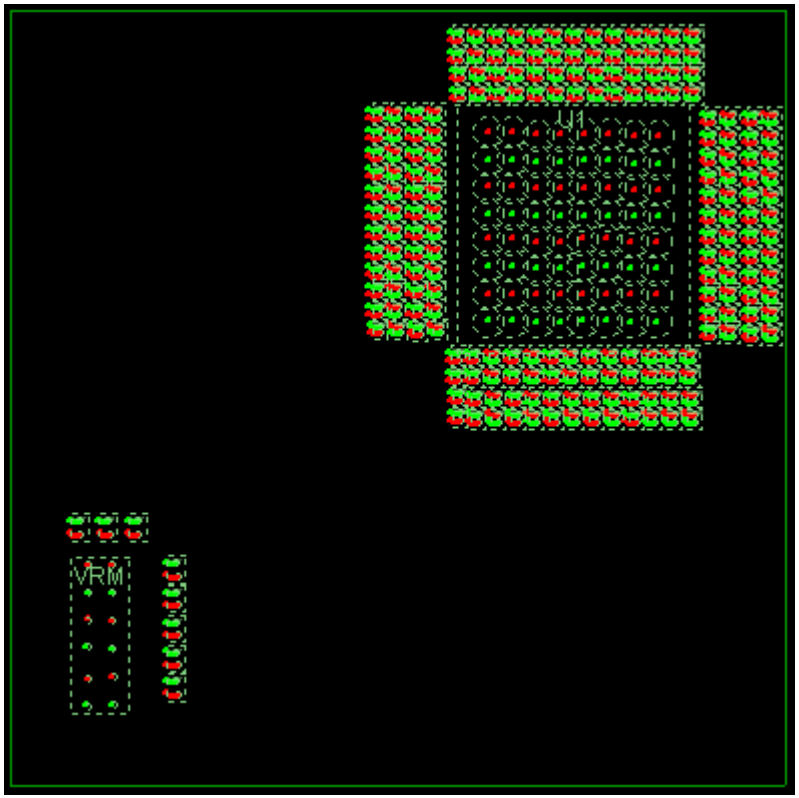

**Red: original design** **Blue: scheme 69**

# Case Study - Resonant peak is reduced by 50% while saving 6-15cents




Original Scheme29(15cents saving) Scheme45(6cents saving)

# Case Study – PDS Optimization in Pre-Layout Design

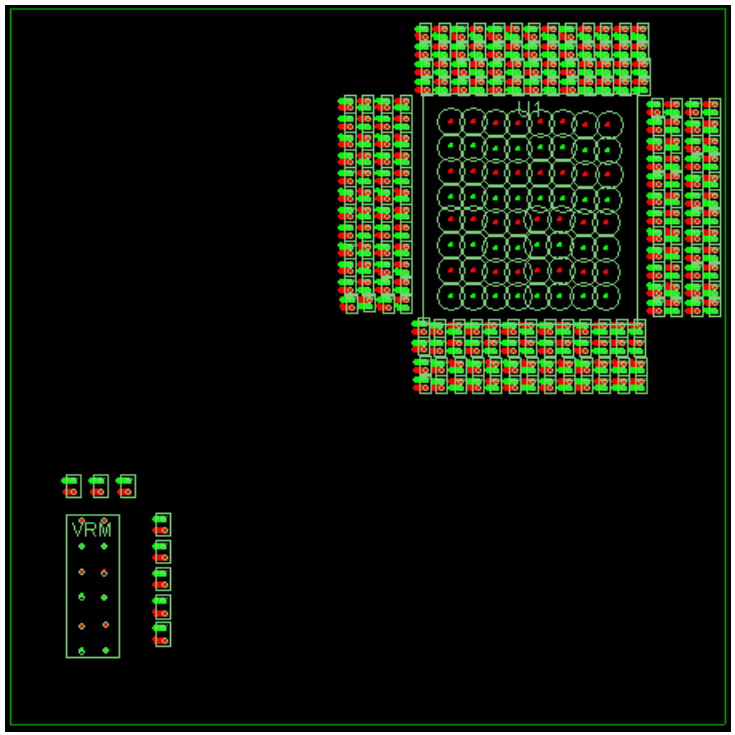


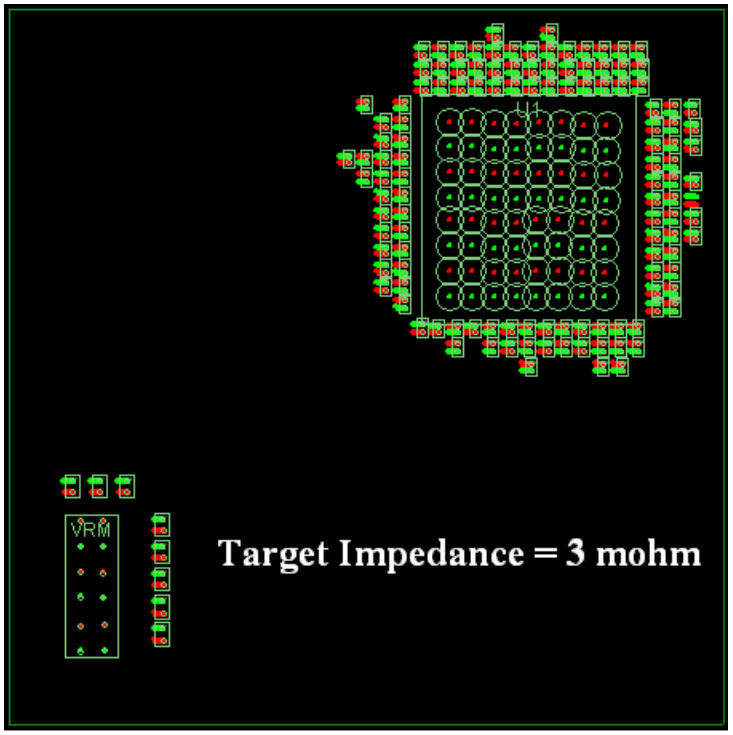

200 possible locations of decaps for U1

8 decaps for VRM (won't be included in Optimization)

Use 1uF for all 200 decaps and 330uF for VRM decaps for original decap setup (users can use any decap values as they wish)

# Before and After Decap Optimization




Before

- **200 x 1uF**

After

- **38x100nF**
- **32x470nF**
- **13x4.7uF**
- **40x1.0uF**

**Total decaps = 123**

# Identify Effective/Ineffective Decap Locations

| Scheme ID | Cost | Impedance ra | C1 | C7 | C12 | C14 | C18 | C19 | C25 | C29 | C34 | C37 | C42 | C44 | C47 | C50 | C54 | C56 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Scheme 1 | 0.17671 | 17.6124 | 9 | X | X | X | 6 | X | 5 | X | 5 | 5 | X | X | X | X | X | 7 |
| Scheme 2 | 0.17695 | 17.479 | 6 | X | X | X | 6 | 6 | 5 | X | 5 | 5 | 5 | X | X | X | X | X |
| Scheme 3 | 0.17813 | 17.4786 | 6 | X | X | X | 6 | X | 6 | X | 5 | 5 | 6 | X | X | X | X | 7 |
| Scheme 4 | 0.1833 | 17.4781 | 5 | X | X | X | 6 | X | 6 | X | 5 | 5 | 5 | X | X | X | X | 14 |
| Scheme 5 | 0.18448 | 17.4351 | 6 | X | X | X | 6 | X | 6 | X | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 6 | 0.18965 | 17.4201 | 5 | X | X | X | 5 | X | 6 | 5 | 5 | 5 | 5 | X | X | X | X | X |
| Scheme 7 | 0.19083 | 17.3998 | 6 | X | X | X | 6 | X | 5 | X | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 8 | 0.196 | 17.3901 | 5 | X | X | X | 5 | 5 | 5 | X | 5 | 5 | 5 | X | X | X | X | X |
| Scheme 9 | 0.19718 | 17.3712 | 5 | X | X | X | 5 | X | 6 | X | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 10 | 0.20353 | 17.3475 | 5 | X | X | X | 5 | X | 5 | X | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 11 | 0.20613 | 17.3408 | 6 | X | X | X | 6 | X | 6 | X | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 12 | 0.2113 | 17.3293 | 5 | X | X | X | 5 | X | 6 | 5 | 5 | 5 | 5 | X | 6 | X | X | X |
| Scheme 13 | 0.21248 | 17.3097 | 5 | X | X | X | 6 | X | 6 | 6 | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 14 | 0.21765 | 17.3008 | 5 | X | X | X | 5 | 5 | 5 | 6 | 5 | 5 | 5 | X | X | X | X | X |
| Scheme 15 | 0.21883 | 17.2806 | 5 | X | X | X | 5 | X | 6 | 6 | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 16 | 0.224 | 17.2805 | 5 | X | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | X | X | X | X |
| Scheme 17 | 0.22518 | 17.2584 | 5 | X | X | X | 5 | X | 6 | 5 | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 18 | 0.22778 | 17.2518 | 6 | X | X | X | 6 | 6 | 6 | X | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 19 | 0.23153 | 17.2421 | 5 | X | X | X | 5 | X | 5 | 5 | 5 | 5 | 5 | X | X | X | X | 7 |
| Scheme 20 | 0.23295 | 17.2387 | 6 | X | X | X | 5 | 6 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | X |
| Scheme 21 | 0.23413 | 17.2156 | 6 | X | X | X | 6 | 6 | 5 | X | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 22 | 0.2393 | 17.2097 | 6 | X | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | X |
| Scheme 23 | 0.24048 | 17.1883 | 6 | X | X | X | 5 | X | 5 | 6 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 24 | 0.24683 | 17.168 | 5 | X | X | X | 5 | X | 6 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 25 | 0.24943 | 17.1645 | 6 | X | X | X | 6 | 6 | 6 | 6 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 26 | 0.25318 | 17.1552 | 5 | X | X | X | 5 | 5 | 5 | X | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 27 | 0.25578 | 17.1287 | 6 | X | X | X | 6 | 6 | 5 | 6 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 28 | 0.26213 | 17.1067 | 6 | X | X | X | 5 | 6 | 5 | 6 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 29 | 0.26848 | 17.0845 | 6 | X | X | X | 5 | 6 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 30 | 0.27483 | 17.0652 | 6 | X | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 31 | 0.27743 | 17.063 | 6 | 6 | X | X | 6 | 6 | 6 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 32 | 0.28118 | 17.0526 | 5 | X | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 33 | 0.28352 | 17.0526 | 4 | X | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 34 | 0.28378 | 17.039 | 6 | 6 | X | X | 5 | 6 | 5 | 6 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 35 | 0.29013 | 17.018 | 6 | 6 | X | X | 5 | 6 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 36 | 0.29648 | 16.9986 | 6 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 37 | 0.30283 | 16.9877 | 5 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | X | X | 7 |
| Scheme 38 | 0.30543 | 16.9857 | 6 | 6 | X | X | 6 | 5 | 5 | 6 | 5 | 5 | 5 | X | 6 | 6 | X | 7 |
| Scheme 39 | 0.30918 | 16.9816 | 5 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 5 | X | X | 7 |
| Scheme 40 | 0.31178 | 16.9642 | 6 | 6 | X | X | 6 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | 6 | X | 7 |
| Scheme 41 | 0.31813 | 16.9434 | 6 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | 6 | X | 7 |
| Scheme 42 | 0.32448 | 16.9338 | 5 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | 6 | X | 7 |
| Scheme 43 | 0.33083 | 16.9295 | 5 | 5 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 6 | 6 | X | 7 |
| Scheme 44 | 0.33718 | 16.9231 | 5 | 5 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | X | 5 | 6 | X | 7 |
| Scheme 45 | 0.33978 | 16.9123 | 6 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 6 | 6 | 6 | X | 7 |
| Scheme 46 | 0.34613 | 16.9026 | 5 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 6 | 6 | 6 | X | 7 |
| Scheme 47 | 0.35248 | 16.8909 | 5 | 6 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 6 | 6 | X | 7 |
| Scheme 48 | 0.36117 | 16.8882 | 5 | 4 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 6 | 6 | X | 7 |
| Scheme 49 | 0.36752 | 16.8865 | 5 | 5 | X | X | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 4 | 5 | 6 | X | 7 |

X = not populated

# Summary

- It is essential to establish design specifications for power delivery systems
- It is very important to establish a streamlined process for power delivery system design in the overall system design flow
- Optimization can play a very important role in the implementation of power delivery systems to achieve better performance, lower cost, smaller area, and shorter time-to-market

# Thank You!