Wireless Proximity Communications for 3D System Integration

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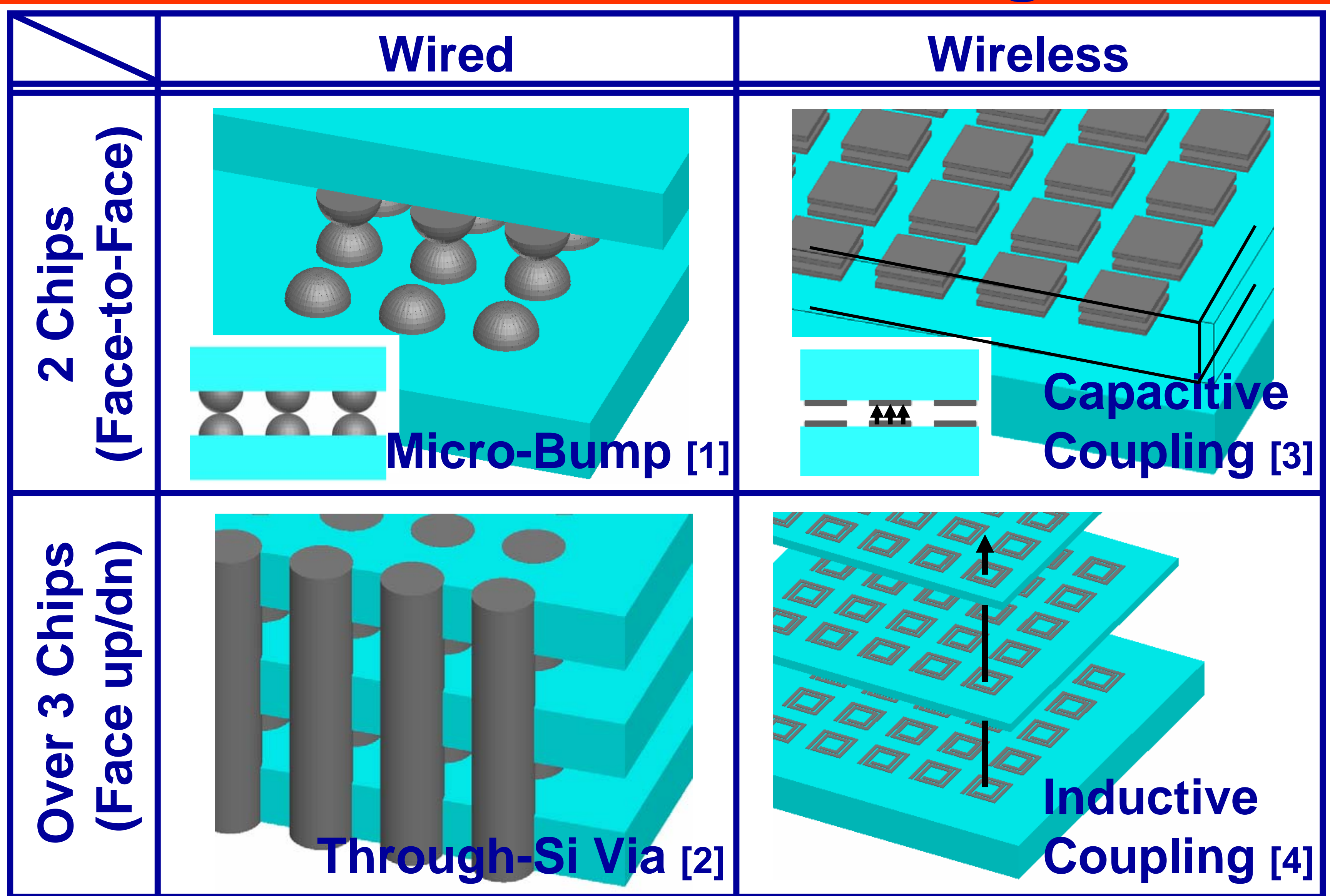
Area Interface for 3D Integration

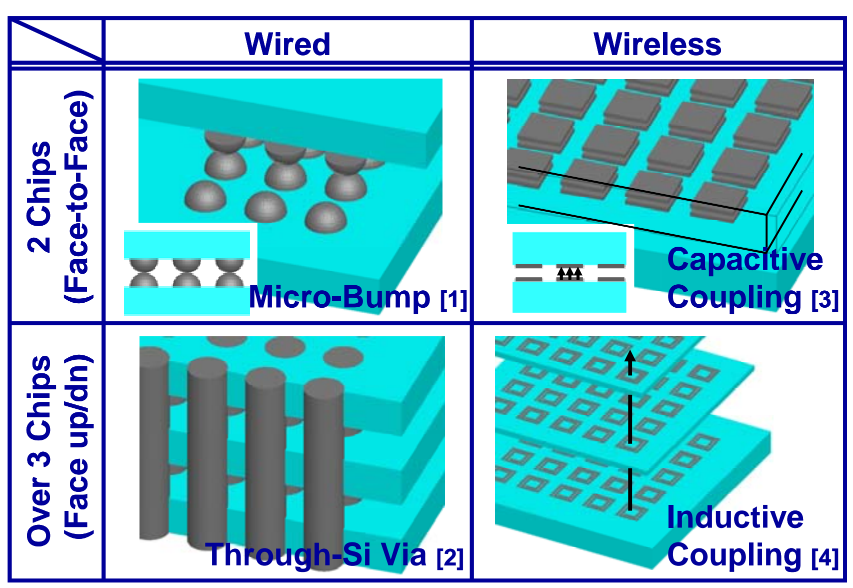


[1] ISSCC'04, Sony [2] ISSCC'01, MIT [3] ISSCC'03, Univ. Tokyo, Keio Univ. [4] ISSCC'04, Keio Univ.

Outline

Inductive and Capacitive Coupling Link for 3D System Integration

- Inductive vs. Capacitive
- Inductive vs. TSV, μ-bump
- 3D Scaling Scenario



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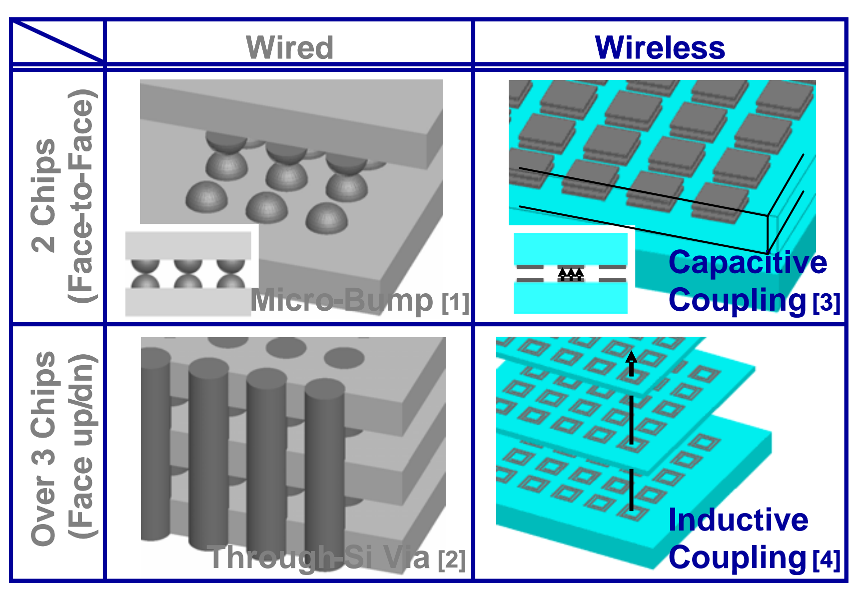
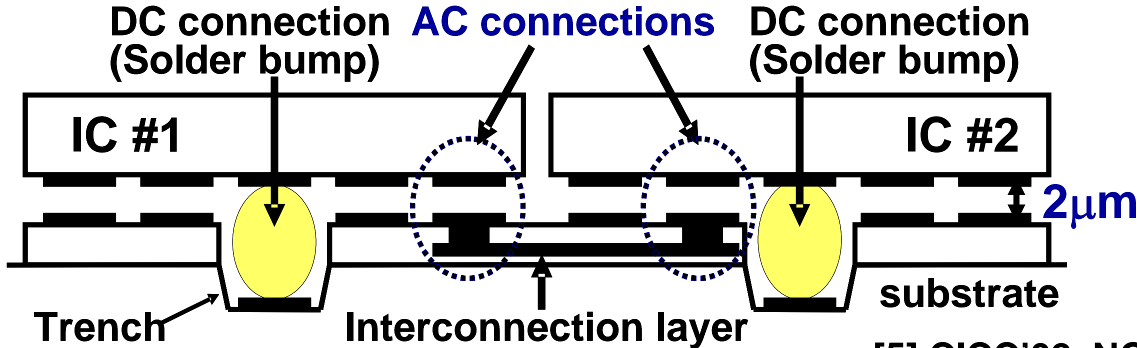


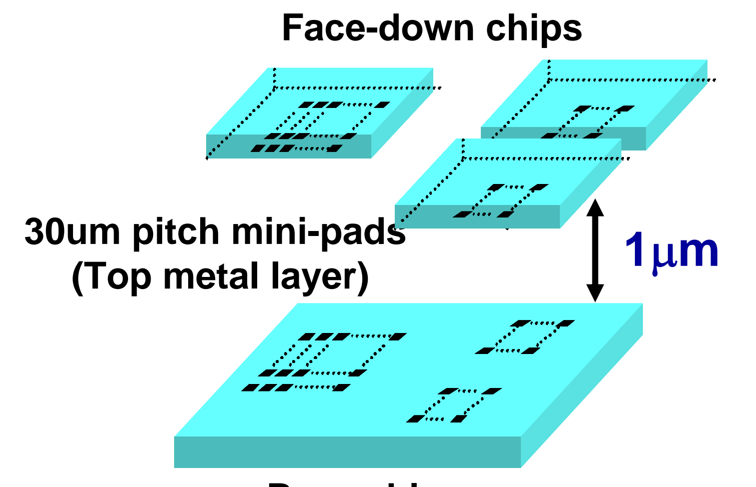
Capacitive-Coupling Link

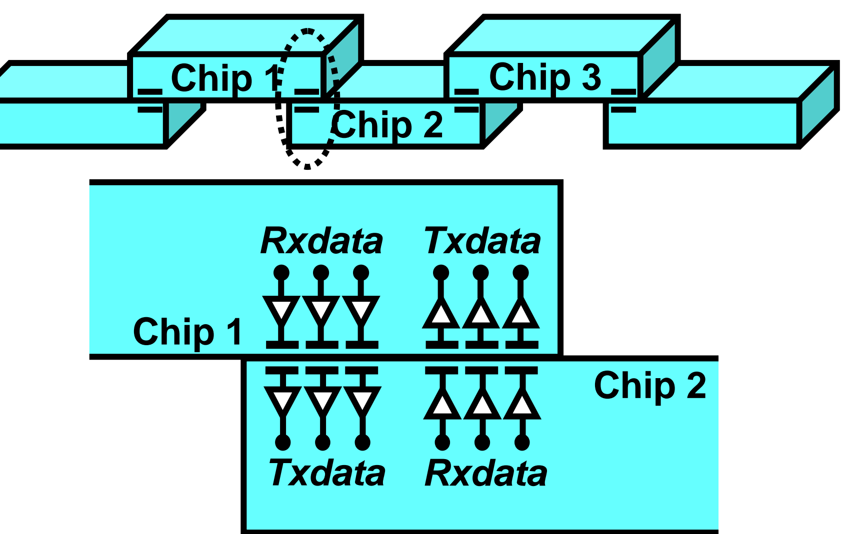
■ Chip to Interposer



[5] CICC'02, NC State Univ.
[6] ISSCC'05, NC State Univ.

■ Chip to Chip

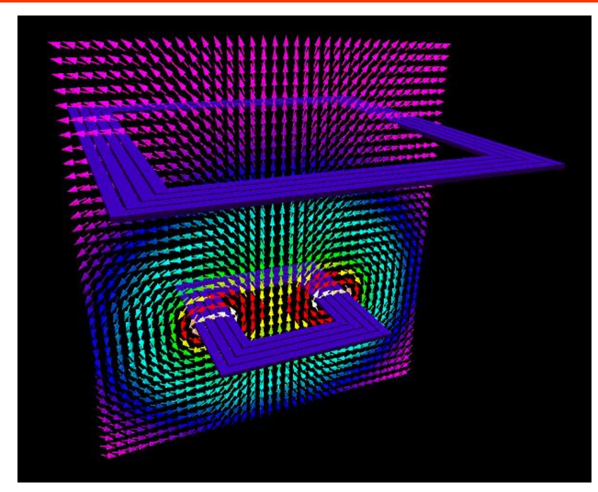




[3] ISSCC'03, Univ. Tokyo and Keio Univ.
[7] CICC'05, Univ. Bologna
[21] ISSCC'07, Univ. Bologna

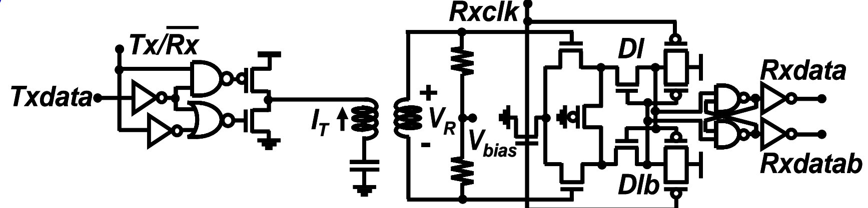
[8] CICC'03, Sun Microsystems
[9] ISSCC'04, Sun Microsystems
[22] ISSCC'07, Sun Microsystems

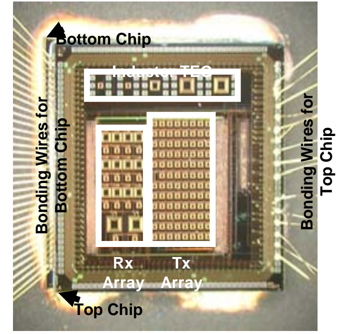
Inductive-Coupling Link



Multi-layer Wires

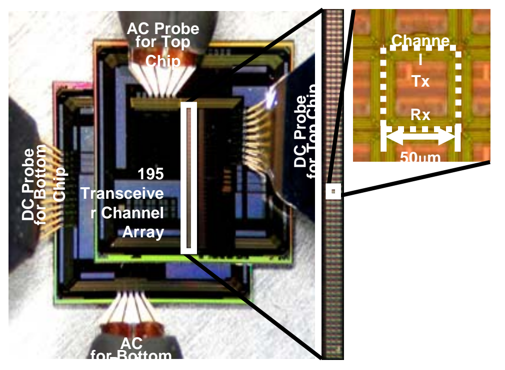
Digital CMOS Circuits





(1Gb/s)

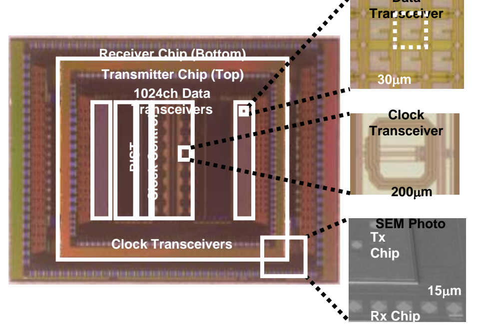
ISSCC 2004
[4] Keio Univ.



(200Gb/s)

ISSCC 2005
[10] Keio Univ.
[11] Hiroshima Univ.

VLSI 2005
[12] Hiroshima Univ.
[13] NC State Univ.



(1Tb/s)

ISSCC 2006
[14] Keio Univ.

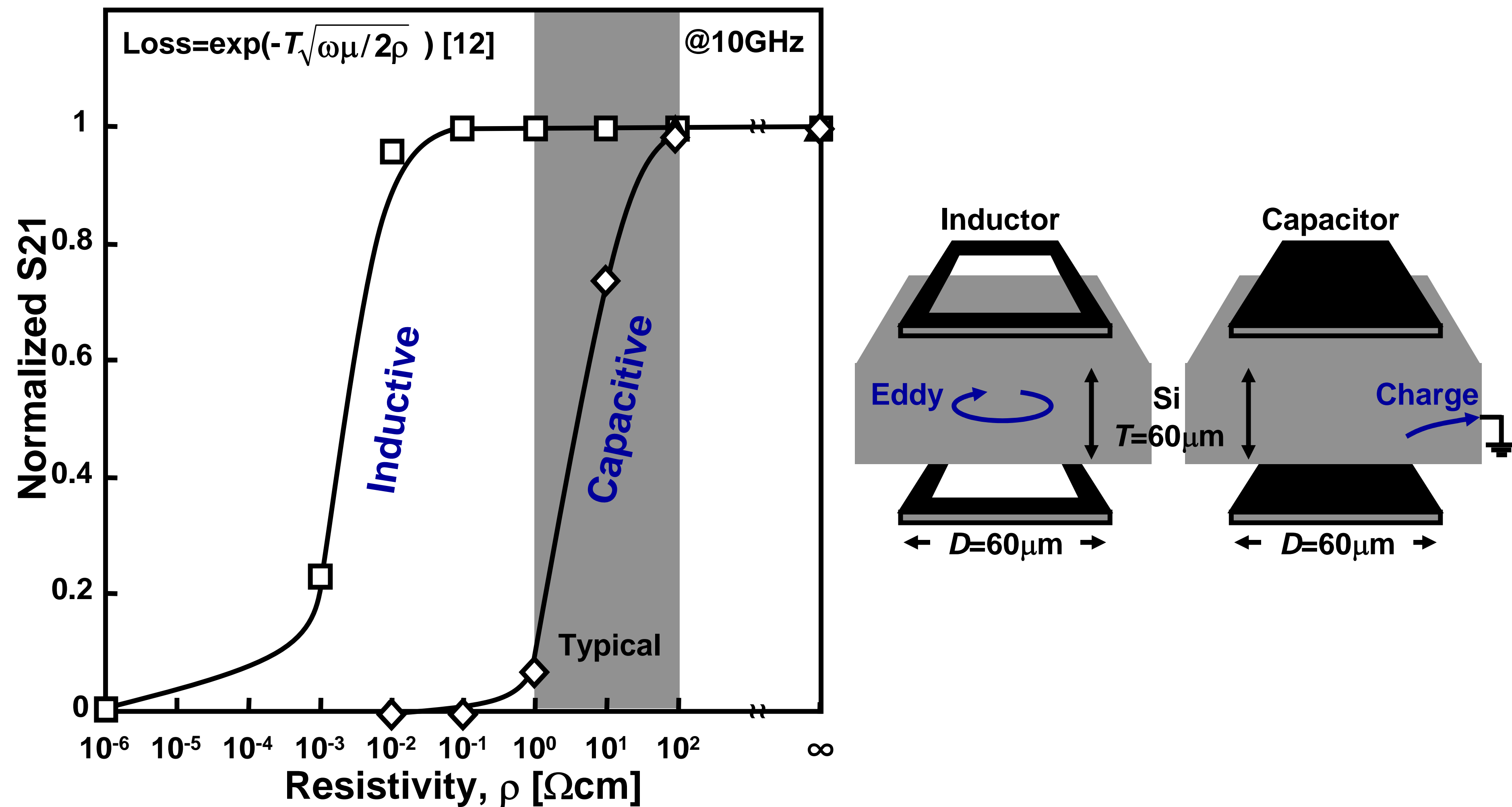
VLSI 2006
[15] Keio Univ.

Tx Chip (10μm-Thick)
Metal Inductor
P=30μm
3x3 Channel Array
Rx Chip (750μm-Thick)

(0.14pJ/b)

ISSCC 2007
[23] Keio Univ.
[24] Keio Univ.

Inductive vs. Capacitive: Loss by Body



- Capacitive: only for 2 chips, placed face-to-face
- Inductive: for 2 chips (face-to-face) and ≥3 chips (face up/down)

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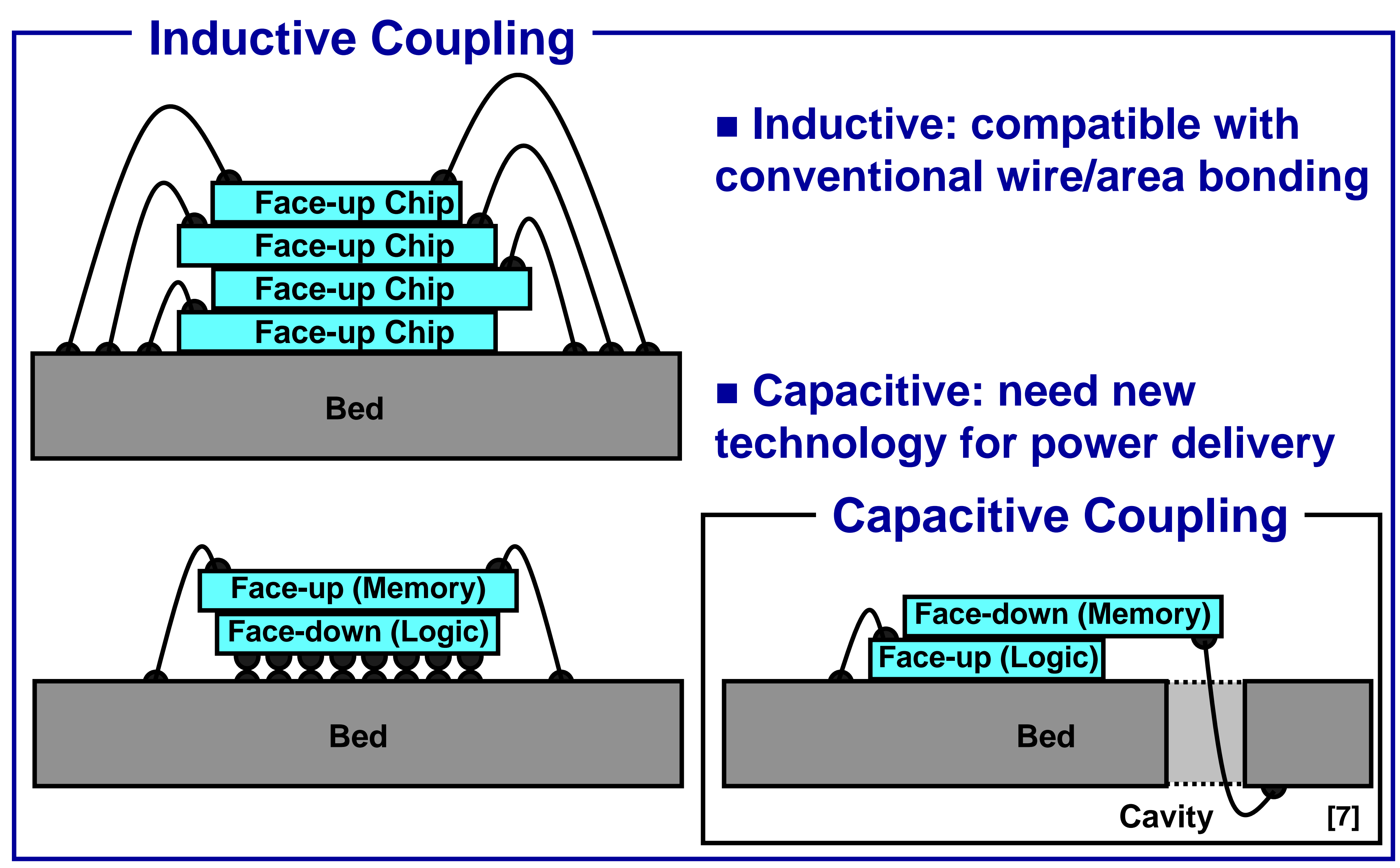
Inductive vs. Capacitive: Package Flexibility



- Inductive: compatible with conventional wire/area bonding
- Capacitive: need new technology for power delivery

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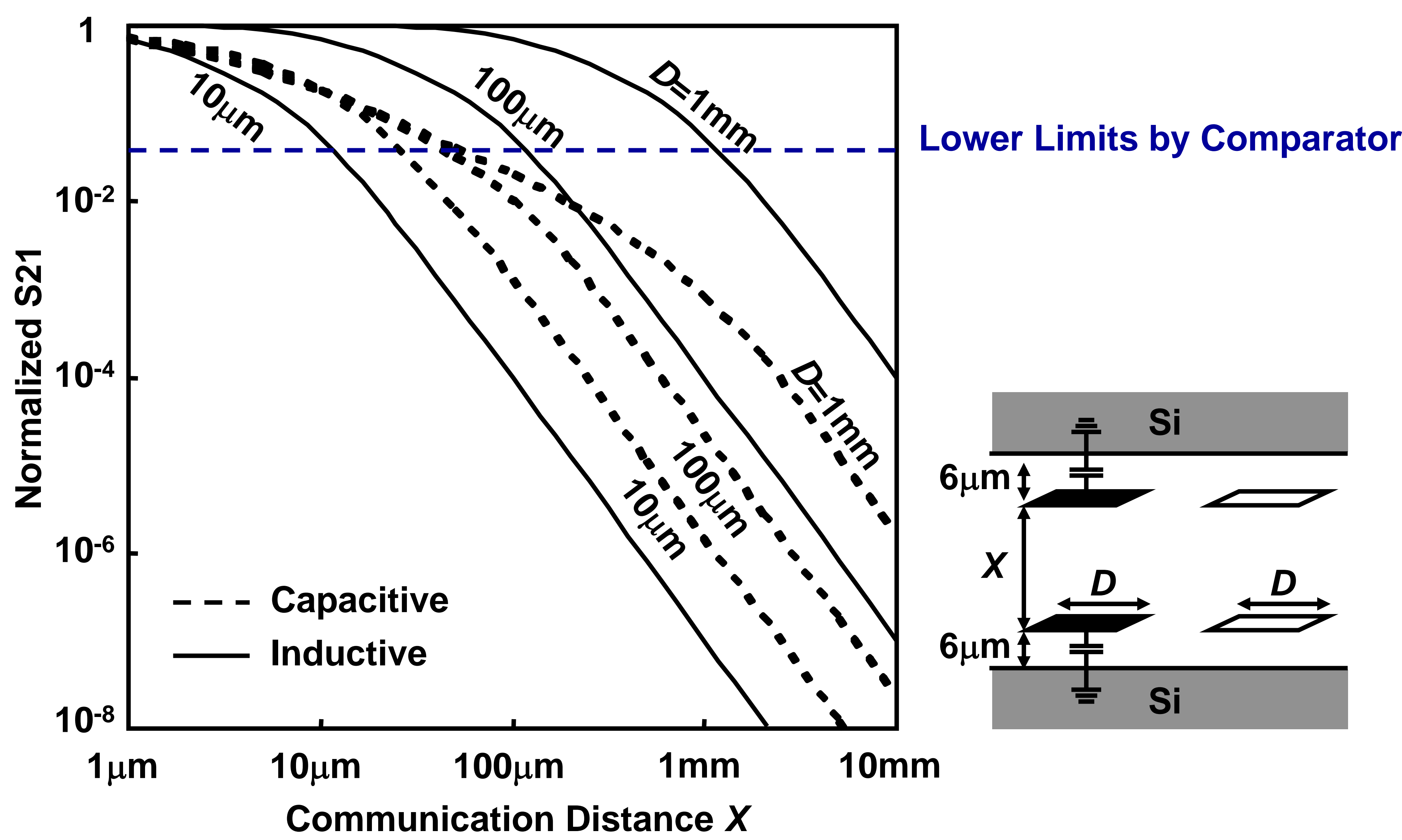
Inductive vs. Capacitive: Range Scalability



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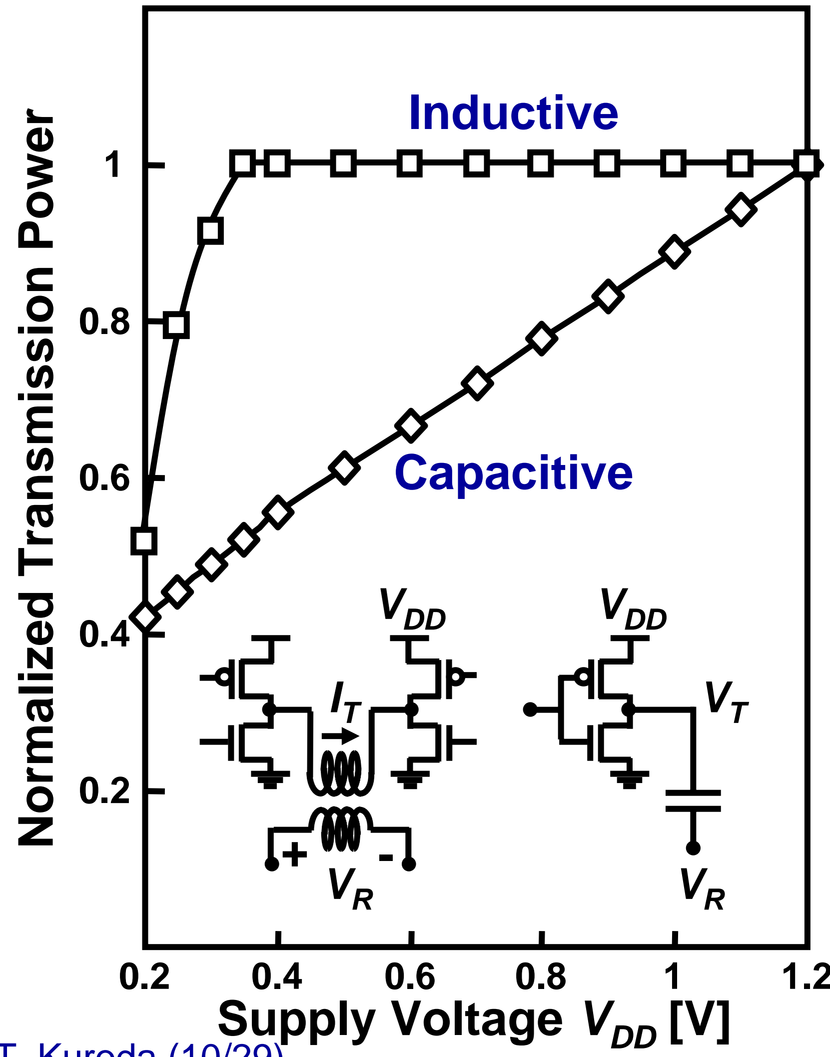
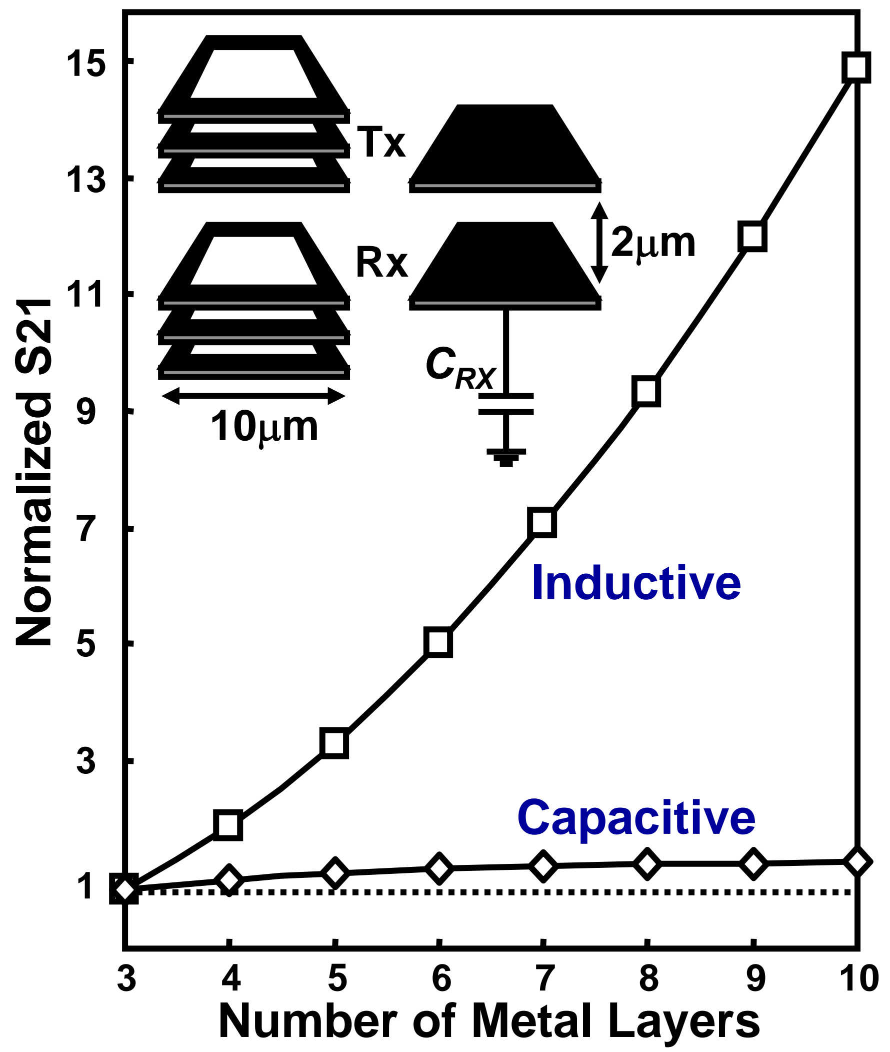
Inductive vs. Capacitive: Device Scalability

- **Transmission power can be secured even at low V_{DD}'s.**
- **Coupling coefficient is enlarged by increasing # of metal layers.**





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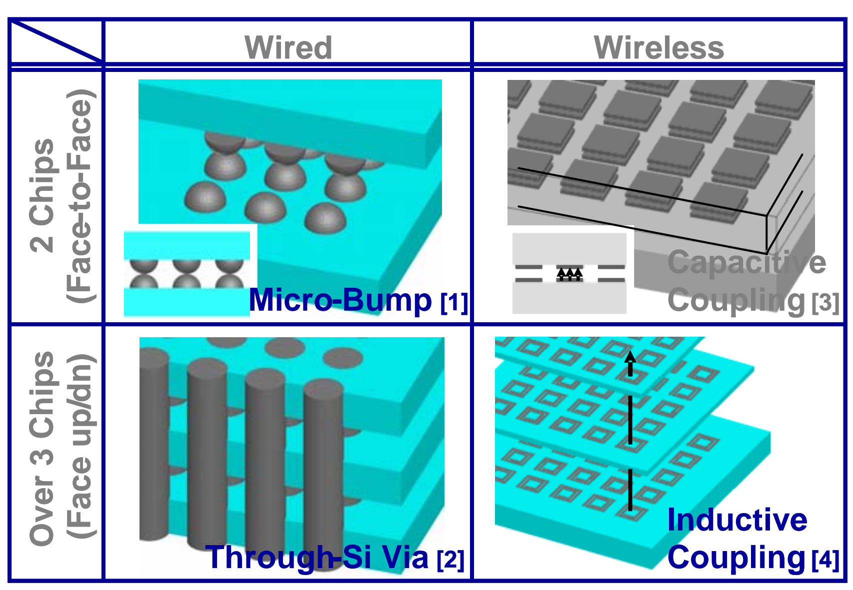
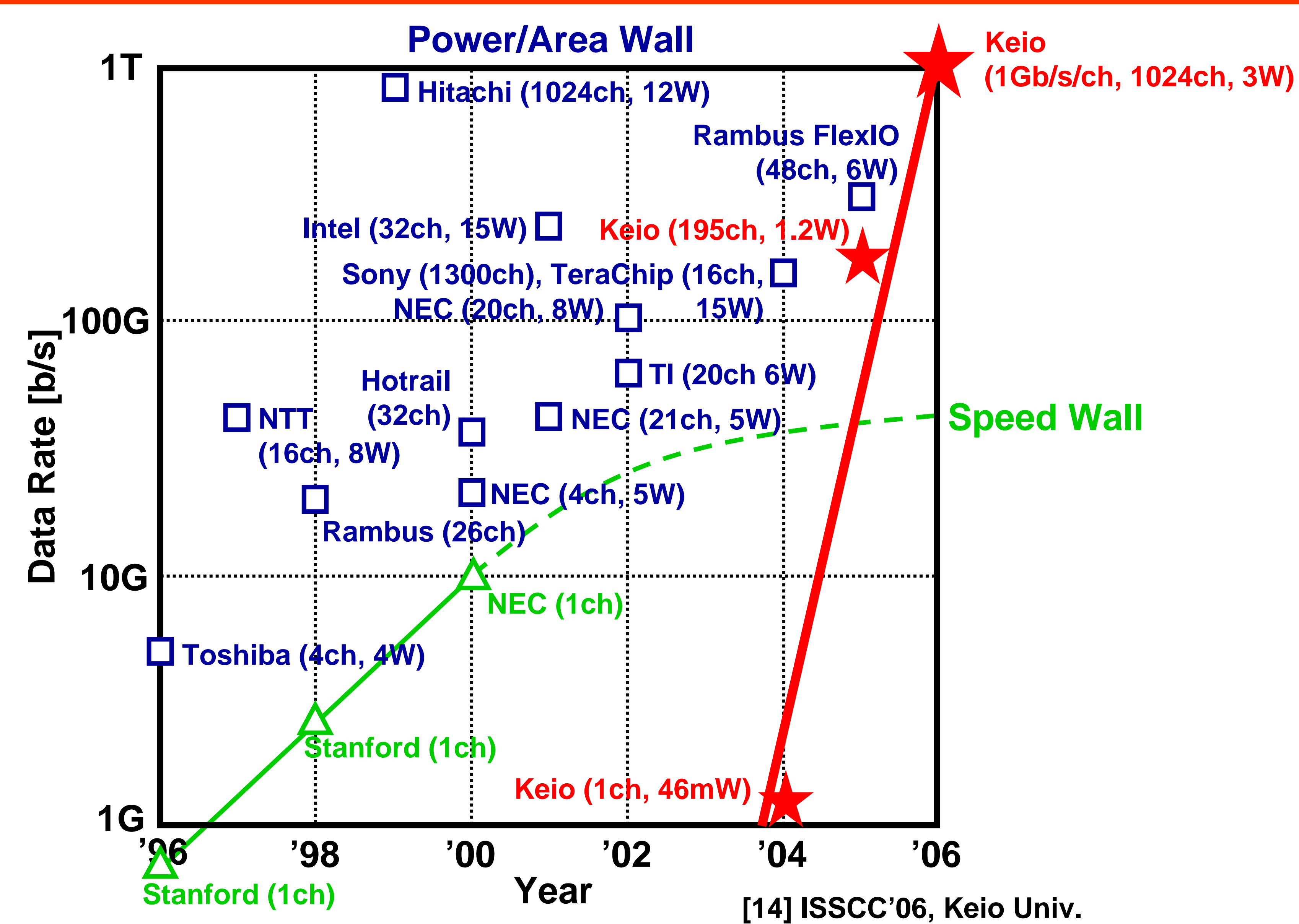
Inductive and Capacitive Coupling Link for 3D System Integration

- Inductive vs. Capacitive
- **Inductive vs. TSV, μ-bump**
- 3D Scaling Scenario



World Fastest (1Tb/s) Data Rate



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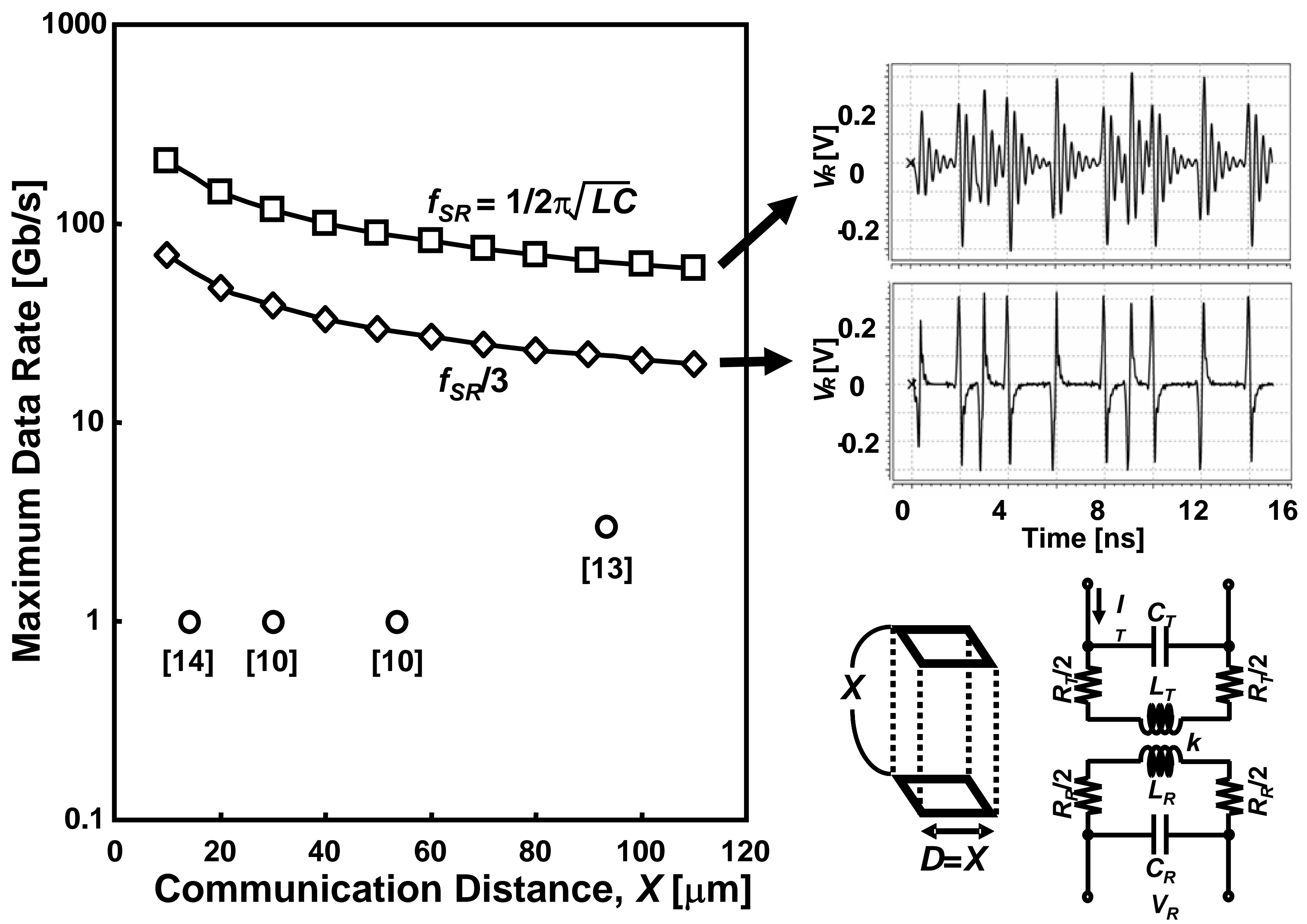
Maximum Data Rate per Channel



[17] Symp. on VLSI Circuits'06, Keio Univ.

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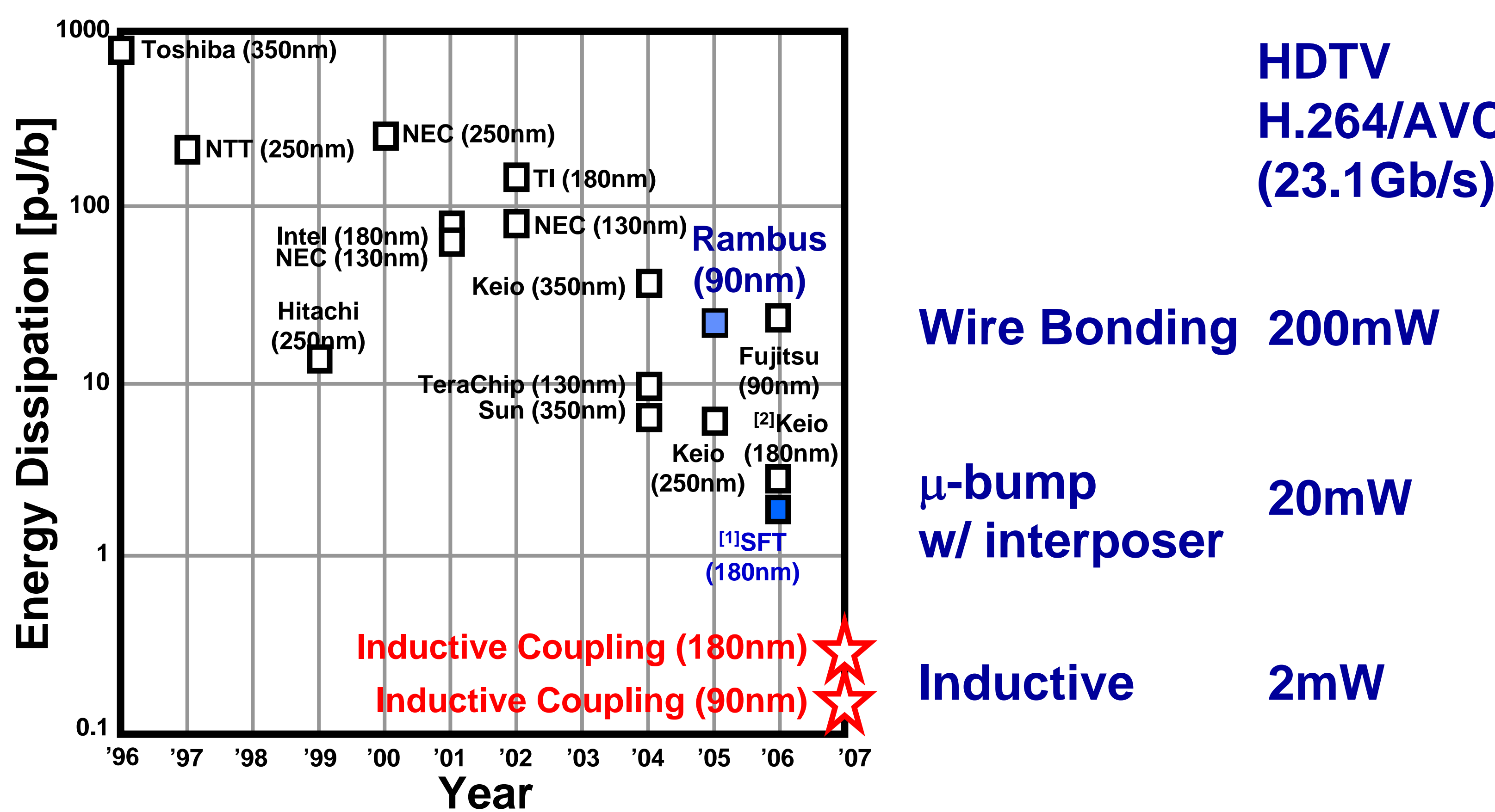
World Lowest Energy (0.14pJ/b)



[20.2] "A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping"

[16] ISSCC'07, Keio Univ.

World Smallest (1mm²/Tb/s)

Layout Area / Data Rate [mm²/Tb/s]

100k
10k
1k
100
10
1

Toshiba
NTT
Hitachi
TI
NEC
Intel
NEC
NEC
Hotrail
Sony
μ-bump
IBM, Sony, Toshiba
Keio (1ch)
Keio (195ch)
Keio (1024ch)

'96 '98 '00 '02 '04 '06

Year

[14] ISSCC'06, Keio Univ.

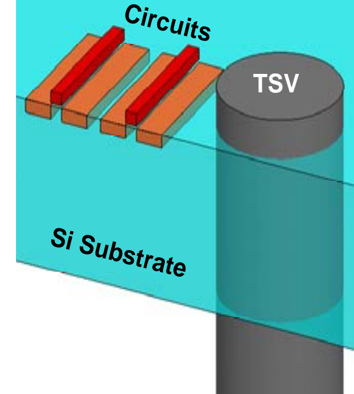
■ Horizontal Size

Inductive: 30μm pitch -> 20μm pitch
incl. transceiver circuits

TSV/μ-bump:
need additional area for circuits
difficult to scale due to ESD

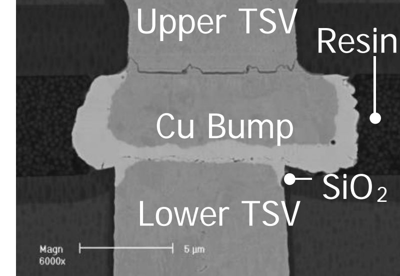
Tx
Rx

Inductor



■ Vertical Size

Inductive: no bump, thinner packaging
TSV/Bump: need bump, thicker



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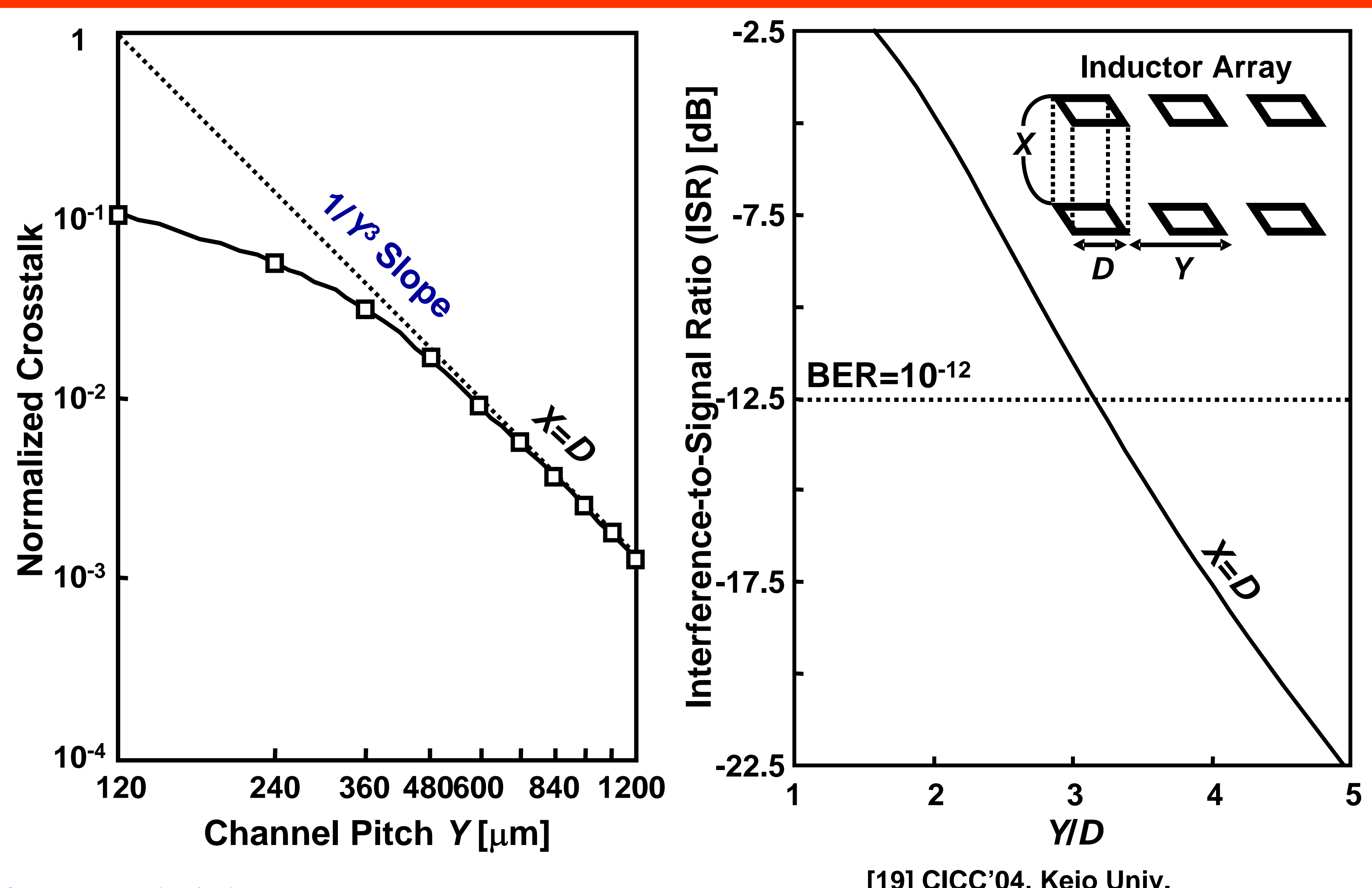
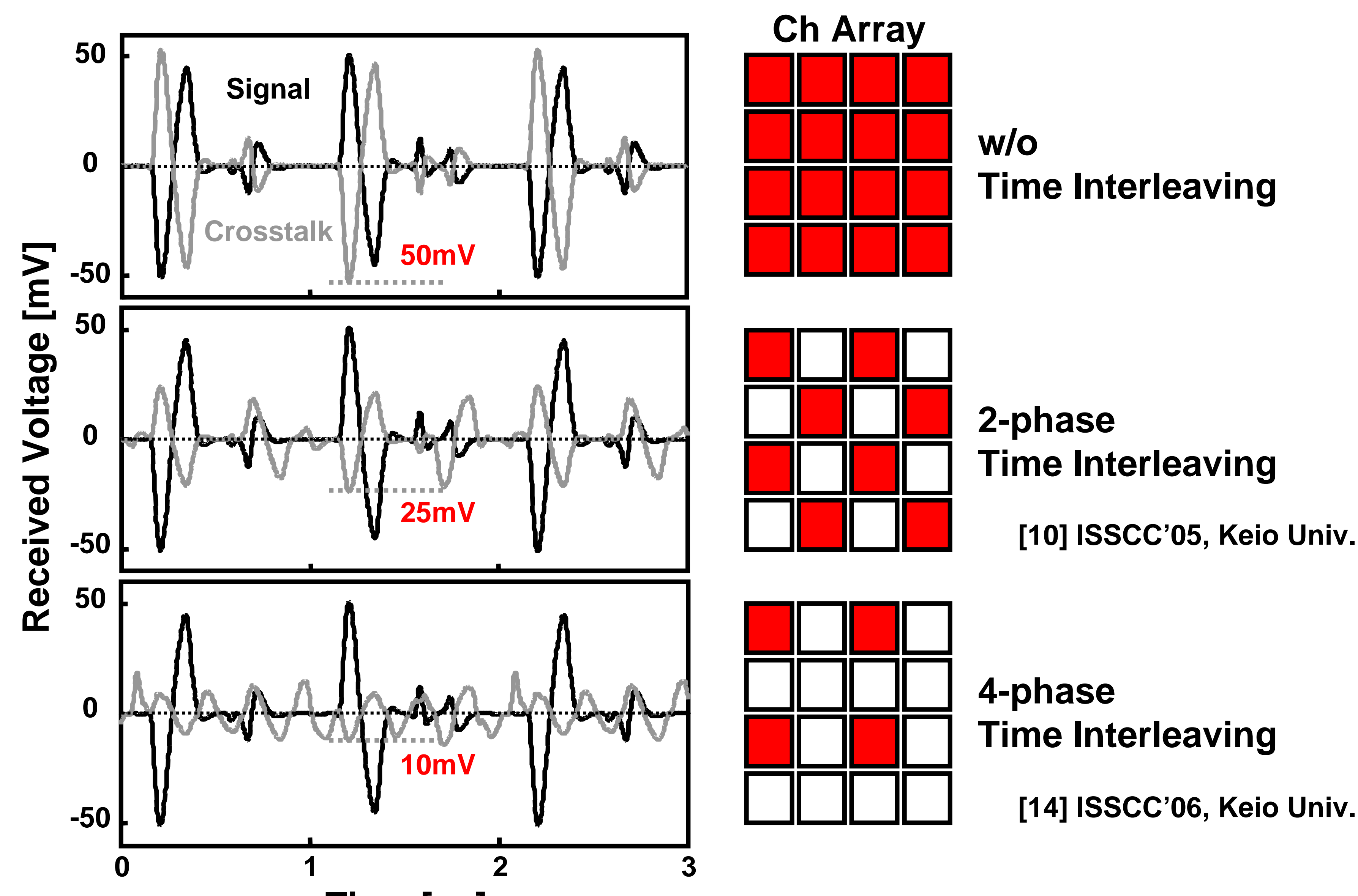
Channel Pitch vs. Crosstalk

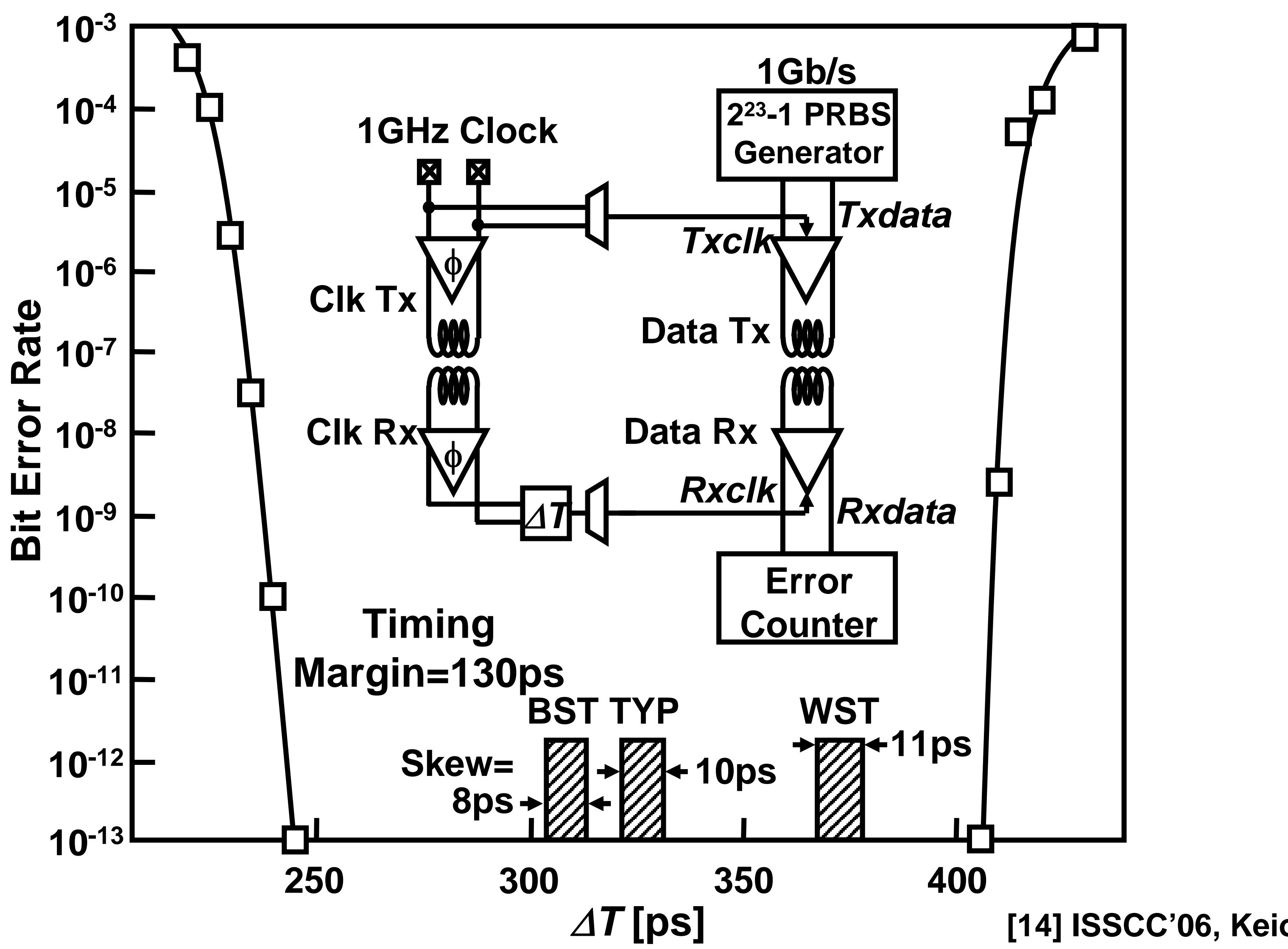


[19] CICC'04, Keio Univ.

Narrower Pitch by Time Interleaving



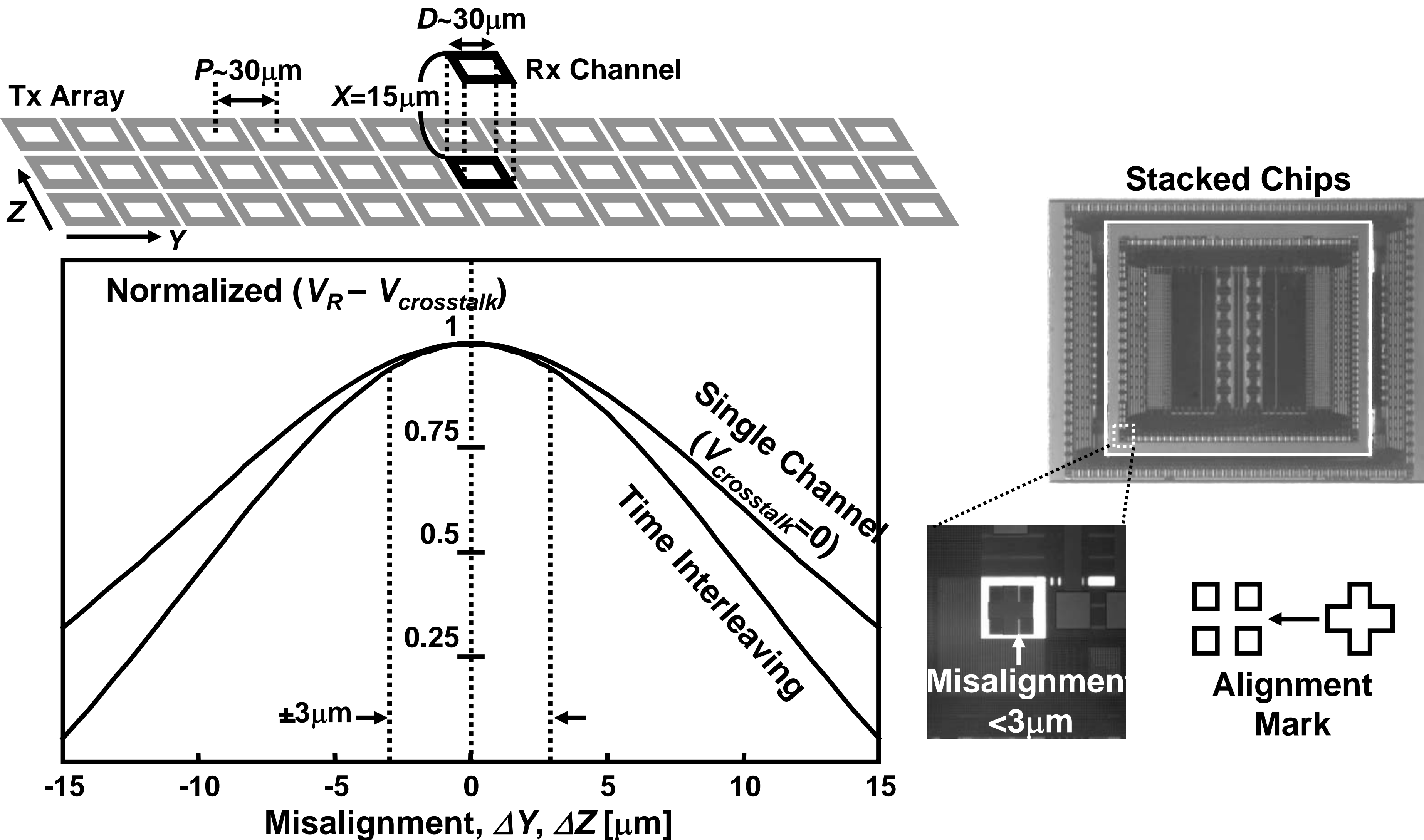
As Reliable As Wireline (BER<10^{-13})



[14] ISSCC'06, Keio Univ.

- Easy to synchronize

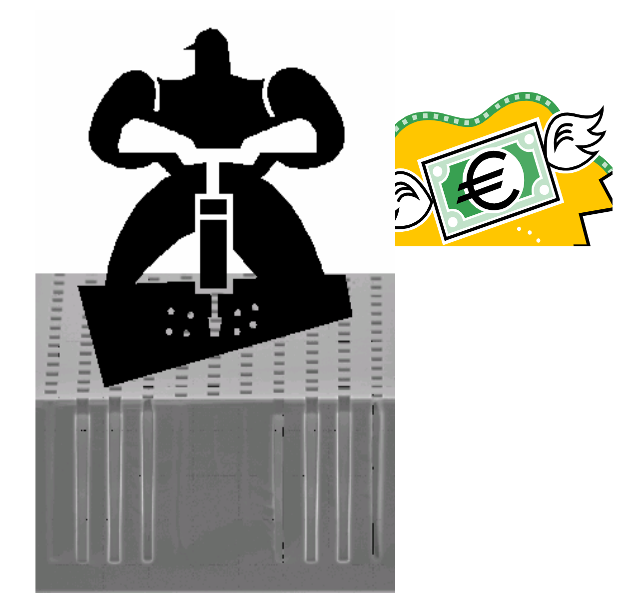
Misalignment Tolerance



- 3μm alignment error can be compensated by 5% power increase.

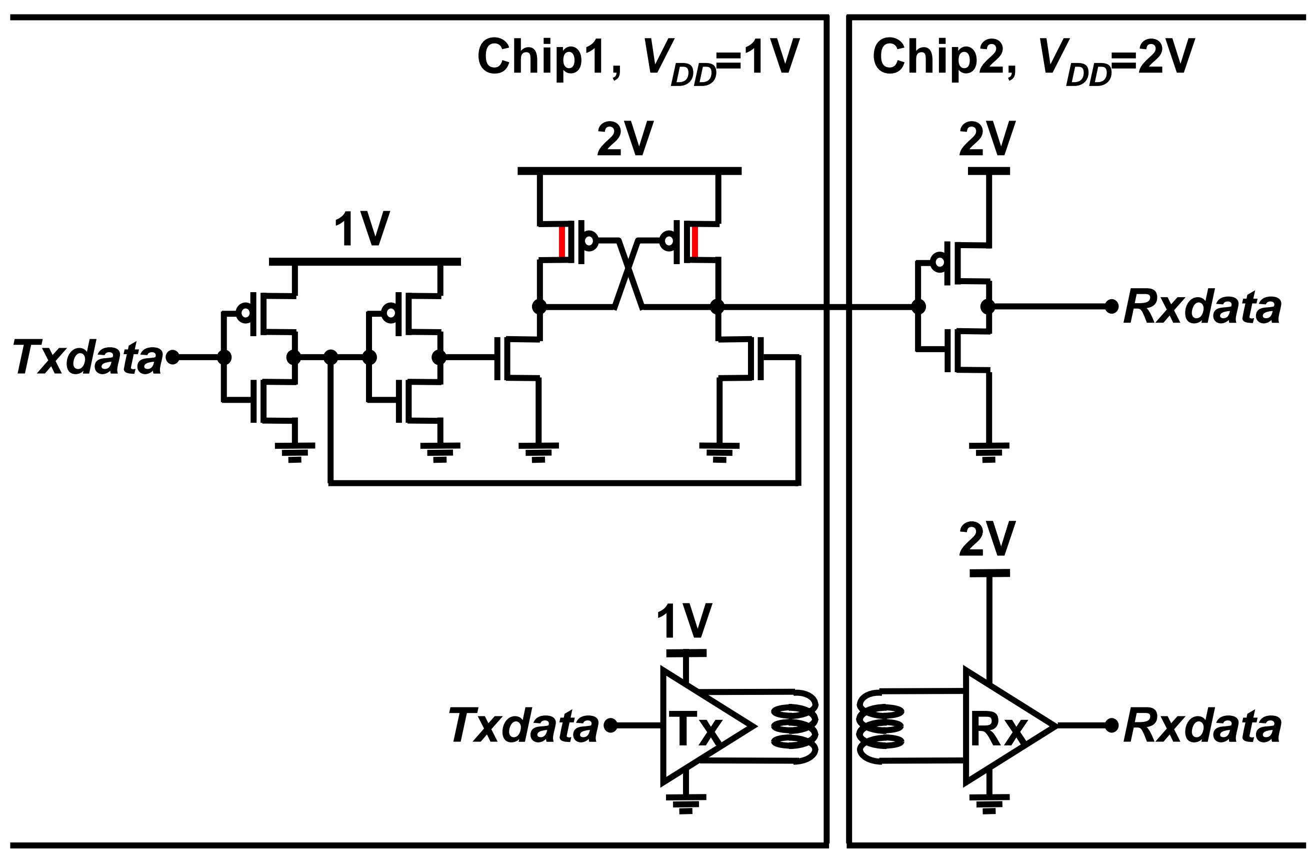
Cost

	Inductive	TSV, μ-bump
Process	Standard CMOS	New development
ESD protection	No need	Need
Cost penalty	Small	Large



AC Coupling

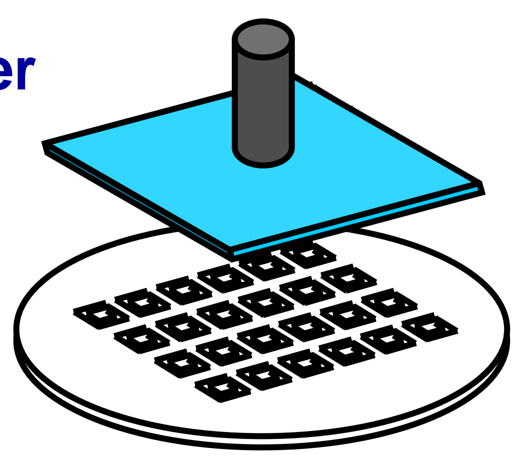
- No need for level shifters under different V_{DD}'s
- No need for additional V_{DD}'s nor thick gate oxide transistors
- V_{DD}'s can change: in burn-in, dynamic voltage scaling

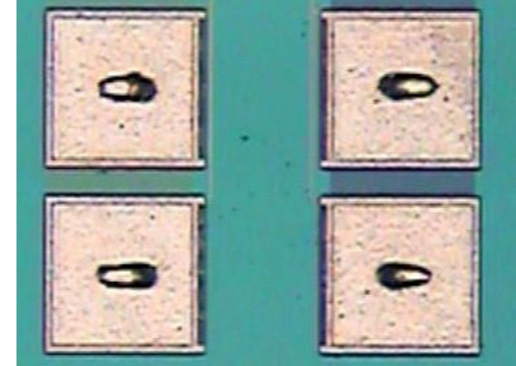


[20] ESSCIRC'06, Keio Univ.

Detachable

- At-speed test possible if same transceiver are arranged in test head:
  - solve KGD problem
  - improve yield
  - remove built-in test circuit
- Wafer entirely test possible:
  - reduce test time and cost (¢3 /min)
- Avoid Pad damage by probe:
  - raise yield
- Replace a high-speed connector:
  - improve reliability
  - reduce cost





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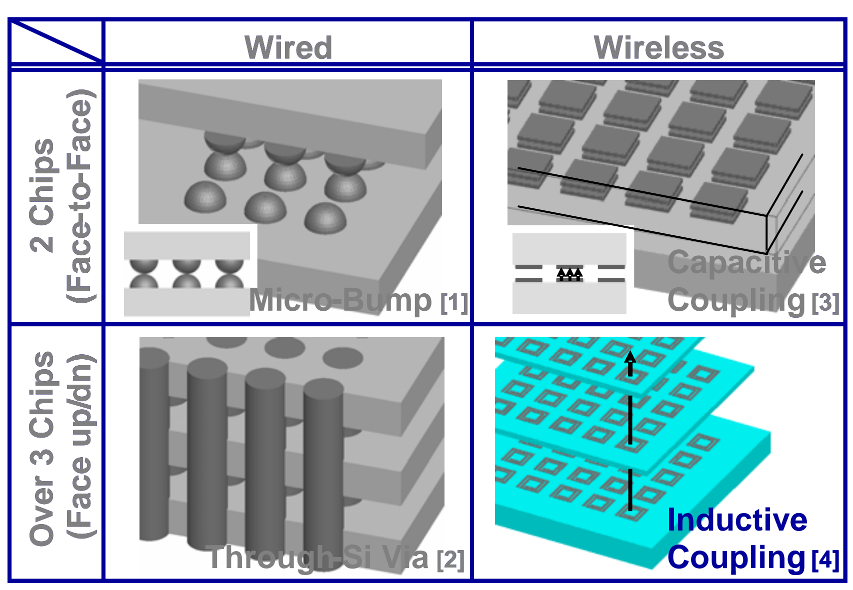
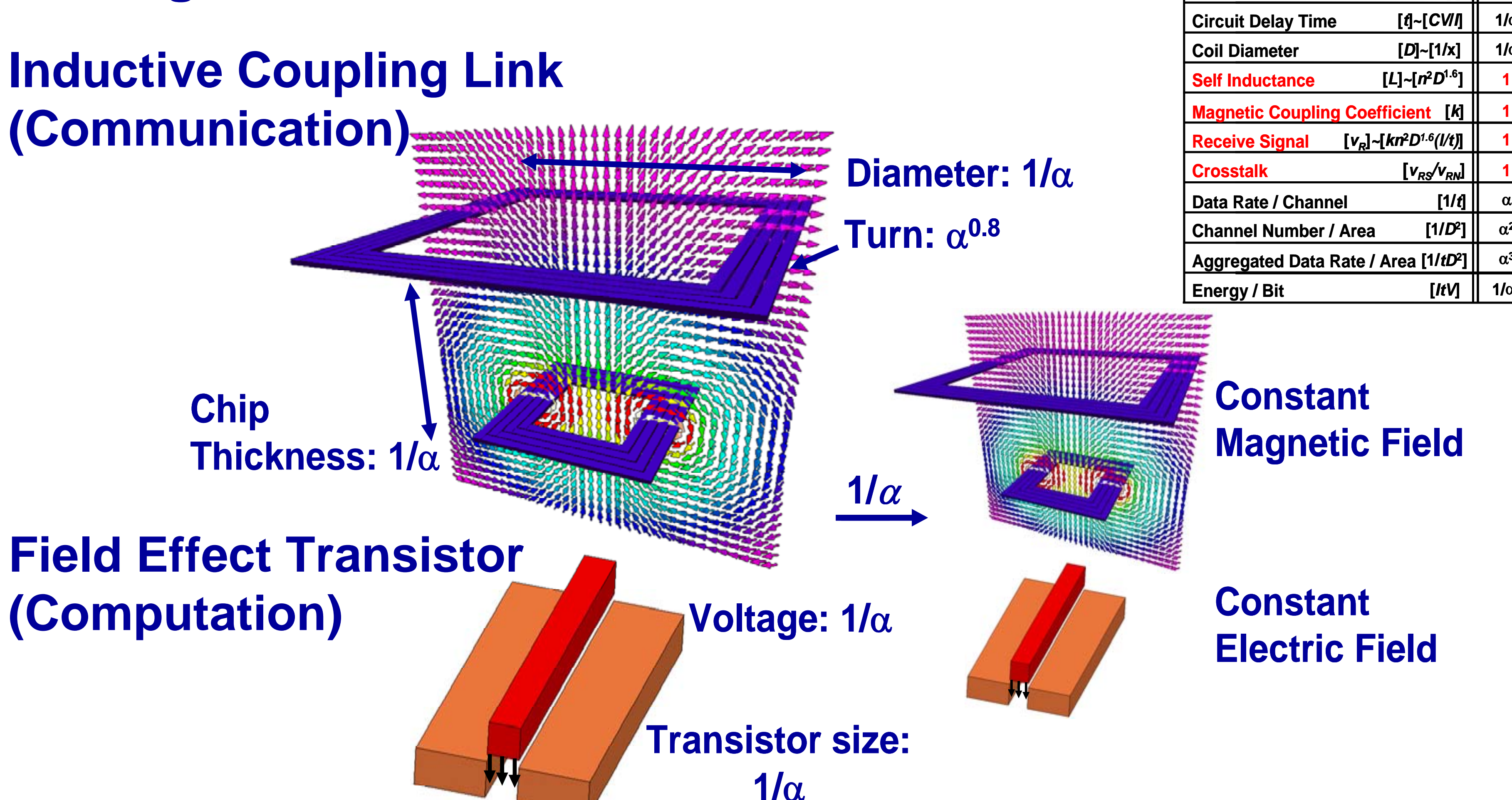


3D Scaling Scenario

Cost/Performance will be improved by a 3D scaling scenario:

Parameter	Symbol	Scaling
Transistor Size	$[x]$	$1/\alpha$
Power Supply Voltage	$[V]$	$1/\alpha$
Chip Thickness	$[T]$	$1/\alpha$
Coil Turn Number (Layer #)	$[n]$	$\alpha^{0.8}$
Current	$[I]$	$1/\alpha$
Circuit Delay Time	$[t]\sim[CV/I]$	$1/\alpha$
Coil Diameter	$[D]\sim[1/x]$	$1/\alpha$
Self Inductance	$[L]\sim[n^2D^{1.6}]$	1
Magnetic Coupling Coefficient	$[k]$	1
Receive Signal	$[v_R]\sim[kn^2D^{1.6}(I/t)]$	1
Crosstalk	$[v_{RS}/v_{RN}]$	1
Data Rate / Channel	$[1/t]$	α
Channel Number / Area	$[1/D^2]$	α^2
Aggregated Data Rate / Area	$[1/tD^2]$	α^3
Energy / Bit	$[ItV]$	$1/\alpha^3$



[20] ESSCIRC'06, Keio Univ.

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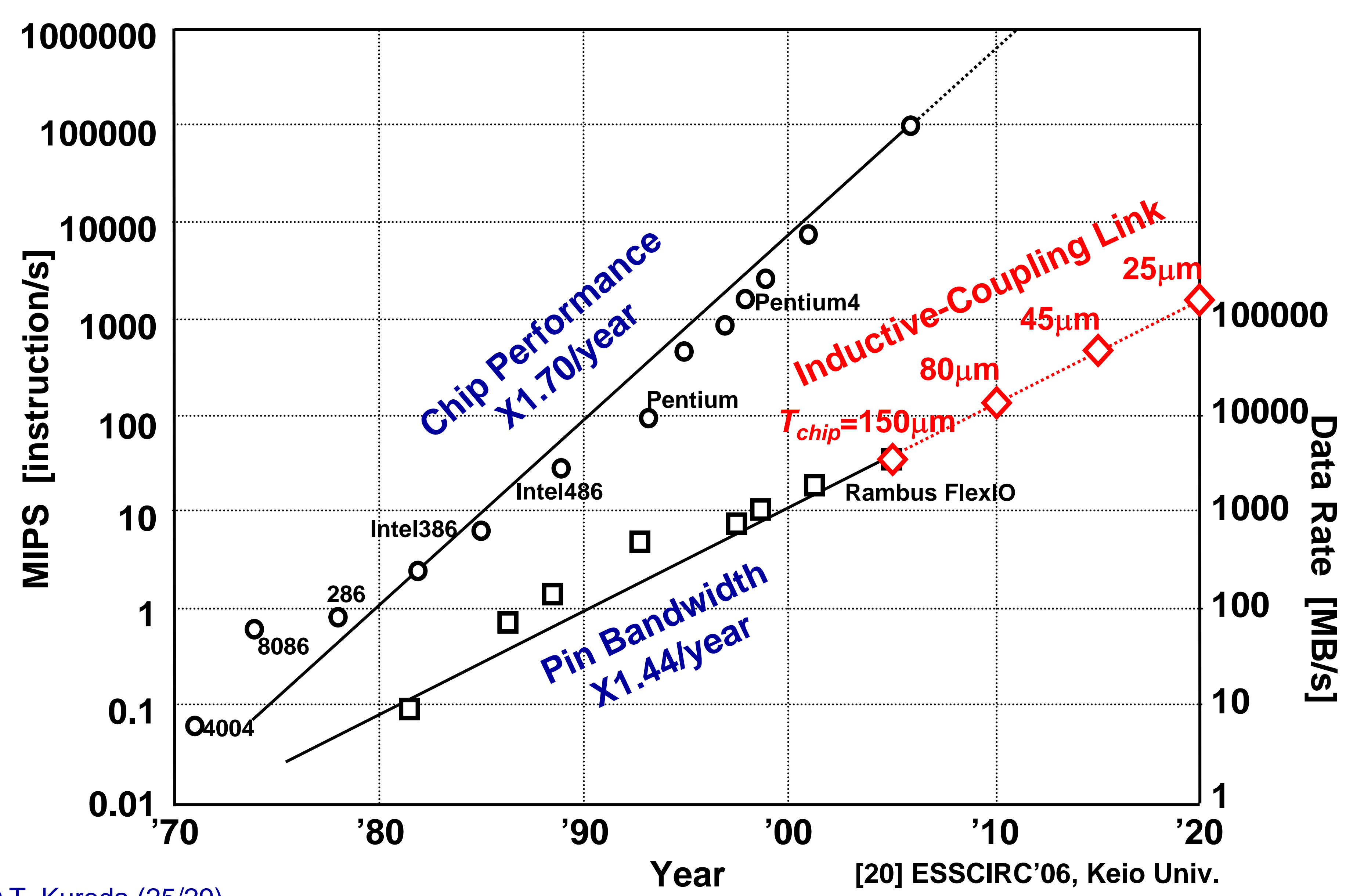
3D Technology Roadmap



[20] ESSCIRC'06, Keio Univ.

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Summary (1) : Inductive vs. Capacitive

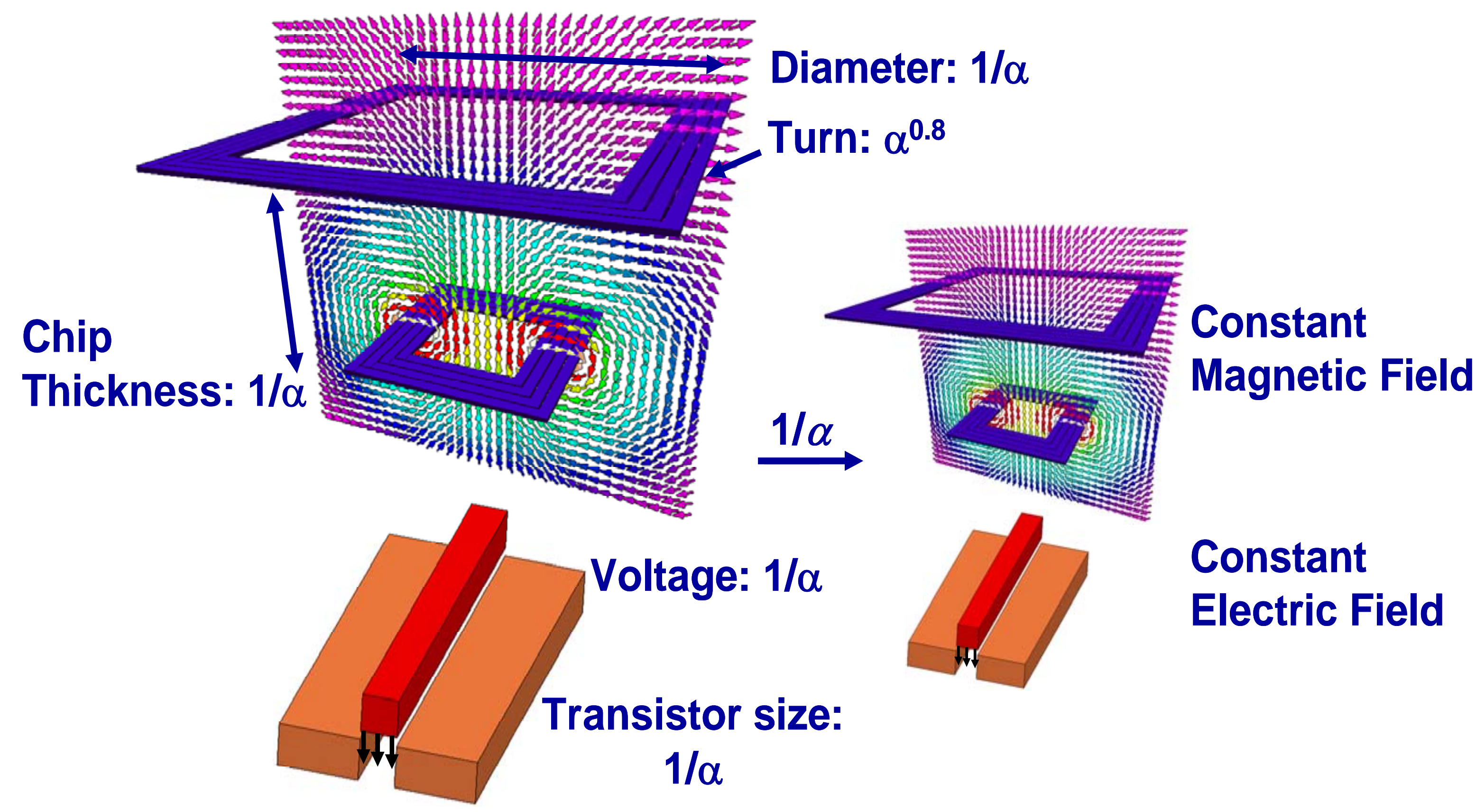
- Inductive coupling has advantages over capacitive coupling in terms of coupling strength through body, package flexibility, communication range scalability, and device scalability.
- Inductive coupling can link >2 chips (face up or down).

Summary (2) : Inductive vs. TSV/μ-Bump

- Inductive coupling bears comparison with TSV/μ-Bump in terms of data rate (1Tb/s), reliability (BER<10^{-13}), energy dissipation (0.1pJ/b)
- Inductive coupling is applicable to a standard CMOS, and less expensive than TSV/μ-Bump.
- Inductive coupling can eliminate ESD protection to lower delay, power, area.
- Inductive coupling exhibits high alignment tolerance.
- Inductive coupling provides with AC coupling link and makes interface design easy under multiple/variable V_{DD}'s.
- Inductive coupling may make non-contact testing possible.

Summary (3) : 3D Scaling Scenario

- Constant magnetic field scaling scenario by thinning chip thickness is proposed as a new guideline for 3D integration.



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To Probe Further

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