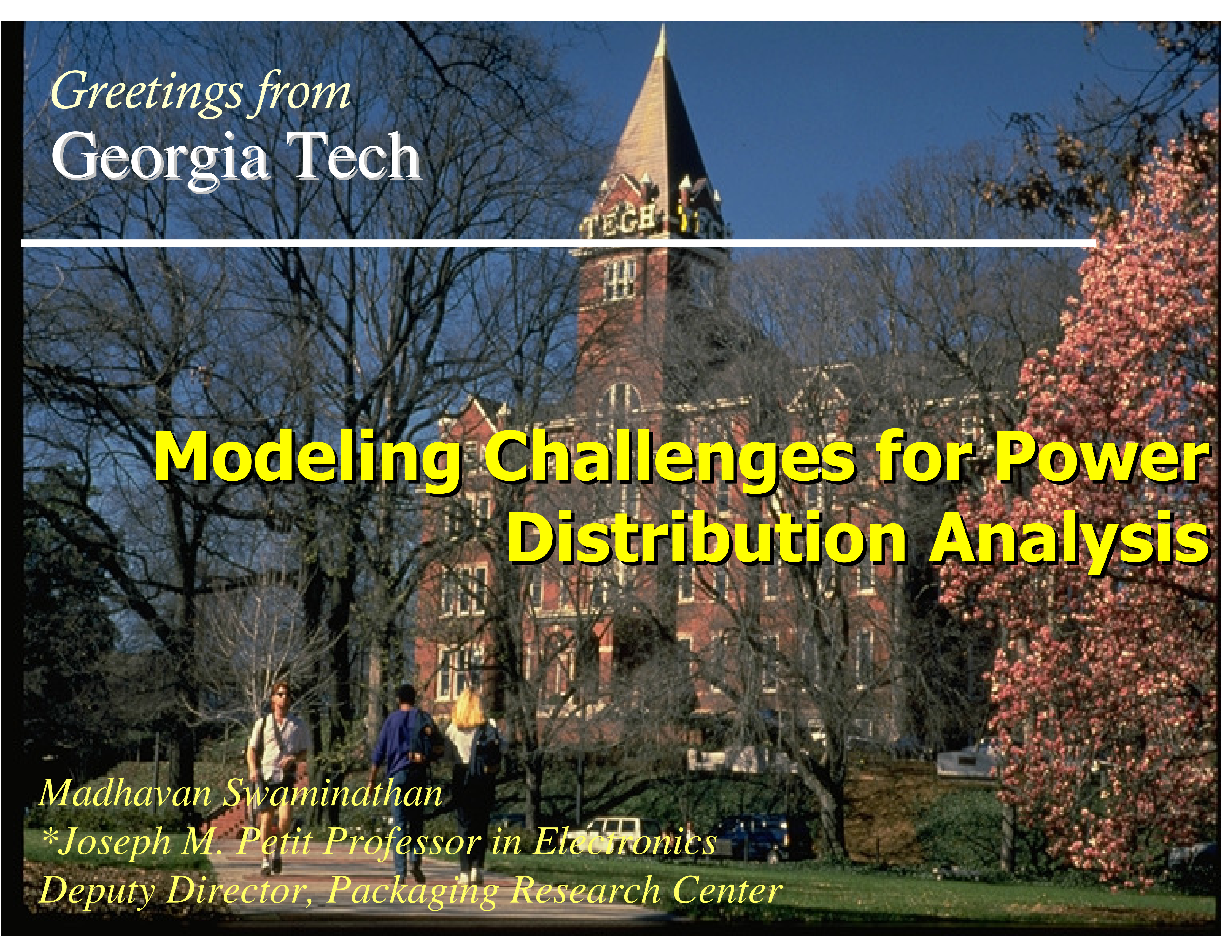
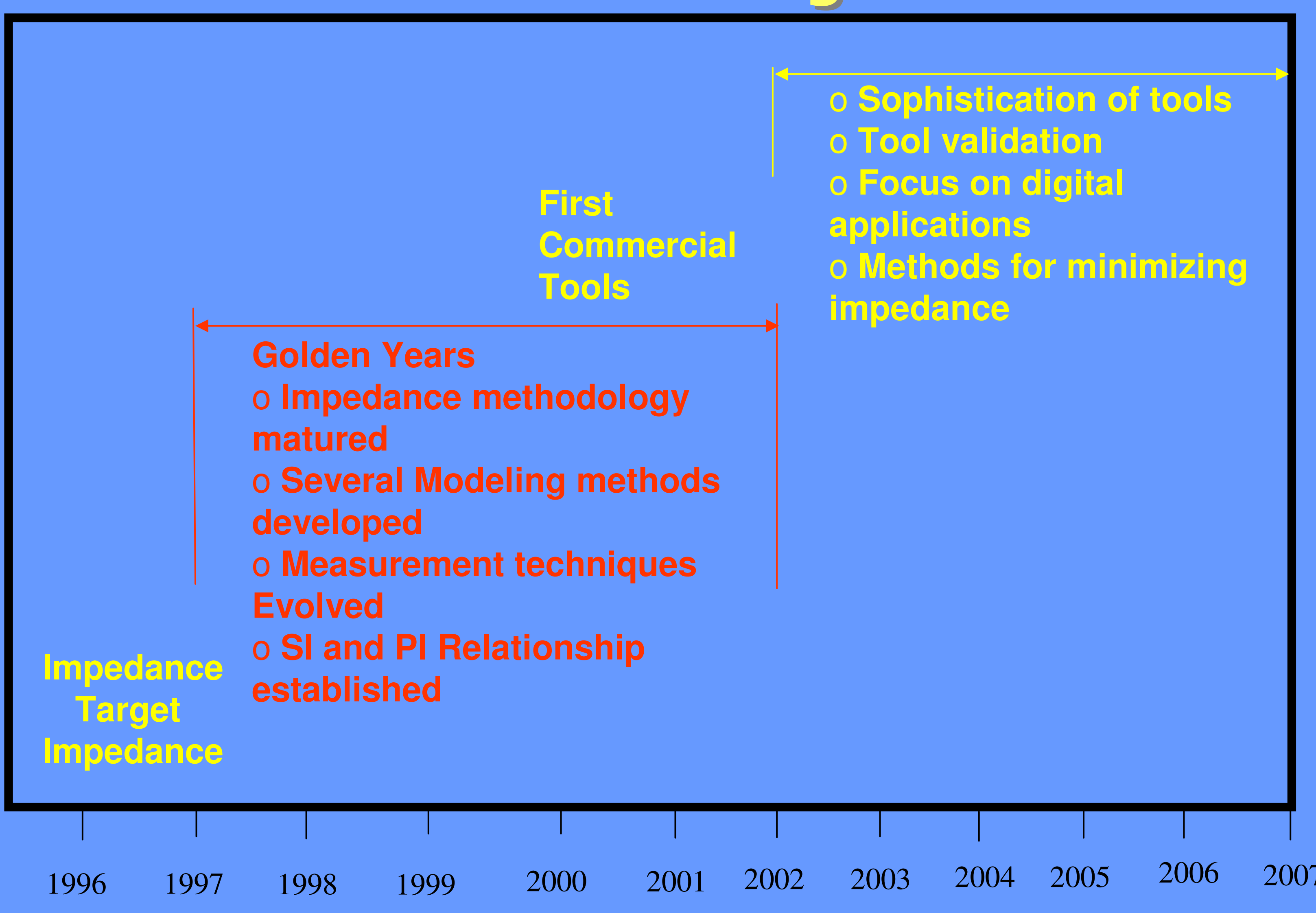

Greetings from
Georgia Tech
TECH
Modeling Challenges for Power Distribution Analysis
Madhavan Swaminathan
*Joseph M. Petit Professor in Electronics
Deputy Director, Packaging Research Center

Outline

- **Power Distribution – Where are we today ?**
- **What are the future Challenges in Power Distribution ?**
- **A few examples to illustrate these challenges**

Power Distribution
A Decade of Progress

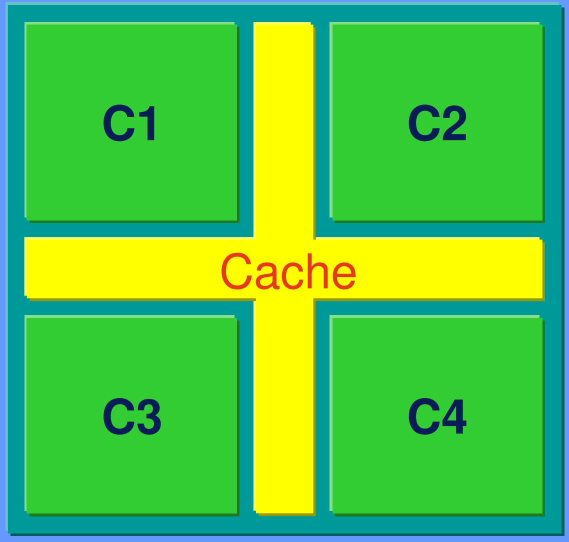


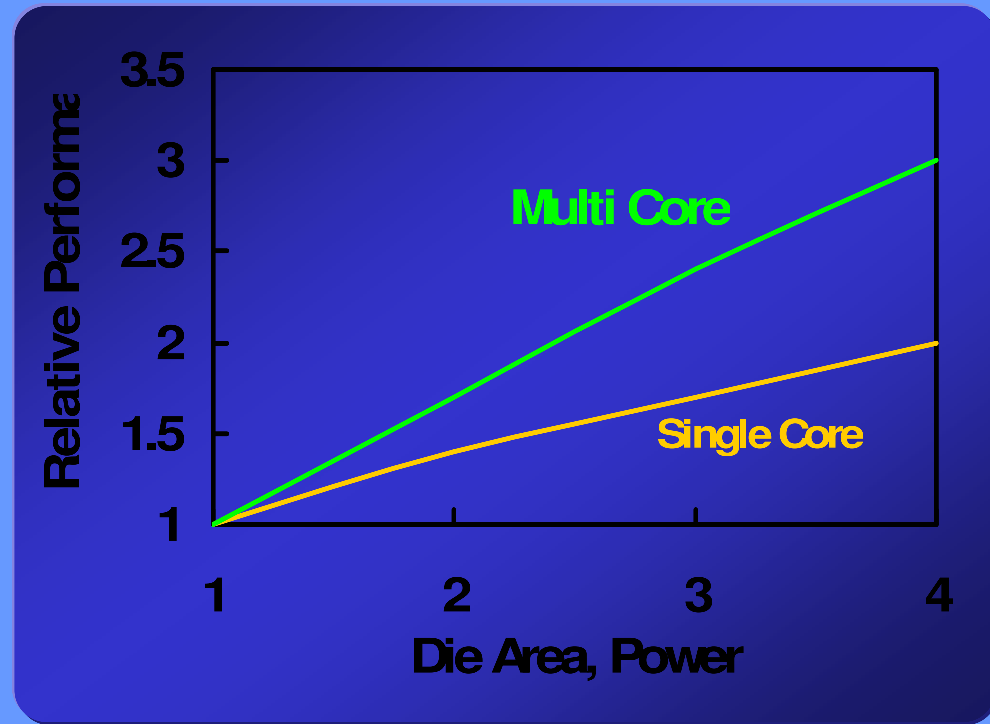
New System Drivers

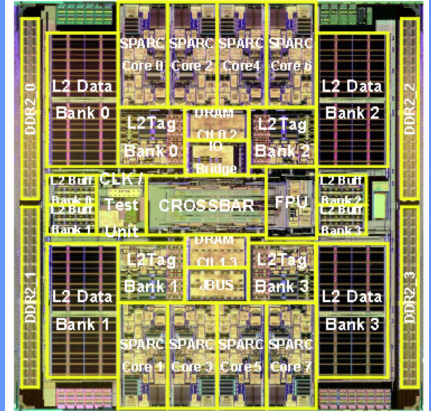
- ❑ Chip Multi-processing
- ❑ Trend Towards Convergent Heterogeneous Systems
- ❑ Emergence of SIP and SOP as new integration approaches
- ❑ Move towards embedded technologies
- ❑ Transition to Cu Low K and Ultra Low K dielectrics by Semiconductor Industry
- ❑ Combination of Chip and Package Integration for system miniaturization leading to new concepts in Chip – Package Co-Design

How do these drivers affect Power Distribution as we know it today ?
What should the focus be for tool development in the future ?

Chip Multi-Processing





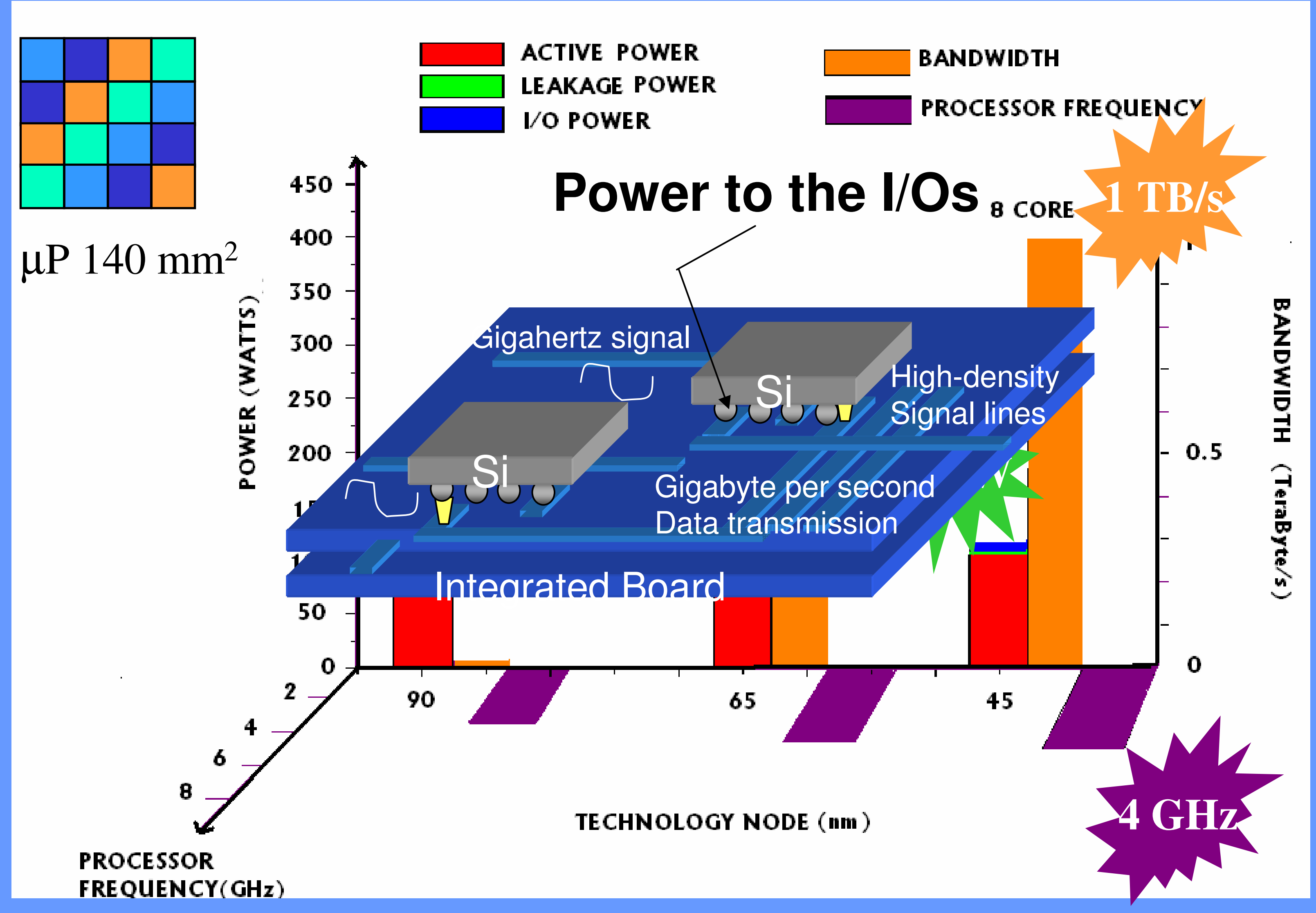


Niagara (SUN)

Courtesy: S. Borkar, Intel

- Multi-core, each core Multi-threaded
- Shared cache and front side bus
- Each core has different Vdd & Freq
- Core hopping to spread hot spots
- Lower junction temperature

Multi-core Processors (Reverse Scaling)

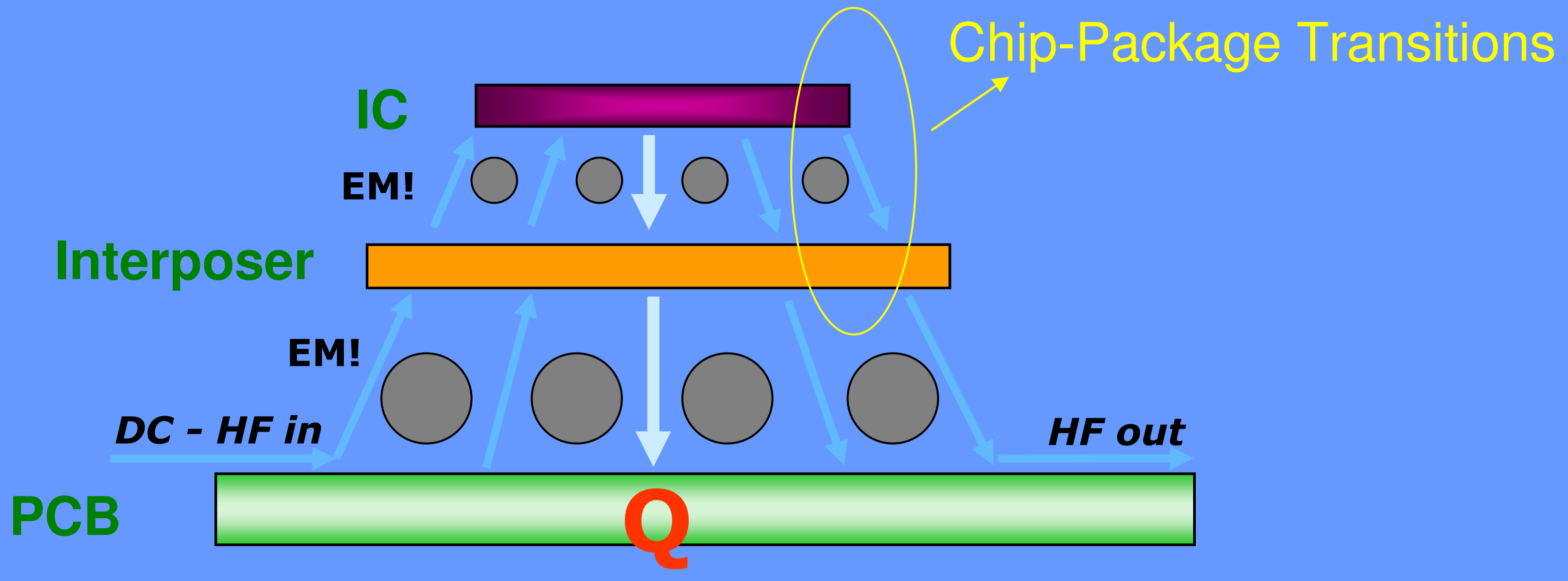


Power Distribution Challenges

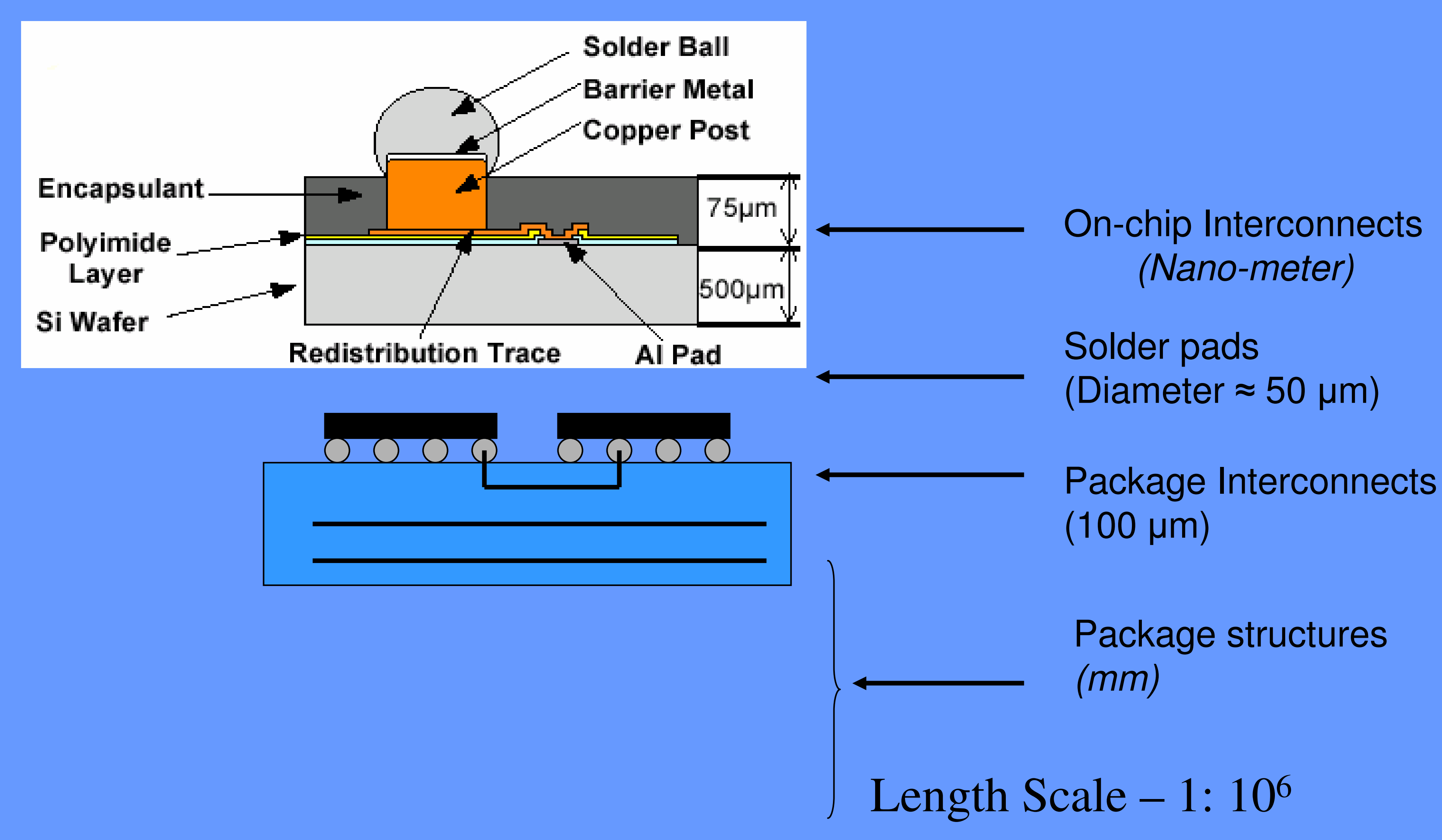
- **Chip – Package Co-Design**
  - Modeling of Multi-scale Structures
- **Managing electromigration in Cu Low K/Ultra Low K Dielectrics**
  - Methods for computing current density and Joule heating at high frequencies
- **Managing Coupling**
  - Problem has moved from the source (digital) to the sink (Analog/RF)
  - Use of embedded technologies
  - Methods for modeling coupling in fine geometries with > -100dB accuracy
- **Managing Eye with Minimum jitter**
  - Use of embedded technologies
  - Methods for Frequency to Time conversion

Chip – Package Co-Design

Chip on Package on System Board

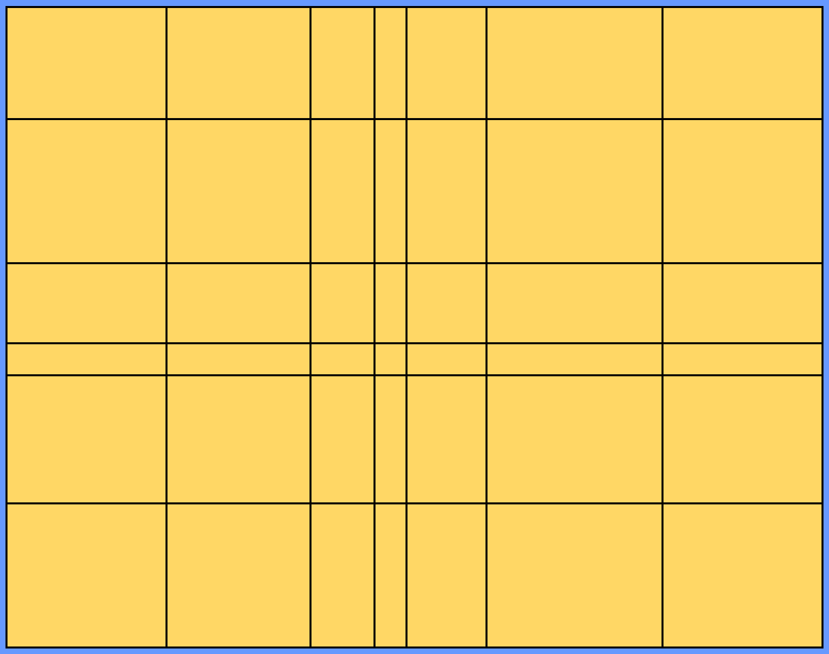


Multiscale Modeling for Chip-Package Co-Design Challenges



Courant Condition Limitation in Time Domain

EM Simulation



Smallest mesh dimension determines the time-step

$$\Delta t \le \frac{1}{v_{\max}} \left(\left(\frac{1}{\Delta x} \right)^2 + \left(\frac{1}{\Delta y} \right)^2 + \left(\frac{1}{\Delta z} \right)^2 \right)^{-\frac{1}{2}}$$

FDTD & Laguerre FDTD - Formulation

E_z

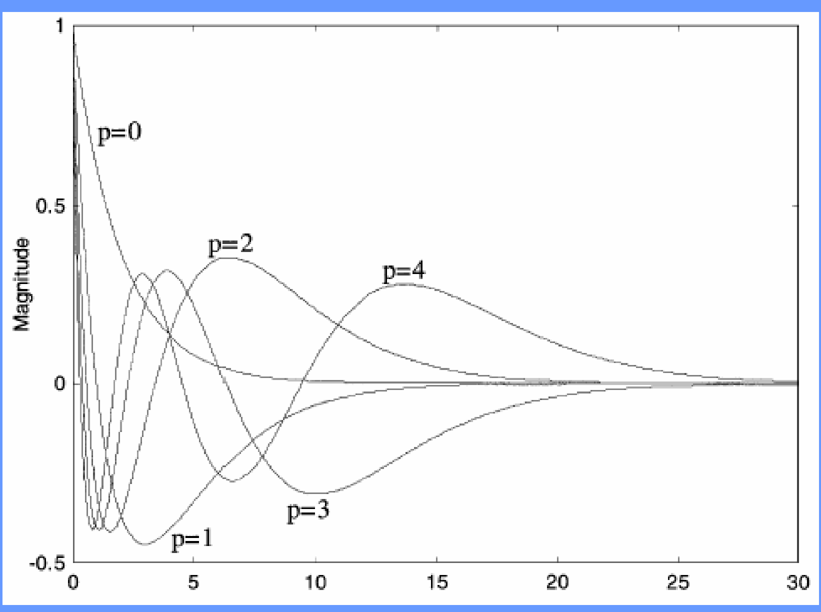
H_y

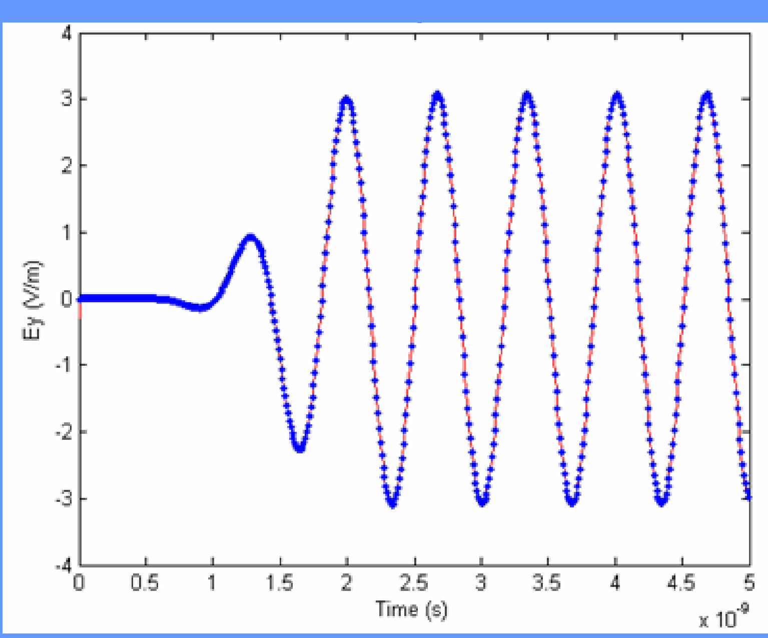
FDTD	SLeEC
Marching on Time	Marching on Degree
$E_z \rightleftarrows H_y$	$E_0, \; E_1, \ldots\ldots, \; E_q$

# of Coefficients << # of Time steps

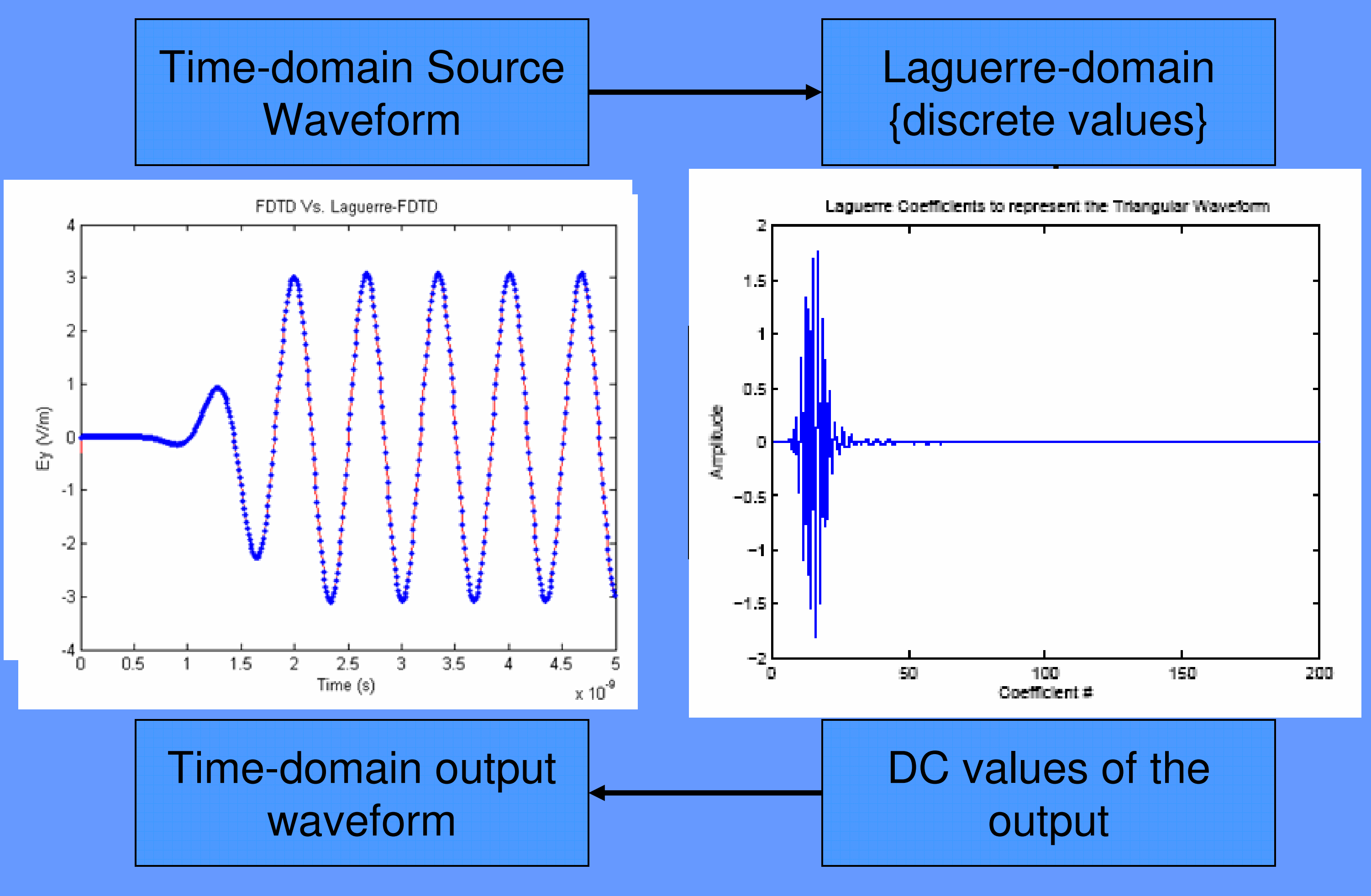
Basis Functions

Time-domain

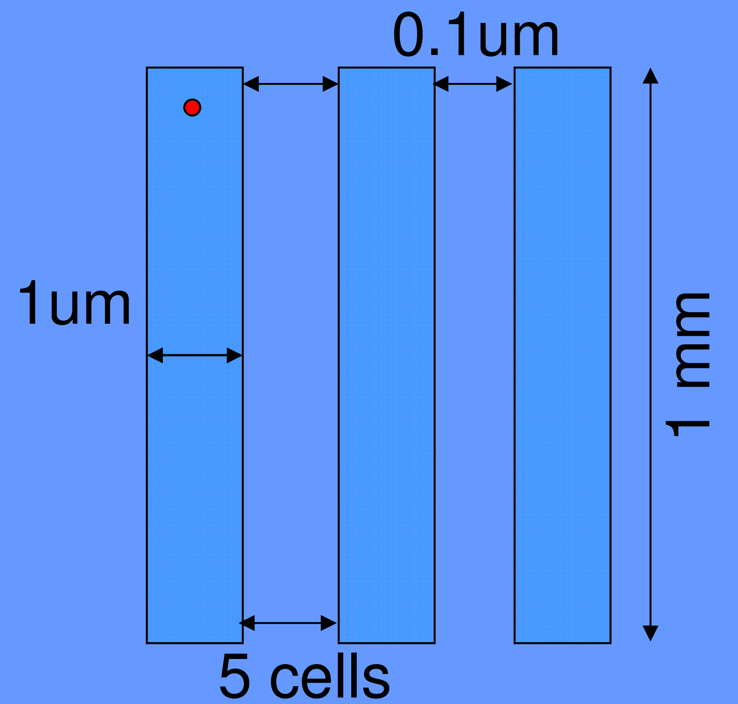




Laguerre Based FDTD Method



On-Chip Coupled Lines (15 000 cells)



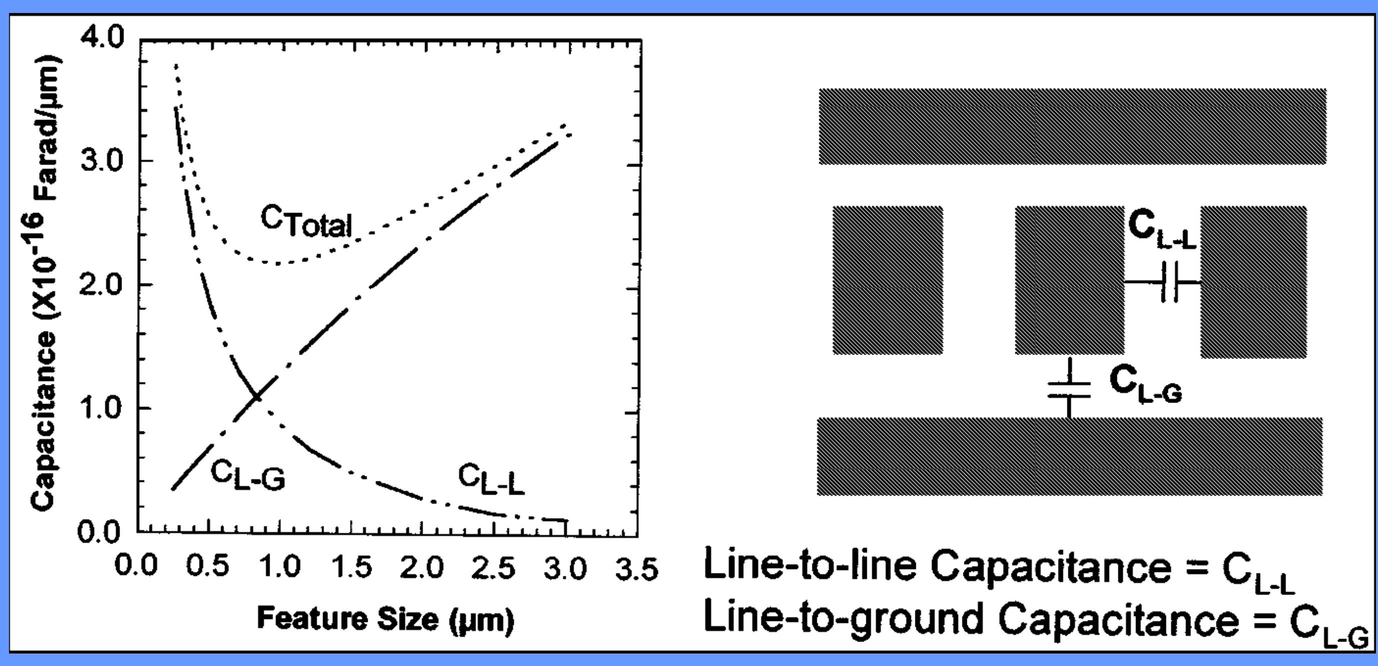
Even if the length is 10mm, the Courant condition is still $\Delta t = 2 \times 10^{-16}$

Solver	Time	Memory
FDTD	2160 min. (36 hours)	1 kB
SLeEC	30 min.	150 MB

Copper Low K and Ultra Low K

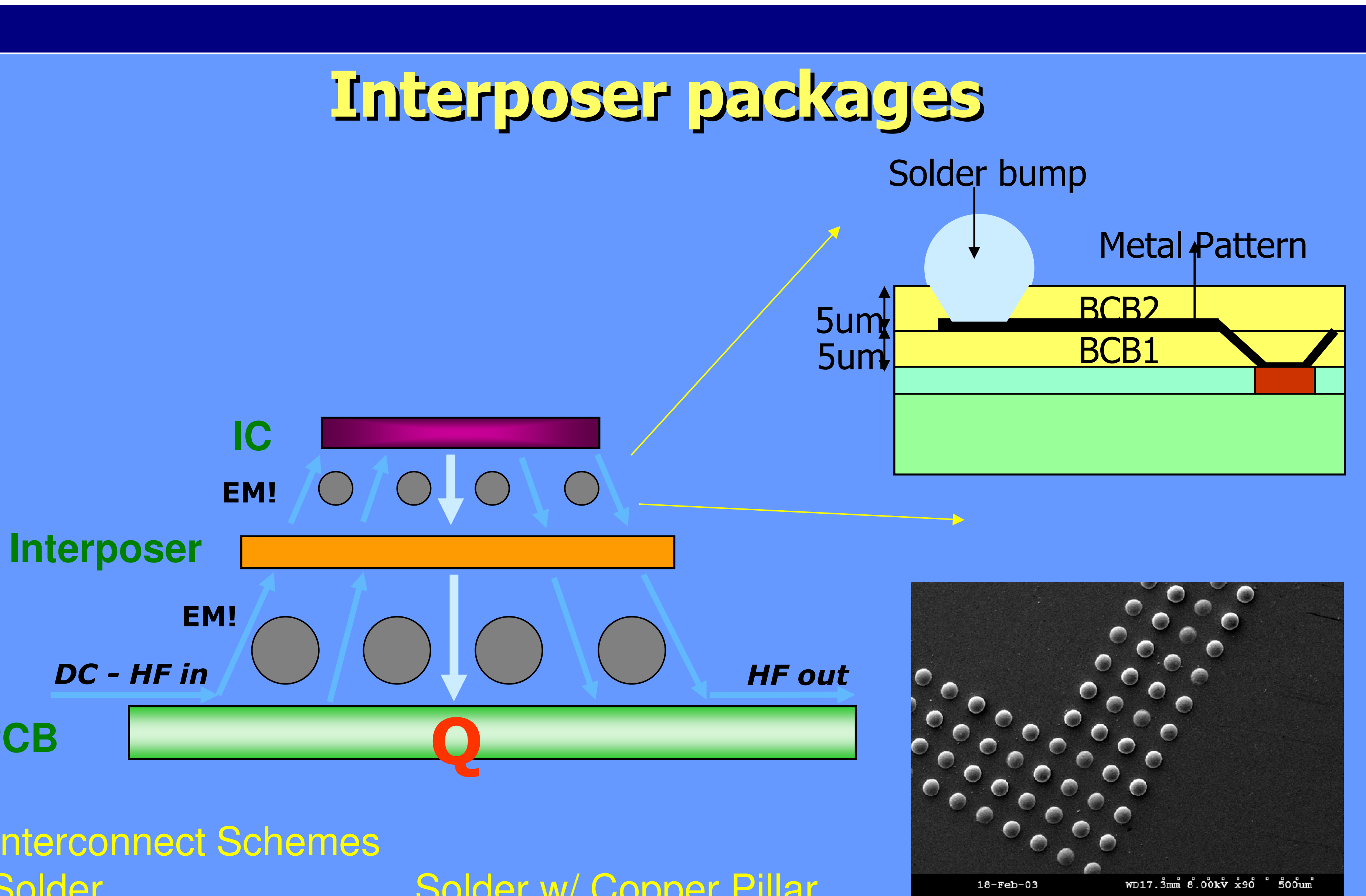
Move to Cu Low K/Ultra Low K

- Cu is a better conductor in terms of resistance capacitance delay
- Miniaturization
- Major concern is electromigration



Ref: Havemann And Hutchby: High-performance Interconnects,Proceedings of The IEEE, VOL. 89, NO. 5, MAY 2001

Interposer packages

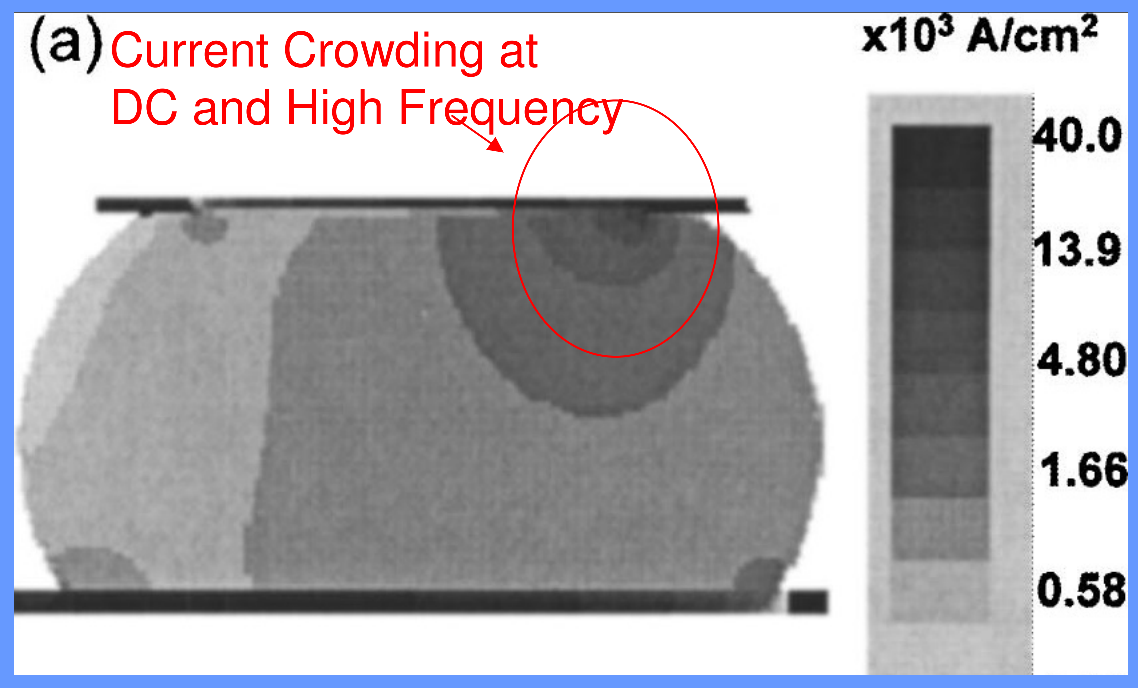


Interconnect Schemes

Solder | Solder w/ Copper Pillar
Nanocomposite | Carbon Nanotubes

20 – 60um Pitch Peripheral Array; 50 – 100um pitch area array

DC and High Frequency Effects in UBM



- ❑ Mean Time To Failure (MTTF) can decrease due to increased current densities
- ❑ Maximum current density allowed in solder joints is lower than Cu
- ❑ Modeling of current densities is needed to define interface metallurgies to maximize MTTF and extract Resistance and Inductance

High Frequency Modeling – IC to Interposer DC – 77 GHz

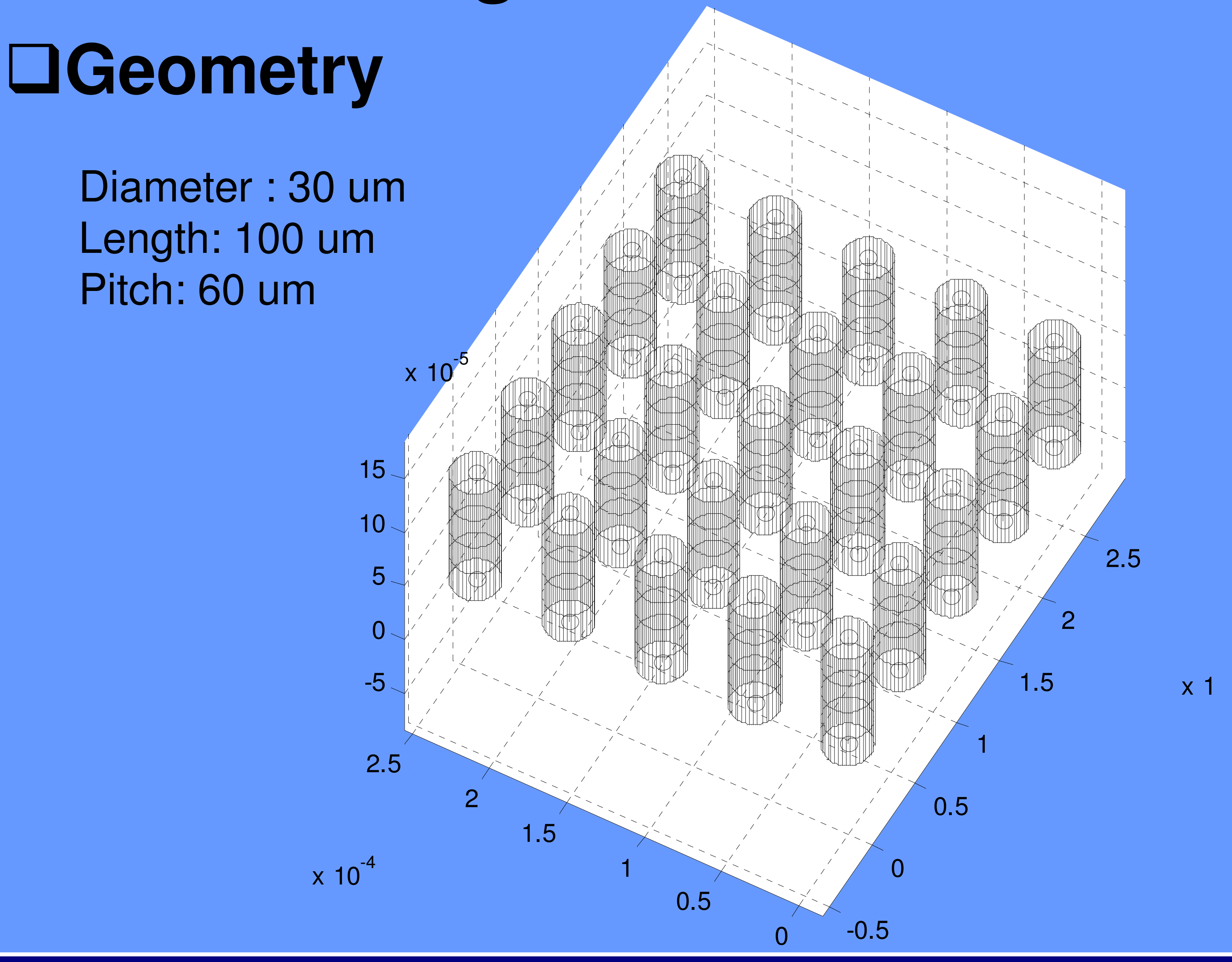
- **High-frequency effects in conductors**
  - o Skin effect
    - o As frequency increases, currents flows through the outer edge of conductor cross section.
    - o Effective area of current flowing decreases, resulting in current flow almost on the outer surface.
    - o Resistance increases with square root of frequency.
    - o Inductance decreases since the internal inductance vanishes.
  - o Proximity effect
    - o When a conductor is near another conductor, currents crowd to a certain region at the outer edge.
    - o Resistance increases with frequency.
  - o Both effects important for UBMs and Package Interconnects
    - o When a conductor is near another conductor, currents crowd to a certain region at the outer edge.
    - o Resistance increases with frequency.

- **Importance of high-frequency modeling in conductors**
  - Increases conductor loss making signal transmission inefficient at high frequencies.
  - Higher local current density causes increased electromigration effects

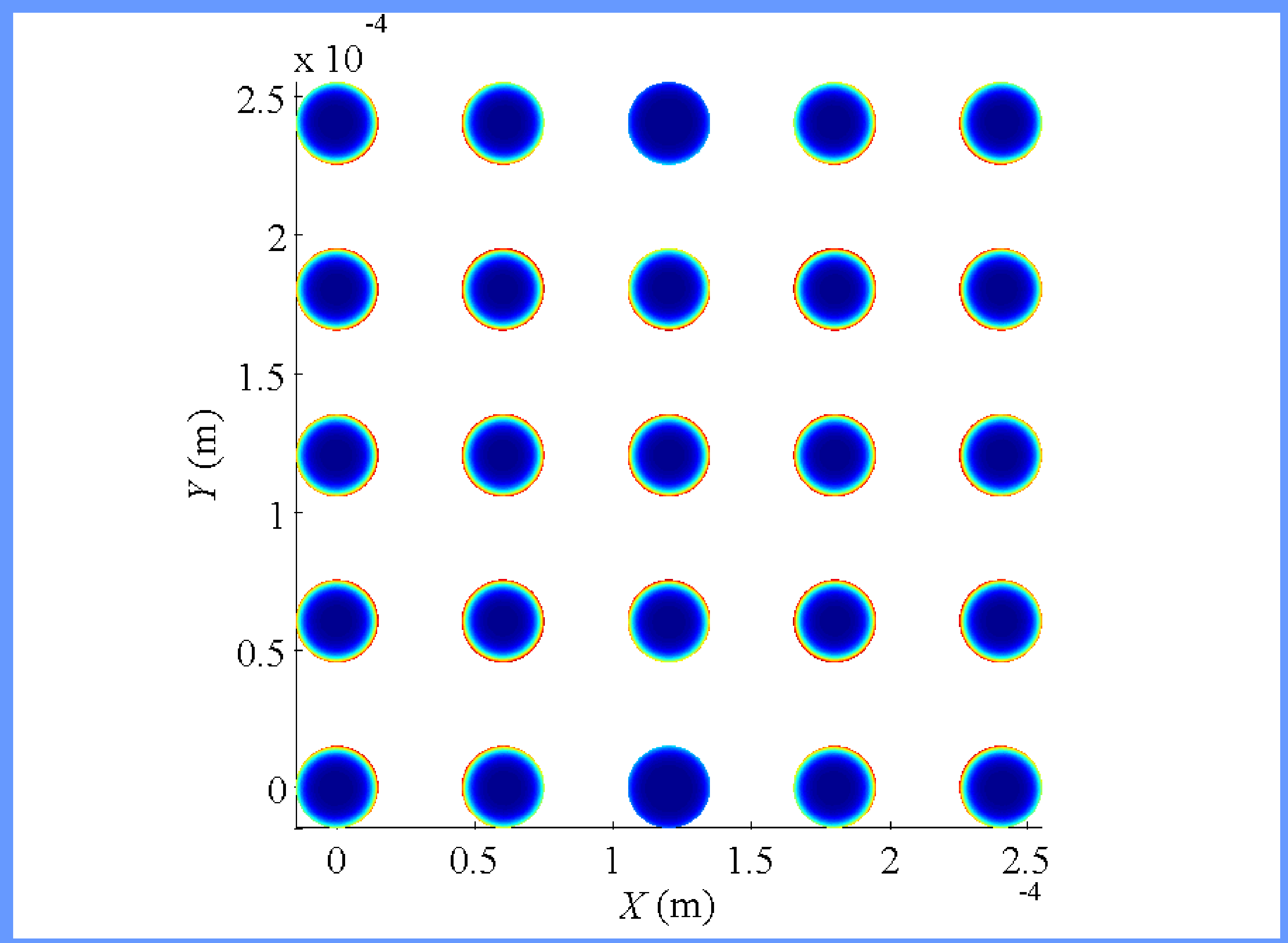
Modeling of Interconnect array

❑Geometry

Diameter : 30 um
Length: 100 um
Pitch: 60 um

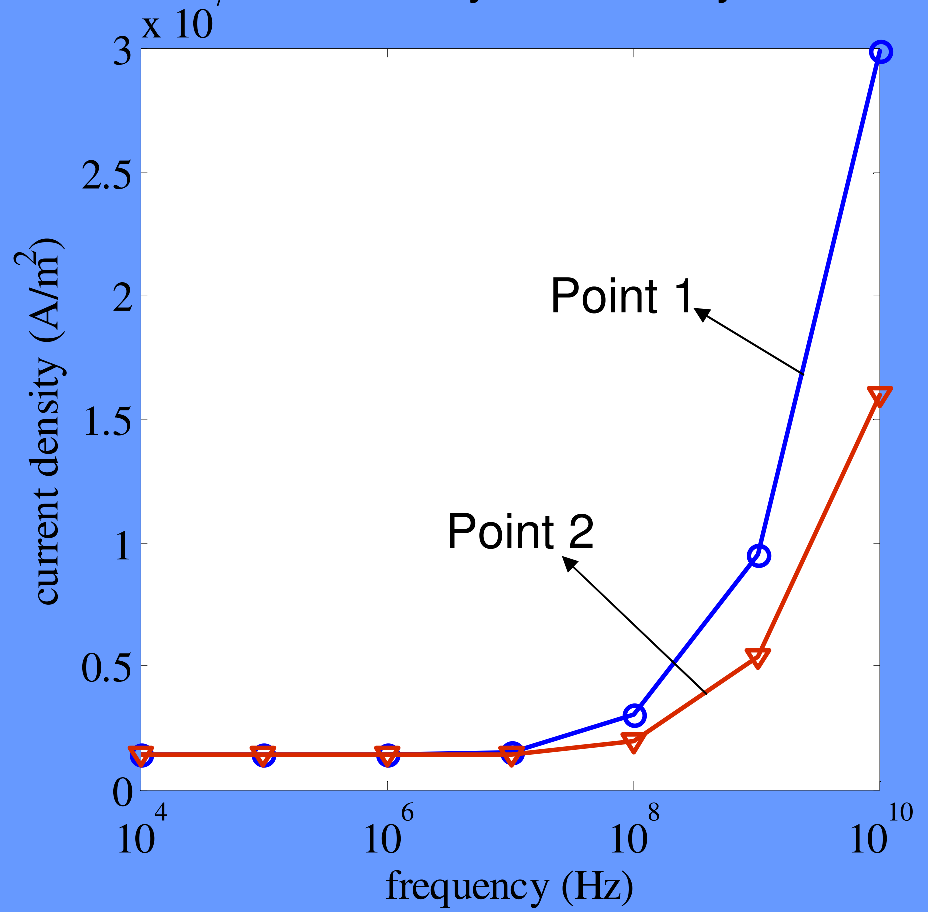


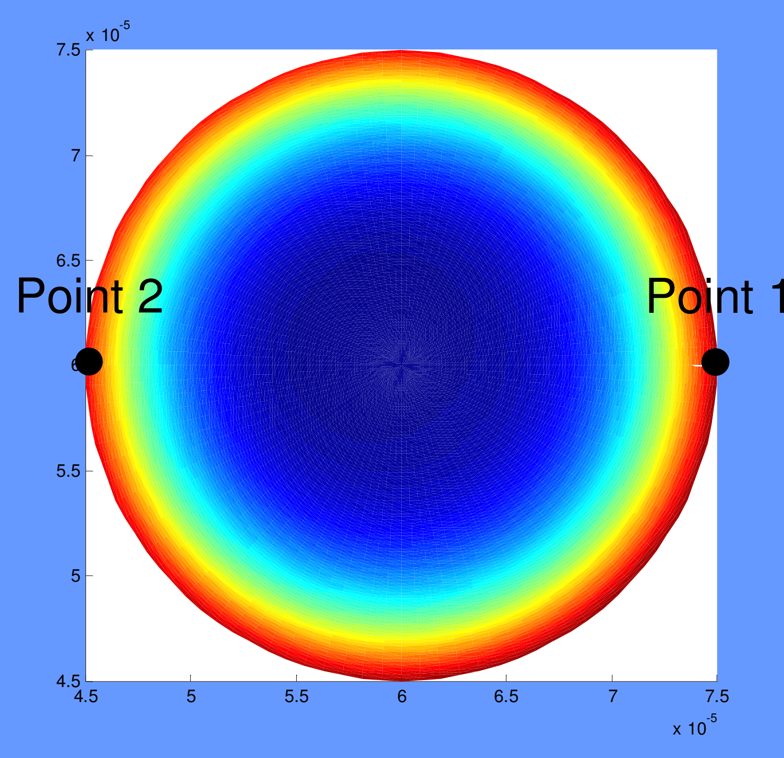
Current density distribution (100 MHz, 1 GHz)



Current Density

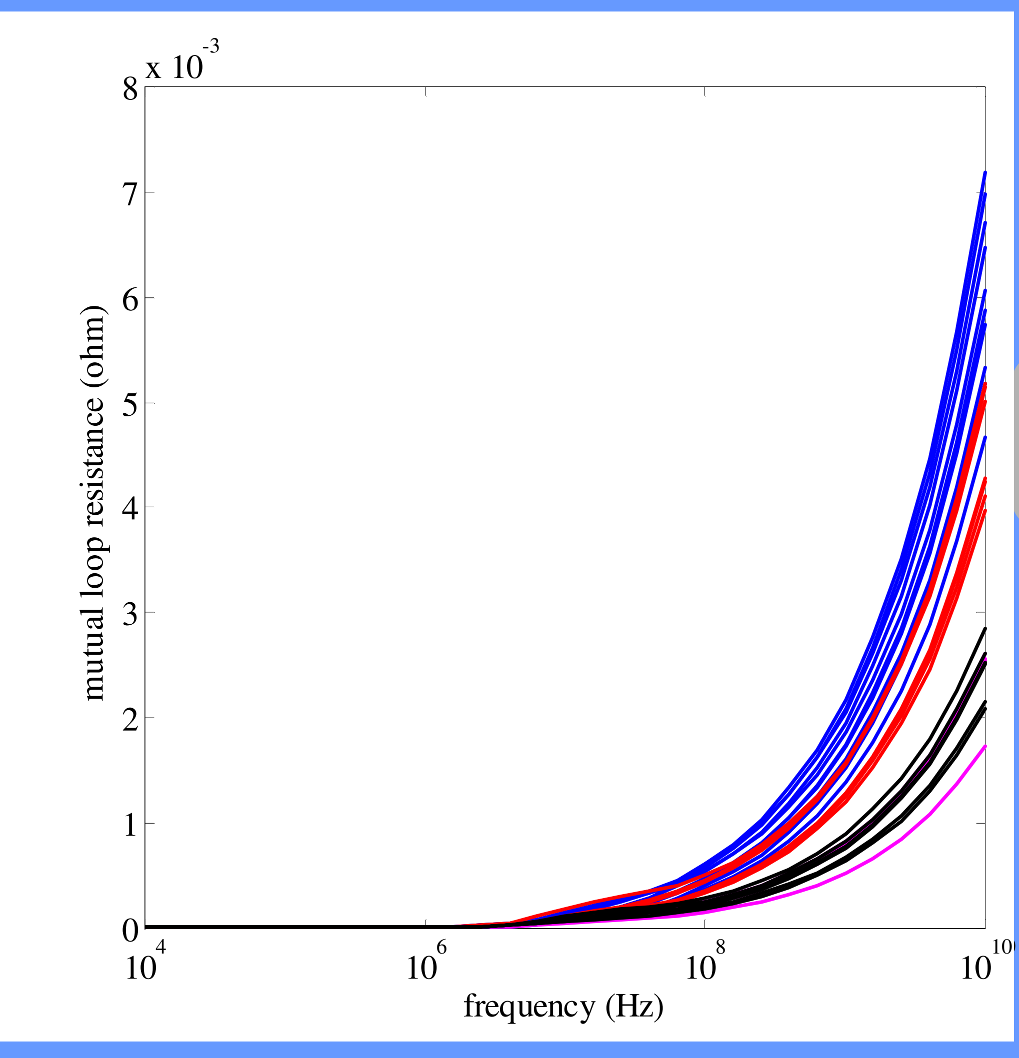
- **Current density increase with frequency**
  - Point 1: affected by skin & proximity effects
  - Point 2: mainly affected by skin effect



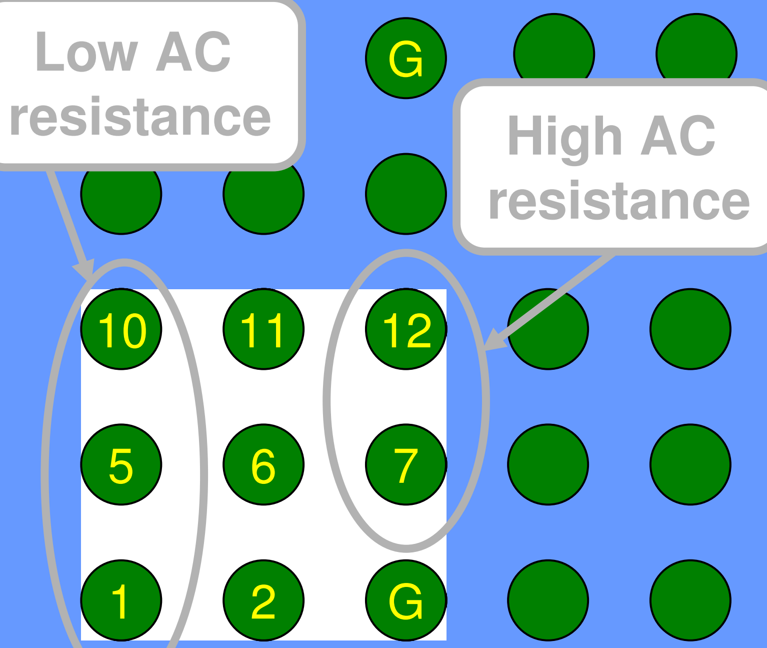


(* under excitation with current source)

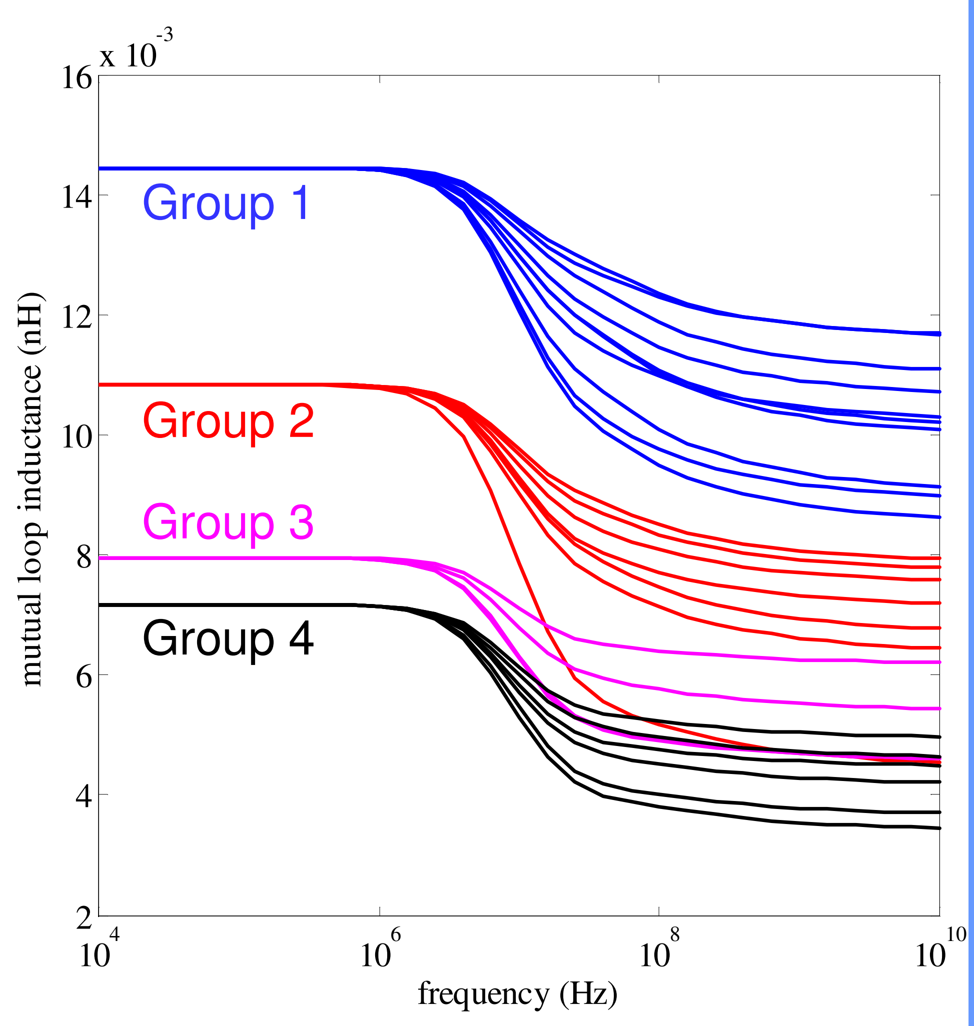
Frequency Dependent Loop Resistance (Self and Mutual)



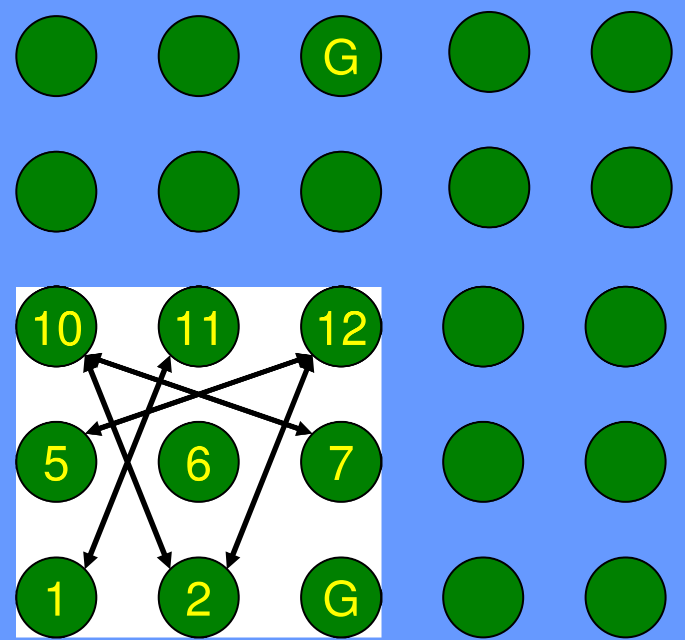
- **Self resistances increase mainly by skin effect, and are modified by proximity effect.**
- **Mutual resistances are zero at low frequencies, but become non-zero and increase at high frequencies.**

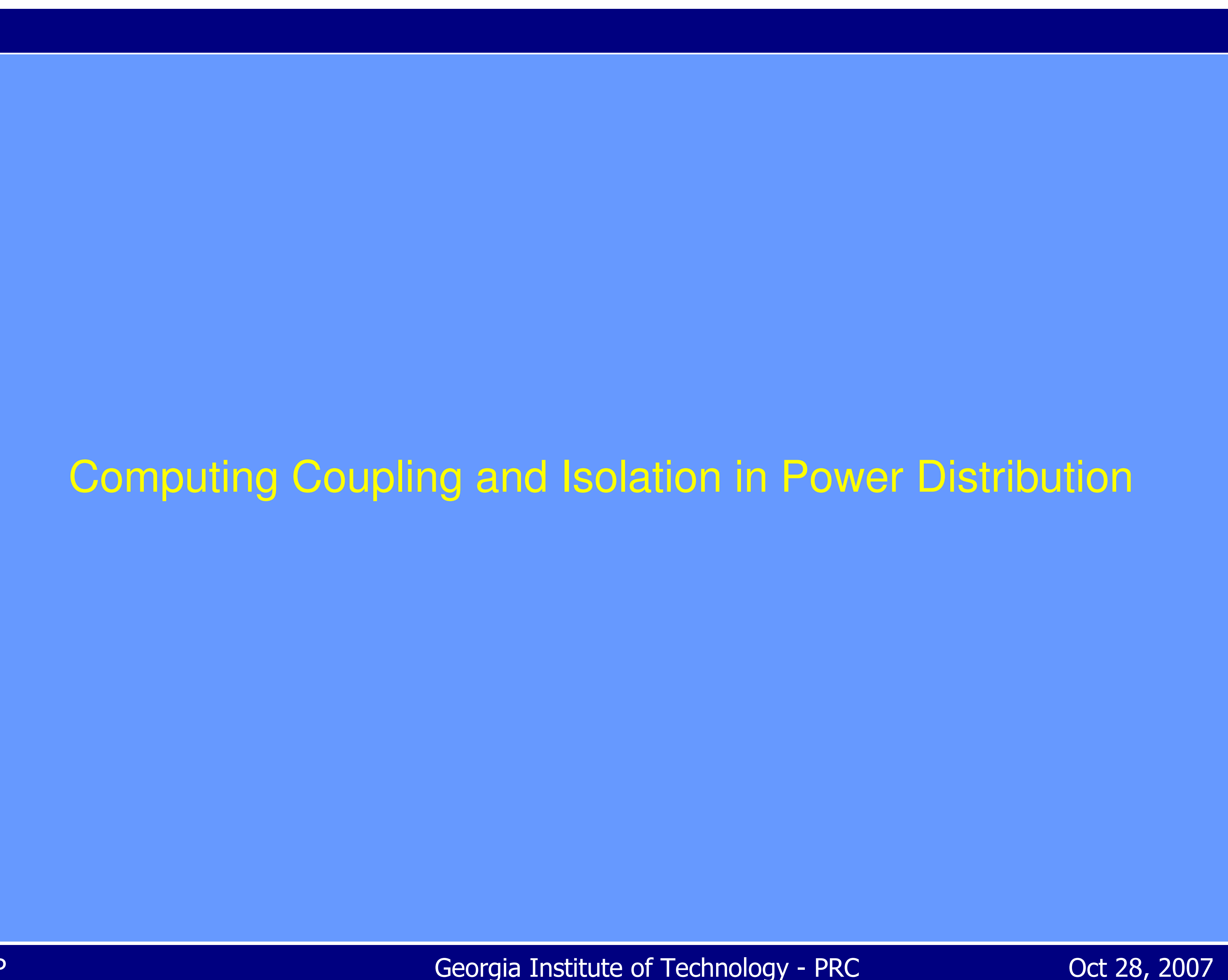


Frequency Dependent Loop Inductance (Self and Mutual)

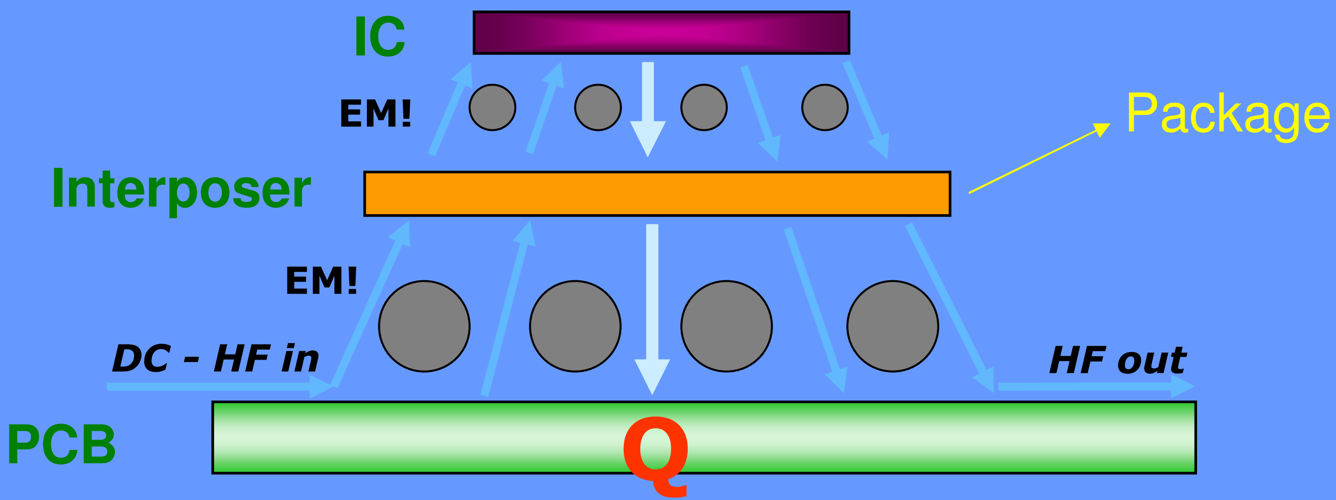


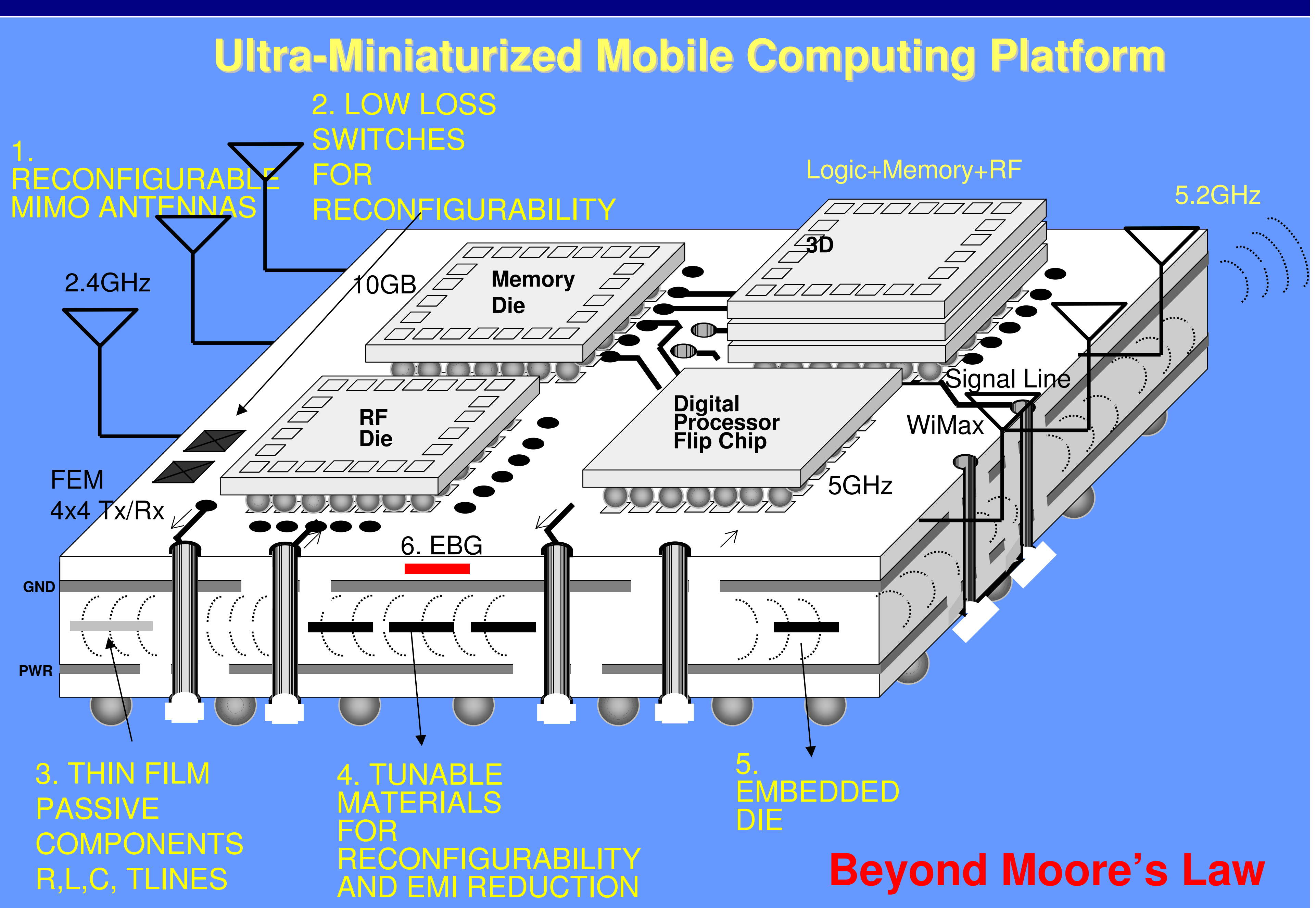
- At low frequencies, all inductances are mainly functions of distance between lines.
- At high frequencies, inductances decrease due to proximity effects.



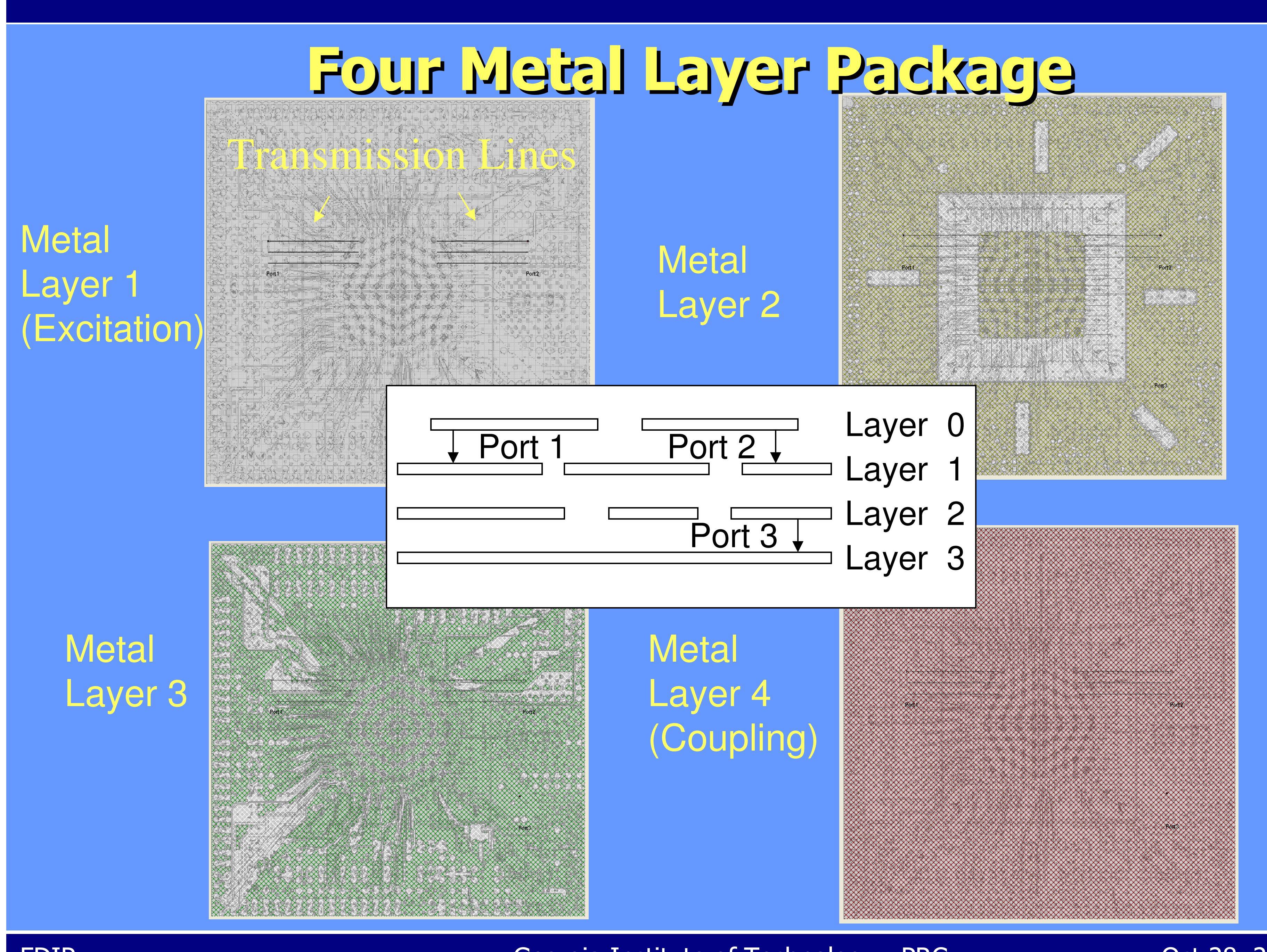

Computing Coupling and Isolation in Power Distribution

Chip on Package on System Board

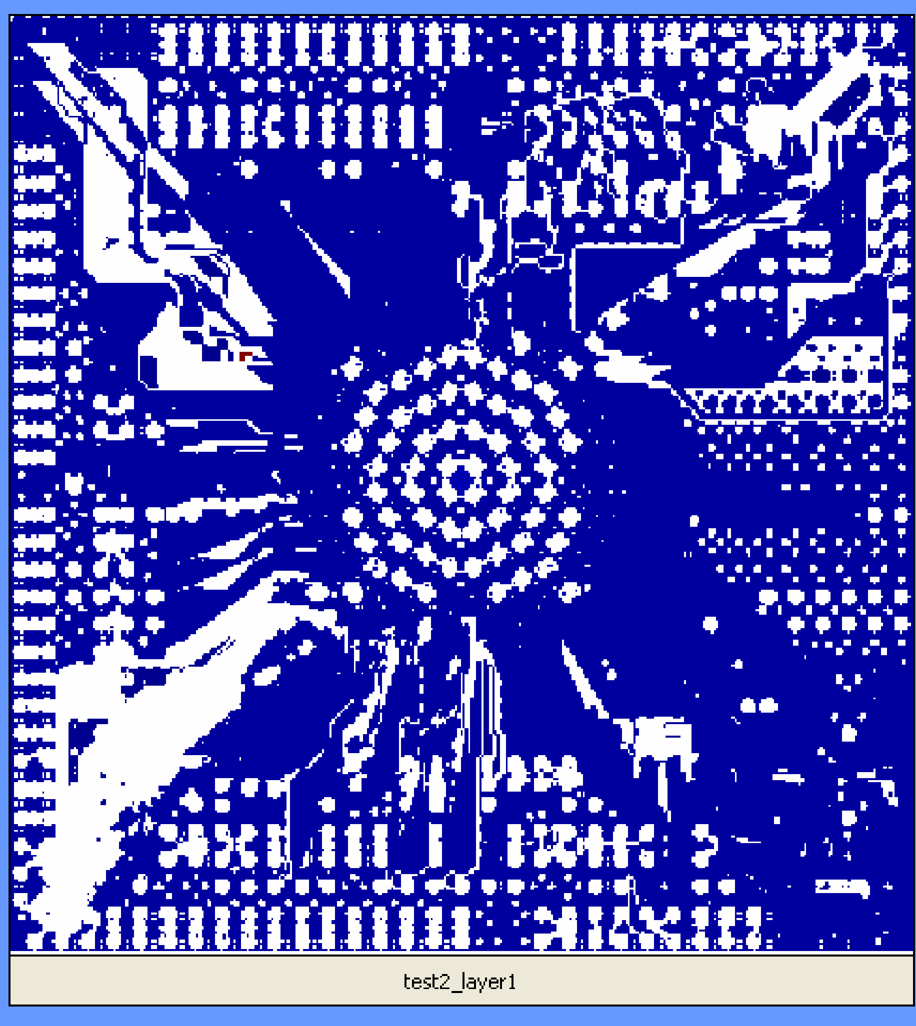



Ultra-Miniaturized Mobile Computing Platform
1. RECONFIGURABLE MIMO ANTENNAS
2. LOW LOSS SWITCHES FOR RECONFIGURABILITY
Logic+Memory+RF
5.2GHz
2.4GHz
10GB
Memory Die
3D
RF Die
Digital Processor Flip Chip
Signal Line
WiMax
5GHz
FEM 4x4 Tx/Rx
6. EBG
GND
PWR
3. THIN FILM PASSIVE COMPONENTS R,L,C, TLINES
4. TUNABLE MATERIALS FOR RECONFIGURABILITY AND EMI REDUCTION
5. EMBEDDED DIE
Beyond Moore's Law

Four Metal Layer Package



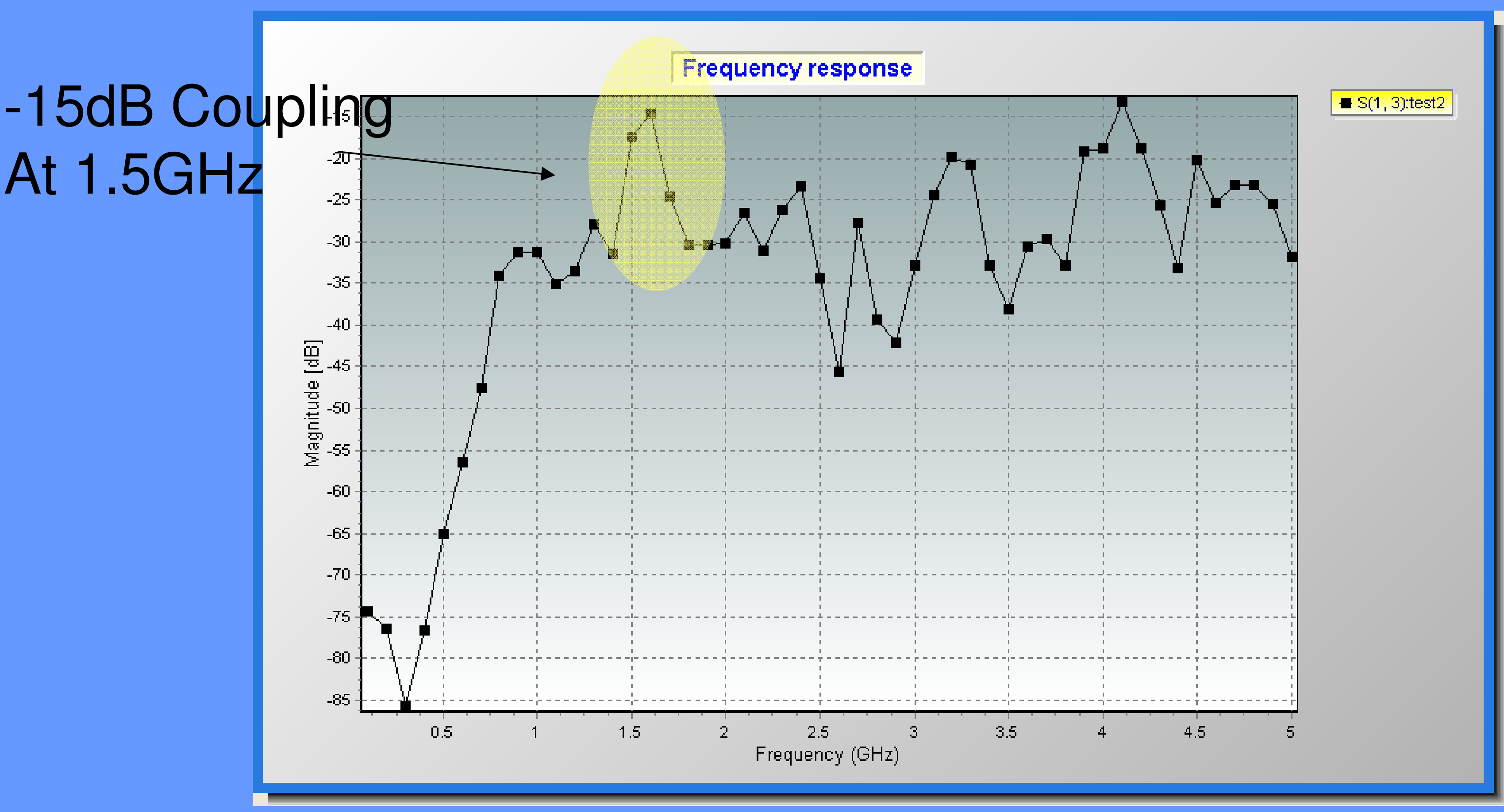
Coupling into Metal Layer 3



Frequency Sweep from 0.1 to 5GHz

Coupling from Top to Bottom Layer

-15dB Coupling
At 1.5GHz



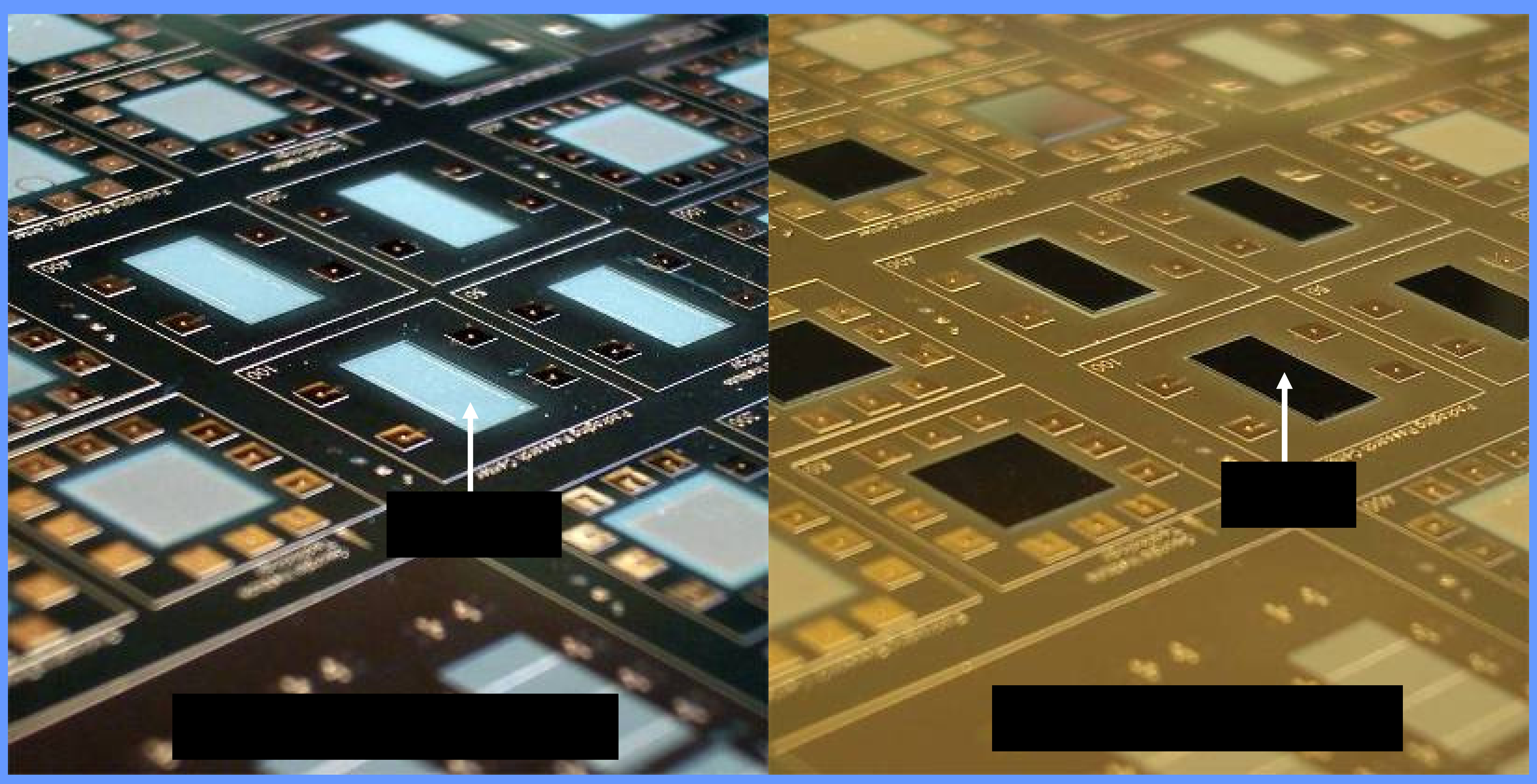
State-of-the-art

	FEM	FDTD	Cavity Resonator	TMM	M-FDM
Arbitrary plane geometries	Yes	Yes	Difficult	Yes	Yes
Arbitrary port locations	Yes	No	Yes	No	No
Calculating noise voltage distribution on each node	Yes	Yes	Difficult	Yes	Yes
Skin effect and substrate losses	Yes	Difficult	Yes	Yes	Yes
Fringe and gap fields	Difficult	Difficult	Difficult	Difficult	Yes
Speed	Good	Good (time domain)	Good for solid rectangular planes	Good	Good
Multilayered planes	Difficult	Difficult	Difficult	Yes (neglects wrap-around currents)	Yes (includes wrap-around currents as well)

Very Important Effect

Ref: Madhavan Swaminathan and Ege Engin, "Power Integrity Modeling and Design for Semiconductors and Systems", Pretice Hall 2007

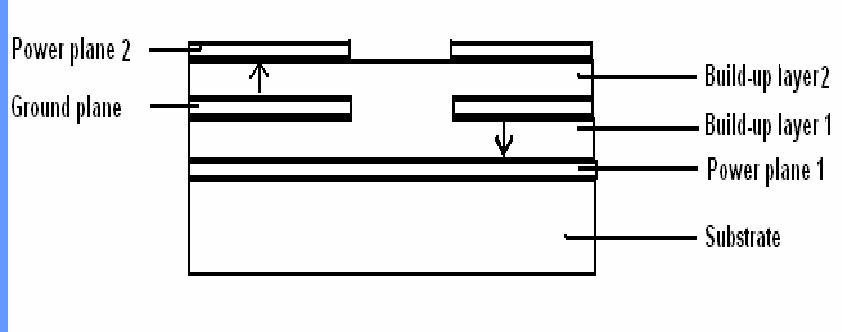
Chip-last Embedded Actives



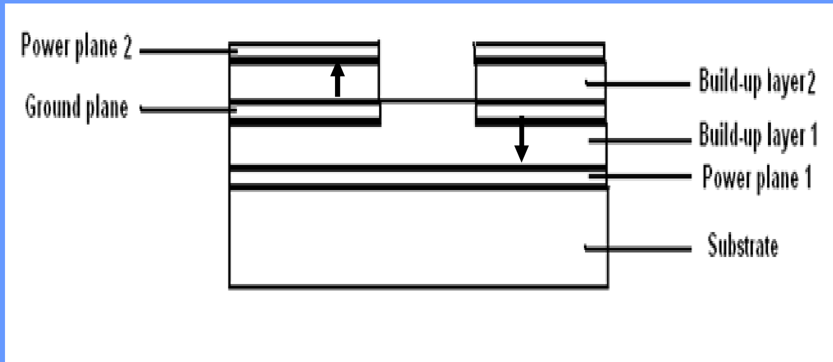
- Cavity size: 4.5×9.0 mm^2 & 7.0×7.0 mm^2
- Cavity depth: 130 um
- 100 um thick chips are embedded with solder bumps

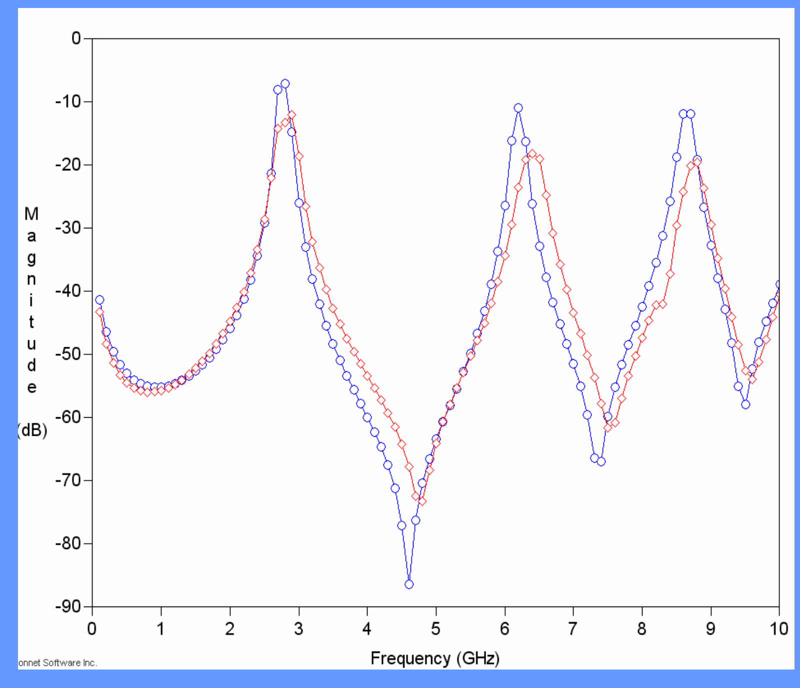
Coupling through Cavities

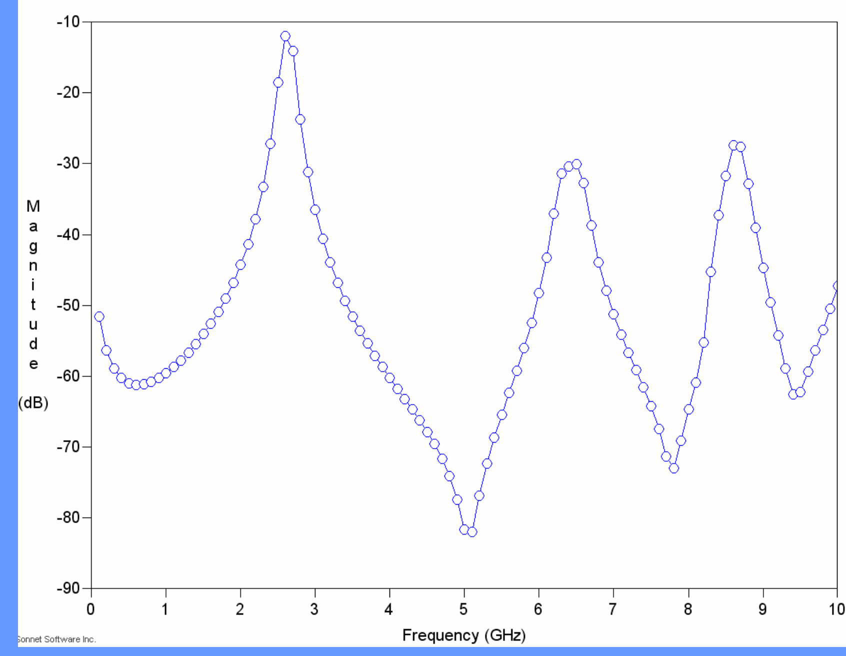
Without Cavity



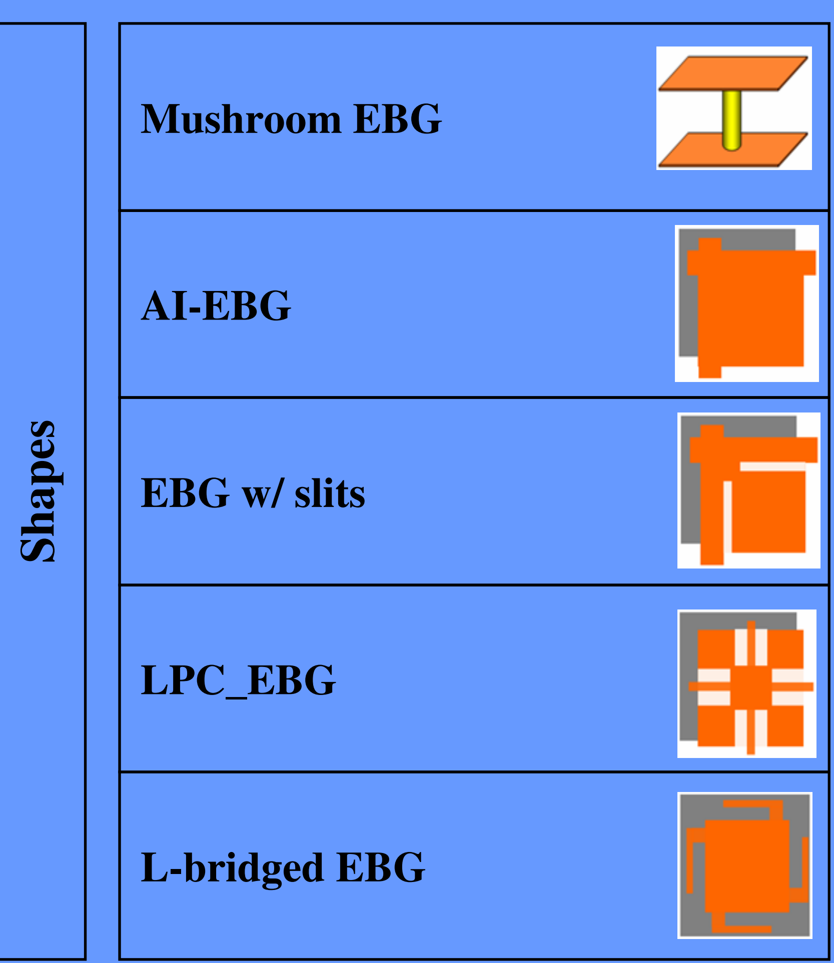
With Cavity

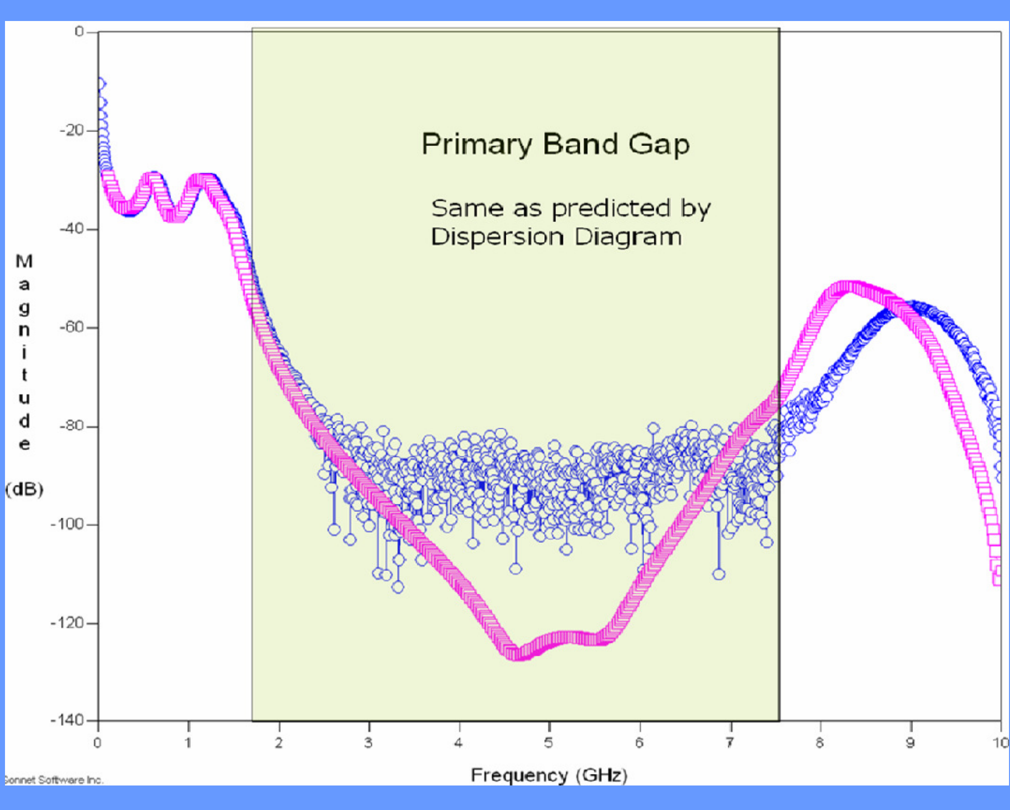




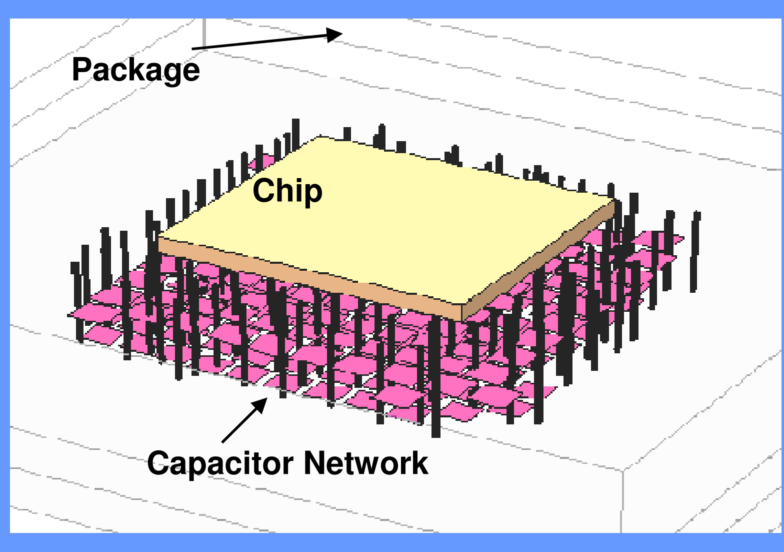


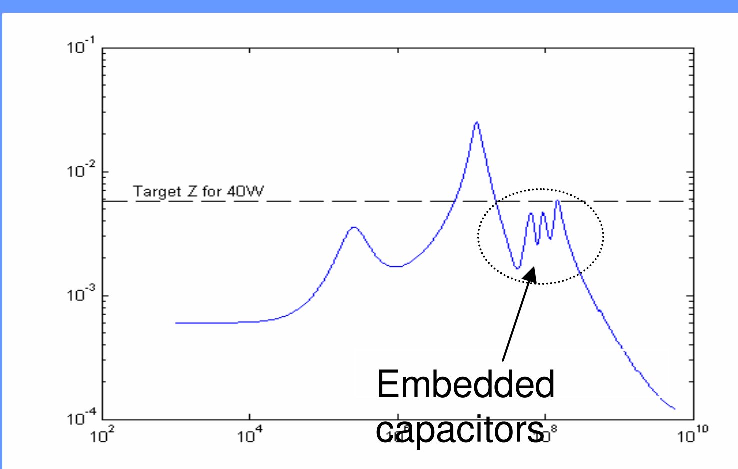
Embedded EBG Structures
Modeling of fine and large metal structures

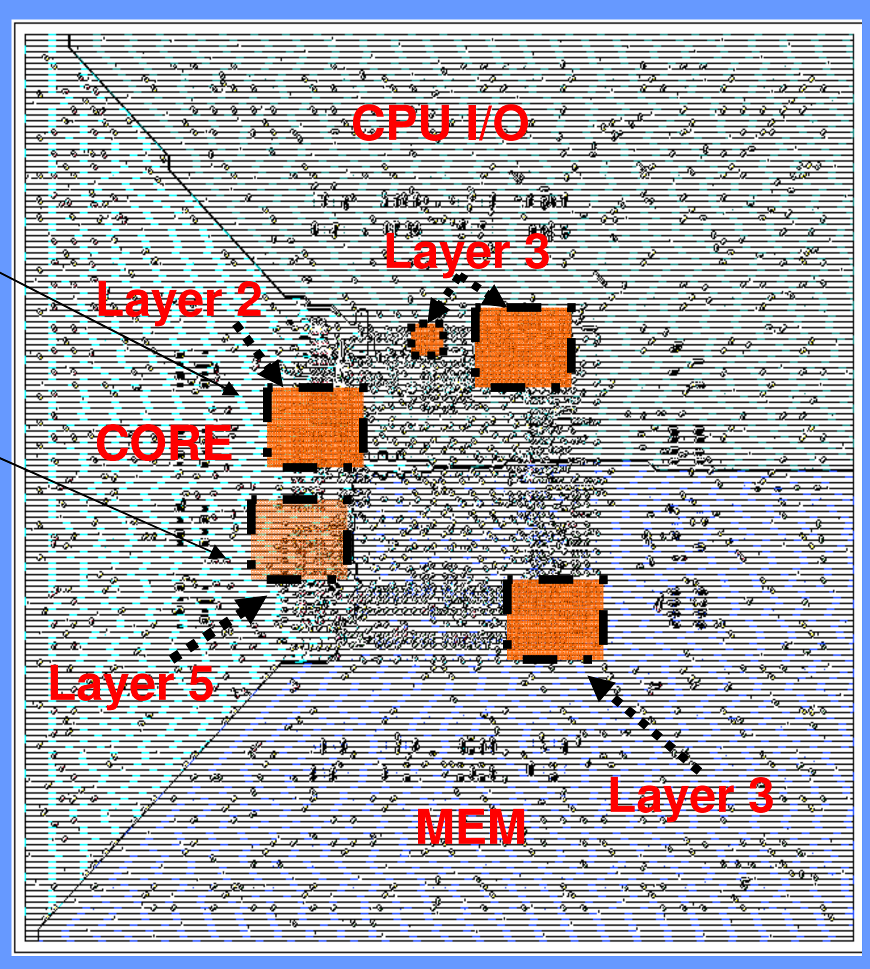




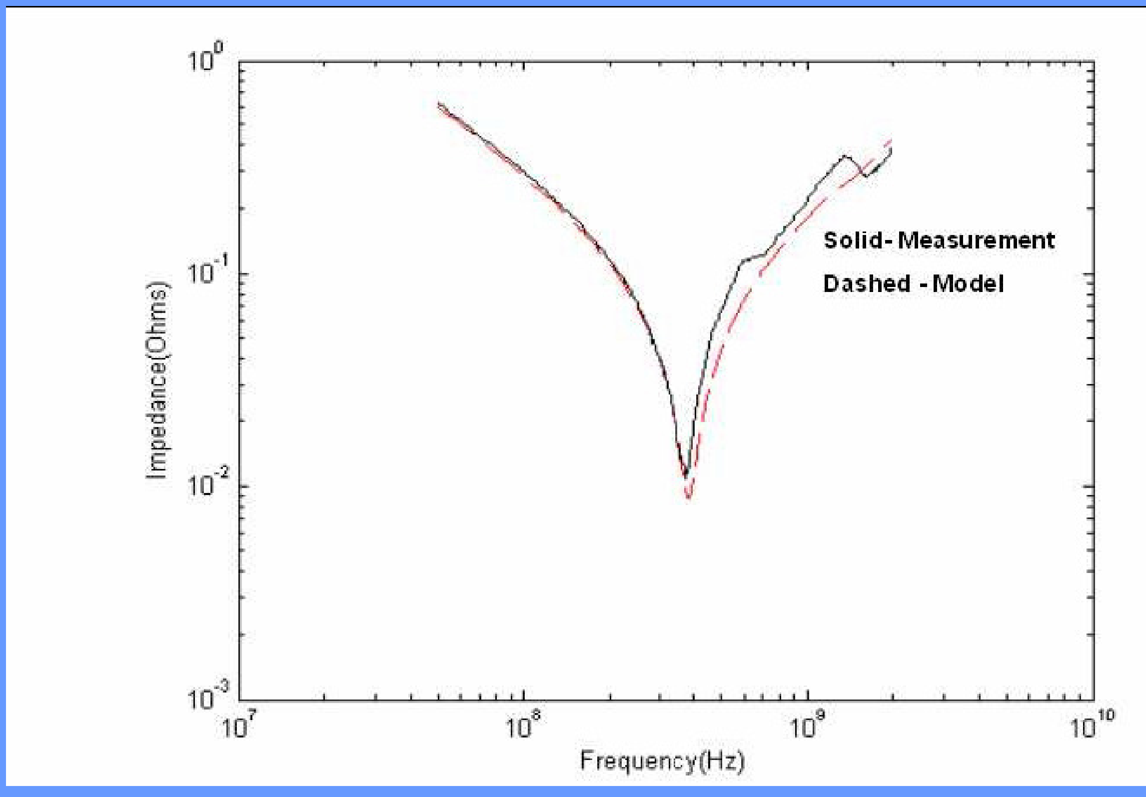
Embedded Decoupling in Package







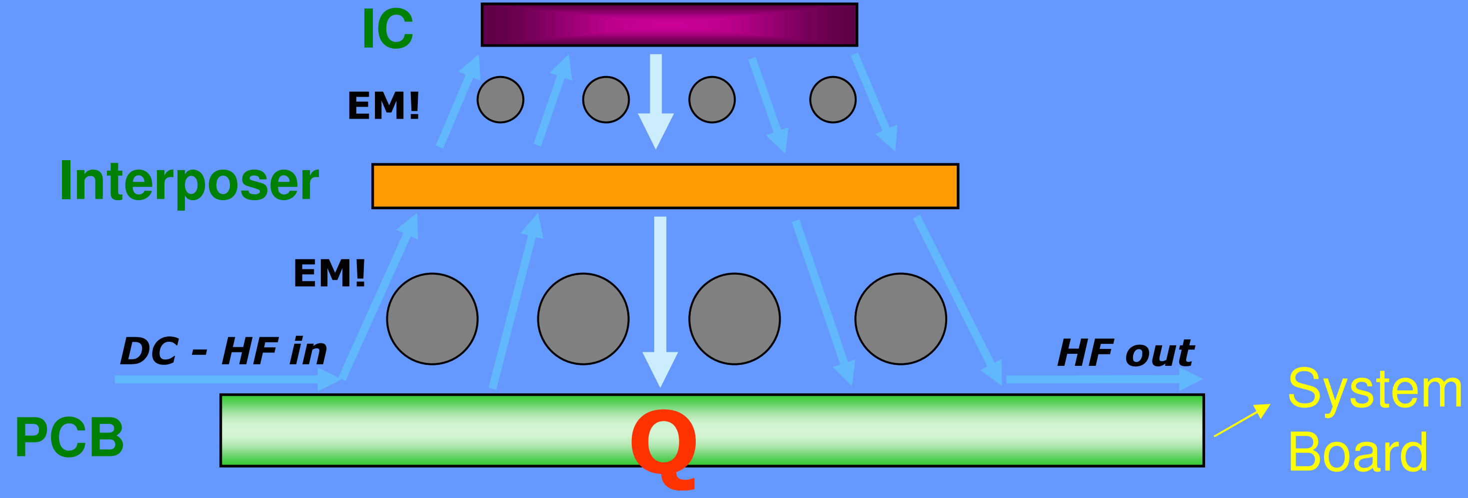
Embedded Capacitors



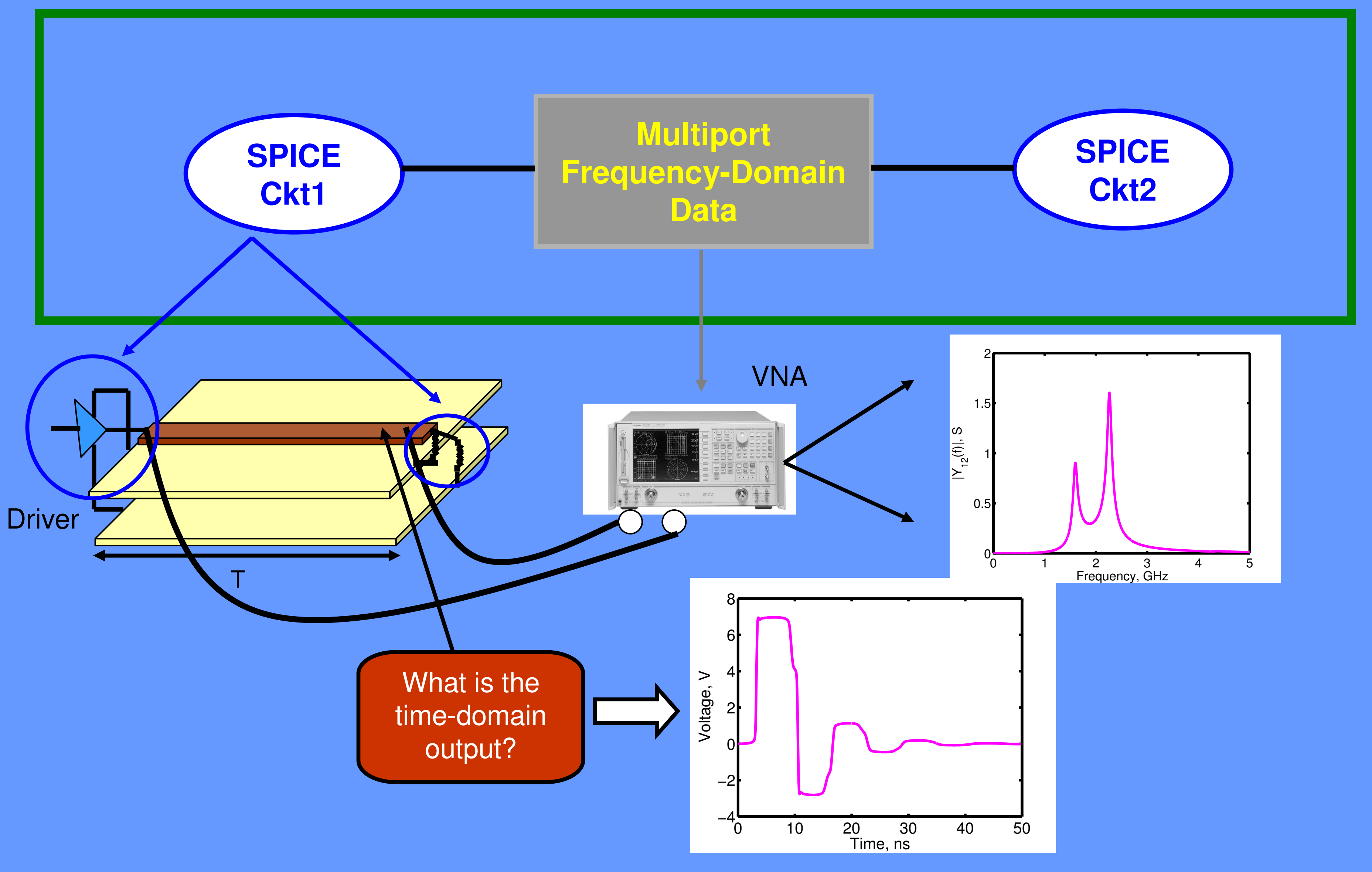
Capacitor Size(mm×mm)	ESC(nF)	ESL(pH)	ESR(mohms)
1.198×1.198	2.84	42.6	16
2×2	8.772	23.8	10.36

Frequency to Time Conversion for Managing Eye and Jitter

Chip on Package on System Board



Transient Simulation with Band-Limited Data



Frequency to Time Conversion

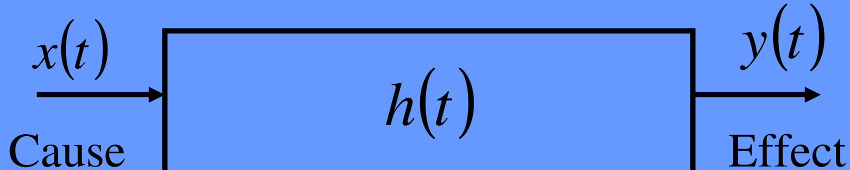
Focus of this presentation

Method	Ports	Stability	Passivity	Causality	Convolution	Problem Type	Robustness
Rational Function	Limited	Yes	Yes	No	O(MN)	Arbitrary	Medium
Signal Flow Graph	Unlimited	Yes	Yes	Yes	O(NlogN)	Distributed networks	Medium
MNA+S-Parameter	Unlimited	Yes	Yes	Yes	O(NlogN)	Distributed networks	High

Beaten to death at EPEP

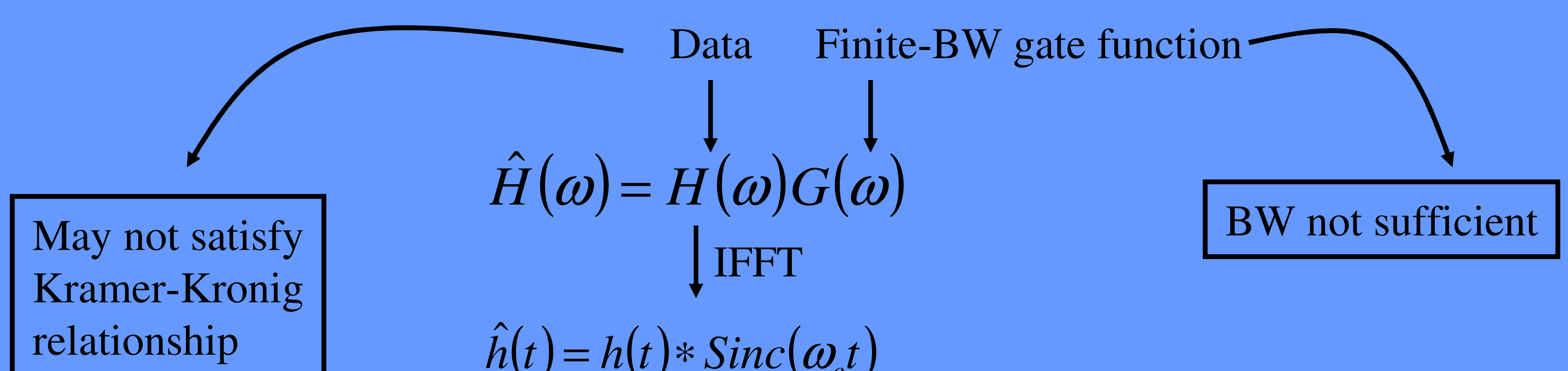
Ref: Madhavan Swaminathan and Ege Engin, "Power Integrity Modeling and Design for Semiconductors and Systems", Pretice Hall 2007

Causality and Its Importance

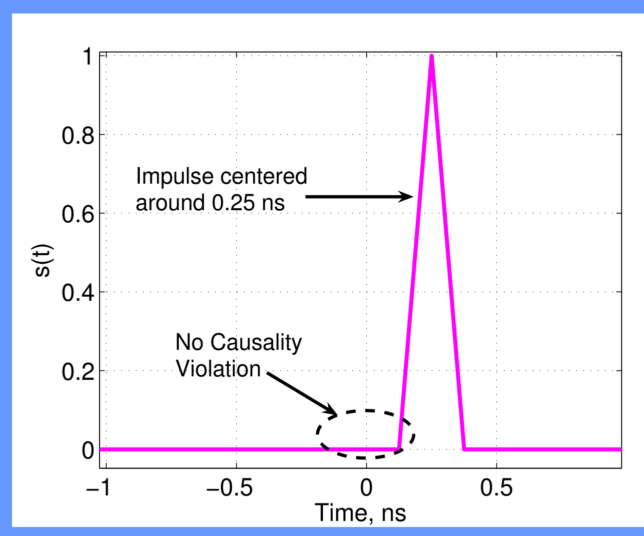


Effect cannot precede the cause

Origin of Noncausality



Propagation Delay = 0.25 ns



Analytical s(t)

BW = 5 GHz

Centered around 0.25 ns

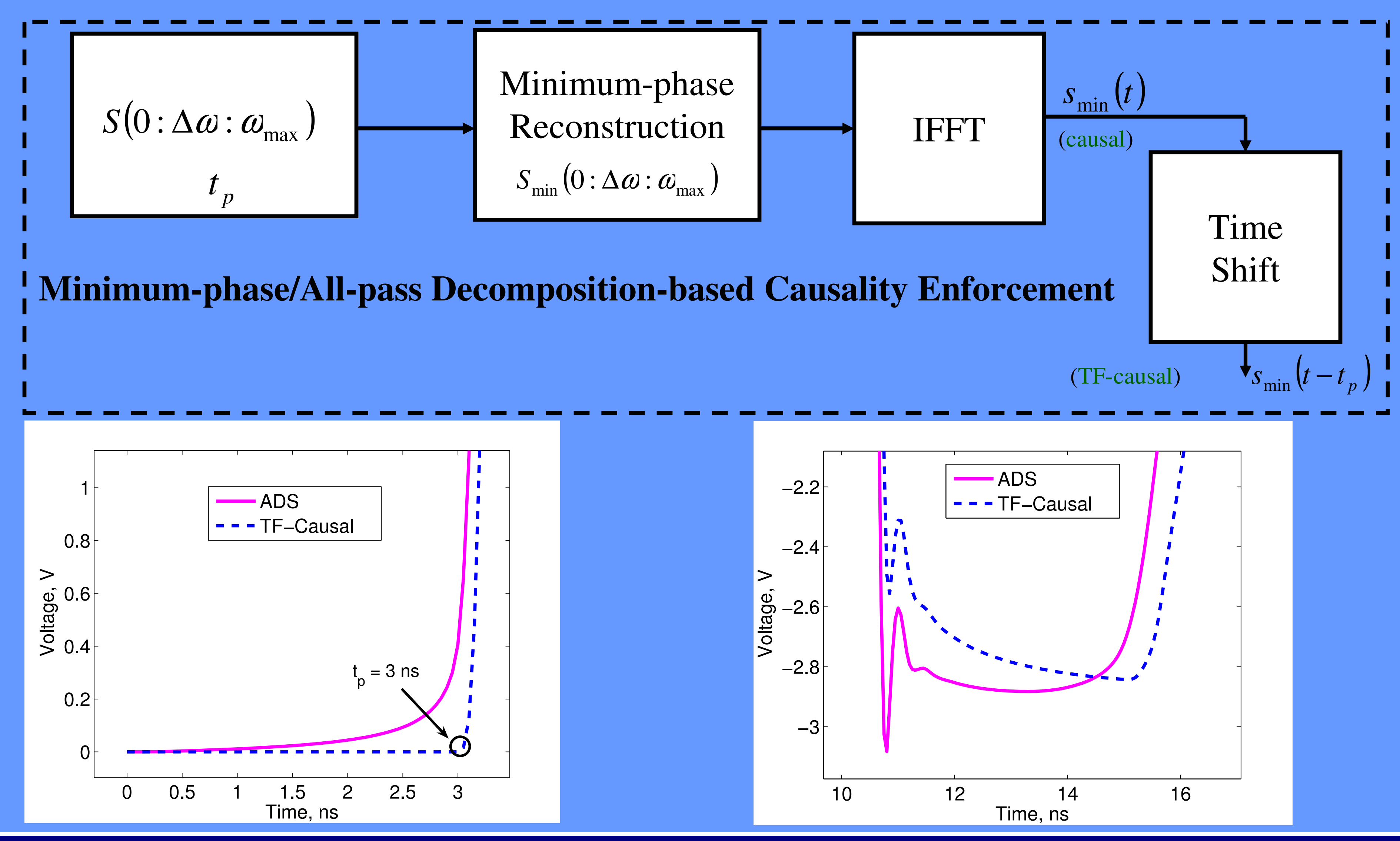
Causality Violation

s(t)

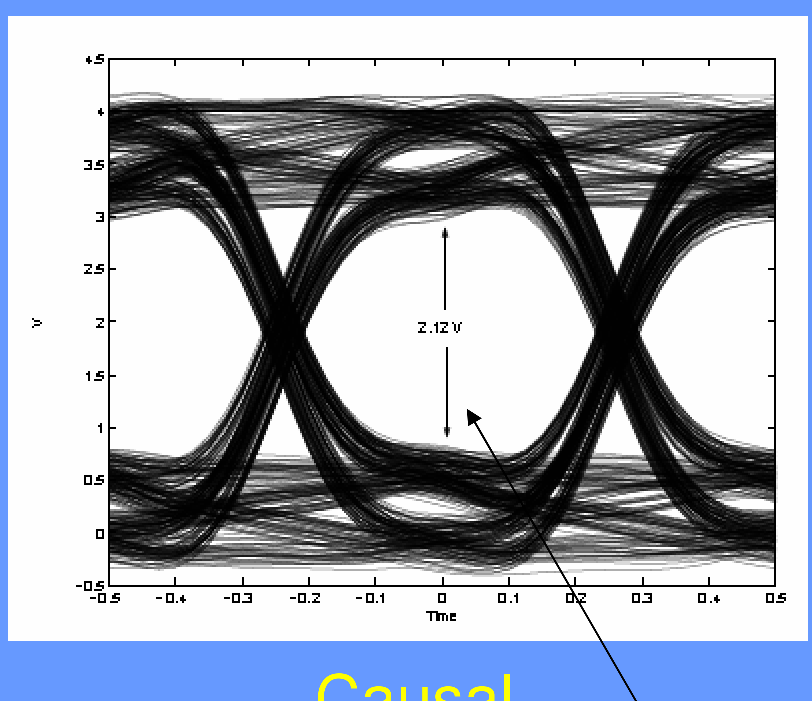
Time, ns

s(t) with band-limited data

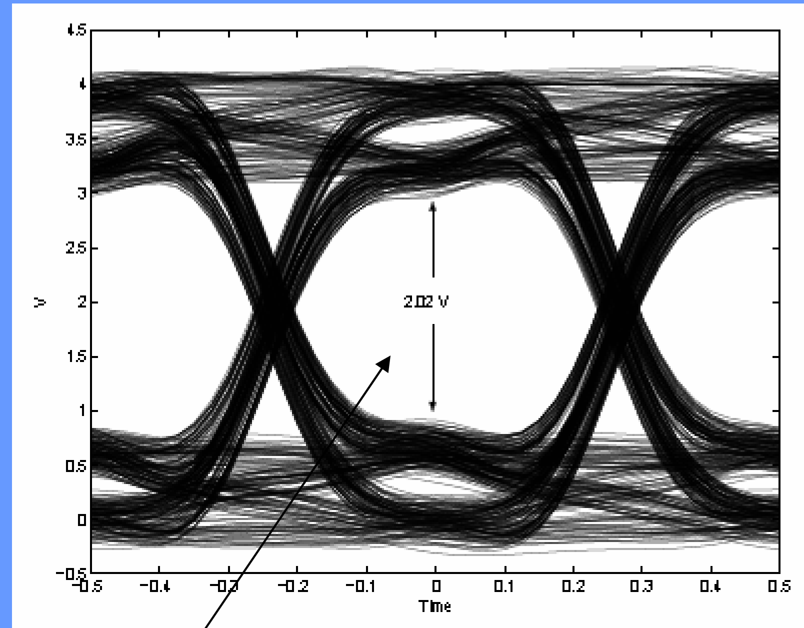
Causality Enforcement Techniques



Causal Vs Non-Causal Simulation



Causal



Non-Causal

100 mV difference in Eye Opening

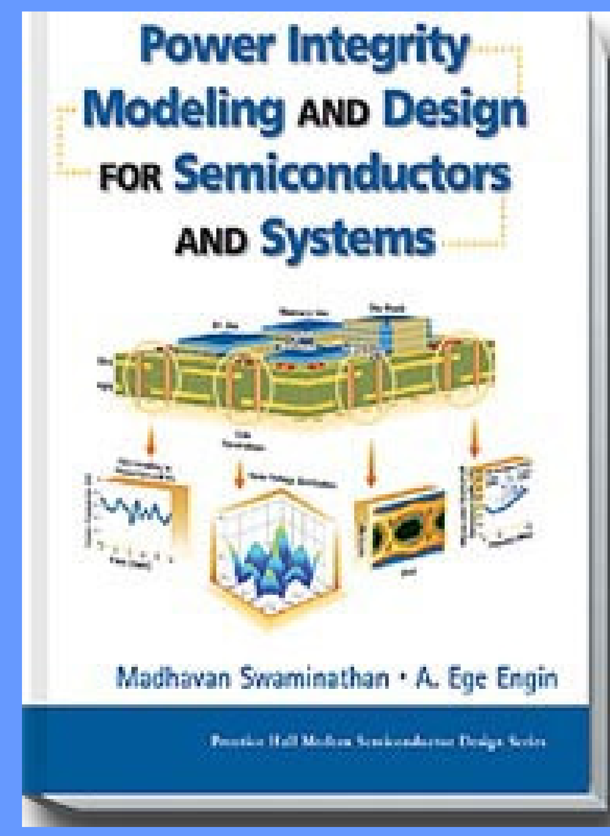
Book on Power Integrity

The First Book on Power Integrity Modeling!

FOR MORE INFORMATION

PLEASE VISIT: www.prenhallprofessional.com/title/0136152066

Availability: Nov ‘07



ISBN: 0_13_615206_6

- Chapters
  - Basic Concepts
  - Plane Modeling
  - Simultaneous Switching Noise
  - Time Domain Simulation Methods
  - Applications
- Provides a comprehensive discussion of the methods available for Power Integrity Modeling
- Contains several examples that can be reproduced using the provided software